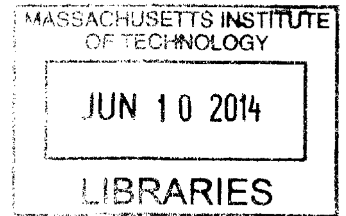
Nano-scale Ohmic Contacts for III-V MOSFETs



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Nano-scale Ohmic Contacts for III-V MOSFETs

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Master of Science in Electrical Engineering

ABSTRACT

As modern silicon CMOS has been scaled down to extremely small dimensions, there is an urgent need for technological innovations of new devices architectures that would allow the continuation of Moore's Law into the future. In particular, for CMOS with nanometer scale pitch size, the intrinsic electronic properties of silicon as channel material represent a significant hindrance to further scaling. As a result, new channel materials are being investigated all over the world that would enable the push into the sub-10 nm regime. Among them, certain III-V compound semiconductors have emerged as the most promising candidates to replace silicon in future generations of CMOS. In particular and as a result of their extraordinary electron or hole transport properties, InGaAs, InAs, and InGaSb enable transistors with faster operation at a lower power consumption. This is the key to enable future scaling.

One of the major challenges of extremely-scaled III-V logic MOSFETs is the series resistance. To achieve the performance goals, it is necessary to fabricate source and drain ohmic contacts with ultra-low contact resistance, perhaps as low as 50 $\Omega\cdot\mu m$. This is particularly difficult to achieve as the device size shrinks down to the 10-20 nm length range since the contact resistance increases drastically for small contact lengths. Moreover, it is not clearly known how to characterize nano-scale metal-semiconductor ohmic contacts. All available test structures and models, such as the transmission line model (TLM), are designed for relatively large ohmic contacts, on the order of micrometers, and are unable to make accurate measurements of extremely small contact resistance.

To deal with nano-scale contacts for III-V CMOS, we need a more accurate test structure capable of extracting extremely small values of contact resistance on very small contacts. In this thesis, a novel test structure, nano-TLM, is developed to address this issue. We demonstrate how the nano-TLM is capable of providing accurate measurements of the contact resistance, metal resistance, and semiconductor resistance of an ohmic contact system at the same time. We demonstrate this new technique in Mo/n^+-InGaAs ohmic contacts where we have achieved an extremely low contact resistance of 32.5 $\Omega\cdot\mu m$ with contact length as small as 19 nm. This contact resistance at this contact length is, to the best of our knowledge, the lowest reported value to date. Our proposed new test structure will help understand and characterize ohmic contacts suitable for future III-V CMOS device fabrication.

Thesis supervisor: Jesús A. del Alamo
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The first two years of graduate student experience at MIT is full of mixed-feelings. Started with excitement and ambition, I experienced times of anxiety and frustration, also happiness and pride (when things work). I was humbled to realize that doing research needs to be based on the desire of understanding God's creation, instead of a pursuit of recognition and approval from people. I am deeply grateful to my mentor, Dr. Liu Ce, who not only gives me advises in my study, but also teaches me word of God.

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CHAPTER 1. INTRODUCTION

1.1 Introduction to III-V MOSFETs

For fifty years, the world has witnessed an incredible revolution in the microelectronic industry. Driven by Moore's law, the silicon complementary-metal-oxide-semiconductor (CMOS) technology has kept making progress at an exponential pace. Inevitable fundamental limits appear to be getting closer. Suffering from leakage currents and short-channel effects, silicon may no longer be able to sustain the scaling trend as the gate length is about to reach 10 nm and below [1]. Besides new technologies, such as multigate transistors [2], that are being developed to mitigate short-channel effects, new materials are also needed to maintain enough performance in a future reduced voltage scenario. In the last few years, III-V compound semiconductors, such as InAs or InGaAs, have emerged as one of the most promising family of materials to replace silicon in the channel [3], [4]. Novel III-V metal-oxide-semiconductor field-effect transistor (MOSFET) prototypes with superior electronic characteristics have been recently demonstrated [5], [6]. It is promising that III-V compound semiconductor devices, such as the InGaAs MOSFET, can succeed Si in sub-10 nm CMOS nodes, and it is anticipated that III-V channel MOSFETs might be introduced in manufacturing as early as 2015, according to the International Roadmap for Semiconductors (ITRS) [7].

Despite the remarkable progress in III-V MOSFET technology, there are still a number of major challenges that need to be solved. First of all, it is critical to achieve a high-k/III-V MOS gate stack with excellent interfacial quality. Now commonly prepared by atomic layer deposition (ALD) [8], the high-k dielectric needs to be deposited with minimum interface state density and ultra-low equivalent oxide thickness (EOT). Test structures such as sidewall capacitors are also

needed in order to characterize interface quality in unconventional device architectures. Secondly, while the n-type InGaAs MOSFET has enjoyed notable success, the demonstration of a good p-type counterpart is lacking. Great efforts are required to match the imbalance between NMOS and PMOS, because hole-based devices tend to have lower performance [3]. Germanium and antimony-based materials are currently the most viable candidates. Last but not least, the contact resistance (R_c) is a major limiting factor in logic transistors. As device footprints keep shrinking, it is more and more difficult to maintain low R_c. Addressing this problem is the goal of this thesis. In this study, we will specifically explore metal-III-V semiconductor ohmic contacts and we will introduce a novel test structure to characterize such contacts in the nanometer regime [9].

1.2 Motivation

1.2.1 Ohmic Contact Scaling

The scaling of ohmic contacts in CMOS devices is better described in two aspects: (1) contact length scaling, and (2) contact resistance scaling. As the gate length of transistors gets smaller and smaller, their logic characteristics improve. To coordinate with the gate length scaling, at the insertion point, III-V logic transistors must have contacts in the 10-15 nm length range. According to the ITRS [7], the half-pitch of logic CMOS will be 19 nm and 13 nm in 2015 and 2018, respectively. Here, half-pitch, or metal-1 half pitch, is defined as half of the distance between the first metal layers of two adjacent transistors, as shown in Figure 1-1. Such an aggressive scaling trend demands the contact length to be scaled down to an even smaller dimension.

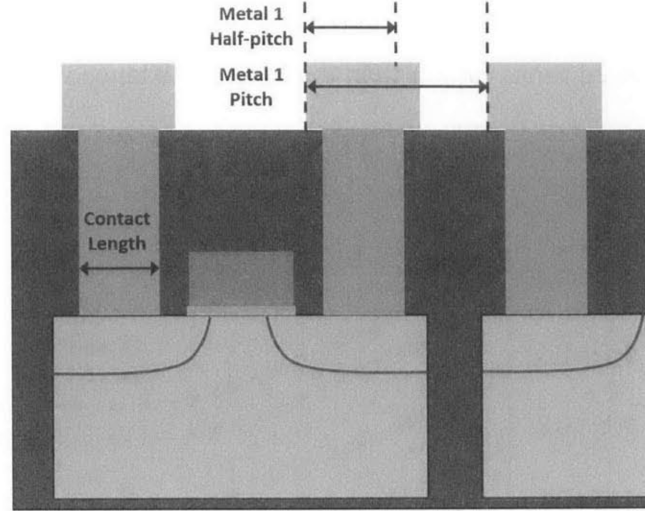


Figure 1-1. Transistor dimension definition, reproduced from ITRS, 2012 [7]. The pitch size is defined as the distance between the metal-1 layers of two transistors. The half-pitch is to be scaled to 13 nm in 2018.

While the length of metal contacts is targeted to below 15 nm, it is necessary to deliver a total source resistance of 50 Ω·μm to keep the scaling trend of III-V logic transistors [3], [7]. To meet this goal, the metal to semiconductor contact resistivity, ρ_c, needs to be lower than 0.5 $\Omega\cdot\mu m^2$. Low values of ρ_c for contacts on n^+-InGaAs between 0.4 and 3.2 Ω·μm2 has been reported [10]–[13]. However, as the dimension of the metal contacts shrinks, the contact resistance increases in a reciprocal fashion. This can be seen from the equation that gives the contact resistance of a metal contact to a thin semiconductor layer:

$$R_c = \sqrt{R_{sh} \cdot \rho_c} \coth(L_c\sqrt{R_{sh}/\rho_c}) \tag{1}$$

R_c (Ω·μm) is the normalized contact resistance, R_{sh} (Ω/□) is the semiconductor sheet resistance, and ρ_c ($\Omega\cdot\mu m^2$) is the contact resistivity, and L_c is the contact length. All things being equal, as the contact length L_c approaches zero, (1) can be approximated to the first order by:

$$R_c \approx \rho_c/L_c \tag{2}$$

Therefore, the contact resistance shoots up while the contact length decreases. Figure 1-2 demonstrates the effect of contact-length scaling on R_c for n-type InGaAs high-electron-mobility

transistors (HEMTs). It is shown that with current technology for HEMT contacts, the contact resistance is still one hundred times higher than the target resistance when L_c is scaled to 10 nm.

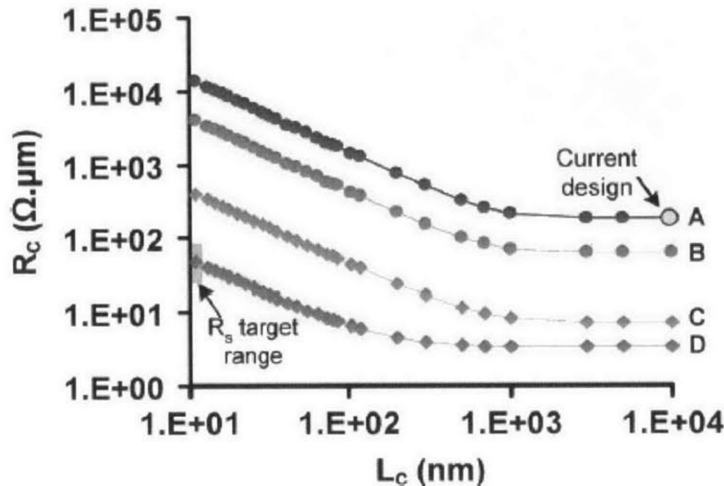


Figure 1-2. Effect of contact-length scaling on R_c for InGaAs HEMT, predicted using tri-layer transmission line model. Fig from N. Waldron [14].

In this study, we attempt to improve the contact resistance in three approaches: (1) we use a metal-first process to minimize surface contamination, (2) we use Mo, a refractory metal, as the contact metal to minimize metal diffusion and achieve high thermal stability, and (3) we use a dry etch process instead of a lift-off one to obtain nanometer-scale contacts. We also achieved extremely thin metal contacts by using electron-beam lithography. More fabrication details will be discussed in Chapter 3. Meanwhile, it is necessary to investigate metal contacts on both n-type and p-type III-V materials.

1.2.2 Need for Contacts for Both N and P-type MOSFETs

The success of modern CMOS is not possible without the matched performance of both n-type and p-type MOSFETs. However, similar to the case in Si, the performance of p-type transistors tends to be inferior to that of n-type [3], because holes generally have higher effective mass than electrons. This has long been a serious issue dragging progress on III-V CMOS. Recently, novel

device prototypes of InGaAs n-MOSFET with excellent performance have been demonstrated [15]. Ohmic contacts to n^+-InGaAs with contact resistivity from 0.4 to 3.2 $\Omega \cdot \mu m^2$ have also been reported. On the other hand, p-type MOSFETs with comparable characteristics are still lacking. Ohmic contacts to p-type III-V semiconductors are overall rather poor as well. Therefore, it is one of the goals of this thesis to investigate and compare ohmic contacts to both n-type and p-type III-V materials.

1.3 A Test Structure to Characterize Nano-scale Ohmic Contacts

As described previously in section 1.2.1, ohmic contact resistance blows up as the contact size scales down. Therefore, this reveals that inherently there is a problem with the direct characterization of nanometer-scale ohmic contacts. Until now, test structures to extract contact resistance are mostly on the scale of several tens of micrometers, and related models are based on the assumption of a large contact area. Widely-used methods, such as the transmission line model (TLM) and cross-bridge Kelvin resistance (CBKR), cannot be applied straightforwardly in the nanometer regime. Therefore, based on the TLM, we have designed a new "nano-TLM" test structure to characterize nano-scale ohmic contacts accurately.

1.4 Thesis Outline

In this project, we design a novel test structure, nano-TLM, to address the issue of characterizing nano-scale ohmic contacts with ultra-low contact resistance. Built upon the conventional TLM, the nano-TLM is a powerful tool, capable of simultaneous measurement of contact resistance, metal sheet resistance, and semiconductor sheet resistance.

We demonstrate this new test structure by fabricating Mo/n^+-InGaAs contacts with various contact lengths. We achieve a record low contact resistance of 12.4 $\Omega \cdot \mu m$ at a contact length of merely 19 nm.

Besides n-type ohmic contacts, we also present preliminary results on p-type Sb-based semiconductors. Because of the lack of understanding of this family of materials, we investigate their contacts using conventional TLM rather than nano-TLM.

This thesis is organized in the following way. Chapter 2 gives a brief overview of the theory of metal-semiconductor contacts and a summary of existing characterization techniques. A complete model of our proposed nano-TLM is introduced with a discussion of the sensitivity and design issues.

In Chapter 3 we explain the details of the nano-TLM fabrication process, starting with an overview of the heterostructure design involved in this work. We also present an advancement of the nano-TLM process with a recess of the capping layer. An alternative approach of fabricating nano-scale metal contacts is provided as well.

Chapter 4 presents the experimental results of both As-based n-type contacts and Sb-based p-type ones. We extract contact resistance and contact resistivity using our nano-TLM test structures and the model derived in Chapter 2. We show that nano-TLM helps reveal how contact resistance increases as contact length scales down.

To conclude in Chapter 5, we summarize the key findings of this work on nano-scale ohmic contacts, and provide suggestions for future work in the field of III-V contact characterization.

CHAPTER 2. NANO-TLM THEORY AND MODEL

2.1 Introduction

In this chapter, we briefly review the physics of metal-semiconductor contacts, and summarize some existing characterization test structures and models. Then, we develop a two-dimensional distributed circuit network to model the proposed nano-TLM test structure. We explain the four-terminal Kelvin measurement schemes, and finalize with a discussion on relevant design issues.

2.1.1 Physics of Metal-Semiconductor Contact

In any microelectronic device, the last connection is always a metallic layer. Therefore, a good ohmic contact is critical for every semiconductor device. A metal-semiconductor contact is essentially a Schottky junction, which has three basic conduction mechanisms, depending on the Schottky barrier height and doping concentration. Those are thermionic emission (TE), thermionic-field emission (TFE), and field emission (FE), as shown in the band diagrams in Figure 2-1. Ideally, a low Schottky barrier height (SBH) is desired to achieve low contact resistance. However, it is often difficult to obtain low SBH, usually due to Fermi-level pinning at the semiconductor surface, or lack of metal with sufficiently low work function. Hence, field emission, which consists in carrier tunneling through the Schottky barrier, is the most preferred conduction mode for most real ohmic contacts.

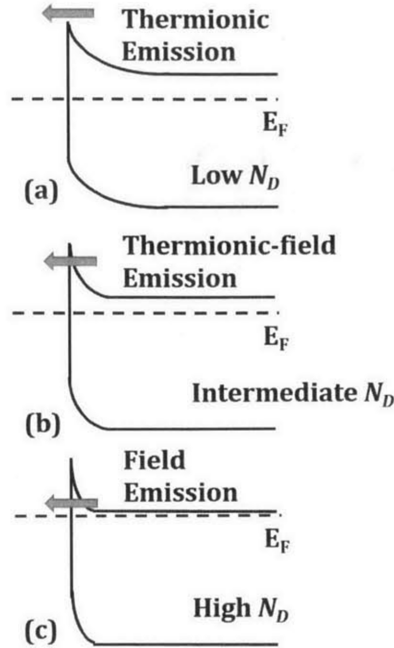


Figure 2-1 Conduction mechanisms of ohmic contacts. The electron flow is indicated by the arrow. The type of conduction mode depends on the doping concentration, N_D. (a) Thermionic emission at low N_D; (b) thermionic-field emission at moderate N_D; (c) field emission at high N_D, the most used type in real ohmic contacts.

2.1.2 Contact Resistance

An ohmic contact is characterized by its contact resistance, R_c (Ω·cm). This depends on geometry and a property of the metal-semiconductor interface which is the contact resistivity, ρ_c (Ω·cm^2). It is defined as the derivative of the voltage drop across the contact with respect to the current density, for a contact with zero contact area:

$$\rho_c = \lim_{V\to 0, A\to 0} A\frac{\partial V}{\partial I} \tag{3}$$

For transport in the field emission regime, the contact resistance, for n-type semiconductor for instance, is given by [16]:

$$\rho_c = \frac{Ck}{qA^*T}e^{q\phi_{Bn}/E_{00}} \tag{4}$$

C is function of doping level N_D and temperature T, k is the Boltzmann constant, A^* is the Richardson's constant, and ϕ_{Bn} is the Schottky barrier height. E_{00} is a characteristic energy proportional to $\sqrt{N_D}$. Based on (4), there are two main approaches to reduce ρ_c: First, reduce ϕ_{Bn} by choosing an appropriate metal-semiconductor system, and second, increase doping level to increase E_{00}, which in effect reduces depletion width of the Schottky junction. For III-V compound semiconductors, a common strategy is to use a heterostructure with a heavily-doped layer of a small bandgap material. In the following sections, we will describe how to measure the specific contact resistivity or contact resistance in actual devices.

2.2 Previous Work

In actual lateral devices like metal-oxide-semiconductor field-effect-transistors (MOSFETs), current flows into the ohmic contact and semiconductor along the surface of the sample as opposed to normal to the surface. Therefore, the contact resistance scales with the contact width, W, but not the contact length, L_c. Careful modeling is needed to extract R_c in lateral devices, and this section is devoted to introduce some well-known test structures designed for such purpose.

2.2.1 Transmission Line Model

The transmission line model (TLM), also known as the transfer length method, is perhaps one of the most widely used techniques to measure contact resistance. In TLM, two ohmic contacts are deposited on the semiconductor as metal thin films. As shown in Figure 2-2, a TLM consists of two contact metals (or pads) separated by a distance of L_d. A mesa of width W between the two contacts is used to confine the current in the active semiconductor layer. The overlap between the pad and mesa defines the contact length, L_c.

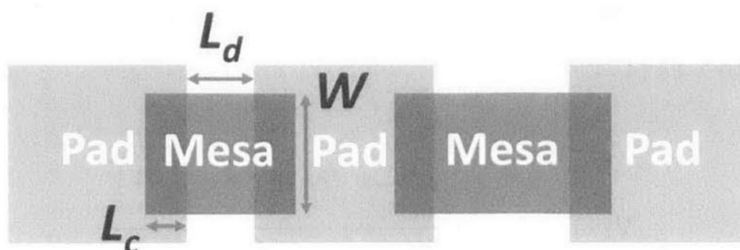


Figure 2-2 Schematic of a transmission line model (TLM) with relevant dimensions

Modeling a TLM is quite straightforward [17]. Figure 2-3 shows that a TLM comprises mainly two components: the contact resistance, R_c (Ω·cm), and the semiconductor sheet resistance, R_{sh} (Ω/□). R_c is usually normalized by multiplying by W to have the units Ω·cm. The total resistance, R_{tot} (Ω) of a TLM is given by:

$$R_{tot} = R_{sh} \cdot \frac{L_d}{W} + \frac{2R_c}{W} \tag{5}$$

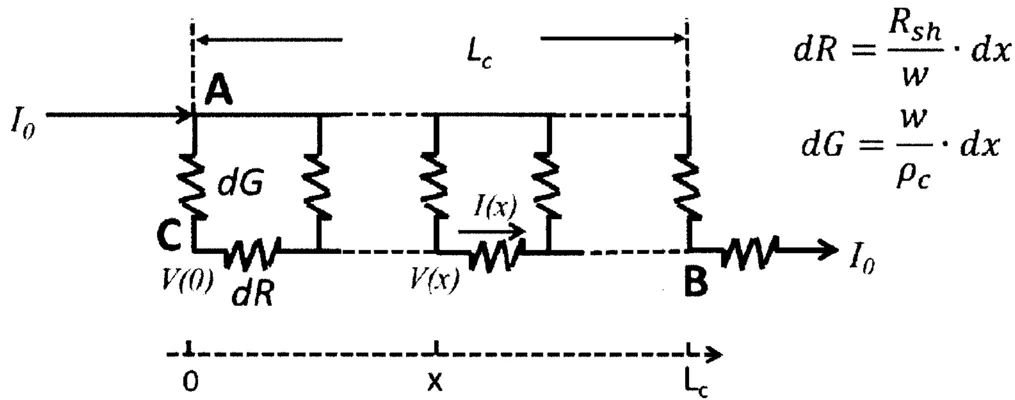


Figure 2-3 2-D resistive network model of an ohmic contact.

In order to find an expression for the contact resistance R_c, an eequivalent circuit network is usually used, as shown in Figure 2-3. In this model, we assume that the active semiconductor layer is very thin so that it is characterized by its sheet resistance, R_{sh}. In most cases, this is valid because the semiconductor layer in contact with the metal is heavily doped and the current flow is confined to a thin sheet along the surface. It is also common to neglect the metal sheet resistance, which is typically much smaller than R_{sh}. The contact is characterized by a differential contact conductance $dg_c = (W/\rho_c)dx$. Assuming a current I_0 entering the contact, we can find the voltage at location x as [17]:

$$\mathrm{V(x)} = I_0 \cdot \frac{\sqrt{R_{sh} \cdot \rho_c}}{W} \cdot \frac{\cosh\left(x \cdot \sqrt{\frac{R_{sh}}{\rho_c}}\right)}{\sinh\left(L_c \cdot \sqrt{\frac{R_{sh}}{\rho_c}}\right)} \tag{6}$$

And the current at that location on the semiconductor is:

$$I(x) = I_0 \cdot \frac{\sinh\left(x \cdot \sqrt{\frac{R_{sh}}{\rho_c}}\right)}{\sinh\left(L_c \cdot \sqrt{\frac{R_{sh}}{\rho_c}}\right)} \tag{7}$$

By dividing the voltage at x = L_c by I_0, one can find the contact resistance. Therefore:

$$R_c = \frac{V(x = L_c)}{I_0} \cdot W = \sqrt{R_{sh} \cdot \rho_c} \cdot \coth\left(L_c \cdot \sqrt{\frac{R_{sh}}{\rho_c}}\right) \tag{8}$$

In (8), the term in the coth is defined as the transfer length, L_T (μm):

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{9}$$

For long contacts, the transfer length represents the effective contact length over which the current transfers from the metal to the semiconductor. A few L_T away from the contact edge, there is no more current left in the semiconductor. To see this, assume $L_c >> L_T$, then $\coth(L_c/L_T) \approx 1$, and (8) becomes:

$$R_c \approx \frac{\rho_c}{L_T} \tag{10}$$

Therefore, for long contacts, most of the current flows over the transfer length. Thus, L_T is a useful measure of whether the contact is short or long. For a good ohmic contact, L_T is usually on the order 50 nm to 1 μm.

On the other hand, in the case of short contacts, $L_c << L_d$, then (8) can be approximated to the first order by:

$$R_c \approx \frac{\rho_c}{L_c} \tag{11}$$

In this case, as the contact is shorter than the transfer length, the current flows across the entire contact area with a uniform current density According to (11), for short contacts, the contact resistance blows up when the contact lengths shrinks down below the transfer length. This is one of the issues that is raised in Chapter 1. Because L_T scales with $\sqrt{\rho_c}$, for ohmic contacts with larger contact resistivity (worse contact quality), the problem of small contacts occurs earlier.

In a TLM, the contact pads are deposited with a separation L_d. By varying L_d and measuring the corresponding R_{tot}, we can extract R_c as half of the intercept at $L_d = 0$, by (5), and the slope is R_{sh}. One of the main limitations of a TLM takes place when R_c is extremely small, as desirable. Figure 2-4 illustrates such situation. If R_c is too low, usually on the order of 10 Ω·μm or below, the intercept is very close to the origin. Therefore, any small inaccuracy in the data can cause a large error at the intercept. As a result, for high quality ohmic contacts, even negative contact resistances can be occasionally read from a TLM measurement. Therefore, a more accurate test structure is indeed needed to characterize good ohmic contacts.

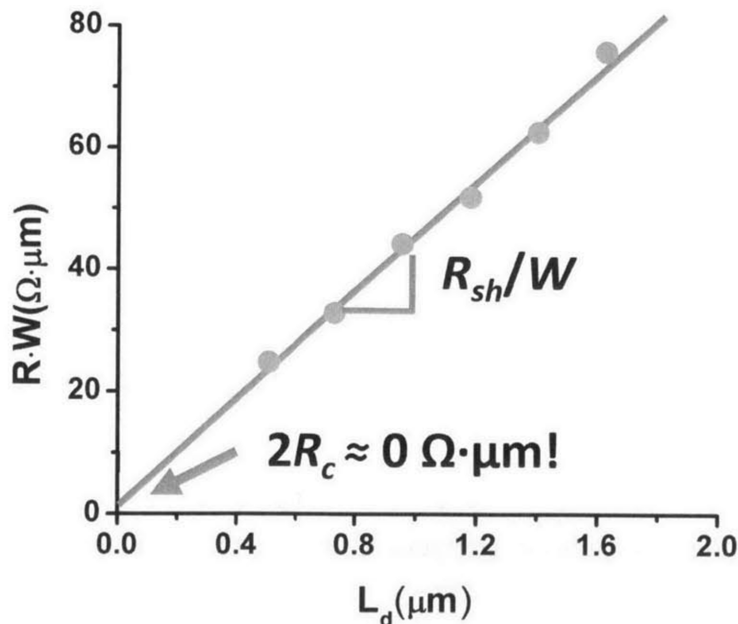


Figure 2-4 A TLM measurement featuring an ultra-low contact resistance. The intercept is close to zero, and it is difficult to make accurate reading of the contact resistance.

2.2.2 Cross-Bridge Kelvin Resistance

Besides the TLM, the cross-bridge-Kelvin-resistance (CBKR) test structure is another popular technique to measure contact resistance [18], [19]. In a TLM, the measurement depends on the underlying semiconductor and the contacting metal, and it is desirable to eliminate the effect of R_{sh} and R_{shm}, the metal sheet resistance. The main advantage of CBKR is that it allows a direct measurement of ρ_c without being affected by either R_{sh} or R_{shm}. The CBKR is a four terminal test structure with a window (via) in the center which forces current to flow vertically from the metal to the semiconductor. The principle of CBKR measurement is illustrated in Figure 2-5. As shown in Figure 2-5(a), by forcing a current from probe pad 1 to probe pad 2, a voltage difference is measured between probe pad 3 and probe pad 4, through the contact via at the center of the test structure. Figure 2-5 (b) illustrates the current path more clearly. It shows that the current path through the contact is vertical instead of lateral, as in the case of TLM where current crowding occurs. Therefore, the contact resistance is simply:

$$R_c = \frac{V_{34}}{I_{12}} \tag{12}$$

And since the current is vertical, the specific contact resistivity is:

$$\rho_c = R_c A_c \tag{13}$$

Where A_c is the contact area.

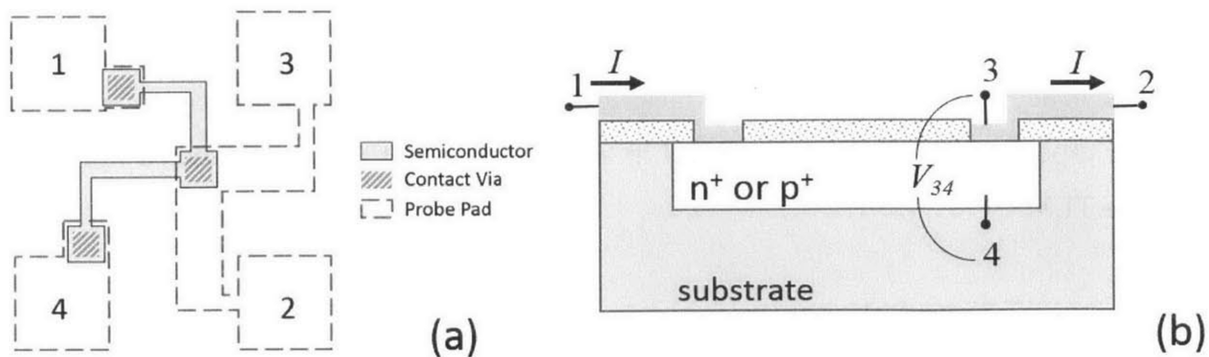


Figure 2-5 (a) top view of a cross-bridge kelvin resistance test structure -[18].(b) cross sectional view of the contact via.

Despite its simplicity, there are several issues in the CBKR method. First, the current flow is orthogonal to the contact, which is not the case in most MOSFETs. As a consequence, the contact length is not defined in such test structure. Second, CBKR assumes the size of the metal via is the same as that of the semiconductor square underneath. Otherwise, it suffers from current crowding due to misalignment. The error introduced by this geometrical problem is more severe for contacts with low resistivity [20]. Last but not least, CBKR is slightly more complicated to fabricate compared to the TLM, as it requires two metal depositions with a contact opening step.

There are many other well developed test structures for ohmic contact characterization. Most of them are variations of the TLM or CBKR introduced above. Nevertheless, none of the existing techniques is suitable for nano-scale ohmic contacts. In the next section, we introduce the nano-TLM test structure.

2.3 Nano-TLM Structure

2.3.1 2-D Circuit Model

A nano-TLM [9] is based on the concept of the conventional TLM explained in Section 2.2.1. As shown in Figure 2-6, it consists of two thin metal lines of contact length L_c, separated by a contact spacing L_d. This enables a four-terminal Kelvin measurement, which will be explained later in this section. Between the metal lines, the shaded area is the mesa region of width W, which confines the current between the two contacts. This unique design enables the fabrication and direct characterization of nano-scale ohmic contacts, which is not possible with any present techniques. The four terminal Kelvin measurement also allows more accurate parameter extraction, especially R_{shm}, which is critical in short contacts but usually neglected in methods such as the TLM.

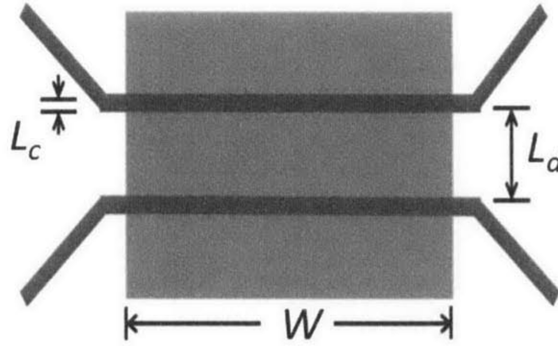


Figure 2-6 Top view of a nano-TLM test structure.

To model the nano-TLM, we borrow the technique of transmission line from conventional TLM. A 2-D equivalent distributed circuit network of nano-TLM is illustrated in Figure 2-7. In this model, the nano-TLM is divided into blocks of resistor meshes of length dx, with dr_m, the differential metal resistance along the metal contacts, and dg_s, the differential conductance between the two contacts.

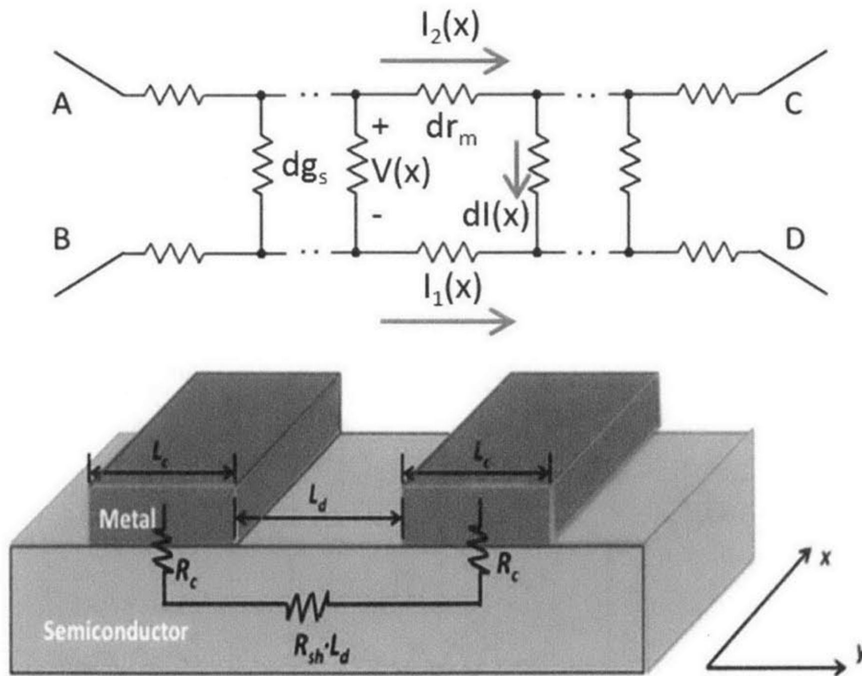


Figure 2-7. (Top) A 2-D distributed circuit network for the modeling of nano-TLM. (Bottom) cross-section of a nano-TLM model, showing the relevant dimensions and resistance components.

At point x, dr_m (Ω) is the elemental metal resistance:

$$dr_m = \frac{R_{shm} dx}{L_c} \tag{14}$$

And dg_s (Ω^{-1}), is the conductance of a conventional TLM of width dx. Therefore, (4) and (7):

$$dg_s = \frac{dx}{R_{TLM}} \tag{15}$$

where R_{TLM} (Ω·cm) is given by (5) and (8):

$$R_{TLM} = R_{sh} \cdot L_d + 2\sqrt{R_{sh}\rho_c} \coth\left(\frac{L_c}{L_{Ty}}\right) = R_{sh} \cdot L_d + 2R_c \tag{16}$$

$$L_{Ty} = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{17}$$

The transfer length in (9) is called L_{Ty} now as this is a two-dimensional problem. Then to establish a relation of the nodal voltage $V(x)$ and current $I(x)$, we apply Kirchhoff's voltage law, assisted by Figure 2-8:

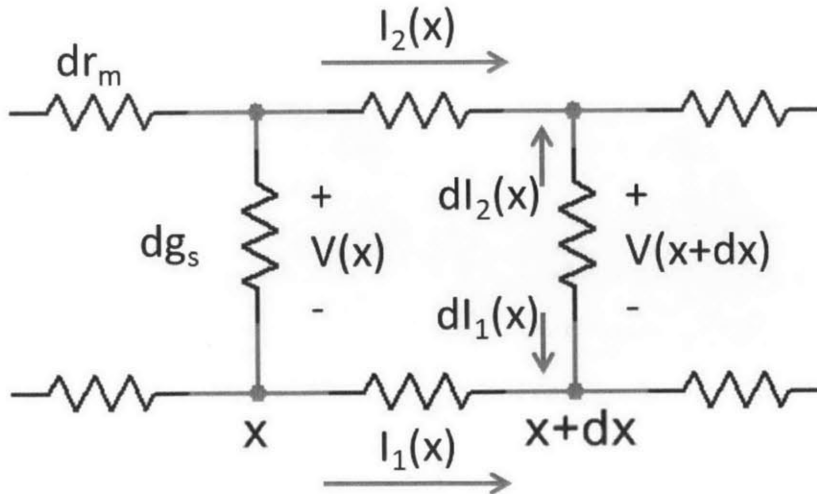


Figure 2-8 A differential unit of nano-TLM.

$$I_2(x)dr_m + V(x+dx) - I_1(x)dr_m - V(x) = 0 \tag{18}$$

Rearranging the terms in (18) gives:

$$V(x) - V(x+dx) = [I_2(x) - I_1(x)]dr_m \tag{19}$$

Therefore,

$$\frac{dV(x)}{dx} = [I_1(x) - I_2(x)] \cdot \frac{R_{shm}}{L_c} \tag{20}$$

At location $x+dx$, according to Figure 2-8,

$$\frac{dI_1(x)}{dx} = V(x+dx) \cdot \frac{dg_s}{dx} = \frac{V(x+dx)}{R_{TLM}} \tag{21}$$

Therefore by taking the derivative of (21) and applying (15), we have (assuming the second order term in $V(x+dx)$ vanishes after differentiation):

$$\frac{d^2I_1(x)}{dx^2} = \frac{1}{R_{TLM}}\frac{dV(x)}{dx} \tag{22}$$

Combining (20) and (22) gives:

$$\frac{d^2I_1(x)}{dx^2} = \frac{R_{shm}}{R_{TLM}L_c}\big(I_1(x) - I_2(x)\big) \tag{23}$$

Before we proceed to find the specific solution, we need to consider what measurements are possible in a nano-TLM. As shown in Figure 2-9, there are two kinds of resistances that can be measured in a nano-TLM, the parallel resistance, $R_{||}$ (Ω), and the cross resistance, $R_{\times}$ (Ω). Both are four terminal Kelvin measurements so that we do not have to include terminal and parasitic resistances. The combination of $R_{||}$ and $R_{\times}$ enables accurate extractions of R_c, R_{sh}, and R_{shm}. In actual measurements, the forcing and sensing ports are interchanged so that four sets of measurements per elemental test structure can be performed.

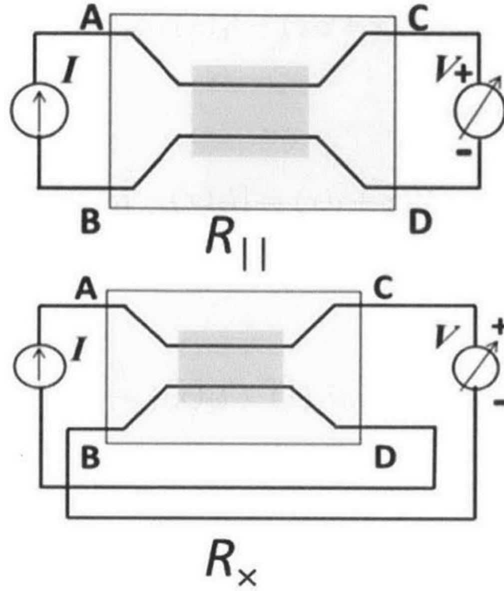


Figure 2-9 Two types of nano-TLM measurements: parallel resistance measurement and cross resistance measurement.

We first solve for $R_{\parallel}$. Due to the symmetry of the problem, $I_1(x) = -I_2(x)$, and boundary conditions are $I_1(0) = -I_0, I_1(W) = 0$. Therefore, from (23):

$$\frac{d^2}{dx^2}I_1(x) - \frac{I_1(x)}{L_{Tx}^2} = 0 \tag{24}$$

L_{Tx} is the transfer length in the x-direction:

$$L_{Tx} = \sqrt{\frac{R_{TLM}L_C}{2R_{shm}}} \tag{25}$$

Solving this differential equation with the boundary conditions above, yields:

$$I_1(x) = I_0\left[\coth\left(\frac{W}{L_{Tx}}\right)\sinh\left(\frac{x}{L_{Tx}}\right) - \cosh\left(\frac{x}{L_{Tx}}\right)\right] \tag{26}$$

Take the derivative of (26), and use (21):

$$V(x) = R_{TLM}\frac{dI_1(x)}{dx} = \frac{R_{TLM}I_0}{L_{Tx}}\left[\coth\left(\frac{W}{L_{Tx}}\right)\cosh\left(\frac{x}{L_{Tx}}\right) - \sinh\left(\frac{x}{L_{Tx}}\right)\right] \quad (27)$$

Therefore, we can find $R_{||}$ (Ω) as:

$$R_{||} = \frac{V(W)}{I_0} = \frac{R_{TLM}}{L_{Tx}}\left[\coth\left(\frac{W}{L_{Tx}}\right)\cosh\left(\frac{W}{L_{Ltx}}\right) - \sinh\left(\frac{W}{L_{Tx}}\right)\right]$$
$$= \frac{R_{TLM}}{L_{Tx}}\operatorname{csch}\left(\frac{W}{L_{Tx}}\right) \quad (28)$$

Next we solve for $R_\times$. In this case, the boundary conditions are $I_1(0) = 0$, and $I_1(W) = I_0$. And at location x, $I_1(x) + I_2(x) = I_0$. Applying this to (23) gives:

$$\frac{d^2I_1(x)}{dx^2} = \frac{R_{shm}}{R_{TLM}L_c}(2I_1(x) - I_0) \quad (29)$$

Using the same definition of L_{Tx}:

$$\frac{d^2I_1(x)}{dx^2} - \frac{I_1(x)}{L_{Tx}^2} + \frac{I_0}{2L_{Tx}^2} = 0 \quad (30)$$

Applying the boundary conditions above, the solution to (30) is:

$$I_1(x) = \frac{I_0}{2}\left\{\left[\coth\left(\frac{W}{L_{Tx}}\right) + \operatorname{csch}\left(\frac{W}{L_{Tx}}\right)\right]\sinh\left(\frac{x}{L_{Tx}}\right) - \cosh\left(\frac{x}{L_{Tx}}\right) + 1\right\} \quad (31)$$

Therefore we can find $V(x)$:

$$V(x) = R_{TLM}\frac{dI_1(x)}{dx} = \frac{R_{TLM}I_0}{2L_{Tx}}\left\{\left[\coth\left(\frac{W}{L_{Tx}}\right) + \operatorname{csch}\left(\frac{W}{L_{Tx}}\right)\right]\cosh\left(\frac{x}{L_{Tx}}\right) - \sinh\left(\frac{x}{L_{Tx}}\right)\right\} \quad (32)$$

For the cross measurement, according to Figure 2-9, we want to find $V_{CB} = V_{CD} + V_{DB}$. V_{CD} is given by:

$$V_{CD} = V(x = W) = \frac{R_{TLM}I_0}{2L_{Tx}}\left[\coth\left(\frac{W}{L_{Tx}}\right) + \operatorname{csch}\left(\frac{W}{L_{Tx}}\right)\right] \quad (33)$$

And computing V_{DB} is just a little more involved:

$$
\begin{aligned}
V_{DB} &= -V_{BD} = -\int_0^W I_1(x) dr_m \\
&= -\frac{R_{shm} I_0}{2L_c} \int_0^W \left\{ \left[\coth\left(\frac{W}{L_{Tx}}\right) + \operatorname{csch}\left(\frac{W}{L_{Tx}}\right) \right] \sinh\left(\frac{x}{L_{Tx}}\right) - \cosh\left(\frac{x}{L_{Tx}}\right) + 1 \right\} dx \\
&= -\frac{R_{shm} I_0}{2L_c} W
\end{aligned} \tag{34}
$$

Therefore:

$$
R_{\times} = \frac{V_{CB}}{I_0} = \frac{R_{TLM}}{2L_{Tx}} \left[\operatorname{csch}\left(\frac{W}{L_{Tx}}\right) + \coth\left(\frac{W}{L_{Tx}}\right) \right] - \frac{R_{shm} W}{2L_c} \tag{35}
$$

Hence, we have completed expressions of the two types of resistances that can be measured in a nano-TLM. Note that, unlike conventional TLMs in which the metal sheet resistance in the intrinsic device is not modeled, here it is taken into account in (28) and (35). As R_{shm} goes to zero, both equations converge to R_{TLM}/W, which coincides with the classic TLM result.

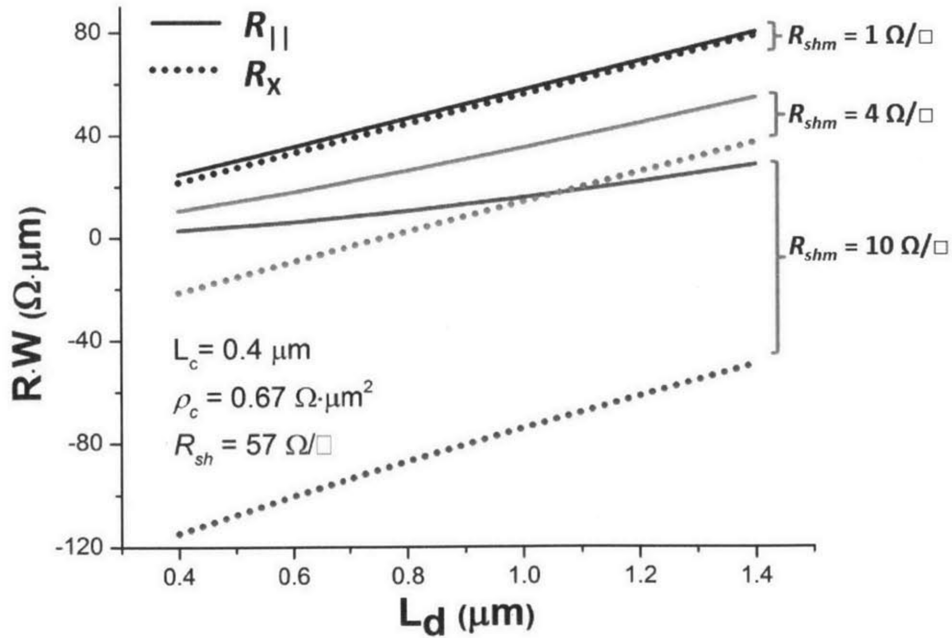
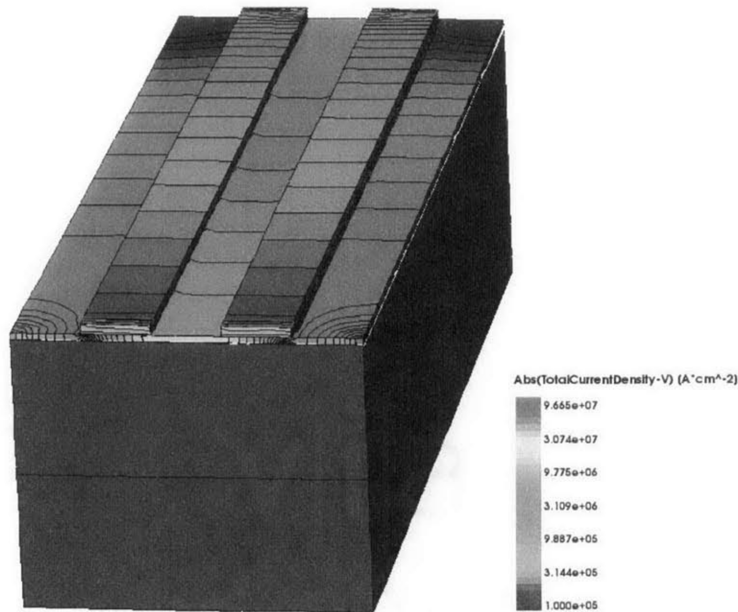


Figure 2-10 Modeled terminal resistances versus contact spacing for various contact lengths, showing the impact of the metal resistance.

We need to understand how the inclusion of the metal sheet resistance, which is not accounted for in conventional TLM or CBKR, will affect the actual measurement. Figure 2.10 shows $R_{\parallel}$ and $R_{\times}$ as a function of L_d for different contact lengths, predicted by the model we just developed. In long contacts, both resistance approach each other, while in short ones, $R_{\times}$ drops below $R_{\parallel}$ due to the negative term in (35) which captures the voltage drop along the thin metal line. Numerical simulation shown in Figure 2-12 also confirms this behavior. We will verify this phenomenon from the experimental results in Chapter 4.

2.3.2 TCAD Simulation

Besides the closed form solution obtained in the previous section, we also want to verify the physical behavior of nano-TLM using numerical simulations. This is because the nano-TLM is a three-dimensional device but our solution deals with a 2-D problem. We therefore use Synopsys Sentaurus TCAD (Technology Computer Aided Design) to build up the simulation. Figure 2-11 shows the structure of the contact system. It consists of a 20 nm n^+-InGaAs ($N_D = 10^{19}$ cm^{-3}) capping layer on top of a layer of InAlAs semi-insulating buffer on top of an InP substrate. The contact metal is 30 nm Mo. We use the same contact system that we experimentally investigate in Chapter 3.



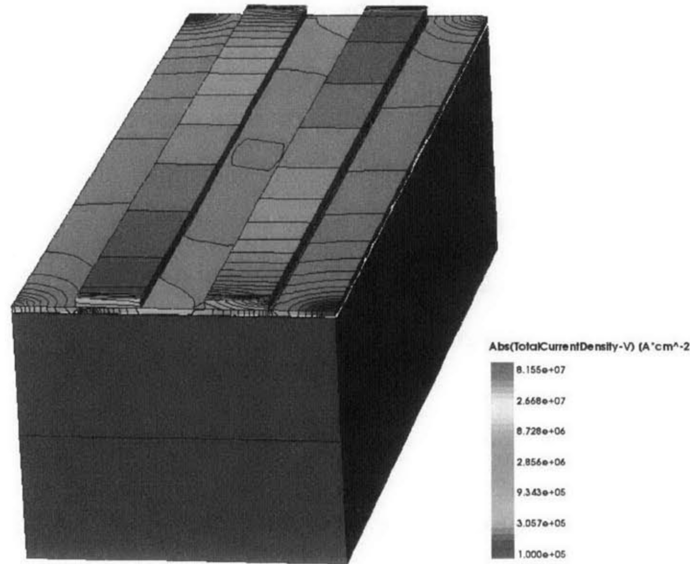


Figure 2-11: Schematic of nano-TLM simulation in Synopsys Sentaurus, L_c = 200 nm and L_d = 200 nm. The color bar shows the total current density of (top) parallel resistance measurement, and (bottom) cross resistance measurement.

As shown in the left part of Figure 2-11, the parallel measurement has a symmetric current density distribution, and in the right part, the cross measurement characteristics is asymmetric. Voltage drops in both x and y directions are observed as a result of the metal resistance and the semiconductor resistance. By simulating nano-TLMs with varying contact separation (L_d), we can extract the contact resistivity from the simulated data, as shown in Figure 2-12, for L_c *values* between 200 nm and 1 μm.

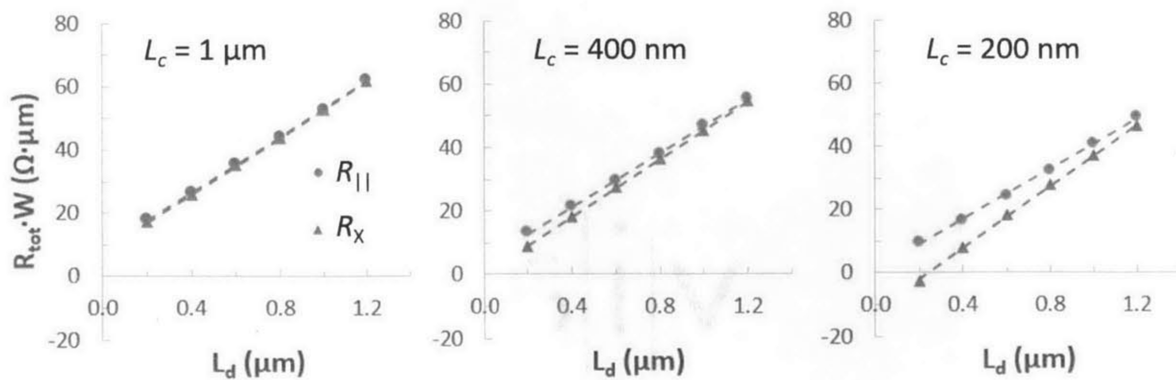


Figure 2-12 Nano-TLM simulation results of (left) contact length of 1 μm, (middle) 400 nm, and (right) 200 nm. The dotted lines are fitted by the analytic model to extract ρ_c, R_{sh}, and R_{shm}.

The simulation assumes a ρ_c of 1 $\Omega\cdot\mu m^2$, R_{sh} of 45 $\Omega/\square$, and R_{shm} of 1.9 $\Omega/\square$. We use the analytic model to fit the simulation results, and the extracted ρ_c is 0.9 $\Omega\cdot\mu m^2$, R_{sh} is 45 $\Omega/\square$, and R_{shm} is 1.8 $\Omega/\square$, showing excellent consistency. This shows that our analytical model agrees well with the numerical simulations.

2.4 Discussion

2.4.1 Error and Sensitivity

One of the motivations for introducing the nano-TLM is that it can provide higher accuracy in the extraction of contact resistance. In a conventional TLM, problems occurs when the contact resistance is small, as already illustrated in Figure 2-4. Another issue arises from errors in the measurement. If there are discrepancies in the semiconductor sheet resistance or the contact resistance, the simple fitting strategy will cause large error, as illustrated in Figure 2-13 [21].

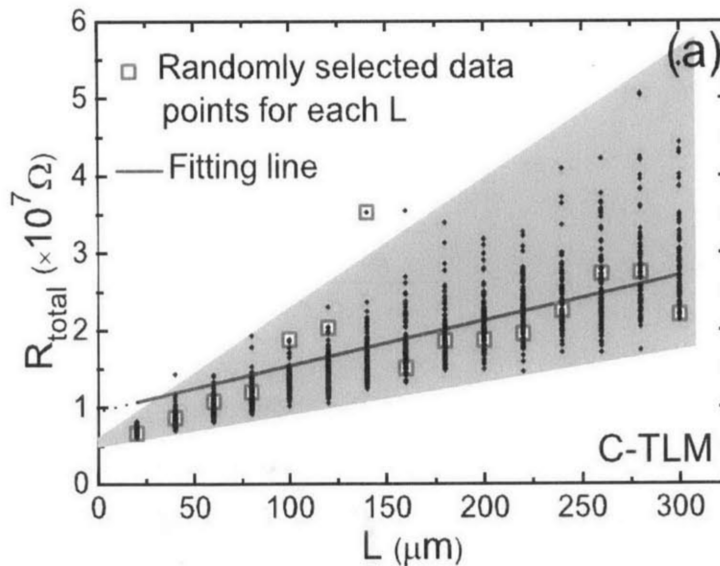


Figure 2-13 Error analysis of conventional-TLM. The shaded group of data is introduced by assuming a Gaussian distribution of electron mobility in the wafer. Fitting the randomly selected data gives an intercept away from the real value. Picture adapted from [21].

Unlike the conventional TLM, nano-TLM allows two measurement schemes, $R_{\parallel}$ and $R_{\times}$, and by interchanging the ports it involves four sets of measurements in total. Therefore, extraction of the contact resistance requires simultaneous nonlinear fitting of four data sets, which requires more

computational cost but provides much better accuracy. We will examine the accuracy of nano-TLM experimentally in Chapter 4.

In our analytic model of nano-TLM, there are two factors that are neglected: (1) the impact of metal sheet resistance in the y-direction, and (2) the impact of the semiconductor sheet resistance underneath the metal contacts. Impact of R_{shm} in the y-direction can be reasonable neglected because it is usually much smaller than R_{sh}. The impact of R_{sh} underneath the metal is often more observable, because the semiconductor sheet resistance under the contact can differ from that in the gap region, as is the case of alloyed contacts. To include these non-idealities in the model, we use R_{sk} (Ω/□) to denote the semiconductor sheet resistance beneath the metal contacts. Then, following a similar procedure as in Section 2.3.1, one can find R_c (Ω·cm) as:

$$R_c = \frac{\rho_c}{L_{Tm}(1+\alpha)^2}\left[(1+\alpha^2)\coth\left(\frac{L_c}{L_{Tm}}\right) + \alpha\left(\frac{2}{\sinh\left(\frac{L_c}{L_{Tm}}\right)} + \frac{L_c}{L_{Tm}}\right)\right] \tag{36}$$

Where α and L_{Tm} are:

$$\alpha = \frac{R_{shm}}{R_{sk}}$$

$$L_{Tm} = \sqrt{\frac{\rho_c}{R_{shm}+R_{sk}}} = \frac{L_{Ty}}{\sqrt{1+\alpha}} \tag{37}$$

Note that the term L_{Ty}, the transfer length in the y-direction, is now replaced by L_{Tm} which replaces R_{sh} by R_{sk} and includes R_{shm}. With the modified equation of R_c, the same expressions of nano-TLM total resistance can be used as in (28) and (35). The modification is small because α is usually less than 0.1 for good metal contact. From numerical analysis, it can be shown that for contact lengths shorter than 1 μm, the resulting error in R_c is less than 10% for a typical metal-semiconductor contact system, and the error drops quickly as the contact length decreases.

2.4.2 Design Issues

The model derived in Section 2.3.1 provides guidance to test structure design for accurate extraction of contact resistance. There are at least three considerations to be accounted for in the

design of a nano-TLM. In general, one would like to have many test structures with identical L_c and different L_d. In particular, one needs: (1) a thick metal layer to minimize $R_{shm,}$ (2) small values of L_d to reduce the impact of R_{sh}, and (3) a small value of contact width, W, to also mitigate the impact of metal resistance. Equations (28) and (35) suggests that W should be on the order of L_{Tx}. Reasonably small W also makes the alignment during fabrication easier. We will make use of the above design guidance in the nano-TLM fabrication as described Chapter 3.

2.5 Summary

In this chapter, we have reviewed the physics of metal-semiconductor contacts. We provide a brief summary of major characterization techniques. Building upon the concept of a TLM, we proposed a novel test structure, the nano-TLM, and develop an analytical model for it. We expect this test structure to be able to make accurate measurements of ultra-low contact resistance on nano-scale ohmic contacts. Then, a short discussion on the sensitivity of the model and design issues of the nano-TLM are presented. In the following chapter, we will describe the fabrication details of nano-TLMs in the Mo/InGaAs system, which allows us to examine the model developed in this chapter.

CHAPTER 3. NANO-TLM FABRICATION

3.1 Introduction

In this chapter, we demonstrate the fabrication of the proposed nano-TLM test structure on the Mo/n$^+$-InGaAs contact system. We use a metal-first process in order to achieve high quality ohmic contacts. We also propose an alternative process which is also capable of characterizing nano-scale contacts. The alternative process costs more fabrication steps but simplify the electrical characterizations. Results from electrical measurement of the fabricated devices will be discussed in the next chapter.

3.2 Overview of Heterostructures

For n-type ohmic contacts, we use an InGaAs-based structure because of its extraordinary electron transport characteristics [3], [15]. Figure 3-1 shows a diagram of the heterostructure that is used in this study. The heterostructure is designed for a FinFET process, which is valuable for this study as we can emulate the ohmic contact process on a real device structure. The heterostructure was grown by SEMATECH using molecular beam epitaxy (MBE).

The heterostructure was grown on a 3-inch semi-insulating InP substrate. First, a 300 nm $In_{0.52}Al_{0.48}As$ buffer layer was grown, which is useful to block the leakage current because it has a wider bandgap (1.46 eV) than that of $In_{0.53}Ga_{0.47}As$ (0.74 eV). Then a 10 nm layer of InP layer and another layer of $In_{0.52}Al_{0.48}As$ are grown, in which the thin InP layer can be served as an etch stop. Following this, a 20 nm $In_{0.53}Ga_{0.47}As$ channel layer is grown with a 2nm InP etch stop right after it. For this project, the most important part of the heterostructure is the 20 nm n$^+$-

$In_{0.53}Ga_{0.47}As$ cap layer. This is heavily doped by Si (1×10^{19} cm^{-3}). The sheet resistance of the cap layer is 54 Ω/□, obtained by a van de Pauw measurement. All layers in this heterostructure are lattice matched to the InP substrate.

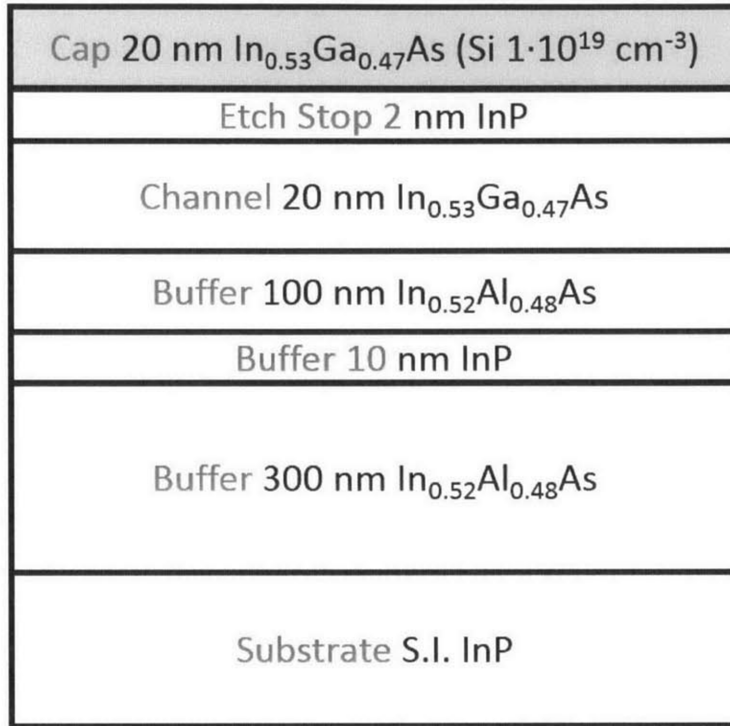
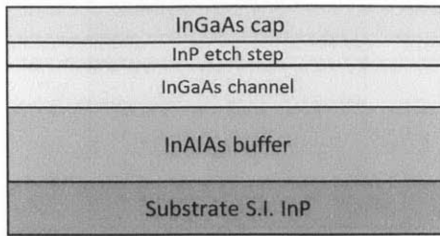


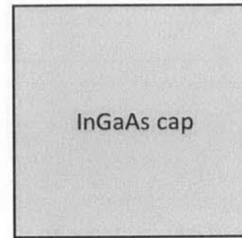
Figure 3-1 Cross section detailing the heterostructure used for nano-TLM fabrication in this study.

3.3 Nano-TLM Process

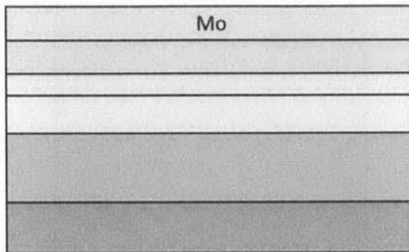
To achieve the nano-TLM test structure shown in Figure 2-6, a process flow is developed for device fabrication. In order to maintain a good ohmic contact interface, we use a contact-first approach to minimize contamination introduced in subsequent fabrication steps. We use Mo, a refractory metal, as the contact metal because of its small Schottky barrier height on InGaAs, and its feasibility for a dry etch process. Figure 3-2 illustrates the details of the process steps that are used in this study. The entire fabrication is done in the cleanrooms of the Microsystem Technology Laboratories (MTL) at MIT.



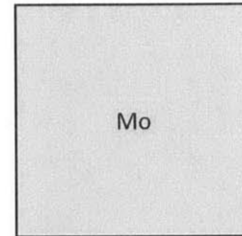
Step 1 (side view)



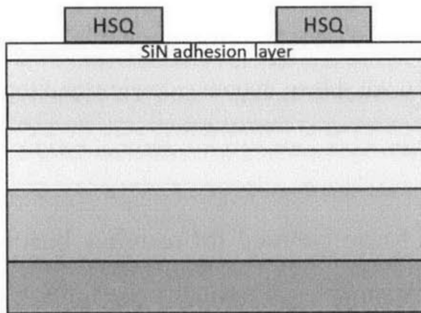
Step 1 (top view)



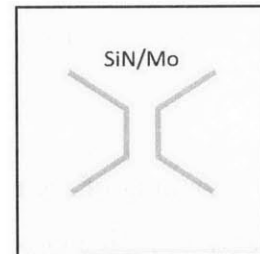
Step 2 (side view)



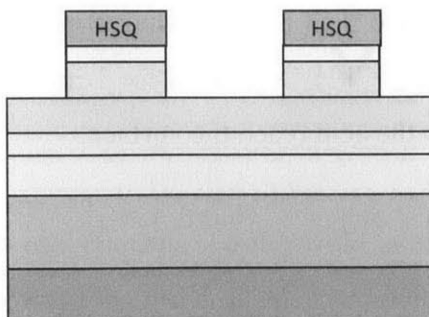
Step 2 (top view)



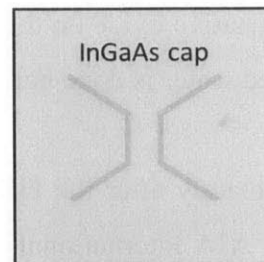
Step 3, 4 (side view)



Step 3,4 (top view)



Step 5 (side view)



Step 5 (top view)

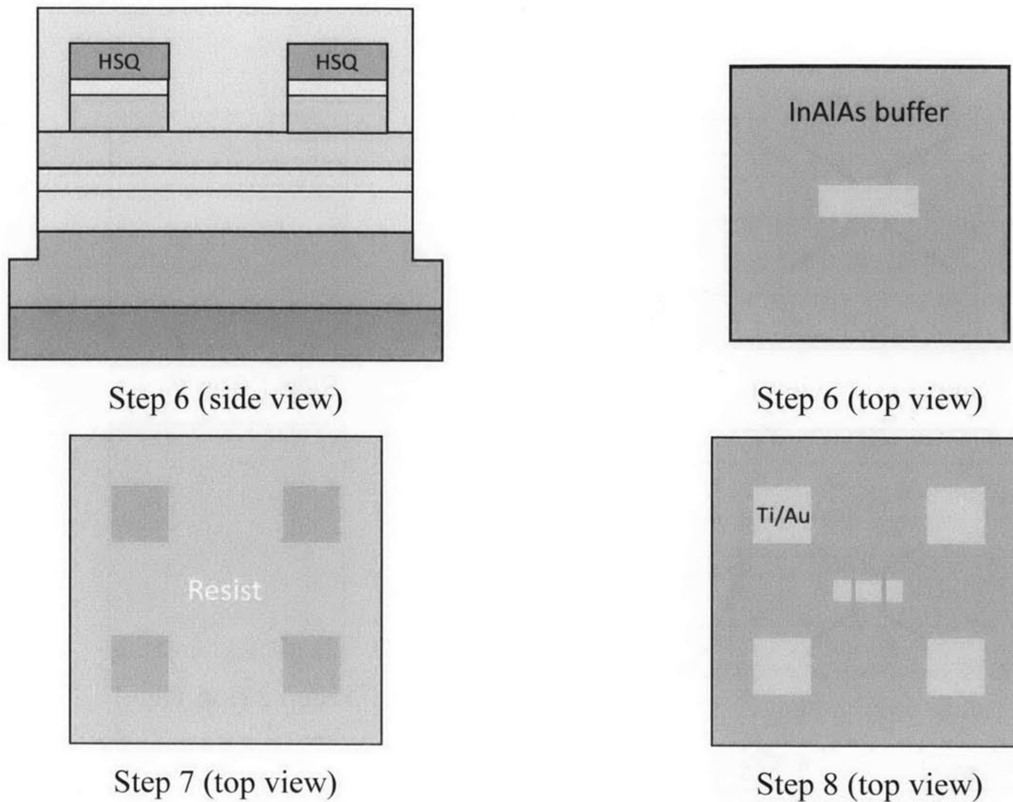


Figure 3-2 Process flow of a nano-TLM fabrication. Steps 1-6 are shown in both side view and top view.

Step 1. At the beginning of the process, the wafer needs to be cleaned thoroughly before metal deposition. The wafer is first cleaved into 10 mm × 10 mm samples. Each sample is then cleaned in ultrasonic deionized water to remove fragments on the surface. Then the sample is rinsed by acetone, methanol, and isopropanol (IPA) each for 1 min and then is dried using a nitrogen gun. Afterward, the native oxide on the sample is etched by 1:3 $HCl:H_2O$ solution for 1 min. A 1 min dip in deionized water is done before the HCl etch to help the acid reach the surface.

Step 2. Immediately after the HCl treatment, the sample is blown dried, and put into vacuum chamber of an AJA International ATC-180 sputter deposition system. It is critical to avoid long exposure to air of the sample to avoid formation of native oxide. The vacuum chamber is pumped down to pressure less than 10^{-7} Torr, Then, a 60 nm layer of Mo is sputtered by Ar DC plasma biased at 100 W, with a 15 sccm flow of Ar. The deposition rate is about 0.8 Å/s.

Step 3. After Mo sputtering, the sample is coated with 2 nm of Si_3N_4, using a ST System chemical vapor deposition (CVD) machine. The 2 nm Si_3N_4 is used to help adhesion of the electron-beam resist on Mo. The sample is then coated with 6% HSQ (hydrogen silsesquioxane), a spin-on glass that can be used as a negative tone electron-beam resist. The HSQ is spin-coated at spin speed of 4000 rpm for 60 s, resulting in a thickness of 97 nm. The sample is baked at 200 °C for 2 min on a hotplate. It shall be noted that after the HSQ coating, the sample needs to be immediately exposed to prevent overdose of HSQ due to self-development in air. The Si_3N_4 adhesion layer is also critical in this process, as HSQ adhere well to Si but poorly to metal. For HSQ patterns with high aspect ratio, good adhesion is required to prevent collapse.

Step 4. Immediately after HSQ coating, the sample is exposed using an Elionix ELS-F125 electron-beam lithography system. The electron gun has an accelerating bias of 125 keV, the step size is 0.625 nm, and the beam diameter is about 1.7 nm. The beam current is 1 nA, and the electron dose is between 6400 to 8200 $\mu C/cm^2$, depending on the pattern size. Usually a dose test is done before the actual exposure to avoid overdose or underdose. After the e-beam exposure, the sample is developed in 25% Tetra-methyl-ammonium Hydroxide (TMAH) solution for 80 s. The sample is then inspected using a high resolution scanning electron microscope (SEM). Figure 3-3 gives an example of well-developed nano-TLM patterns.

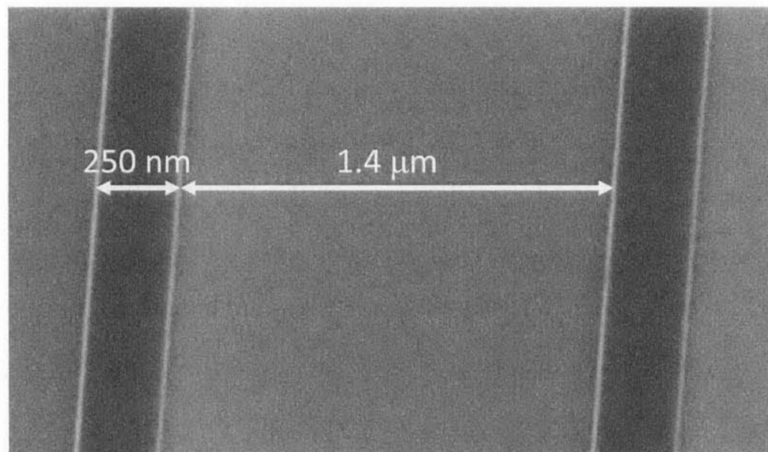


Figure 3-3 SEM picture of two developed HSQ lines after electron-beam lithography.

Step 5. The 60 nm Mo layer is then etched with SF_6/O_2 plasma. A Plasmaquest electron cyclotron resonance (ECR) reactive ion etcher (RIE) is used. Prior to the dry etch, the chamber is

cleaned by $CF_4/O_2/He$ plasma for 10 min and preconditioned for an extra 10 min. Then, Mo is etched in 90/10 SF_6/O_2 plasma at 20 °C. The oxygen ratio cannot be too large as it makes the etching more isotropic. The ECR plasma is biased at 250 W, with a RF power of 50 W. The etch rate is approximately 3.5 Å/s. Figure 3-4 shows resulted Mo lines of width 40 and 30 nm, respectively. After the Mo etch, the HSQ hard mask is not removed intentionally, as it can protect the thin Mo line in the subsequent process.

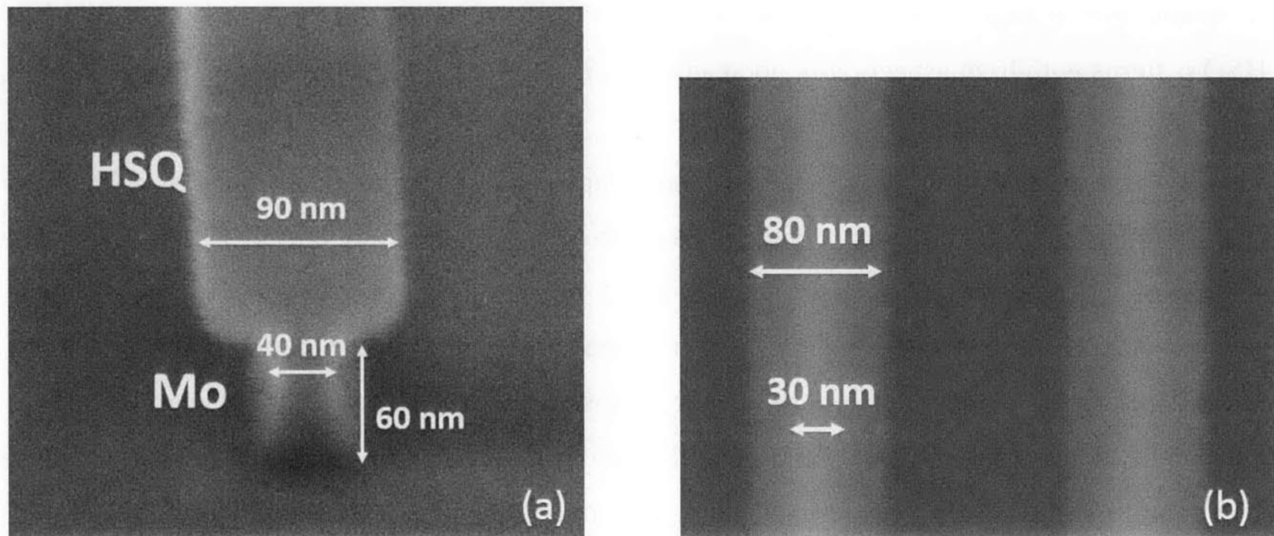


Figure 3-4 Dry etched Mo lines using HSQ as hard mask. (a) Side view of a 40 nm wide Mo line; (b) top view of 30 nm Mo.

Step 6. The mesa region is then defined by photolithography. The sample is first rinsed sequentially in acetone, methanol, and IPA for 1 min each. Then the sample is coated with OCG825 g-line photoresist, followed by a 5 min pre-bake at 80 °C. The sample is exposed for 11 s by a Karlsuss MA-6 contact alignment/exposure tool. The photoresist is developed in OCG934 developer for about 1 min. The sample is inspected under microscope to ensure complete development.

The mesa is dry etched using BCl_3/N_2 plasma. A SAMCO 200iP inductively coupled plasma (ICP) RIE is used for this purpose. The etching is carried out at room temperature, with BCl_3 and N_2 gas flow of 13.5 and 5.5 sccm, respectively. The ICP is biased at 20 W, with a RF power of 160 W. The pressure of the chamber is 0.25 Pa during etching. The etch rate is approximately 1.8

nm/s. The high density ICP plasma creates a vertical etch profile, as shown in Figure 3-5. Figure 3-6 shows a nano-TLM after the mesa etch, with the resist covering the mesa area.

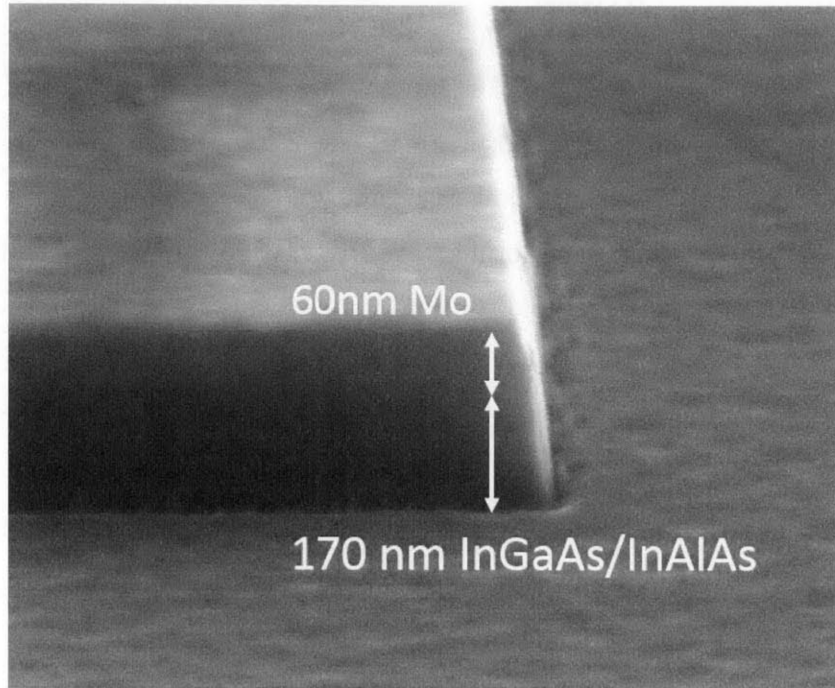


Figure 3-5 Side view of the finished mesa ICP etch.

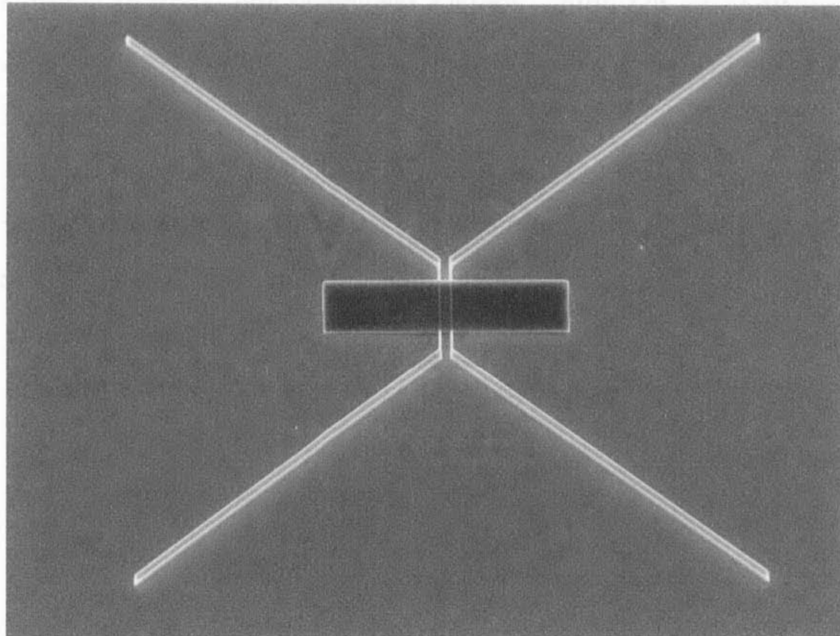


Figure 3-6 Nano-TLM after the mesa etch, corresponding step 5 in Figure 3-2.

Step 7. The OCG825 resist is ashed away for one hour. The sample is then cleaned again with organic solvents, and is ready for the final metallization step. This is done in another photolithography step, using AZ5214, an image reversal photoresist which is useful for lift-off. The resist is spin-coated at 3000 rpm for 30 s, and pre-baked at 80 °C for 5 min. Then the sample is exposed for 7 s using MA-6. After exposure, a 120 °C 2 min reversal bake is carried out. The temperature of the reversal bake is critical to ensure the correct crosslinking of the exposed resist. A flood exposure of 90 s is performed. Afterwards the sample is developed in AZ422 developer for 2 min or more until the field is clear.

Step 8. We then proceed to the final metallization. Prior to metal deposition, the sample is descummed in oxygen plasma for 5 min in an asher. Then the sample surface is cleaned in 1:3 $HCl:H_2O$ for 1 min to strip the oxide. Right away, the sample is coated with 10/100 nm Ti/Au using a Temescal FC-2000 electron beam evaporator. Then the sample is soaked in acetone for 2 hours to finish the lift-off process. The sample is cleaned with isopropanol and blown dry with N_2.

Step 9. In order to improve the ohmic contact resistance and study its thermal stability, rapid thermal annealing (RTA) is performed from 250 to 500 °C in pure N_2 ambient for 1 min. During RTA, the sample is put facing down on a GaAs wafer as proximity cap to avoid surface decomposition [22]. In the following chapter we will present the thermal stability study of Mo contacts. A SEM picture of the finished nano-TLM structure is shown in Figure 3-7. Figure 3-8 shows a nano-TLM with the smallest contact length, 19 nm, that is achieved in this process. It shall be noted that, in order to perform accurate measurement and parameter extraction, all dimensions such as L_c and L_d are measured by SEM on each individual structure.

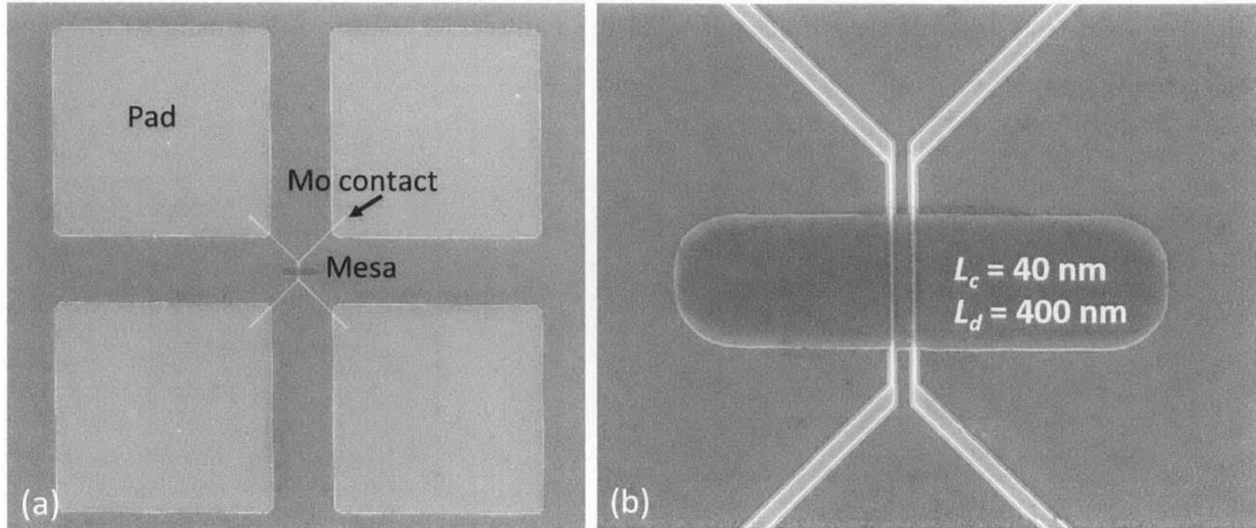


Figure 3-7 SEM pictures showing (a) the entire nano-TLM test structure; (b) the mesa and Mo contact region.

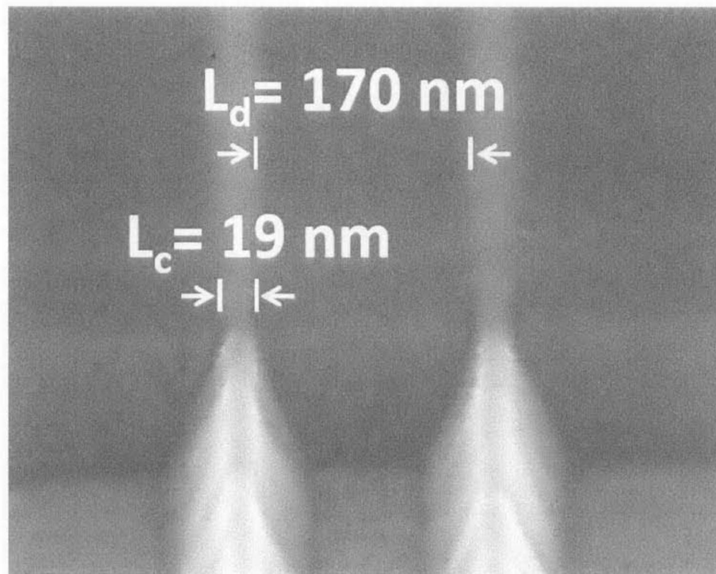
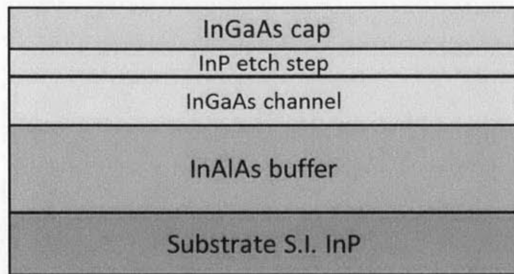


Figure 3-8 Nano-TLM with 19 nm contact length.

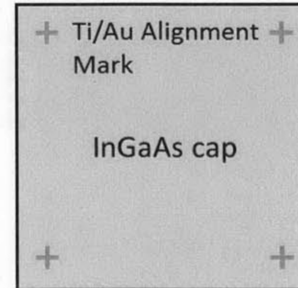
3.4 Alternative Process

In the previous section, we described a fabrication process for the nano-TLM test structure. There is also an alternative way to fabricate a conventional TLM structure with nano-scale contacts. This is a two-terminal test structure. It is more difficult to fabricate than the nano-TLM, but it is relatively more straightforward to characterize. Therefore, we briefly present the process

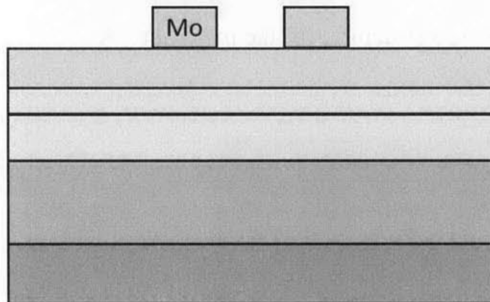
flow of such test structure as an alternative to the nano-TLM. Figure 3-9 illustrates the major steps in the process.



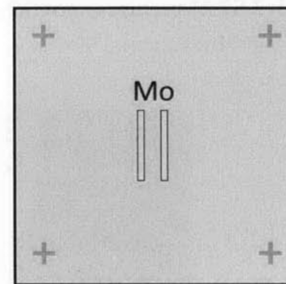
Step 1 (side view)



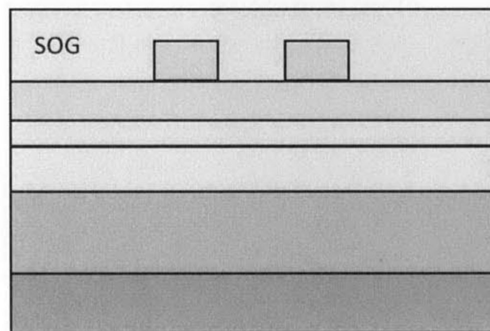
Step 1 (top view)



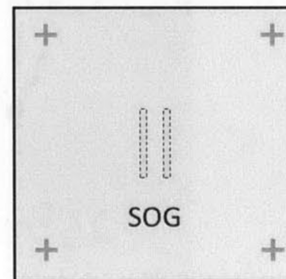
Step 2 (side view)



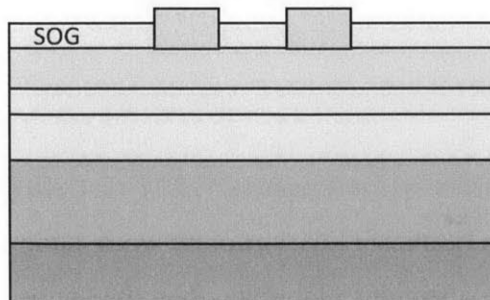
Step 2 (top view)



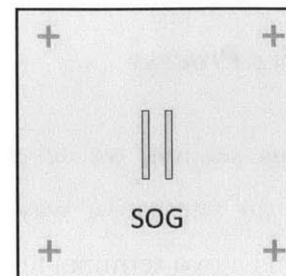
Step 3 (side view)



Step 3 (top view)



Step 4 (side view)



Step 4 (top view)

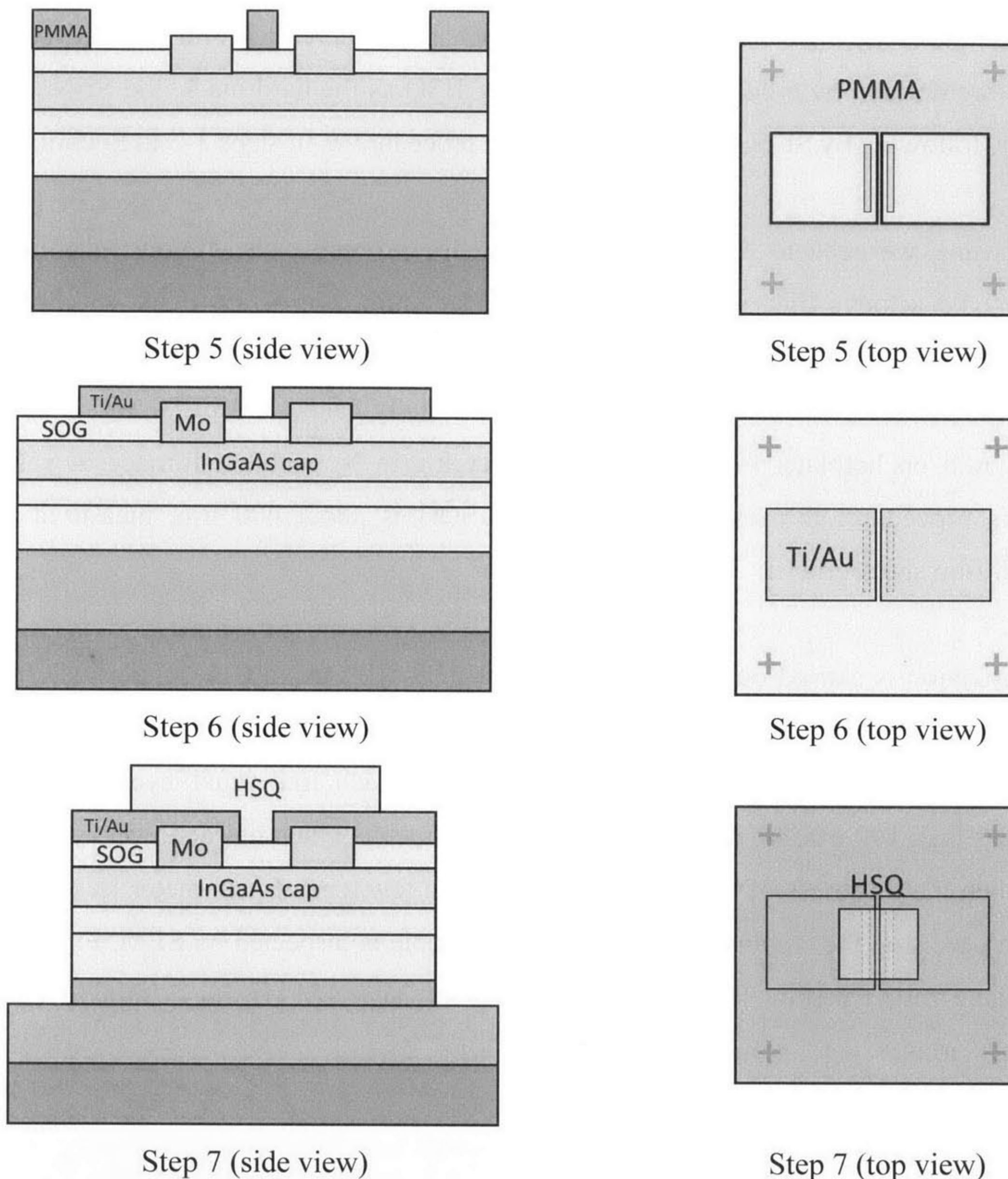


Figure 3-9 Process flow of an alternative fabrication method of nano-scale TLM test structure.

Step 1. Unlike the nano-TLM process in Section 3.3, this process needs to start with alignment mark deposition, as it involves two e-beam lithography steps that require precise alignment. Starting with the same surface cleaning procedure as in Section 3.3, the sample is coated with PMMA (polymethyl methacrylate) A8, a high resolution positive e-beam resist. Then the alignment marks are defined by e-beam lithography, and developed in 1:3 MIBK (methyl isobutyl ketone): IPA solution for 90 s.

Step 2. The sample is then is cleaned with 1:3 $HCl:H_2O$ and sputtered with 80 nm Mo. The Mo nano-contacts are defined by e-beam lithography using HSQ as the hard mask and Si_3N_4 as the adhesion layer, following by SF_6/O_2 RIE. It is the same procedure as in steps 1-5 in Section 3.3.

Step 3. Afterward, we need to find a way to deposit the probing pads without touching the semiconductor. To achieve this, we incorporate a planarization step using FOX 16 (flowable oxide), a spin-on-glass (SOG) available from Dow Corning. The FOX 16 is spin-coated on the sample at 5000 rpm for 60 s. Then the coating is sequentially baked at 150 °C for 2 min and 200 °C for 2 min on hotplate, followed by 1 hour curing in N_2 ambient furnace at 350 °C. Following this procedure, the resulted thickness of SOG is about 400 nm, measured by a Filmetrics thin film spectrometer.

Step 4. Planarization is carried out in the Plasmaquest ECR RIE, using CH_4/H_2 plasma. This is an oxide etch recipe with an etch rate of approximately 30 nm/min. The sample is etched with 1 min cycles, and the thickness of SOG is measured after each individual cycle. When the thickness is less than 100 nm, we use a CF_4-based plasma recipe which has a slower etch rate of 8 nm/min. When the thickness of the SOG layer is about a few tens of nanometer less than that of Mo (80 nm), we stop the etching procedure and the sample is inspected by SEM. Figure 3-10 shows the planarization result. The sample is dipped in 25% TMAH for 1 min to remove residues on the surface.

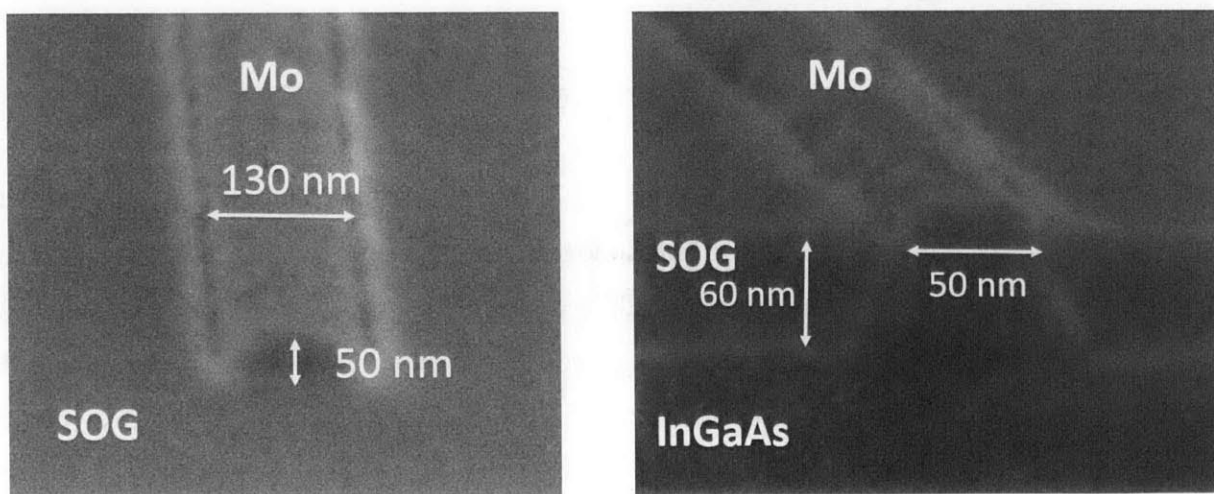


Figure 3-10 Planarization results of nano-scale TLM test structure. The spin-on-glass (SOG) is etched to a few tens of nanometers below the Mo contact. (left) tilted top view; (right) side view.

Step 5. After planarization, the sample is patterned with PMMA A8 for pad deposition. As shown in Figure 3-9, because the distance between two nano-contacts is small (in our case, 0.4 – 1.4 μm), it is difficult to use photolithography. Therefore, we again use e-beam lithography to align and pattern the pads. After exposure, the e-beam resist is developed in MIBK:IPA solution for 90 s as in step 1.

Step 6. The sample surface is cleaned with diluted HCl solution and immediately transferred into vacuum for pad deposition. 10 nm Ti and 200 nm Au is then e-beam evaporated and lifted-off in acetone.

Step 7. Finally, the mesa area is patterned with HSQ using e-beam lithography. The mesa region is etched by BCl_3/N_2 ICP plasma, with a depth of approximately 150 nm. The finished sample is RTA annealed if needed. Figure 3-11 portraits the completed nano-scale TLM.

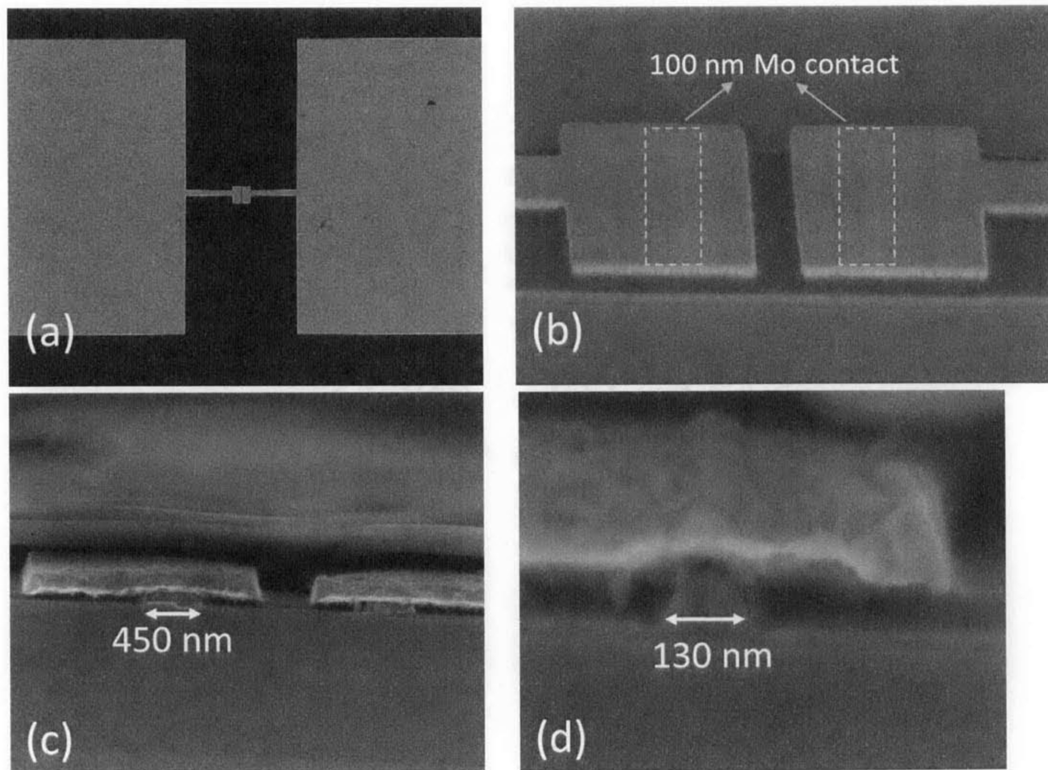


Figure 3-11 SEM pictures of the finished nano-scale TLM structure: (a) top view showing the entire test structure, (b) the mesa area, (c) side view of a nano-contact of L_c = 130nm and (c) a nano-contact of L_c = 450 nm.

3.5 Summary

In this chapter, we developed a process flow to fabricate the proposed nano-TLM test structure. Critical steps were illustrated and explained in details. Using this contact-first process, we successfully fabricated nano-TLMs with contact lengths as small as 19 nm. It can be concluded that this test structure is straightforward to fabricate, and can be easily integrated into an actual device process. In addition, we also provide an alternative process flow of nano-scale conventional TLM, a two-terminal test structure. In the following chapter, we will present the results from electrical measurements.

CHAPTER 4. EXPERIMENTAL RESULTS

4.1 Introduction

In the last chapter, we have demonstrated the fabrication process of the proposed nano-TLM test structure. In this chapter, we present the electrical characterization part of this study, and show results from the nano-TLM measurement of the Mo/n^+-InGaAs contact system. Thanks to the advantage of the nano-TLM, we demonstrate contact resistance extractions with very high accuracy, and we are able to measure R_c as a function of contact length, which ranges from 19 to 450 nm. Our Mo contacts have an average contact resistivity of 0.69 ± 0.3 Ω·μm^2, which is the lowest value reported for n^+-InGaAs at the doping level of 10^{19} cm^{-3}, to the best of our knowledge. For relatively long contacts (> 110 nm), this corresponds to an extremely small R_c of 6.6 ± 1.6 Ω·μm.

4.2 Nano-TLM Measurement and Parameter Extraction

As introduced in Chapter 2, each nano-TLM is a four-terminal test structure so it is measured using the Kelvin measurement scheme, which eliminates the impact of probe and wire resistances. Figure 4-1 illustrates the four possible measurement configurations. The nano-TLM consists of two types of resistances, the parallel resistance $R_{||}$ and cross resistance $R_{\times}$. Therefore, we have four measurements in total by interchanging the ports.

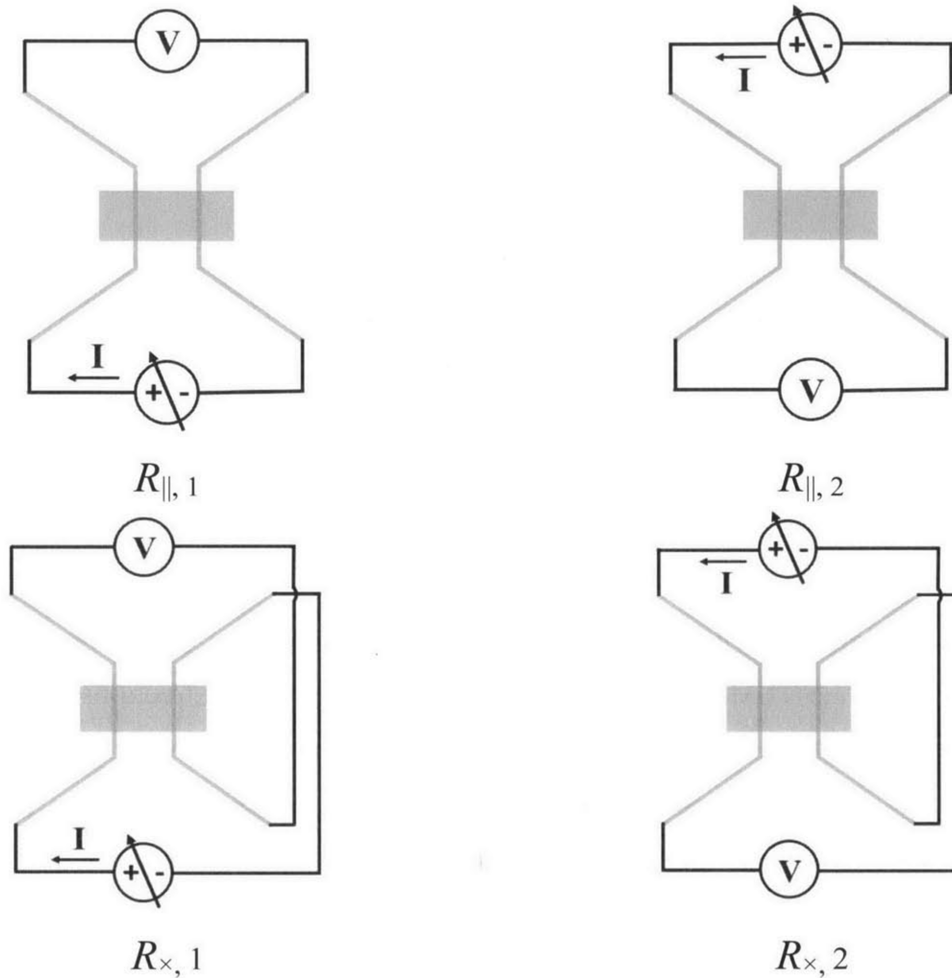


Figure 4-1 Nano-TLM four-terminal measurement schemes.

We use an Agilent 4155A semiconductor parameter analyzer to perform the electrical characterization. As shown in Figure 4-1, a voltage sweep is applied at two terminals, and the injected current is measured at the SMU ports. Then the voltage difference at the other two terminals is measured. Figure 4-2 shows an example of I-V characteristics of a typical nano-TLM. The I-V curve is supposed to be linear for ohmic contact behavior. Then the total resistance R_{tot} ($\Omega \cdot \mu m$) is found by taking the slope of the curve and multiplying by the contact width W. In our experiment, a set of nano-TLM consists of 6 individual nano-TLMs of the same contact length but different contact separations. Therefore, after measuring each of the 6 nano-TLMs, we generate a plot of R_{tot} versus L_d, as shown in Figure 4-3, which is obtained from the data in Figure 4-2. Note that for the cross measurement, the total resistance can be negative due to the metal sheet resistance, as predicted in Section 2.3.1.

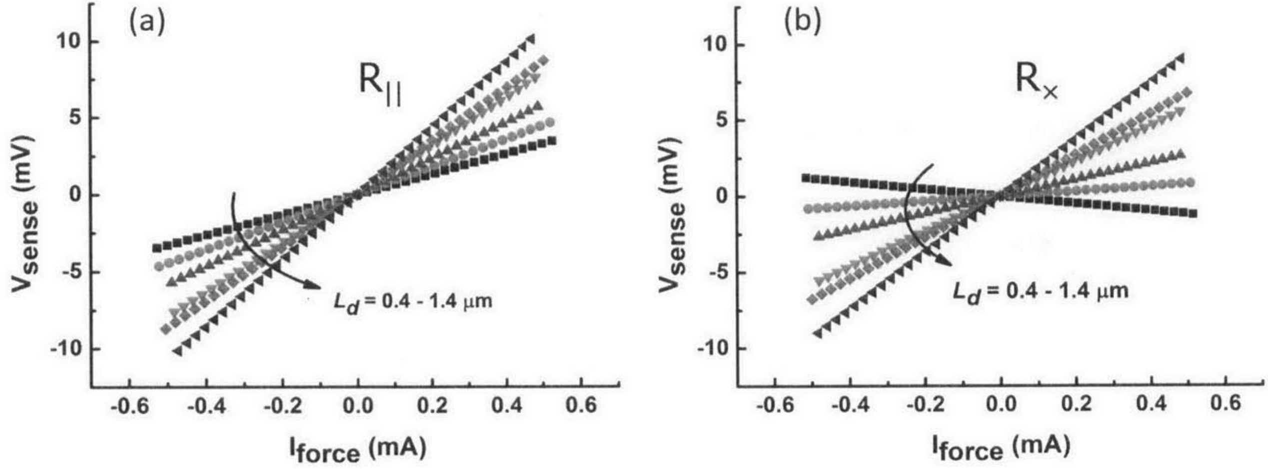


Figure 4-2 I-V characterisitics of nano-TLM of L_c = 96 nm from (a) parallel measurement, and (b) cross measurement.

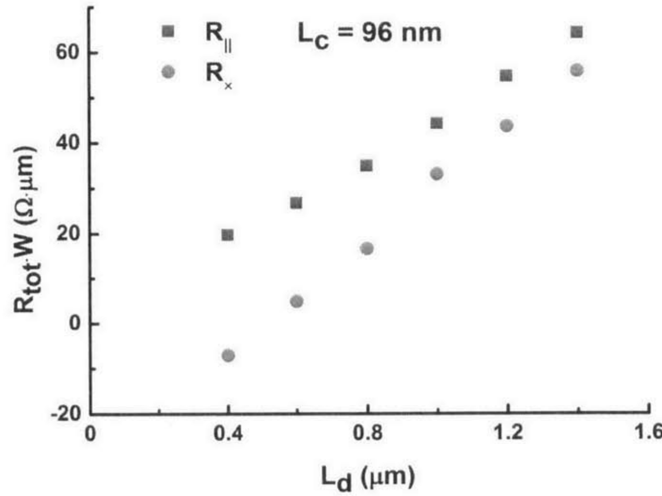


Figure 4-3 Total nano-TLM resistance derived from the I-V measurement.

The nano-TLM model developed in Chapter 2 is then used to extract the parameters: R_c, R_{sh}, and R_{shm}. For each set of 6 nano-TLMs, we use a nonlinear least-square fitting program, implemented in MATLAB, to fit the total resistance data to Equations (28) and (35), assuming the same values of R_c, R_{sh} and R_{shm}. Each set of four data points, $R_{||,1}$, $R_{||,2}$, $R_{\times,1}$ and $R_{\times,2}$ as in Figure 4-1 is fitted simultaneously. In addition, it shall be noted that all relevant dimensions L_c, L_d, and W are measured by SEM. This is critical for sensitive nano-scale contact resistance measurement, because the actual dimensions of nano-TLM are generally different from nominal ones, due to

the proximity effect in lithography and undercut induced by RIE. The extraction results are presented in the following sections.

4.3 Contact Resistance of Mo/n⁺-InGaAs

4.3.1 Contact Resistance

In this section, we report on the contact resistance obtained from our Mo/n^+-$In_{0.53}Ga_{0.47}As$ contact system. As we anticipate the contact resistance to scale with contact length, we fabricate nano-TLMs with L_c ranges from 19 to 450 nm. Figure 4-4 shows the fitting results of three nano-TLM test structures of different L_c of 416, 95, and 19 nm, respectively. It can be observed that the separation of $R_{\parallel}$ and $R_{\times}$ enlarges as L_c decreases, and $R_{\parallel}$ remains positive and larger than $R_{\times}$, which is consistent with the analytical model in Chapter 2, indicating the impact of R_{shm}. Such splitting allows us to extract the metal sheet resistance in order to better determine the contact resistance.

In this experiment, we measured 30 sets of test structures, a collective of 180 nano-TLM devices. For relatively long contacts, having a contact length much larger than the transfer length in the y direction (>113 nm for this contact system), an extremely small $R_c = 6.6 \pm 1.6\ \Omega\cdot\mu m$ is achieved. The average R_{sh} and R_{shm} of all test structures are 54 Ω/□ and 1.2 Ω/□, respectively. To verify the accuracy of our extraction, we also measured R_{sh} and R_{shm} directly from conventional TLMs and Van der Pauw structures elsewhere on the sample. The average discrepancies of R_{sh} and R_{shm} are 10% and 16% across the entire sample.

For all nano-contacts, assuming that $R_{sh} >> R_{shm}$, we can extract the contact resistivity using Equation (8) and (9) as in the standard TLM model. We find that $\rho_c = 0.69 \pm 0.3\ \Omega \cdot \mu m^2$.This the lowest contact resistivity reported for contacts to n^+-InGaAs at $N_D = 1 \cdot 10^{19}\ cm^{-3}$, to the best of our knowledge. Figure 4-5 shows a summary of the contact resistivity of refractory ohmic contacts to n^+-InGaAs in the literature to date, including this work [9]–[11], [13], [23]–[26]. The reference of n^+-Si ohmic contacts is also shown in the plot, as it can be concluded that ohmic contacts to n^+-InGaAs demonstrate superior performance over those to n^+-Si.

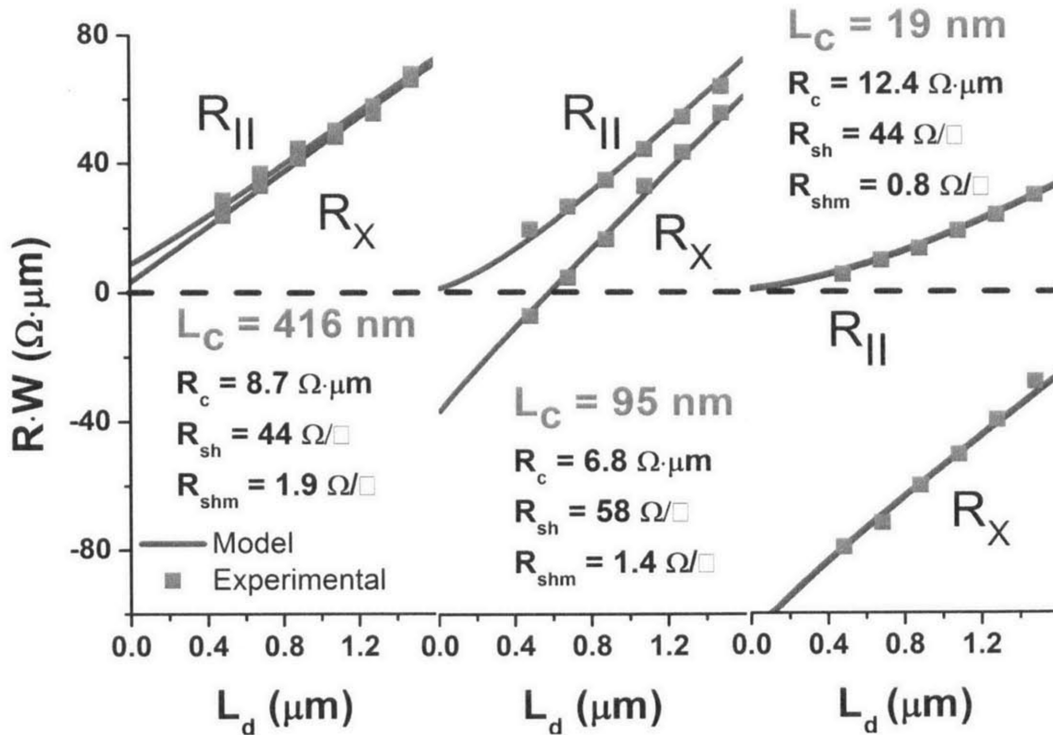


Figure 4-4 $R_{||}$ and $R_\times$ as a function of contact spacing of Mo/n^+-$In_{0.53}Ga_{0.47}As$ nano-TLMs with average contact lengths of 416, 95, and 19 nm.

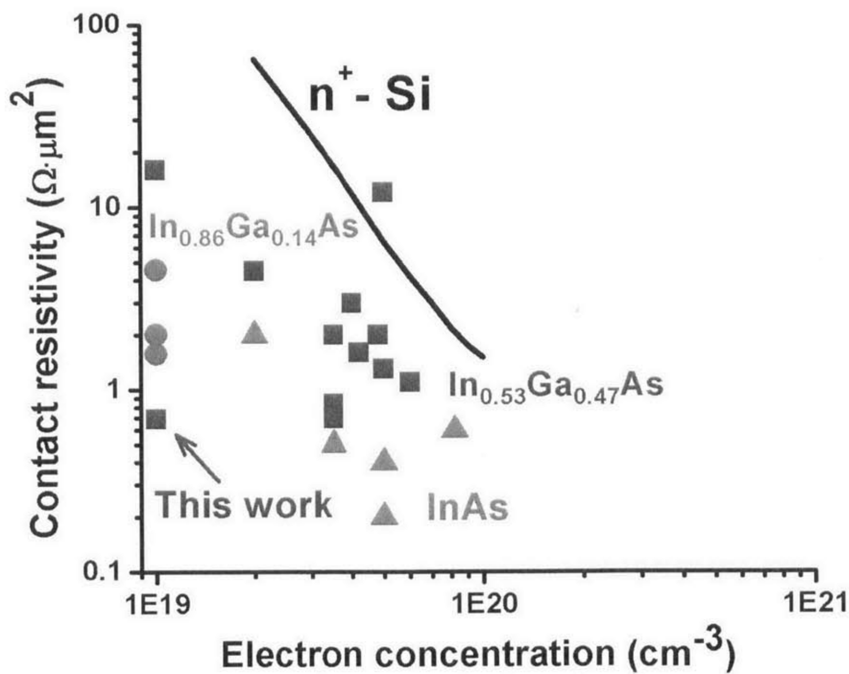


Figure 4-5 Contact resistivity versus electron concentration of state of the art ohmic contacts to n^+-InGaAs to date. The color corresponds to different indium concentration. Literature data from [9]–[11], [13], [23]–[26].

4.3.2 Ohmic Contact Scaling

One of the motivations of fabricating nano-TLMs is to directly characterize how ohmic contacts scale in the nanometer regime. Figure 4-6 shows contact resistance measured in Section 4.3.1 plotted against contact length. Using the average value of $\rho_c = 0.69\ \Omega \cdot \mu m^2, R_{sh} = 54\ \Omega/\square$, the standard TLM model [17] provides an excellent fit with the nano-TLM data for all contact lengths. Indeed, for relatively long contacts, R_c is constant, and it shoots up rapidly as the contact length decreases, as predicted by:

$$R_c = \sqrt{R_{sh} \cdot \rho_c}\coth\left(L_c\sqrt{\frac{R_{sh}}{\rho_c}}\right) \approx \frac{\rho_c}{L_c} \qquad for\ L_c \ll L_{Ty} = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{38}$$

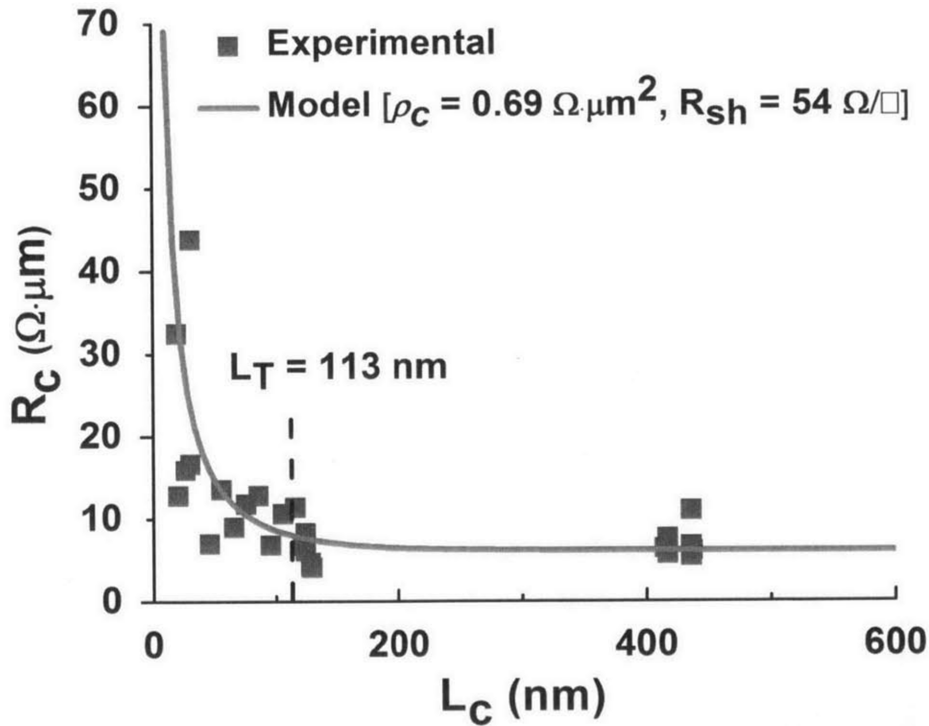


Figure 4-6 Contact resistance versus contact length for Mo/n^+-$In_{0.53}Ga_{0.47}As$ contacts, with an average contact resistivity of $0.69 \pm 0.3\ \Omega \cdot \mu m^2$.

The fact that R_c blows up imposes great challenges to the ohmic contact scaling, as already discussed in Chapter 1. It also shows that the nano-TLM test structure is able to characterize both long contacts and extremely small ones with excellent accuracy. Discrepancies can be attributed

to non-uniformities in heterostructure growth and test structure fabrication, and errors in the SEM measurements.

4.3.3 Thermal Stability

Besides studying the ohmic contact scaling, we also study the effect of thermal annealing of Mo/n^+-$In_{0.53}Ga_{0.47}As$ ohmic contacts. After the nano-TLM fabrication, we measure the test structures, and then do RTA at a relatively low temperature (for example, 250 °C). We then measure the nano-TLMs again, and perform RTA at elevated temperature, and keep doing this until the ohmic contacts start to degrade or the semiconductor seems to decompose. Figure 4-7 shows the contact resistance of Mo/n^+-InGaAs versus annealing temperature. The Mo contacts turn to be thermally stable up to at least 400 °C, in good agreement with [13], [27]. Figure 4-8 shows a FIB (focused ion-beam)-SEM dual-beam image of the cross section of the contact after 400 °C anneal. Unlike most alloyed contacts, the non-alloyed Mo contact has a smooth interface without any diffusion or void.

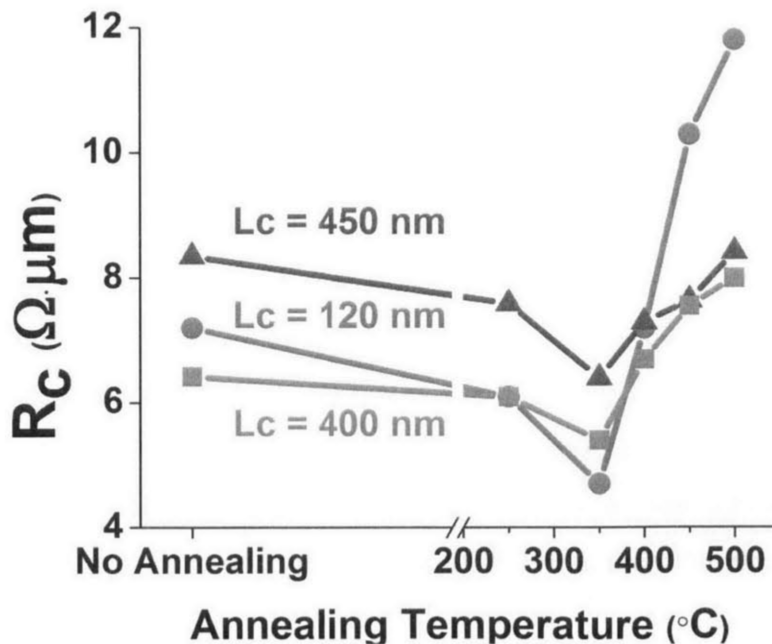


Figure 4-7 Thermal stability of Mo/n^+-$In_{0.53}Ga_{0.47}As$ ohmic contacts.

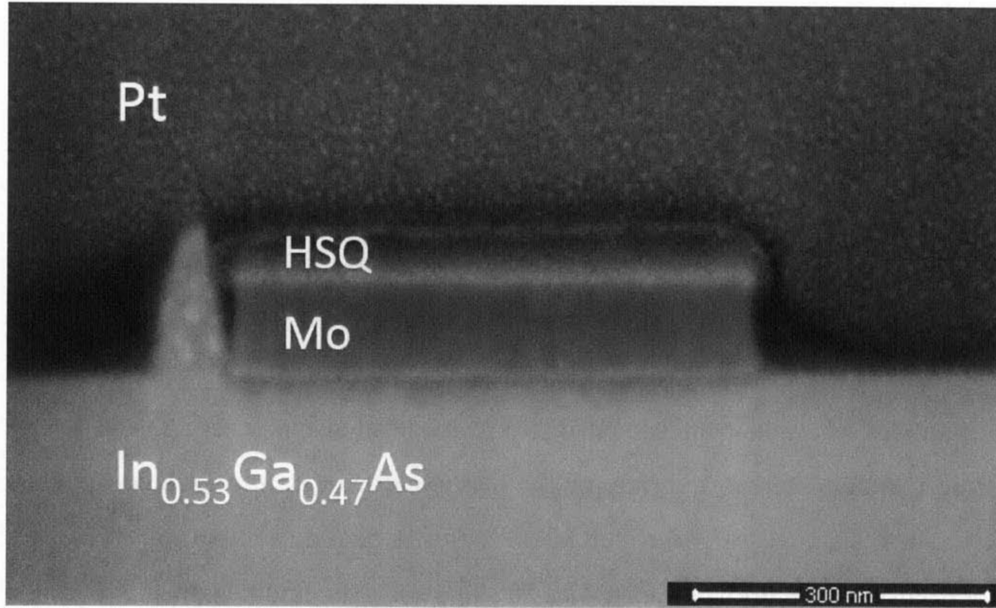


Figure 4-8 FIB-SEM dual-beam image of the cross section of the Mo/n$^+$-$In_{0.53}Ga_{0.47}As$ ohmic contact after 400 °C RTA in N_2 ambient. The triangular feature to the left of the contact structure is an artifact of the ion milling process.

4.3.4 Contact Resistance of the Alternative Process

In Section 3.4, we provide an alternative process to obtain TLM test structures with nano-scale contact length. In this section, we report on the electrical characteristics of this test structure. Due to sample shortage, we use a similar sample as in the nanoTLM process in previous sections. The major difference is that the capping layer has doping concentration of $3 \cdot 10^{19}$ cm^{-3} and thickness of 10 nm. We have obtained contact lengths ranging from 40 nm to 600 nm.

Figure 4-9 plots the total resistance as a function of contact spacing, for structures with contact length of 40 nm. Figure 4-10 shows the evolution of contact resistance as a function of contact length. The entire data set corresponds to R_{sh} = 241±9 Ω/□ and ρ_c = 4.5±0.4 Ω·μm^2, which is 5 times larger than the nano-TLMs fabricated from the same sample. This is likely due to the resist contamination from the alignment mark associated with lift-off before Mo deposition. Also, the 1 hour annealing of the spin-on glass at 350 °C might degrade the contact interface. Both process problems can be optimized to further improve R_c. Nevertheless, this process is effective for its simple parameter extraction, with the tradeoff of a reasonably more complicated process.

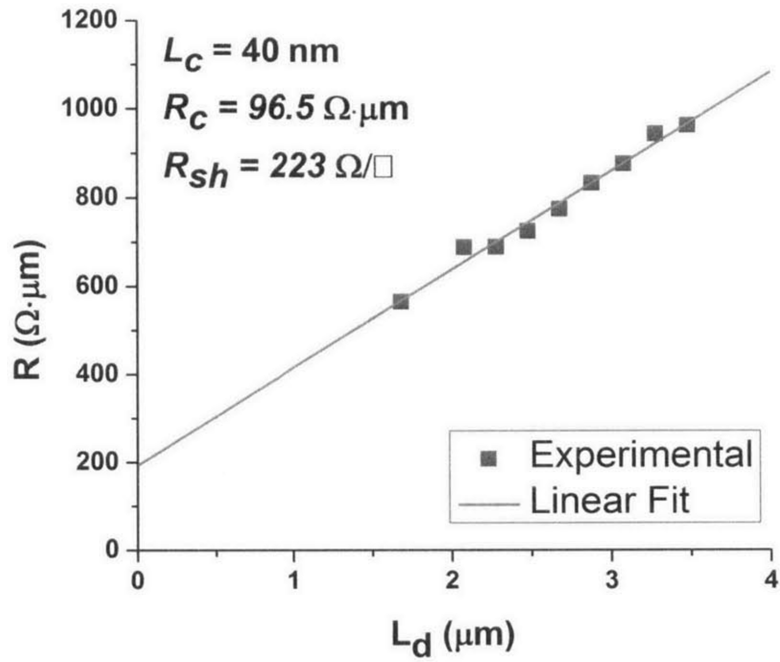


Figure 4-9 Total resistance versus contact spacing for nano-scale TLM fabricated using the alternative process as in Section 3.4.

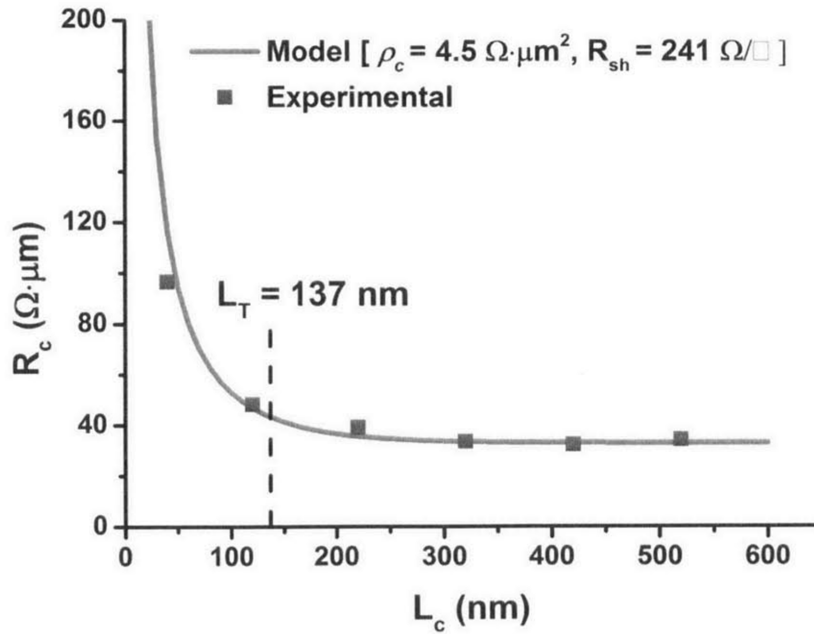


Figure 4-10 Contact resistance versus contact length for Mo/n^+-$In_{0.53}Ga_{0.47}As$ (10 nm, $N_d = 3\times10^{19}$ cm^{-3}) contacts using the alternative process, with an average contact resistivity of 4.5 $\Omega\cdot\mu m^2$.

4.4 Discussion

So far, we have reported the experimental results from the Mo/n$^+$-$In_{0.53}Ga_{0.47}As$ nano-contacts. We obtained a record low contact resistivity from this contact system. The key factors of the low contact resistivity are: (1) low Schottky barrier height (~0.2 eV) of Mo/n$^+$-$In_{0.53}Ga_{0.47}As$ interface [28], [29], (2) we use a contact-first process, and (3) we use sputtered Mo instead of electron-beam evaporated one to produce higher metal quality [30].

In addition to measure the contact resistance, it is also interesting to use the nano-TLM to measure the series resistance from the cap layer to the channel. This requires a cap-recess process, which ought to be done using dry etch instead of wet etch because the metal contact is too narrow to suffer from the undercut induced by wet etch. This is currently being investigated as an extension of this study.

In this study, we focused on n-type nano-TLMs. As described in Section 1.2.2, there is a need for both n-type and p-type high quality ohmic contacts. Figure 4-11 demonstrates our preliminary results on Ni/p$^+$-GaAsSb (N_A = $2 \cdot 10^{19}$ cm^{-3}) ohmic contacts, which shows promising contact resistance of 72 Ω·µm and contact resistivity of $3.2 \cdot 10^{-6}$ Ω·cm^2. Table 4-1 summarizes different metal/p$^+$-antimonide-based semiconductor ohmic contacts that we have investigated or reported in literature. Because we are lack of full understanding of p-type contact systems, we used conventional TLMs instead of nano-TLMs.

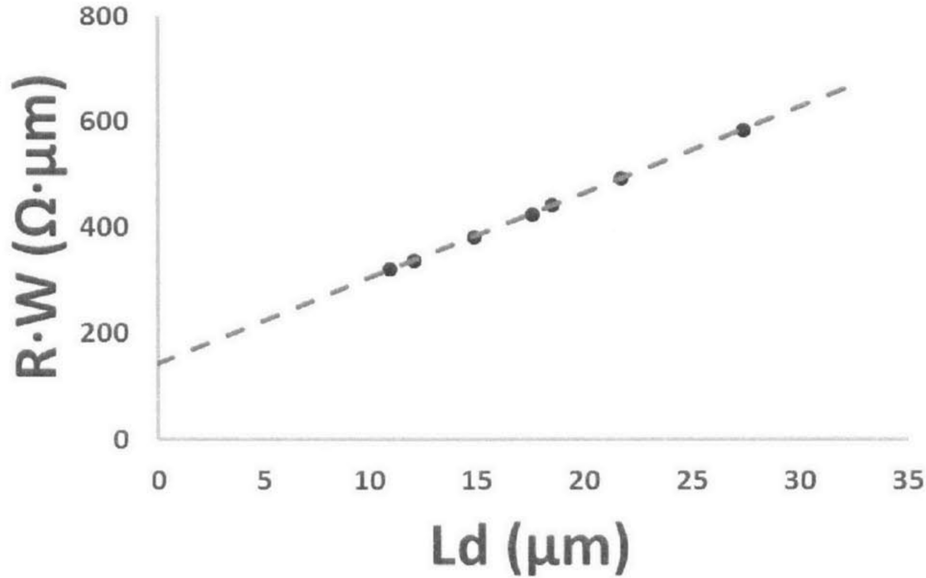


Figure 4-11 TLM measurement of Ni/p$^+$-GaAsSb contacts.

Semiconductor	Metal	N_A (cm^{-3})	R_c (Ω·µm)	ρ_c (Ω·cm^2)	Reference
InAs	Pd/Pt/Au	$2\cdot10^{19}$	N/A	$1.6\cdot10^{-6}$	[31]
	Ni/Pt/Au	$1\cdot10^{19}$	7.7	$5.6\cdot10^{-6}$	This work
GaSb	Ti/Pt/Au	$6.6\cdot10^{19}$	N/A	$5.8\cdot10^{-6}$	[32]
	Ni/Au	$6.2\cdot10^{19}$	N/A	$1\cdot10^{-5}$-$3\cdot10^{-5}$	[33]
	Pd/Au	$6.2\cdot10^{19}$	N/A	$3\cdot10^{-7}$-$3\cdot10^{-6}$	[33]
	Ni/Pt/Au	$2\cdot10^{19}$	8.5	$7.8\cdot10^{-6}$	This work
GaAsSb	Ni/Pt/Au	$2\cdot10^{19}$	72	$3.3\cdot10^{-6}$	This work
InGaSb	Pd/W/Au	$1.8\cdot10^{19}$	80	$3\cdot10^{-7}$	[34]
InAlSb/InAs	Pd/Pt/Au	N/A	70	$1.6\cdot10^{-7}$	[35]

Table 4-1 Summary of state-of-the-art ohmic contacts to p-type antimony-based III-V semiconductor.

4.5 Summary

In this chapter, we reported on the experimental results of nano-TLM measurement. We showed that the nano-TLM test structure is capable of accurately extracting the contact resistance, semiconductor sheet resistance, and metal sheet resistance. From the Mo/n$^+$-$In_{0.53}Ga_{0.47}As$ ohmic

contacts, we obtained a record low contact resistivity of $\rho_c = 0.69 \pm 0.3\ \Omega \cdot \mu m^2$, which is close to the requirement for future nanometer-scale CMOS. Also, using nano-TLMs, we described how the contact resistance scales with contact length, from the entire data set of contact lengths in the 19-450 nm range. We also reported on the thermal stability of this contact system. We concluded that the nano-TLM measurement demonstrates good match to the analytical model developed in Chapter 2, and this technique is suitable for the future generation of III-V MOSFET technology.

CHAPTER 5. CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this thesis work, a novel test structure, nano-TLM, is proposed to characterize the electrical properties of nano-scale ohmic contacts for future III-V CMOS technology. Using a 2-D distributed circuit network, we developed an analytic model for the nano-TLM test structure. Unlike the conventional TLM, two types of Kelvin measurements are possible for nano-TLM. This allows the extraction of the contact resistance, the semiconductor sheet resistance, and the metal sheet resistance at the same time. We also developed a fabrication process to demonstrate this technique in Mo/n^+-$In_{0.53}Ga_{0.47}As$ contacts. We demonstrates nano-contacts with contact lengths range from 19 to 450 nm, where we have obtained an extremely low average contact resistivity of $0.69 \pm 0.3\ \Omega\cdot\mu m^2$. For long contacts, this corresponds to a contact resistance of $6.6 \pm 1.6\ \Omega\cdot\mu m$, which matches the state-of-the-art in the Mo/n^+-InGaAs system. Nano-TLM measurement successfully illustrates for the first time how contact resistance scales with contact length.

Although we have only demonstrated this technique in one ohmic contact system, we expect that the nano-TLM is versatile and can be easily applied to other material systems. We conclude that this novel test structure can be integrated into the process of next generation high-performance III-V MOSFETs.

5.2 Suggestions for Future Work

To conclude this thesis, we list here some suggestions and possibilities for future studies that could be carried out as useful extension of this research.

1. Use the nano-TLM test structure to characterize p-type ohmic contacts, which are as important as their n-type counterpart but much more lacking in understanding.

2. Apply the nano-TLM test structures to other types of ohmic contacts, such as alloyed contacts or ion-implanted contacts.

3. Dry etch the cap layer between nano-contacts to measure the series resistance which includes both the contact resistance and the cap-to-channel resistance. This is of great interests as it allows us to decompose and measure each component of the source and drain resistance in a MOSFET. Because the cap layer is usually very thin (~10 nm) and the nano-contact is narrow, the RIE needs to be slow, precisely controllable and highly anisotropic.

4. Extend the nano-TLM test structure, which is designed for planar devices, to nano-fin-TLM, which can be used to characterize contacts of FinFETs or other non-planar device structures.

5. Incorporate the nano-TLM process into actual InGaAs nMOSFET fabrication.

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