SiGe Virtual Substrate Engineering for Integration of III-V Materials, Microelectromechanical Systems, and Strained Silicon MOSFETs with Silicon

by

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ABSTRACT

SiGe virtual substrates are versatile platforms with which the performance and functionality of Si-based microelectronic systems can be extended. In this thesis, the physical and electronic properties of relaxed SiGe are utilized to create novel heterostructures and electronic devices. The results demonstrate the great promise inherent in the use of relaxed SiGe in future system-on-a-chip solutions.

The materials quality of SiGe virtual substrates degrades upon grading to high Ge concentrations due to the formation of threading dislocation pileups. A two-part strategy for the control and elimination of these pileups is proposed and utilized to fabricate relaxed SiGe layers of unprecedented quality on Si. The combination of growth on offcut Si substrates and intermediate planarization steps allows graded SiGe layers of arbitrary final Ge content to be grown with threading dislocation densities lower than 10^6 cm^{-2}. Virtual substrates graded to 100% Ge content have been used to demonstrate the monolithic integration of GaAs-based materials and devices on Si. Record minority carrier lifetimes for GaAs on Si have been achieved, demonstrating the feasibility and promise of III-V-based electronic and optoelectronic devices integrated with Si.

Undoped relaxed SiGe layers of Ge contents greater than 20% display superior etch stop performance in wet Si etchants utilized in the formation of microelectromechanical systems (MEMS). These undoped layers are also ideal for the integration of on-chip electronic devices. SiGe layer structures have been designed and utilized in the production of MEMS devices. Several manufacturing obstacles to a move to relaxed SiGe for MEMS, such as wafer curvature, part curvature, and part strain, have been identified and resolved.

SiGe virtual substrates are also utilized in the fabrication of strained Si metal-oxide-semiconductor field-effect transistors (MOSFETs). The biaxial tensile strain in Si layers grown on relaxed SiGe enhances the innate carrier mobilities of Si, enabling the production of enhanced performance devices. N- and p-channel strained Si MOSFETs are fabricated via a novel short-flow process with a deposited gate oxide and a single photolithography step. The effects of strain and channel thickness on device mobilities are investigated. In agreement with theoretical predictions, different mobility

enhancement saturation behaviors are observed for strained Si n- and p-MOSFETs. The process stability of strained Si devices is also studied. The effects of wafer planarization via chemical-mechanical polishing (CMP) and enhanced thermal budgets on the MOSFET mobilities are examined. Strained Si devices are fabricated on virtual substrates of negligible surface roughness for the first time. The mobility enhancements of these devices are virtually identical to those of devices on unplanarized SiGe substrates. The effects of Ge interdiffusion explain the mobility degradation of strained Si MOSFETs annealed at temperatures over 1000°C. These results demonstrate the great promise of strained Si devices and suggest a path for future investigations.

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Matthew Currie
Cambridge, MA
January 2001

Chapter 1

Introduction and Background

1.1 Motivation for a SiGe-Based Integration Platform

From the invention of the modern monolithic integrated circuit by Robert Noyce in 1960 to the production of the complex microprocessors of today, increased levels of integration have led to the massive success of the Si microelectronics industry[1]. SiGe alloys present one way of extending the performance and functionality of the Si-based microelectronics platform. The larger lattice parameter of the SiGe alloy enables the monolithic integration of Ge, SiGe, and III-V materials and devices with Si. The unique etch-stop properties of SiGe allow the fabrication of novel microelectromechanical systems (MEMS). Strained Si and SiGe layers can be used to increase the carrier mobilities of Si, enabling higher speed electronics with lower power consumption. The combination of any or all of these SiGe-based technologies could lead to ultimate system-on-a-chip solutions in the future. However, several materials challenges remain before such solutions can be realized. These include the effects of the lattice and thermal mismatch between Si and Ge and the surface roughness of SiGe films.

1.2 Strained and Relaxed SiGe on Si

The physical and electronic properties of strained and relaxed SiGe form the framework by which the Si microelectronics platform can be extended. The larger lattice parameter of relaxed SiGe alloys provides a template for the heterointegration of the larger III-V materials, as well as the means for introducing tensile strain into Si itself. The electronic properties of thin strained Si and SiGe layers can be utilized in the design of high

performance microelectronic devices. The unique etch stop properties of undoped relaxed SiGe, which are related to its energy band structure, enable the fabrication of SiGe-based MEMS devices. Perhaps even more importantly, with the average cost of a Si microelectronic fabrication plant rising to beyond 10 billion dollars in less than 10 years, the economic pressure to utilize existing infrastructure is immense[2]. Since SiGe technology is inherently compatible with mainstream Si very large scale integration (VLSI) fabrication techniques, it can extend the performance of Si in an economically feasible manner.

1.2.1 Lattice Parameter of SiGe Alloys

Si and Ge are completely miscible over the entire composition range, as shown in the phase diagram of Figure 1.1. Although this makes the reproducible, economical bulk crystal growth of particular SiGe alloys impossible in practice, SiGe alloy layers fabricated via vapor phase epitaxy are robust and immune to phase segregation[3]. To first order, the lattice constant of a SiGe alloy can be determined from the Vegard's Law[4] linear interpolation between the lattice constants of Si and Ge:

$$a_{SiGe} = a_{Si} + (a_{Ge} - a_{Si})x$$

where a_{Si} = 5.428 Å, a_{Ge} = 5.658 Å, and x is the Ge content of the alloy. High resolution X-ray diffraction studies have shown that the lattice parameter of the alloy is slightly smaller than this approximation, but the deviation is less that 0.2%[5].

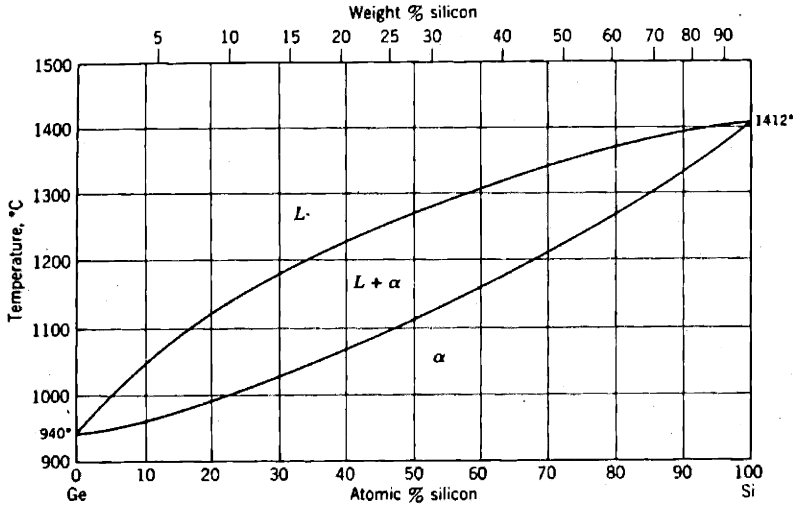

Figure 1.1 The SiGe binary phase diagram. Si and Ge are completely miscible over the entire composition range. Image from Ghandhi [6].

1.2.2 Lattice Mismatch and Dislocation Formation

SiGe alloys have a larger lattice parameter than Si, and epitaxial SiGe deposited on Si will initially be pseudomorphically strained to the substrate. The SiGe lattice is tetragonally distorted as its in-plane lattice constant matches that of Si. As the thickness of the deposited film increases, the misfit strain energy stored in the film increases as well. At a certain film thickness, termed the critical thickness, the introduction of misfit dislocations to relieve the lattice mismatch becomes energetically favorable[7]. This phenomenon is illustrated in Figure 1.2, in which misfit dislocations are present at the film/substrate interface and the film has relaxed to its equilibrium lattice constant.

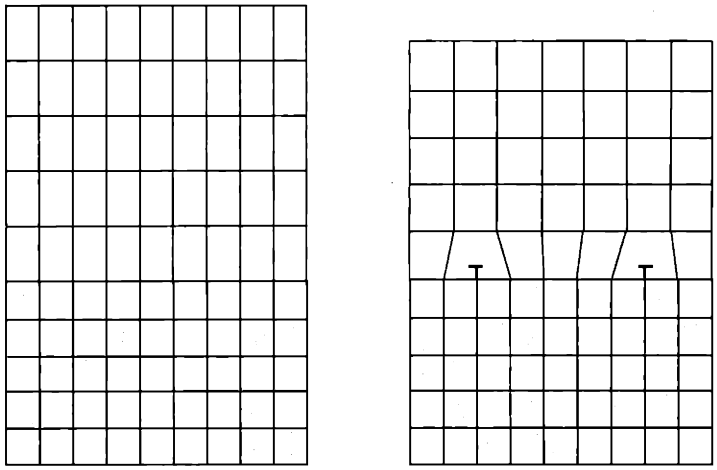

Figure 1.2 **Relaxation of a mismatched heteroepitaxial film. The film is initially pseudomorphically strained to the substrate lattice parameter *(left)*. When the layer thickness exceeds the critical thickness, misfit dislocations provide strain relief *(right)*.**

The expression for the critical thickness h_c is given by:

$$h_c = \frac{D(1-\nu\cos^2\alpha)(b/b_{eff})\left[\ln\left(\frac{h_c}{b}\right)+1\right]}{2Yf}$$

where D is the average shear modulus at the interface, ν is Poisson's ratio, α is the angle between the Burgers vector b and the dislocation line direction, b_{eff} is the in-plane component of the Burgers vector, Y is the biaxial Young's modulus of the film, and f is the mismatch between the film and the substrate[8]. The reader is directed to Ref. 8 for a thorough treatment of the critical thickness in strained layer epitaxy. In practice, the observed critical thickness is larger than that predicted by this thermodynamic model. Because dislocation nucleation and glide are thermally activated processes, dislocation-free films can be grown at low temperatures to thicknesses far beyond the predicted critical thickness. These films are metastable, and may relax via misfit dislocation

introduction if heated to temperatures beyond the growth temperature, limiting their usefulness in practice. Figure 1.3 shows the observed metastable critical thicknesses for SiGe layers grown on Si at 500°C compared with the thermodynamic model of Matthews and Blakeslee[9].

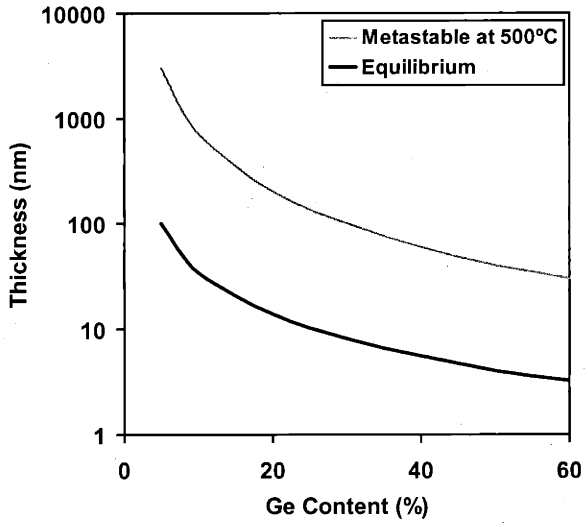

Figure 1.3 Equilibrium and metastable critical thicknesses for SiGe layers grown on Si substrates. Metastable values are for growth at 500°C.

Both Si and Ge have the diamond cubic crystal structure, and hence have the {111}<110> slip system. Therefore, the misfit dislocations formed to relieve lattice mismatch will form an orthogonal array along the in-plane <110> directions on a (100) surface. The dislocations most often observed in low-mismatch SiGe heteroepitaxy are the 60° dislocations, named for the 60° angle formed between their Burgers vector and the interface line direction. The 60° dislocations glide on the {111} planes to provide relief from mismatch strain. Pure edge dislocations, with Burgers vectors perpendicular to the line direction, would provide more efficient strain relief but are sessile in this

crystal system. However, in cases of large lattice mismatch such as the direct growth of Ge or GaAs on Si, a high density of pure edge dislocations is observed in the relaxed layer[8].

Dislocations cannot terminate within a crystal, so the strain-relieving misfit dislocations that do not terminate at the wafer edge or on other dislocations are always accompanied by segments that thread to the film surface. These segments are termed threading dislocations and are illustrated in Figure 1.4. The threading dislocations glide to relieve mismatch strain, leaving increasing lengths of misfit dislocations in their wake. High densities of threading dislocations can wreak havoc with the operation of semiconductor devices. They act as non-radiative recombination sites and as nucleation sites for dark line defects, creating reliability problems in light-emitting diodes (LEDs) and lasers. Threading dislocations can lead to increased junction leakage and act as fast diffusion "pipes" for dopant species. At the highest densities, threading dislocations can scatter carriers, decreasing carrier mobilities for majority carrier devices such as field-effect transistors (FETs). Thus, the control and reduction of threading dislocation density is the foremost issue faced in the field of mismatched epitaxy.

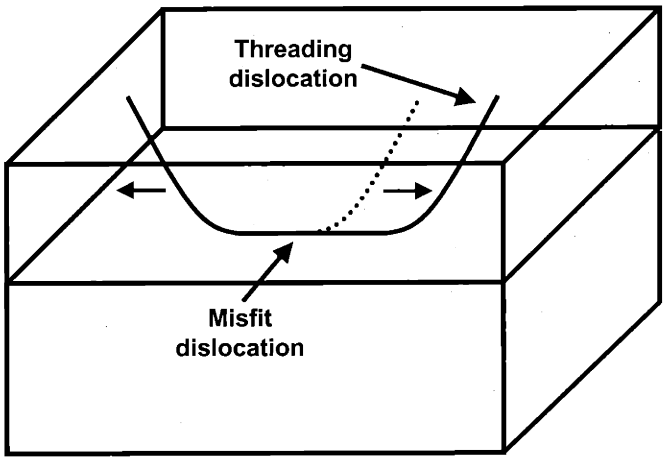

Figure 1.4 Schematic of misfit and threading dislocations in mismatched heteroepitaxy.

1.3 Control of Threading Dislocation Density

Direct heteroepitaxial growth of highly mismatched layers, such as Ge or GaAs on Si, results in high densities of threading dislocations. The large amount of mismatch strain necessitates rampant dislocation nucleation in order to relieve this high strain level. Final threading dislocation densities can reach levels beyond 10^9-10^{10} cm^{-2} in these films, rendering them unsuitable for reliable operation of most electronic devices. In fact, most semiconductor lasers demand threading dislocation densities of 10^3 cm^{-2} or lower for reliable operation. The generally accepted limit for LEDs and majority carrier devices is higher, in the 10^5-10^6 cm^{-2} range. Indeed, the National Technology Roadmap for Semiconductors places the upper limit for threading dislocation density in silicon-on-insulator (SOI) substrates for advanced microelectronics in the 10^6 cm^{-2} range[10]. Thus, many strategies for the reduction of threading dislocation density in heteroepitaxial layers have been proposed and attempted, with varying amounts of success.

1.3.1 Post-Nucleation Dislocation Density Reduction

As a threading dislocation glides through a heteroepitaxial layer to relieve mismatch strain, the possibility exists for it to encounter another dislocation of the appropriate Burgers vector and annihilate. Some techniques for the control of threading dislocation density have attempted to take advantage of this fact. First among these is the simple growth of thick uniform buffer layers. When a uniform heteroepitaxial layer is grown, dislocations nucleate and will glide to relieve the mismatch strain. When this strain is large, dislocation nucleation dominates the process, resulting in a high threading dislocation density and short misfit dislocation lengths at the interface. After the layer relaxes to its equilibrium lattice constant, dislocation glide stops, and the dislocations are left threading through the film to the surface. Because many of these dislocations thread up at an angle to the substrate, growth of additional buffer thickness will, in effect, move these threads in relation to each other. As the buffer thickness increases, the probability of favorable dislocation annihilation events increases, decreasing the threading dislocation density. A similar technique relies upon the fact that heteroepitaxial films often have different thermal expansion coefficients than the substrate. Thermal mismatch strain, which can cause dislocation glide, can result from thermal cycling of such layers. Again, the more the film is thermally cycled, the higher the probability of threading dislocation annihilation events. Unfortunately, both of these techniques tend to be victims of their own success. As the threading dislocation density is decreased, so does the probability of further successful dislocation interactions. For this reason, threading dislocation density reduction below the 10^7 cm^{-2} level is unlikely with these techniques[11].

1.3.2 *Relaxed Graded Buffer Technology*

The most successful and proven technique for the production of highly mismatched semiconductor epilayers with low threading dislocation densities is the relaxed graded buffer. First employed in the SiGe materials system by Fitzgerald, *et al.* in 1991[12,13], the relaxed graded buffer operates on a straightforward premise: maintain a low strain state to prevent rampant dislocation nucleation while maintaining a high growth temperature to maximize dislocation glide. Thus, the highly mismatched target layer is approached gradually via the deposition of many layers of low lattice mismatch. Each layer in the buffer relaxes to its intermediate lattice constant, and a low strain state is maintained throughout, minimizing dislocation nucleation. Additionally, threading dislocations from previous layers are "reused" at each subsequent interface as they glide to create misfit dislocations. A high growth temperature is utilized to maximize the glide length of each threading dislocation at each interface, obviating the need for additional dislocations for strain relief. In the ideal case, the threading dislocations created during the very first layer of the graded buffer can be reused to relax every layer up to the desired final composition. This results in a steady-state threading dislocation density independent of the final Ge concentration of the SiGe graded buffer. Figure 1.5 illustrates this recycling of threading dislocations in the graded buffer.

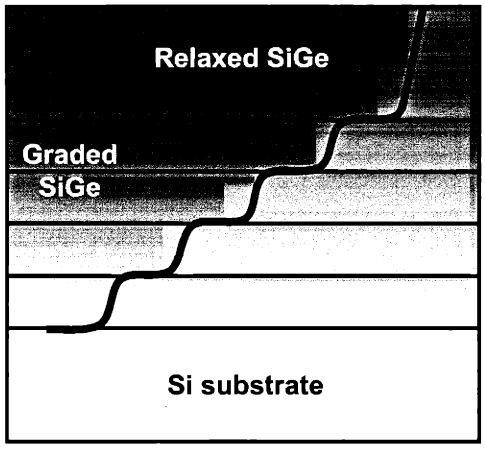

Figure 1.5 Schematic of a relaxed graded buffer. Threading dislocations from initial layers glide to relieve strain at subsequent mismatched interfaces.

In practice, maintaining a steady-state threading dislocation density becomes difficult when grading to highly mismatched layers with high Ge contents, as will be discussed later in this document. The relaxed graded buffer technique has been successfully used to control threading dislocation densities in the SiGe/Si, InGaAs/GaAs[14], and the InGaP/GaP[15] materials systems. Often, a successfully produced graded buffer acts as a template for heteroepitaxial growth not possible with the more conventional Si, GaAs, or InP substrates. This application of a relaxed graded buffer provides the motivation for its alternate moniker—the virtual substrate. Virtual substrates have been used to integrate dissimilar materials and create novel electronic and optoelectronic devices previously impossible to fabricate.

1.4 Integration of III-V Materials and Devices with Silicon

Si wafers are strong, light, and nearly defect-free at diameters of 12 inches. Si is also blessed with a sturdy, passivating oxide that facilitates device operation and isolation. These benefits have allowed low-cost Si CMOS technology to dominate the worldwide microelectronics industry. However, Si does possess a few disadvantages. It is an indirect bandgap semiconductor, rendering the operation of light-emitting devices nearly impossible. Si is also saddled with relatively low carrier mobilities, particularly that of the hole. For these reasons, the integration of III-V semiconductors with Si has long been a goal of research. The successful coupling of faster, light-emitting III-V materials with mature, large-scale Si CMOS would lead to production of novel optoelectronics and usher in a new era in the semiconductor industry. Unfortunately, attempts to date have relied upon costly hybrid mounting schemes because the successful monolithic integration of III-V materials with Si faces a few key materials challenges.

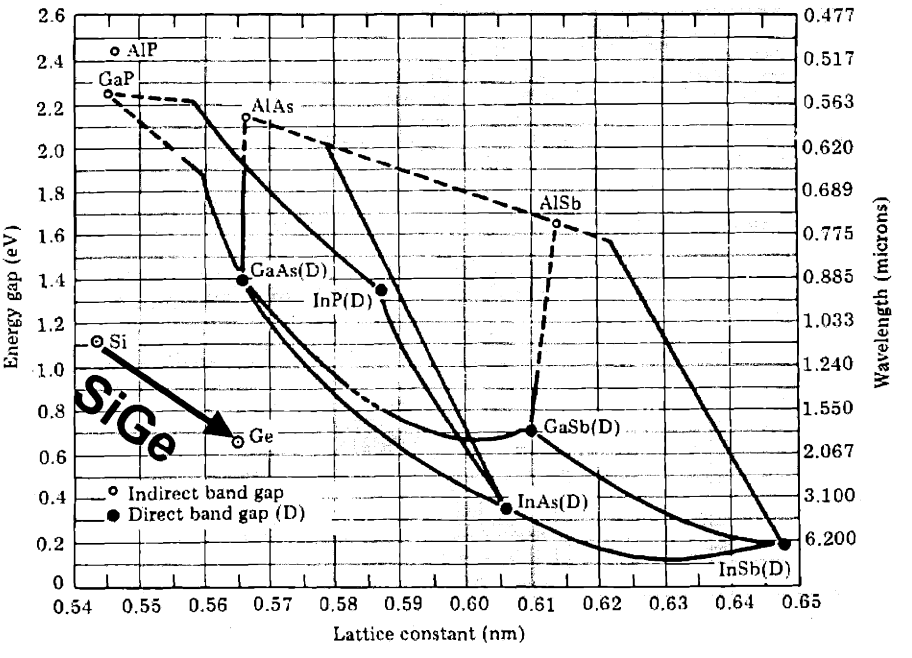

Figure 1.6 The lattice constant vs. energy gap diagram for group IV and III-V semiconductors. SiGe alloy lattice constants span the gap between Si and GaAs. Image from Mayer and Lau[16]

Figure 1.6 shows the lattice constants and bandgaps of several semiconductor materials. The large lattice mismatch between Si and GaAs is the foremost problem facing integration attempts. As discussed previously, direct growth of GaAs on Si can result in threading dislocation densities on the order of 10^{10} cm^{-2}, rendering the material useless for device applications. Note however that GaAs is nearly lattice-matched with Ge. In fact, GaAs-based solar cells for space applications are routinely fabricated on Ge substrates because they are larger, stronger, and lighter than GaAs substrates. InGaAs/InAlAs metamorphic high electron mobility transistors (HEMTs) have also been successfully fabricated on Ge substrates[17]. These HEMTs display identical mobilities to devices grown on GaAs substrates. Substantial research has been performed on the

optimization of this GaAs/Ge growth interface, and the minimization of cross-diffusion and elimination of antiphase domains have been demonstrated[18]. Thus, provided with a SiGe virtual substrate graded to 100% Ge content with low threading dislocation density, one could transfer the advantages of GaAs-based materials to the Si platform. Not only is Si lighter, stronger, and more thermally conductive than GaAs, but much larger wafers of Si are available. Successful integration of GaAs with Si would instantly result in availability of GaAs wafers sized 8 inches and above. Other challenges to successful GaAs/Si integration, including thermal expansion mismatch, dislocation pile-up formation, and surface roughness will be described later. As proof of this concept, InGaP-based LEDs have been successfully integrated with Si via a SiGe virtual substrate[19].

1.5 Integration of Novel MEMS Devices with Silicon

The term microelectromechanical systems (MEMS) encompasses a steadily growing group of microscopic sensors, actuators, and other systems that are fabricated using many of the same techniques as microelectronic devices. For this reason, single crystal Si has become the dominant material in the MEMS community as Si VLSI knowledge has been leveraged into this emerging field. During the fabrication of MEMS devices, complex structures such as proof masses, turbines, and drug delivery systems are etched from Si wafers. Hence, reliable Si etch stops are often required in order to achieve the maximum reliability and reproducibility in a MEMS fabrication process. Currently, etch stops for dissolved Si wafer processes are produced by diffusion of boron into the substrate at concentrations near the solid solubility limit. Although such etch-stops contain

gradations in boron concentration, misfit dislocation density, and other defects, boron concentrations of greater than 7×10^{19} cm^{-3} provide very high etch selectivity in wet Si etchants such as ethylenediamine pyrocatechol (EDP) or potassium hydroxide (KOH). However, boron-diffused etch stops have a number of disadvantages. The use of a diffusion process sets an upper bound on the thickness of the micromachined layer, and also creates difficulties if the MEMS process is to be integrated with other Si microelectronics. Neither sensor structures requiring p-n junctions nor CMOS devices can be integrated on such material[20]. In addition, the gradient in defects in diffused layers can lead to curvature of the micromachined parts that must be remedied by further high temperature annealing. Furthermore, the highest selectivity etchant for boron-diffused Si is the highly toxic EDP, which presents environmental and health-related concerns about the fabrication process. An ideal replacement for heavily boron-doped Si would have no reliance on doping in order to facilitate integration of other Si microelectronic technologies. It would also have very high etch selectivity to more benign Si etchants such as KOH or tetramethyl ammonium hydroxide (TMAH).

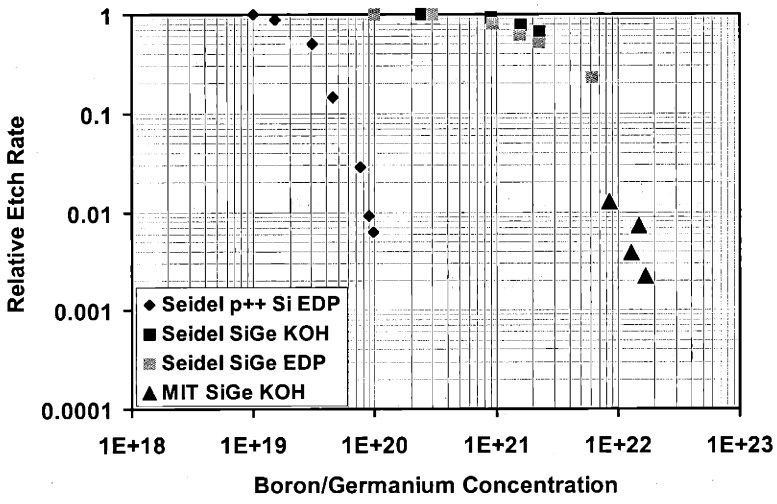

Figure 1.7 Relative etch rates of boron-doped Si and undoped relaxed SiGe in KOH and EDP. Rates are relative to the etch rate of undoped Si, approximately 18 μm/hr.

Relaxed SiGe layers have proven to be good candidates for etch stops for Si micromachining. Figure 1.7 shows a comparison of the etch selectivity of boron-doped Si and relaxed SiGe layers in KOH and EDP[21]. The MIT SiGe samples are compared with previous work by Siedel[22], who found no significant etch stop behavior for Ge concentrations up to 12%. The 30% Ge content SiGe sample displays higher etch selectivity than any of the boron-doped Si samples. The similarity of the etch rate dependence on dopant or Ge concentration suggests a similarity in the etch stop mechanism in these two types of samples. The exponential drop in etch rate with boron concentration suggests an etch stop mechanism highly dependent on the Fermi level position of the material. The commonly accepted explanation for the etch stop mechanism in p^{++} Si samples states that the high boron doping level allows tunneling of

holes from the Si to the electrolyte. These holes feed an oxidation process at the interface of the Si with the etchant:

$$Si\cdots Si + OH^- + h^+ \Rightarrow Si\cdots O\cdots Si + \frac{1}{2}H_2.$$

High boron concentrations lead to high hole injection at the interface, which in turn results in a passivating oxide being formed on the Si surface[23,24]. It is this oxide layer that prevents the etching of heavily boron doped Si in etchants such as KOH. Since the etch rate dependence is qualitatively similar in the case of relaxed SiGe samples, a similar band structure model has been proposed for SiGe etch stops[21]. Figure 1.8 displays a qualitative comparison of the band alignments of Si and SiGe in the etchant. It is obvious from the band diagram that the addition of Ge into the Si reduces both the band-bending and the potential barrier for hole injection into the electrolyte. This is due to the fact that both the bandgap E_g and the electron affinity χ are decreased with the addition of Ge. These effects have been exaggerated in the figure for clarity. At Ge concentrations of approximately 20%, the hole barrier is decreased enough to allow the formation of the passivating oxide layer as in the boron-doped Si case above.

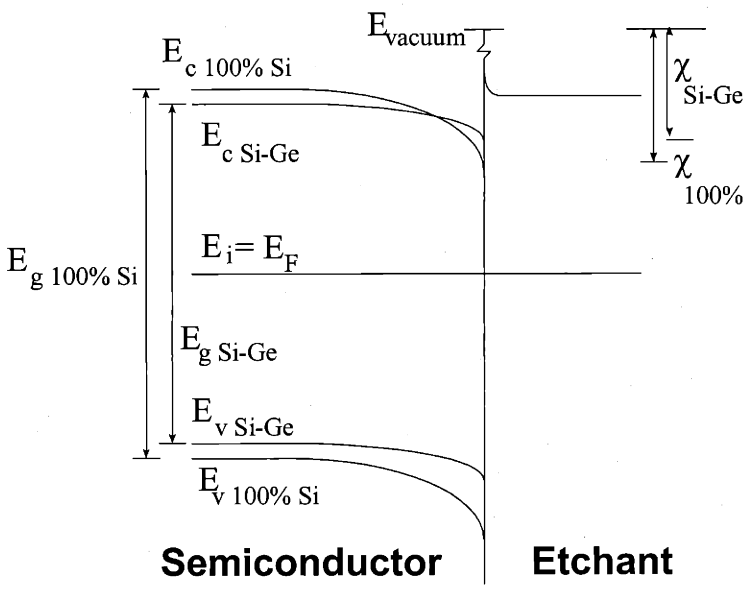

Figure 1.8 **Qualitative comparison of the band alignments of Si and relaxed SiGe with the etchant. The effect of adding Ge has been exaggerated to emphasize the decreased bandgap and electron affinity. The passivating oxide layer forms as the barrier to hole injection from the semiconductor decreases, slowing the etch.**

Since the etch stop mechanism for relaxed SiGe does not rely upon doping in the material, MEMS devices can be integrated with conventional Si electronics more easily. SiGe layers could be grown and released in selected areas and interfaced with control circuitry to produce integrated MEMS devices on a single chip. Therefore, the design and growth of SiGe layers for MEMS processing, as well as fabrication of actual parts, are required to demonstrate the capabilities of relaxed SiGe as a MEMS material.

1.6 Fabrication of High Performance Transistors

Advances in the growth of SiGe and SiGe virtual substrates have also enabled the fabrication of high speed Si-based transistors. Although Si CMOS has come to dominate

the microelectronics spectrum due to its many processing advantages, Si does possess lower carrier mobilities than many other semiconductors. The bulk mobilities of Si are compared with those of other materials in Table 1.1. Changes in these carrier mobilities can directly impact the performance of electronic devices. SiGe technology has enabled changes to be made in the carrier mobilities of the Si platform via the use of strain and the addition of Ge.

Material	Electron Mobility ($cm^2/V \cdot s$)	Hole Mobility ($cm^2/V \cdot s$)
Si	1900	500
Ge	3800	1820
GaAs	8800	400
InP	4600	150
InAs	33000	460
GaSb	4000	1400

Table 1.1 Average bulk carrier mobilities of several group IV and III-V semiconductors at room temperature.

The semiconductor carrier mobility μ can be described by:

$$\mu = \frac{e\tau}{m^*}$$

where τ is the scattering time constant and m^* is the carrier effective mass. Therefore, carrier mobility can be increased by either increasing the scattering time or decreasing the effective mass. Both factors come into play in the design of high performance SiGe-based transistors.

1.6.1 Bandgap of SiGe Alloys

The first effect of the addition of Ge to Si is a change in the bandgap energy. Figure 1.9 shows a comparison of the measured bandgap of relaxed SiGe alloys[25] with the calculated bandgaps of strained SiGe on Si and strained Si on relaxed SiGe[26].

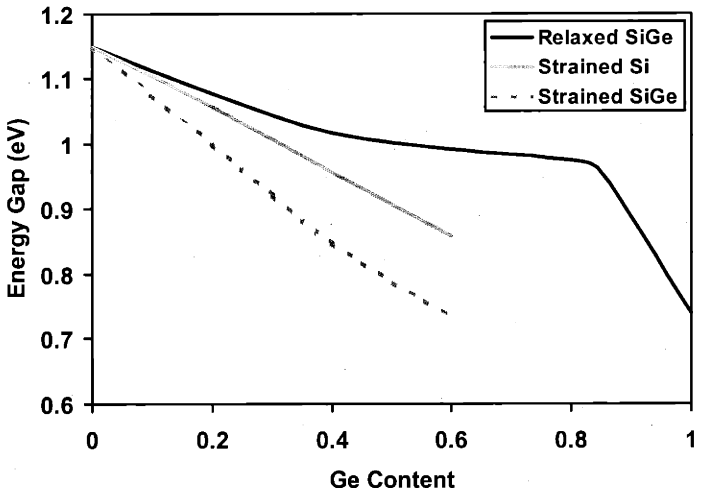

Figure 1.9 Schematic of the effects of Ge content and strain on the bandgaps of Si and SiGe alloys. Note that both strained Si and strained SiGe have smaller bandgaps than that of the relaxed alloy.

The calculations show that either biaxial tensile or compressive strain reduces the bandgap of these materials below that of the bulk. Notable in this figure is the Δ-L crossover point at about 85% Ge content. At this point, the L-valley of the conduction band shifts below the Δ-point, and the band structure becomes more Ge-like. The calculated strained SiGe bandgaps from Figure 1.9 have been experimentally verified by photodiode measurements[27].

1.6.2 Effect of Strain on the Valence Band

The valence band of Si and SiGe is composed of the heavy hole (HH), light hole (LH), and split-off (SO) bands. In unstrained material, the HH and LH bands are degenerate at the energy maximum, while the SO band is slightly lower (approximately 44 meV) in energy. Intervalley scattering between the three subbands is the primary reason for the low hole mobility of bulk Si. The effects of biaxial tensile and compressive strain on the valence band are shown in Figure 1.10[28].

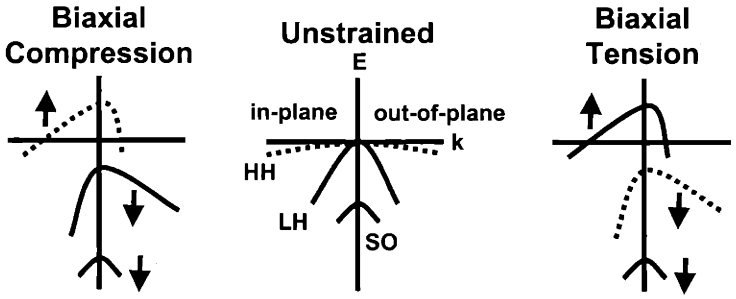

Figure 1.10 The effects of biaxial compressive and tensile strain on the valence band of Si. Strain splits the degeneracy of the light hole and heavy hole subbands. The shapes of the subbands are also deformed, altering the effective hole mass anisotropically.

Compressive strain splits the subband degeneracy, and raises the HH band in energy relative to the LH band. Tensile strain acts in much the same way, raising the LH band in energy. Both strain types also deform the valence subbands, altering the effective hole mass. In both cases, the in-plane effective mass is reduced relative to the unstrained case. Since the subband deformation is strain-dependent and anisotropic, the HH and LH nomenclature is used only to keep track of the relative movement of the subbands. Notice that either compressive or tensile strain can be used to improve in-plane hole mobility. The subband splitting tends to increase the scattering time τ by limiting phonon

scattering, and the band deformation decreases the effective mass m^* in both the in-plane and perpendicular directions.

1.6.3 Effect of Strain on the Conduction Band

As noted above, the conduction band minimum occurs at the Δ-point for Si and Si-rich SiGe alloys, and at the L-valley for Ge and Ge-rich alloys. The device work in this thesis deals exclusively with Si and Si-rich alloys, so only the Δ-point will be considered here. In the absence of strain, this conduction band minimum is six-fold degenerate. Biaxial strain splits the degeneracy of the Δ bands into two separate subbands—the two-fold degenerate Δ_2 perpendicular band and the four-fold degenerate Δ_4 in-plane band. The constant energy surfaces of the conduction band are shown in Figure 1.11.

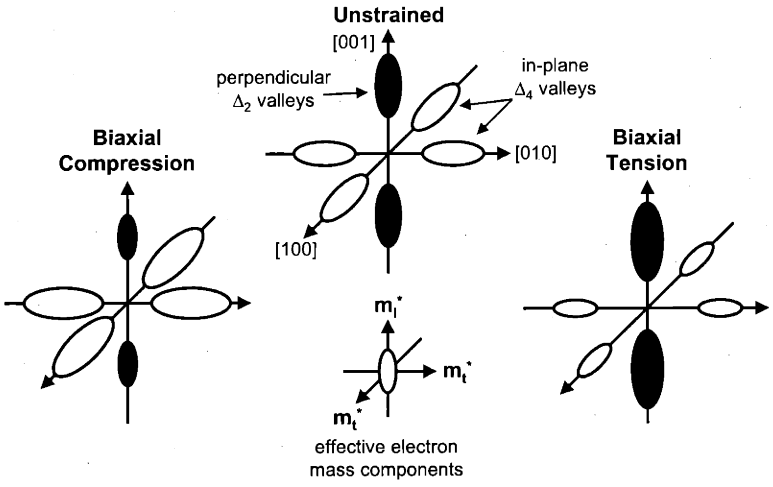

Figure 1.11 The effects of biaxial compressive and tensile strain on the conduction band. The six-fold degeneracy is split between the Δ_2 and Δ_4 subbands, but their shapes remain unchanged. Also indicated are the longitudinal and transverse components of the electron effective mass.

Neither compressive nor tensile strain deforms the shape of the subbands, leaving the longitudinal and transverse effective masses unchanged[29]. Under tensile strain, the Δ_2 subband is reduced in energy relative to the Δ_4 subband. Conversely, the Δ_4 subband is at lower energy under compressive strain. Although the effective masses of the subbands are unchanged, tensile strain allows one to take advantage of the smaller transverse electron mass for in-plane transport, increasing the electron mobility. Similarly to the valence band case, the subband splitting also improves mobility by increasing the scattering time τ via the elimination of intervalley phonon scattering.

1.6.4 Strained SiGe on Si: Type-I Band Alignment

The band offsets of SiGe-based heterostructures can be used for carrier confinement. Figure 1.12 shows the type-I band alignment of a strained SiGe layer grown on a Si substrate. In this case the band offset between the two materials occurs almost exclusively in the valence band, forming a potential well for holes in the SiGe layer[30]. The amount of this offset in eV is given by:

$$\Delta E_v = 0.74x$$

where x is the Ge fraction in the strained SiGe layer[31]. For a strained 30% Ge content alloy on Si, the valence band offset is approximately 200 meV. Strained SiGe on Si has been successfully used to fabricate high performance electronic devices.

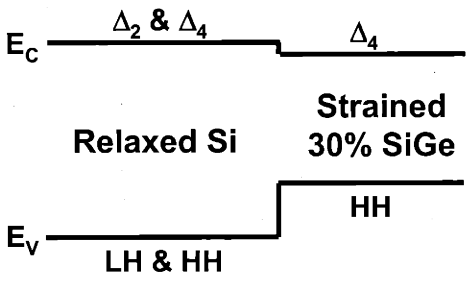

Figure 1.12 Schematic of the type-I band alignment of a strained Si layer on Si. The band offset falls almost entirely in the valence band, creating a hole potential well in the strained Si layer.

Heterojunction Bipolar Transistors

The most successful of the type-I offset devices has been the heterojunction bipolar transistor (HBT)—a bipolar junction transistor (BJT) with a strained SiGe base. The improved performance of the HBT is due to the valence band offset in the base, which reduces the amount of hole injection from the base to the emitter. This leads to improvements in gain. The base can also be graded in Ge content and highly doped, reducing the base transit time and improving high frequency performance of these devices. SiGe BiCMOS chips, in which SiGe HBTs are integrated with mainstream Si CMOS, are now available commercially[32].

P-Channel Field Effect Transistors

The type-I band offset has also been utilized in the fabrication of high mobility p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) and modulation-doped field-effect transistors (MODFETs). The pseudomorphic SiGe p-MOSFET has been the subject of intense study as a way to improve upon the lackluster hole mobility of bulk Si

PMOS devices. Figure 1.13 shows a band diagram of this device. Hole mobility enhancement is achieved in the two-dimensional hole gas (2DHG) formed in the compressively strained SiGe layer[33]. A Si cap layer has been grown on top of the strained SiGe channel layer in order to insure a high quality interface with the gate oxide. The Si cap layer also tends to reduce surface scattering in the SiGe well, improving the hole mobility further. Care must be taken to make this layer as thin as possible so that it does not invert and create a lower mobility parallel conduction path.

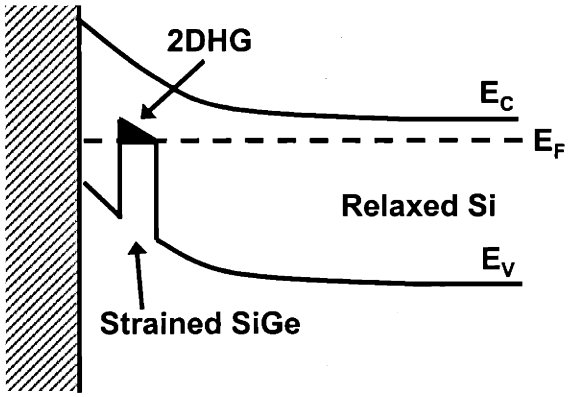

Figure 1.13 Band Diagram of the pseudomorphic SiGe p-MOSFET. Enhanced hole mobility is provided by the strained SiGe, while the Si cap layer forms a high quality interface with the gate oxide.

The benefits of compressive strain can also be harnessed in high Ge content layers. The Ge hole is extremely light, so Ge p-channel devices should exhibit extremely high performance. In the p-MODFET, strained layers of 80-100% Ge are grown on SiGe virtual substrates of lower Ge content. Pure Ge channel MODFETs on 60% Ge substrates have produced record hole mobilities of 1870 $cm^2/V \cdot s$ at room temperature[34]. Metal Schottky gates are used in these structures, limiting their voltage swing during operation. Thus, modulation doping is utilized to provide carriers to the potential well.

When modulation doping, the dopants are physically removed from the device channel to minimize ionized impurity scattering effects. Compressive strain causes small-scale surface undulations in these layers that can impair hole mobility. Recognition of this fact led to the achievement of the highest hole mobility in the SiGe materials system[35]. A pure Ge channel grown on a 60% SiGe substrate was modulation doped such that the 2DHG formed at the bottom interface, as far away from the surface undulations as possible. A hole mobility of 55,000 $cm^2/V\bullet s$ was achieved at 4.2 K. Hole mobilities of compressively strained 80% SiGe channels on 30% SiGe substrates have proven to be much lower than those of Ge channels[36], indicating that alloy scattering may play a large role in these structures.

1.6.5 Strained Si on SiGe: Type-II Band Alignment

The band alignment for a tensile strained Si layer on relaxed SiGe is shown in Figure 1.14. Similar offsets occur in both the conduction and valence bands in this type-II alignment, creating a potential well for electrons in the strained Si[37]. Thus, all devices requiring this conduction band offset, *e.g.* high performance FETs, require the use of a high-quality relaxed SiGe layer on Si as a substrate. The conduction band offset in the strained Si layer in eV is given by:

$$\Delta E_c = 0.6x$$

where x is the Ge fraction in the virtual substrate. This relation holds for Ge fractions of 60% or less. In the case of strained Si on 30% SiGe, the conduction band offset is

approximately 180 meV. A number of high performance electronic devices have been produced with tensile strained Si layers.

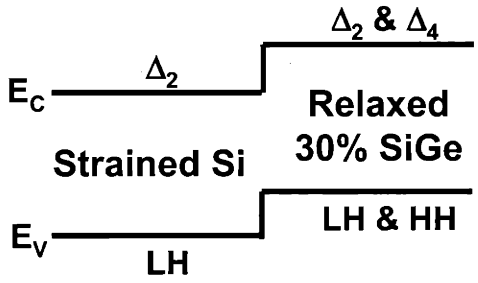

Figure 1.14 Schematic of the type-II band alignment of tensile strained Si on relaxed SiGe. The conduction band offset in the strained Si layer forms a well for electrons.

Strained Si N-Channel Field Effect Transistors

Electron mobility is increased in strained Si devices in two ways. First, the in-plane effective electron mass is reduced by the subband splitting. In unstrained Si, electrons occupy all six degenerate valleys equally, and thus the in-plane effective mass is given by:

$$m^* = \left[\frac{1}{3}\left(\frac{1}{m_l} + \frac{2}{m_t}\right)\right]^{-1}$$

where the longitudinal mass $m_l = 0.98m_o$ and the transverse mass $m_t = 0.19m_o$. By this calculation, the in-plane effective mass of unstrained Si is $0.26m_o$. As mentioned earlier in Section 1.6.3, biaxial tensile strain lowers the Δ_2 subband in energy. Most electrons will lie in this subband and will have effective masses equal to the transverse electron mass, $0.19m_o$. Thus, the mobility enhancement due to this effect alone will be 1.36, the ratio of these two effective masses. Experiments performed at low temperature in the

absence of phonon scattering have confirmed this mobility enhancement for strained Si due to the lower effective mass[38]. At room temperature, where phonons become a major scattering mechanism, the advantage of strained Si is even more pronounced. The strain-induced conduction band splitting results in a reduction in intervalley phonon scattering. This increases the scattering time τ, increasing the electron mobility at room temperature. Buried strained Si channel modulation-doped structures have achieved record electron mobilities of 2830 $cm^2/V\bullet s$ at room temperature[39] and over 8×10^5 $cm^2/V\bullet s$ at 15 K[40]. Surface channel strained Si MOSFETs that show electron mobility enhancements of 1.8 over bulk Si MOSFETs have also been fabricated[41].

Strained Si P-Channel Field Effect Transistors

As discussed in Section 1.6.2, tensile strain also improves hole mobility via a reduction in effective mass and a reduction in intervalley phonon scattering. However, since the valence band offset of tensile strained Si forms a potential barrier to hole occupation, buried p-channel devices are impossible to produce. A surface channel device, in which the gate bias forces the holes into the strained Si layer, can be achieved. This is the premise of the strained Si p-MOSFET[42]. Figure 1.15 shows the band structure of such a device in operation. At low gate biases holes will tend to populate the underlying relaxed SiGe layer, but at high vertical fields, the holes will be forced into the high mobility strained Si surface layer.

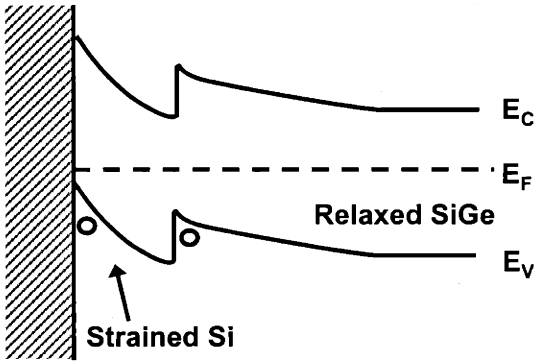

Figure 1.15 Band diagram of the strained Si p-MOSFET. Holes are confined in the low mobility SiGe layer by the band discontinuity at low gate bias. Transport in the strained Si layer is dominant at high gate bias as holes are forced to the surface.

High Field Carrier Transport in Strained Si MOSFETs

Enhancements in low field mobility translate directly into increased drift velocities in long-channel MOSFETs, thus directly enhancing the speed of such devices. At the high lateral electric fields experienced by carriers in deep submicron MOSFETs, carrier velocities saturate and no longer directly depend on the low field mobility. However, device performance is still enhanced in deep submicron strained Si MOSFETs. In very short device channels, carriers can traverse the channel of the device without experiencing a scattering event, in effect increasing their velocity over the saturation velocity. Thus, device performance will be enhanced in deep submicron devices beyond that predicted by the saturation velocity. Theoretical calculations of strained Si channels predict enhanced velocity overshoot for both electron[43] and hole transport[44]. Although these models rely upon an unphysical constant channel potential, this effect may enhance the performance of deep submicron strained Si n- and p-MOSFETs. More likely, the

velocity at which carriers are injected from the source into the channel increases with strain, enhancing device performance at short channel lengths. Deep submicron strained Si MOSFETs fabricated on 20% SiGe virtual substrates do exhibit enhanced performance over bulk Si MOSFETs[45].

1.7 Scope and Organization of Thesis

This work details the investigation and demonstration of relaxed SiGe-based materials and devices suitable for integration with Si microelectronics technology. The following chapter describes the methods of growth and characterization of the SiGe materials used in this project. The fabrication of high quality relaxed SiGe layers of high Ge content is discussed in Chapter 3. The key materials improvement involves the control and elimination of threading dislocation pileups. A discussion of the integration of III-V and Ge-based devices on this material concludes the chapter. Chapter 4 describes the production of relaxed SiGe-based MEMS devices. The design of the SiGe layers and results from the fabrication of parts at Draper Laboratories are included. The key manufacturing challenges for relaxed SiGe MEMS are identified and resolved. Chapter 5 details the fabrication of strained Si MOSFETs on relaxed SiGe material. All relevant steps of the device fabrication and characterization process are included. The effects of changing materials parameters on these devices, as well as their process stability, are reported. The thesis concludes with a summary and suggestions for extensions of this work in Chapter 6.

Chapter 2

Growth and Characterization of SiGe Virtual Substrates

2.1 Ultrahigh Vacuum Chemical Vapor Deposition of SiGe

All of the SiGe virtual substrates described in this work were grown via ultrahigh vacuum chemical vapor deposition (UHVCVD). Initially developed as a method to grow thin Si layers at low temperatures[46], UHVCVD has been successfully used to grow high quality SiGe heteroepitaxial layers by many groups[47-50]. The advantage of UHVCVD arises from the fact that as the background pressures of oxygen and water in the system decrease, SiO_2 becomes unstable at low temperatures[51,52], allowing the growth of high quality Si and SiGe layers. The low background pressure also eliminates the need for carrier gases like H_2, which are used in some other growth methods.

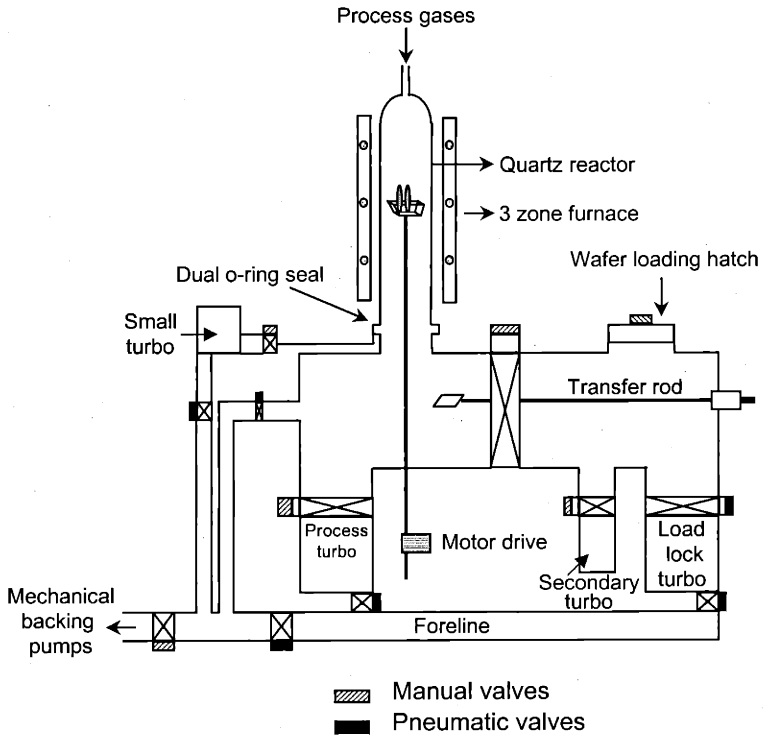

Figure 2.1 Schematic of the UHVCVD reactor utilized in this work.

Figure 2.1 shows a schematic of our unique UHVCVD reactor. It is a vertical, hot-walled system equipped with a load lock. Both the growth chamber and the load lock are evacuated by turbo pumps, which are backed by a roots and mechanical pump combination. The quartz tube seals to the rest of the reactor via a dual o-ring seal. The space between the o-rings is evacuated by a smaller turbo pump, allowing the inner o-ring to achieve a UHV seal. The background pressure in the UHVCVD reactor is normally in the 10^{-9} Torr range at 900°C. A manual gate valve over the reactor turbo pump can be partially closed, retarding its pumping efficiency. This allows the growth pressure to be adjusted in the range of 3-25 mT. The growth pressure is calibrated by flowing Ar into the chamber before the growth sequence and adjusting this manual valve accordingly. Normally, up to ten 4" wafers can be grown upon at once, although wafers of any size from 2" to 6" can be used with a quartzware change. SiH_4 and GeH_4 gases act as the precursors for Si and Ge growth, and B_2H_6 and PH_3 are used as p-type and n-type dopant sources. The reactor has been extensively calibrated at temperatures of 450-900°C. High growth temperatures and pressures facilitate the fast growth of SiGe virtual substrates that are typically several microns thick. Lower growth temperatures and pressures are utilized for the growth of thin device layers where exact thickness control is important. Lower temperatures are also used for Ge-rich SiGe layers in order to avoid gas-phase nucleation of GeH_4.

Prior to epitaxial growth, the Si wafers are cleaned in a piranha solution, consisting of a 3:1 mixture of H_2SO_4 and H_2O_2, for 10 minutes. After a rinse in deionized water, the wafers are dipped into a dilute HF solution for one minute to create a

hydrophobic, hydrogen-terminated surface and then immediately loaded into the reactor load lock. After the load lock is allowed to pump down for several hours, the wafers are introduced into the growth chamber via a transfer rod. The wafers are then annealed in the reactor at approximately 200°C for 30 minutes to desorb any water vapor or organic contaminants. Afterward, the wafers undergo a high temperature (850-900°C) oxide desorption step for 5-10 minutes. A thick Si buffer layer is then grown on the wafers to provide a clean surface for heteroepitaxial growth. The remainder of the growth then proceeds at the desired temperature and pressure. The low background impurity pressure in the reactor allows temperature changes to be performed within a growth sequence, even though temperature drops can take hours in this large hot-walled system.

2.2 Characterization of SiGe Virtual Substrates

Accurate and detailed characterization of the defect morphology, layer thicknesses, lattice parameter, and surface roughness is necessary for the production of optimum SiGe relaxed graded buffers. Several different techniques have been used in conjunction in order to analyze the samples produced in this work.

2.2.1 Transmission Electron Microscopy

Transmission electron microscopy (TEM) requires samples that have been thinned to electron transparency, less than 1 μm thick. This is accomplished via repeated mechanical polishing, followed by argon ion milling. Samples viewed in cross-section (XTEM) provide accurate layer thickness data for SiGe virtual substrates, as can be seen in Figure 2.2. This XTEM micrograph shows a portion of a SiGe relaxed graded buffer.

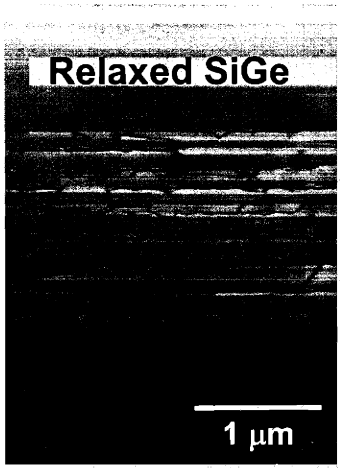

Figure 2.2 Cross-sectional TEM micrograph of a SiGe relaxed graded buffer.

Some details of the dislocation morphology can also be gleaned from such pictures, although determination of accurate threading dislocation densities from XTEM is usually impossible. Due to the small area actually imaged in XTEM, normally only an upper bound on the threading dislocation density can be obtained since no threading dislocations will appear in the image. Fallacious reports of "dislocation-free" material in the literature, stemming from misinterpretation of dislocation-free XTEM pictures, underscore the necessity for threading dislocation density studies to be performed with multiple techniques if possible. Only if the threading dislocation density is very large, on the order of 10^9 cm^{-2}, can fairly accurate threading dislocation densities be determined from such a sample.

Plan-view samples can also be used in TEM studies. Such samples may provide more detailed information about the dislocation density of the uppermost layer of a SiGe virtual substrate. Still, because the sample size is small, threading dislocation density counts require the use of several samples and many pictures for accurate statistical data to

be obtained. Due to these sample area limitations, plan-view TEM provides accurate measurements only for samples with dislocation densities on the order of 10^7 cm^{-2} or greater[8]. Figure 2.3 shows a plan-view TEM micrograph of a SiGe virtual substrate with threading dislocations visible. Because many of the virtual substrates utilized in this study have threading dislocation densities lower than 10^7 cm^{-2}, a large-area technique is required for an accurate determination of dislocation density.

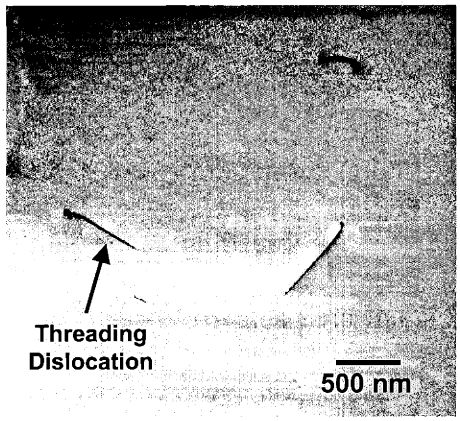

Figure 2.3 Plan-view TEM micrograph of the uniform cap layer of a SiGe virtual substrate.

2.2.2 Etch Pit Density Measurements

Etch pit density (EPD) measurements are the primary large-area technique for determining threading dislocation density used in this study. In this technique, a selective etchant is used to reveal threading dislocations intersecting the surface of the virtual substrate. Then, differential interference (Nomarski) optical microscopy is used to image the dislocations, allowing determination of threading dislocation densities on very large areas. Because samples can be centimeters on a side, large scale defect morphology can also be examined in great detail. A typical EPD photo in which threading dislocations

are revealed is shown Figure 2.4. With this technique, threading dislocation densities of 10^5 cm^{-2} or below can be determined quickly and efficiently.

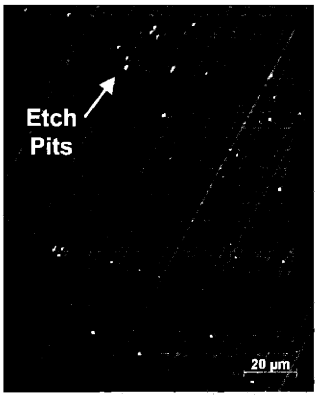

Figure 2.4 Nomarski optical micrograph of a selectively etched SiGe sample for EPD analysis of threading dislocation density.

However, much like TEM, EPD can provide incorrect data if used on the wrong type of sample. In samples with very high threading dislocation densities, the threads will many times tend to group together in bundles. When EPD is utilized on such a sample, individual threads cannot be resolved, and each bundle will appear as a single etch pit. Hence, threading dislocation densities will be obtained that are orders of magnitude lower than actual values. Thus, the choice of technique is very important when attempting to accurately determine threading dislocation densities. EPD should only be used when the density is on the order of 10^6 cm^{-2} or lower, while other more defective samples should be studied with TEM. Borderline samples can be studied with both techniques, and the results will normally correlate quite closely.

The large-area EPD technique is also uniquely suited for the determination of misfit dislocation densities in thin strained surface layers. Figure 2.5 shows misfit dislocations revealed by an EPD etch. Since the misfit dislocations are actually imaged

over a large area, very small amounts of relaxation can be detected with this technique. Other methods, such as X-ray diffraction and Raman scattering, are insensitive to misfit dislocation densities below 10^5 cm^{-1}[53].

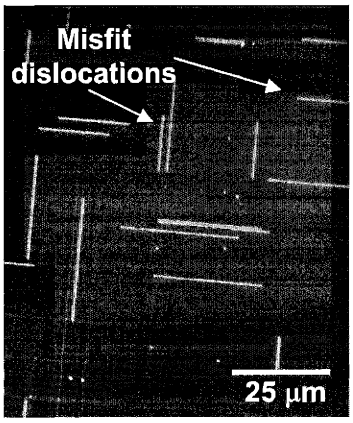

Figure 2.5 Nomarski optical micrograph of misfit dislocations in a surface strained Si layer revealed by selective etching. Note that this technique is sensitive to even very low misfit dislocation densities.

Two selective etchants were used for EPD studies of our SiGe virtual substrates. For samples with low Ge content, a dilute Schimmel etch[54,55] was used. This etch consists of a 5:4 mixture of 0.3M chromic acid (aqueous CrO_3) and 49% hydrofluoric acid (HF). Figure 2.6 shows the etch rate of this solution for samples of various Ge contents[56]. The etch rate becomes vanishingly small for Ge contents of approximately 80-85%. Not coincidentally, this is the point at which the band structure of SiGe becomes more Ge-like. Hence, for Ge and Ge-rich layers, another etch was used for EPD measurements. The iodine etch[57] consists of a 5:10:11 mixture of HF, nitric acid (HNO_3), and acetic acid (CH_3COOH) combined with 30 mg of powdered iodine (I_2) per 260 ml of solution. This solution etches Ge-rich layers extremely quickly, more than 2000 Å/s. Thus, normally only very short etch times are required for the EPD of Ge-rich

layers. For Ge layers with threading dislocation densities on the order of 10^6 cm^{-2}, plan-view TEM measurements were also used and correlated quite well with the EPD results.

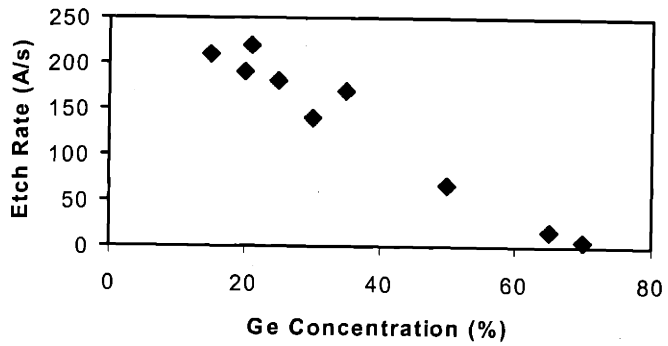

Figure 2.6 **A plot of the dependence of the etch rate of the dilute Schimmel EPD etchant on the Ge content in the SiGe alloy. The etch loses effectiveness as the alloy band structure approaches the Δ-L crossover point and becomes more Ge-like.**

2.2.3 Other Characterization Techniques

Other techniques were also used to analyze the characteristics and quality of the materials used in this study. The effects of surface roughness on the defect morphology and the suitability for processing of SiGe virtual substrates are another essential facet of this thesis. Atomic force microscopy (AFM) is capable of providing extremely accurate measures of surface roughness over a wide area. Figure 2.7 displays a typical AFM scan of a SiGe virtual substrate. This technique has also been used to determine threading dislocation density of SiGe virtual substrates by imaging surface pits created by the dislocations.

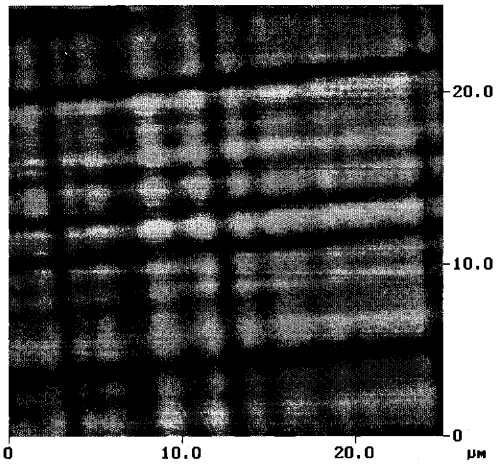

Figure 2.7 Atomic force microscopy scan of the surface morphology of a SiGe virtual substrate. Note the characteristic crosshatch pattern of the surface roughness due to the strain fields of underlying misfit dislocations. The pictured rms roughness is approximately 9 nm.

The accurate determination of the lattice parameter of the SiGe material, hence providing compositional data, was also of utmost importance. X-ray diffraction (XRD) was used to ascertain composition of SiGe samples, and combined with XTEM measurements in order to calibrate UHVCVD growth parameters over the wide range of temperature and pressure described earlier. In samples where the composition was well known, XRD was also used to determine the degree of relaxation of the films. This is especially important for growth at low temperatures where incomplete relaxation of the SiGe layers may occur.

Chapter 3

SiGe Virtual Substrates for the Integration of III-V Materials with Si

3.1 Dislocation Dynamics in Relaxed Graded Buffers

As mentioned earlier in Section 1.3.2, relaxed graded buffer technology operates via the reuse of existing threading dislocations as misfit strain is gradually accommodated. Since threading dislocation glide creates the misfit dislocation length that relaxes the graded buffer during growth, we can estimate the threading dislocation density required to relax the mismatch strain. The rate of mismatch strain relief $\dot{\delta}$ is related to the dislocation glide velocity v by the following:

$$\dot{\delta} = \frac{\rho_t b v}{2}$$

where ρ_t is the threading dislocation density and b is the Burgers vector. The empirical expression for the dislocation velocity v is given by:

$$v = BY^m \varepsilon_{eff}^m e^{\frac{-U}{kT}}$$

where B is a constant, Y is the biaxial Young's modulus, ε_{eff} is the effective strain on the dislocation, m is a constant typically between 1 and 1.2, and U is the activation energy for dislocation glide[58,59]. Since the rate of strain relief is approximately linear with thickness for thicknesses greater than the critical thickness[19], we can relate the strain relief rate to growth parameters. After combining these expressions, we achieve:

$$\rho_t = \frac{2R_g R_{gr} e^{\frac{U}{kT}}}{bBY^m \varepsilon_{eff}^m}$$

where R_g is the growth rate of the graded buffer and R_{gr} is the grading rate. For the case of SiGe virtual substrates, R_{gr} is equivalent to the amount of Ge introduced into the buffer

per unit thickness. It is interesting to note that, for reasonable values of the above parameters, the threading dislocation density required to achieve equilibrium relaxation in a graded buffer is on the order of 10^5-10^6 cm^{-2}[60]. It can also be seen that this value cannot be easily reduced in a practical manner. The only three variables in the above expression that can be changed by altering the growth parameters are the growth rate, the grading rate, and the growth temperature. Unfortunately, none of these variables can be changed by orders of magnitude in order to reduce the threading dislocation density. Orders of magnitude reduction in the growth rate lead to impossibly long growth times. Large grading rate reductions lead to very thick graded buffers, creating potential problems with thermal mismatch between materials. Moreover, while the growth temperature can be increased, and should be increased to promote dislocation glide, it is restrained by practical bounds as well. Growth system concerns notwithstanding, the growth temperature obviously cannot be increased above the melting temperature of the material being deposited. Additionally, while high melting point materials can be deposited at higher temperatures, U tends to increase for these materials as well. Thus, many reports of wafer-scale graded buffer threading dislocation densities vastly lower than 10^5 cm^{-2} are likely the result of incomplete relaxation of the buffer, or of inadequate threading dislocation counting methodologies.

3.2 Material Degradation in SiGe Virtual Substrates

In the absence of excess dislocation nucleation, a steady-state threading dislocation density can be predicted for our SiGe virtual substrates. Thus, regardless of the final Ge content, approximately constant threading dislocation densities in SiGe virtual substrates

should be observed. In reality, very different behavior is observed. Figure 3.1 displays the total threading dislocation densities of a series of SiGe virtual substrates grown at a grading rate of 10% Ge/μm. There is a clear increase in threading dislocation density as the final Ge content of the buffer increases, counter to the model derived above. Clearly, some mechanism is activated when grading to high Ge contents that causes the nucleation of excess threading dislocations.

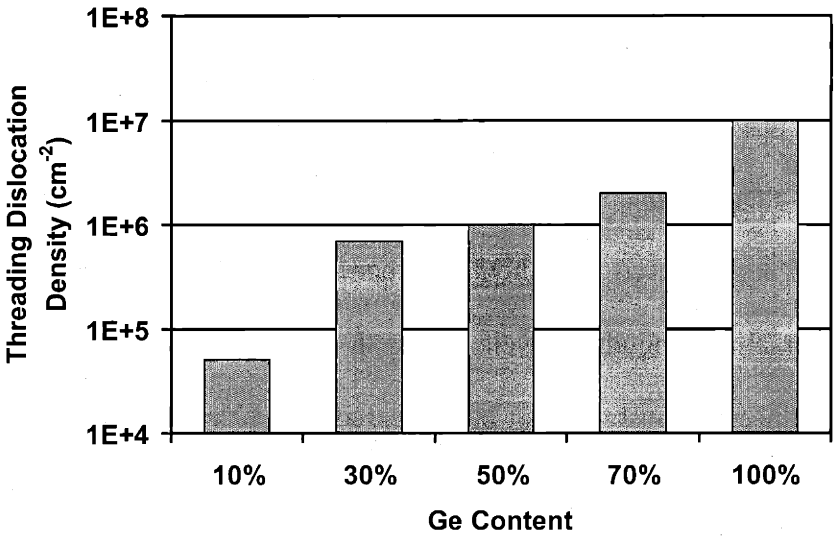

Figure 3.1 Plot illustrating the escalation of threading dislocation density with increasing final Ge content of SiGe graded buffers. All samples were graded at 10% Ge/μm.

During the relaxation of SiGe graded buffers, misfit dislocations form an orthogonal pattern along the in-plane <110> directions. The strain fields of these misfit dislocations affect the local growth rate of the film, resulting in the characteristic "crosshatched" surface morphology of SiGe virtual substrates. The rms surface roughness of SiGe virtual substrates also tends to increase with the final Ge content[61,62].

This trend mirrors the observed increase in threading dislocation density. In fact, it has been shown that the two phenomena are linked—the increase in one results in the increase of the other. The mechanism for these trends is the threading dislocation pileup.

3.3 Threading Dislocation Pileups

Dislocation pileups were noted during early defect morphology studies of graded SiGe layers[19]. As shown in the EPD photo of Figure 3.2, dislocation pileups are lines composed of many threading dislocations that can extend for tens or hundreds of microns across a virtual substrate. Often, they occurred near particles or other heterogeneous dislocation nucleation sources, but their origin was not well understood. Beginning with dislocation blocking, a model for dislocation density was recently formulated[63].

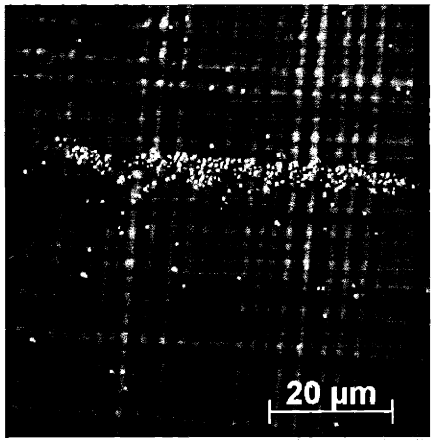

Figure 3.2 Nomarski optical micrograph of a dislocation pileup revealed by selective EPD etching.

The possibility exists that an orthogonal misfit dislocation will arrest the movement of gliding threading dislocations[64]. The strain field of the misfit dislocation, which decays radially, reduces the effective strain that moves the threading dislocation.

In effect, the gliding dislocation must pass above the region surrounding the misfit where the strain field is most heavily concentrated. Calculations show that in SiGe virtual substrates like the ones in this study, the effect of perpendicular misfit dislocations was not enough to arrest the motion of gliding dislocations. However, when the effects of surface roughness are included, a model for dislocation pileup formation can be postulated. Figure 3.3 shows a schematic of the creation of a dislocation pileup. A bundle of orthogonal misfit dislocations lies in the path of gliding threading dislocations. Such a bundle of misfit dislocations can arise due to heterogeneous nucleation from particles or other sources. The strain field from the misfit dislocations also locally affects the growth rate of the SiGe layer, leading to a deep trench in the crosshatch pattern. The combination of the misfit dislocation strain field and the deep surface roughness arrests the glide of threading dislocations, and a pileup forms along the misfit bundle. The trapped threading dislocations can no longer glide to relieve the mismatch strain of the graded buffer, and more dislocations must therefore be nucleated to relax the layer.

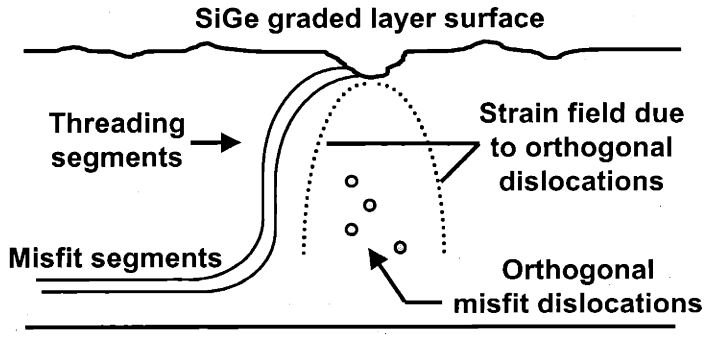

Figure 3.3 **Schematic of the mechanism of dislocation pileup creation. Gliding threading dislocations become trapped by the combination of perpendicular misfit dislocations and deep surface roughness.**

Thus, dislocation pileup formation leads to the observed increase in threading dislocation density in SiGe graded buffers. Moreover, the trapped threading dislocation sites are energetically unfavorable positions for further growth of the layer. This creates a vicious cycle in which trapped threading dislocations lead to increased surface roughness which leads to more trapped threading dislocations, *ad infinitum*. Thus, it is clear that control of the surface and defect morphologies of the SiGe virtual substrate is required to prevent the threading dislocation density escalation caused by dislocation pileups.

3.4 Strategy for Dislocation Pileup Control

3.4.1 Growth of SiGe Virtual Substrates on Offcut Substrates

The first step that can be taken to control the formation of dislocation pileups is the elimination of the large bundles of orthogonal misfit dislocations. Such bundles can occur quite easily in the vicinity of a heterogeneous nucleation source. The activation energy for dislocation nucleation is reduced, and large numbers of dislocations can emanate from the source. The source can be a particle on the wafer introduced from the environment prior to growth, or from the reactor wall during epitaxy. Naturally, every attempt must be made to minimize the exposure of a wafer to a non-cleanroom atmosphere prior to the growth process. However, total elimination of all heterogeneous sources is impossible in practice. Thus, if large bunches of misfit dislocations are to be avoided another technique must be used. Upon examination of a SiGe virtual substrate grown upon a (001) Si substrate, it is clear that the orthogonal misfit array dictated by the active slip system contributes to the formation of these dislocation bundles. A schematic

of the typical orthogonal misfit array on an on-axis (001) substrate is shown in Figure 3.4. When misfit dislocations emanate from a heterogeneous source on this substrate, they must all lie in parallel paths along one of the in-plane <110> directions. Thus, the probability that a closely spaced bundle will form long dislocation pileups is quite high.

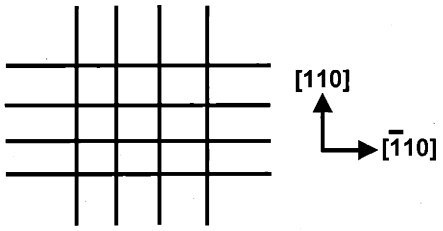

Figure 3.4 Plan view illustration of the orthogonal misfit dislocation array that forms on an on-axis (001) Si substrate.

The development of long, parallel misfit dislocation bundles can be controlled by the use of offcut Si substrates. When these wafers are cut from the Si boule, they are purposely miscut at an angle from the on-axis (001) plane. This substrate miscut causes the {111} planes intersecting the wafer surface to no longer lie in an orthogonal array. Rather, they cross each other in patterns that depend upon the miscut direction. Figure 3.5 shows schematics of the misfit arrays formed on the two types of offcut wafers used in this experiment. On the first substrate, which has been offcut 6° toward the in-plane <110> direction, the misfit dislocations cross each other in the offcut direction and continue to lie parallel in the other <110> direction. On the second substrate, which has been offcut 6° toward the in-plane <100> direction, the entire orthogonality of the original misfit array has been destroyed. In both <110> directions, the misfit dislocations are nonparallel. Offcut wafers are routinely used for polar on non-polar epitaxial growth,

as they prevent the formation of antiphase domains[65]. Hence, the use of offcut substrates is necessary also for the growth of SiGe graded buffers for III-V integration.

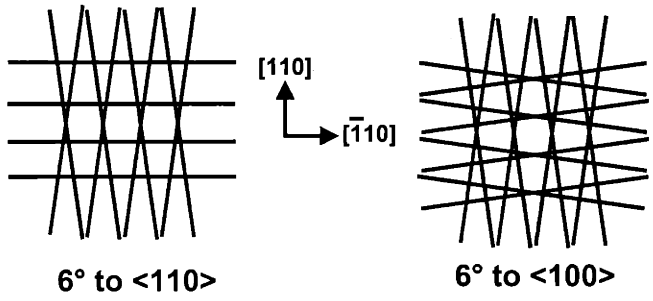

Figure 3.5 **Plan view illustration of the misfit dislocation arrays that form on the offcut substrates used in this study. The misfit dislocations lie nonparallel in one direction on the wafer offcut 6° to the in-plane <110> *(left)*, and in both directions on the wafer offcut 6° to the in-plane <100> *(right)*.**

SiGe graded buffers grown on offcut substrates should have lower densities of threading dislocations, lower dislocation pileup densities, and lower rms surface roughness. To investigate the effect of substrate offcut, a graded buffer was grown to 50% Ge content on the three different substrates. The buffer was graded at a rate of 10% Ge/μm, and the growth temperature and pressure were 750°C and 25 mT. After growth, the surface roughness was measured on all three samples with AFM, and EPD was performed to obtain the threading dislocation and pileup densities. Table 3.1 shows the comparison of pileup density and rms roughness of the three samples. The drastic decrease in both pileup density and rms roughness for the offcut samples indicates that the misfit arrays on these offcut wafers do not block the glide of threading dislocations as efficiently.

Substrate offcut	None	6° to <110>	6° to <100>
Pileup density (cm^{-1})	68.6	32.3	28.6
RMS roughness (nm)	21.4	17.6	4.9

Table 3.1 **Comparison of the dislocation pileup density and surface roughness for identical 50% SiGe graded buffers grown on an on-axis wafer and on the two types of offcut wafers. The use of substrate offcut reduces the number of dislocation blocking events that lead to pileup formation.**

The threading dislocation densities of the three samples are compared in Figure 3.6. The total threading dislocation density has been divided into two portions so the effect of the dislocation pileups can be easily distinguished. The upper part of each bar refers to the threading dislocations trapped in dislocation pileups. The lower part corresponds to the density of threading dislocations that appear between pileups, which we term the field density.

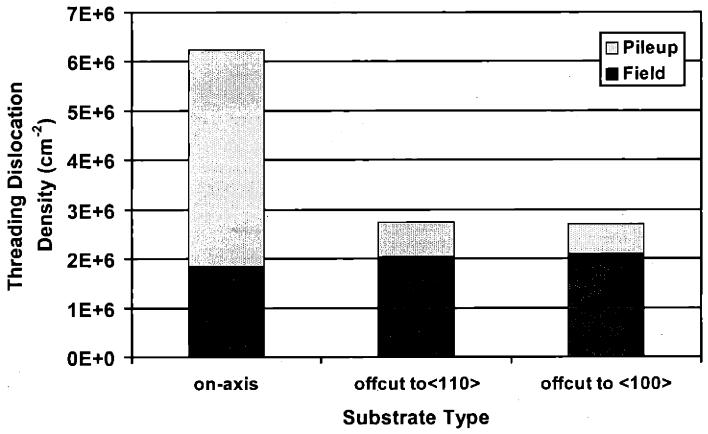

Figure 3.6 **Comparison of the total threading dislocation density of 50% SiGe graded buffers grown on the on-axis and two offcut substrates. The use of offcut substrates dramatically reduces the threading dislocation density, particularly the density of threads trapped in pileups.**

Often in the literature, the field dislocation density is reported as the total density, and the effect of pileups is ignored. As is obvious from Figure 3.6, threading dislocations trapped in pileups can have a large impact on the total density. The samples grown on the offcut substrates have total threading dislocation densities less than half that of the on-axis sample. Because the substrate offcut has decreased the pile-up density, and therefore the number of threads trapped in pileups, the overall defect and surface morphologies of these samples is improved. However, Table 3.1 and Figure 3.6 do indicate that dislocation pileups still form on these substrates, so a change in substrate type cannot completely solve the pileup formation problem.

3.4.2 Intermediate Chemical-Mechanical Polishing of Virtual Substrates

The other factor in the creation of dislocation pileups is the effect of surface roughness. The surface crosshatch pattern forms due to the influence of the strain fields of the underlying misfit dislocations. The use of CVD growth exacerbates the problem, because CVD growth rates are highly dependent on crystallographic orientation. Hence, once the crosshatch forms, it tends to get rougher during CVD growth. If the prevention of dislocation pileup formation is to be accomplished, a method of controlling the surface roughness of the graded buffer must be identified.

Chemical-mechanical polishing (CMP) is a planarization process used in the production of semiconductor wafers. It combines the advantages of a chemical etch of the surface material with the planarizing effect of mechanical action to create substrates of negligible surface roughness[66]. CMP has also been used on the backend of Si CMOS

processes, planarizing wafers between each layer of interconnection metal and interlayer dielectric. If CMP could be used to successfully planarize partially grown SiGe virtual substrates, it could retard the formation of dislocation pileups. A virtual substrate can be grown to an intermediate Ge content and planarized to remove the surface roughness. The growth can then continue to the final desired Ge concentration. Wafers with intermediate planarization can be compared to those grown uninterrupted to gauge if CMP can retard pileup formation and reduce the final threading dislocation density. Figure 3.7 shows a schematic of this intermediate planarization strategy.

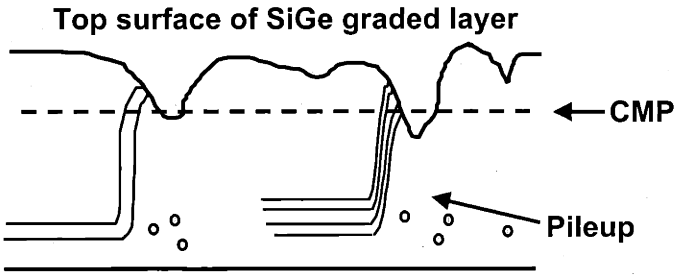

Figure 3.7 Strategy of dislocation pileup reduction via intermediate planarization.

In order to ascertain the effects of intermediate CMP on SiGe virtual substrates, a comparison was made between samples graded to 100% Ge content with and without an intermediate CMP step. Samples A and B refer to the samples graded to 100% Ge without the intermediate CMP. Sample C refers to the sample graded to 50% Ge that underwent the CMP process. Sample D is the sample graded to 100% Ge grown atop sample C. In addition to the CMP step, other growth modifications were made in the growth procedure of sample D. These modifications were made in order to prevent

surface cracks due to the thermal mismatch between Ge and Si and particulate defects due to gas phase nucleation events.

The control sample in this experiment, sample A, was graded from Si to 100% Ge at a rate of 5% Ge/μm. It was grown at 750°C and 25 mT and topped with a 3 μm Ge cap. A linear grade was approximated by increasing the Ge concentration in 2.5%, 5000Å steps. Sample B was graded to 100% Ge at a rate of 10% Ge/μm, at a temperature of 800°C, and at a pressure of 50 mT. This structure is the sample structure from previous reports on the formation of dislocation pileups[63,67]. Sample C was grown to only 50% Ge at a grading rate of 10% Ge/μm and topped with a 1.5 μm 50% Ge cap. The graded region of sample C was composed of 2% Ge, 2000Å jumps. Although not optimized for minimum threading dislocation densities, these 50% Ge substrates are known to typically possess threading dislocation densities of approximately 3×10^{6} cm^{-2}[67]. Wafers with dislocation densities on this order were fine virtual substrates for this study.

The top 5000 Å of sample C was then removed via CMP on a Strasbaugh Model 6EC Laboratory Planarizer. The pad was a Rodel IC1000, which is a perforated pad made of polyethylene. The slurry was Cabot Semi-Sperse 25, which consists of 100 nm diameter silica particles suspended in a KOH-based solution. Although this pad and slurry combination is designed for oxide polishing, good uniformity was achieved during SiGe polishing. The standard CMP parameters used in this study are shown in Table 3.2.

CMP Parameter	Setting
Down force	3.5 psi
Quill speed	25 rpm
Table speed	25 rpm
Slurry flow	100 ml/min
Back pressure	1.0 psi

Table 3.2 Standard CMP parameters for the SiGe planarization performed in this work.

Figure 3.8 shows variation of the polish rate with Ge content. The decrease in polish rate with increased Ge content is probably due to reduced effectiveness of the KOH chemical etch component.

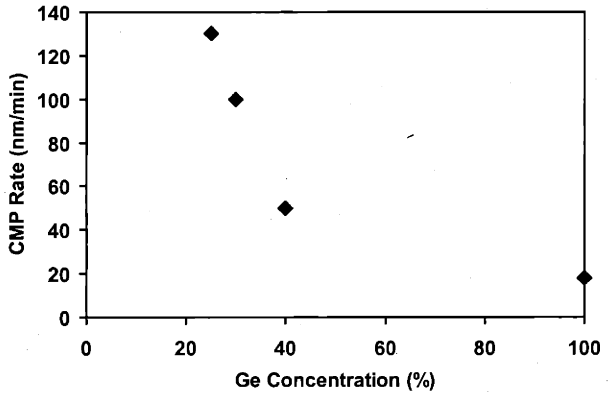

Figure 3.8 Variation of SiGe CMP material removal rate with Ge content. The etch rate decreases with Ge content due to reduced effectiveness of the KOH chemical component, as well as SiGe alloy strengthening.

After CMP, the wafers were quickly rinsed with deionized water and cleaned in an Evergreen wafer cleaning system to remove any remnant slurry particles. The Evergreen utilizes megasonic jets of deionized water and ammonium hydroxide

(NH_4OH) to clean the wafers. This step is of the utmost importance, since any particles left on the wafer can act as heterogeneous dislocation nucleation sites for subsequent mismatched epitaxy. Deposition after inadequate post-CMP cleaning can lead to very defective layers that appear hazy to the eye. After the post-CMP cleaning, the wafers were subjected to a 10 minute HF soak to dissolve any remnant SiO_2 particles from the slurry. The standard pre-growth clean described in Section 2.1 was then performed before regrowth on the wafers.

After CMP, a 50-100% Ge graded buffer was grown on top of sample C at a rate of 10% Ge/μm, again in 2%, 2000 Å steps. This sample, sample D, had other modifications incorporated into its growth as shown schematically in Figure 3.9. In the 50-76% Ge portion of the deposition, the growth conditions were held constant at 750°C and 25 mT. Then the growth was halted and the temperature and pressure were lowered to 550°C and 3 mT. The growth of the graded buffer then continued until a Ge concentration of 92% was reached. The final jump in Ge concentration was made from 92% to 100% and a 1.5 μm uniform cap was deposited.

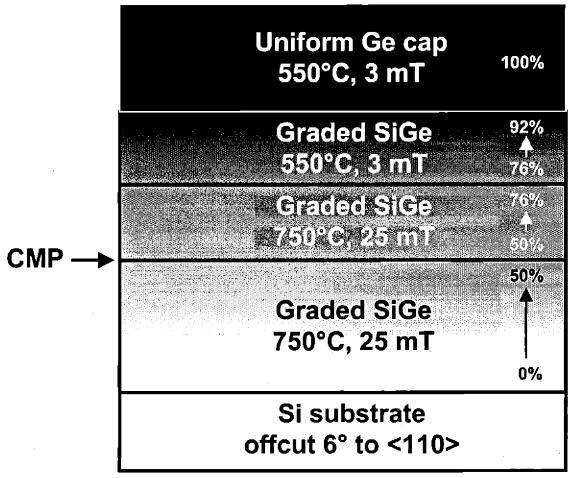

Figure 3.9 Schematic of the growth sequence of sample D. Intermediate planarization was performed at 50% Ge content.

Figure 3.10 is a XTEM micrograph of the upper graded region and the uniform cap of sample D. All of the samples in the study were grown on (100) Si wafers offcut 6° to the in-plane <110>. As already mentioned, these offcut wafers reduce the dislocation pileup density of the SiGe virtual substrates and form a surface suitable for subsequent III-V growth.

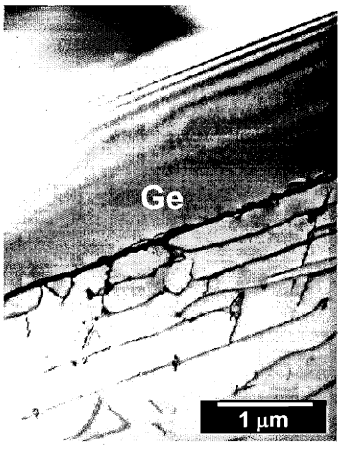

Figure 3.10 Cross-sectional TEM micrograph of the uniform Ge cap and upper graded buffer layers of sample D.

3.5 Effect of CMP on Defect and Surface Morphology

The relevant characterization results from the four samples are presented in Table 3.3. When comparing the threading dislocation densities of the four samples, we find both expected and unexpected results. Since sample A was grown at a slow grading rate, one would expect it to have a lower threading dislocation density if one does not consider the deleterious effects of surface roughening and pileup formation. Of course, just as mentioned previously, these factors create a high density of threading dislocations in sample A, approximately 10^7 cm^{-2}. As expected, sample B, a similar sample graded at a faster rate of 10% Ge/μm, has an even larger threading dislocation density. The trend from sample A to sample B corresponds to published reports on 30% SiGe graded buffers, in which the total threading dislocation density increased with grading rate[68]. The sample C data also confirms the threading dislocation density escalation with Ge concentration shown previously—at 50% Ge, the threading dislocation density is already in the 10^6 cm^{-2} range. However, sample D, in effect a grade to 100% at 10% Ge/μm, has a similar or even slightly lower threading dislocation density than sample C—considerably lower than that of both sample A and sample B. The addition of the CMP step at 50% Ge has arrested the increase in threading dislocation density with Ge concentration.

	Sample A	Sample B	Sample C	Sample D
Final Ge composition	100%	100%	50%	100%
Grading rate (%Ge/μm)	5	10	10	10
Total epitaxial thickness (μm)	23	12	6.5	12
Growth temperature (°C)	750	800	750	50-76%: 750 76-100%: 550
Growth pressure (mT)	250	500	250	50-76%: 25 76-100%: 3
CMP at 50%	No	No	—	Yes
Threading dislocation density (cm^{-2})	$1.1\pm0.1\times10^{7}$	$1\text{-}5\times10^{7}$	$6.3\pm0.1\times10^{6}$	$2.1\pm0.2\times10^{6}$
Crack density (cm^{-1})	47±5	0	0	0
Particle density (cm^{-2})	1250±100	600±40	50±5	150±10
RMS roughness (nm)	35.9	47	37.3	24.2
$a_{\perp}$ of top layer (Å)	5.6559	5.6558	5.5327	5.6597
$a_{\parallel}$ of top layer (Å)	5.6559	5.6552	5.5352	5.6409

Table 3.3 Characterization data from samples A-D. Sample C is a 50% SiGe graded buffer that was planarized. Sample D is the 100% Ge graded buffer grown on sample C. Samples A and B are graded to 100% Ge without intermediate planarization.

Hence, the planarization of the surface during this step must free the threads seen in pileups in sample C and allow the dislocations to relieve the strain introduced in the subsequent growth, eliminating the driving force for the nucleation of additional threading dislocations. Nomarski optical micrographs comparing the EPD of samples C and D are shown in Figure 3.11. The densest pileups seen in sample C have been eliminated by the CMP and regrowth step and the threading dislocation density in the remaining pileups has decreased substantially. A remarkable observation is that the overall defect morphology is actually improved with further relaxation to higher Ge content.

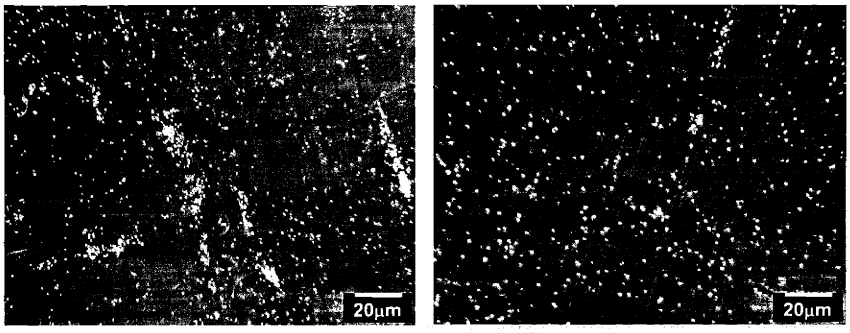

Figure 3.11 Nomarski optical EPD micrographs of sample C *(left)*, the 50% SiGe virtual substrate, and sample D *(right)*, the graded layer to 100% regrown on sample C after planarization. Note that the dense dislocation pileups seen in sample C have been eliminated by the planarization step and further grading.

Measurements of the surface roughness were performed on a Digital Instruments Dimension 3000 Nanoscope IIIa AFM in tapping mode. The scan area was 100 μm × 100 μm for all of the samples. Deeper crosshatch, like the troughs that lead to dislocation pileup formation, is often widely spaced on the sample. Thus, rms roughness measured by AFM tends to increase with increasing scan area. Therefore, direct comparison of this data with other SiGe virtual substrate data in the literature is difficult. Often AFM scans are performed on areas that are 10 μm × 10 μm or smaller. By examining the AFM data from our four samples, we recognize the influence of surface roughness on threading dislocation density. With the inclusion of the CMP step in sample D, the resulting final surface roughness, 24.2 nm, is much lower than that of sample B despite the same grading rate, and lower than that of the more slowly graded sample A. This result is a parallel observation to the threading dislocation density data discussed previously, and it emphasizes the importance of the inclusion of a CMP step in thick graded buffer growth.

3.6 Thermal Mismatch Effects in High Ge Content Virtual Substrates

When a thick graded SiGe buffer like sample A is grown at high temperatures, cracks in the surface can result during cooling due to the thermal mismatch between Si and Ge. Between the sample A growth temperature of 750°C and room temperature, the thermal expansion coefficient of Si, α_{Si}, varies from 4.27×10^{-6} K^{-1} to 2.57×10^{-6} K^{-1} and α_{Ge} varies from 8.55×10^{-6} K^{-1} to 5.90×10^{-6} K^{-1}. Because the coefficient of thermal expansion of Ge is greater than that of Si, severe tensile stresses can result in the upper Ge-rich portion of the buffer. In sample A, the tensile strain due to thermal mismatch when cooling to room temperature is calculated from:

$$\varepsilon = \Delta\alpha\Delta T$$

where $\Delta\alpha$ is the change in thermal expansion coefficient and ΔT is the change in temperature during cooling. The result is approximately 0.2%, resulting in a high density of surface cracks. When growing sample D, we added growth modifications specifically designed to alleviate this cracking problem. By grading at twice the rate, we decrease the total amount of deposited material and the strain energy from the thermal stress accordingly. More importantly, the fast grading rate at lower temperature and the final Ge concentration jump in sample D, from 92% to 100%, incorporate metastable compressive residual stress into the buffer at the growth temperature. Since the compressive lattice mismatch opposes the tensile thermal mismatch, sample D is left in a nearly stress-free state at room temperature. The X-ray diffraction data indicates that the top layer is still actually slightly compressive, preventing any surface cracking.

Additionally, due to the large final jump in Ge concentration the graded buffer of sample D has nearly 1 μm less Ge-rich material than sample B. Hence, even though neither sample D nor sample B experienced surface cracking after growth, sample D will be the superior substrate for subsequent integration of III-V materials. In much the same way as Ge deposition on Si, growth of III-V materials on Si or SiGe substrates can also result in tensile stress due to thermal mismatch.

3.7 Gas Phase Nucleation During UHVCVD Growth

The rate of GeH_4 gas phase nucleation increases with growth pressure and increases exponentially with growth temperature[69]. During the final stages of growth of high Ge content virtual substrates, the ratio of GeH_4 to SiH_4 increases. This leaves the growth much more susceptible to particulate contamination from gas phase nucleation events. The lower growth temperature and pressure during the high Ge portion of sample D decreased the particle density relative to that of samples A and B. These particles can leave some wafer areas useless for subsequent III-V integration, as they create large pits on the wafer surface. Large area III-V devices such as solar cells can suffer from junction shorts when fabricated on these pits[70]. The remaining particle density in sample D is most likely due to particles from the reactor walls. Since the UHVCVD system is hot-walled, material is also deposited on the quartz reactor tube as it grows on the wafers. Thermal cycles, like the one during the growth of sample D, can dislodge particles of this material, dropping it onto the wafers.

3.8 Dislocation Annihilation in SiGe Virtual Substrates

The benefits of the intermediate CMP step are illustrated in Figure 3.12. The threading dislocation densities of two sets of samples are shown. On the left, a 25% Ge graded buffer grown at 750°C has a total threading dislocation density in the mid-10^5 cm^{-2} range. This sample does contain some pileups, but the majority of the threading dislocations are in the field. This sample was planarized via CMP, and then a graded layer was regrown on top to a final Ge concentration of 50%.

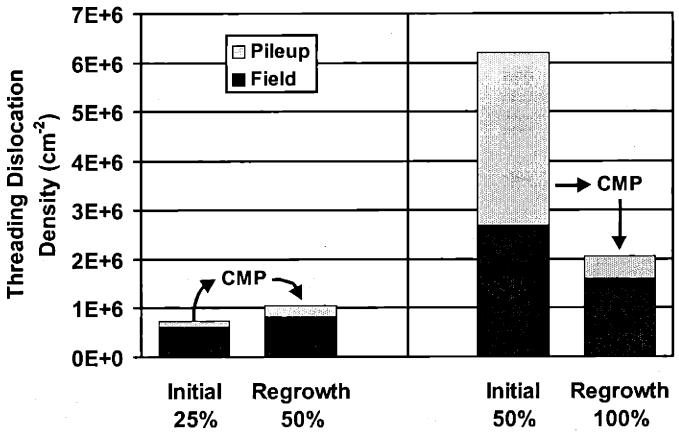

Figure 3.12 Effect of intermediate planarization on total threading dislocation density when grading from 25% SiGe to 50% SiGe *(left)*, and when grading from 50% SiGe to 100% Ge *(samples C and D, right)*. The 50% sample with intermediate planarization has a much lower threading dislocation density than the one without. Also, notice that much of the excess threading dislocation density from the 50% SiGe sample on the right has disappeared upon regrowth to 100% Ge.

While the total threading dislocation density has increased slightly, the majority of the threads are in the field. In this case, the intermediate CMP step has hindered the formation of dislocation pileups that can lead to large increases in threading dislocation

density. We can contrast this 50% Ge sample to the one on the right side, which is sample C from the previous section. Sample C was grown under identical growth conditions—750°C growth temperature, 25 mT growth pressure, and 10% Ge/μm grading rate—but without the intermediate CMP step at 25% Ge. We see a drastic increase in threading dislocation density. In this case, over half of the threading dislocations in the sample are trapped in pileups, forcing the total dislocation density far above the equilibrium level. Also interesting to note is the fact that the field dislocation density in sample C is larger than that of the sample with the intermediate CMP step. An increase in threading dislocation density as pileups form is expected—as threads get trapped in pileups, others must be nucleated in the field to continue contributing to strain relief. However, the increase in field threading dislocation density cannot be explained by this model. The increase in field dislocation density with pileup density has also been observed in the growth of other SiGe virtual substrates[71]. As dislocation pileups form, the strain fields of the dislocations in the pileups may act to retard the motion of gliding threading dislocations. The motion of such threads may be slowed while still in the "field" regions of the sample. A higher number of field threading dislocations will therefore be required to relax the graded buffer, since their effective glide velocity has been decreased due to this interaction with the pileups.

Sample C was also planarized with CMP, and as described earlier, was regrown upon to create sample D. Interestingly, after the regrowth, the threading dislocation density actually decreases. The threading dislocation density of sample C was much larger than that ideally required to relax the mismatch strain due to pileup formation.

These extraneous threading dislocations, once immobile in pileups, were freed to glide after surface planarization. The decrease in their number cannot be explained by dislocation glide and exit at the edge of the wafer, because the mismatch strain applied during the regrowth is inadequate to move the dislocations those distances. Hence, dislocations must be annihilated via encounters with other threads of the appropriate Burgers vector. Obviously, in the dense dislocation pileups, the probability of dislocation annihilation must increase, and the overall threading dislocation density recovers to a number much closer to the equilibrium value. This relationship can be expressed as:

$$\dot{\rho} = \dot{\rho}_{nucleation} + \dot{\rho}_{annihilation} = 0$$

where nucleation and annihilation act in unison to leave the change in threading dislocation density $\dot{\rho}$ at a net zero, leaving the dislocation density at its steady-state equilibrium value.

For the case of highly mismatched films like Ge or GaAs on Si, threading dislocation densities have been experimentally observed to decrease with increasing film thickness. This reduction has a 1/h dependence, where h is the film thickness, and has been observed universally for many materials combinations, including InAs/GaAs, GaAs/Ge/Si, GaAs/InP, and InAs/InP[72]. This dependence weakens or saturates below a threading dislocation density of approximately 10^7 cm^{-2}, so while GaAs films have been grown on Si with threading dislocation densities of 10^6 cm^{-2}, thicknesses of well over 100 μm were required[73]. As mentioned previously, the annihilation of threading dislocations in thick uniform layers occurs due to geometric effects. Since the threads are inclined with respect to the substrate, as the film grows thicker, the threads may approach one

another. Figure 3.13 shows a depiction of this relative motion during uniform layer deposition. If threads with the appropriate Burgers vectors move close together in this manner, they may annihilate. Extensive modeling of this phenomenon has confirmed the experimentally observed 1/h dependence of threading dislocation density reduction with film thickness[74-76].

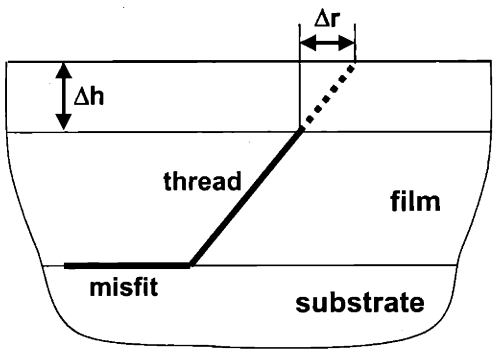

Figure 3.13 Schematic of the relative motion of a threading dislocation during deposition of a thick homoepitaxial layer. Deposition of a film thickness Δh causes the threading dislocation to move a distance Δr. Annihilation events are possible during uniform layer growth due to the geometry of the threading dislocation. After Romanov, *et al.*[75]

In the case of a graded buffer growth, annihilation events become even more probable. Not only are threads undergoing the relative motion due to film growth described above, but they are also gliding to relax the lattice strain being applied. The distance each thread travels and hence the probability for annihilation events increases. This threading dislocation motion is depicted in Figure 3.14. In the absence of nucleation and of blocking events such as dislocation pileup formation, calculations show that threading dislocation density reduction will occur at an exponential rate with film thickness[77]. Thus, we can infer that if excess mobile threading dislocations are present in

a graded buffer, they may annihilate quickly during buffer growth. Of course, if annihilation events decrease the threading dislocation density below the equilibrium value required for relaxation, the necessary threads will be supplied via nucleation events. Our experimental data is the first experimental evidence of threading dislocation density reduction via annihilation during graded buffer growth.

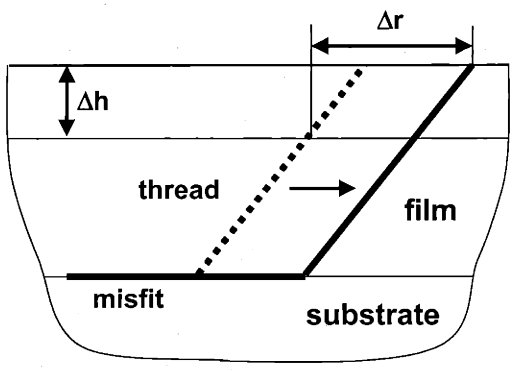

Figure 3.14 Schematic of the motion of a threading dislocation during mismatched heteroepitaxy. Deposition of a film thickness Δh causes the threading dislocation to move a distance Δr. The thread glides to relieve mismatch strain, moving much farther than it would due to geometry alone. Hence, Δr is larger than in the case of Figure 3.13. This motion increases the opportunity for dislocation annihilation events.

An experiment was performed to determine if dislocation annihilation could be used to decrease the threading dislocation density of SiGe virtual substrates. Since we have posited that a steady-state threading dislocation density is required to achieve equilibrium relaxation, dislocation annihilation and dislocation nucleation must be working in tandem to achieve this balance. Indeed, if enough dislocations annihilate such that not enough exist to relax the layer, the system will attempt to replace them via dislocation nucleation. Likewise, as we have seen already, if an excess number of dislocations are free to glide, annihilation will dominate. In this experiment, a set of 20%

Ge virtual substrates was grown at 750°C. The samples were grown at a 10% Ge/μm grading rate and topped with a 1 μm uniform 20% Ge cap. The resulting threading dislocation density was in the low 10^5 cm^{-2} range, as indicated on Figure 3.15.

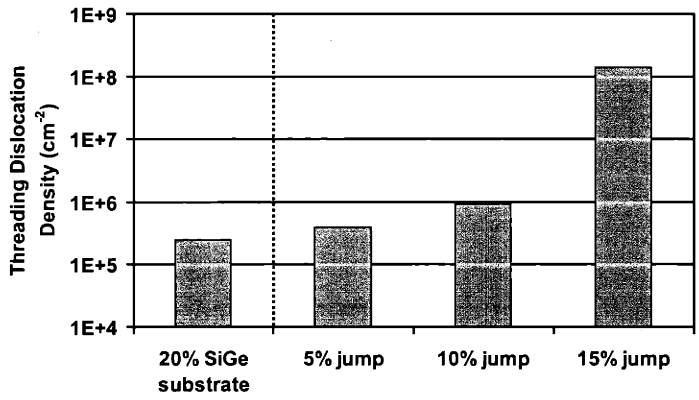

Figure 3.15 Threading dislocation densities of the wafers in the annihilation experiment. Uniform layers with mismatches of 5, 10, and 15% Ge were grown on the 20% SiGe virtual substrate *(leftmost sample)*. Rampant nucleation caused the dislocation densities to increase, masking any effects of annihilation.

Different regrowths were performed on these substrates in order to determine if small amounts of lattice mismatch strain could be used to drive dislocation annihilation. In an attempt to prevent thermally activated dislocation nucleation from replacing annihilated threads, the regrowths were performed at a low temperature, 550°C. Figure 3.15 shows the threading dislocation densities of 1 μm uniform regrowths of 25%, 30%, and 35% Ge content on the 20% Ge substrates. The threading dislocation density increases as the compositional jump of the regrowth layer increases. This result is similar to that seen in graded buffers, in which the lowest threading dislocation densities are achieved with the smallest jumps in Ge content while grading[68]. Additionally, all of the

final threading dislocation densities are larger than that of the initial substrate. Hence, although dislocations may be annihilating in these layers, this is masked by the effect of nucleation. Nucleation occurs to reestablish the equilibrium threading dislocation density for the new growth conditions. Thus, our attempt to control the dislocation density by lowering the growth temperature has backfired. Not only is the nucleation process still very active, we have slowed dislocation glide enough to require a large amount of nucleation to relax the layer.

The fact that rampant dislocation nucleation will dominate in these mismatched samples grown at low temperature can be explained by the dependence of dislocation nucleation rate and of dislocation glide velocity on strain. Both dislocation nucleation and glide are thermally activated and thus have an exponential dependence on temperature. Therefore, at lower temperatures, the magnitude of both nucleation and glide decrease. As the dislocation glide velocity decreases, however, strain builds up in the mismatched layer. Since dislocation nucleation is also exponentially dependent on strain[19], the strain increase will lead to large amounts of nucleation. Dislocation glide is merely linearly dependent on strain, a much weaker dependence[78]. Thus, at low temperatures and high strain levels, nucleation will dominate the dislocation dynamics in the mismatched layer, since dislocation glide alone cannot relax the layer. This experiment directly counters the assertion in some of the literature that relaxed buffer growth at low temperatures is the key to attaining low threading dislocation density because nucleation is limited[79]. The samples in these reports may either have not been totally relaxed, or the threading dislocation counting methodology may have been

inappropriate. Clearly, as established earlier, high temperatures and slow grading rates are the best method to limit threading dislocation densities in SiGe virtual substrates. Furthermore, through use of an intermediate planarization step, we have successfully harnessed dislocation annihilation to reduce excess threading dislocations in a graded buffer for the first time.

3.9 Integration of Ge and III-V Devices with SiGe Virtual Substrates

By including a CMP step in our graded buffer growth and by making several growth modifications, we have grown a 100% Ge virtual substrate that exhibits a final threading dislocation density of approximately 10^6 cm^{-2}. Minor refinements to the growth process have resulted in even lower threading dislocation densities for these Ge-on-Si substrates. There have been other reports in the literature of Ge or GaAs layers on Si with comparable or better threading dislocation densities[11,79-81]. However, none of these reports has bolstered its claims with supporting evidence. In this section, we report superior results from Ge and III-V devices fabricated on our substrates, testifying to their high material quality.

3.9.1 Ge Photodetectors

The 0.66 eV bandgap of Ge has spurred interest in Ge as a material for optical communications applications. However, the large lattice mismatch between Ge and Si has presented difficulties with the integration of Ge photodetectors with Si substrates. The large threading dislocation density that has resulted in previous attempts in the

literature[82,83] have led to high dark currents (and therefore high noise levels) in these Ge detectors. Using the optimized virtual substrates graded to 100% Ge content, Ge p-n mesa photodiodes were fabricated[84]. These detectors displayed ideality factors of 1.1. Under a 1 V reverse bias, these detectors have dark currents of less than 0.2 mA/cm^2. This dark current value is at least two orders of magnitude lower than any previously reported in the literature for a Ge detector on Si. The dark current is also only 3-5 times larger than the theoretically predicted reverse saturation current for such a device, testifying to the high quality of the SiGe virtual substrate. Clearly, the defect density in our substrates has been reduced close to the point where further reductions would have little effect on minority carrier device performance. This implies that the spacing between threading dislocations is now larger than the minority carrier scattering length. This point is reinforced by the results in the next section.

3.9.2 High Efficiency III-V Solar Cells on Si

Previous efforts to successfully integrate GaAs on Si have been thwarted by the 4% lattice mismatch between the materials. The high threading dislocation densities resulting from such mismatch result in poor minority carrier transport, rendering the fabrication of minority carrier devices such as lasers and solar cells impossible. Direct growth of GaAs on Si typically results in threading dislocation densities greater than 10^8-10^9 cm^{-2}. The best previous efforts to reduce this number have involved thermally cycling the material in an attempt to promote dislocation annihilation. The thermal mismatch between the two materials creates strain and hence dislocation glide. This method is analogous to the thick buffer growth described in Sections 1.3.1 and 3.8, and at

best has resulted in dislocation densities in the high 10^6 cm^{-2} range[85-87]. The best reported minority carrier lifetimes in such material are 2-3 ns, compared with the 20 ns lifetimes typical of homoepitaxial, low-doped GaAs films[88]. Obviously, further reductions in threading dislocation density are required for high minority carrier lifetimes in GaAs films on Si.

Utilizing the optimized Ge virtual substrates described earlier, minority carrier lifetimes over 10 ns have now been reported for GaAs films on Si[89]. The lifetime was measured via time-resolved photoluminescence (TRPL) measurements on AlGaAs/GaAs double heterostructures grown on our virtual substrates, and verified by the National Renewable Energy Laboratory. Avoidance of antiphase domain (APD) formation and cross-diffusion at the GaAs/Ge interface normally requires the use of thick GaAs buffer layers. The use of thick GaAs layers on a Si/SiGe/Ge virtual substrates is precluded by the thermal mismatch between GaAs and Si that can lead to surface cracks. However, controlled nucleation of the GaAs film has eliminated both APD formation and cross-diffusion[18,90], allowing these results to be achieved with GaAs buffer layers as thin as 0.1 μm. These high minority carrier lifetimes are the best ever reported for GaAs films on Si, and are a testament to the high quality of our SiGe virtual substrates. These results are compared to calculated minority carrier lifetimes of low-doped n-type GaAs[91] in Figure 3.16.

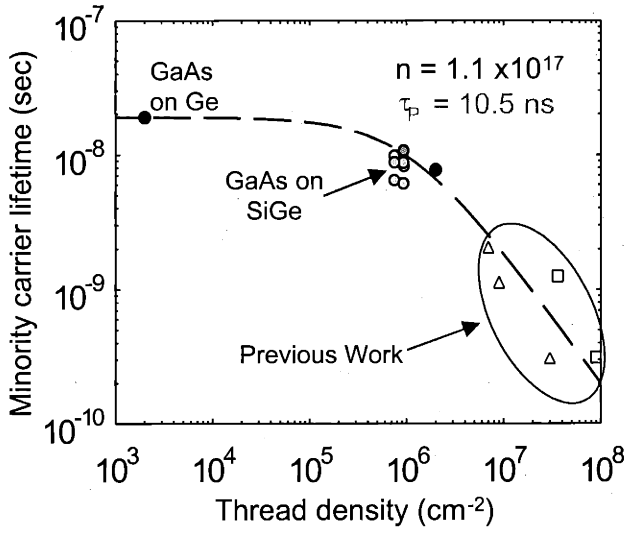

Figure 3.16 Minority carrier lifetimes of GaAs films on Si compared to the calculated curve for low-doped GaAs. The minority carrier lifetime of GaAs grown on the 100% Ge virtual substrates of this study is much higher than any previously reported.

The lifetimes on our SiGe virtual substrates are substantially higher than those previously reported. Our results are also near the point where further threading dislocation density reduction will have little impact on the minority carrier lifetime. Thus, the incorporation of the intermediate planarization step into the SiGe virtual substrate growth has provided the bulk of the necessary threading dislocation density reduction required for good minority carrier transport. Indeed, Ge virtual substrates with threading dislocation densities in the mid-10^5 cm^{-2} range will provide results equivalent to GaAs grown on bulk Ge substrates. Reductions to these levels should certainly be possible with minor growth refinements or a move to a production environment.

Calculations show that single junction GaAs solar cells grown upon our virtual substrates will display efficiencies comparable to the 24-25% AM1.5 efficiencies of

state-of-the-art GaAs/GaAs cells[92]. Indeed, preliminary results from single junction InGaP/GaAs cells grown on SiGe virtual substrates show carrier collection efficiencies that are comparable to cells on GaAs substrates. Open circuit voltages (V_{oc}) of over 980 mV have been obtained in these cells, the highest ever reported for GaAs cells on Si[93].

3.9.3 III-V Light Emitting Devices on Si

The promises inherent in merging conventional Si-based IC technology with the direct bandgap optoelectronic capabilities of III-V semiconductor technology have inspired many different strategies for growing GaAs-based devices on silicon substrates. Minority carrier devices such as laser diodes are the most sensitive to defects resulting from the mismatched GaAs/Si heterojunction. The optimization of SiGe virtual substrates has bridged this once insurmountable lattice mismatch gap, creating device-quality substrates upon which GaAs-based light-emitting and laser diode structures can be grown and evaluated.

AlGaAs visible light emitting diodes (LEDs) and AlGaAs/InGaAs infrared LEDs have been grown with organometallic chemical vapor deposition (OMCVD) on SiGe virtual substrates graded to 100% Ge, and these devices have been characterized and compared with identical structures grown on standard GaAs substrates[94]. Side-emitting double-heterostructure strained quantum well devices were fabricated with $Al_{0.41}Ga_{0.59}As$ cladding layers and an $In_{0.2}Ga_{0.8}As$ active region luminescing at 980 nm. The light is confined to the active region by GaAs separate confinement heterostructure (SCH) layers. A schematic of the device structure is shown in Figure 3.17.

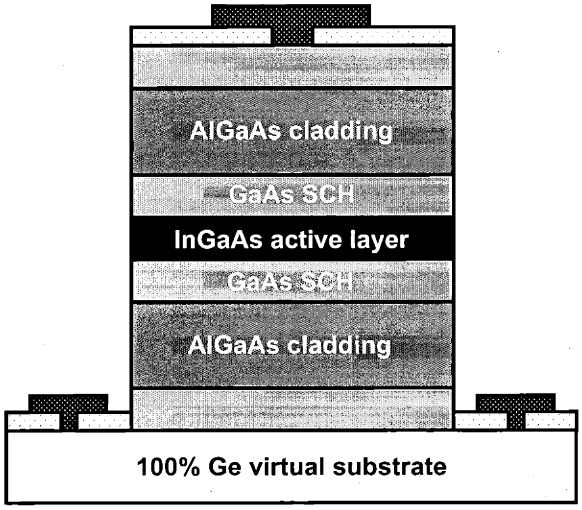

Figure 3.17 Schematic of the InGaAs/GaAs LED structure integrated with Si by use of the 100% Ge virtual substrates.

This device structure with the InGaAs active layer was chosen in order to optimize the material and fabrication process for future attempts at InGaAs-based laser integration with Si. Laser diode active layers containing In are much less prone to the nucleation of dark line defects (DLDs). DLDs occur when large concentrations of point defects condense near threading dislocations, and they impair the reliability of laser diodes. Since DLD formation is more likely in devices containing larger densities of threading dislocations, the In-containing active layer was chosen for integration attempts on the SiGe virtual substrates.

Turn-on voltages of 1.5 V and series resistances on the order of 4 Ω for the InGaAs diodes on SiGe were measured. Similar values were recorded for the devices grown on GaAs, as shown in Figure 3.18.

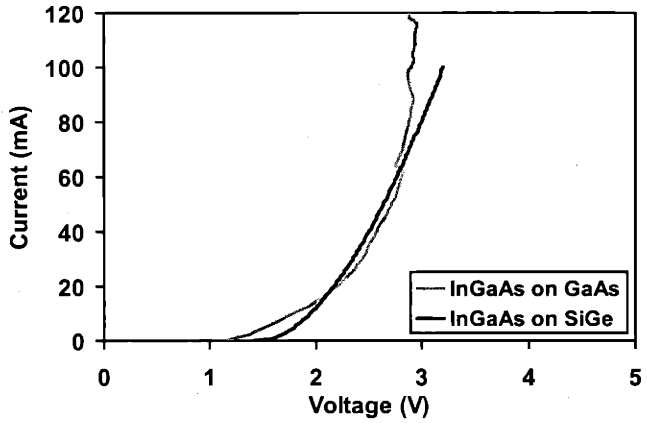

Figure 3.18 Current/voltage characteristics of InGaAs/GaAs LEDs grown on SiGe virtual substrates graded to 100% Ge and on GaAs. Devices on both substrates display similar characteristics.

Electron-beam induced current (EBIC) images of both devices showed threading dislocation densities of approximately 4×10^{6} cm^{-2} for the devices grown on SiGe and much lower densities ($<10^{-4}$ cm^{-2}) in the devices grown on GaAs. Despite the differences in threading densities, both devices showed comparable luminescence characteristics, with external quantum efficiencies slightly more than an order of magnitude apart. Figure 3.19 shows a comparison of the luminescence of the two LEDs. Contact problems, which are responsible for the lower efficiencies, have been found in the devices on the SiGe virtual substrates. Cathodoluminescence (CL) studies, as well as the solar cell results of the previous section, show that the internal quantum efficiencies are very similar for devices on GaAs and SiGe virtual substrates. Optimization of the LED contacts should bring the performance of these devices on par to that of the devices on GaAs substrates.

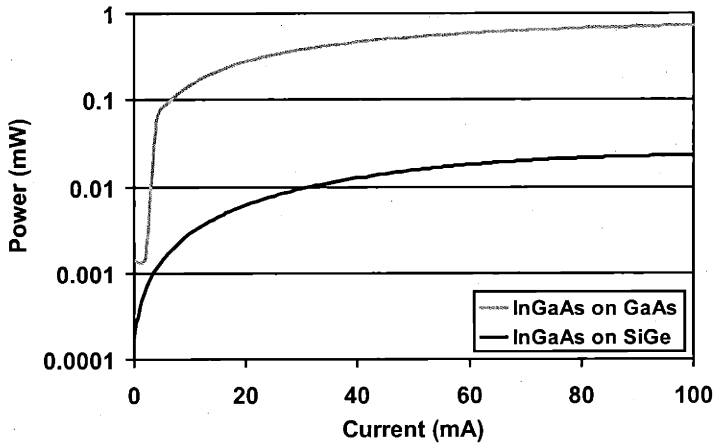

Figure 3.19 **Comparison of the luminescence characteristics of InGaAs/GaAs LEDs grown on SiGe virtual substrates graded to 100% Ge and on GaAs. Poor contacts and a higher threading dislocation density reduce the efficiency of the device on SiGe.**

Chapter 4

Fabrication of Novel SiGe-Based MEMS Devices

4.1 The Potential of SiGe-Based MEMS

Prior to 1997, investigations into the possibility of the utilization of SiGe as a material for MEMS devices culminated with the identification of the etch stop properties of relaxed SiGe at Ge concentrations of 20% or greater. This work was completed in a research collaboration with Draper Laboratories of Cambridge, Massachusetts. The bulk dissolved wafer process[95,96] has been utilized at Draper to fabricate a wide variety of MEMS devices, including gyroscopes and accelerometers. Typically, heavily boron-doped Si is utilized at the etch stop material in this process. The p^{++} Si is obtained either via boron diffusion into the Si substrate or by epitaxial deposition. A schematic of the dissolved wafer process is shown in Figure 4.1.

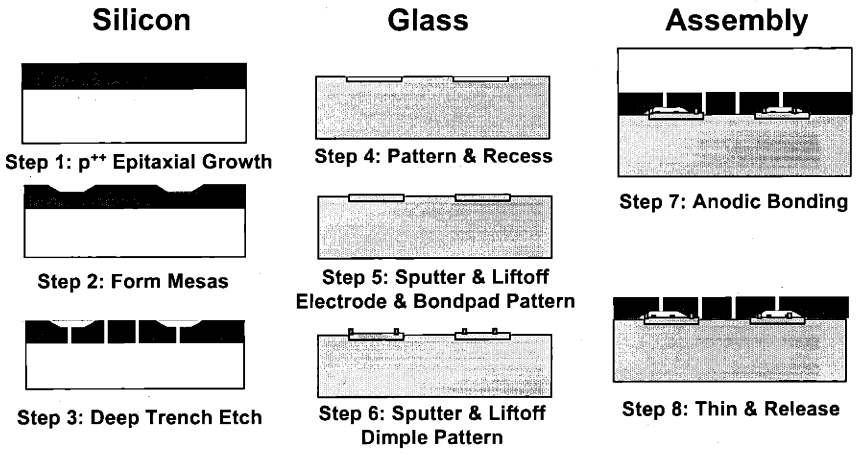

Figure 4.1 Schematic of the dissolved wafer process utilized at Draper Laboratories for the fabrication of MEMS devices.

The etch stop material is patterned, and mesas utilized in the anodic bonding process are formed. Then, the actual MEMS devices are fabricated in the etch stop material via deep trench etching. The glass wafer used in the process has also been patterned, and metal

electrodes and bonding pads have been deposited. The two wafers are then anodically bonded, and the backside of the Si wafer is etched away. The etch selectivity of the etch stop material has a direct effect on the dimensions of the completed part, and hence, a direct effect on the performance of the part. Some of the details of MEMS device design and processing sequences are proprietary to Draper Laboratories and thus cannot be revealed in this document.

Since the favorable etch stop properties of undoped relaxed SiGe material had been identified, the continuing research collaboration with Draper Labs became focused toward the goal of the fabrication of actual MEMS devices with relaxed SiGe. Successful fabrication of MEMS devices with undoped SiGe layers could lead to new integration schemes. On a single SiGe virtual substrate, MEMS devices could be integrated with Si or SiGe-based microelectronics, leading to small, low power sensing solutions for a variety of applications. The use of SiGe could also lead to a reduction in the toxicity of the dissolved wafer process. A "hard," *i.e.* high selectivity, etch stop material like SiGe could enable the use of an etchant like TMAH, which is already used in microelectronics processing in photoresist developer solutions.

4.2 Relaxed SiGe Layer Design for MEMS Fabrication

In order to further the study of relaxed SiGe etch stops and identify the issues facing the replacement of p^{++} Si parts in the MEMS process, new SiGe layers were designed. Since the etch selectivity of relaxed SiGe begins to increase at a Ge content of 20%Ge, a Ge content of 30% was targeted for the parts to obtain a superior etch stop. Our graded

buffer experience was utilized in the design of the new layers. In an effort to limit the threading dislocation density in the final layer, a graded buffer layer was utilized. However, in these structures, the graded layer cannot extend all the way to the 30% SiGe etch stop layer. Since the etch selectivity of SiGe increases at 20% Ge, the etch would stop in the middle of the graded layer, which contains large densities of misfit dislocations. Released parts in this scenario would contain a gradient in Ge content as well as a large density of dislocations. Therefore, a strategic jump was utilized during the relaxed buffer growth. A graded layer was grown to 15% Ge content, whereupon the Ge content was increased to 30% in one jump. Although this 15% jump in Ge content will result in the nucleation of many threading dislocations, the density will be smaller than that of a uniform 30% layer on Si. A uniform 30% Ge cap 13 μm thick was grown for the experiment. The growth was performed at 750°C and 25 mT, and the graded portion was graded at 10% Ge/μm. The uniform cap layer was doped with boron to facilitate electrical contact to the layer. The doping level, less than 10^{18} cm^{-3}, is much too low to influence the etch stop mechanism in these layers. An illustration of the new layer design is shown in Figure 4.2.

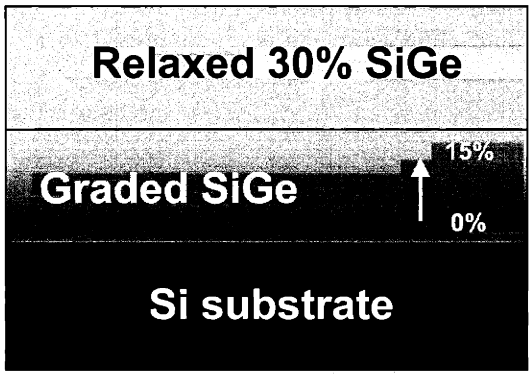

Figure 4.2 Design of relaxed SiGe layers for MEMS device fabrication. The strategic jump in Ge concentration at 15% Ge allows the defective graded buffer region to be etched away with the Si substrate.

Several etch selectivity measurements were performed on the relaxed SiGe layers. The etch selectivity was determined via the use of a cylindrical groove and etch process. This process is shown schematically in Figure 4.3. A cylindrical groove, which extended beyond the etch stop layer, was ground into the wafer. The wafer was then placed in the Si etchant for the selectivity measurement. At the bottom of the groove, the exposed Si etches rather quickly, forming a deep trench. The etch stop layer at the top of the groove etches much more slowly.

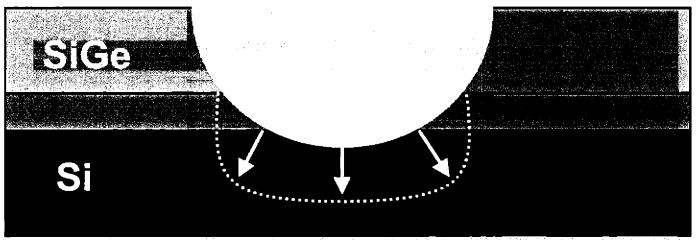

Figure 4.3 Cylindrical groove and etch process for the determination of etch selectivity of the relaxed SiGe layers.

After etching, the surface topology was measured with a WYKO white light interferometer. The selectivity was calculated from the relative etch rates of the SiGe and the underlying Si. For comparison, identical experiments were performed on epitaxial and diffused-boron p^{++} Si layers. The etch selectivity results are shown in Table 4.1. For each etch, the relaxed SiGe displayed the highest selectivity. More importantly, the etch selectivity of the relaxed SiGe layer in 2% TMAH is comparable to the selectivity of p^{++} Si in EDP. Thus, a move to SiGe etch stop material could be coupled with a move to a less hazardous etchant.

Etchant	Boron-diffused Si	p^{++} Epitaxial Si	Relaxed 30% SiGe	Si etch rate (μm/hr)
KOH (11.3%, 85°C)	230	340	1222	61.1
EDP (95°C)	298	410	656	65.6
TMAH (2%, 85°C)	—	—	236	64.3
TMAH (25%, 85°C)	20	12	154	24.7

Table 4.1 Comparison of the etch selectivity of relaxed 30% SiGe with that of boron-diffused and epitaxial p^{++} Si in different Si etchants. For each etchant, the relaxed SiGe exhibits the highest selectivity.

As a test of the SiGe material, tuning fork gyroscopes were fabricated by the dissolved wafer process with various Si etchants. Figure 4.4 is a picture of a section of the comb resonator on the released device.

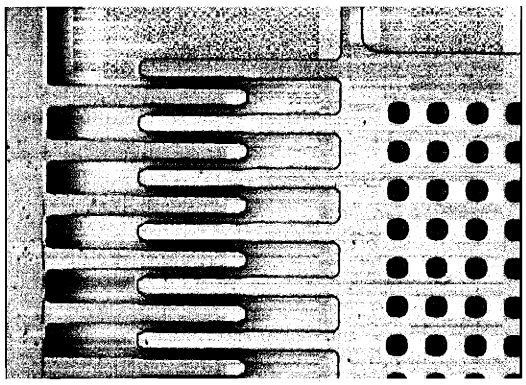

Figure 4.4 Comb resonator of a tuning fork gyroscope fabricated from a relaxed SiGe etch stop material. The comb finger linewidth loss for SiGe in EDP is negligible, less than that in a diffused-boron device.

The width of the comb fingers was decreased by approximately 0.25 μm during an etch in TMAH. This result is identical to the linewidth loss of a p^{++} Si structure etched in EDP[97]. When the SiGe material was etched using EDP, the excellent etch stop performance led to no detectable linewidth loss, an illustration of the superiority of the SiGe material for this application.

4.3 Manufacturability of Relaxed SiGe Etch Stops

Many yield-related issues appear during the movement of a novel material from the research stage to the manufacturing process. Several of the manufacturing challenges specific to relaxed SiGe-based MEMS technology are explored in this section.

4.3.1 Surface Roughness

The Draper dissolved wafer process relies upon anodic bonding of the etch stop layer to a glass substrate, whereupon the rest of the Si wafer is etched away and the parts are released. The surface roughness of the relaxed SiGe layers was identified as a problem,

since strong wafer bonding relies upon very flat surfaces. In addition, lithography on rough surfaces can be problematic due to depth of focus issues. The crosshatch rms surface roughness on the SiGe layers grown for this study was relatively severe, measuring over 22 nm on a 20 μm × 20 μm AFM scan. The SiGe CMP process that was utilized so effectively in previous sections was again used to alleviate the surface roughness problem. The effect of the CMP on the SiGe layer is illustrated in Figure 4.5. Approximately 0.5 μm of SiGe was removed in the process, and the roughness was reduced to approximately 1 nm.

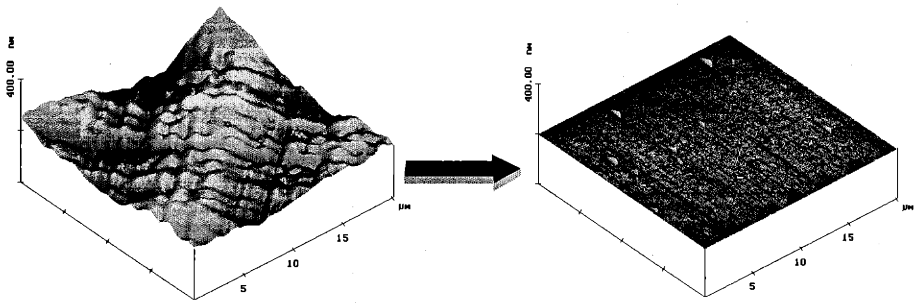

Figure 4.5 AFM scans demonstrating the effect of planarization on the relaxed SiGe MEMS layer. The surface roughness has been decreased from 22.4 nm *(left)* to 1.2 nm *(right)*.

4.3.2 Wafer Curvature

Other issues proved to hinder the manufacturability of the relaxed SiGe etch stops. The thick SiGe layers were originally grown on single-side polished Si wafers. Since the UHVCVD process deposits material on both sides of the wafer, polycrystalline material grows on the backside. The difference in strain from the thick frontside monocrystalline

layer and the thick polycrystalline material on the backside resulted in severe wafer bow. This large wafer curvature creates many of the same problems as the severe surface roughness, presenting problems in the bonding process and resulting in nonuniform lithography. The effect of the wafer bow on the lithography can be seen in Figure 4.6. In the center of the wafer where the bow is most severe, the lithography of the comb fingers was compromised, resulting in unusable devices. The edges of the wafers proved to be in focus, and the parts from the wafer edges were successfully fabricated.

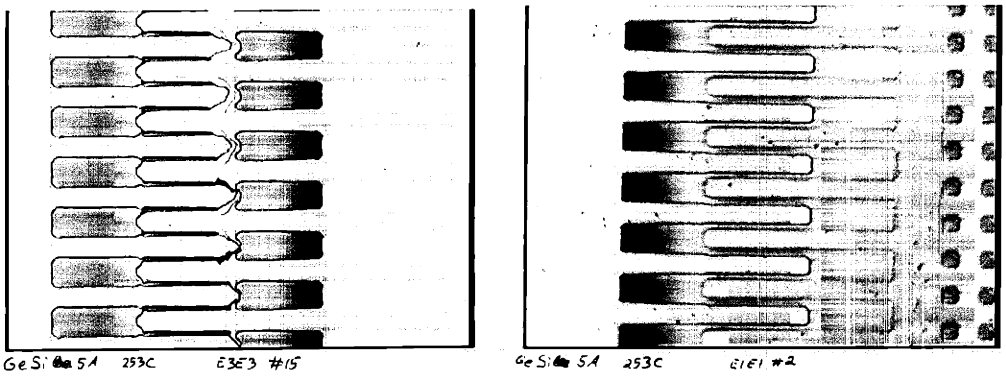

Figure 4.6 Comparison of the fingers of a comb resonator fabricated from the center *(left)* and the edge *(right)* of a wafer with severe wafer bow. The wafer bow compromises the lithography in the center region, leaving the fingers only partially patterned.

To solve this problem, an identical set of SiGe samples was grown on double-side polished Si wafers. Since identical single crystal material is deposited on both sides of these wafers, residual compressive strain exists on both sides of the wafer, leaving the wafer flat. A comparison of the wafer bow of samples grown on single-side and double-side polished wafers is shown in Figure 4.7. The move to double side polished wafers results in wafers of superior flatness, as the amount of strain is exactly matched on both

sides of the wafer. Moreover, most of the wafer bow of the double-side polished wafers was present even before epitaxial growth of the SiGe layer. The wafer curvature is virtually unchanged by the epitaxial growth process, as expected for double-side polished substrates.

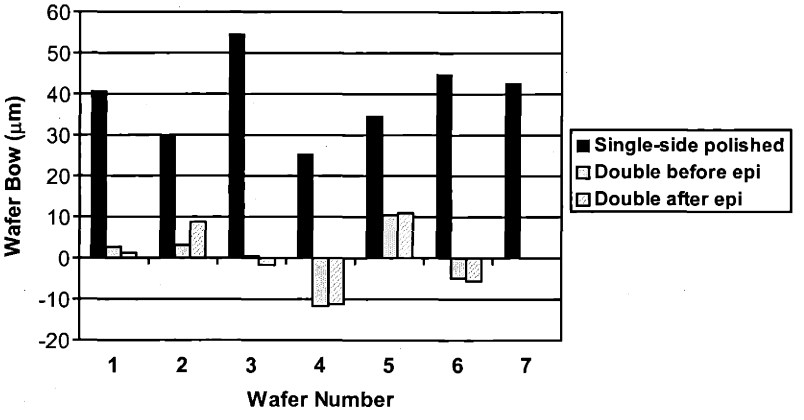

Figure 4.7 **Wafer curvature measurements for relaxed SiGe layers grown on single-side and double-side polished wafers. High levels of compressive strain in the single-side polished wafers lead to large wafer bow. This affect is alleviated by the move to double-side polished wafers, which exhibit virtually the same wafer bow before and after deposition of the SiGe etch stop layer.**

Comb fingers fabricated from the center and edge of the double-side polished wafers are shown in Figure 4.8. As shown, the improved wafer flatness resulted in consistency across the wafer.

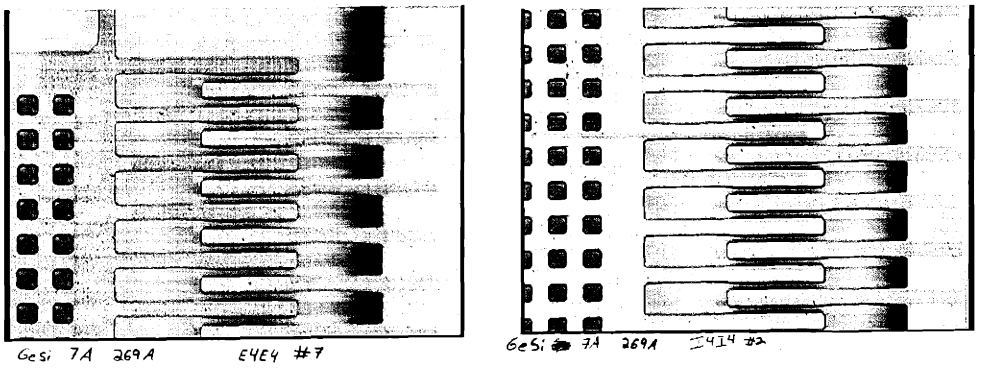

Figure 4.8 **Comparison of the fingers of a comb resonator fabricated from the center *(left)* and the edge *(right)* of a double-side polished wafer with no wafer bow. Elimination of the severe wafer curvature results in consistent lithography across the entire wafer.**

A potential problem with the use of double-side polished wafers is the fact that the wafers are actually subjected to twice the amount of stress, since it is applied on both sides evenly. At large epitaxial layer thicknesses on these wafers, this increased stress can lead to wafer cracking and breakage. An attempt was made to grow thicker relaxed 30% SiGe MEMS layers on double side polished wafers. After the strategic jump in Ge content to 30%, 35 μm thick uniform caps were grown at 750°C. Upon cooling from the growth temperature in the load lock, the large amount of thermal stress in the wafers caused many of them to crack apart. This thermal shock effect could perhaps be alleviated by slower cooling from the growth temperature to room temperature, but 35 μm is certainly an upper thickness limit for 30% SiGe layers grown on double-side polished wafers.

4.3.3 *Part Curvature*

When boron-diffused Si etch stops are used in the dissolved wafer process, curvature in the released parts can result from the gradient in boron content in these layers. This part curvature is remedied by a high temperature annealing step. During the anneal, the boron redistributes and the part flattens. Because the SiGe layers are epitaxially grown and designed to be fully relaxed, problems with part curvature were not anticipated. However, upon fabrication of sample MEMS devices from the SiGe etch stop material, cantilever structures were found to have severe deflections upon release. Figure 4.9 shows the tip deflections of cantilevers made from the relaxed SiGe material. The tip of a 2500 μm beam deflects by an unacceptably high amount, over 30 μm.

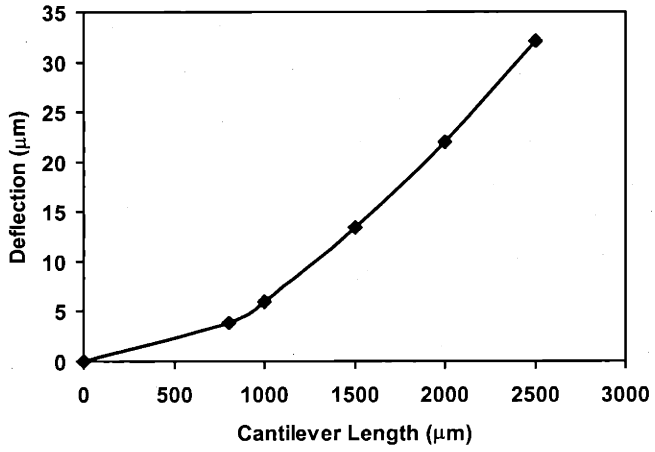

Figure 4.9 Tip deflections of cantilevers made from relaxed SiGe etch stops. This unacceptably high part curvature was eliminated via high temperature annealing steps.

SIMS scans of the as-grown material displayed exceptional uniformity in both Ge and boron content in the layers, so an explanation of this part curvature remained elusive.

XTEM studies of the thick uniform SiGe layers finally provided the microstructural clues behind the part curvature problem. Networks of misfit dislocations were observed within the uniform layer itself, rather than being totally confined to the interface with the graded layer underneath. An XTEM micrograph showing these misfit dislocations in the thick uniform layer is shown in Figure 4.10.

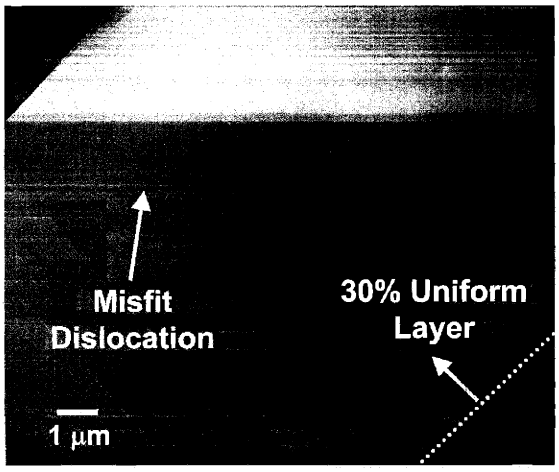

Figure 4.10 Cross-sectional TEM micrograph of the thick relaxed SiGe layer for MEMS fabrication. Networks of misfit dislocations, caused by continued relaxation of the thick uniform layer, can be seen throughout the thickness of the layer.

Normally, relaxed mismatched layers retain an equilibrium amount of lattice strain that is not offset by misfit dislocation introduction. As the thickness of such a layer increases, further relaxation occurs and this equilibrium strain level decreases. As the SiGe layer was grown to a thickness of over 10 μm, misfit dislocations were injected, resulting in continued relaxation. These dislocations create slight gradients in the lattice constant of the released etch stop layer and lead to the cantilever beam deflections. Much like with the boron-diffused material, this curvature of the cantilevers was eliminated via

high temperature annealing. The high temperature anneal allows a redistribution of Ge in the layer, resulting in flat devices. Exact details of the annealing process are proprietary to Draper Laboratories.

4.3.4 Part Strain

One remaining problem with the implementation of relaxed SiGe etch stop material in the Draper dissolved wafer MEMS process is the issue of part strain. Upon fabrication, high amounts of strain were observed between the SiGe parts and the glass substrates to which they were bonded. Specially designed pointer beam structures in the released parts allow an accurate measurement of the part strain. Figure 4.11 shows pictures of a pointer beam. The beam is roughly T-shaped, with the pointer at the bottom tip. The left and right tines of the T are slightly offset. Therefore, upon release of the pointer beam, tensile part strain will cause the pointer to deflect in one direction; compressive strain will have the opposite effect. A corrugated scale near the tip of the pointer beam allows accurate conversion of the pointer beam deflection into remnant part strain.

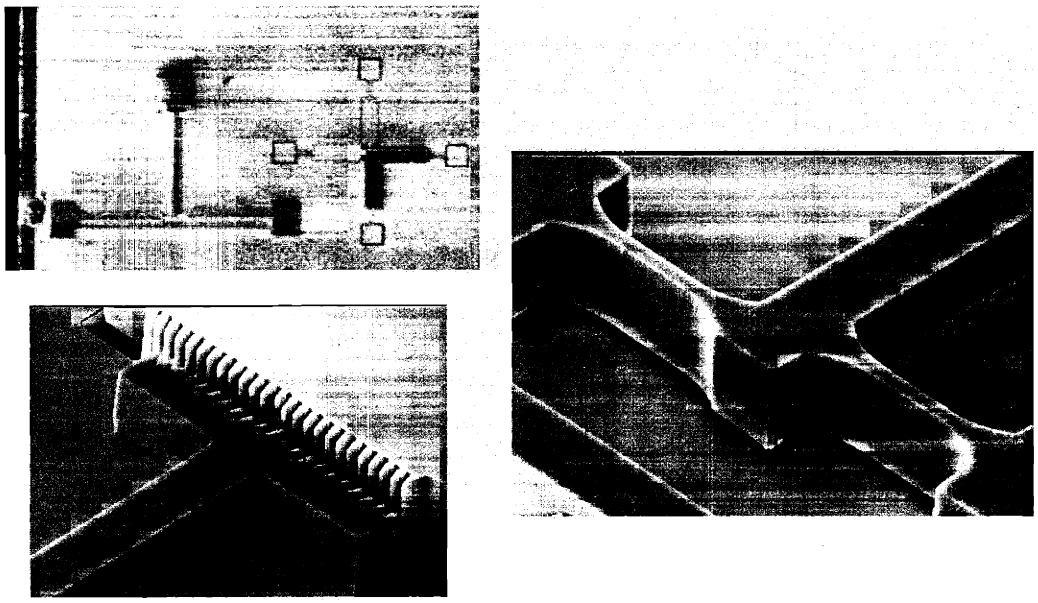

Figure 4.11 SEM micrographs of the pointer beam structure utilized for part strain determination.

Part strain results from the thermal expansion mismatch between the SiGe and the glass used in the process. Figure 4.12 shows a comparison of the thermal expansion mismatch strain experienced by Si parts and SiGe parts upon cool down from the anodic bonding temperature.

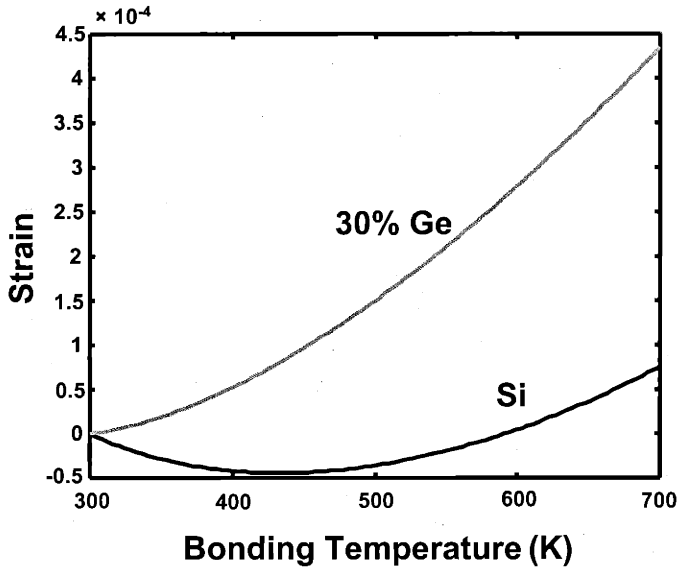

Figure 4.12 Comparison of the thermal expansion mismatch strain experienced by Si and SiGe MEMS layers bonded to glass substrates. The appropriate choice of bonding temperature will leave the Si part strain-free, but the SiGe part ends up tensile regardless of bonding temperature.

The choice of an appropriate bonding temperature will result in a net zero strain in a Si part because the thermal mismatch strain changes from compressive to tensile at approximately 600 K. Unfortunately, the final thermal mismatch strain between 30% SiGe and the glass is tensile over the entire bonding temperature range. Bonded SiGe parts will therefore always display high strain levels after processing. Although working SiGe MEMS structures were fabricated with this process, this part strain remains a concern. Possible solutions being investigated include the use of different types of glass substrates. Many types of glass have been engineered with various thermal properties, and one could be chosen to eliminate this part strain. Alternatively, compressive layers could be incorporated into the SiGe layer itself to cancel out the tensile part strain.

Obviously, the use of such layers would preclude the high temperature annealing step of the previous section, which would lead to relaxation of the compressive strain.

4.4 Summary of SiGe-Based MEMS Results

Relaxed SiGe layers for MEMS began as a simple laboratory curiosity with the identification of their etch stop properties, their full potential unutilized. From that point, relaxed SiGe layers have been engineered for use in the Draper Laboratories dissolved wafer MEMS fabrication process. These materials enabled the change from the use of the highly toxic EDP etchant to that of the more benign TMAH. Several problems were overcome in order to make the fabrication of MEMS components a reality. The problem of part curvature was resolved via high temperature annealing to redistribute small gradients in Ge. The use of double-side polished wafers eliminated wafer curvature, facilitating the anodic bonding and lithography processes. The application of the CMP process perfected in the graded buffer work presented in the previous chapter resulted in crosshatch-free smooth wafer surfaces. Possible solutions to the issue of part strain were also identified. The MEMS devices fabricated to date with relaxed SiGe display extremely good etch selectivity and capability for integration with other microelectronic devices.

Chapter 5

SiGe Virtual Substrates for the Fabrication of Strained Si MOSFETs

As detailed in Section 1.6.5, when a thin layer of strained Si is grown on relaxed SiGe, the resulting type-II band offset forms a potential well for electrons. Additionally, the biaxial tensile strain in the Si layer splits the six-fold degeneracy of the conduction band, lowering the two perpendicular valleys in energy relative to the four in-plane valleys. Electrons confined to these lower energy Δ_2 valleys experience both a reduction in in-plane electron mass and a reduction in intervalley phonon scattering, increasing their mobility. The first efforts to produce modulation-doped tensile strained Si layers utilized highly defective, uniform SiGe substrate layers[37,98]. The 4 K electron mobilities of these early attempts ranged from 2-17×10^3 $cm^2/V•s$, no higher than the mobilities of bulk NMOS inversion layers. Clearly, the strained Si electron mobilities were limited by the high density of threading dislocations in the uniform SiGe layers, well over 10^8 cm^{-2}. The advent of the SiGe relaxed graded buffer technique in 1991[12,13] enabled the growth of relaxed SiGe layers with vastly reduced threading dislocation density. Immediately, the maximum mobilities of tensile strained Si layers increased by more than a factor of five, reaching 1-2×10^5 $cm^2/V•s$ on these virtual substrates at 4 K[99,100]. Since then, relaxed graded SiGe has continued to act as a substrate for high carrier mobility layers. SiGe virtual substrates have enabled record silicon electron mobilities of 2830 $cm^2/V•s$ at room temperature[39] and over 8×10^5 $cm^2/V•s$ at 15 K[40]. Record Ge hole mobilities of 1870 $cm^2/V•s$ at room temperature[34] and 55,000 $cm^2/V•s$ at 4.2 K[35] have also been achieved in this materials system.

Another benefit of SiGe-based heterostructure devices is their inherent compatibility with the Si microelectronic fabrication process. With the fabrication of

SiGeOI material[101-103], the performance benefits of Si/SiGe heterostructures can also be combined with the decreased capacitance and lower leakage of an insulating substrate. Thus, SiGe technology provides an inexpensive way to extend the capabilities of the Si platform into the high performance realm dominated by III-V devices. Strained Si/SiGe devices have the potential to dominate both high speed digital CMOS and high frequency analog device spaces.

Enhanced carrier mobilities allow strained Si MOSFETs to exhibit vastly increased performance over their bulk Si counterparts at identical gate lengths. These performance gains are independent of traditional Si MOSFET scaling laws and device geometries. Buried channel strained Si devices generally have higher low-field mobilities and lower noise characteristics, making them suitable for high-frequency applications[104]. For high electric field applications like state-of-the-art CMOS, the improved scalability and increased high-field mobility enhancement of the surface channel strained Si device allow it to excel[105]. Increased performance has also been observed in deep submicron strained Si n-MOSFETs[45], demonstrating the benefits of these structures at the high electric fields of state-of-the-art CMOS operation. Biaxial tensile strain also splits the degeneracy of the valence band in Si, enabling the fabrication of enhanced hole mobility surface channel strained Si p-MOSFETs[106].

In this study, we have fabricated surface channel strained Si n- and p-MOSFETs via a novel short-flow MOSFET process incorporating a deposited SiO_2 gate dielectric and high temperature implant activation anneals. The effect of increasing strain on carrier mobilities was investigated, and the saturation of the mobility enhancement in

these structures is compared. The process stability of these devices is also investigated, including the effects of well implantation, implant activation anneal temperature, and CMP of the SiGe virtual substrate on carrier mobility enhancement. The effect of Si channel thickness on electron mobility is also investigated for surface channel n-MOSFETs.

5.1 Growth and Characterization of Si/SiGe MOSFET Heterostructures

5.1.1 UHVCVD Growth of Strained Si Device Structures

Many different device structures were fabricated during the course of this study. The SiGe virtual substrates were grown to Ge contents of 10-30% at 900°C, 25 mT, a grading rate of 10% Ge/μm, and were topped by a 1.5 μm uniform composition cap. The slow grading rate and high growth temperature result in completely relaxed graded layers with threading dislocation densities of approximately 10^5 cm^{-2} and low surface roughness[71]. Some samples were doped *in situ* n- or p-type to concentrations of 1×10^{16} cm^{-3}. The reactor temperature was then dropped to 650°C for the deposition of the strained Si device structure. 0.5 μm of SiGe matching the final Ge content of the graded buffer was deposited, followed by the desired strained Si channel thickness. In general, strained Si thicknesses less than the equilibrium critical thickness were chosen to eliminate misfit dislocation introduction during elevated processing temperatures. This offers a sharp contrast to typical strained Si device fabrication methods, in which thick, metastable Si layers are grown at low temperatures and the processing thermal budget is decreased

dramatically to prevent strain relaxation. A schematic and a band diagram of a typical device structure are shown in Figure 5.1.

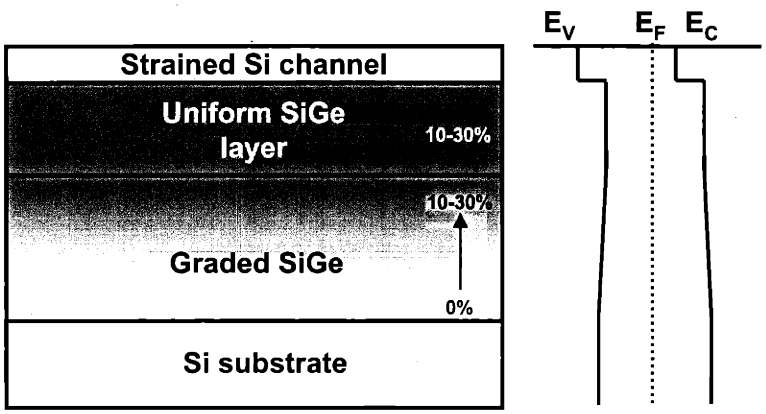

Figure 5.1 Layer structure and band diagram of a typical surface-channel strained Si MOSFET grown by UHVCVD.

5.1.2 Device Structure Characterization

The Ge content of the virtual substrates was confirmed by XRD measurements of the lattice parameter on a Bede D^3 X-ray diffractometer. XTEM was performed to verify the strained Si channel thicknesses. Selective chemical etching with the dilute Schimmel etchant was performed to verify the absence of misfit dislocations in the strained Si layer. This type of selective etching, basically an EPD measurement, is one of the most sensitive methods for detecting low densities of misfit dislocations in strained layers. Other methods, such as X-ray diffraction and Raman scattering, are insensitive to misfit dislocation densities below 10^5 cm^{-2}[153]. The potential margin of error when utilizing one of these methods to determine the level of relaxation in strained Si layers can be estimated by the following formula:

$$S = \frac{b_{eff}}{\delta},$$

in which the misfit dislocation spacing S is related to the effective Burgers vector of the Si film and the plastic strain δ[8]. The misfit dislocation density is simply the inverse of the misfit spacing, and b_{eff}, the in-plane component of the Burgers vector, is b/2. Hence,

$$\delta = \frac{b\rho_{MD}}{2}.$$

Thus, taking b as 4 Å, the potential plastic strain relief in a strained Si layer with a misfit dislocation density of 10^5 cm^{-1} is 0.2%. Since the total mismatch strain between Si and Ge is approximately 4%, this potential error is equivalent to an uncertainty of 5% Ge content in the virtual substrate. Since the selective etching technique allows the measurement of vastly smaller misfit dislocation densities over very wide areas, more accurate measurements of the film strain state can be obtained. Moreover, thin Si films can be assumed to be fully strained if misfit dislocations are not revealed by the selective etch.

5.2 Short-Flow MOSFET Process

The strained Si MOSFET processing was performed in the Integrated Circuits Lab (ICL) and the Technology Research Lab (TRL) of the MIT Microelectronics Technology Laboratory. In order to facilitate the investigation of many device structural variants, a novel short-flow MOSFET process was utilized. In this process, large geometry (~100-200 μm) ring transistors are fabricated with a single lithography step[107]. Room temperature electrical measurements were then performed on finished devices using a

Hewlett Packard 4145B Semiconductor Parameter Analyzer and a Hewlett Packard 4192A LF Impedance Analyzer.

5.2.1 Motivation for the Short Flow MOSFET

The primary device metric extracted from the large MOSFETs fabricated in this study is the effective carrier mobility. Carrier mobilities can also be extracted from strained Si heterostructures via measurement of the Hall mobility. However, the Hall mobility differs from the MOSFET drift mobility by the Hall scattering factor. This factor differs for various scattering mechanisms and has not been extensively studied in strained Si. Thus, the most realistic measure of performance of strained Si heterostructures is via the fabrication of actual MOSFETs. Typical MOSFET processes can take months, even under ideal conditions, limiting the number of variants that can be processed over time. The short-flow MOSFET process has been designed to take 1-2 weeks in the MIT lab, vastly increasing device turnaround.

5.2.2 MOSFET Fabrication Process

A plan view schematic of a short-flow MOSFET is shown in Figure 5.2. The ring geometry of the device allows it to be fabricated with a single lithography step yet remain electrically isolated from the rest of the substrate. The main steps of the processing sequence are illustrated in Figure 5.3 and described in detail below.

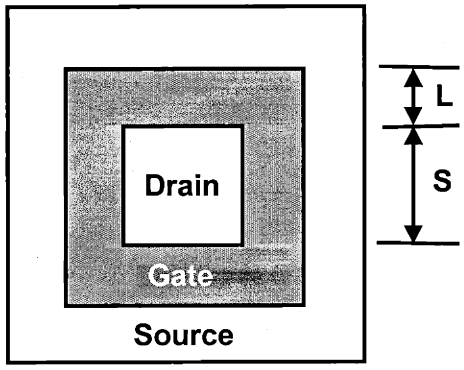

Figure 5.2 **Plan view schematic of a short-flow ring transistor. The dimensions L and S are utilized in device mobility extractions.**

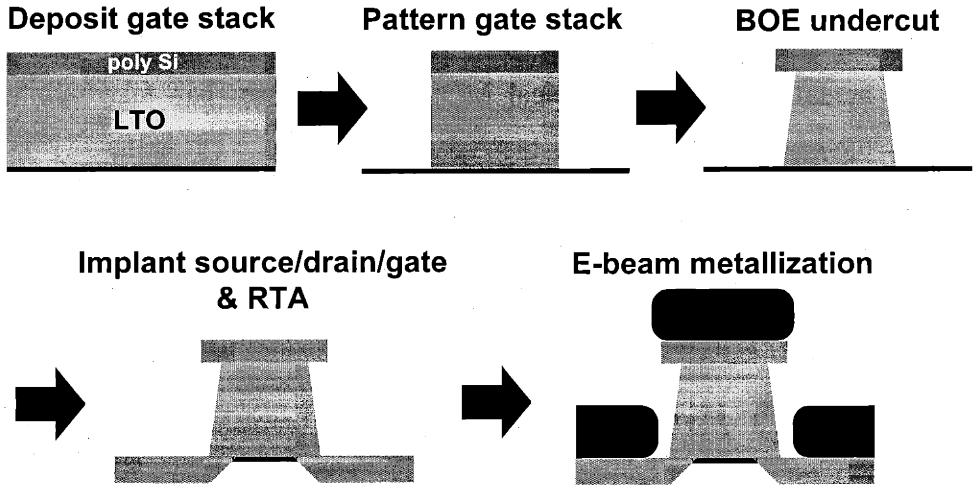

Figure 5.3 **The short-flow MOSFET processing sequence. The transistors are fabricated with a single lithography step. Much like a traditional lift-off process, the metal is patterned upon deposition by the geometry of the device.**

Gate Stack Deposition

The standard cleaning procedure prior to a MOSFET gate oxidation is the three-part RCA clean. The initial SC-1 step, a 5:1:1 mixture of water (H_2O), hydrogen peroxide (H_2O_2),

and ammonium hydroxide (NH_4OH), is typically performed at 80°C for 10 minutes. The SC-1 removes organic contaminants from the wafer, and etches Si quite aggressively at a rate of 5 Å/min. The thin oxide formed in this step is removed during a 30 second dip in 50:1 H_2O:HF. The final SC-2 step, a 6:1:1 mixture of H_2O, H_2O_2, and hydrochloric acid (HCl), is performed at 80°C for 15 minutes. The short-flow MOSFET process begins with a modified RCA clean, with either an abbreviated SC-1 step (< 3 minutes) or a piranha clean in place of the traditional 10 minute SC-1 clean. The less aggressive clean prevents rampant etching of the thin surface strained Si device layer. The modified clean is followed by deposition of the 3000 Å thick SiO_2 gate dielectric via low pressure chemical vapor deposition (LPCVD) at 400°C. The choice of an LTO gate dielectric is not made to preserve a low thermal budget for the process. Rather, a thick oxide is *required* for this short-flow process. Since thermal oxidation would entirely consume the thin strained Si channel layer, we must resort to the use of a deposited gate dielectric. Capacitors fabricated with densified MIT LTO have demonstrated interface state densities on par with thermal oxides ($\sim 5\times10^{10}$ cm^{-2} eV^{-1}), a testament to the high quality of this deposited oxide[107]. The LTO layer was followed by deposition of 500 Å of polysilicon at 560°C to complete the gate stack.

Backside Clear and Device Patterning

The LTO and polysilicon on the wafer backside are etched away to facilitate backside electrical contact. After coating the front sides of the wafers with photoresist, the backside polysilicon is removed with a HBr/Cl_2 dry etch chemistry in an Applied Materials Precision 5000 reactive ion etcher (RIE). Next, the wafers are dipped into a

buffered oxide etch (BOE) bath to remove the backside LTO. After resist removal, ring transistors are patterned in the sole lithography step of the process with the MOBIL mask. The MOSFETs are then defined via RIE etching. The polysilicon is again etched with HBr/Cl_2, and the LTO is etched with a CHF_3/O_2 mixture. The LTO etch is stopped approximately 100 Å away from the wafer surface to prevent surface damage from the dry etch. The wafers are then subjected to a 15 second BOE dip to remove the remaining LTO from the source and drain regions. This step also serves to underetch the gate polysilicon and form a large "T-gate" geometry that will be essential for the metal deposition step.

Source/Drain/Gate Implantation and Anneal

Uniform BF_2 or As ion implants are performed at 35 keV to dope the source, drain, and gate contact regions. Four identical implants were used, each after a 90° rotation of the wafer, to prevent shadowing effects due to the T-shaped geometry of the gate. The implants are performed at an outside vendor, and the wafers are piranha-cleaned upon reintroduction to the lab. This is followed by a high temperature activation rapid thermal anneal (RTA) in a nitrogen (N_2) ambient in an AG Associates Heatpulse 210. The RTA is typically performed at 1000°C for 1 second. Because the strained Si layers are at equilibrium and not merely metastable, no relaxation via misfit dislocation introduction occurs during this high temperature step.

Device Metallization

Next, the wafers are subjected to a standard pre-metallization clean to insure that good ohmic contacts to the devices are obtained. This clean consists of a piranha clean followed by a 20 second 50:1 HF dip. Blanket Ti/Al metallization is then performed in a Temescal e-beam deposition system. Typically, 500 Å of Ti and 1000 Å of Al are used. Specially designed wafer holders are used during the e-beam metallization to insure perpendicular incidence of the metal. Due to the extreme geometry of the "T-gate" MOSFET structure, breaks occur in the metal which isolate the source, gate, and drain regions without further lithography, much like a traditional liftoff process. The metallization self-patterning process is the motivation behind the use of such a thick gate dielectric. A thinner gate stack would result in the metal shorting between the source/drain and the gate, rendering the device useless. The backside contact is formed via deposition of 1 μm of Al. A 30 minute 400°C sinter in forming gas (5% H_2 in N_2) completes the MOSFET fabrication. Figure 5.4 shows an XTEM micrograph of a completed short-flow MOSFET structure. The details of the processing sequence, including the MTL machine names, are included in Table 5.1.

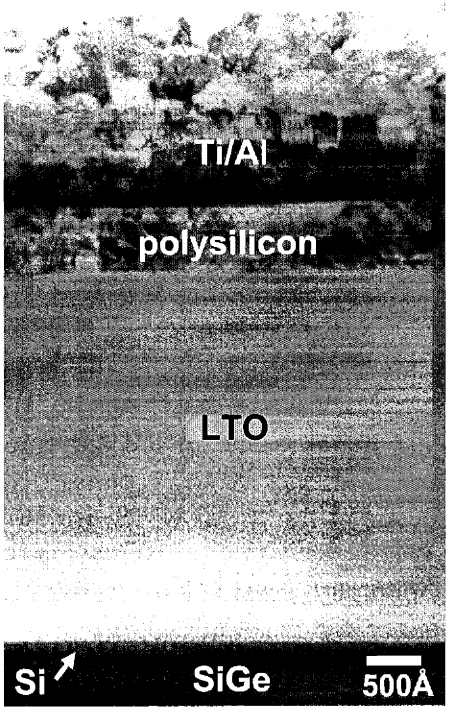

Figure 5.4 **Cross-sectional TEM micrograph of a short-flow MOSFET gate stack.**

Machine Name	Step Description
Gate Stack Deposition	
rca	Abbreviated RCA clean
TubeA7	3000 Å LTO deposition
TubeA6	500 Å polysilicon deposition
Backside Clear	
HMDS	HMDS deposition
Coater6	Coat frontsides & hardbake resist
AME5000	Etch backside polysilicon
oxide	BOE etch backside LTO
asher	Ash photoresist
Device Patterning	
HMDS	HMDS deposition
Coater6	Photoresist coat
Stepper2	Exposure with MOBIL mask
Developer	Photoresist develop
Coater6	Postbake resist
AME5000	Etch frontside polysilicon
UV1280	Check LTO thickness
AME5000	Etch frontside LTO
asher	Ash resist
oxide	BOE undercut of polysilicon
Source/Drain Implantation	
Outside vendor	Implant source/drain/gate
Premetal	Post-implantation piranha clean
RTA2	RTA at 1000°C for 1 second
Metallization	
Premetal	Pre-metallization piranha clean
e-beam	500 Å Ti/1000 Å Al at zero tilt
e-beam	1 μm Al on backsides
TRL tubeA3	400°C sinter in H_2/N_2 for 30 minutes

Table 5.1 **Detailed short-flow MOSFET processing sequence. Machine names are MTL designations.**

5.3 Carrier Mobility Extraction

In order to investigate the carrier mobility enhancement in the strained Si MOSFETs, the effective mobility as a function of effective vertical electric field[108,109] was calculated for each set of devices. This relation is the basis for the "universal mobility" curves for Si MOSFETs, in which the inversion layer mobility is independent of substrate doping[110]. Figure 5.5 shows a schematic of the universal curve of bulk Si MOSFET mobility at room temperature.

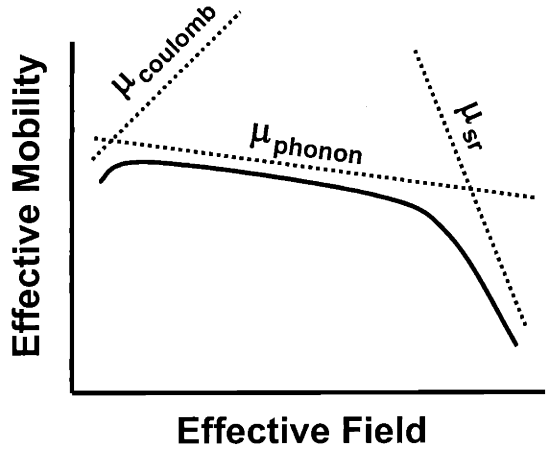

Figure 5.5 Schematic of the universal mobility curve of Si MOSFETs at room temperature. Carrier mobility is limited by Coulomb scattering, phonon scattering, and surface roughness scattering.

Three regimes of mobility behavior are evident in this figure. At low fields, carrier mobility is dominated by Coulomb scattering, which is more effectively screened out at higher fields (and thus higher carrier densities in the inversion layer). At moderate fields, the carrier mobility is determined by phonon scattering. Phonon scattering depends on $E_{eff}^{-0.3}$ for electrons and has a slightly stronger dependence for holes. A decrease in

temperature will raise the phonon scattering-limited mobility. Finally, in the high field regime, surface roughness scattering dominates carrier mobility, with a dependence of E_{eff}^{-2} for electrons and E_{eff}^{-1} for holes. It will be shown in Section 5.6 that surface strained Si MOSFETs also follow a universal behavior in which mobility is independent of substrate doping.

The effective carrier mobility μ_{eff} was extracted from the linear regime device current, given by:

$$I_D = \frac{W}{L}\mu_{eff} C_{ox}(V_{GS} - V_T)V_{DS}$$

where *W/L* was replaced by the appropriate factor for the transistor's ring geometry[107]. Rearranging the equation after this substitution, we obtain:

$$\mu_{eff} = \frac{GI_D}{C_{ox}V_{DS}(V_{GS} - V_T)}$$

where C_{ox} is the gate oxide capacitance, V_T is the threshold voltage, V_{GS} is the applied gate-source voltage. The source-drain voltage V_{DS} was fixed at 100 mV, and the geometry factor *G* is found in Table 5.2.

Device Name	L (μm)	S (μm)	G
500M250	500	250	0.240
200M250	200	250	0.138
100M250	100	250	0.081
50M250	50	250	0.045

Table 5.2 **Geometry factor G for various devices found on the MOBIL mask used in the short-flow MOSFET process. The dimensions L and S are indicated on Figure 5.2. Table originally appeared in Armstrong[107].**

The effective vertical field E_{eff} is given by:

$$E_{eff} = \frac{Q_b + \eta Q_{inv}}{\varepsilon_S}$$

where η is a fitting parameter. Typically, values of 1/2 for electrons and 1/3 for holes are chosen for η in order to attain the universal mobility behavior described above. Q_b is the bulk depletion charge, and Q_{inv} is the inversion layer charge. Because of uncertainties in the substrate doping of the device substrates, particularly those without *in situ* doping, the normal $N_a x_{d,max}$ approximation for the bulk charge was not used. Instead, the following formulation was utilized. From electric displacement continuity at the oxide/semiconductor interface, we know that:

$$E_{ox}\varepsilon_{ox} = E_S\varepsilon_S$$

where E_{ox} is the electric field in the gate oxide, E_S is the peak electric field at the semiconductor surface, and ε_{ox} and ε_S are the dielectric constants of the oxide and the semiconductor, respectively. E_S can be derived from Gauss's Law as:

$$E_S = \frac{Q_{inv} + Q_B}{\varepsilon_S}$$

and thus, the bulk charge can be approximated as:

$$Q_b = E_{ox}\varepsilon_{ox} - Q_{inv}$$

resulting in:

$$E_{eff} = \frac{E_{ox}\varepsilon_{ox} - (1-\eta)Q_{inv}}{\varepsilon_S}.$$

Q_{inv} was taken as $C_{ox}(V_{GS}-V_T)$, and E_{ox} was assumed to be equal to V_{GS}/t_{ox}, which holds for cases when the MOSFET channel is at approximately the same potential as the source, *i.e.* $V_{DS} << V_{GS}$[111]. C_{ox} is the oxide capacitance and t_{ox} is the oxide thickness. ε_S of the SiGe virtual substrate was linearly interpolated from the values for Si and Ge, ε_{Si} = 11.9 and ε_{Ge} = 16.0. Thus, our final formulation for the effective field is given by:

$$E_{eff} = \frac{C_{ox}\left(V_T + \eta\left(V_{GS} - V_T\right)\right)}{\varepsilon_S}.$$

Once the effective mobility and effective field were calculated for the strained Si MOSFETs, the mobility characteristics could be compared to the universal curves.

5.4 Effect of Strain on Electron Mobility

The amount of strain in the surface strained Si channel was varied via growth of SiGe virtual substrates to Ge contents of 10-30% on p^- Si wafers. A channel thickness of 100 Å was chosen for all of the devices. Selective etching experiments were performed to verify the absence of misfit dislocations in the strained Si layers. Thus, all of the layers were fully strained in this experiment. N-channel MOSFETs were fabricated via the short-flow process outlined in Section 5.2, and the carrier mobilities were evaluated as a function of strain in the Si layer. Devices were also coprocessed on a bulk Si wafer for comparison.

Figure 5.6 shows the effective electron mobility vs. effective field data for the strained Si NMOS devices and a coprocessed bulk Si device. The peak mobilities obtained, nearly 1000 $cm^2/V\cdot s$ at 0.1 MV/cm, are comparable to the highest values for surface channel strained Si NMOS previously reported[41].

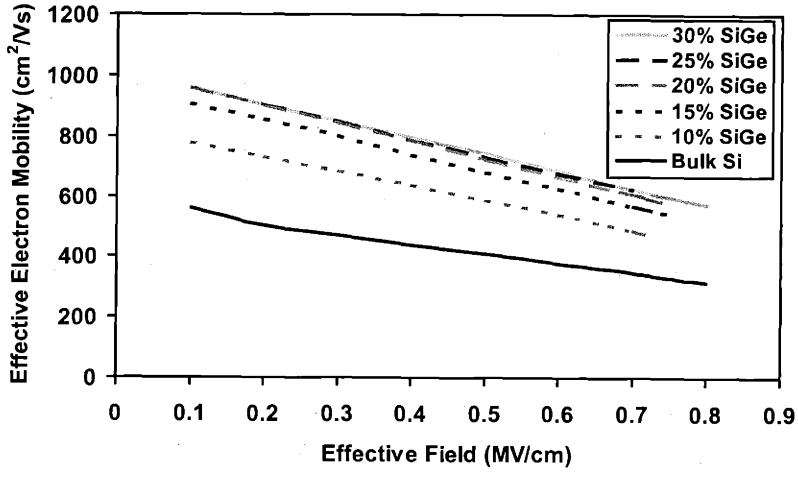

Figure 5.6 **Effective electron mobility data for surface channel strained Si MOSFETs on various SiGe virtual substrates. Electron mobility increases with strain, but saturates for substrate Ge contents 20% and greater.**

The high mobilities are a testament to the high quality of our device material. This result also underscores the importance of the short-flow MOSFET process. Our short turnaround process enables the investigation of scores of MOSFET materials variants in less time than the completion of a single standard CMOS lot. For students processing devices in a university lab, the usefulness of the short-flow process as a diagnostic tool cannot be understated. Figure 5.7 shows the electron mobility enhancement of the strained Si devices as a function of the effective vertical field. All values are in comparison to the coprocessed bulk Si device.

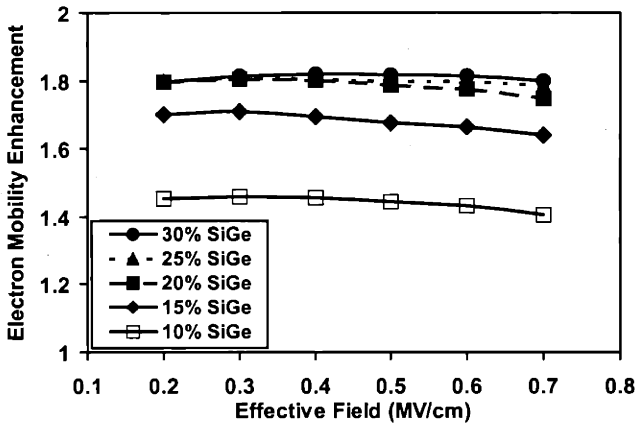

Figure 5.7 Strained Si electron mobility enhancement over coprocessed bulk Si devices. Mobility enhancements are relatively independent of effective field.

The mobility enhancements for each device are relatively constant over the entire field range, and the enhancement saturates at around 1.8 for devices having substrate Ge contents over 20%. The saturation of electron mobility arises because at these strain levels, the subband splitting in the Si conduction band is large (>130 meV). Thus, all of the carriers occupy the lower-energy Δ_2 subbands and intervalley phonon scattering is suppressed. This behavior is in excellent agreement with theoretical studies of electron mobility enhancement in strained Si MOSFETs[112]. The mobility enhancements of these devices do drop off very slightly at high fields, due to the unexpectedly high mobility of the bulk Si device at high fields. This may be due to low interface roughness between the bulk Si wafer and the deposited LTO gate dielectric, as this behavior is also observed in the p-MOSFETs of Section 5.5. When compared to the mobility of the 10% SiGe device, as in Figure 5.8, we see that the mobility enhancements of the other devices remain constant with increasing effective field.

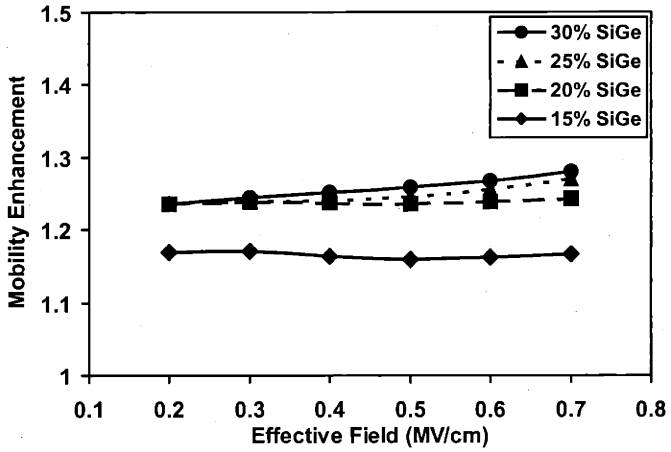

Figure 5.8 Strained Si electron mobility enhancement over that of the strained Si device on 10% SiGe. The mobility enhancements of the other devices are independent of effective field.

Figure 5.9 shows the electron mobility data plotted on a logarithmic scale. At moderate fields of 0.3-0.5 MV/cm, we observe the normal $E_{eff}^{-0.3}$ dependence of phonon-limited mobility. The electric field dependence strengthens at higher fields, signifying the onset of surface roughness as a limiting mechanism. At low fields, the mobilities of both the strained Si and the bulk MOSFETs display a weaker dependence on electric field. This is likely due to higher oxide charge in the deposited LTO than is present in dry thermal oxides of state-of-the-art MOSFETs, as this is known to weaken the dependence of mobility at moderate fields[110].

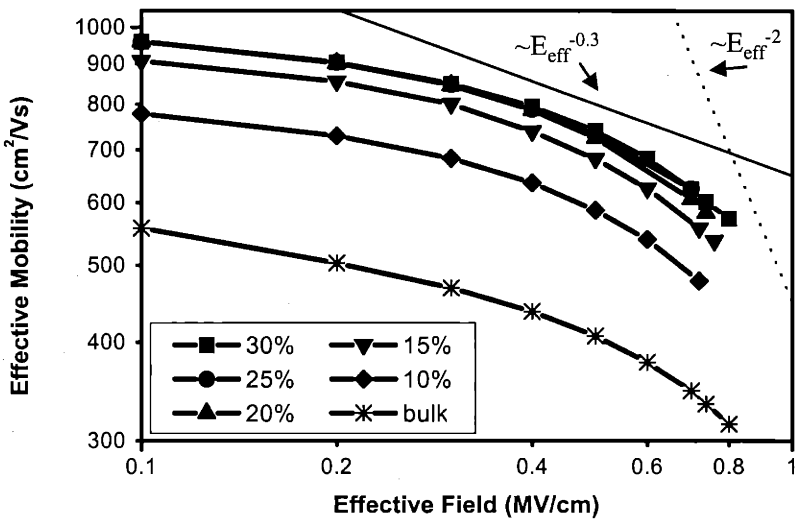

Figure 5.9 Strained Si effective electron mobility data presented on a logarithmic scale for comparison with the universal mobility curve.

Similar behavior has been observed in other experiments when both strained Si devices and bulk devices were fabricated with low temperature wet gate oxides[41] or CVD gate oxides[113]. With higher quality gate oxides, strained Si n-MOSFETs will attain even higher peak mobilities due to decreased Coulomb scattering, but their mobility enhancements over coprocessed bulk devices will remain constant.

5.5 Effect of Strain on Hole Mobility

Device structures identical to those in Section 5.4 were grown on n^- Si substrates to investigate the effect of strain on surface strained Si p-MOSFETs. As described above, analysis of the effective hole mobility as a function of effective field was performed, with

η=1/3 in the effective field calculation. The effective mobility data for the strained Si PMOS devices is shown in Figure 5.10.

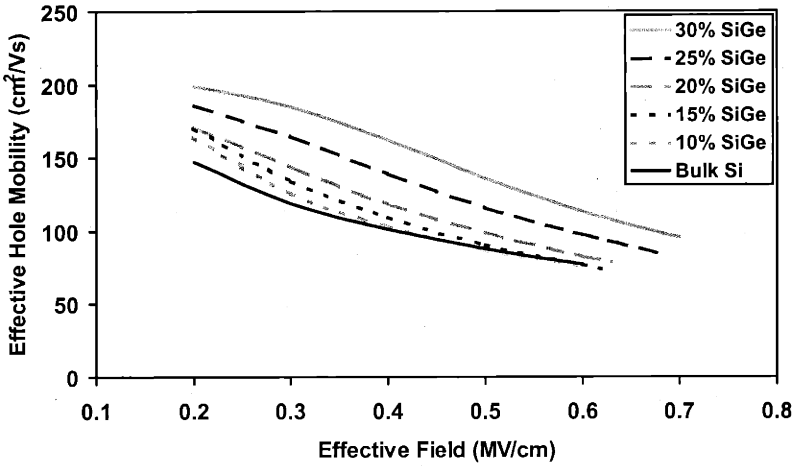

Figure 5.10 Surface channel strained Si effective hole mobility for devices fabricated on various virtual substrates. Hole mobility increases with increasing substrate Ge fraction but does not saturate at these strain levels.

The peak mobility for the 30% SiGe device, nearly 200 $cm^2/V \cdot s$, is the highest ever reported in the literature for a strained Si PMOS device. The effect of strain on effective mobility in the PMOS devices is very different from that of the NMOS devices of Section 5.4. As we can see from Figure 5.11, the mobility enhancement of these devices increases with strain and does not saturate.

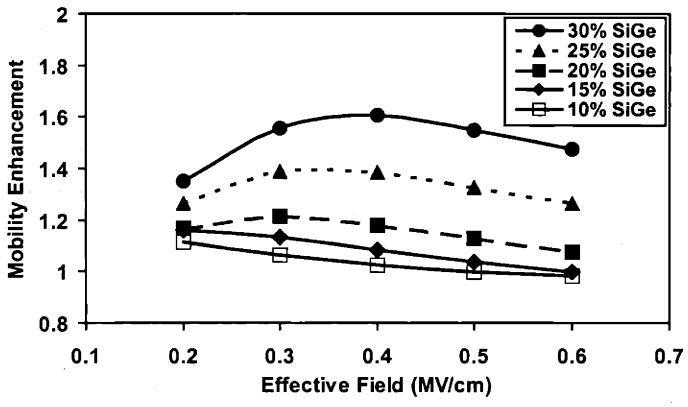

Figure 5.11 Strained Si hole mobility enhancement over coprocessed bulk Si devices. Hole mobility enhancement increases with strain and does not saturate at these strain levels.

Again, this behavior is in agreement with theoretical predictions for strained Si PMOS devices[114]. The rate of Si valence band energy splitting with tensile strain is significantly lower than in the conduction band. The subband splitting is only 77 meV for Si on 20% SiGe, and both the LH and HH subbands are still partially occupied at these strain levels. Thus, intervalley phonon scattering still occurs and limits the mobility of these devices. The mobility enhancement for strained Si PMOS devices is predicted to increase rapidly with strain for virtual substrate Ge contents up to 40%[114]. At these strain levels, the valence subband splitting is high enough so that only the LH band is occupied. With further increases in strain, the mobility enhancement should saturate, as intervalley scattering has been suppressed. Of course, the critical thickness of Si films on SiGe with Ge contents over 40% is less than 50 Å, making fabrication of devices very difficult at these strain levels. The saturation behavior is analogous to the behavior of strained Si n-MOSFETs on SiGe virtual substrates of Ge content 20% and higher, as shown in the previous section.

Also noticeable in Figure 5.11 is the different shape of the mobility enhancement curves compared to those of the strained Si NMOS devices. The mobility enhancement increases to a peak at effective fields of approximately 0.3 MV/cm, and then decreases with further increases in field. This behavior can be explained in the following way. Because of the type-II band offset of the strained Si/SiGe p-MOSFET, a parasitic hole channel forms in the SiGe virtual substrate. This parasitic channel in the low mobility SiGe leads to decreased mobility enhancement in the strained Si PMOS devices at low effective fields. As the effective field increases, the population of the high mobility surface channel increases relative to that of the parasitic channel, leading to an increase in mobility enhancement. We can see the effect of the sharp valence band discontinuity if we compare these results to those of Rim, *et al.*[115] and Welser[105]. The first group fabricated surface channel strained Si p-MOSFETs with a gradeback layer beneath the Si channel. The gradeback is a 300-400 Å tensile strained SiGe layer underneath the channel that is graded from 0% Ge to the Ge content of the virtual substrate. This gradeback smoothes out the valence band discontinuity and promotes hole population of the high mobility surface Si layer. Thus, at low effective fields, this structure will exhibit higher mobility. A comparison of the band diagrams of strained Si MOSFET structures with and without gradeback layers is shown in Figure 5.12.

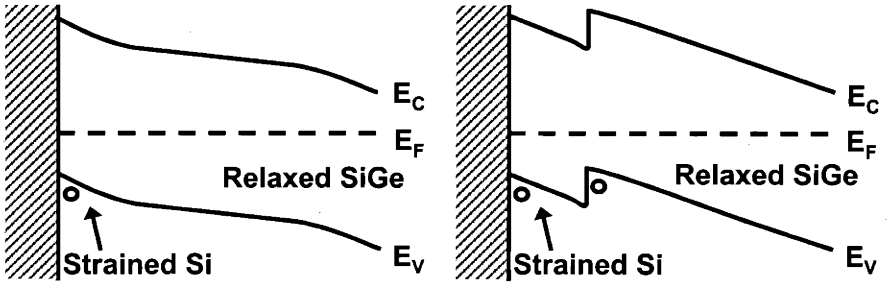

Figure 5.12 Comparison of the energy band diagrams of strained Si p-MOSFETs with *(left)* and without *(right)* a strained gradeback layer beneath the channel. The gradeback eliminates the parallel hole channel in the underlying SiGe but decreases the critical thickness of the surface Si channel.

The use of a gradeback layer can have disadvantages, however. Because the gradeback is also under tensile strain, it effectively reduces the critical thickness of the surface Si channel layer. Thus, misfit dislocation introduction and relaxation can occur at vastly reduced Si thicknesses. Moreover, at high vertical effective fields, the valence band bending is sufficient to force effectively all of the holes into the surface Si layer, even in the absence of a gradeback layer[116]. Welser fabricated a single strained Si PMOS device on a 30% SiGe substrate without a gradeback layer. The structure is nearly identical to those in this work.

A comparison of the mobility enhancement behavior of the p-MOSFETs of this work with those of Rim and Welser is shown in Figure 5.13. All of the curves correspond to mobility enhancements over coprocessed bulk Si devices. The bulk devices of Rim and Welser had lower substrate doping levels, and their mobility data only extended to 0.2-0.3 MV/cm.

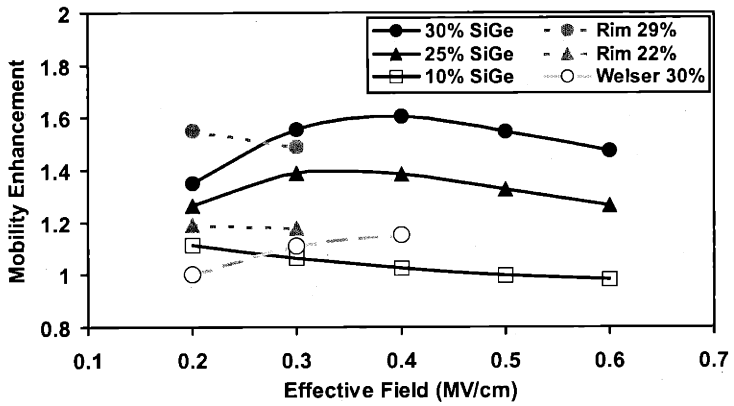

Figure 5.13 Comparison of strained Si p-MOSFET mobility enhancements to others in the literature. Devices by Rim, *et al.* featured a gradeback layer and have a different dependence on effective field. Elimination of the parallel hole channel enables higher hole mobilities at low fields. Enhancements are relative to coprocessed bulk Si devices.

With the gradeback layer, Rim's mobility enhancements decrease with increasing effective field, with a slope very similar to that of our data at 0.5-0.6 MV/cm. In contrast, Welser's data shows a dependence very similar to ours. The mobility enhancement increases with effective field as an increasing number of holes is forced into the strained Si surface layer. The effect of the gradeback is also shown in Figure 5.14, a comparison of the mobility enhancement of the strained Si p-MOSFETs over coprocessed strained Si devices on 10% SiGe.

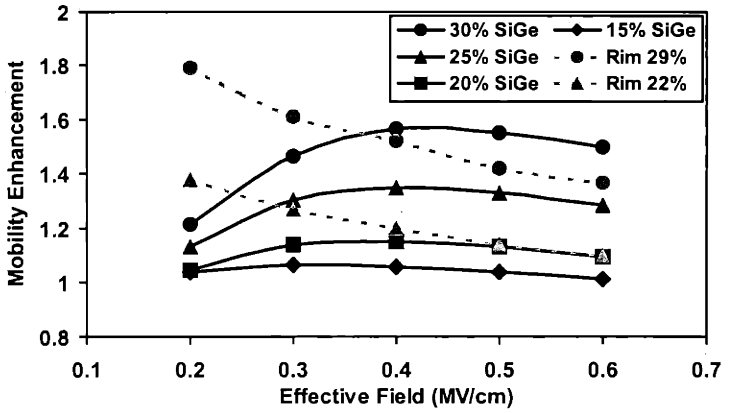

Figure 5.14 Comparison of strained Si p-MOSFET mobility enhancements to those of Rim, *et al.* Enhancements are relative to coprocessed devices on 10% SiGe virtual substrates. The slopes of the mobility enhancement data are identical at high effective fields. At these high fields, the holes are all populating the surface strained Si layer even without a gradeback layer.

The qualitative behavior of the different device structures is the same as in Figure 5.13. At low effective fields, Rim's devices display superior mobility enhancements. However, as effective field increases, Rim's mobility enhancements decrease to levels comparable to or worse than those of our devices on similar substrates. This may be due to slight relaxation in their device layers that was not detected by their characterization method. Thus, we find that although gradeback layers increase the mobility enhancements of strained Si p-MOSFETs at low effective fields, they are unnecessary at high effective fields. The negligible influence of the parasitic SiGe hole channel has been confirmed by Monte Carlo simulations of strained Si p-MOSFETs at high fields[114]. Additionally, gradeback layers decrease the critical thickness of strained Si device layers and may cause layer relaxation and loss of mobility enhancement.

Monte Carlo calculations of surface strained Si p-MOSFETs predict a mobility enhancement of 2.3 for a device on 30% SiGe[114]. They also predict the decrease in mobility enhancement with increasing effective field observed in our data. The strain-induced subband splitting is smaller in the valence band than in the conduction band. At high effective fields, the average kinetic energy of the strained Si holes increases. Therefore, at high enough fields, holes can scatter from the LH band to the HH band, leading to decreased mobility. Figure 5.15 shows the effective mobility curves for the p-MOSFETs plotted on a logarithmic scale.

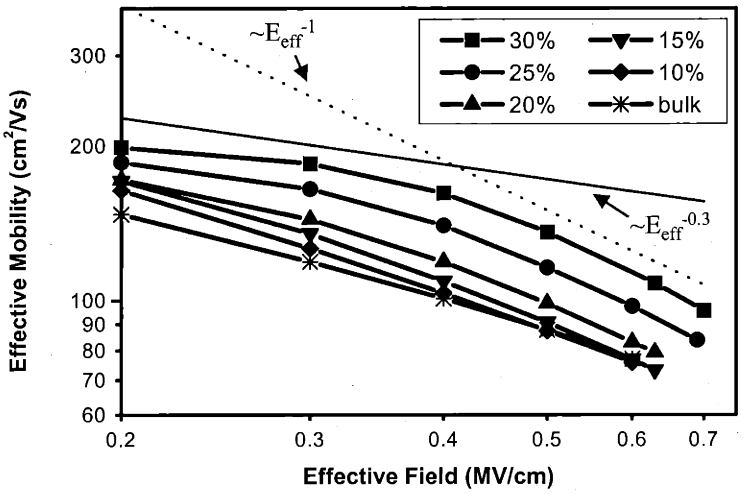

Figure 5.15 Strained Si effective hole mobility data presented on a logarithmic scale for comparison with the universal mobility curve.

As predicted by the universal mobility curve described earlier, we see a mobility dependence on electric field that is slightly larger than $E_{eff}^{-0.3}$ at moderate fields. By effective fields of 0.3 MV/cm or so, the effect of surface roughness is noticeable, and this dependence increases to E_{eff}^{-1}. Just as in the n-MOSFET case, the effect of the surface

roughness seems lessened in the bulk Si device, possibly due to low interface roughness with the LTO. Some small-scale roughness may have been introduced by the epitaxial growth of the SiGe-based device layers that is not present on the pristine bulk Si wafers. This decreased surface roughness dependence of the bulk device mobility decreases our mobility enhancements slightly at high fields.

5.6 Effect of Channel Implantation on Strained Si Mobility

Surface channel strained Si MOSFETs exhibit proven performance increases, but several process integration challenges remain before they can become a mainstream manufacturable technology. In this section, we study one such challenge, the effects of a channel implant on the mobility enhancement of strained Si devices. Although our Si/SiGe heterostructures are epitaxially grown and the channel regions could therefore be *in situ* doped, ion implantation is the preferred doping technique in terms of both reproducibility and uniformity. Additionally, *in situ* doping is known to degrade the electronic quality of subsequently deposited layers in many cases. Obviously, ion implantation is also required for any integration of n- and p-channel devices on the same wafer. In the experiment described in Sections 5.4 and 5.5, half of each wafer was subjected to a well implant before the beginning of the short-flow MOSFET process. The well implants were 13 keV boron for the NMOS wafers and 45 keV phosphorous for the PMOS. The implant dose was 1×10^{12} cm^{-2} in both cases. Unimplanted areas were masked by 1 μm of photoresist.

After processing, the implanted devices displayed the same mobility enhancement and high field mobility as the unimplanted devices. Figure 5.16 shows the effective mobility comparison between unimplanted and implanted n-MOSFETs.

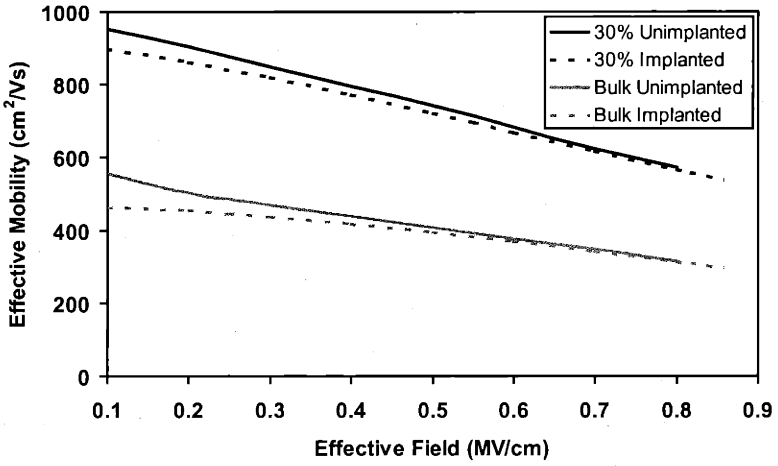

Figure 5.16 Effect of channel implantation on strained Si electron mobility. The electron mobilities for all devices were identical except at the lowest effective fields, where increased Coulomb scattering is observed.

The graph shows the data for the bulk devices as well as those on the 30% SiGe substrate. The other strained Si devices displayed identical behavior, and those data are omitted here for clarity. At low effective fields, the implanted devices exhibit slightly lower mobilities due to an increase in ionized impurity scattering, as expected. As effective field increases, the curves converge and eventually reach identical values. This behavior mirrors the universality of bulk Si device mobility, which is independent of doping at high fields[110]. The p-MOSFETs show exactly the same behavior, as can be seen in Figure 5.17. Data from other implant doses have also confirmed this universality of strained Si mobility[107]. Since surface channel strained Si devices are designed for high

field applications such as high-speed digital CMOS, increased Coulomb scattering should have no effect of their performance.

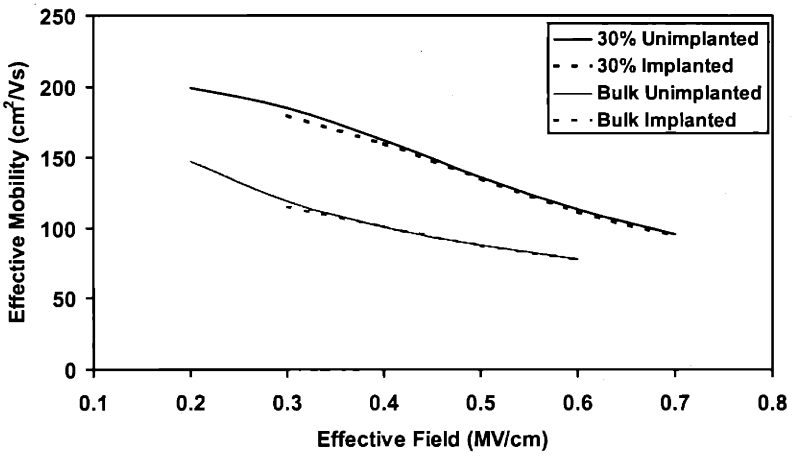

Figure 5.17 Effect of channel implantation on strained Si hole mobility. The hole mobilities for all devices were identical except at the lowest effective fields, where increased Coulomb scattering is observed.

5.7 Effect of Virtual Substrate Planarization

Another potential showstopper for the manufacturability of strained Si MOSFETs is the surface roughness of the SiGe virtual substrate. The depth of this characteristic crosshatch pattern, caused by the strain fields of the misfit dislocations in the graded layer, depends on the film growth parameters[19]. Rms surface roughnesses greater than 10 nm are typical, and are large enough to prohibit fine-line lithography. The length scale of the crosshatch is much larger than the carrier mean free paths, which are on the order of 10 nm, and hence should have no negative impact on carrier mobility in these devices[117,118]. Therefore, while we expect no increase in carrier mobility with the elimination of the surface crosshatch, the suitability of the substrates for manufacturing

will increase. To achieve manufacturability of strained Si devices, a reliable and repeatable method of eliminating the surface roughness must be established. CMP is an established back-end planarization method in microelectronics fabrication, and is a necessary element for state-of-the-art chips with several metallization layers[66]. Here, we use CMP to planarize SiGe at the "front-end," prior to device fabrication. Because our surface strained Si layers are much thinner than the characteristic surface roughness of SiGe virtual substrates, the device structure must be regrown on the virtual substrate after planarization. This SiGe CMP and regrowth procedure has been successfully used in graded SiGe layers to eliminate dislocation pile-ups and decrease threading dislocation density in high Ge content layers[119], as described in Section 3.5.

5.7.1 Effect of Thick SiGe Regrowth Layer

In this experiment, SiGe virtual substrates grown for the experiment in Sections 5.4 and 5.5 were planarized via CMP. Approximately 0.5 μm of the uniform SiGe cap layer was removed during this process. The rms surface roughness of the planarized wafers was approximately 1 Å in a 15 μm × 15 μm AFM scan. The effect of the CMP process on SiGe virtual substrates was previously shown in Figure 4.5. After thorough post-CMP cleaning, regrowth was performed on each of the device wafers. 0.5 μm of SiGe was deposited on each wafer at 900°C, followed by 0.5 μm SiGe and 100 Å strained Si layers at 650°C. Thus, the device layers are identical to those in Sections 5.4 and 5.5, but the surface roughness of the wafers was greatly reduced. Some surface crosshatching did begin to reappear on the wafers during regrowth due to the influence of the strain fields

of the underlying misfit array of the graded layer; however, the overall rms roughness remained much lower than that of the as-grown SiGe buffer layer. The CMP and regrowth process does result in some contamination at the regrowth interface, namely increased concentrations of carbon and oxygen visible in SIMS scans of planarized samples. However, careful post-CMP cleaning allows one to regrow SiGe layers with no increase in threading dislocation density. The experiment described in Sections 5.4 and 5.5 was repeated with planarized wafers, and identical carrier mobility results were achieved. Figure 5.18 and Figure 5.19 show comparisons of the mobility between devices on the original and on the planarized substrates.

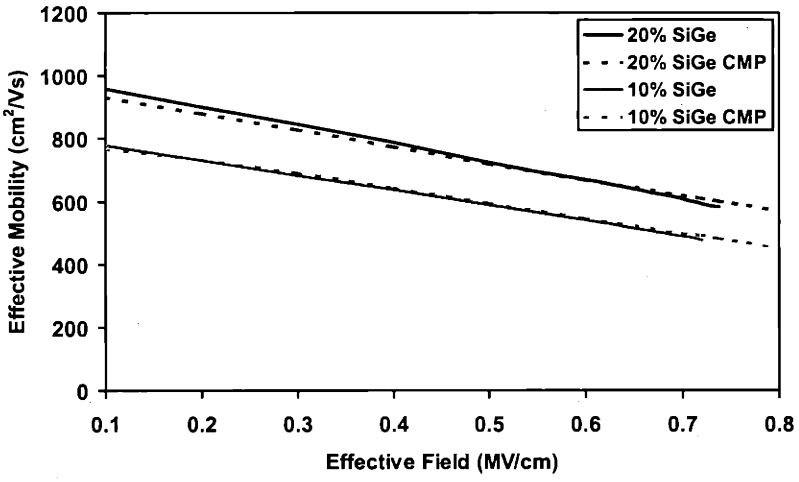

Figure 5.18 Comparison of strained Si electron mobility for devices on substrates with and without planarization. Virtually identical results were obtained for all devices.

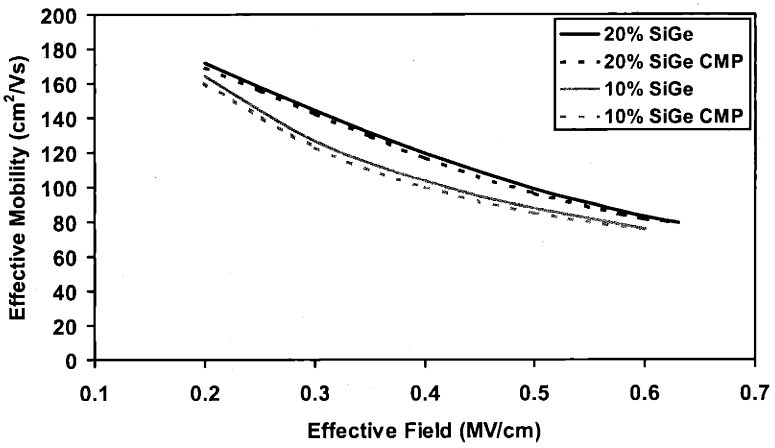

Figure 5.19 Comparison of strained Si hole mobility for devices on substrates with and without planarization. Virtually identical results were obtained for all devices.

Virtually identical curves were obtained for both cases on all of the substrates in the experiment, but only the results on the 10% SiGe and 20% SiGe substrates are shown for clarity. Thus, for the first time, carrier mobility enhancement of surface channel strained Si n- and p-MOSFETs has been demonstrated with wafers smooth enough for state-of-the-art lithographic techniques. Note that the strained Si channels in these devices were far away (approximately 1 μm) from the regrowth interface, so no deleterious effects from contaminants at this interface would be expected[120].

5.7.2 Effect of Regrowth Thickness

In order to determine the impact of proximity to the CMP and regrowth interface on strained Si MOSFET mobility, another experiment was performed. Two sets of 25% SiGe virtual substrates were grown at 900°C, 25 mT, and graded at 10% Ge/μm. The growths finished with 2 μm uniform 25% SiGe cap layers. One set was *in situ* doped

1×10^{16} cm^{-3} p-type for the fabrication of NMOS devices. The other was doped n-type at the same concentration for PMOS. These wafers were then planarized via CMP. 0.5 μm of the uniform cap layer was removed in the CMP process. After the thorough post-CMP cleaning procedure described in Section 3.4.2, a series of regrowth experiments was performed with the planarized wafers. Various thicknesses of 25% SiGe were grown on the wafers, followed by 85 Å strained Si channel layers. The thicknesses of the regrown 25% SiGe were 500, 100, 50, and 10 nm. Another wafer had no regrown SiGe layer—the strained Si channel was regrown directly on the CMP interface.

The surface roughness of the regrown device wafers was measured with AFM. Figure 5.20 shows the variation of the rms surface roughness of the wafers with the thickness of the SiGe regrowth layer.

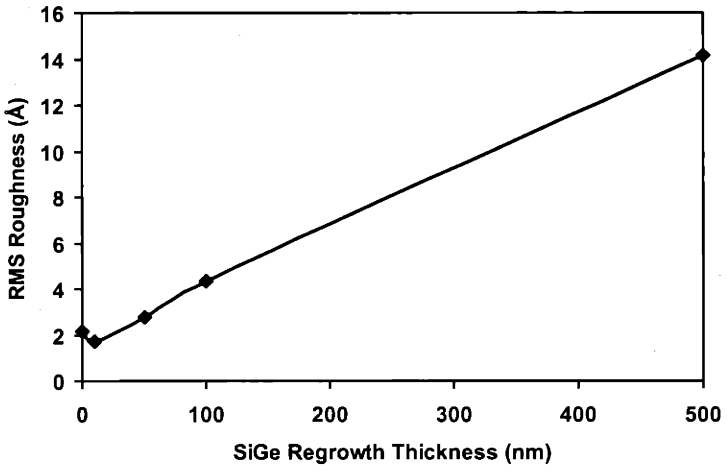

Figure 5.20 The effect of the SiGe regrowth thickness on the rms surface roughness of the strained Si device substrate. The surface roughness increases with regrowth thickness due to the effect of the strain fields of underlying misfit dislocations, as well as the dependence of CVD growth rate on crystallographic orientation.

Generally, the surface roughness increases with increasing regrowth thickness. This increase in roughness is due to the influence of the strain fields of the underlying misfit dislocations of the SiGe virtual substrate. These strain fields affect the local growth rate during the regrowth, and the characteristic crosshatch pattern begins to reemerge. Compounding this effect is the CVD growth dependence on crystalline orientation, discussed earlier in the context of dislocation pileup formation. The planarized wafer surface is inherently unstable once the crosshatch pattern begins to appear, leading to a monotonic increase in surface roughness with regrowth thickness. Regrowths performed with molecular beam epitaxy (MBE), in which growth rate is orientation-independent, would display a different behavior. Just as with CVD growth, the surface would initially roughen due to the influence of the underlying misfit dislocations. The misfit strain fields decrease as 1/r, where r is the distance from the dislocation. Hence, during MBE, eventually the surface roughness would stabilize, not worsening with thicker growth, as the effects of the strain fields diminished.

A secondary ion mass spectrometry (SIMS) analysis was performed on the wafers in order to see the level of contamination at the planarized regrowth interfaces. The SIMS was performed by Evans East, utilizing Cs^+ ion bombardment at an energy of 3 keV. All of the samples exhibited similar sharp spikes in carbon, oxygen, and nitrogen at the regrowth interface. The data from the 100 nm SiGe regrowth sample is shown in Figure 5.21.

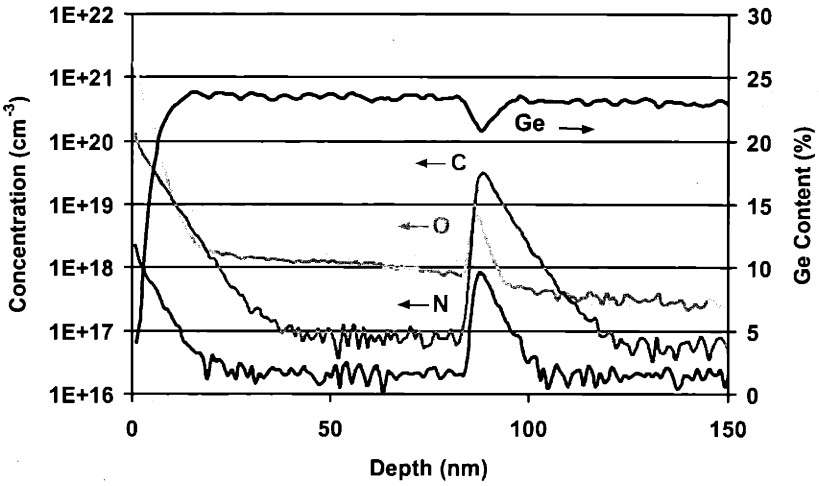

Figure 5.21 SIMS data from a planarized device wafer. The SiGe regrowth thickness was 100 nm. Contamination spikes of carbon, oxygen, and nitrogen can be seen at the regrowth interface.

The carbon spike peaks at approximately 3×10^{19} cm^{-2}, and the width of the peak is 30 nm. On both sides of the peak, the carbon content decreases to the mid-10^{16} cm^{-2} detection limit. The oxygen and nitrogen spikes peak at 6×10^{18} cm^{-2} and 9×10^{17} cm^{-2}, respectively, and both spikes are 10-15 nm wide. As with carbon, on either side of the spike, the level of these elements also decreases to the detection limit of the instrument. A slight dip in the Ge content of the layer is also seen at the regrowth interface. Ge depletion at a SiGe growth interruption has been observed previously[121], and may be due to reduced Ge sticking coefficients due to hydrogen passivation. Moreover, thermal desorption of oxide at high temperatures preferentially depletes Ge from the SiGe surface. In this case, it could also be due to the post-CMP and pre-epitaxial cleaning procedures, which will etch Ge preferentially to Si. The Ge depletion effect has been observed in other SiGe regrowth experiments[122].

Short-flow MOSFETs were fabricated on all of the wafers, and bulk Si wafers were coprocessed for comparison. The n-MOSFET results are shown in Figure 5.22. The effective mobility is graphed for each regrowth thickness variation.

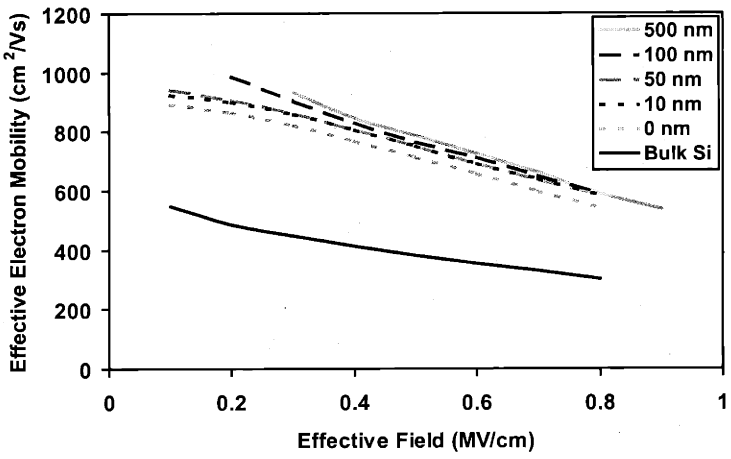

Figure 5.22 The effect of regrowth thickness after planarization on electron mobility in strained Si MOSFETs. Decreasing regrowth thickness has little effect on mobility. The mobility of the channel grown directly on the planarized interface is decreased by only 7-12%. This device still exhibits mobility enhancements greater than 1.8 over the bulk Si device.

The distance between the channel and the regrowth interface has little impact on the device mobility. The electron mobility of the devices with no SiGe regrowth layer is decreased 7-12% compared to those with the 500 nm regrowth layer. Despite this slight decrease, the devices with no SiGe regrowth layer still exhibit high-field mobility enhancements of greater than 1.8 over the coprocessed bulk Si devices. The low-field mobility is also decreased slightly for the samples with a 50 nm regrowth or less. This result is similar to low-temperature mobility measurements on buried strained Si heterostructures with a regrowth interface[122]. Electron traps at the regrowth interface

reduced the electron mobility significantly at regrowth thicknesses of 50 nm or less. This would explain why such traps only affect these devices at low fields—at higher fields, the room temperature mobility is limited by phonon scattering. Figure 5.23 shows the mobility data for the PMOS devices.

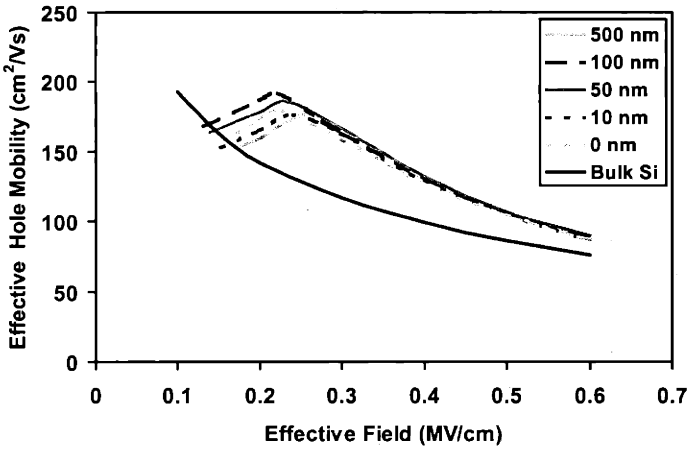

Figure 5.23 The effect of post-planarization regrowth thickness on hole mobility in strained Si MOSFETs. Decreasing regrowth thickness has virtually no effect on mobility.

The hole mobilities of all of the devices are virtually indistinguishable, indicating no evidence of mobility degradation with decreasing regrowth thickness. The decrease in mobility at fields less than 0.2 MV/cm is due to parallel conduction through the low mobility SiGe underlayer. As the electric field increases, the holes are increasingly forced into the surface Si layer. This effect can be alleviated via the use of thicker Si channels or strained gradeback layers that smooth the abrupt valence band discontinuity between the relaxed SiGe and strained Si. Similar behavior has been observed in other strained Si p-MOSFETs fabricated without gradeback layers, including those of Section 5.5.

This investigation reveals that the spike of contamination at the regrowth interface has virtually no effect on the room temperature carrier mobility of strained Si MOSFETs. This result will have particular impact on the ability to fabricate strained Si devices on SiGeOI substrates. Just as with silicon-on-insulator (SOI) devices, the buried oxide layer in these structures is on the order of 200 nm or less below the surface. A SiGeOI wafer fabricated by the bond and etchback process would have a strained Si layer regrown on top prior to device fabrication[102]. Thus, if thick SiGe regrowth layers were required to attain high carrier mobilities in the strained Si layers, many benefits of the buried oxide layer would be lost. This experiment shows that for room temperature device operation, strained Si device layers could be grown with very thin SiGe underlayers on SiGeOI wafers with little or no deleterious effect on the carrier mobility.

5.7.3 Fabrication of Strained Si n-MOSFET on SiGeOI

As a proof of concept, device layer regrowth was performed on a 25% Ge content SiGeOI wafer prepared by the bonding and etchback technique[123]. Utilizing the above procedure, 100 nm of 25% SiGe and an 85 Å strained Si channel were regrown on the wafer. A cross-sectional schematic of the final SiGeOI device wafer is shown in Figure 5.24.

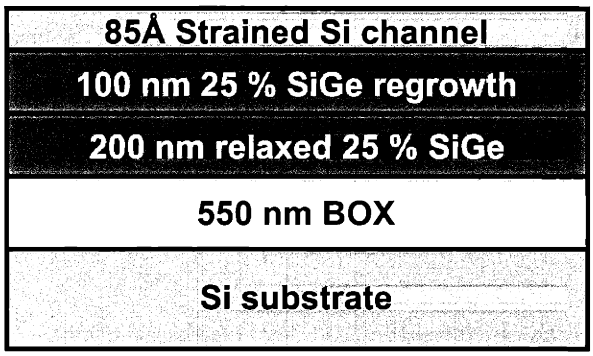

Figure 5.24 **Layer structure of the strained Si n-MOSFET fabricated on a SiGeOI substrate with a 550 nm buried oxide layer. Growth sequence was identical to the 100 nm SiGe regrowth of the previous section.**

Strained Si n-MOSFETs were fabricated on the wafer via the short-flow process. Figure 5.25 shows the effective electron mobility data from devices on the SiGeOI wafer compared with the 100 nm regrowth devices from the planarization experiment and coprocessed bulk devices.

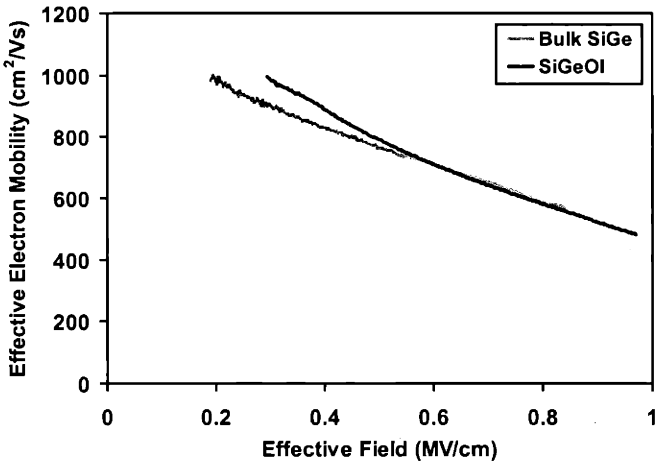

Figure 5.25 **Electron mobility of the strained Si MOSFET on SiGeOI compared to that of the planarized device of the previous section and to a coprocessed bulk Si device. Nearly identical results are obtained with the SiGeOI device.**

The mobility of the devices on the SiGeOI wafer is nearly identical to that of the bulk strained Si devices. Strained Si MOSFETs have been previously reported on 10% Ge content SiGeOI substrates produced by the separation-by-implanted-oxygen (SIMOX) technique[124]. However, the thermal instability of GeO makes the fabrication of SiGeOI substrates via SIMOX impossible for Ge contents above 30%[125]. Indeed, SIMOX SiGeOI substrates have been successfully demonstrated only for Ge contents up to 18%[126,127]. This marks the first time that strained Si n-MOSFETs have been fabricated on SiGeOI wafers with Ge contents greater than 10%. The feasibility of the fabrication of a wide variety of SiGeOI-based devices has also been proven, since the bond and etchback technique can be used to create SiGeOI wafers with arbitrary Ge fractions.

5.8 Effect of Channel Thickness

The choice of channel thickness in strained Si MOSFET design is an important one. In the thinnest regime, carrier confinement will decrease with decreasing thickness due to quantum effects in the well. This leads to carrier conduction through the low-mobility relaxed SiGe underlayer, degrading the overall device mobility. Layers thicker than the equilibrium critical thickness also present potential problems. Even if the Si is grown metastable at low temperatures, high-temperature processing can lead to misfit dislocation introduction. These misfit dislocations are effective carrier scattering sites; thus high densities of misfits will degrade device mobilities. Moreover, if substantial strain is lost from the Si layer though misfit dislocation introduction, carrier mobilities will also decrease due to strain loss.

In this experiment, a series of surface channel strained Si n-MOSFETs was fabricated with different Si channel thicknesses. 20% SiGe virtual substrates were used for all devices. As in the above experiments, the effective electron mobility was evaluated as a function of effective field, and the mobility enhancements over a coprocessed bulk Si device were calculated. Figure 5.26 shows the electron mobility enhancement of the devices as a function of the surface Si channel thickness. The tabulated thicknesses for the devices are the thicknesses after processing, since some strained Si is consumed in the initial substrate clean. All of the mobility enhancements are calculated relative to the coprocessed bulk Si devices at 0.4 MV/cm.

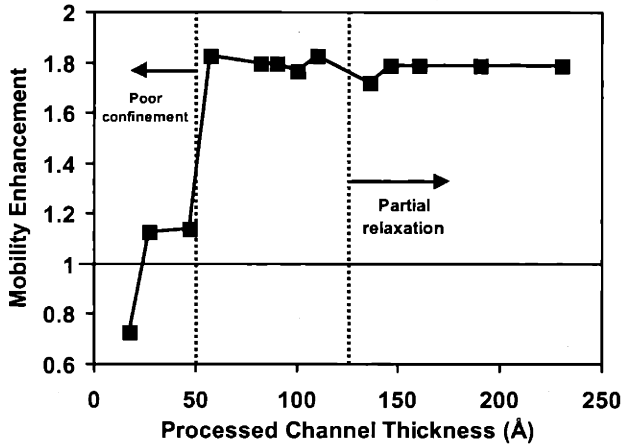

Figure 5.26 Electron mobility enhancement of strained Si n-MOSFETs as a function of channel thickness. Poor confinement degrades the mobility of the thinnest channels. The slightly relaxed thickest channels exhibit no mobility degradation.

Large degradations in mobility enhancement are obvious for the thinnest channel devices in the study. The first sample, with a channel thickness of less than 20 Å, actually has a worse mobility than the coprocessed bulk device. This can be attributed to

poor confinement in the Si channel, as many electrons are no doubt conducting through the low-mobility relaxed SiGe. An increased interface state density due to the close proximity of the oxide to the SiGe will also limit the performance of this device. The electron mobility enhancement increases slightly for the channels in the 30-50 Å thickness range to approximately 1.14, but poor confinement limits them to values much reduced compared to the thicker channel devices. In fact, once the channel thickness increases beyond 50 Å, the mobility enhancement is vastly increased. All of the samples with channel thicknesses of 57-120 Å exhibit the expected mobility enhancements of 1.7-1.8, in line with our previous NMOS devices on 20% SiGe substrates. These samples are all thick enough not to be significantly impacted by confinement issues. All of the layers thinner than 120 Å are fully strained, as the absence of misfit dislocations was confirmed by selective etching of the as-grown wafers.

The channel thicknesses 135 Å and greater were partially relaxed, as confirmed by selective etching. The misfit dislocation densities of these layers is still very low, as the layers maintained a high level of metastability at the 650°C growth temperature. The thickest 230 Å channel had an as-grown misfit dislocation density of approximately 300 cm^{-1}. Misfit densities this low would be virtually undetectable by most characterization methods, and obviously have little or no impact on the electron mobility in these devices. Significant mobility enhancements would most likely still be exhibited by samples with even higher misfit dislocation densities, due to two competing effects. As shown above, thin partially relaxed channels have extremely low misfit dislocation densities. Thicker channels lead to more misfit dislocation introduction, but the carrier conduction is also

occurring farther away from these misfit dislocations, making them less effective scattering sites[128]. This explains the observation that strained Si channels much thicker than the critical thickness have been used to fabricate devices which exhibit significant mobility enhancement. Of course, substantial tensile strain will be lost in the thickest layers, decreasing the mobility back toward that of bulk Si.

Strained Si layers for n-MOSFETs can be grown as thin as 50 Å and still exhibit large mobility enhancements. These channel layers can be extremely thin because the longitudinal (out-of-plane) electron effective mass is very large, $0.98m_o$. Recall that it is the $0.19m_o$ transverse electron mass that leads to mobility enhancement in strained Si n-MOSFETs. The high longitudinal effective mass limits the spatial extent of the electron wave function, effectively squeezing it to less than 50 Å. Thus, as long as the channel thickness exceeds this value, the electrons will be confined in the channel and no thickness effect will be observed. Self-consistent solutions of Poisson's and Schrödinger's equations have confirmed that the high longitudinal electron mass confines the wave function ground state to 50 Å[129], in agreement with our experimental results.

The situation is very different for strained Si p-MOSFETs. In the valence band, the longitudinal hole effective mass is actually lighter than the in-plane transverse mass[28]. The hole wave function will be quite large in this case, unlike that of the electrons. Thus as the channel thickness is decreased, mobility degradation should occur at a greater thickness. Although this experiment was not repeated for p-MOSFETs, comparison of some of the previous data can lend some insight into this phenomenon. Figure 5.27 shows the effective hole mobility of two samples from previous experiments. The 100 Å

channel sample is from the original experiment on the effect of strain on hole mobility in Section 5.5. The 85 Å channel sample was fabricated in the planarization experiment of Section 5.7.

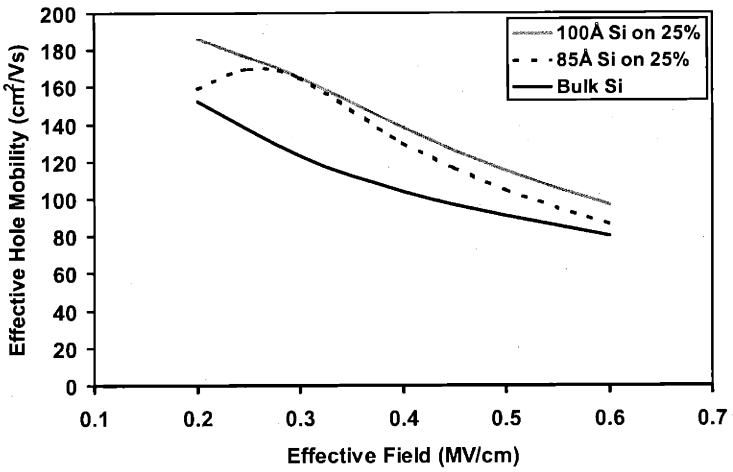

Figure 5.27 Comparison of the effective hole mobilities of two strained Si p-MOSFETs with different channel thicknesses. The device with the thicker channel exhibits higher hole mobility because of the light transverse hole effective mass.

The thicker channel exhibits higher hole mobility, particularly at higher effective fields. Therefore, thick channels may be required to harness the full potential of strained Si p-MOSFETs. Of course, high strain levels in these devices also result in higher mobilities—the hole mobility enhancement does not saturate at the strain levels studied in these experiments. Because high levels of strain limit the equilibrium critical thickness of strained Si, a tradeoff must be made between strain level and channel thickness. Proper choice of the strained Si p-MOSFET channel thickness will be of paramount importance in future device designs.

5.9 Thermal Budget Evaluation

Perhaps the most daunting perceived challenge facing the transfer of strained Si devices from the research laboratory to a manufacturing environment is their limited thermal budget. Fortunately, reduction in thermal budget is already the trend in the microelectronics industry, due to the need to preserve sharp dopant profiles and precise junction depths[130]. Still, some fabrication modules are performed at high temperatures, particularly oxidation for device isolation and gate formation. However, with the advent of shallow trench isolation using deposited oxides, and with deposited, alternative material gate dielectrics close to becoming a reality, thermal budgets in silicon microelectronics fabrication will decrease even more in the near future.

Another fabrication module that takes place at high temperature is the dopant activation anneal. These elevated temperatures can wreak havoc with strained Si/SiGe heterostructures, leading to strain relaxation in metastable films and dopant and Ge diffusion into strained Si channels. As mentioned earlier, some previous studies of strained Si MOSFETs have utilized thick, metastable (or even partially relaxed) Si channels. In an effort to avoid further strain relaxation, these studies have had a limited thermal budget, which can lead to high gate oxide interface state densities and high series resistance. Our short-flow MOSFET also has a reduced thermal budget, as we utilize a LTO gate dielectric rather than thermal oxide. This is due to the fact that we require a very thick oxide layer for the "lift-off" metal self-patterning deposition, thicker than is possible with thermal oxidation of our thin strained Si layers. Thus, we are in a position to determine elevated temperature effects in our structure via one step—the RTA used to

activate our source/drain implant. RTA is the most widely used dopant activation technique in microelectronics fabrication[131]. In order to minimize dopant diffusion and maximize implantation-induced defect removal, high temperature (>1000°C) anneals for very short times are desirable. These short RTAs make possible the shallow, low resistance junctions necessary for state-of-the-art CMOS fabrication.

In this experiment, we fabricated short-flow MOSFETs on 30% Ge virtual substrates. The as-grown strained Si channel thickness was 100 Å, but some of the Si is consumed in the clean prior to the LTO deposition. After processing, XTEM measurements revealed that the channel thickness had been reduced to approximately 75 Å, which is close to the equilibrium critical thickness for this structure. Thus, upon annealing to high temperatures, we expect no misfit dislocation introduction in our device structure. Instead, the major device performance limiter will be Ge diffusion from the virtual substrate into the Si channel. Severe Ge diffusion will smear out the strained Si channel, effectively reducing the channel thickness. Loss of carrier confinement can occur if the channel thickness is reduced enough, leading to poor mobility in the device. As Ge atoms diffuse into the strained Si channel, alloy scattering may also cause degradation of device performance. Ge segregation into as-grown Si on SiGe layers can also play a large role if Ge atoms reach the Si/SiO_2 interface of a MOS device. This effect has degraded the effective mobilities of pseudomorphic SiGe p-MOSFETs with thin Si cap layers[33].

A series of post-implant anneals was performed on our device wafers. The RTA temperature was monitored by a thermocouple mounted on a Si chip next to the wafer, as

well as by a pyrometer underneath the wafer. The pyrometer had been calibrated over a temperature range of 500-1100°C by use of a full wafer thermocouple[132]. The temperature profile of each RTA was controlled by the thermocouple, and the pyrometer reading was monitored in parallel. The anneals were performed at 950°C for 1 second and 1000°C for 1-30 seconds. The nominal temperature ramp rate was 100°C/sec for all anneals. For the 1 second anneals, the pyrometer registered a temperature overshoot of over 100°C. In the longer 1000°C anneals, the pyrometer temperature initially overshot by approximately 100°, and then recovered to roughly 50° above the thermocouple reading for the length of the anneal. Thus, there is some uncertainty to the actual temperature profile experienced by each wafer during the anneal sequence. For comparison, bulk Si device wafers were annealed at 875°C for 1 second (1000°C on the pyrometer) and at 1000°C for 10-30 seconds. For the subsequent discussion, the anneals will be referred to by the temperatures registered by the thermocouple, keeping in mind that the actual wafer temperature might be significantly higher.

If any of the RTA sequences on the strained Si devices resulted in carrier mobility degradation, Ge diffusion from the virtual substrate would be the predicted reason. Therefore, no mobility degradation of the bulk Si devices was anticipated. However, for the anneals at 1000°C for 10 seconds and longer, the bulk devices do exhibit mobility degradation in both NMOS and PMOS devices. Figure 5.28 shows the bulk NMOS mobility data from the various RTA splits.

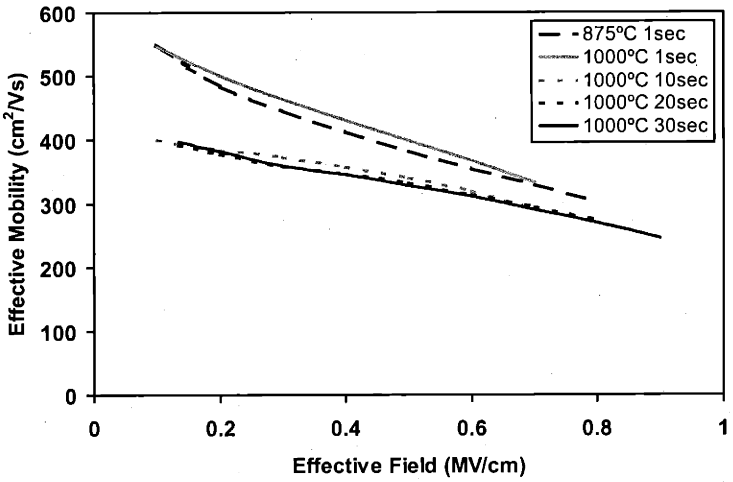

Figure 5.28 Electron mobility data for bulk Si devices subjected to different RTA cycles. Anneals at 1000°C for 10 seconds or more cause mobility degradation.

Both the 875°C and 1000°C spike annealed samples display mobilities representative of the bulk samples in the other experiments. However, some mechanism leads to electron mobility degradation after 10 seconds at 1000°C, particularly at low effective fields. This degradation can most likely be attributed to densification of the LTO gate dielectric during the RTA. Cross-sectional SEM photos of the finished devices showed no gross shape change of the gate structure, but densification can lead to outgassing and microstructural changes at the interface between the LTO and the Si. The quality of this interface directly impacts the carrier mobility of Si MOSFETs. The bulk PMOS devices showed similar behavior, as shown in Figure 5.29.

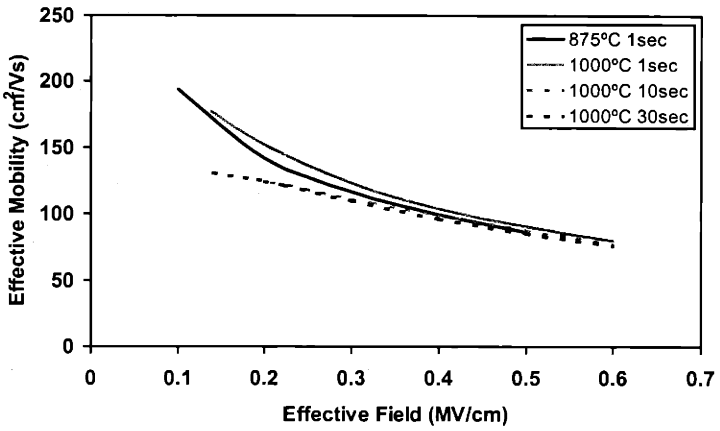

Figure 5.29 Hole mobility data for bulk Si devices subjected to different RTA cycles. Anneals at 1000°C for 10 seconds or more cause mobility degradation.

For anneal times 10 seconds and beyond, the hole mobility is degraded slightly below that of the other samples. The effect is not as severe as in the NMOS case, however. When the mobility enhancements of the strained Si devices were calculated, this effect was factored out by comparing each strained Si mobility to the mobility of the bulk device annealed for the same amount of time. Thus, any remaining mobility degradation should be attributable to Ge diffusion from the underlying virtual substrate or from misfit dislocation introduction.

The mobility enhancements of the strained Si NMOS devices were calculated and are presented in Figure 5.30. The data was calculated at an effective field of 0.6 MV/cm.

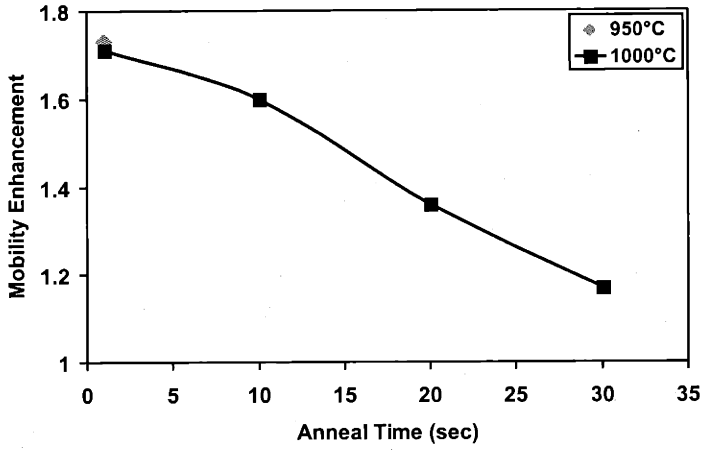

Figure 5.30 Effect of RTA cycle on electron mobility enhancement of strained Si MOSFETs. The mobility enhancement decreases with increasing anneal time.

The device with the 950°C spike RTA exhibited a mobility enhancement of 1.73. However, the devices annealed at 1000°C exhibited mobility degradation with increasing anneal time. The enhancement of 1.73 after 1 second decreases to below 1.2 after a 30 second anneal. The RTAs had similar effects on the PMOS devices, as shown Figure 5.31.

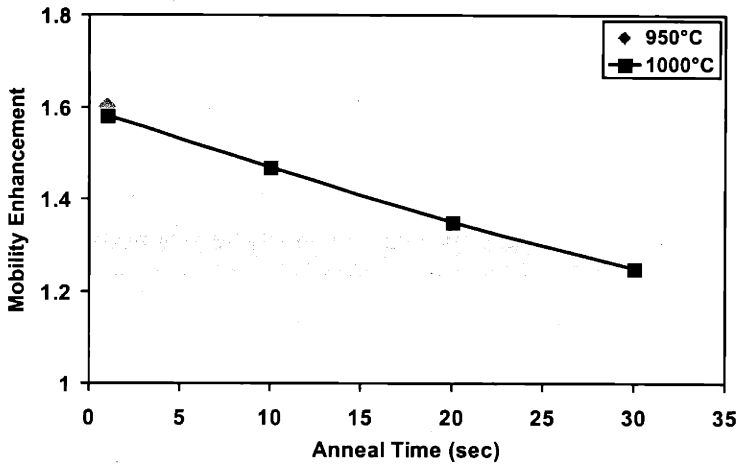

Figure 5.31 Effect of RTA cycle on hole mobility enhancement of strained Si MOSFETs. The mobility enhancement decreases with increasing anneal time. The effect of increasing anneal time is not as severe as with the n-MOSFETs.

The 950°C spike annealed sample had a mobility enhancement of 1.6, and the 1000°C series showed a mobility decrease from 1.58 to 1.25. Investigations were carried out to determine the origin of the mobility degradation of the strained Si devices with increasing anneal time.

If misfit dislocations were introduced by the exposure to high temperatures, it is unlikely enough dislocations would form to relax an appreciable amount of the strain in the surface Si layer. Thus, loss of strain at high temperatures, even if it did occur, would not be enough to explain the mobility degradation of these devices. However, misfit dislocations are effective carrier scattering sites[133], and could still lead to mobility degradation if present. To determine whether misfit dislocations had been introduced, selective etching experiments were performed on the processed wafers. The metal layer was stripped with a H_2SO_4/H_2O_2 solution, and the polysilicon gate layer was stripped

using a mixture of KOH, potassium dichromate (KCr_2O_4), and water. The LTO was then etched in HF, leaving the strained Si/SiGe device structure intact. Selective etching with the dilute Schimmel etch revealed no misfit dislocations in any of the surface strained Si layers. Thus, because the device layers used for these strained Si layers were thinner than the equilibrium critical thickness, we have avoided misfit dislocation introduction even at high temperatures. However, the choice of a thin surface channel layer can also have drawbacks, as evidenced by the samples annealed at 1000°C.

Since misfit dislocation introduction has been eliminated as a mobility degradation mechanism, we now consider the effects of Ge diffusion on the mobility of these devices. In one published report, Ge diffusion destroyed the 77 K Hall mobility of buried strained Si heterostructures after anneals of 1000°C for 3 minutes[134]. Utilizing the diffusion parameters found in this report, simulations show that, while some interdiffusion will occur in our structures after 30 seconds at 1000°C, it is not enough to destroy our strained Si channel. Even if the higher pyrometer temperature is utilized in the simulations, complete intermixing of the channel will not occur in 30 seconds—at least 50 Å of the Si channel will remain at the surface. In order to investigate the motion of Ge into the strained Si channel, a high-resolution XTEM study of the processed device layers was undertaken. Figure 5.32 shows a XTEM micrograph from the 950°C spike annealed sample.

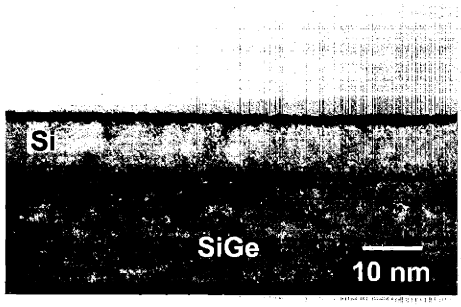

Figure 5.32 High-resolution cross-sectional TEM micrograph of the strained Si channel of the device annealed at 950°C for 1 second. The 75 Å Si channel is clearly evident.

The 75 Å surface Si channel is clearly visible beneath the LTO gate dielectric. This channel begins to narrow as the annealing times increase, as shown in Figure 5.33. After 10 seconds at 1000°C, the channel in XTEM appears to have narrowed to approximately 50 Å, a clear indication of Ge diffusion from the virtual substrate. In the XTEM pictures of the 20 and 30 second anneals at 1000°C, no sharply defined channel layer is evident, so a substantial amount of intermixing has occurred. The exact Ge profiles in these samples are impossible to obtain via TEM.

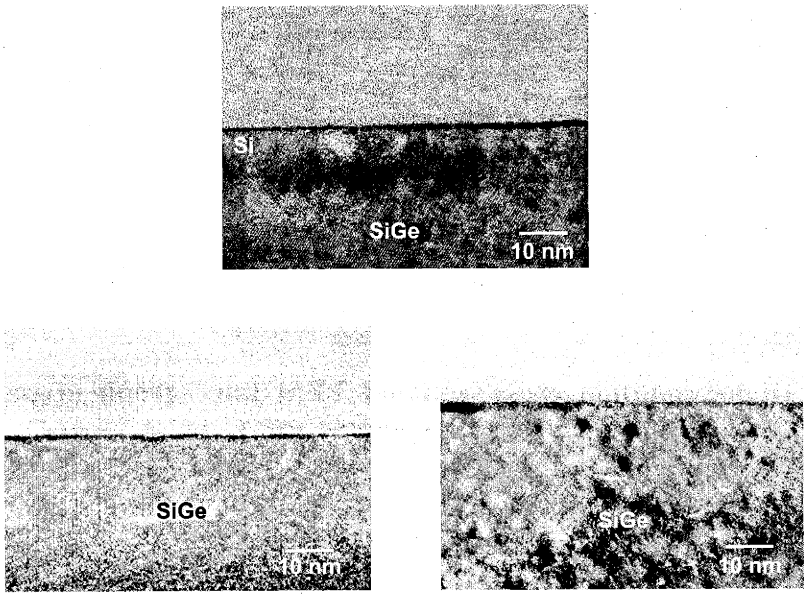

Figure 5.33 High-resolution cross-sectional TEM micrographs of the strained Si channels of devices annealed at 1000C. A 50 Å channel can still be seen after the 10 second anneal *(top)*, but interdiffusion has obscured it after 20 *(bottom left)* and 30 second anneals *(bottom right)*.

A method such as ultra-low energy SIMS would be required to quantify the amount of Ge near the surface. It is clear, however, that either some factor is enhancing the Ge diffusion into the Si channel or that the RTA temperature is higher than the measured value.

The effective carrier mobility of a MOS inversion layer is very sensitive to Ge diffusion since Ge atoms can create interface states at the Si/SiO_2 interface. This increased interface state density can drastically degrade MOSFET mobility and shift the threshold voltage[110]. During our anneals at 1000°C, we expect more Ge atoms to reach the Si/SiO_2 interface with increasing anneal time. Since Ge segregation has been shown to occur in Si layers grown on SiGe via UHVCVD above temperatures of 515°C[135], some Ge will already be present in our as-grown device layer in close proximity to the oxide

interface. Our strained Si MOSFETs also exhibit an increasing threshold voltage shift with increasing 1000°C anneal time, further evidence that the Ge-induced interface states are degrading the mobility. This interface state density of mid-10^{12}-10^{13} cm^{-2} eV^{-1} drastically reduces the MOSFET mobility at low fields, as the interface state charge decreases the Coulomb-limited mobility in the channel[110]. This effect is shown schematically in Figure 5.34. As $\mu_{Coulomb}$ decreases, the net carrier mobility drops precipitously at low fields.

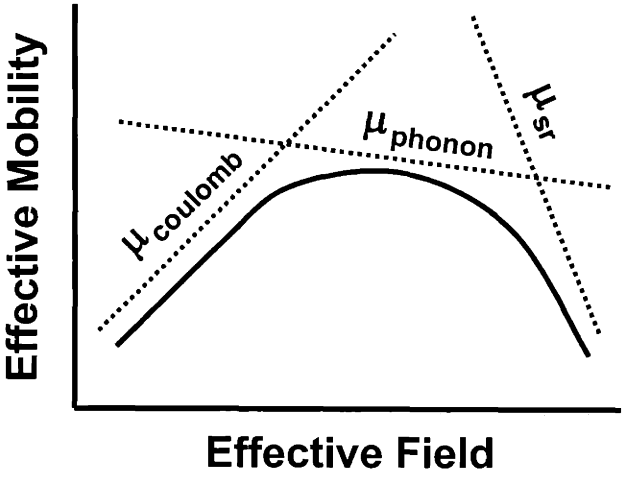

Figure 5.34 Effect of large interface state density on the effective carrier mobility curve. Increased Coulomb scattering decreases the mobility at low effective fields.

The effective electron mobility data from the sample annealed at 1000°C for 10 seconds is shown in Figure 5.35. Clearly, the interface state charge limits the mobility at low fields. As the effective field increases, this effect is vastly reduced, and there is little or no effect of the interface state charge on the mobility near 1 MV/cm[110]. The drop in mobility enhancement measured here at 0.5-0.6 MV/cm can therefore be at least partially attributed to the interface state density.

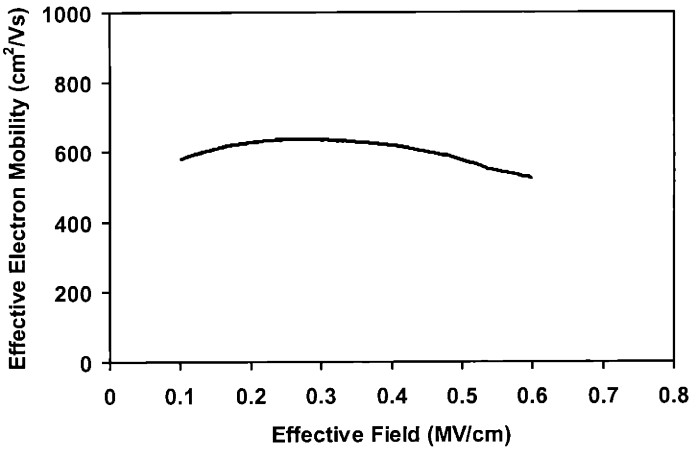

Figure 5.35 Effective electron mobility of strained Si n-MOSFET annealed at 1000°C for 10 seconds. Increased interface state density due to Ge diffusion and LTO densification depresses the mobility at low fields.

Since Ge diffusion causes intermixing between the virtual substrate and the device channels, alloy scattering could also be degrading the carrier mobility. Alloy scattering has almost exclusively been studied in the context of holes in compressively strained pseudomorphic SiGe p-MOSFETs, and the mechanism and the effects on room temperature mobility are not yet fully understood[136]. However, alloy scattering certainly affects the carrier mobility of bulk unstrained SiGe alloys, since both the electron and hole mobilities of SiGe alloys are depressed below those of pure Si and Ge[137]. As more Ge diffuses into the strained Si MOSFET layers, the average Ge content of the channel will increase. This will increase the potential impact of alloy scattering and may degrade the channel mobility. Although alloy scattering has not been studied for tensile strained SiGe, models predict that it will impact electrons more than holes due to the different orbital characteristics of the conduction band and the valence band[138]. This may play a role in the fact that the hole mobility enhancement decreases at a slower rate with

annealing time than the electron mobility enhancement. The thickness of the strained Si could also be a factor. Since the undiffused channel is only 75 Å thick, the hole mobility may be depressed due to parallel conduction in the SiGe underlayer, as described in the previous section. Thus, the channel interdiffusion will not impact the hole mobility as much as the electron mobility.

A drawback of utilizing a thin strained Si channel for surface channel MOSFETs has been identified. While thin, sub-critical thickness layers are not susceptible to misfit dislocation introduction at high temperatures, they will be more susceptible to Ge diffusion from the underlying SiGe buffer. Thus, thicker strained Si layers may be preferable for devices with increased thermal budgets. Another technique to reduce the susceptibility of strained Si MOSFETs to Ge diffusion is the use of lower growth temperatures or growth in a hydrogen ambient, as this will eliminate Ge segregation into Si layers[135], increasing the distance Ge must diffuse to reach the oxide interface. The strained Si MOSFETs in this study exhibit outstanding mobility enhancements after spike anneals at 950-1000°C, but may be more susceptible to mobility degradation during longer anneals. Hence, the tradeoff between metastability and susceptibility to Ge interdiffusion must be weighed when designing strained Si MOSFET devices.

5.10 Effect of the SiGe Virtual Substrate

As mentioned in the introductory section of this chapter, the full benefits of the type-II band offset in tensile strained Si were unrealized until the advent of the relaxed graded buffer. Earlier attempts at fabricating high electron mobility strained Si channels utilized highly defective uniform SiGe layers. In deference to the historical development of SiGe

virtual substrates, a final experiment was performed. Strained Si n-MOSFETs were fabricated on uniform 25% SiGe layers grown directly on Si substrates. During the planarization and regrowth experiment of Section 5.7.2, only a few planarized SiGe wafers were used in each growth run. In order to fill the quartz wafer boat and avoid loading effects during UHVCVD growth, several bare Si wafers were inserted during each run. One of these Si wafers with a directly grown 500 nm 25% SiGe layer and 85 Å strained Si channel was coprocessed with the planarized and regrown samples. A comparison of the electron mobilities of samples with and without graded buffer layers is shown in Figure 5.36. The device without the underlying graded buffer exhibits lower electron mobility than the bulk Si device, confirming the importance of a well-engineered SiGe virtual substrate.

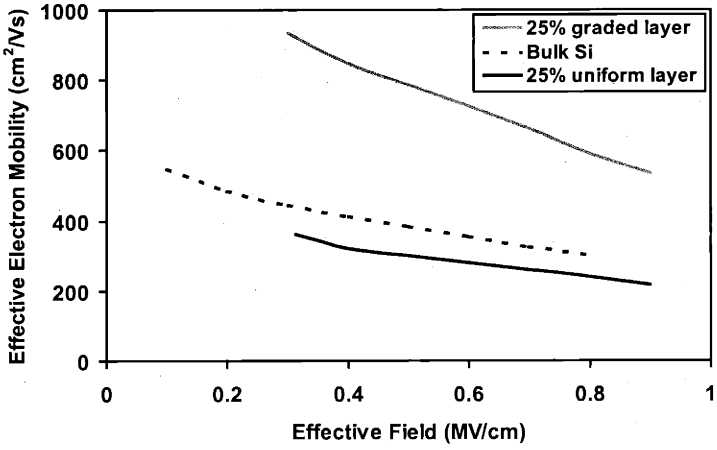

Figure 5.36 Comparison of the electron mobility of strained Si MOSFETs with and without the relaxed graded buffer layer. The device on the highly defective uniform layer exhibits lower mobility than the coprocessed bulk Si sample.

Chapter 6

Conclusions and Suggestions

SiGe virtual substrate technology provides numerous new avenues by which to extend the performance of the Si microelectronic platform. If even one of the integration schemes described in this work comes to commercial fruition, it will lead to single-chip systems of unprecedented functionality. The integration of III-V materials, MEMS devices, and high performance FETs with Si, while a daunting task, is technologically feasible. As further research and development continues, the SiGe virtual substrate has the potential to be the defining integration framework of our time.

6.1 Summary of Experimental Work

A review of SiGe relaxed graded buffer technology and its impact on material quality was presented. Dislocation pileups were identified as the culprit responsible for the escalation of threading dislocation density and surface roughness in layers graded to high Ge contents. A two-part strategy for pileup elimination involving use of offcut substrates and intermediate planarization steps was proposed and implemented. Control of dislocation pileup density has decreased the threading dislocation density in high Ge virtual substrates by over an order of magnitude. Moreover, dislocation annihilation was conclusively demonstrated during relaxed graded buffer growth for the first time. The trend of threading dislocation density with Ge content in SiGe graded buffers is approaching steady-state, as shown in Figure 6.1. Although a slight increase remains, production of SiGe virtual substrates with arbitrary Ge content and threading dislocation densities of 10^6 cm^{-2} or less is now possible.

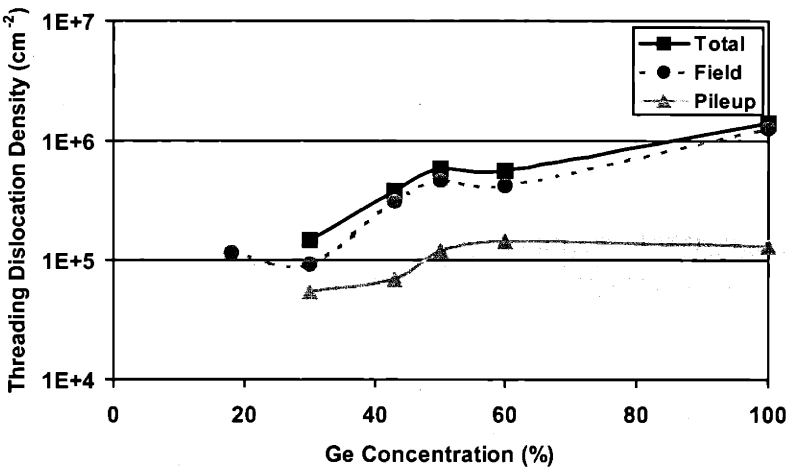

Figure 6.1 Graph of lowest threading dislocation density achieved for SiGe virtual substrates of various final Ge fractions grown by this research group. The total threading dislocation densities are within an order of magnitude of each other, signifying the approach of a steady-state dislocation density.

Low defect density SiGe virtual substrates have enabled the demonstration of record minority carrier lifetimes in GaAs on Si and the fabrication of low dark current Ge photodetectors and high quality InGaAs/GaAs LEDs on Si. The prospects for high-lifetime lasers on Si loom near as well.

New SiGe virtual substrate structures were proposed to take advantage of the etch stop properties of undoped relaxed SiGe. Growth of these layers enabled the fabrication of SiGe MEMS devices while utilizing less hazardous Si etchants. SiGe planarization via CMP was used to address surface roughness concerns, and problems with wafer bow and part curvature were also resolved. The origins of part strain in SiGe structures, as well as possible solutions, were identified. These revelations have developed relaxed SiGe into a feasible MEMS material that can be integrated with a host of other technologies.

A novel short-flow process was utilized to study several materials and processing variants of strained Si MOSFET technology. Strained Si n- and p-MOSFETs with mobility enhancements of 1.8 and 1.6 over bulk Si devices, respectively, were fabricated. The NMOS devices displayed mobility enhancement saturation for substrate Ge contents greater than 20%, while no such saturation behavior was seen for PMOS devices out to 30% Ge content in the virtual substrate, due to the smaller subband splitting in the valence band of tensile strained Si. The process stability of surface channel strained Si MOSFETs was also examined. Well implantation was found to have no negative effects on carrier mobility, except at very low fields due to increased ionized impurity scattering. This confirms that the universality of strained Si MOSFET mobility is identical to that of bulk Si MOSFETs. Planarization of the underlying SiGe virtual substrate was also found to have no negative effects on the carrier mobility of strained Si MOSFETs. Even when the SiGe regrowth thickness below the strained Si channel was decreased to 10 nm, no carrier mobility decrease was observed. The growth of the strained Si channel directly on the planarized SiGe surface decreased the electron mobility by approximately 10%, yet had no impact on the hole mobility. This confirms the suitability of these devices for state-of-the-art CMOS processing, as enhanced-mobility materials can be achieved on planar substrates suitable for fine-line lithographic techniques. The effects of high-temperature implant activation anneals were studied for strained Si devices with sub-critical thickness channel layers. Increased interface state density from Ge interdiffusion was found to be a mobility-limiting mechanism in these devices, although enhanced mobilities were achieved even after 30 second anneals at 1000°C. Alloy scattering may

also play a role in these device layers. We would expect even better high-temperature stability of thicker, more abrupt strained Si layers. For NMOS devices, the effect of channel thickness on mobility enhancement was also studied. Large mobility degradations were observed for the thinnest channel devices due to loss of carrier confinement and conduction through the SiGe underlayer. Devices with channels thicker than 50 Å displayed mobility enhancements of 1.7-1.8, even those in which low densities of misfit dislocations had been introduced. More gradual mobility degradation is expected for thick, partially relaxed channels, since carrier conduction occurs farther away from the Si/SiGe interface even as more misfit dislocations are being introduced. Generally, surface channel strained Si MOSFETs were found to display large mobility enhancements and high process stability, confirming their suitability for future application in high performance digital CMOS. Additionally, the short-flow MOSFET process was validated as an invaluable research tool, since it enabled the fabrication and study of literally hundreds of device wafers during this project.

6.2 Suggestions for Further Study

SiGe-based monolithic integration has proven to be a feasible path toward increased functionality of the Si platform. Truly, attempts to further improve the material quality of SiGe virtual substrates are being limited by the research environment. As SiGe technology moves into the manufacturing environment, some material quality improvements will naturally follow, in part due to reductions in particulate contamination. Still, dislocation dynamics and annihilation in graded buffers should be examined in greater detail. Since the use of offcut substrates can lead to net Burgers

vector populations, the effect of substrate offcut on dislocation annihilation should be analyzed. Methods to control dislocation pileup density *in situ*, perhaps via the use of planarizing tensile layers, should also be investigated. The fabrication of relaxed SiGe coplanar with Si should be addressed, perhaps via growth in recessed patterns. Other III-V devices such as lasers and optical communication links should also be fabricated in order to demonstrate the potential of SiGe virtual substrates.

The manufacturability of relaxed SiGe MEMS has been demonstrated. This achievement should facilitate new microstructural studies of the physics of MEMS devices. The quality (Q) factor of a MEMS device, related to the energy conserved during its operation, is certainly a function of the microstructure. In order to study the effects of threading dislocation density, Ge content, and p-type doping level on the Q factor of MEMS devices, a series of SiGe layers has already been grown. Samples with the partial graded buffer utilized in this study will be compared to uniform SiGe layers grown on Si to gauge the impact of increased defect density. Ge content can be altered at concentrations above the 20% etch stop boundary in order to study the effect of Ge content. The background doping of the MEMS layer can also be altered at will since the SiGe etch stop operates independent of doping. These studies lead to better MEMS material design. Additionally, they will allow an investigation of the relationship between the microstructural details and the macroscopic performance of MEMS devices.

SiGe-based heterostructure transistors obviously have the potential to extend the performance level of Si microelectronics. Several new device designs and studies should be undertaken to gauge the ultimate capabilities of this technology. Strained Si p-

MOSFETs should be studied in greater detail, particularly the effect of channel thickness on hole mobility, and the ultimate saturation of hole mobility with strain. Parallel hole conduction through the SiGe virtual substrate could be addressed via the use of compressively strained SiGe underlayers. A high Ge content strained layer directly below the strained Si layer would provide a high mobility path for those holes not confined in the channel. As an ultimate extension of this idea, complete heterostructure CMOS layer structures should be designed and fabricated to address the disparity between the mobilities of electrons and holes. The combination of tensile strained Si for electron transport with compressive Ge for hole transport has the potential of symmetric carrier mobilities enhanced far above those of bulk Si. This would lead to decreases in circuit capacitance and provide avenues for novel circuit design. Finally, the effects of alloy scattering in tensile strained SiGe should be studied systematically through the fabrication of alloy channel MOSFETs. The use of the short-flow MOSFET process will certainly enable the investigation of these and other variants in an efficient and effective manner.

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