The Hydrogen-induced Piezoelectric Effect in InP HEMTs
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Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
[September 2003]
August 2003

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ABSTRACT

Hydrogen exposure of III-V HEMTs has been shown to cause a threshold voltage shift, ΔV_T. This is a serious reliability concern. This effect has been attributed to a H-induced piezoelectric effect. Formation of TiH_x expands the Ti layer in the gate, causing mechanical stress in the underlying semiconductor. This induces piezoelectric charge in the heterostructure underneath the gate that shifts the threshold voltage. This thesis investigates the influence of the gate and heterostructure dimensions and composition on the H-induced ΔV_T in order to come up with practical device level solutions to this problem. Towards this goal, a model for the impact of the hydrogen-induced piezoelectric effect on the threshold voltage of InP HEMTs was developed using 2D finite element simulations to calculate the mechanical stress caused by a Ti-containing gate that has expanded due to hydrogen absorption. A simple electrostatics model was used to calculate the impact of this piezoelectric polarization charge on the threshold voltage. This model explained the experimentally observed gate length dependence of ΔV_T in InP HEMTs. Then, this model was experimentally verified using advanced InP HEMTs with a WSiN/Ti/Pt/Au gate or a thick Ti-layer in the Ti/Pt/Au gate stack. We have found that only a thin top layer of the thick Ti layer expanded after exposure to hydrogen. The impact of hydrogen on the threshold voltage of these devices is one order of magnitude smaller than conventional Ti/Pt/Au-gate HEMTs. The model showed that there are two main causes for the improvement of the H-sensitivity. First, the separation of the Ti-layer from the semiconductor by a thick non-expanding layer significantly reduces the stress in the active layer. Additionally, the thinner heterostructure and the presence of an InP etch-stop layer with a small piezoelectric constant underneath the gate reduces the amount of threshold voltage shift that is caused by the mechanical stress. This thesis concludes that the H-induced piezoelectric ΔV_T can be significantly reduced by placing a non-expanding layer underneath the Ti-layer in the gate stack. Thinning the channel and insulator also helps mitigate the H-induced ΔV_T.

Acknowledgements

This thesis would not have been possible without the help of many people.

First, I would like to thank Prof. Jesus del Alamo for imparting me with an ethically sound approach to research. Throughout the past six years, he provided great answers and also posed the right questions. I would also like to thank my readers, Prof. Clifton Fonstad and Prof. Rajeev Ram, for their comments and suggestions to improve this thesis.

Roxann Blanchard established a solid foundation upon which I based my research. I would like to thank her for her efforts and for her invaluable help during the past six years.

I learned a lot about InP HEMTs through my discussions with Tetsuya Suemitsu and I would like to thank him and Takatomo Enoki for providing the advanced InP HEMTs which added an important experimental component to this research.

This thesis would not have been possible without the tremendous support of the MTL and its expert staff and amazing students. The radius-of-curvature and Auger Electron Spectroscopy measurements were very successful thanks to the expert help of Tim McClure and Libby Shaw.

I would like to thank Christine Tsau for helping me run simulations at TELAC and Matthew Varghese for helping with ABAQUS. I am very grateful to Joachim Knoch for his contributions to the 2D finite element calculations and processing and to Andy Fan for all his help with processing issues.

It would not have been as much fun as it has been to come to work every day without the amazing colleagues of the Gigahertz Power Transistor group: Joerg Appenzeller, Roxann Blanchard, Ritwik Chatterjee, James Fiorenza, Joachim Knoch, Sergei Krupenin, Tassanee Payakapan, Jorg Scholvin, Mark Somerville, Tetsuya Suemitsu, Anita Villanueva, Niamh Waldron and Joyce Wu. I was lucky to work with such talented colleagues and friends. I have learned so much from all of you.

I must thank my other friends here in Boston, especially the players from MIT rugby, for making this a fun place to live. My friends back in Belgium have also been very

supportive, keeping in touch is not always easy but it is certainly worthwhile. Without these friends it would not have been such joy to work on this doctorate.

The last couple of years would not have been so amazing without my girlfriend, Sara Carney. Thank you for all your love, which is always a great inspiration. This thesis was greatly improved because of your editing work. I would also like to thank her parents, Mike and Laurie Carney for cheering me on.

I would not have been able to undertake this work without the endless support of my parents, Nico and Gilda Mertens-Behaeghel and the Mertens and Behaeghel families. Thank you mama and papa for encouraging me to pursue my dreams, even though it meant I could not see you as often as I wanted. I hope my brother Kenneth enjoys his PhD research as much as I have.

This work has been made possible by the Army Research Office, HRL, NTT and Triquint. This work made use of the MRSEC Shared Facilities supported by the National Science Foundation under Award Number DMR-9400334.

For my grandmothers, Yvonne Vanhalst and Cecile Vanrietvelde

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Chapter 1

Introduction

InAlAs/InGaAs High Electron Mobility Transistors (HEMT), also known as Modulation Doped Field Effect Transistors (MODFET) are fulfilling their promise for low-noise and power millimeter-wave applications that arise from their extremely high frequency response [1]. As InP HEMT technology approaches the specifications needed for 100 Gb/s mixed-signal communications applications interest in it has grown significantly [2].

Several issues must be resolved if these devices are to meet their potential. Technological problems with scaling down the transistor and reducing of parasitic capacitance have to be solved [2]. Manufacturability limits the number of transistors in a circuit to a few thousand [3]. In addition, reliability issues still hinder the development of several InP HEMT applications [4] This work focuses on a key reliability concern, occurring when the HEMTs operate in an atmosphere containing hydrogen.

1.1. InP HEMTs

One path to high-speed optical communication networks relies on the ability to build reliable 100 Gbit/s integrated circuits [2]. This requires transistors with cut-off frequencies, f_T, over 280 GHz and a transconductance, g_m, over 1.4 S/mm. InP HEMTs

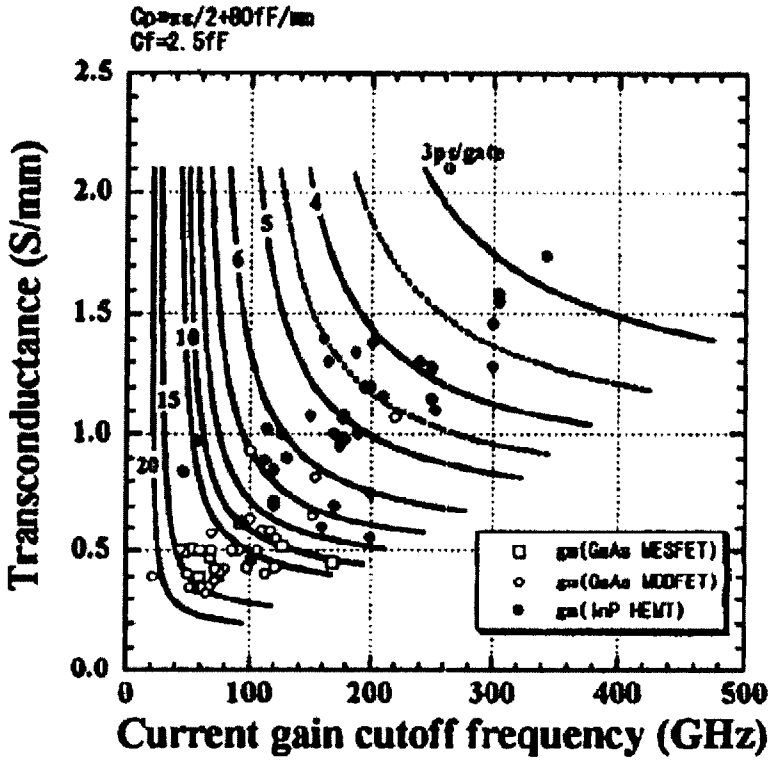

Figure 2.1: Contours of calculated gate delay time for source-coupled FET logic inverters and transconductance, g_m, vs current-gain cutoff frequency, f_T, for different planar transistor technologies (figure used from [2]). The points represent experimental observations for several planar transistor technologies. The lines present the minimum requirement of g_m and f_T needed for a certain gate delay time.

are better suited than other planar transistor technologies to meet these specifications [2] (Fig. 1.1). The graph shows experimental observations of g_m as a function of f_T for different types of planar transistors: GaAs MESFETs, PHEMTs and InP HEMTs. In order to attain a certain gate delay, both f_T and g_m have to be high enough, as shown by the lines. It can be seen that InP HEMTs show the highest combination of f_T and g_m. A gate delay of under 3 ps/gate is required for 100 Gb/s operation. InP HEMTs are the only planar transistors that have shown to be capable of this level of performance to date.

A conventional InP HEMT is shown in Fig. 1.2. The $In_{0.53}Ga_{0.47}As$ channel is sandwiched between a δ-doped $In_{0.52}Al_{0.48}As$ insulator and an $In_{0.52}Al_{0.48}As$ buffer layer. This results in a 2D-electron gas in the undoped channel. In Fig. 1.2, the device layers are lattice matched to InP and grown on an InP substrate. InP Metamorphic HEMTs,

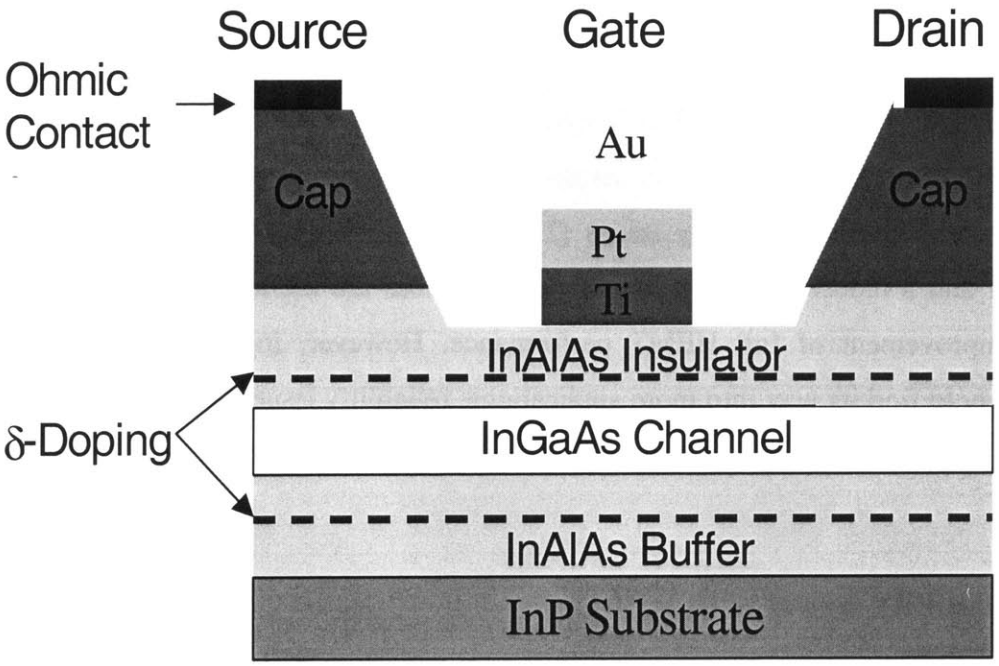

Figure 1.2: Sketch of an InP HEMT.

MHEMTs, are grown on a GaAs substrate and the lattice mismatch is solved by using a graded buffer layer under the lattice-matched buffer. Recently, strained channels in which the In-content in the channel of InP HEMTs is increased, compared to the InGaAs that is lattice matched to InP, are being used. This improves the electrical characteristics because electron velocity increases with In-content ([5] and [6]). A GaAs Pseudomorphic HEMT, PHEMT, has an AlGaAs insulator and buffer and an InGaAs channel and is grown on a lattice matched GaAs substrate.

The gate of an InP HEMT typically consists of a Ti/Pt/Au stack. The Ti layer forms the Schottky contact. The Pt is a barrier layer that is used to avoid a reaction between Ti and Au [7]. The thick Au layer reduces the gate resistance. The Ti/Pt/Au gate stack assures a simple and low-damage fabrication process [8].

This material system currently holds the speed records amongst all three-terminal devices for the highest cut-off frequency f_T= 562 GHz [9] and the highest maximum frequency of oscillation f_{max}= 600 GHz [10]. The circuit speed performance of these devices has been very impressive. Recently, a 100Gb/s multiplexing and demultiplexing

logic IC was presented [1]. Low Noise Amplifiers for very high frequencies have been demonstrated, a 6-stage amplifier showed a 15 dB gain at 215 GHz [11].

InP HEMT and GaAs PHEMT technologies have now become rather mature. Research has recently focused on issues of circuit performance, device integration, manufacturability and reliability issues [12]. Enoki has found that the scaling of the transistor and a reduction of the parasitic capacitances are the biggest concerns for the future improvement of InP HEMT performance. However, in order for InP HEMT technology to find its way into more applications, reliability issues must also be resolved [4].

1.2. Reliability Issues with HEMTs

Virtually all aspects of InP-based HEMTs have been observed to degrade during device operation. The variety of reported degradation mechanisms is as vast as that of the material structures and metallizations used in the fabrication of HEMTs. Amongst the different degradation mechanisms that have been reported, the most important are described next.

- Schottky gate contact degradation due to metallurgical interactions (particularly gate sinking) has been reported for different gate stacks and heterostructures [13], [14]. In this mechanism, the gate metal diffuses into the Schottky-barrier layer causing the threshold voltage to shift and the drain current to degrade [15].
- Reportedly, hot electrons in the gate-drain region have caused ohmic contacts to degrade [16]. Surface degradation caused by hot electrons has also been observed [17].
- Deterioration of the InAlAs surface has been identified as a cause of drain current degradation for lattice-matched InP HEMTs [18]. If the surface layer is not passivated, Al can diffuse out of the semiconductor lattice to oxidize at the surface [18].

- The diffusion of Ti into the AlInAs insulator under the gate has been reported to decrease the sheet carrier concentration [19].
- The crystalline structure of the channel and the insulator have been found to degrade under thermal stressing [20]. This degradation decreases the mobility in the channel.
- The atmosphere surrounding the devices significantly influences the reliability of InP HEMTs. Fluorine-contamination from the air has been noted as a failure mechanism [21], whereby the F decreases the intrinsic sheet carrier concentration.
- Hydrogen degradation is a serious reliability concern in III-V FETs in general and InP HEMTs in particular [22]. In applications demanding hermetically-sealed packaging, such as satellite or fiber-optic systems, exposure occurs when H out-gasses from the packaging material and becomes trapped inside the package cavity [23]. With enough time, H diffuses into the transistor and alters its electrical characteristics, eventually leading to parametric module failure.

This thesis studies the degradation of HEMTs caused by exposure to H.

1.3. H-effects in III-V FETs

The effects of hydrogen on compound semiconductors have been studied extensively. Hydrogen has been used to passivate defects during growths [24, 25] as defect-hydrogen complexes are formed. Hydrogen passivation of shallow impurities [26-29] has been observed for both donors and acceptor states, increasing the electron mobility. H improves the passivation of compound semiconductor surfaces, as it reacts with the free As on the surface, forming volatile arsine. The arsine disappears from the surface together with the generation-recombination centers and surface leakage that are associated with free As [24].

Camp [23] and Hu [30] linked degradation of GaAs FETs to the presence of H. They suggested that the Ti/Pt/Au gates play a role in the degradation mechanism. Pt is a known catalyst for molecular hydrogen, helping to break it up into atomic hydrogen. Work by

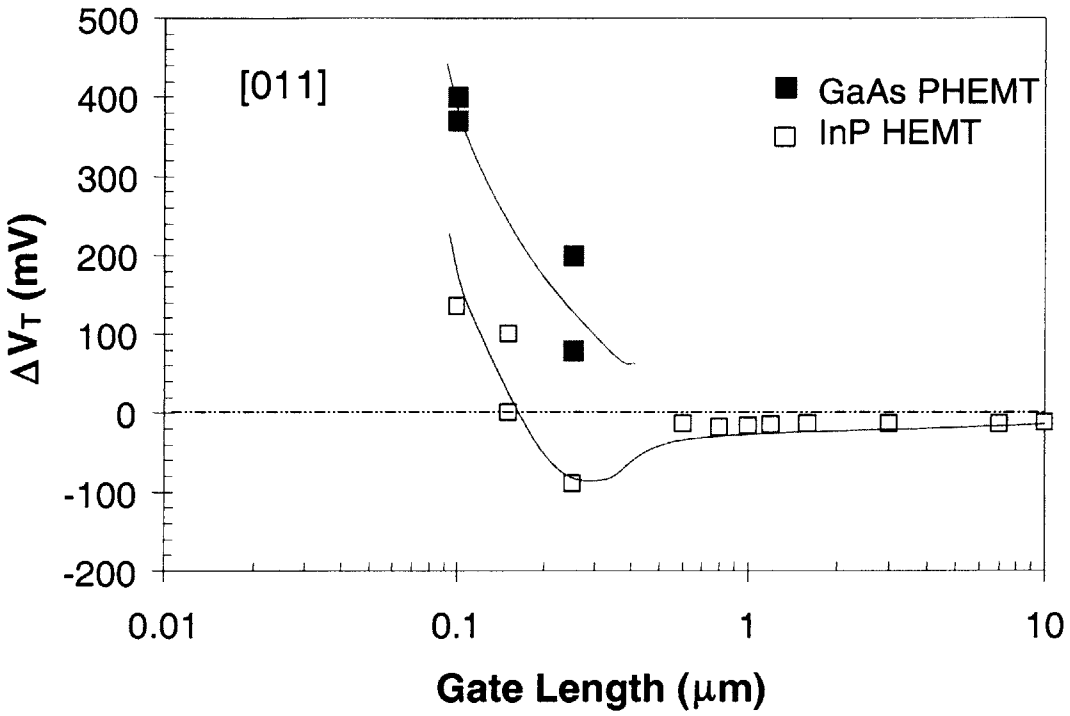

Fig. 1.3: Literature reports of ΔV_T caused by hydrogen exposure as a function of gate length for InP HEMTs and GaAs PHEMTs with gates oriented along the [011] direction [31, 33, 34, 35, 36].

Chao et al. [31] showed that the device degradation was affected by the thickness of the Pt layer in the gate stack. Later, Chao et al. [32] showed that the Ti layer was crucial to the degradation mechanism. The same degradation was seen in devices with a pure Ti gate and devices with a Ti/Pt/Au gate stack [32]. The former have a much higher Mean-Time-To-Failure, MTTF, showing the presence of Pt speeds up this mechanism.

The major effect of H-absorption on HEMT characteristics is a shift in the threshold voltage. The few published reports of the sign and magnitude of ΔV_T in InP HEMTs and GaAs PHEMTs seem contradictory (all devices have Ti/Pt/Au gates). While reports on [011]-oriented GaAs PHEMTs indicate a positive ΔV_T [31], [011]-oriented InP HEMTs have been found to display positive [33], negative [31], and even negligible V_T shifts [34]. When all the data are graphed together a compelling picture emerges (Fig. 1.3) [22]. It appears that for GaAs PHEMTs, ΔV_T is always positive and increases as the gate length is reduced. However, no data exists for long devices. For long gate length InP HEMTs, ΔV_T is negative and increasing in magnitude with decreasing L_g. At a certain L_g

there is a sign reversal and the H-induced ΔV_T becomes positive. For shorter devices ΔV_T increases.

Other changes in device characteristics have been observed to degrade because of H-exposure [37]. The extrinsic sheet carrier concentration has been seen to decrease, increasing the off-state breakdown-voltage and the parasitic resistances. These effects are relatively less significant than the shift in V_T, which this thesis focuses on.

A shift in the threshold voltage can affect circuit performance severely. In differential amplifiers, a change in the threshold voltage, ΔV_T, will cause a difference in the offset voltage of $\Delta V_T/2$ [38]. In digital circuits, a shift of 100 mV in threshold voltage has been observed to cause a 20 % reduction of the operation speed [39]. Circuit-design techniques such as self-biased current regulation can significantly reduce the effects of threshold voltage changes on the bias current of a low-noise amplifier. The change in the bias current is proportional to the magnitude of the change in threshold voltage [40]. Process variation causes a standard deviation of 13 mV in the threshold voltage of HEMTs for different devices on a wafer [41]. Any circuit design has to take threshold voltage shifts of this magnitude into account.

1.4. Physical Mechanisms of H-induced ΔV_T

Blanchard [37] found that there are two mechanisms that shift the threshold voltage of HEMTs during exposure to H. In the first mechanism, the molecular H_2 is absorbed by the Pt-layer in the gate stack where it dissociates into atomic H. This atomic H reacts with the Ti in the gate stack to form TiH_x platelets. This causes a mechanical expansion of the Ti-layer, which creates a mechanical stress in the underlying semiconductor. Since III-V semiconductors are piezoelectric, a piezoelectric polarization charge is induced underneath the gate, shifting the threshold voltage of the HEMT. This mechanism is dependent on the gate orientation and gate length. A second degradation mechanism, also identified by Blanchard, causes a negative threshold voltage shift that is attributed to the penetration of H^+ ions in the semiconductor, which shifts the threshold voltage negatively in [35]. In Blanchard's work, this shift is of the order of –8 mV, independent of the gate

length and gate orientation [37]. This is small compared to the standard deviation of V_T from device to device on a wafer. This thesis did not study this degradation mechanism.

The degradation mechanism behind the H-induced piezoelectric effect was experimentally verified in an independent manner by [37]. Blanchard observed the formation of TiH_x using Auger Electron Spectroscopy of Pt/Ti-covered wafers that were exposed to H_2 at an elevated temperature [35]. The concentration of TiH_x decreased significantly with depth increasing within the Ti layer. The formation of TiH_x was reversible during an anneal in N_2. Radius-of-curvature measurements showed that the formation of TiH_x causes compressive stress in the Ti layer [42].

The H^+-penetration hypothesis was tested by exposing a HEMT to a forming gas environment at an elevated temperature and a constant V_{GS}. After the shift in threshold voltage saturated, V_{GS} was changed, changing the vertical electric field across the heterostructure. This resulted in a shift of the threshold voltage consistent with the H^+ atoms being swept away from under the gate by the field caused by the gate-to-source voltage.

After the work by Blanchard et al., the physical mechanism behind the H-induced piezoelectric effect is now relatively well understood. How different aspects of the device design, such as the gate length, the gate stack dimensions, or the heterostructure, alter the H-induced V_T-shift is not. As is shown in Fig. 1.3, the magnitude of ΔV_T can differ from device to device by an amount greater than an order of magnitude. Additionally, the sign of ΔV_T seems to depend on the gate length. The experimental data on Fig. 1.3 suggests ΔV_T increases in absolute magnitude as the gate length shortens, but it is not well understood why. State-of-the-art short InP HEMTs should show large V_T shifts. In addition, practical device level solutions that mitigate this reliability problem are still unknown. Establishing how the device design impacts the H-sensitivity is important to developing device level solutions to this problem.

1.5. Thesis Goals and Outline

Hydrogen causes severe reliability concerns in InP HEMTs. A few degradation mechanisms have been identified experimentally [37], but the gate length dependence of

the threshold voltage shift has not been explained. A goal of this work was to develop a model for the H-induced piezoelectric V_T shift that would allow studying the influence of different gate lengths, heterostructures and gate stacks on the H-sensitivity and identifying device level solutions to this problem.

The model simulated the effect of the expansion of the TiH_x-layer in the gate structure on the threshold voltage shift, and contained the different device parameters that impact the hydrogen sensitivity. The details of the model are presented in Chapter 2. In essence, two-dimensional mechanical simulations of the mechanical stress were performed using ABAQUS. The resulting atomic displacements were then used to calculate the piezoelectric charge in the semiconductor using MATLAB [43]. From this, the H-induced V_T shift was calculated using a one-dimensional electrostatic model at the center of the gate.

It is important to experimentally verify the model's theoretical predictions using industrial devices of different designs. This has been done in collaboration with industrial partners, from whom a number of experimental devices were received. The H-induced threshold voltage shift was observed as a function of the different design parameters, most importantly, the gate length. Chapter 3 shows the study of the H-sensitivity of advanced InP HEMTs with a thin heterostructure and a WSiN-layer underneath the Ti/Pt/Au gate-stack. Separating the expanding Ti layer from the semiconductor by a non-expanding WSiN layer reduces the stress, and thus the piezoelectric charge, in the semiconductor. Experimentally these devices showed very small H-induced V_T-shifts. The simulation framework was then used to explain the reduced V_T-shift of these devices when compared with conventional devices.

One of the important predictions of the model presented in Chapter 2 is that the V_T-shifts increase when the Ti layer in the Ti/Pt/Au gate stack thickens. To test this hypothesis, InP HEMTs with a 1000 Å thick Ti layer in the gate were studied. Chapter 4 presents the experimental and simulation results on these devices. Two different degradation mechanisms were observed: a H-induced piezoelectric effect plus an additional degradation that has been attributed to a processing issue. The H-induced piezoelectric effect caused very small V_T-shifts, inconsistent with a homogeneously expanding Ti layer. The simulation framework showed that the results can be explained if

only the top layer of the Ti reacts to form TiH_x. This hypothesis was confirmed using Auger Electron Spectroscopy through which the depth of TiH_x formation into the Ti layer was determined.

Understanding the factors that influence H-reliability of InP HEMTs leads to proposals for device level solutions to this problem. Chapter 5 discusses the limitations of the model and how the scaling of the different aspects of device design impact the H-induced piezoelectric effect. Device level solutions are proposed at the end of the chapter.

Finally, Chapter 6 summarizes the main findings of this thesis and makes suggestions for further work.

Chapter 2

Model for H-induced piezoelectric effect in InP HEMTs and GaAs PHEMTs

2.1. Motivation

The physical mechanism behind the H-induced piezoelectric effect was explained by Blanchard [37]. The experimental observations of the H-induced ΔV_T, as shown in Fig. 1.3, change in sign and in magnitude between a couple of mV to several hundreds of mV depending on the gate length. Previous work on this effect has been focused on the physical mechanisms [37]. The dependence of the H-induced ΔV_T on the gate length and the device design, however, has not been studied systematically.

In this thesis, the H-induced piezoelectric effect was studied using a modeling environment, which is discussed in this chapter. The model enabled an investigation of the key parameters that affect the H-induced piezoelectric effect. The modeling approach involved: i) performing two-dimensional mechanical stress simulations of the device structure, ii) computing the resulting piezoelectric charge in the semiconductor heterostructure, and iii) estimating its effect on V_T. In the mechanical simulations it was

Material	Young Modulus [GPa]	Poisson's ratio
Ti	116 [44]	0.32 [44]
Pt	168 [44]	0.38 [44]
Au	78 [44]	0.44 [44]
$In_{0.53}Ga_{0.47}As$	100 [45]	0.25 [45]
$In_{0.52}Al_{0.48}As$	96 [45]	0.26 [45]
$Al_{0.24}Ga_{0.76}As$	73 [45]	0.23 [45]
$In_{0.22}Ga_{0.78}As$	111 [45]	0.24 [45]
SiN	320 [44]	0.32 [44]

Table 2.1: Mechanical material constants.

Material	d_{14} [C/dyne]	μ [10^{10} dyne/cm^2]
GaAs	3.36 [46]	48.6 [45]
InAs	1.14 [47]	31.4 [45]
AlAs	5.00 [48]	44.2 [45]

Table 2.2: Piezoelectric material constants. The ternary compounds are linearly interpolated in between the binaries.

assumed that the transistor was infinitely wide to enable a 2D model. This is a fair assumption, since the width of the gate is significantly larger than its length.

This chapter first discusses the mechanical simulation framework and how it is translated into an electrostatic problem. Then, the derivation of a 1D model for the V_T shift induced by a piezoelectric charge in the semiconductor is detailed. The 1D approximation is a valid assumption, since for a low V_{DS} the threshold voltage is set at the center of the gate. The model is applied to a reference structure, similar to the HEMTs that were studied in [37], and the gate length dependence of the H-induced ΔV_T is explained. The chapter finishes with a discussion of some aspects of the influence of the gate design and the heterostructure on the H-induced V_T shift.

2.2. Mechanical Modeling

First, a 2D finite-element simulation tool, ABAQUS, was used to calculate the mechanical stress in the device layer structure that is caused by the formation of TiH_x in the Ti/Pt/Au gate. The expansion of the Ti layer was modeled as a thermal expansion of the bottom layer of the gate stack. Here, the complete Ti layer expanded homogeneously. The results of the simulations, the mechanical displacements used to calculate the mechanical stresses and strains, are linearly proportional to the amount of expansion of the Ti layer. Because of this, all results are presented in arbitrary units since the expansion of the Ti layer is not known.

The mechanical properties of the materials used in the simulations can be found in Table 2.1. In general, the values of these material properties are not very well established for the semiconductor material. Fig. 2.1 shows a sketch of the mechanical mesh that was used. This sketch is not a perfectly scaled representation, but an illustration showing the different grid sizes that were employed. A finer mesh was used near the surface of the heterostructure and directly underneath the gate to provide a detailed picture of the mechanical stress where it has the biggest impact on V_T. Symmetry was exploited by only simulating half of the structure. This implied that the center of the structure was fixed in space, so no displacement could occur in the horizontal direction for any point in

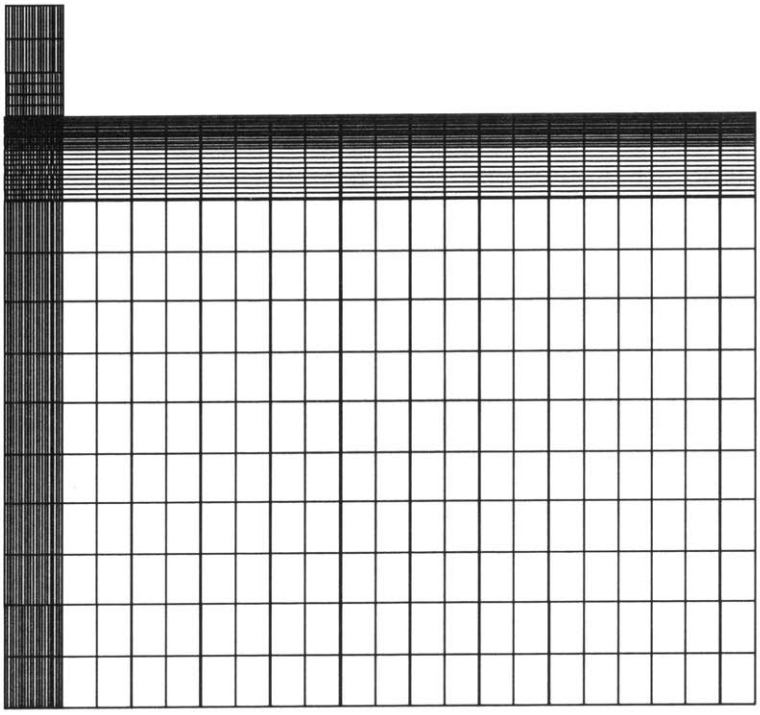

Fig. 2.1: Sketch of the mesh used in the 2D mechanical simulations.

the heterostructure and the gate stack exactly under the center of the gate. The mesh extended by 20 μm in the vertical direction and 50 μm in the horizontal direction from the center of the gate. Because the HEMT is surrounded by material that is not expanding, the mechanical structure was also fixed at the bottom and on the side far from the gate. There were 16,000 mesh nodes in the semiconductor heterostructure and 6,400 mesh nodes in the gatestack and passivation layer. The product of this simulation was the atomic displacements u_x, along the length of the gate and u_z perpendicular to the semiconductor heterostructure.

A HEMT with a 300Å insulator layer, a 200Å channel and a 2500Å buffer layer was selected for the model device (Fig. 2.2). This structure is similar to the InP HEMTs studied in [37]. Most of the experimental results in Fig 1.3 were observed on HEMTs with this device design. The gate stack is made of 250Å Ti/ 250Å Pt/3000Å Au and is oriented parallel to [011]. The device is entirely covered by 600Å of Si_3N_4. The InP HEMTs have an $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As/In_{0.48}Al_{0.52}As$ heterostructure and the GaAs PHEMTs have an $Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As/Al_{0.24}Ga_{0.76}As$ heterostructure.

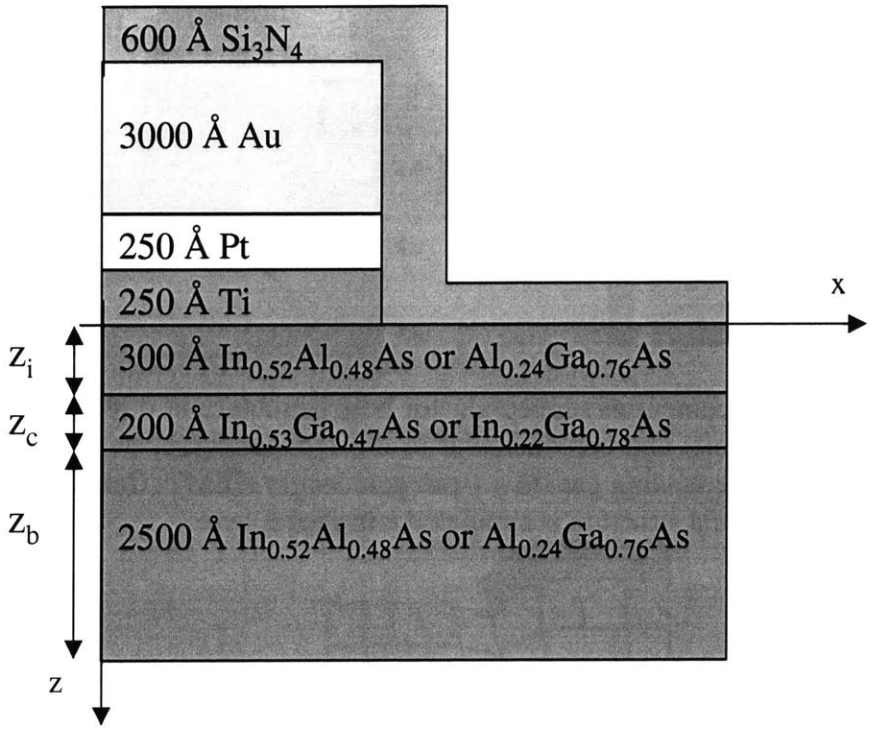

Fig. 2.2: Simulated device structures. Both the InP HEMT (first material in heterostructure) and GaAs PHEMT (second material in heterostructure) were simulated.

A typical result of the 2D finite-element mechanical simulations is shown in Fig. 2.3, which graphs the atomic displacements in the heterostructure of a 1 μm gate length InP HEMT (u_x on left, u_z on right). All results are plotted using arbitrary units, because they are linearly proportional to the expansion of the Ti-layer. The expanding gate compresses the semiconductor in the extrinsic portion of the device away from the gate and down, while stretching and pulling up the material underneath the gate, as sketched in Fig. 2.4. u_x is maximal directly below the edge of the gate. The semiconductor is pushed down the most directly underneath the edge of the gate and pulled up the most directly underneath the center of the gate.

2.3. Piezoelectric Charge

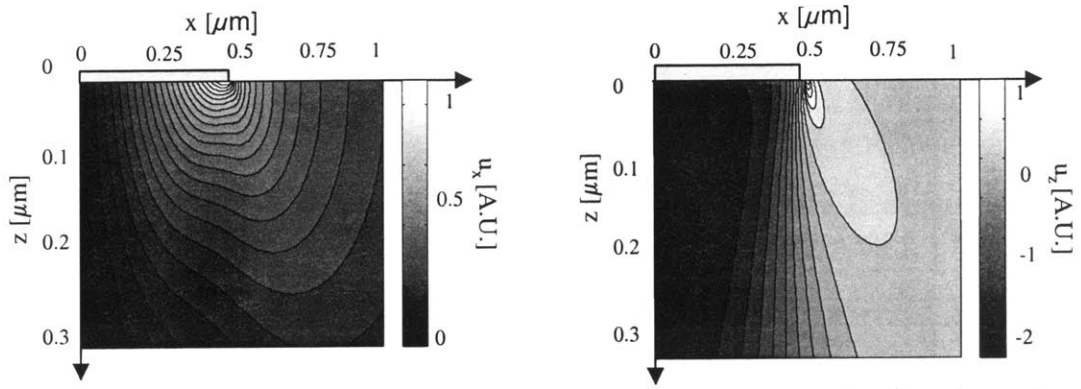

Fig. 2.3: Relative displacement of semiconductor heterostructure in directions along the length of the gate (left) and perpendicular to the semiconductor heterostructure (right) produced by an expanding gate in a 1 μm gate length HEMT. Calculations by ABAQUS. Only half of the structure is simulated and shown here.

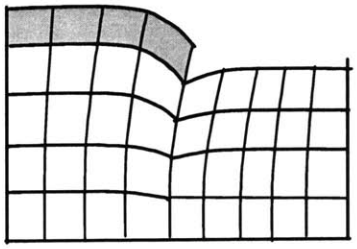

Fig. 2.4: Sketch of the displacement in the semiconductor caused by an expanding gate.

In the second step, u_x and u_z were used to compute the polarization vector field, $\vec{P}$, and the polarization charge distribution, ρ_{pol}, throughout the device [30]. The components of the polarization vector for a III-V semiconductor with a gate in the (100) plane and a gate orientation at an angle φ relative to the [001] orientation are respectively given by [49]:

$$P_x = -\mu\, d_{14} \cos\varphi \sin\varphi \left(\frac{du_x}{dz} - \frac{du_z}{dx} \right) \qquad [2.1]$$

$$P_y = \frac{\mu\, d_{14}}{2} \left(\cos^2\varphi - \sin^2\varphi \right) \left(\frac{du_x}{dz} - \frac{du_z}{dx} \right) \qquad [2.2]$$

$$P_z = -\mu\, d_{14} \cos\varphi \sin\varphi \frac{du_x}{dx} \qquad [2.3]$$

In these equations, μ is the Voight average shear modulus and d_{14} is the piezoelectric constant of the material [45-48]. The values of these constants are specific to each semiconductor layer. Since experimental or theoretical values were unavailable for the ternary compounds studied in this work, μ and d_{14} were obtained by interpolation from the binaries (Table 2.2).

For a gate in the [011] orientation, φ=45°, and the components of the polarization vector are given by:

$$P_x = -\frac{\mu d_{14}}{2}\left(\frac{du_x}{dz} - \frac{du_z}{dx}\right) \qquad [2.4]$$

$$P_y = 0 \qquad [2.5]$$

$$P_z = -\frac{\mu d_{14}}{2}\frac{du_x}{dx} \qquad [2.6]$$

The piezoelectric charge can be calculated using:

$$\rho_{pol} = -\nabla \cdot \vec{P} \qquad [2.7]$$

As discussed in the next section, computing the piezoelectric charge is not essential to deriving ΔV_T. However, since ρ_{pol} is a scalar, it provides for a compact way of visualizing and understanding the impact of stress on the electrostatics of the problem.

The piezoelectric polarization is highly dependent on the orientation of the gate [37]. The sign of the piezoelectric polarization flips when the gate orientation is parallel to $[01\bar{1}]$ instead of [011]. When the gate-orientation is parallel to the [010] or [100] direction, P_x=0 and P_z=0 and no piezoelectric charge is induced, as can be seen by calculating equations [2.1] and [2.3] with φ=0° and φ=90°. Regrettably, placing the gates in the [010] orientation in order to mitigate the H-sensitivity of HEMTs is undesirable due to fabrication issues.

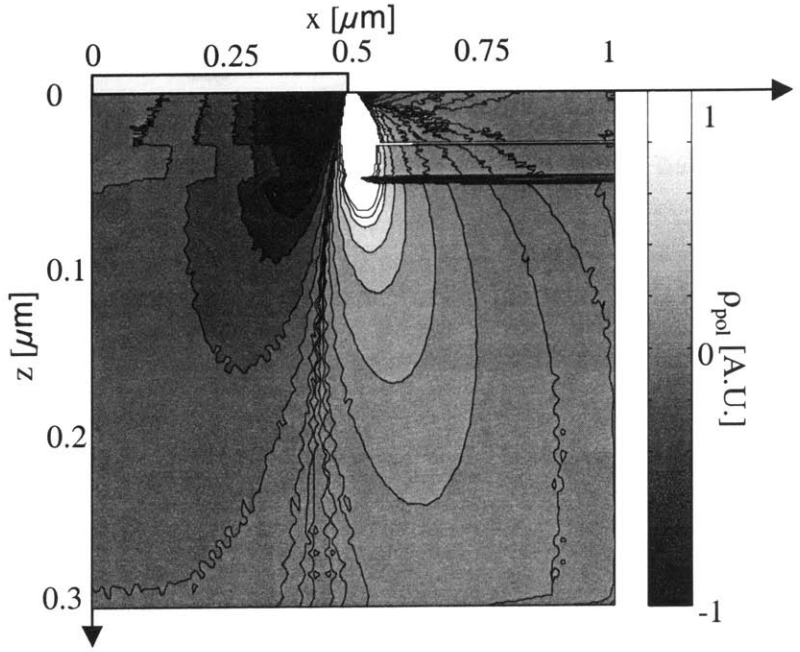

Fig. 2.5: Relative 2D piezoelectric charge distribution in the heterostructure of a 1 μm HEMT stressed by an expanding gate. Only half of the structure is simulated and shown here.

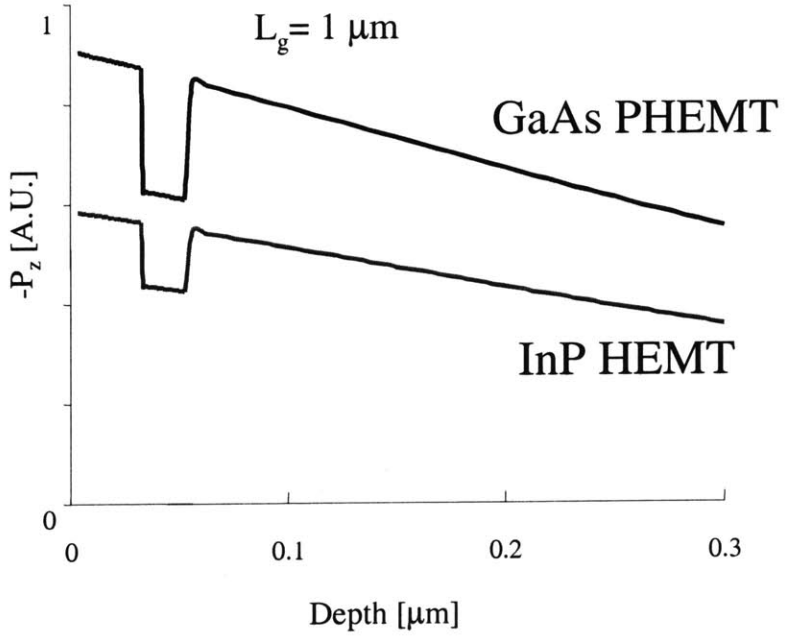

Fig. 2.6: Piezoelectric polarization vector in the direction perpendicular to the semiconductor heterostructure, $-P_z$, for an InP HEMT and a GaAs PHEMT with 1 μm gate length.

The atomic displacement information from Fig. 2.3 was used to calculate the corresponding piezoelectric charge distribution in the device and shown in Fig. 2.5, which exhibits lobes of charge emanating from the edge of the gate. This charge is positive underneath the gate and positive next to the gate. As is shown in the next section, the threshold voltage shift depends only on the component of the piezoelectric polarization perpendicular to the semiconductor surface directly underneath the center of the gate, $-P_z(x=0,z)$. Since the stress in the semiconductor decreases with distance from the edge of the gate, $-P_z(x=0,z)$ decreases with depth into the semiconductor as is shown on Fig. 2.6 for a HEMT with a gate length of 1 μm.

2.4. Model for the V_T shift

The final step was to compute the effect of the polarization charge on V_T. For simplicity, a 1D model was assumed in which ΔV_T is calculated at the center of the gate. This is a fair assumption particularly if V_T is experimentally extracted in the linear regime as is commonly done [33,35] and because the gate length is typically much larger than the thickness of the insulator and channel. Symmetry arguments show that at the center of the gate the component of the polarization vector along the length of the gate, P_x, is zero. Hence, we are only concerned with P_z, its component perpendicular to the semiconductor heterostructure. In our V_T model, we assumed that the inversion layer at threshold appears at the bottom of the channel, as sketched in the band diagram in Fig. 2.7, next to the buffer-channel interface, as is the case with double-heterostructure HEMT (it is easy to adapt the theory for other device designs).

A boundary condition with significant impact on the ΔV_T model is the nature of the buffer-substrate interface. We have studied two extreme cases, in which the Fermi-level is either unpinned or perfectly pinned at the heterostructure-substrate interface.

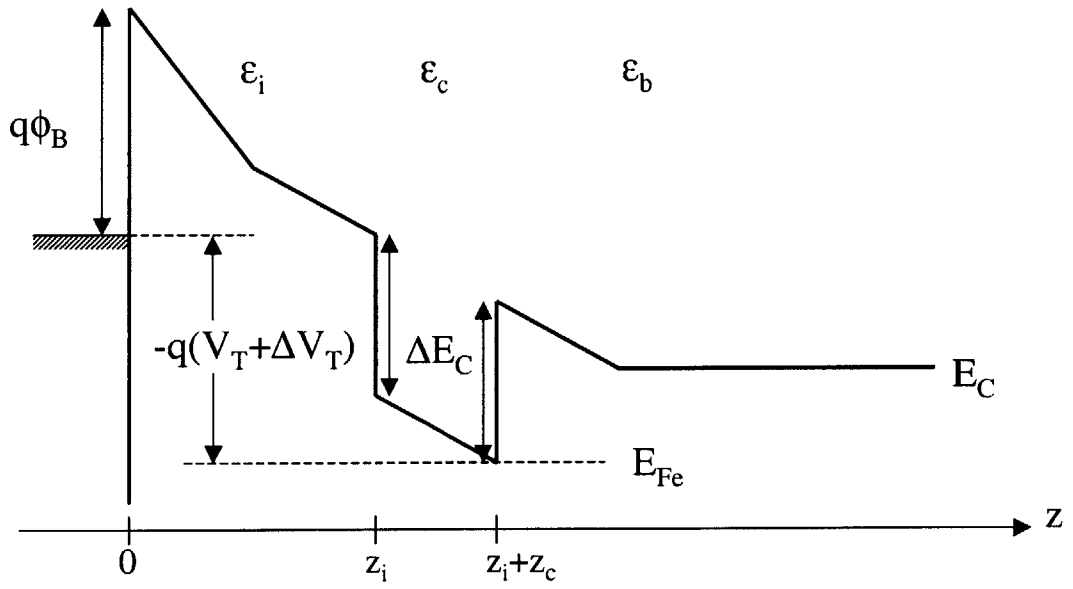

Fig. 2.7: Conduction energy band diagram at threshold at the center of the gate of a HEMT, perpendicular to the gate.

2.4.1. Unpinned Fermi-level at Buffer-heterostructure Interface

First, a 1D model for V_T was developed for the case in which the Fermi-level is unpinned at the heterostructure-substrate interface. Looking at the band diagram in Fig. 2.7, it can be seen that in this situation:

$$q\phi_B - q(V_T + \Delta V_T) = E_C(0) - E_C(z_i + z_c) + \Delta E_C \qquad [2.8]$$

In this equation, V_T is the threshold voltage without any polarization charge, ΔV_T is the threshold voltage shift induced solely by the polarization charge, $q\phi_B$ is the Schottky barrier height of the gate metal, ΔE_C is the discontinuity in the conduction band between channel and buffer (and insulator), and E_C is the energy level of the conduction band edge. z_i and z_c are the thicknesses of the insulator and the channel layer, respectively, as sketched in Fig. 2.2.

Poisson's law states:

$$\frac{d\left[\varepsilon(z)E(z) + P_z(z)\right]}{dz} = \rho(z) \qquad [2.9]$$

where $\rho(z)$ is the Coulombic charge present in the structure, $E(z)$ is the electric field, and $\varepsilon(z)$ is the permittivity of the material. The values of $\varepsilon(z)$ in the insulator, channel and buffer layer are denoted ε_i, ε_c and ε_b respectively.

Equation [2.9] can be integrated from a point z_0 to another point z to find:

$$E(z) = \frac{\varepsilon(z_0)E(z_0) + P_z(z_0)}{\varepsilon(z)} - \frac{P_z(z)}{\varepsilon(z)} + \frac{1}{\varepsilon(z)}\int_{z_0}^{z}\rho(z)dz \qquad [2.10]$$

The conduction band energy difference between two points, z_1 and z_2, in the structure now becomes:

$$\begin{aligned} E_C(z_2) - E_C(z_1) &= q\int_{z_1}^{z_2}E(z)dz \\ &= q\left[\varepsilon(z_0)E(z_0) + P_z(z_0)\right]\int_{z_1}^{z_2}\frac{dz}{\varepsilon(z)} - q\int_{z_1}^{z_2}\frac{P_z(z)}{\varepsilon(z)}dz + q\int_{z_1}^{z_2}\frac{1}{\varepsilon(z)}\left(\int_{z_0}^{z}\rho(z)dz\right)dz \end{aligned} \qquad [2.11]$$

In order to derive an expression for $V_T+\Delta V_T$, we select $z_0=\infty$, $z_1=z_i+z_c$ (the location of the channel) and $z_2=0$ (the gate/semiconductor interface). At $z_0=\infty$, $E(\infty)=0$, and $P(\infty)=0$. Then the conduction band build up between the bottom of the channel to the semiconductor surface is:

$$E_C(0) - E_C(z_i + z_c) = q\int_{z_i+z_c}^{0}E(z)dz = -q\int_{z_i+z_c}^{0}\frac{P_z(z)}{\varepsilon(z)}dz + q\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z)}\left(\int_{\infty}^{z}\rho(z)dz\right)dz \qquad [2.12]$$

Plugging this in [2.8], we get:

$$V_T + \Delta V_T = \phi_B - \frac{\Delta E_C}{q} + \int_{z_i+z_c}^{0}\frac{P_z(z)}{\varepsilon(z)}dz - \int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z)}\left(\int_{\infty}^{z}\rho(z)dz\right)dz \qquad [2.13]$$

Only one term on the right side of the equation is dependent on the piezoelectric charge. Then ΔV_T is given by:

$$\Delta V_T = -\int_{0}^{z_i+z_c}\frac{P_z(z)}{\varepsilon(z)}dz \qquad [2.14]$$

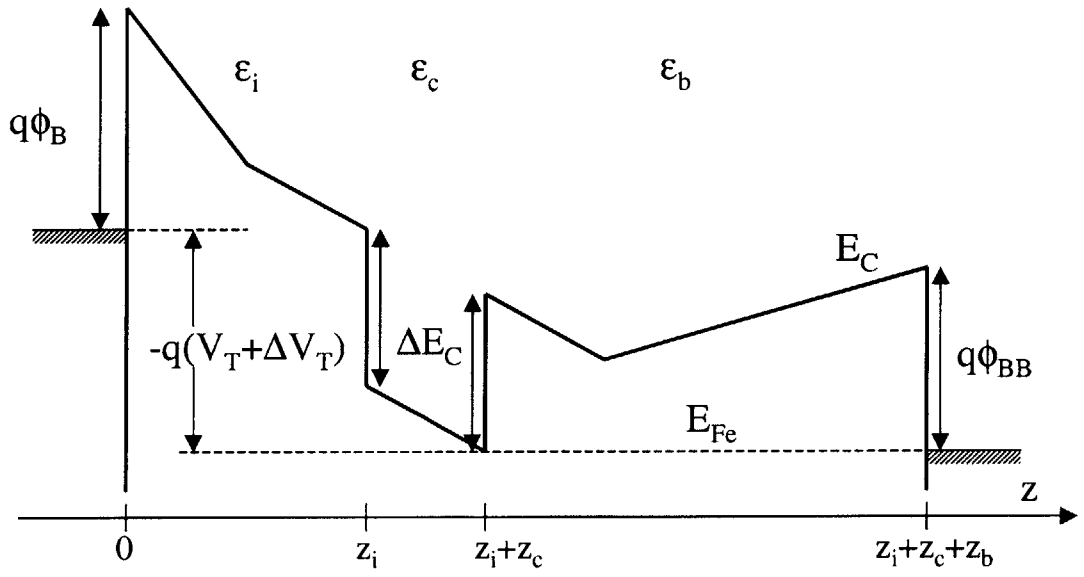

Fig. 2.8: Conduction energy band diagram at threshold at the center of the gate of a HEMT, perpendicular to the gate. The Fermi-level at the buffer-substrate interface is pinned.

This result suggests that in the absence of Fermi-level pinning below the channel, the threshold voltage shift only depends on the piezoelectric charge between the gate and the channel.

2.4.2 Fermi-level Pinned at Buffer-heterostructure Interface

If Fermi-level pinning at the buffer-substrate interface is assumed, which is a fair assumption in InP HEMTs grown by MBE [50] or OMVPE [51] and GaAs PHEMTs [52], the model needs to be modified. The corresponding energy band diagram can be seen in Fig. 2.8. In this case, equation [2.8] still holds, but there is an additional constraint imposed by pinning:

$$\Delta E_C = E_C(z_i + z_c) - E_C(z_i + z_c + z_b) + q\phi_B \qquad [2.15]$$

where z_b is the thickness of the buffer layer. We now apply equation [2.11] from $z_1=z_i+z_c$ to $z_2=0$, selecting $z_0=z_i+z_c+z_b$:

$$E_C(0)-E_C(z_i+z_c)=q\left[\varepsilon_b E(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)\right]\int_{z_i+z_c}^{0}\frac{dz}{\varepsilon(z)}$$

$$-q\int_{z_i+z_c}^{0}\frac{P_z(z)}{\varepsilon(z)}dz+q\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z)}\left(\int_{z_i+z_c+z_b}^{z}\rho(z)dz\right)dz \qquad [2.16]$$

Equation [2.11] is used between $z_1=z_i+z_c$ and $z_2=z_i+z_c+z_b$ and substituted in [2.15]:

$$E_C(z_i+z_c)-E_C(z_i+z_c+z_b)=q\left[\varepsilon_b E(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)\right]\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{dz}{\varepsilon(z)}$$

$$-q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{P_z(z)}{\varepsilon(z)}dz+q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{1}{\varepsilon(z)}\left(\int_{z_i+z_c+z_b}^{z}\rho(z)dz\right)dz=\Delta E_C-q\phi_B \qquad [2.17]$$

Solving for $\varepsilon_b E(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)$ in [2.17] shows:

$$\left[\varepsilon_b E(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)\right]=\frac{1}{q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{dz}{\varepsilon(z)}}\left[\Delta E_C-q\phi_{BB}+q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{P_z(z)}{\varepsilon(z)}dz-q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{1}{\varepsilon(z)}\left(\int_{z_i+z_c+z_b}^{z}\rho(z)dz\right)dz\right] \qquad [2.18]$$

plugging this value into [2.16] gets

$$E_C(0)-E_C(z_i+z_c)=\frac{\int_{z_i+z_c}^{0}\frac{dz}{\varepsilon(z)}}{\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{dz}{\varepsilon(z)}}\left[\Delta E_C-q\phi_{BB}+q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{P_z(z)}{\varepsilon(z)}dz-q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{1}{\varepsilon(z)}\left(\int_{z_i+z_c+z_b}^{z}\rho(z)dz\right)dz\right]\int_{z_i+z_c}^{0}\frac{dz}{\varepsilon(z)}$$

$$-q\int_{z_i+z_c}^{0}\frac{P_z(z)}{\varepsilon(z)}dz+q\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z)}\left(\int_{z_i+z_c+z_b}^{z}\rho(z)dz\right)dz \qquad [2.19]$$

Using equation [2.8] finally yields:

$$V_T + \Delta V_T = \phi_B - \frac{\Delta E_C}{q} - \int_{z_i+z_c}^{0} \frac{1}{\varepsilon(z)} \left(\int_{z_i+z_c+z_b}^{z} \rho(z)dz \right) dz + \int_{z_i+z_c}^{0} \frac{P_z(z)}{\varepsilon(z)} dz$$
$$- \frac{\int_{z_i+z_c}^{0} \frac{dz}{\varepsilon(z)}}{q \int_{z_i+z_c+z_b}^{z_i+z_c} \frac{dz}{\varepsilon(z)}} \left[\Delta E_C - q\phi_{BB} + q \int_{z_i+z_c+z_b}^{z_i+z_c} \frac{P_z(z)}{\varepsilon(z)} dz - q \int_{z_i+z_c+z_b}^{z_i+z_c} \frac{1}{\varepsilon(z)} \left(\int_{z_i+z_c+z_b}^{z} \rho(z)dz \right) dz \right] \quad [2.20]$$

Only two terms on the right hand side are dependent on the piezoelectric charge. They are responsible for the shift in V_T. Hence,

$$\Delta V_T = - \int_{0}^{z_i+z_c} \frac{P_z(z)}{\varepsilon(z)} dz + \frac{\int_{0}^{z_i+z_c} \frac{dz}{\varepsilon(z)}}{\int_{z_i+z_c}^{z_i+z_c+z_b} \frac{dz}{\varepsilon(z)}} \int_{z_i+z_c}^{z_i+z_c+z_b} \frac{P_z(z)}{\varepsilon(z)} dz \quad [2.21]$$

Or in simpler terms:

$$\Delta V_T = - \int_{0}^{z_i+z_c} \frac{P_z(z)}{\varepsilon(z)} dz + \frac{1}{z_b} \left(\frac{z_i}{\varepsilon_i} + \frac{z_c}{\varepsilon_c} \right) \int_{z_i+z_c}^{z_i+z_c+z_b} P_z(z)dz \quad [2.22]$$

When compared with equation [2.14] this equation shows an extra term. This term is induced by the charge that pins the Fermi level at the buffer-substrate interface. When Fermi-level pinning occurs far enough from the bottom of the channel, or with an unpinned substrate-buffer interface, this equation converges towards equation [2.14], as one would expect.

The displacement parallel to the length of the gate, u_x, increases moving away from the center of the gate to the edge of the gate. Therefore, according to equation [2.4], with a gate orientation parallel to [011], P_z mostly has a negative value underneath the center of the gate. Because of this it is simpler to focus on the behavior of $-P_z$, which is predominantly positive. Ignoring the differences in permittivity among the various layers, and with an average value $\langle\varepsilon\rangle$ for all of them, equation [2.22] can be rewritten as:

$$\Delta V_T \approx \frac{z_i + z_c}{\langle \varepsilon \rangle} \left[\langle -P_z \rangle_{ins+chan} - \langle -P_z \rangle_{buf} \right] \qquad [2.23]$$

This suggests that ΔV_T is roughly proportional to the *difference* between the average of $-P_z$ above the channel-buffer interface and the average of $-P_z$ in the buffer layer underneath the channel. In the absence of Fermi-level pinning at the buffer-substrate interface, only the first term matters. However in the more general case of Fermi-level pinning, all aspects of the heterostructure design are important, including the details of the buffer layer.

2.5. Modeling Results

The model presented in the previous section was used to study how the H-induced ΔV_T depends on several key parameters of the device design. First, the dependence on the gate length was investigated. Then, the influence of the gate structure and the heterostructure design were studies. Finally, the calculated H-induced V_T shifts in InP HEMTs are compared to those in GaAs PHEMTs.

2.5.1. Dependence on Gate Length

The model for ΔV_T requires $-P_z$ at the center of the gate. This is shown in Fig. 2.6 for a 1 μm InP HEMT and GaAs PHEMT under identical stress conditions. The discontinuities in $-P_z$ at the channel boundaries occur because of the change in the material constants at the two heterointerfaces. Since the mechanical stress decreases with increasing depth, $-P_z$ also decreases. With the same stress, GaAs PHEMTs have a slightly larger piezoelectric polarization than InP HEMTs. This is due to the larger material constants of the different active layers in GaAs PHEMTs with respect to InP HEMTs.

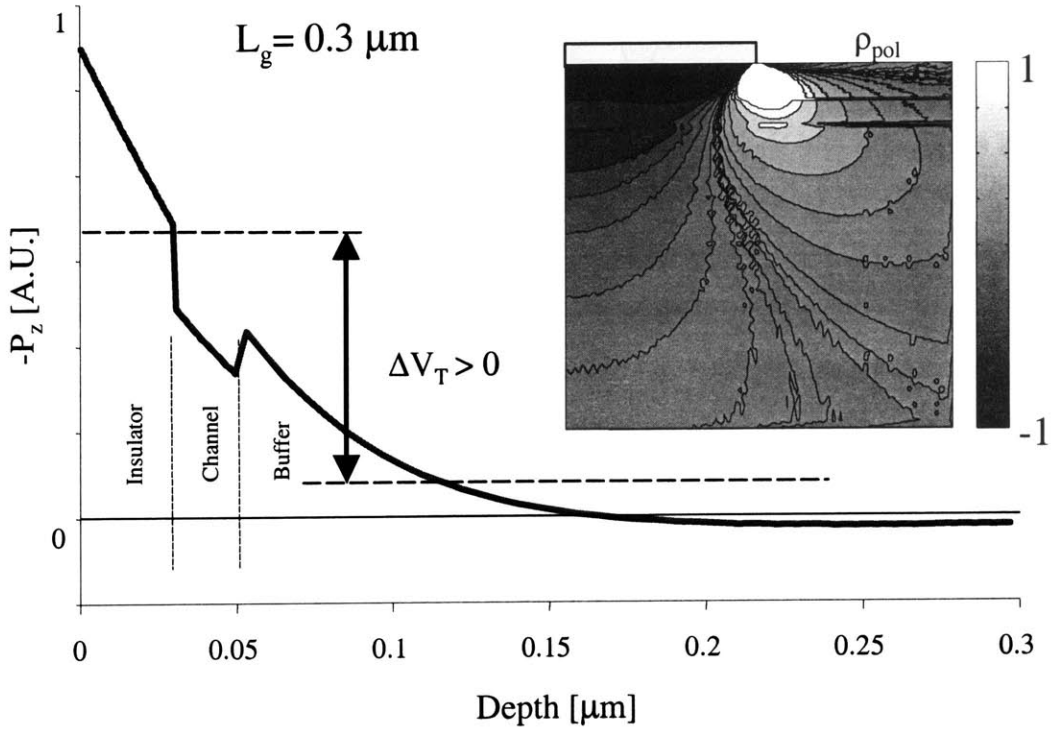

Fig. 2.9: Piezoelectric polarization vector in the direction perpendicular to the gate, $-P_z$, for an InP HEMT with 0.3 μm gate length. Inset shows the corresponding piezoelectric charge distribution.

The device gate length has a big impact on the piezoelectric charge distribution and the resulting P_z landscape. In the case of a short InP HEMT with a gate length of 0.3 μm, Fig. 2.9 shows the piezoelectric charge throughout the device structure (inset) and the resulting $-P_z$ directly underneath the center of the gate. The mechanical stress emanates from the edge of the gate and decreases with increasing distance from its origin. Because the gate length is short, the mechanical stress and the piezoelectric charge are large throughout the active device, in particular underneath the center of the gate. This causes $-P_z$ underneath the center of the gate to decrease sharply with depth. Therefore, the average of $-P_z$ above the bottom of the channel is significantly larger than the average of $-P_z$ below the channel, resulting in a *positive* and large threshold voltage shift. For very short devices the H-induced ΔV_T saturates with decreasing gate length. $-P_z$ decreases so fast with increasing depth, counteracting the increase of $-P_z$ at the gate-insulator interface.

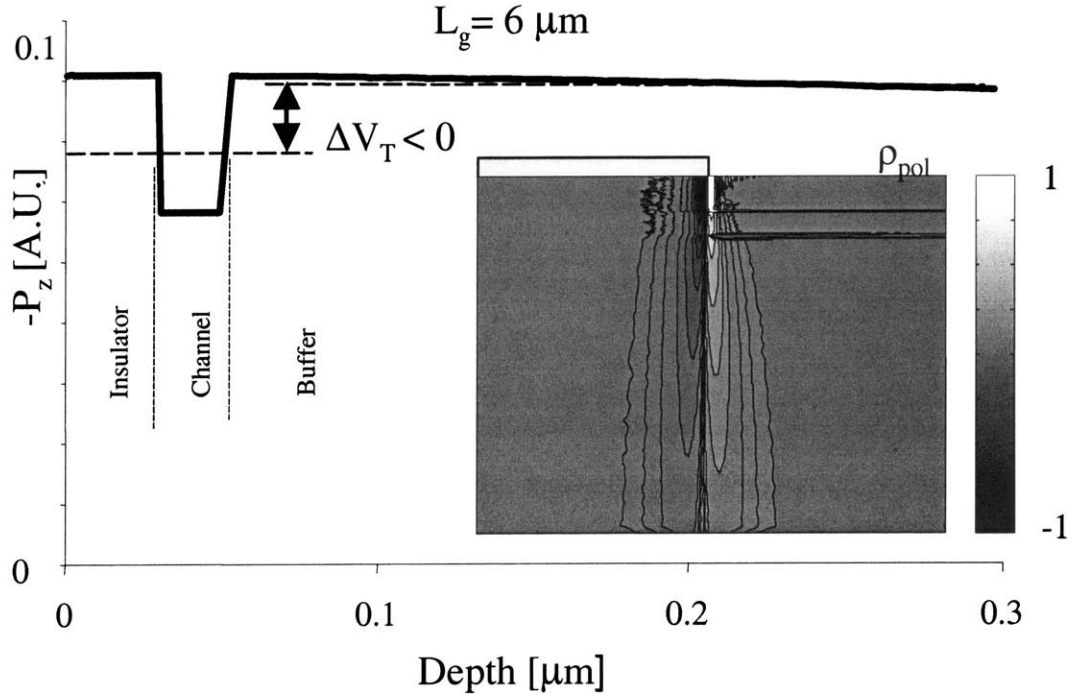

Fig. 2.10: Piezoelectric polarization vector in the direction perpendicular to the gate, $-P_z$, for an InP HEMT with 6 μm gate length. Inset shows the corresponding piezoelectric charge distribution.

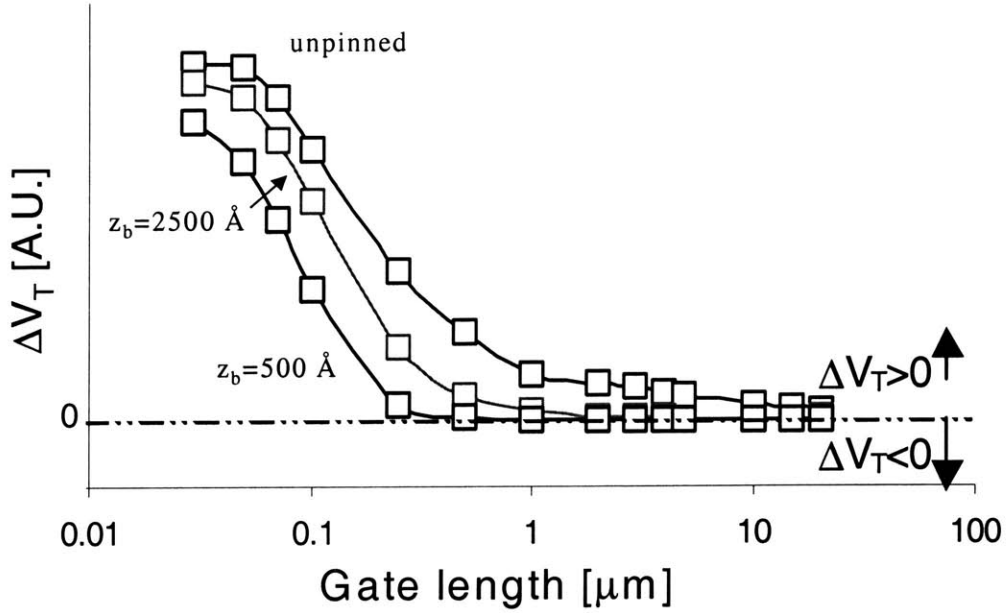

Fig. 2.11: Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths. The different lines are calculations for two different buffer layer thicknesses (with a pinned Fermi level at the buffer/substrate interface), as well as for an unpinned buffer/substrate interface.

In contrast, a long InP HEMT with a gate length of 6 μm (Fig. 2.10) exhibits a piezoelectric charge that is almost negligible underneath the center of the gate, far from the origin of the stress. At this location, $-P_z$ becomes smaller by an order of magnitude as compared to the 0.3 μm HEMT and is almost constant, except in the channel where it is lower because of the different material constants. This causes the average of $-P_z$ to be lower above the channel-buffer interface than below it, resulting in a small but *negative* threshold voltage shift.

Fig. 2.11 shows calculations of ΔV_T for InP HEMTs of different L_g. The evolution of ΔV_T with L_g is similar to the experimental observations summarized in Fig. 1.3. For long devices, a negative ΔV_T is found with a magnitude that increases as the gate length is shortened. For short devices, a positive ΔV_T occurs that increases as the gate length decreases.

2.5.2. Dependence on Heterostructure

Buffer thickness plays an important role in ΔV_T if the Fermi-level is pinned at the buffer-substrate interface, as can be seen in Fig. 2.11. Without Fermi-level pinning, ΔV_T is positive for all gate lengths and increases as the gate becomes shorter. With Fermi-level pinning, for thinner buffer layers, ΔV_T decreases and the gate length at which ΔV_T changes sign becomes shorter. As z_b decreases, $\langle -P_z \rangle$ in the buffer tends to increase, since $-P_z$ decreases with increasing depth, causing a negative shift in ΔV_T.

Other details of the layer structure also affect the overall magnitude of ΔV_T and the gate length at which ΔV_T changes sign. Looking at the depth profile of $-P_z$ in Fig. 2.6, the average of $-P_z$ in the insulator, $\langle -P_z \rangle_{ins}$, is higher than the average of $-P_z$ in the channel, $\langle -P_z \rangle_{chan}$. A thinner insulator layer causes the average of $-P_z$ above the channel-buffer interface, $\langle -P_z \rangle_{ins+chan}$, to decrease relative to the average of $-P_z$ below the channel, $\langle -P_z \rangle_{buf}$, because the contribution of $\langle -P_z \rangle_{chan}$ to $\langle -P_z \rangle_{ins+chan}$ becomes more significant. Hence, ΔV_T becomes more negative and it changes sign at shorter gate lengths (Fig. 2.12). Increasing the thickness of the channel has the same effect on ΔV_T.

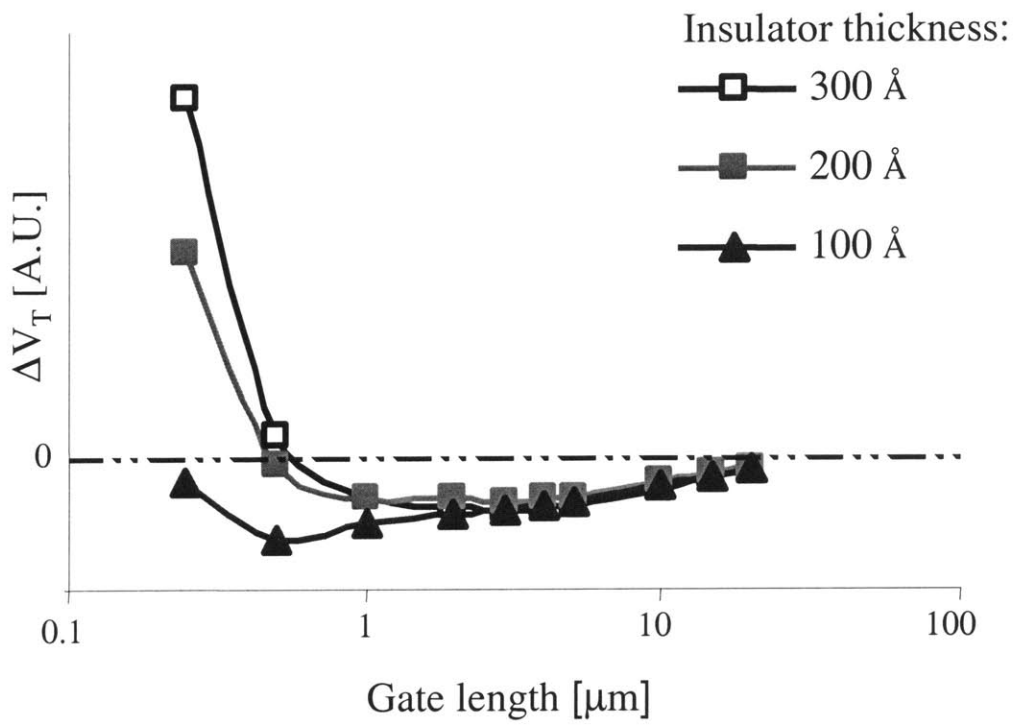

Fig. 2.12: Relative hydrogen-induced ΔV_T for InP HEMTs with insulator thicknesses of 100, 200 and 300 Å. The Fermi-level is pinned 500 Å below the channel.

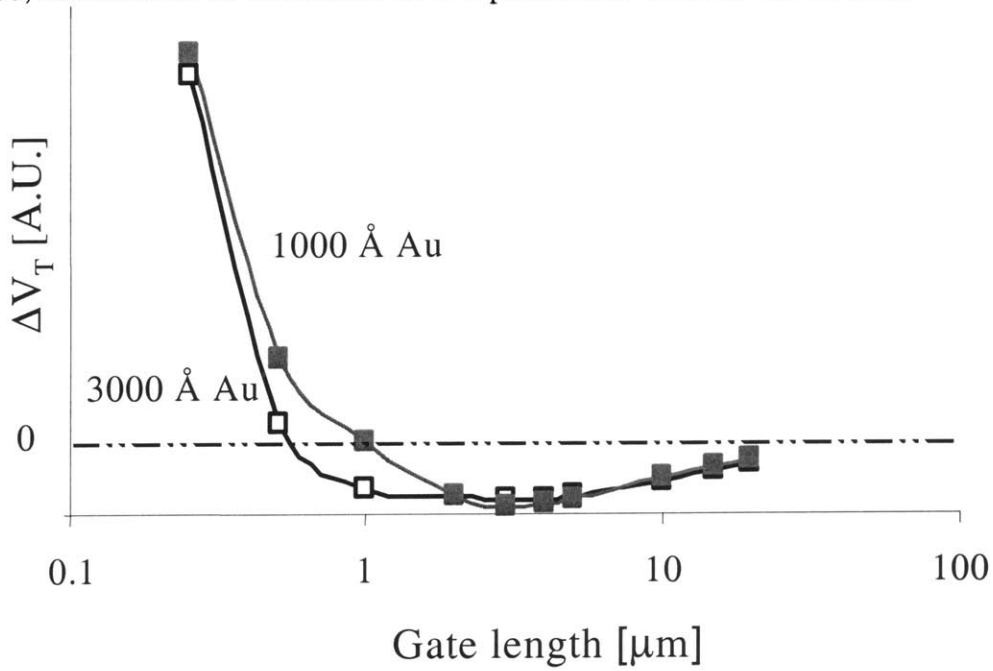

Fig. 2.13: Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths with an Au thickness of 1000 Å and 3000 Å. The Fermi-level is pinned 500 Å below the channel.

2.5.3. Dependence on Gate Stack

The design of the gate stack affects ΔV_T greatly. Increasing the rigidity of the gate material above the expanding Ti layer, for example, by increasing the thickness of these layers increases or selecting materials with a higher Young's, causes these layers to absorb more of the stress caused by the expanding TiH_x. This decreases the stress in the heterostructure underneath, resulting in a lower ΔV_T for short gate lengths and a change in sign at a shorter gate length. Fig. 2.13 shows that when the thickness of the Au layer in the gate increases from 1000 Å to 3000 Å, the rigidity of the gate increases and ΔV_T decreases for short gate lengths. Chapter 3 discusses a second method of increasing the rigidity of the gate by inserting a thick WSiN layer underneath the expanding Ti layer, which reduces the mechanical stress in the semiconductor.

On the other hand, lowering the rigidity of the gate increases ΔV_T and causes the sign-change to occur at longer gate length. In fact any decrease in the rigidity of the mechanical device structure has this effect on the H-induced ΔV_T. By removing the silicon nitride layer in our simulations, the stress in the heterostructure increases and at shorter gate lengths, ΔV_T increases significantly (Fig. 2.14). Nitride adds rigidity to the device structure.

A thicker expanding Ti layer induces more stress and greater polarization charge in the underlying semiconductor, as long as the Ti layer expands homogeneously. This increases ΔV_T and causes ΔV_T to change sign at longer gate length. Chapter 4 discusses the effect of a thick Ti layer in the gate stack on the H-induced piezoelectric effect.

2.5.4. Differences between InP HEMTs and GaAs PHEMTs

The experimental observations of the H-induced ΔV_T showed that GaAs PHEMTs showed larger shifts than InP HEMTs at short gate lengths that increased as the devices shortened (Fig. 1.3).

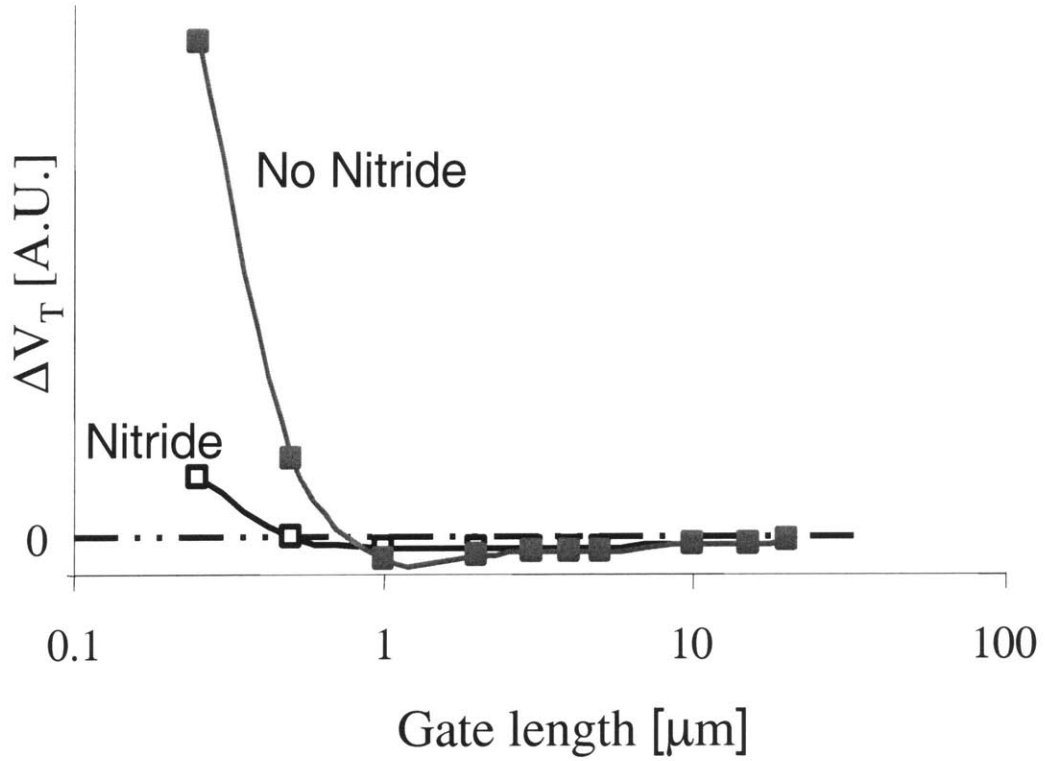

Fig. 2.14: Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths, with and without silicon nitride covering the gate. The Fermi-level is pinned 500 Å below the channel.

The only difference between InP HEMTs and GaAs PHEMTs is the magnitude of the material constants. As a consequence, similar conclusions about the dependence of the H-induced ΔV_T on different device design parameters can be made for GaAs PHEMTs. This is seen on Fig. 2.15, which shows the H-induced threshold voltage shift for GaAs PHEMTs and InP HEMTS of different gate lengths. For identical conditions, it is found that GaAs PHEMTs show a larger ΔV_T than InP HEMTs, but otherwise similar behavior. This is consistent with the experimental observations of Fig. 1.3, where the GaAs PHEMTs showed larger H-induced ΔV_T.

2.6. Reducing the H-induced Piezoelectric Effect

The results obtained in this chapter suggest that the H-induced piezoelectric effect in III-V HEMTs can be mitigated through the design of the gate stack and the

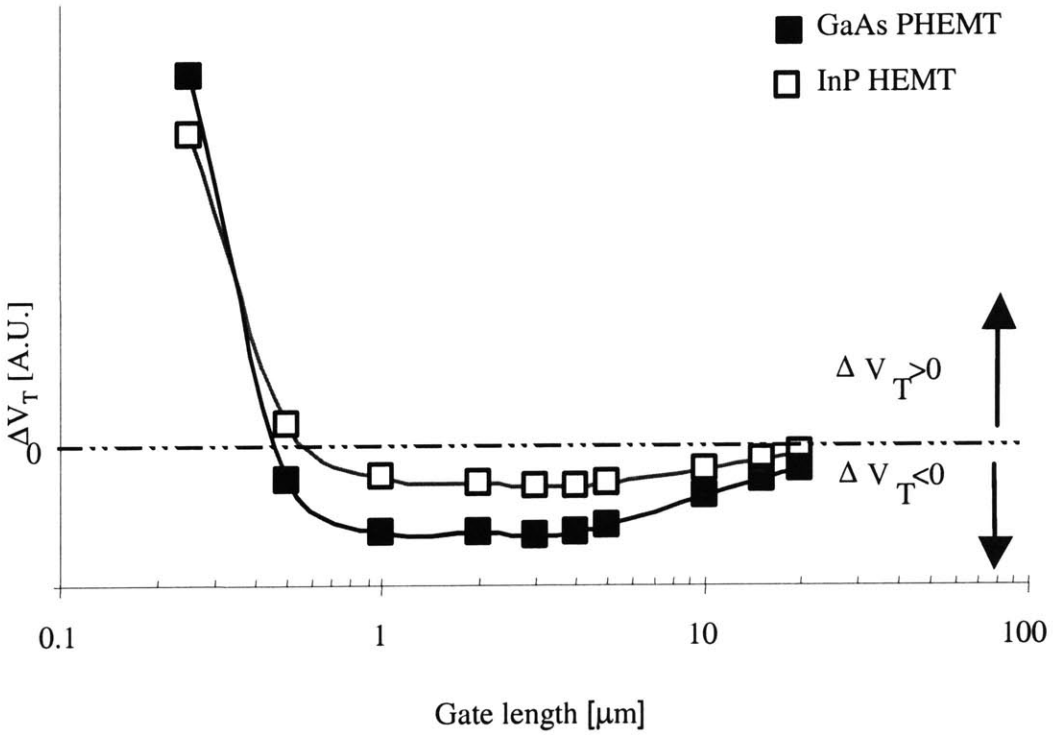

Fig.2.15: Relative hydrogen-induced ΔV_T for InP HEMTs and GaAs PHEMTs of different gate lengths. The different lines are calculations for the Fermi level pinned at 500 Å below the channel.

heterostructure of the device. Changing the gate orientation to [010] would, according to this model, eliminate any H-induced piezoelectric ΔV_T. Blanchard showed this experimentally [35]. This solution is not viable for technological reasons, mainly associated with the sidewall orientation that results after chemical etching [53].

The gate-stack can be redesigned to minimize the stress in the device hetero-structure. Thinning the Ti-layer, which reduces the magnitude of the stress, or adding layers on top of the Ti layer, which absorb stress, should accomplish this. Any measure that increases the rigidity of the gate structure decreases ΔV_T. Separating the Ti layer from the semiconductor structure should also diminish ΔV_T significantly, because the stress is most important immediately underneath the Ti layer. This approach is further discussed in Chapter 3.

The H-induced piezoelectric effect can also be mitigated by engineering the heterostructure. This is not always a viable solution, since the active layers set the performance of the HEMT. Increasing the thickness of the channel compared to the

thickness of the insulator decreases ΔV_T, because of the lower polarization in the channel. Thinning the buffer layer and setting the point where Fermi-level pinning takes place closer to the channel-buffer interface also reduces ΔV_T.

2.7. Summary

This chapter has presented a model for the impact of the hydrogen-induced piezoelectric effect on the threshold voltage of InP HEMTs and GaAs PHEMTs. 2D finite element simulations were used to calculate the mechanical stress caused by a Ti-containing metal gate that has expanded due to hydrogen absorption. The 2D piezoelectric charge distribution was calculated in the semiconductor heterostructure. A simple 1D electrostatics model was used to calculate the impact of this piezoelectric polarization charge on the threshold voltage. The model explained experimental observations of the gate length dependence of the hydrogen-induced threshold voltage shifts, both in InP HEMTS and in GaAs PHEMTs. The impact of several parameters of the device design were also studied. This suggested ways to mitigate the hydrogen sensitivity of these devices, by reducing the mechanical stress in the semiconductor through gate design and reducing the impact of the piezoelectric charge through design of the active layer structure.

Chapter 3

Hydrogen Sensitivity of Advanced InP HEMTs with WSiN-based Gate Stack

3.1. Motivation

Conventional InP HEMTs with a Ti/Pt/Au gate stack show a significant sensitivity to H. Chapter 2 presented a model for the H-induced ΔV_T and how different design parameters influence it. It was found that the H-induced ΔV_T highly depends on both the heterostructure and the gate structure. This chapter presents the experimental and modeling results for state-of-the-art InP HEMTs with a WSiN/Ti/Pt/Au gate. Because the expanding Ti layer is the source of the stress, the introduction of WSiN at the bottom of the gate stack is expected to mitigate H sensitivity by separating the Ti-layer from the heterostructure. An advanced HEMT heterostructure is also significantly thinner than the conventional devices that were studied earlier [37]. The advanced devices feature an InP etch stop in the insulator which has a lower piezoelectric constant. These features help mitigate the H reliability problem. Some of the results of this chapter have been published in [54].

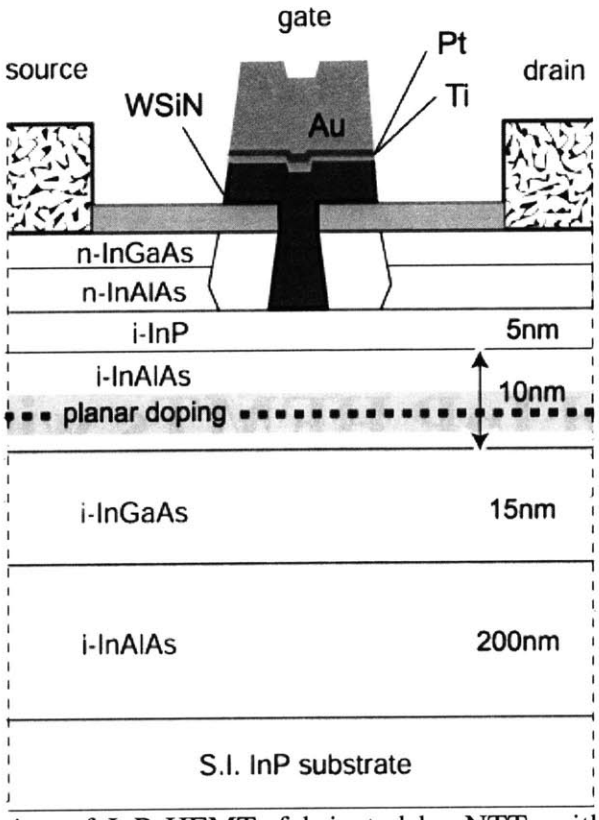

Fig. 3.1: Cross-section of InP HEMT, fabricated by NTT, with a WSiN/Ti/Pt/Au gate stack and an advanced thin heterostructure that features an InP etch-stop layer [55, 56].

3.2. ΔV_T Measurements

A cross-section of the investigated InP HEMTs is shown in Fig. 3.1. In contrast with conventional InP HEMTs, these devices, which are fabricated by NTT, feature a WSiN/Ti/Pt/Au gate stack and an InP gate recess etch-stop layer in the intrinsic heterostructure [55]. The active device structure consists of a 2000 Å InAlAs buffer, a 150 Å InGaAs channel, a 100 Å InAlAs insulator and a 60 Å InP etch stop [56]. The thickness of the WSiN layer is 1000 Å thick.

The H sensitivity of these devices was studied following a methodology similar to that of [35]. The experiments consist of three phases. First, the devices were baked in N_2 at 195°C for over 60 hours to saturate all thermally induced degradation. In a second phase, the thermal stability was evaluated by baking the devices again at 195°C

for 2 h under N_2. Finally, the devices are baked again at 195°C for 2h [35] in forming gas (5 % H_2/95 % N_2). It is in this step where hydrogen degradation took place.

This methodology allowed us to compare the effects of a 2-hour thermal bake in N_2 and H_2, and thus estimate the H effects in a single device. In separate experiments, a few devices were monitored in-situ during the N_2 and H_2 anneals. V_T was measured at regular intervals at 195°C. In some cases, after the forming gas bake, the effect of a 2h recovery anneal in N_2 was evaluated at 200°C.

Device characterization was carried out at room temperature before and after every phase. For this purpose, a rather "benign" device characterization test suite was developed that would not affect the device characteristics. This characterization suite involved measurements of the parasitic resistances, the output, transfer and subthreshold characteristics, and the threshold voltage. The measurements and extraction of the figures of merit were controlled by a PC and used a fixed planar probe configuration. Emphasis was placed on the threshold voltage which is defined at V_{DS}=0.1 V and I_D=1 mA/mm above leakage.

The studied devices had gate lengths between 30 nm and 1 μm [55]. The HEMTs were designed and optimized for the [01$\bar{1}$] gate orientation, but devices along the [011] direction were also available. Fig. 3.2 shows the transfer characteristics in the linear regime of a 0.1 μm transistor with a [01$\bar{1}$] orientation after 60 h pre-bake in N_2 at 195°C and after subsequent 2 h bakes in N_2 or H_2 at 195°C. The additional 2 h bake in N_2 did not affect the device. This confirmed that the 60 h prebake in N_2 was enough to exhaust all thermal effects. In contrast, the effect of H exposure is mainly a negative shift in V_T. A recovery bake for 2h in N_2 at 195°C did not shift V_T back.

Fig. 3.3 shows the time evolution of V_T for a 0.1 μm InP HEMT with a [01$\bar{1}$] gate orientation in-situ during N_2 anneal, H_2 exposure and N_2 recovery. Before these anneals, the devices were prebaked in N_2 for 60 h at 195°C. The time evolution shows that V_T shifted negatively during the forming gas anneal, while it was largely unaffected by the

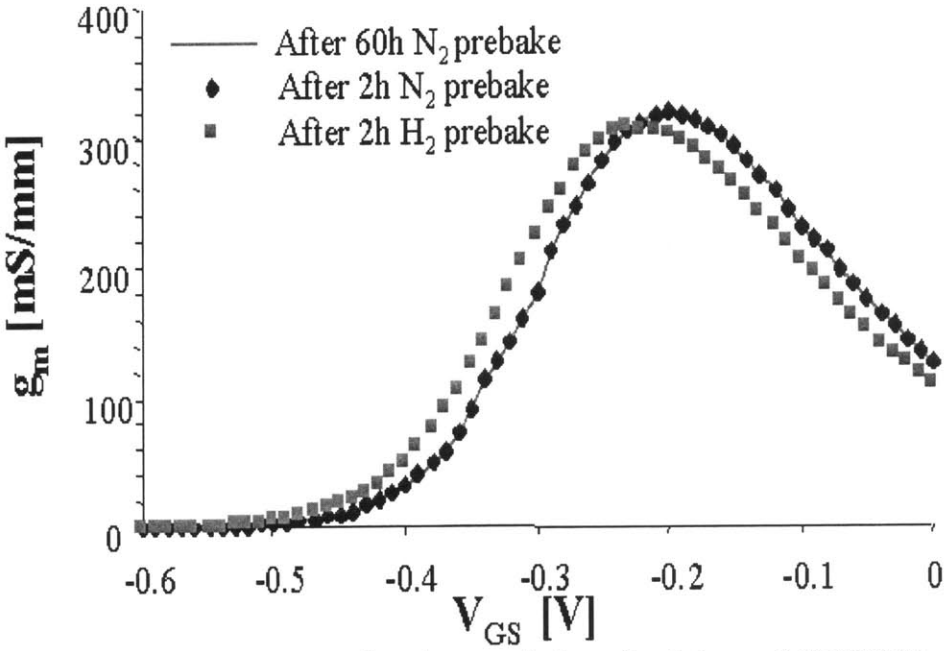

Fig. 3.2: Room-temperature transfer characteristics of a 0.1 μm InP HEMT with a [01$\bar{1}$] gate orientation after 60 h prebake in N_2 at 195 °C, after a subsequent 2 h bake in N_2 at 195 °C and after another 2 h bake in forming gas (5 % H_2/95 % N_2) at 195 °C (V_{DS}=0.1 V).

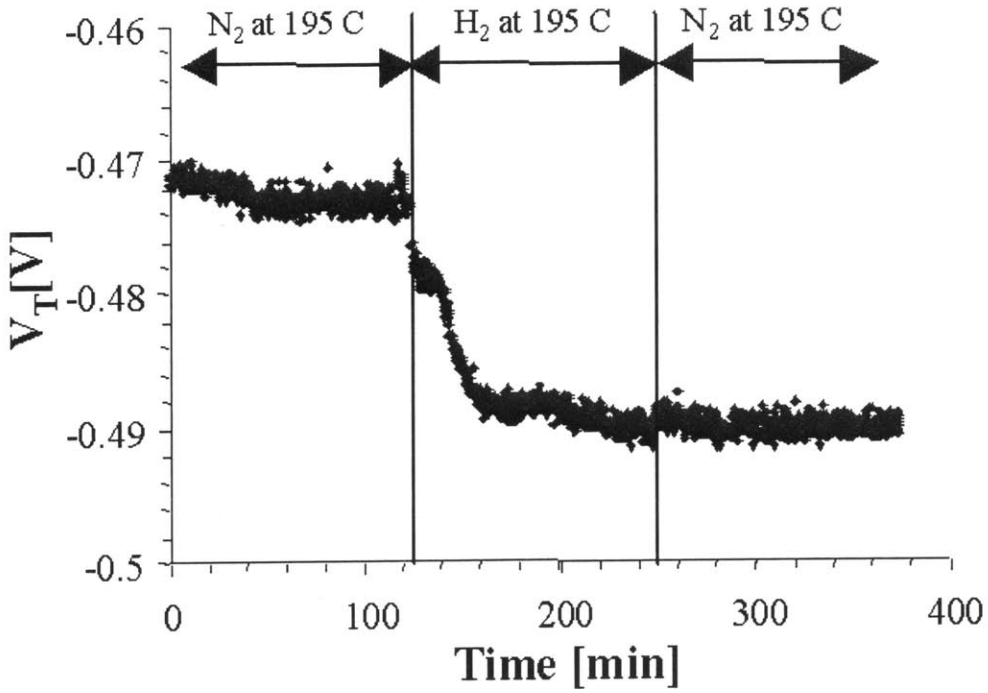

Fig. 3.3: Time evolution of V_T during a typical experiment (T=195 °C), the HEMT was after a prebake in N_2 at 195°C, consecutively baked at 195 °C in N_2 for 2h, in N_2/H_2 for 2h and in N_2 again for 2h. The device has a 0.1 μm gate length and a [01$\bar{1}$] gate orientation.

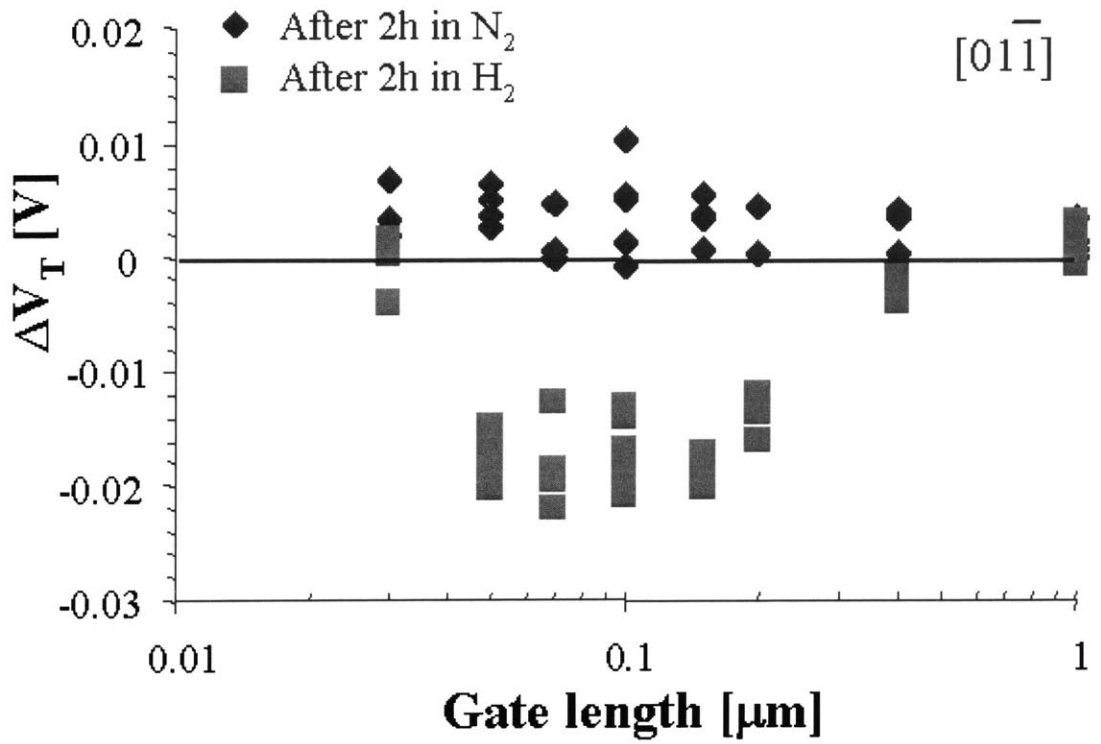

Fig. 3.4:Threshold voltage shifts caused by a 2h bake at 195°C in N_2 and in forming gas (5% H_2/95% N_2) as a function of gate length. The devices have a [01$\bar{1}$] gate orientation.

bakes in a N_2 atmosphere at the same temperature. Also, the impact of H_2 saturated after about 50 minutes of exposure to forming gas. Furthermore, there is no indication of any recovery in a post-H exposure N_2 anneal. All devices behaved this way under these conditions.

For HEMTs with an [01$\bar{1}$] gate orientation, Fig. 3.4 shows ΔV_T as a function of the gate length. The 2h N_2 treatment at 195°C seemed to shift V_T slightly positive. In contrast, the equivalent H_2 treatment caused a distinct and statistically significant negative ΔV_T, which was largest in magnitude for the 0.1 μm devices. This is the first detailed study of the gate length dependence of the H-induced ΔV_T in advanced InP HEMTs. Fig. 3.5 shows ΔV_T in devices with an [011] gate orientation under identical conditions. Here, N_2 treatment also caused a small ΔV_T. The H_2 bake caused a negative shift with a gate length dependence that was almost a mirror image of that of Fig. 3.4, except that it was shifted by about –10 mV.

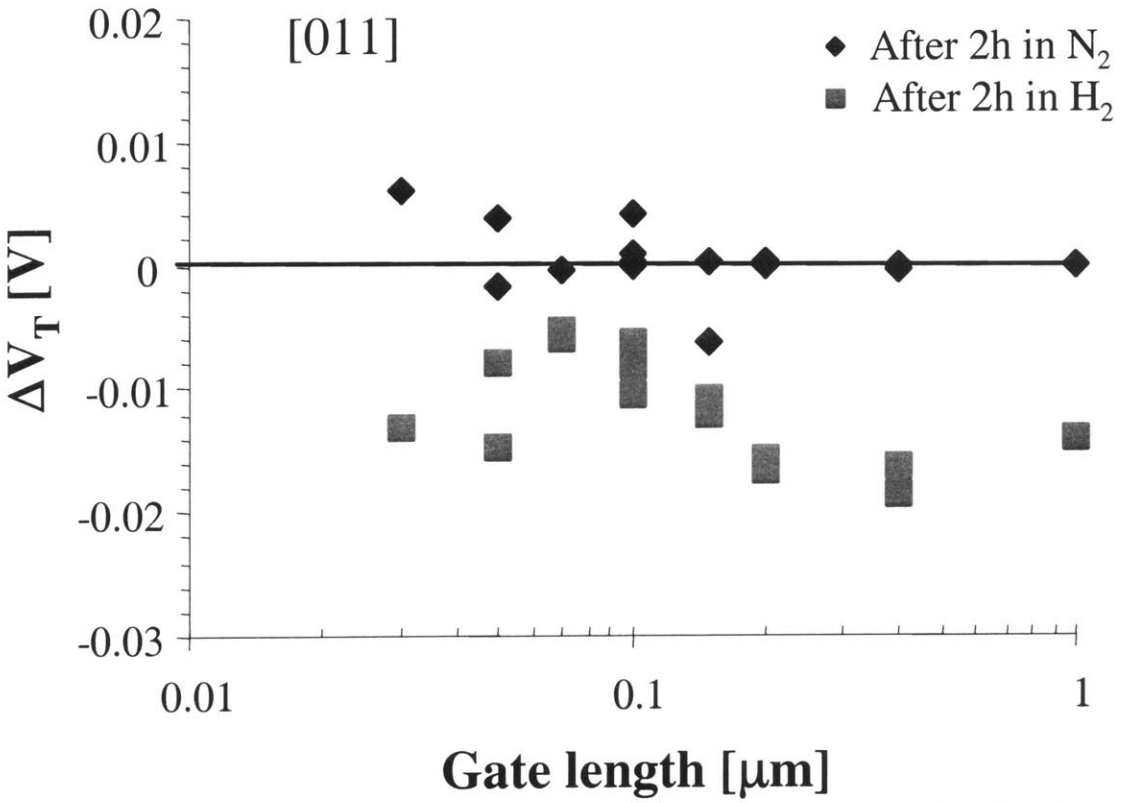

Fig. 3.5: Threshold voltage shifts caused by a bake at 195°C in N_2 and in forming gas (5% H_2) . The devices have a [011] gate orientation.

The maximum value of ΔV_T for short gate length devices that was observed in any gate orientation was in the order of 15 to 20 mV, an order of magnitude smaller than previous observations on InP HEMTs of this gate length under similar condition [31, 33, 34, 35, 36], which are plotted on Fig. 1.3. These are important and promising results, as they experimentally show small H-induced V_T shifts for very short devices.

3.3. Stress Measurements

The effect of the WSiN layer on the stress caused by the expanding TiH_x layer in the WSiN/Ti/Pt gate stack was examined using radius-of-curvature measurements. Si wafers coated with a 1500Å Si_3N_4/250Å Ti/250Å Pt stack and with a 1500Å Si_3N_4/4000Å WSiN/250Å Ti/250Å Pt stack were studied using a Tencor FLX-2320, with a laser operating at 670 nm. The temperature and environment were changed during the

measurement, enabling in-situ measurements of the stress during exposure to forming gas.

The stress in the film was first measured during a bake in N_2. After reaching thermal equilibrium, the environment was changed to forming gas (5% H_2/95% N_2) and the stress was monitored. The radius-of-curvature measurements quantify the stress caused by the expanding films on the whole wafer. The extra rigidity provided by 4000 Å of WSiN is negligible compared to the whole Si wafer. There was no significant statistical difference between the H-induced stress in the wafer with 4000 Å of WSiN underneath the Ti layer or without. This suggests there is no reaction between the WSiN and the hydrogen, which expands or shrinks WSiN.

3.4. Modeling Results

To understand the gate length dependence and the magnitude of the observed H-induced ΔV_T, device simulations were carried out using the model described in Chapter 2. 2D finite element simulations were performed using ABAQUS and 1D electrostatics calculations were made using MATLAB. For comparison with the results of Chapter 2, a "reference" device with a standard Ti/Pt/Au gate stack and a layer structure consisting of 2500 Å InAlAs/300 Å InGaAs/ 200 Å InAlAs (from bottom to top) [43] was simulated. Then, the impact of thinning the heterostructure down to a layer structure consisting of 2000 Å InAlAs/150 Å InGaAs/ 160 Å InAlAs was studied. This layer structure is referred to as the "thinner heterostructure". The effect of introducing an InP etchstop underneath the gate using a layer structure consisting of 2000 Å InAlAs/150 Å InGaAs/ 100 Å InAlAs/ 60 Å InP (from bottom to top) [56] was investigated. This layer structure is referred to as "improved heterostructure". Subsequently, a thick WSiN layer was added at the bottom of the gate stack. The results of these simulations are shown in Fig. 3.6 for an [011] gate orientation. Identical results are predicted for the [01$\bar{1}$] gate orientation, except for an opposite sign in ΔV_T. These results are analyzed in the next two subsections.

3.4.1. Influence of Heterostructure

As Fig. 3.6 shows, thinning the reference device down to the thinner heterostructure reduced ΔV_T by about 20 %. As the model of Chapter 2 suggested, the threshold voltage shift is, to the first order proportional to the combined thickness of the insulator and channel, z_i+z_c, and to the difference between the average piezoelectric field above the channel-buffer interface and below it, $<P_z>$. Thinning z_i+z_c slightly increases $<P_z>$, but the product of z_i+z_c and $<P_z>$ still decreases, except for gate lengths where $<P_z>$ is near zero. Thinning down the insulator and channel layer decreases ΔV_T, but the decrease is less than proportionally. Thinning the buffer layer also decreases ΔV_T, which is shown in Fig. 2.8. Generally, thinning the heterostructure lowers ΔV_T.

Introduction of the 60 Å InP etch-stop layer, which has a very low piezoelectric constant, reduced ΔV_T by another 35 %. This caused a decrease of the average piezoelectric field in the channel and the insulator. With these two changes the improved heterostructure exhibited decreased H-sensitivity by more than 50 % at short gate lengths when compared with the reference device.

3.4.2. Influence of Gate Structure

The presence of the thick WSiN layer in the gate stack further lowered the H-sensitivity by about a factor of 3 at a gate length of 0.1 μm and even more at shorter gate lengths (Fig. 3.6). According to the simulations, the WSiN layer absorbed a large part of the stress induced by the expanding Ti layer, resulting in a reduction of the mechanical stress in the semiconductor. This caused a proportional reduction of the piezoelectric polarization, and thus, in ΔV_T. The simulations showed that a thicker WSiN layer further reduced ΔV_T more. This can be seen in Fig. 3.7, which shows the calculated ΔV_T in function of the gate length, for WSiN thicknesses of 0 Å, 100 Å, 500 Å and 1000 Å.

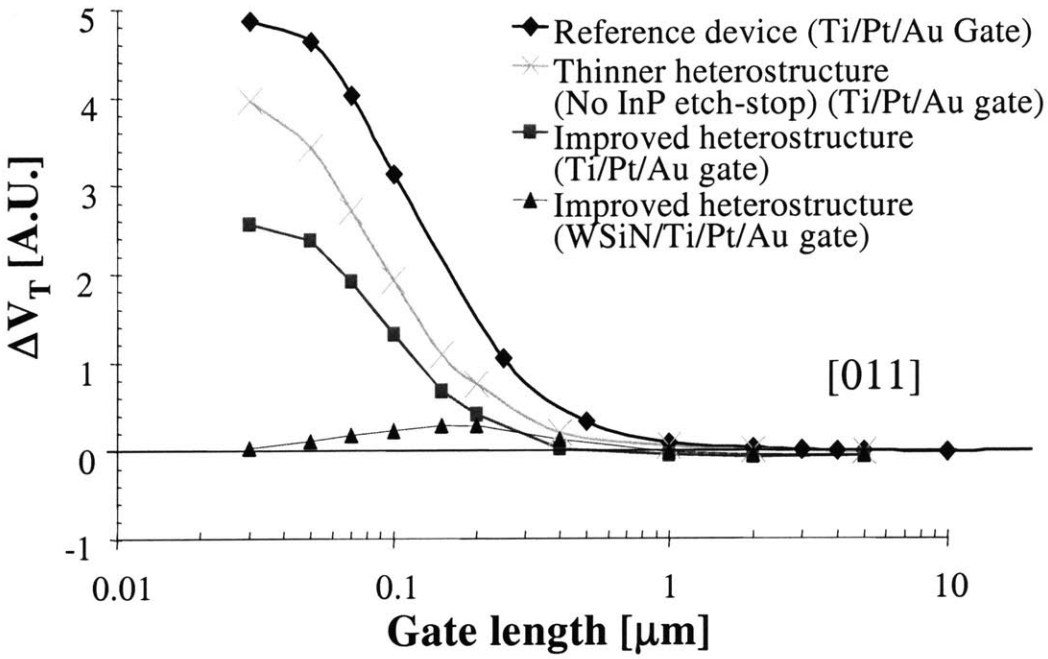

Fig. 3.6: Calculated ΔV_T vs. gate length for: 1) reference structure with Ti/Pt/Au gate; 2) thinned heterostructure with Ti/Pt/Au gate, 3) improved heterostructure (including InP etch stop layer) with a Ti/Pt/Au gate, and 4) improved heterostructure with a WSiN/Ti/Pt/Au gate. Gate orientation is [011].

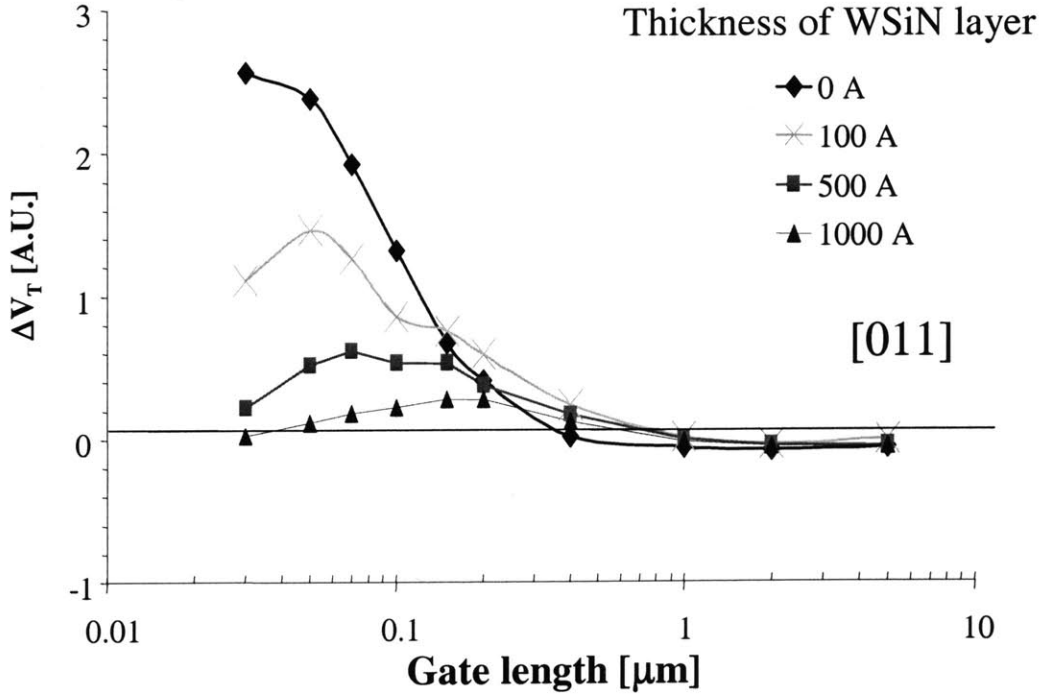

Fig. 3.7: Calculated ΔV_T vs. gate length for InP HEMTs with the improved heterostructure with a WSiN/Ti/Pt/Au gate for different thicknesses of the WSiN layer (0 Å, 100 Å, 500 Å and 1000 Å). Gate orientation is [011].

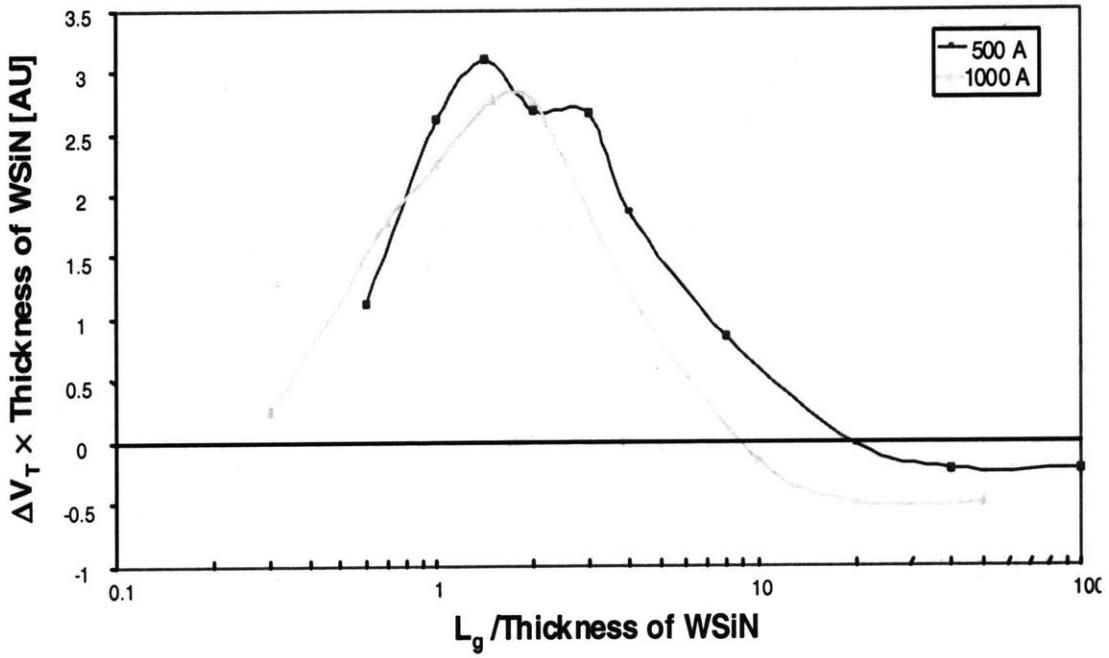

Fig. 3.8: Calculated ΔV_T times the thickness of WSiN vs. the ratio of gate length to WSiN thickness for InP HEMTs with the improved heterostructure with a WSiN/Ti/Pt/Au gate for different thicknesses of the WSiN layer (500 Å and 1000 Å). Gate orientation is [011].

Devices with a WSiN/Ti/Pt/Au gate show a maximum ΔV_T for a certain gate length. The peak ΔV_T occurs at a longer L_g for thicker WSiN because the ratio of the gate length to the thickness of the WSiN, t_{WSiN}, affects ΔV_T. In the case of $L_g/t_{WSiN}<1$, when L_g/t_{WSiN} decreases, the geometry causes the mechanical stress to decrease in the semiconductor, and thus, ΔV_T to decrease. The mechanical stress dissipates with increasing depth from the expanding gate at a rate which is proportional to L_g. This can be seen on Fig. 3.8, which shows the calculated ΔV_T scaled by t_{WSiN} vs. the ratio of L_g to t_{WSiN}, with t_{WSiN} equal to 500 Å and 1000 Å. Fig. 2.6 shows that in short devices, the piezoelectric field decreases rapidly with depth in the semiconductor. For short devices, ΔV_T is on the first order proportional to the piezoelectric field, induced by the stress, at the top of the insulator. As the WSiN layer thickens, the stress in the semiconductor decreases proportionately, and so does ΔV_T. The scaling rules behind this reduction in the H-induced ΔV_T are further discussed in Chapter 5.

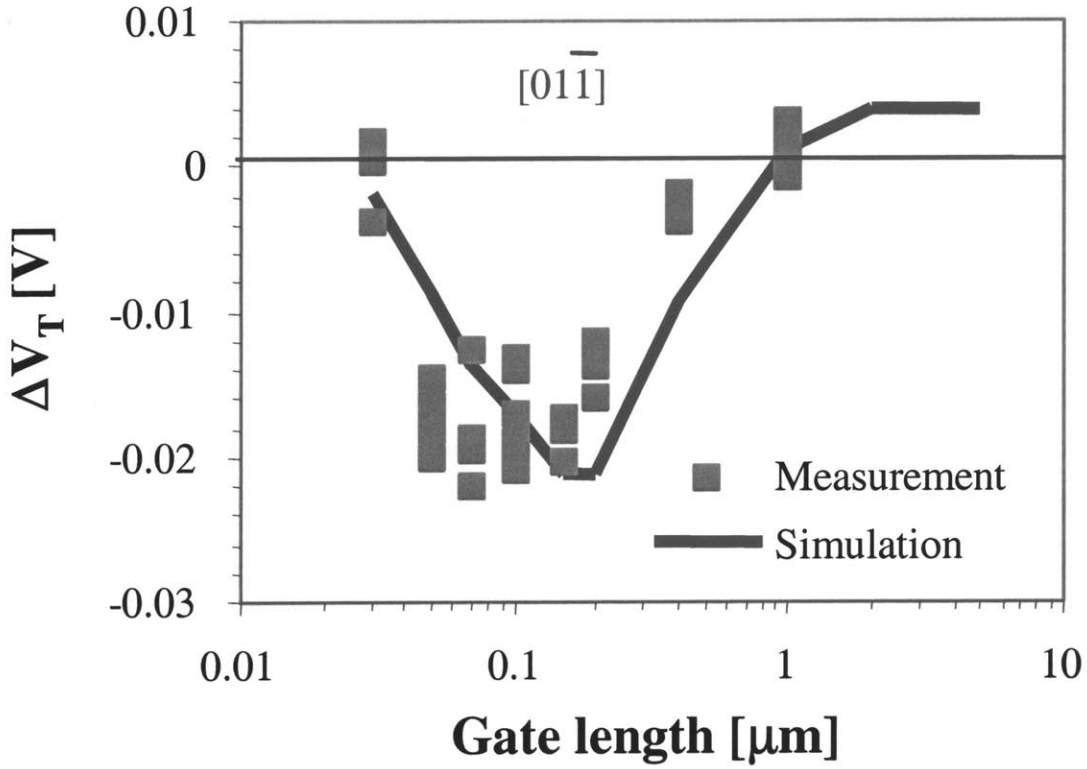

Fig. 3.9: Measured and simulated ΔV_T for the improved InP HEMTs with a WSiN-based gate stack and InP etch-stopper. Gate orientation is [01$\bar{1}$].

Devices with a high L_g/t_{WSiN} show a decreasing ΔV_T as L_g/t_{WSiN} increases. In this case, the piezoelectric field slowly declines with depth in the semiconductor. ΔV_T is very small and sensitive to the details of both gate and device structure, and is no longer inversely proportional to t_{WSiN}.

The combined effect of the thinned heterostructure, the presence of the low piezoelectric material above the bottom of the channel and the thick WSiN underneath the Ti layer is a reduction of ΔV_T by an order of magnitude. The overall reduction of mechanical stress causes an overall reduction of the polarization and ΔV_T in the semiconductor.

3.5. Comparison of model with experiments

The simulated results shown in Fig. 3.6 for the advanced heterostructure with a WSiN gate can be compared to the experimental data. This requires appropriate scaling because the simulated ΔV_T scale linearly with the amount of stress used in the model and the actual stress introduced by the expanding gate is unknown. The comparison is shown in Fig. 3.9 where excellent agreement is found for the [01$\bar{1}$] gate orientation. Interestingly, the simulations not only predict a large and negative ΔV_T centered around 0.1 μm, but also a marked H insensitivity for 30 nm devices, as observed in the experiments. In very short devices, the gate length is shorter than the thickness of the WSiN layer, dramatically reducing the mechanical stress at the center of the gate.

By comparing Figs. 3.4 and 3.5 one sees that the shapes of the ΔV_T curves for the [011] and [01$\bar{1}$] gate orientations are not exactly a mirror image of each another around the x-axis, which is what the H-induced piezoelectric effect predicts. There appears to be a rigid shift of about −10 mV in ΔV_T for the devices with a [011] gate orientation. The origin of this difference is unknown, but could be related to the fabrication process, which has been optimized for the [01$\bar{1}$] gate orientation. For [011] oriented devices, other aspects of the fabricated device come into play that are not captured in the simulations.

These results are encouraging and important because they represent a device level solution to the reliability problems caused by the H-induced piezoelectric effect. Designing a device with a WSiN/Ti/Pt/Au gate should mitigate this problem without requiring hermetic packaging provided with hydrogen getterers.

3.6. Summary

InP HEMT designs with a WSiN layer at the bottom of the gate stack and InP etch-stop layers inside the thinner intrinsic heterostructure feature a hydrogen sensitivity that is about one order of magnitude smaller than conventional InP HEMTs. Thinning the heterostructure reduces the effect of the piezoelectric polarization on V_T proportionally to the thickness of the channel and insulator. Using a material with a low piezoelectric constant, such as InP, above the bottom of the channel reduces the piezoelectric polarization there and thus ΔV_T. The mechanical stress in the semiconductor is reduced significantly because the expanding Ti layer is removed from the semiconductor by the

non-expanding WSiN layer. This reduces the piezoelectric charge and the H-induced ΔV_T. This means the H-induced piezoelectric effect can be mitigated by a suitable gate stack design.

The following chapter discusses the effect of a very thick Ti layer in the gate stack. The model predicts an increased ΔV_T if the full Ti layer expands. Surprisingly, small H-induced ΔV_T were experimentally observed. Only the top layer of the Ti expands and the non-expanding Ti layer has a similar effect on the H-induced ΔV_T as the WSiN layer.

Chapter 4

Hydrogen sensitivity of InP HEMTs with a thick Ti-layer in the Ti/Pt/Au gate stack

4.1. Motivation

The model for the H-induced piezoelectric effect presented in Chapter 2, implies that devices with a thick Ti layer should exhibit a large V_T shift. The H-induced ΔV_T is proportional to the stress in the semiconductor and a thicker expanding Ti layer increases the mechanical stress in the heterostructure. This suggests the H-sensitivity can be mitigated by thinning the Ti layer. To verify this, the H sensitivity of InP HEMTs with a thick Ti layer in the gate stack was studied. Surprisingly, the experimentally observed piezoelectric H-sensitivity of these devices was very low. It was nearly as low as that of the devices with WSiN in the gate stack, which were presented in Chapter 3. This is an important finding because it implies that the H sensitivity of Ti/Pt/Au-gate HEMTs can be improved significantly without requiring drastic process changes. A second H-induced degradation mechanism was identified that was likely related to an undesirable processing issue. Some of the results of this chapter have been published in [57].

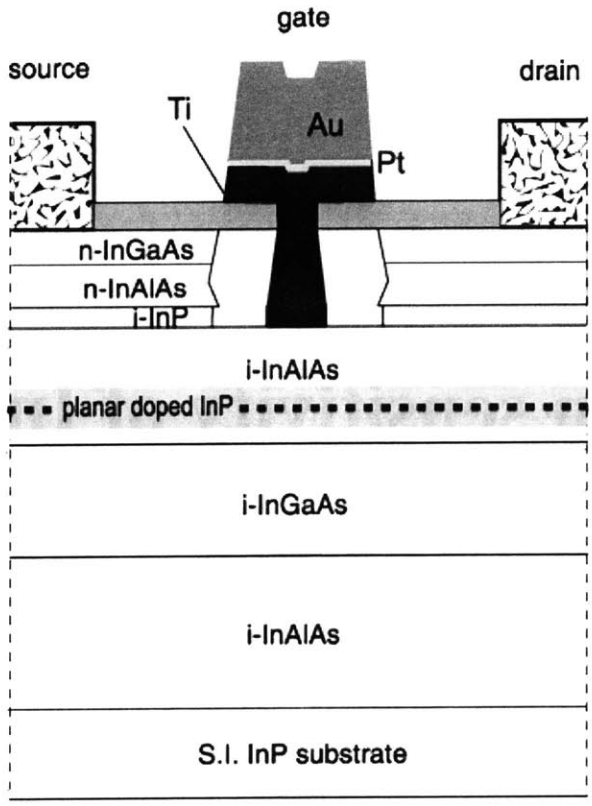

Fig. 4.1: InP HEMTs studied in this work. The intrinsic heterostructure consists of from bottom to top: 2000 Å InAlAs/ 150 Å InGaAs/ 90 Å InAlAs. The gate consists of 1000 Å Ti topped with Pt and Au layers.

4.2. ΔV_T Measurements

The investigated InP HEMTs (Fig. 4.1) feature a Ti/Pt/Au gate stack with a 1000 thick Ti layer and gate lengths between 30 nm and 1 μm. These devices were fabricated by Dr. Suemitsu from NTT for this study of the H-sensitivity. The intrinsic heterostructure consists of a 2000 Å InAlAs buffer, a 150 Å InGaAs channel, and a 90 Å InAlAs insulator. These devices were originally designed and optimized for the [01$\bar{1}$] gate orientation and a WSiN/Ti/Pt/Au gate. All experimental results in this chapter are for HEMTs with gates in the [01$\bar{1}$] orientation.

An experimental methodology was followed similar to that of section 3.2, consisting of three phases. Electrical device characterization was carried out at room temperature before and after every phase. The characterization suite was developed to minimally alter

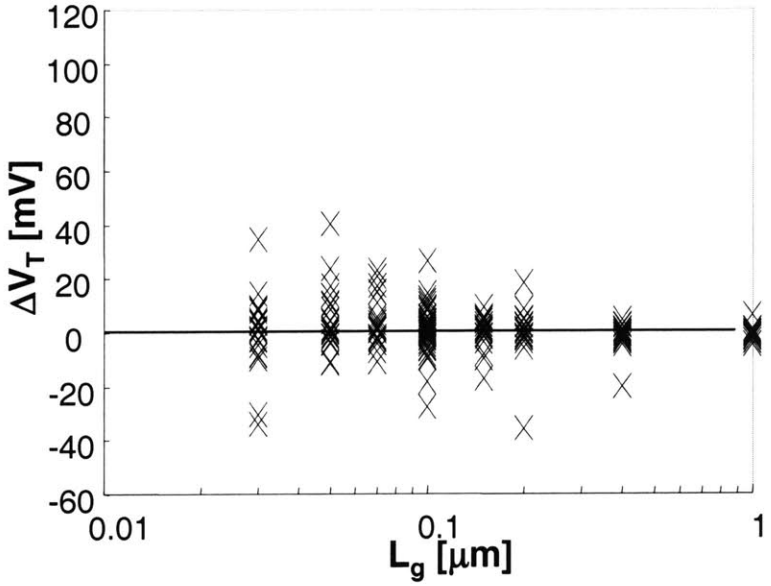

Fig. 4.2: Threshold voltage shifts caused in InP HEMTs with a thick Ti layer in the Ti/Pt/Au gate stack with a gate orientation parallel to [01$\bar{1}$] by a bake at 195°C in N_2.

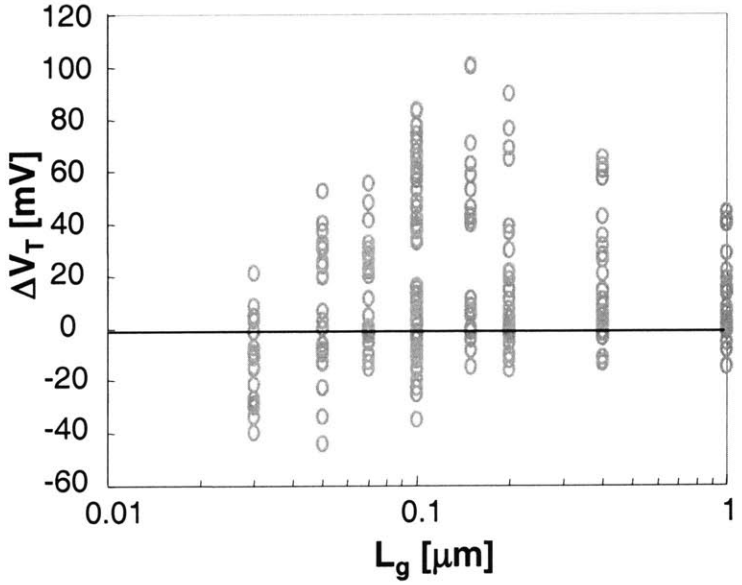

Fig. 4.3: Threshold voltage shifts caused in InP HEMTs with a thick Ti layer in the Ti/Pt/Au gate stack with a gate orientation parallel to [01$\bar{1}$] by a bake at 195°C in forming gas (5% H_2/95% N_2).

the device behavior. First, the devices were baked in N_2 at 195°C for over 100 hours to saturate all thermally induced effects. In a second phase, the thermal stability was evaluated by baking the devices again at 195°C for 2 h under N_2. Finally, the devices are baked at 195°C for 2h in forming gas containing 5% N_2. This allows a comparison of the

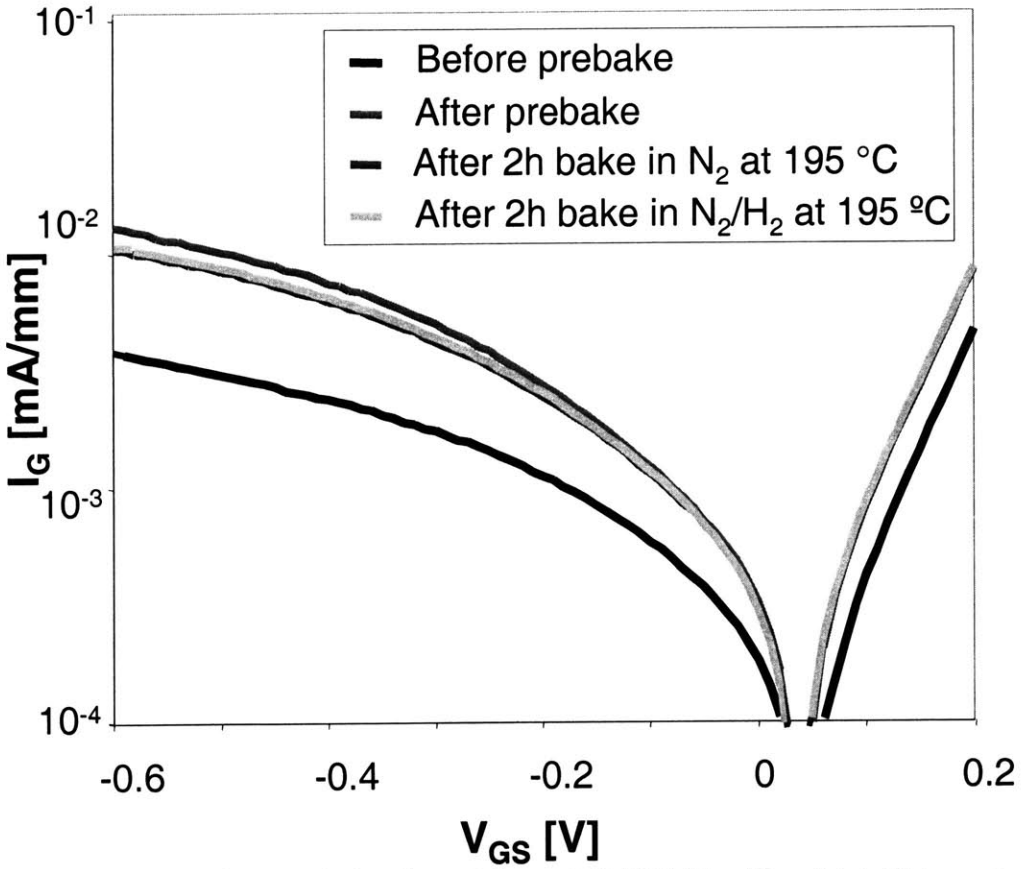

Fig. 4.4: I_G vs. V_{GS} characteristics for a 0.1 μm InP HEMT with a thick Ti layer in the Ti/Pt/Au gate stack and a gate-orientation parallel to $[01\bar{1}]$ during different stages in the degradation experiment. The H-induced V_T shift was –7 mV. The characteristics are shown before and after the prebake in N_2 at 195 °C and after the consecutive 2h bakes in N_2 and forming gas (5% H_2/95% N_2) at 195 °C.

effects of a 2h bake in N_2 and a 2h bake in forming gas, and thus, an estimate of the effects of H in a single device.

Figs. 4.2 and 4.3 show ΔV_T as a function of the gate length after the 2h N_2 and H_2 treatments, respectively, for devices with a gate orientation parallel to $[01\bar{1}]$. After 2h N_2 annealing, V_T typically changes less than 10 mV. In contrast, under forming gas, V_T changes over a wide range. A cluster of devices exhibits very small and mostly negative V_T changes, while in others, V_T shifts by as much as 100 mV. According to the model of Chapter 2, the H-induced piezoelectric effect induces large negative shifts for gate lengths around 0.1 μm. The observations in Figs. 4.2 and 4.3 cannot be explained by the H-induced piezoelectric effect alone.

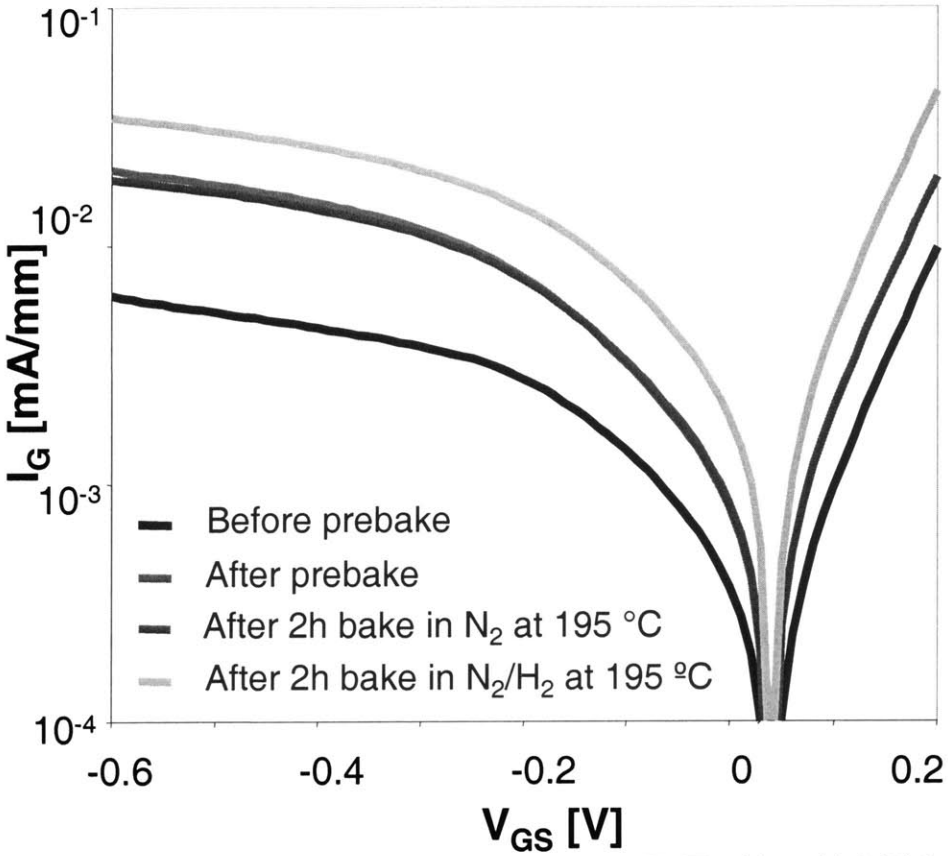

Fig. 4.5: I_G vs. V_{GS} characteristics for a 0.1 μm InP HEMT with a thick Ti layer in the Ti/Pt/Au gate stack and a gate-orientation parallel to [01$\bar{1}$] during different stages in the degradation experiment. The H-induced V_T shift was +40 mV. The characteristics are shown before and after the prebake in N_2 at 195 °C and after the consecutive 2h bakes in N_2 and forming gas (5% H_2/95% N_2) at 195 °C.

4.3. Different Degradation Mechanisms

In order to bring some understanding to this picture, many other figures of merit, such as R_D, R_S and I_G, were monitored during the experiment. The I_G characteristics were studied before and after the different bakes. Fig. 4.4 shows I_G vs. V_{GS} for a 0.1 μm InP HEMT that showed a small H-induced ΔV_T of –7 mV. The prebake in N_2 at 195 °C caused the forward gate current to increase significantly. The consecutive 2h bakes in N_2 and forming gas (5% H_2/95% N_2) did not affect the forward gate current.

Fig. 4.5 shows the I_G characteristics of a 0.1 μm InP HEMT that showed a large H-induced ΔV_T of +40 mV. The first two bakes had the same effects as on the I_G

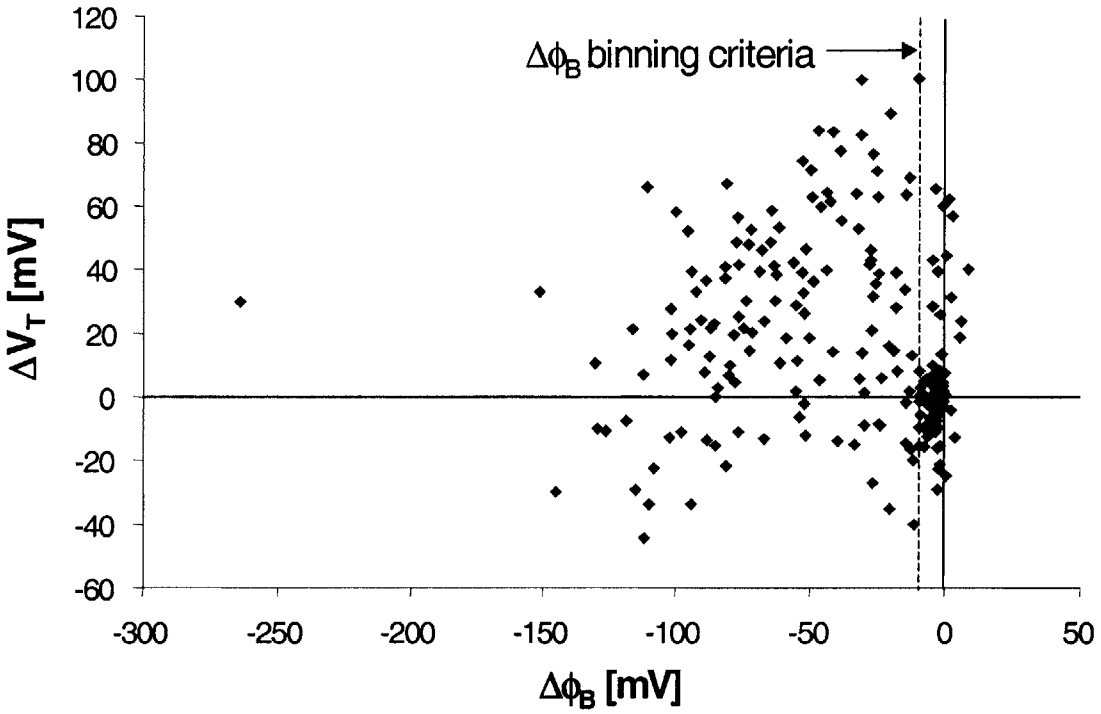

Fig. 4.6: Shift in V_T in function of the change of the Schottky-barrier height, $\Delta\phi_B$, during a 2h exposure to forming gas at 195°C. The binning criteria of $\Delta\phi_B$= 10 mV has been marked.

characteristics for the device shown in Fig. 4.2. The prebake caused a significant increase in the forward gate current, while the consecutive 2h bake in N_2 did not affect it. The 2h bake in forming gas, on the other hand, caused a significant increase in the forward gate current.

To quantify this different degradation behavior, the increase in forward I_G was translated into a shift of the Schottky barrier height of the gate, $\Delta\phi_B$, by examining the forward voltage that resulted in I_G= 1 mA/mm. At this current level, the forward branch of I_G followed an ideal exponential behavior. When $\Delta\phi_B$ during H-exposure is plotted in Fig. 4.6 as a function of ΔV_T for all devices, an interesting picture emerged. One cluster of devices showed both small shifts in V_T and in ϕ_B, while the rest of the devices showed a wide scatter in $\Delta\phi_B$ and ΔV_T.

If the H-induced ΔV_T is plotted in function of the reverse leakage current at V_{GS}=-0.6 V and V_{DS}=0.1 V after the prebake, a similar picture emerges in Fig. 4.7. A cluster of devices show a small leakage current and small negative ΔV_T, while the other devices

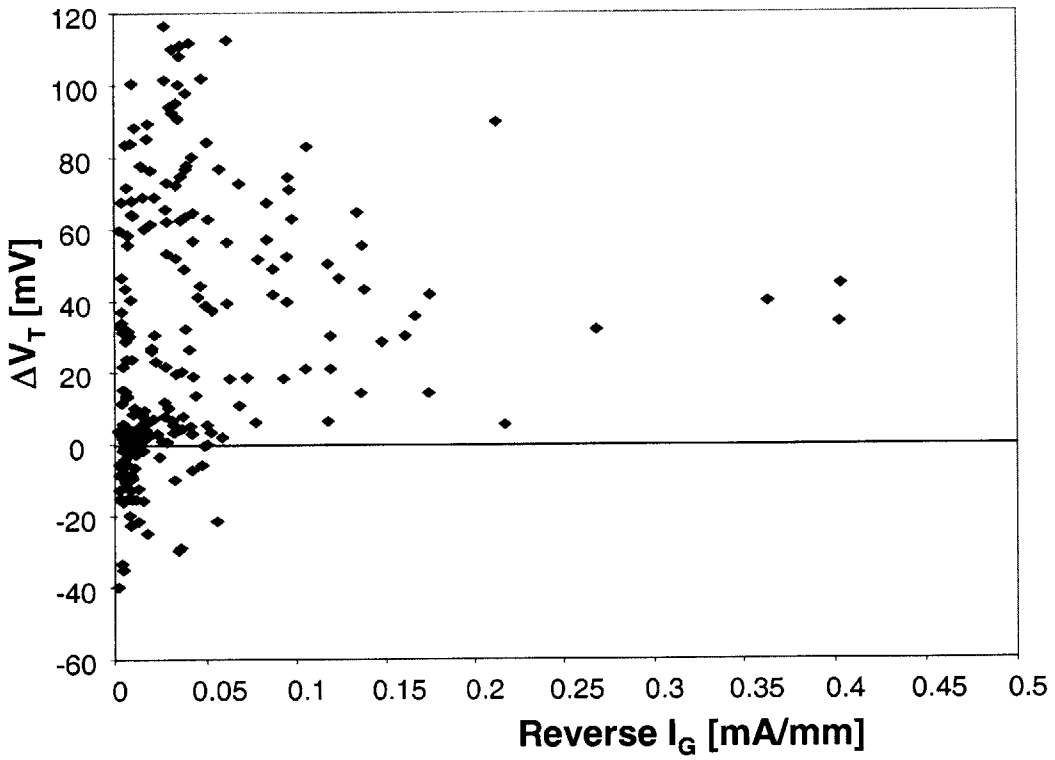

Fig. 4.7: Shift in V_T in function of I_G at V_{GS}=-0.6 V and V_{DS}=0.1 V after the prebake.

show widely scattered ΔV_T and reverse leakage currents. This suggests the two populations show differences around the gate-semiconductor interface.

This suggests that there are two distinct device populations. In one population, the H-induced degradation is characterized by small, negative ΔV_T and very small shifts in the parasitic resistances and the forward-biased gate current. The leakage current of these devices is relatively small. In the other population, the H-induced ΔV_T is large and widely scattered. Here, the forward-biased gate current increases significantly and the parasitic resistances decreases. Previous observations of the H-induced piezoelectric effect did not show any H-induced changes in the Schottky-barrier height [37].

The relative location of these transistors on the wafer showed that the two populations were differently distributed on the wafer. The devices showing significant H-induced $\Delta\phi_B$ were mostly located on the edge of the wafer, while the devices showing very small $\Delta\phi_B$ were mostly found in the center, which is sketched on Fig. 4.8.

These results suggest that there are two different mechanisms at play. In order to separate them, the transistors were binned in two groups according to the shift in ϕ_B that

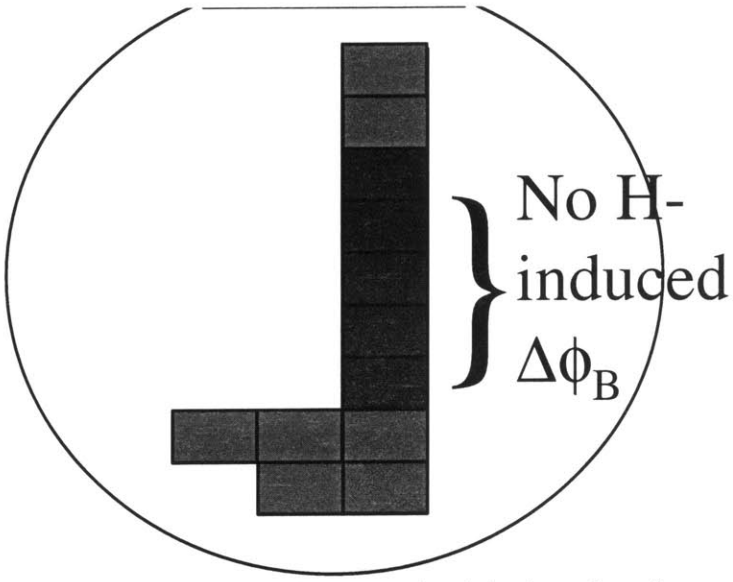

Fig. 4.8: Location on wafer of dies that contained devices that showed no significant H-induced shift in the Schottky Barrier height.

took place during H-exposure. This selection criteria was intended to separate devices in which ΔV_T took place through the piezoelectric effect from those in which V_T shifted by a different mechanism. A binning criteria of $\Delta\phi_B$=10 mV was selected. Figs. 4.9 and 4.10 showed the ΔV_T distribution of devices, induced by a 2h bake in N_2 and in forming gas (5% H_2/95% N_2), respectively, of devices that exhibited a H-induced $\Delta\phi_B$ smaller than 10 mV. These HEMTs were all located towards the center of the wafer. With a few exceptions, devices with short gate lengths in this population showed small negative ΔV_T of the order of 20 mV, while long devices showed a small positive ΔV_T of the order of 30 mV. Some devices showing large shifts still remained. It is likely that the selected binning criteria did not filter out these outliers. $\Delta\phi_B$ decreased with increasing gate length for all devices, independent of the amount of H-induced ΔV_T. This caused the binning criteria to be significantly less effective in separating the two populations in long devices.

When the location of the device on the wafer, as shown on Fig. 4.8, is used to bin the devices, a similar picture emerges. The V_T shifts induced by the 2h bake in N_2 and in forming gas are plotted in function of the gate length in respectively Figs. 4.11 and 4.12.

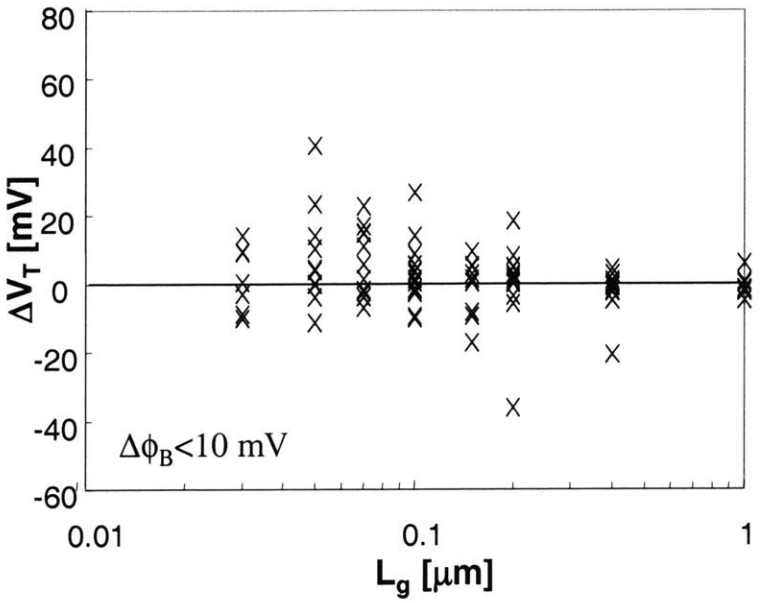

Fig. 4.9: Threshold voltage shifts caused by a bake at 195°C in N_2 for the devices from Fig.4.2 that showed a $\Delta\phi_B$ less than 10 mV during the bake in forming gas (5% H_2/95% N_2).

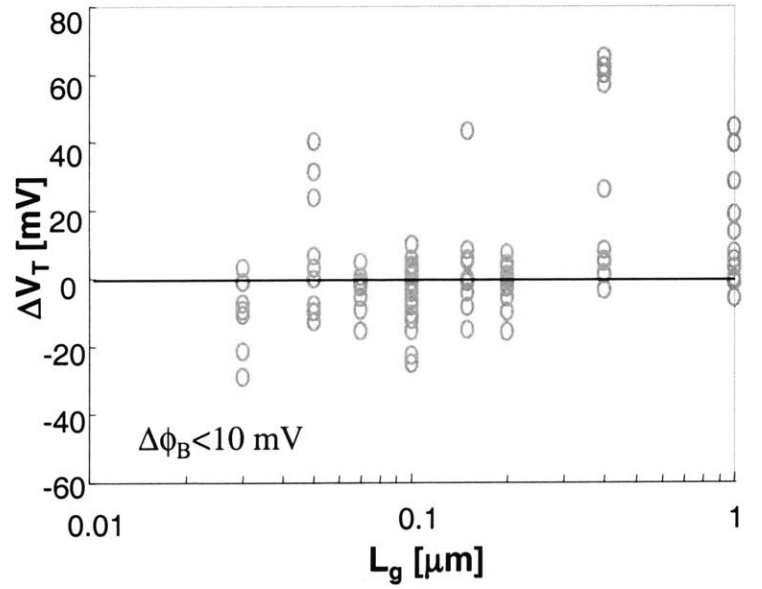

Fig. 4.10: Threshold voltage shifts caused by a bake at 195°C in forming gas (5% H_2/95% N_2) for the devices from Fig.4.2 that showed a $\Delta\phi_B$ less than 10 mV during the bake in forming gas.

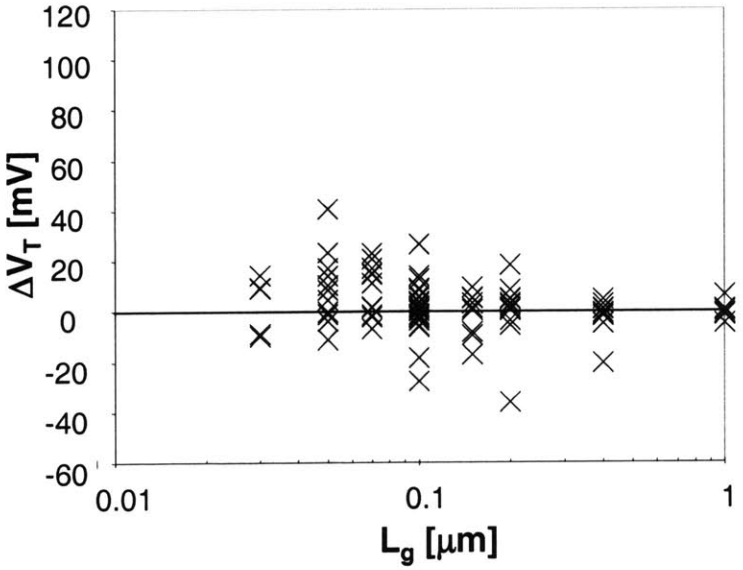

Fig. 4.11: Threshold voltage shifts caused by a bake at 195°C in N_2 for the devices from Fig.4.2 at the center of the wafer.

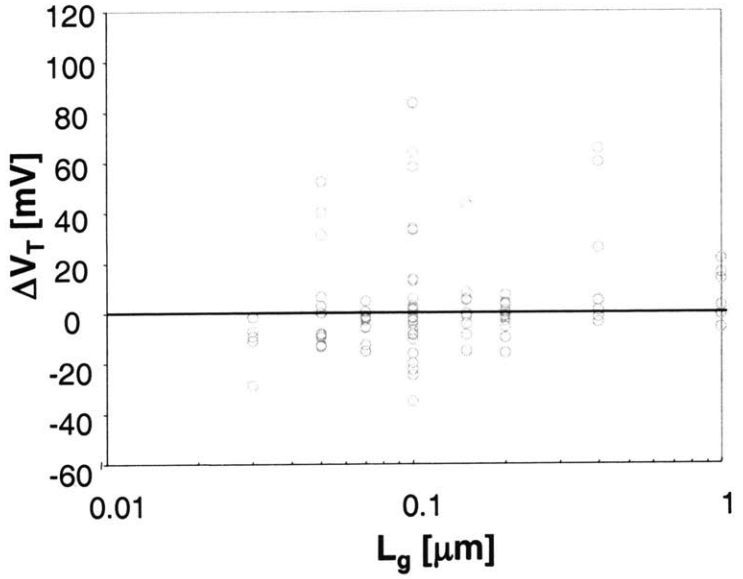

Fig. 4.12: Threshold voltage shifts caused by a bake at 195°C in forming gas (5% H_2/95% N_2) for the devices from Fig.4.2 that were located at the center of the wafer.

For short gate lengths, the H-induced ΔV_T are about an order of magnitude smaller than those observed in devices with Ti/Pt/Au gates containing a thin Ti layer under similar H-exposure conditions, as can be seen on Fig. 1.3. The H-induced ΔV_T are comparable to the most H-insensitive devices reported that feature a WSiN gate, as can be seen in Fig. 3.4. Other H-induced changes in the device characteristics were consistent with those previously attributed to the H-induced piezoelectric effect, such as a constant Schottky barrier height and small increases in the parasitic resistances [22, 35]. The medians of ΔV_T at a set gate length range between –9 mV and +5 mV (the average is not a good statistical figure of merit for a distribution such as this one that is spread around a value close to zero).

The second population of devices, mainly located towards the edge of the wafer, showed a widely scattered distribution in ΔV_T and $\Delta\phi_B$ and a reduction in the parasitic resistances. These changes in the device characteristics were similar to those occurring during the prebake in N_2 and were not consistent with the H-induced piezoelectric effect. The degradation that occurred during the prebake is most likely caused by a reaction between the gate and the underlying semiconductor ("gate sinking"). The H-induced degradation probably has a similar origin to the prebake. The localization of the two populations on the wafer suggests that this type of degradation is related to processing variations during the fabrication of the devices. The higher reverse gate leakage current in these HEMTs shows that there is a difference between the two populations in the gate-semiconductor area. For instance, if the InP etch stop layer is not completely etched, it comes in contact with the Ti layer in the gate stack. During annealing, the Ti sinks into the InP layer changing the electrical characteristics of the metal/semiconductor interface [58]. The prebake should completely exhaust this effect, however, it is possible that the presence of hydrogen enhances it. This mechanism is not related to the piezoelectric effect or any other previously reported H-induced degradation mechanism, but it is most likely a processing issue. It should not affect the H-sensitivity of properly fabricated and designed InP HEMTs with Ti/Pt/Au gates.

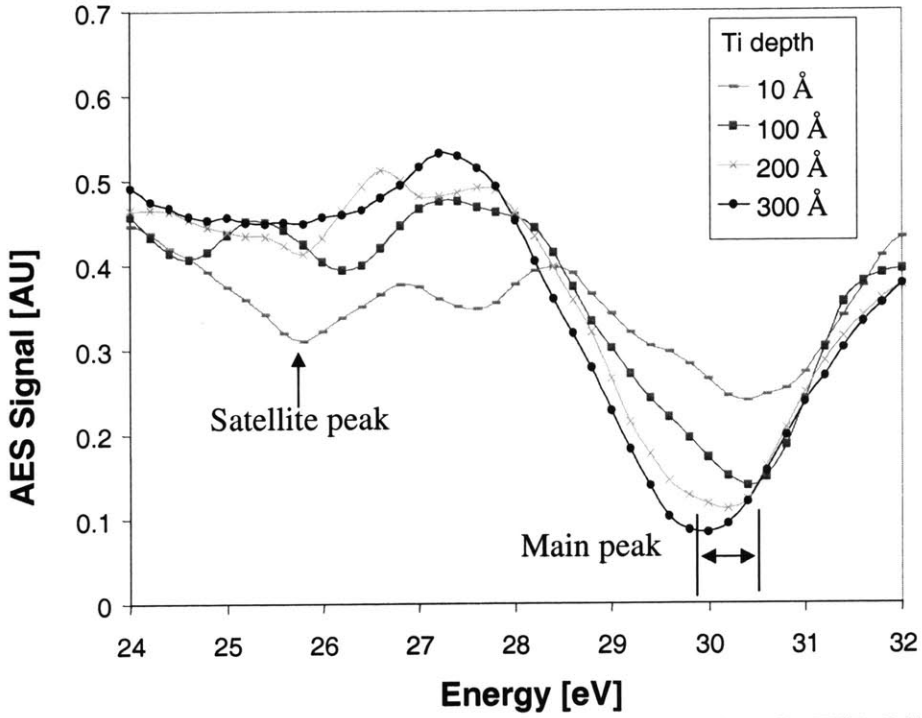

Fig. 4.13: Auger spectra of low-energy Ti peak at different depths of a Ti/Pt bilayer after 2h exposure to forming gas at 200 °C. Sample structure is shown in inset of Fig. 4.14.

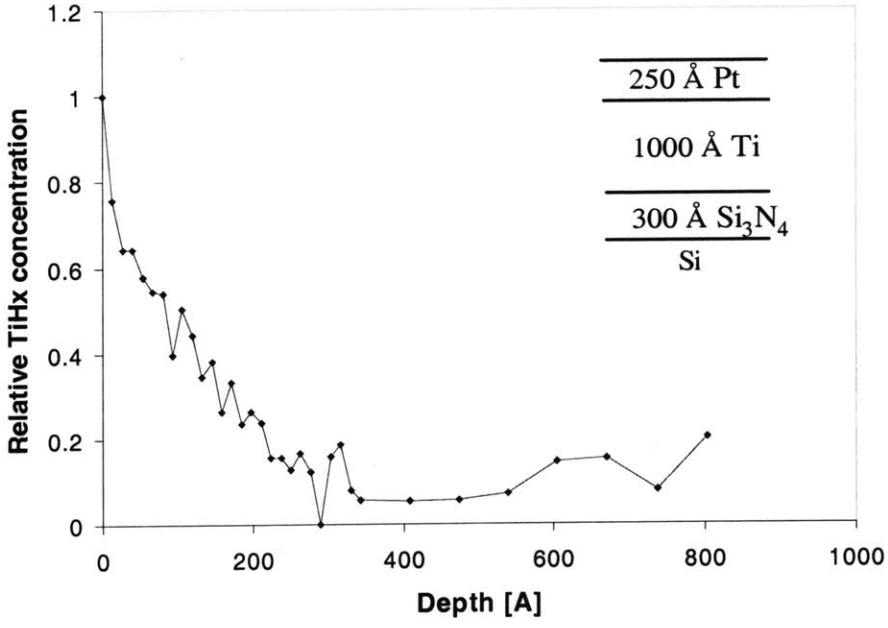

Fig. 4.14: Depth profile of TiH_x concentration, normalized to its value at the Pt/Ti interface, as measured by Auger Electron Spectroscopy. The sample structure is shown in the inset. Data obtained after 2h exposure to forming gas (5% H_2/95% N_2) at 200 °C.

4.4. Auger Electron Spectroscopy Observations

The small V_T shift caused by the H-induced piezoelectric effect, observed in the previous section, is inconsistent with a homogenous expanding Ti layer model. According to the model discussed in Chapter 2 for this orientation, the H-induced piezoelectric effect results in a very large, negative ΔV_T which should scale with the thickness of the expanding Ti layer. This suggests that a ΔV_T of several hundreds of mV should have been expected for the devices presented in this chapter. A result of the few tens of mV could be explained if Ti hydrogenation occurred only in a shallow region at the top of the Ti layer. The remaining Ti absorbs part of the mechanical stress and reduces the overall H sensitivity of the device. This is very likely because TiH_x is a known barrier for H-diffusion [59]. The diffusion mechanism of H in Ti occurs via the same tetrahedral sites that H occupies in TiH_x [60]. The Pt layer in the gate stack is a catalyst for breaking up molecular H_2 into atomic H. So, diffusion of the atomic hydrogen into the Ti-layer mostly initiates from the Ti/Pt interface. This atomic H reacts with the Ti to form TiH_x which blocks further diffusion of atomic H through the Ti.

In order to verify this hypothesis, an experiment was designed to determine how deep into the Ti layer, TiHx is formed. Test samples consisting of a Si substrate covered with Si_3N_4, 1000 Å of Ti and 250 Å of Pt were exposed to forming gas at 200 °C for 2 h. Then the composition of the Ti layer was experimentally evaluated as a function of depth using Auger Electron Spectroscopy (AES) [42]. The Auger spectra were collected using a primary beam energy of 2 keV with a modulation voltage of 2 V. The measurement system used a rastered beam. The composition profiles were obtained using Ar ion sputtering. The energy spectrum around the low energy Ti-peak was studied. The characteristic AES signatures of TiH_x are a shift of +1 eV in the low energy Ti peak and an emergence of a smaller hydride peak 5 eV below it [61].

AES spectra of the low energy Ti peak at different depths are shown in Fig. 4.13. The upper layers were representative for TiH_x. Looking deeper into the Ti layer, the main peak shifted by –1 eV and the sattelite peak slowly disappeared. At 300 Å in depth, the Ti

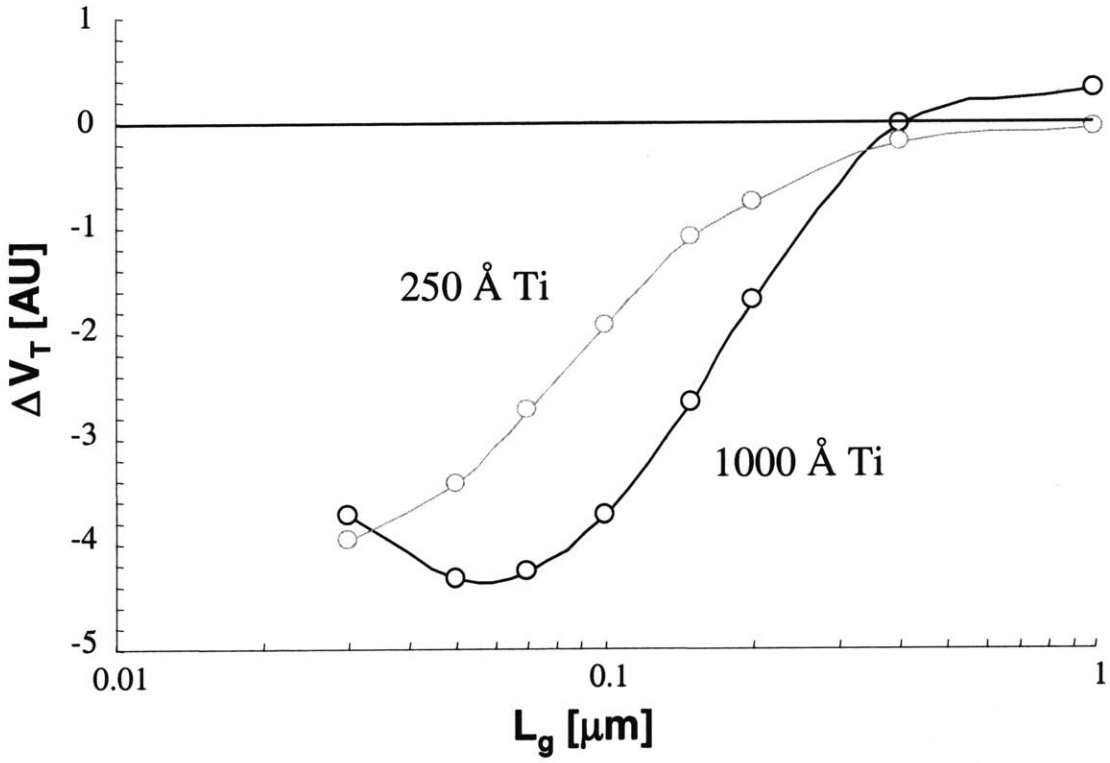

Fig. 4.15: Calculated ΔV_T vs. gate length for an InP HEMT with a 250 Å Ti /250 Å Pt /3000 Å Au and a 1000 Å Ti /250 Å Pt /3000 Å Au gate stack and a layer structure consisting of 2000 Å InAlAs/150 Å InGaAs/ 100 Å InAlAs (from bottom to top).

was essentially unreacted. An estimate for the relative TiH_x content as a function of depth is shown in Fig. 4.14. This estimate is the height of the low-energy Ti-peak normalized to the value at the Ti/Pt interface. Only the upper 250 Å of the Ti contain TiH_x. This explains the small H sensitivity of HEMTs with a thick Ti layer in the gate stack.

4.5. Modeling Results

In order to verify this explanation, device simulations were carried out using the techniques described in Chapter 2, which involve 2D finite element simulations using ABAQUS and 1D electrostatics calculations using MATLAB. A device was modeled with a layer structure consisting of 2000 Å InAlAs/150 Å InGaAs/100 Å InAlAs (from bottom to top). First, devices with a thin homogeneously expanding Ti layer were

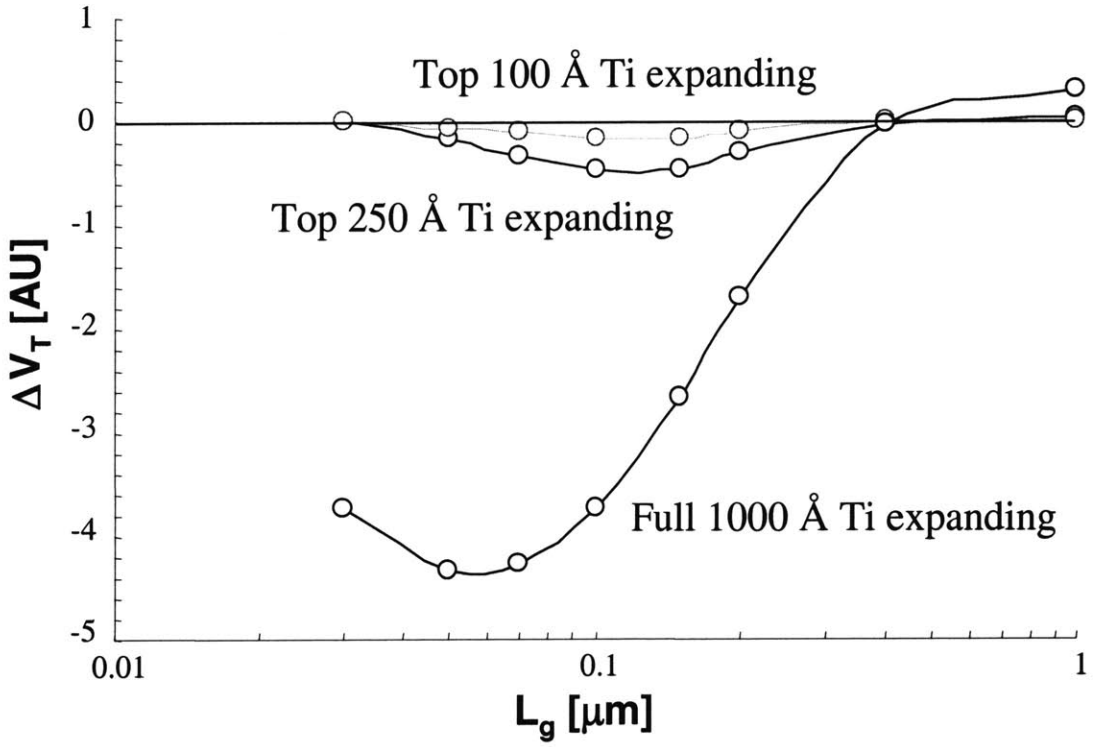

Fig. 4.16: Calculated ΔV_T vs. gate length for an InP HEMT with a 1000 Å Ti /250 Å Pt /3000 Å Au gate stack and a layer structure consisting of 2000 Å InAlAs/150 Å InGaAs/ 100 Å InAlAs (from bottom to top). Three data sets are shown. In one, the complete Ti layer expands. In the other two only the top 250 Å or 100 Å of the Ti layer expand.

modeled with a 250 Å Ti/ 250 Å Pt/ 3000 Å Au gate stack. Fig. 4.15 shows that when the homogeneously expanding Ti layer is thickened to 1000 Å, the H-induced ΔV_T increases by a factor of 2, except for very short devices. The results of these simulations are shown in Fig. 4.16 for a $[01\bar{1}]$ gate orientation. How the H-induced ΔV_T scales with the dimensions of the gate is further discussed in chapter 5.

Next, three different scenarios were simulated in the case of a 1000 Å Ti layer in the gate stack. In the first scenario the complete Ti gate reacted with H and expanded. In the second and third case, respectively, the top 250 Å and the top 100 Å of the Ti layer respectively formed TiH_x and expanded. Fig. 4.16 shows the calculated ΔV_T as a function of the gate length for these three different situations. If only the top 250 Å of Ti layer expanded as opposed to the entire layer, ΔV_T at short gate lengths decreased by as much

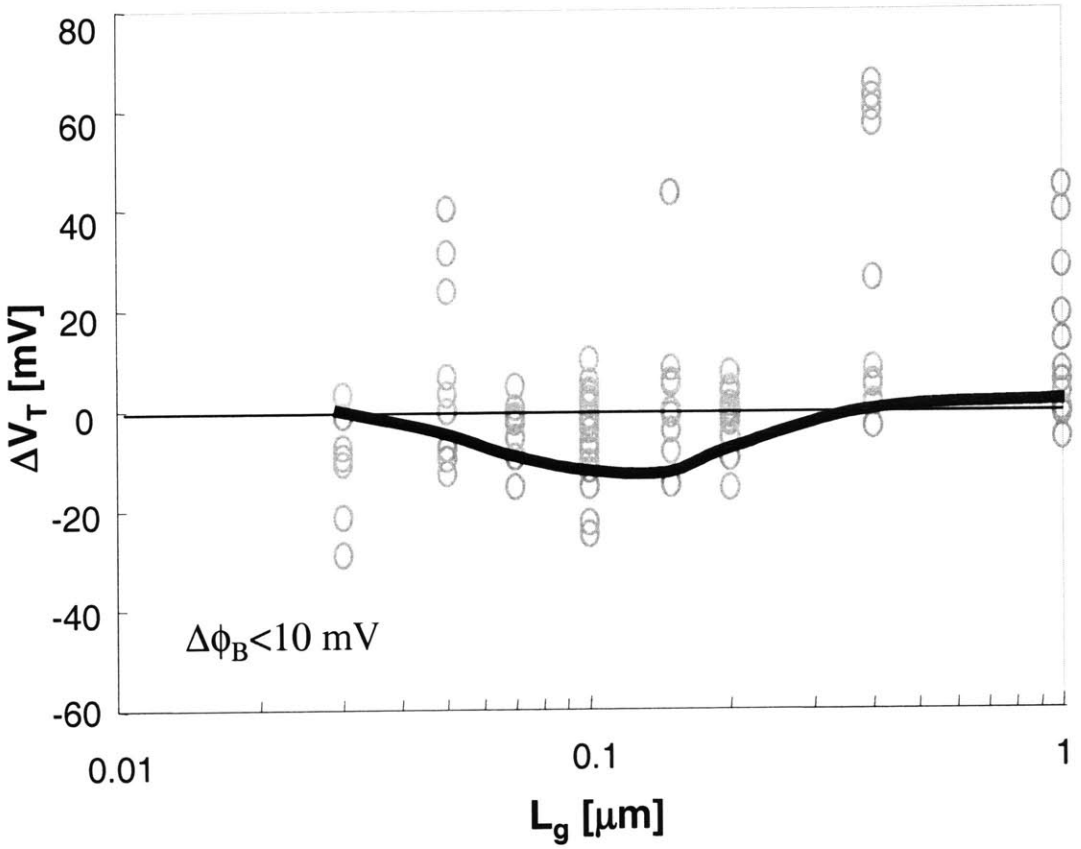

Fig. 4.17: The experimentally observed H-induced ΔV_T from Fig. 4.9 and the calculated ΔV_T using the model from Chapter 2, scaled by a proportionality factor and simulated with a model in which the top 250 Å of the Ti layer expands.

as an order of magnitude. When the thickness of the expanding layer further shrunk to 100 Å, ΔV_T halved again. This is consistent with the experimental observations of Figs. 4.9 and 4.10. As the expanding layer thinned and was further removed from the semiconductor, the mechanical stress in the semiconductor decreased, which resulted in a reduction in piezoelectric charge and a hydrogen-induced ΔV_T.

Fig. 4.17 plots the experimentally observed ΔV_T together with the calculated ΔV_T when only the top 250 Å of the Ti layer expanded. Since the calculated values are linearly proportional to the mechanical stress, they were scaled to match peak values. The large scatter in the data prevents any judicious discussion.

4.6. Summary

A thick Ti-layer in the Ti/Pt/Au gate of an InP HEMT reduced the sensitivity to the H-induced piezolectric effect by an order of magnitude. At first glance, this appears contradictory to the model of chapter 2. The diffusion mechanism of H in Ti, which limits hydrogenation of the Ti layer to a thin sheet at the top, explains this. Auger Electron Spectroscopy showed that TiH_x is only formed in the top 250 ′ of the Ti-layer. A second hydrogen mechanism that induced a larger positive ΔV_T, but was likely related to an anomalous processing issue, was observed. Assuming that the processing issue can be resolved, these results represent good news for InP HEMTs, as the H-induced piezoelectric effect in these devices can be mitigated by using a Ti/Pt/Au gate stack with a thick Ti layer. This approach, compared to using a WSiN-layer to separate the thin Ti-layer from the semiconductor, has advantages in simplicity.

In the next chapter, a discussion of how the H-induced ΔV_T scales with the different dimensions of the device structure, such as gate length and thicknesses of the layers in the gate stack and the heterostructure. The chapter also suggests practical device-level solutions to the H-induced piezoelectric ΔV_T.

Chapter 5

Discussion

The model for the H-induced piezoelectric ΔV_T presented in Chapter 2 is consistent with the qualitative experimental observations of the H-sensitivity of advanced InP HEMTs with a WSiN schottky gate metal and with a thick Ti layer in the Ti/Pt/Au gate stack discussed in Chapters 3 and 4. A few factors hinder the development of a fully quantitative model of the H-induced ΔV_T. There are great uncertainties in the mechanical model, such as the material properties and the precise mechanical expansion of the Ti gate. Additionally, the use of a 1D electrostatic model might be insufficient. These problems are discussed in this chapter.

This chapter also discusses in greater detail how ΔV_T scales with the different dimensions of gate and heterostructure. The gate length dependence is explained by examining how the depth distribution of the stress in the semiconductor heterostructure changes with L_g and how this affects ΔV_T. This chapter further discusses how other aspects of gate design, such as the thickness of the expanding TiH_x layer or the underlying WSiN layer affect the stress distribution. The details of the heterostructure determine how much the polarization charge shifts ΔV_T. How the thicknesses of the heterostructure layers influence ΔV_T is also explained. The chapter finishes with a summary of device design features that mitigate the H-sensitivity of InP HEMTs.

5.1. Limitations of the Model

The model for H-induced piezoelectric effect presented in Chapter 2 fits experimental observations of H-induced threshold voltage shifts relatively well. The dependence of ΔV_T on the gate length and different aspects of the device design are reasonably well predicted by the model, as discussed in Chapters 3 and 4.

This model, although it qualitatively explains the H-induced ΔV_T fairly well, is not a quantitative model. Several limitations hinder the development of a truly quantitative model. The reasons are discussed in this section.

5.1.1. Limitations of the Mechanical Model

First, the strain caused by the formation of TiH_x in the Ti layer is not precisely known. The stress in the semiconductor can be measured using radius-of-curvature measurements such as those presented in section 3.3. However, these stress measurements are imprecise. The Auger measurements in Chapter 4 showed a great uncertainty in the depth distribution of the formation of TiH_x, making it difficult to model the expansion of the Ti layer.

The mechanical model of the gate is dependent on the details of its structure. The exact form of the T-shaped or mushroom gate and how the gate rests on the HEMT significantly influence the mechanical stress induced in the semiconductor. Furthermore, the device passivation has a big impact on the mechanical rigidity of the structure. The exact details of the device structure may differ greatly among relatively similar devices because of process variations.

The piezoelectric and mechanical properties of the materials involved are not known precisely. The values reported in Tables 2.1 and 2.2 are the best known values at this time. No experimental data exists for the ternary compounds that are present in InP HEMTs.

Although these factors may introduce significant quantitative errors in the mechanical model of the stress in the semiconductor, they are not expected to impact the qualitative agreement between the model and the experimental observations that have been reported in earlier chapters.

5.1.2. Limitation of the 1D Electrostatics Model

The model for the threshold voltage uses a 1D electrostatic model at the center of the gate. As shown in Chapter 2, the piezoelectric charge is concentrated near the edge of the gate, so the stress-induced potential shift changes significantly there. When V_{DS} is small, the threshold voltage is mostly set by the potential at the center of the gate, since V_T is determined where the conduction band in the channel is highest with respect to the source. Because the H-induced potential shift changes significantly with location under the gate, the conduction band could move enough for the threshold voltage to be set at a different point.

Fig. 5.1 shows the stress-induced piezoelectric charge in a 0.1 μm InP HEMT with the structure of Fig. 3.1 and a [011] gate orientation. A significant amount of piezoelectric charge is located near the edge of the gate. To evaluate the relative significance of 2D electrostatic effects of this charge distribution on the potential, the 2D electrostatics problem was solved using MATLAB.

To enable the calculation with a PC, the 2D model used a coarser grid than the mechanical simulations. Only 40 points parallel to the gate length and 50 points perpendicular to the semiconductor heterostructure were used. MATLAB was used to transform the very fine grid used in the mechanical simulations into a coarser electrostatic grid, as is shown in Fig. 5.1. The grid was extended 0.1 μm from the center of the gate in the direction parallel to the gate length and to the bottom of the buffer in the direction perpendicular to the semiconductor heterostructure.

Poisson's equation and the charge distribution were translated into a 2000x2000 matrix using a finite difference technique. The electrostatic potential, U, was calculated

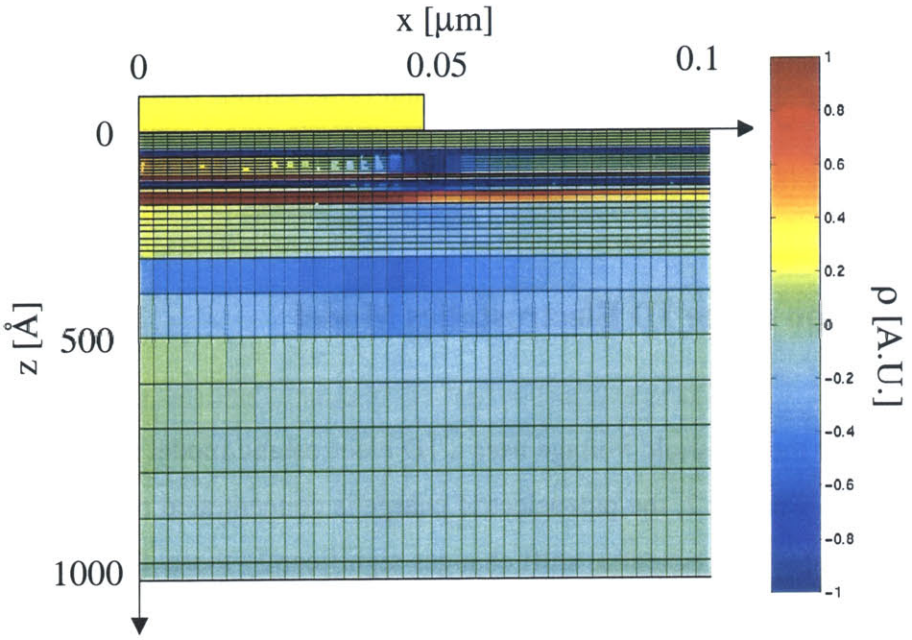

Fig. 5.1: Piezoelectric charge distribution in 0.1 μm InP HEMT with WSiN/Ti/Pt/Au gate stack oriented in the [011] orientation, induced by an expanding Ti layer.

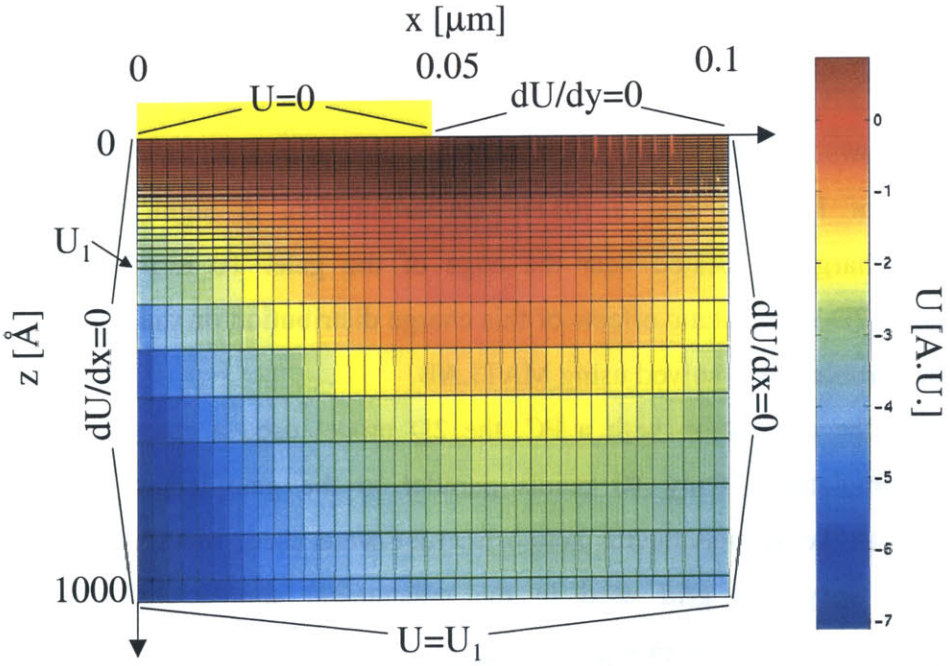

Fig. 5.2: H-induced potential shift in 0.1 μm InP HEMT with WSiN/Ti/Pt/Au gate stack oriented in the [011] orientation, induced by an expanding Ti layer in the case that no Fermi-level pinning takes place at the surface next to the gate. This is calculated using the charge distribution of Fig. 5.1 and the shown boundary conditions.

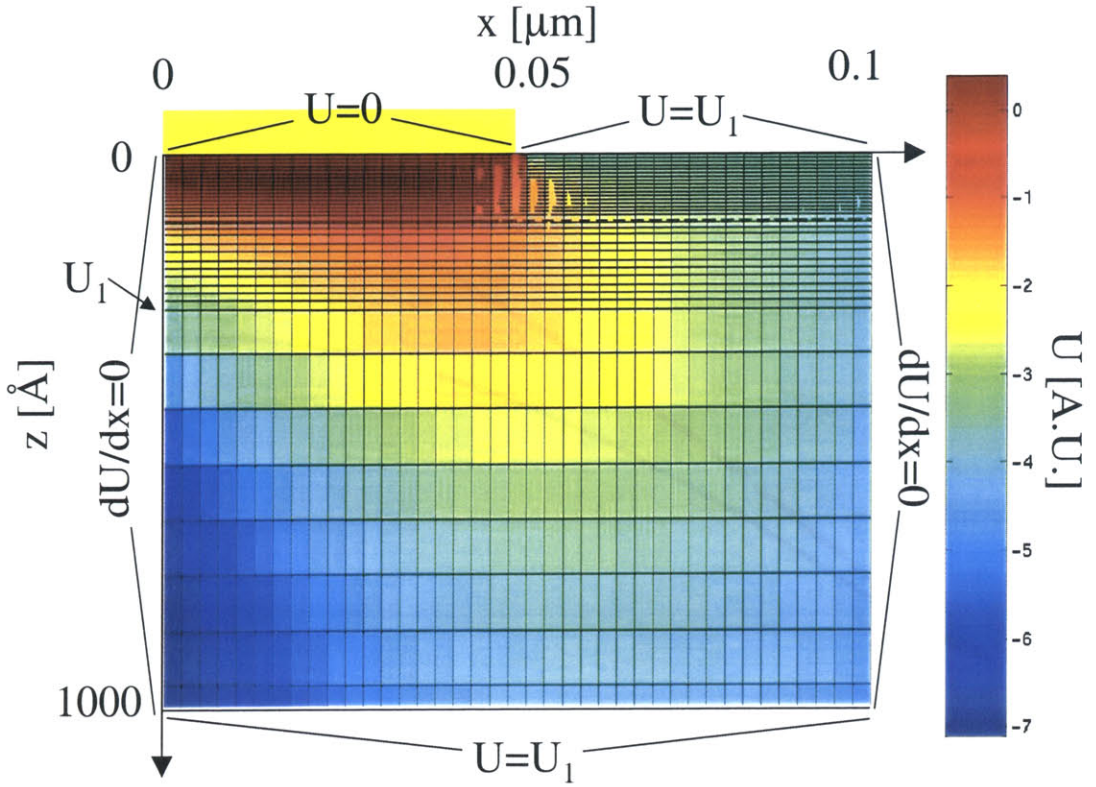

Fig. 5.3: H-induced potential shift in 0.1 μm InP HEMT with WSiN/Ti/Pt/Au gate stack oriented in the [011] orientation, induced by an expanding Ti layer in the case when Fermi-level pinning takes place at the surface next to the gate. This is calculated using the charge distribution of Fig. 5.1 and the shown boundary conditions.

setting different boundary conditions at the edges of the grid. These boundary conditions are sketched in Figs. 5.2 and 5.3. At the gate/semiconductor interface U=0 was fixed. At the bottom of the buffer the Fermi-level was pinned by setting the potential equal to the potential at the bottom of the channel at the center of the gate, U_1. At the center of the gate and at the edge of the grid distant from the gate an open boundary was set: dU/dx=0.

Two scenarios were considered for the boundary condition at the top surface next to the gate. In the first scenario, an open boundary was set: dU/dy=0. Fig. 5.2 shows the calculation of the H-induced potential shift in the top 1000 Å of the active device structure under this assumption. The electrostatic potential changes significantly with distance from the center of the gate at the bottom of the channel depending on the location beneath the gate.

In the second scenario, the Fermi-level was pinned at the surface next to the gate, $U=U_1$, which is a good assumption in III-V semiconductors. Fig. 5.3 shows the H-

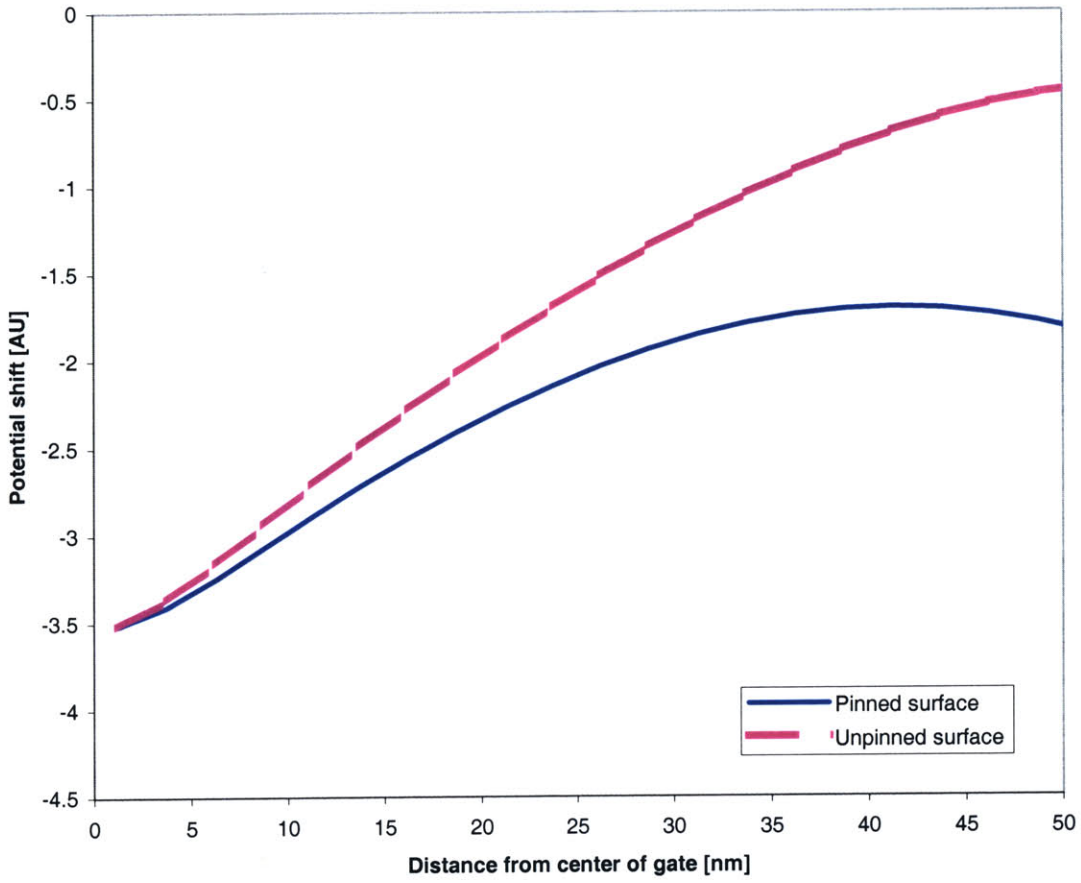

Fig. 5.4: The potential shift induced by the piezoelectric charge at the bottom of the channel of a 0.1 μm InP HEMT with a [011] gate orientation in function of the distance from the center of the gate in the cases that the Fermi-level at the surface next to the gate is pinned and unpinned.

induced potential shift in the top 1000 Å of the active device structure with the new surface boundary condition. The Fermi-level pinning screens the charge near the edge of the gate, thereby reducing the H-induced potential shift around that location.

In both scenarios, the potential shift at the bottom of the channel at the center of the gate is the same as the one found in the 1D electrostatics model. The potential shift induced by the polarization charge at the bottom of the channel as a function of the distance along the gate from the center of the gate is plotted on Fig. 5.4 for both surface boundary conditions. In both cases, the potential shift becomes less negative closer to the edge of the gate. The threshold voltage is set where the conduction band is the highest at the bottom of the channel. For small V_{DS} and without piezoelectric charge, this point is at

the center of the gate. Fig. 5.4 shows that the piezoelectric charge shifts the conduction band edge further down towards the edge of the gate. Therefore, the center of the gate remains the point that sets the threshold voltage regardless of 2D effects. This calculation therefore shows that for the [011] gate orientation the simple 1D electrostatics model is sufficient for the calculation of the H-induced ΔV_T.

In devices with a gate orientation parallel to $[01\bar{1}]$, the sign of the potential shift in Fig. 5.4 is flipped. Here, the piezoelectric charge brings the conduction band up. The lift of the conduction band increases towards the edge of the gate. If the stress-induced potential shifts are high enough, the conduction band could be highest at a location other than the center of the gate. This might reduce the magnitude of the large negative shifts predicted in short HEMTs. In long HEMTs, ΔV_T could become more positive. Calculation of the potential distribution at the bottom of the channel at threshold requires a model that incorporates Poisson's and Fermi-Dirac equations, which was not implemented here. The model might overestimate the H-induced shift ΔV_T for large negative shifts. The qualitative findings of the model still hold.

5.2. Scaling rules of piezoelectric ΔV_T

The model discussed in Chapter 2 explains several experimental observations of the H-induced piezoelectric ΔV_T in InP HEMTs fairly well. The following sections discuss how scaling of the device dimensions affects the H-induced ΔV_T, bringing further insight into the physics behind the H-sensitivity. First, the influence of the gate length and the gate structure on ΔV_T are presented. The expanding Ti layer in the gate induces the mechanical stress, therefore the gate structure determines the mechanical stress distribution in the semiconductor. The polarization charge is proportional to the mechanical stress and the material properties. How much this charge shifts V_T depends on the heterostructure, which is discussed in the final part of the section.

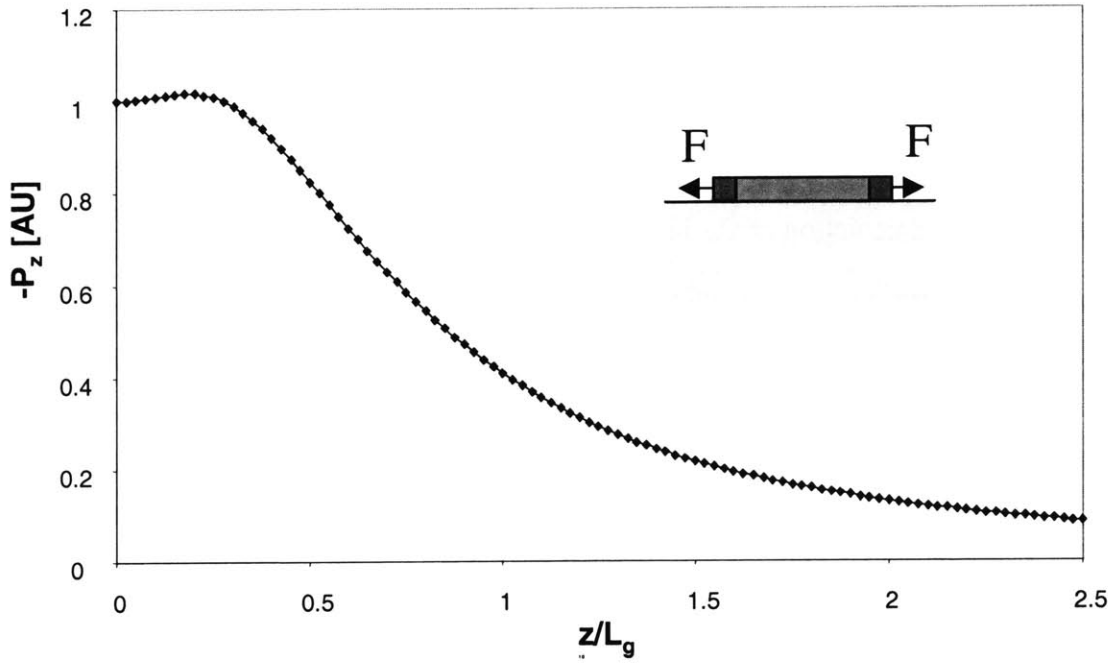

Fig. 5.5: Calculated $-P_z$ as a function of depth into the semiconductor at the center of the gate according to the model of Blech and Meieran [62]. The depth scales proportionally with L_g, while $-P_z(0)$scales inversely proportional with L_g.

5.2.1. Analytical model for the stress

5.2.1.a. The thin-gate approximation

The calculation of ΔV_T requires the depth profile of $-P_z$ underneath the center of the gate. To better understand how this depth profile depends on different device dimensions, a simplified analytical model is now presented. Blech and Meieran developed a simple two-dimensional analytical model for the stress induced by a thin finite expanding film on an underlying semi-infinite elastic solid [62]. This model is valid for very thin films. The stress exerted by the thin film on the underlying solid is modeled as being induced by two incremental forces acting at the two edges of the film, this is sketched in the inset of Fig. 5.5. The model predicts the following displacement parallel to the length of the film, u, at a distance x from the center of the gate and at a depth, z:

$$u(x,z)=\frac{2F}{\pi E}\left[(1-\nu^2)\ln\left(\frac{\left(\frac{L_g}{2}+x\right)^2+z^2}{\left(\frac{L_g}{2}-x\right)^2+z^2}\right)+(1+\nu)(3-4\nu)\left[\left(\frac{\left(\frac{L_g}{2}+x\right)^2}{\left(\frac{L_g}{2}+x\right)^2+z^2}\right)-\left(\frac{\left(\frac{L_g}{2}-x\right)^2}{\left(\frac{L_g}{2}-x\right)^2+z^2}\right)\right]\right] \quad [5.1]$$

where E is Young's modulus, ν is Poisson's constant, L_g is gate length and F is the force at the edge of the gate, which in thin films is given by the product of the thickness of the film, t, and the stress in the film, σ:

$$F=\sigma t \quad [5.2]$$

Differentiating equation [5.1] by x yields:

$$\frac{du(x,z)}{dx}=2F\left[\frac{1-\nu^2}{\pi E}\left(\frac{2\left(\frac{L_g}{2}-x\right)}{\left(\frac{L_g}{2}-x\right)^2+z^2}+\frac{2\left(\frac{L_g}{2}+x\right)}{\left(\frac{L_g}{2}+x\right)^2+z^2}\right)+\frac{(1+\nu)(3-4\nu)}{2\pi E}\left[\left(\frac{2\left(\frac{L_g}{2}-x\right)z^2}{\left(\left(\frac{L_g}{2}-x\right)^2+z^2\right)^2}\right)+\left(\frac{2\left(\frac{L_g}{2}+x\right)z^2}{\left(\frac{L_g}{2}+x\right)^2+z^2}\right)\right]\right] \quad [5.3]$$

At the center of the gate, x=0, this becomes:

$$\frac{du(x=0,z)}{dx}=\frac{4F(1+\nu)}{L_g\pi E}\left[\frac{(1-\nu)}{\frac{1}{4}+\left(\frac{z}{L_g}\right)^2}+\frac{(3-4\nu)\left(\frac{z}{L_g}\right)^2}{\left(\frac{1}{4}+\left(\frac{z}{L_g}\right)^2\right)^2}\right] \quad [5.4]$$

Plugging this in equation [2.6] provides $-P_z$ at the center of the gate:

$$-P_z(x=0,z)=\frac{4F(1+\nu)\mu d_{14}}{L_g\pi E}\left[\frac{1-\nu}{\frac{1}{4}+\left(\frac{z}{L_g}\right)^2}+(3-4\nu)\frac{\left(\frac{z}{L_g}\right)^2}{\left(\frac{1}{4}+\left(\frac{z}{L_g}\right)^2\right)^2}\right] \quad [5.5]$$

$-P_z$ at the gate-insulator interface, $-P_z(x=0,z=0)$, is given by:

$$-P_z(x=0,z=0)=\frac{16F(1-\nu^2)\mu d_{14}}{\pi E}\frac{1}{L_g} \quad [5.6]$$

An important result here is that $-P_z(x=0,z=0)$ is inversely proportional to L_g. $-P_z(x=0,z)$ can be normalized to its value at the gate-insulator interface:

$$\frac{-P_z(x=0,z)}{-P_z(x=0,z=0)}=\frac{1}{4}\left[\frac{1}{\frac{1}{4}+\left(\frac{z}{L_g}\right)^2}+\frac{(3-4\nu)}{(1-\nu)}\frac{\left(\frac{z}{L_g}\right)^2}{\left(\frac{1}{4}+\left(\frac{z}{L_g}\right)^2\right)^2}\right] \quad [5.7]$$

The resulting depth distribution, $-P_z(x=0,z)$, is plotted in a normalized way on Fig. 5.5, with a value of ν corresponding to InAlAs from Table 2.1. $-P_z(x=0,z)$ is proportional to the force F, which in thin layers, according to [5.2], is proportional to the layer thickness. The key result that this simple model provides is that $-P_z(x=0,z)$ depends on L_g and z according to:

$$-P_z(x=0,z)=\frac{1}{L_g}f\left(\frac{z}{L_g}\right) \quad [5.8]$$

where $f\left(\frac{z}{L_g}\right)$ is a function of $\frac{z}{L_g}$. $-P_z(x=0,z)$ depends on the depth z scaled by L_g. Therefore, $-P_z(x=0,z)$ decreases faster with increasing depth the shorter the gate length of the HEMT.

5.2.1.b Comparison of Simple Analytical Model with Numerical Model

This simple analytical model shows that $-P_z(x=0,z=0)$ scales with $1/L_g$ and that $-P_z(x=0,z)$ depends on the depth scaled by L_g. Now, the results of this simple model are compared with the results of a 2D simulator, which uses the mechanical properties of the whole device.

Fig. 5.6 shows $-P_z(x=0,z)$ normalized by $-P_z(x=0,z=0)$, as a function of depth scaled by L_g calculated by ABAQUS for gate lengths of 0.03, 0.1 and 1 μm using the device structure of Fig. 2.2. The 2D numerical calculations confirm that $-P_z(x=0,z)$ depends on depth scaled by L_g. Fig. 5.7 shows $-P_z(x=0,z=0)$ calculated by ABAQUS as a function of the gate length. Here, it is found that $-P_z(x=0,z=0)$ also roughly scales with $1/L_g$ except for very long gate lengths. This is what the simple analytical model predicts.

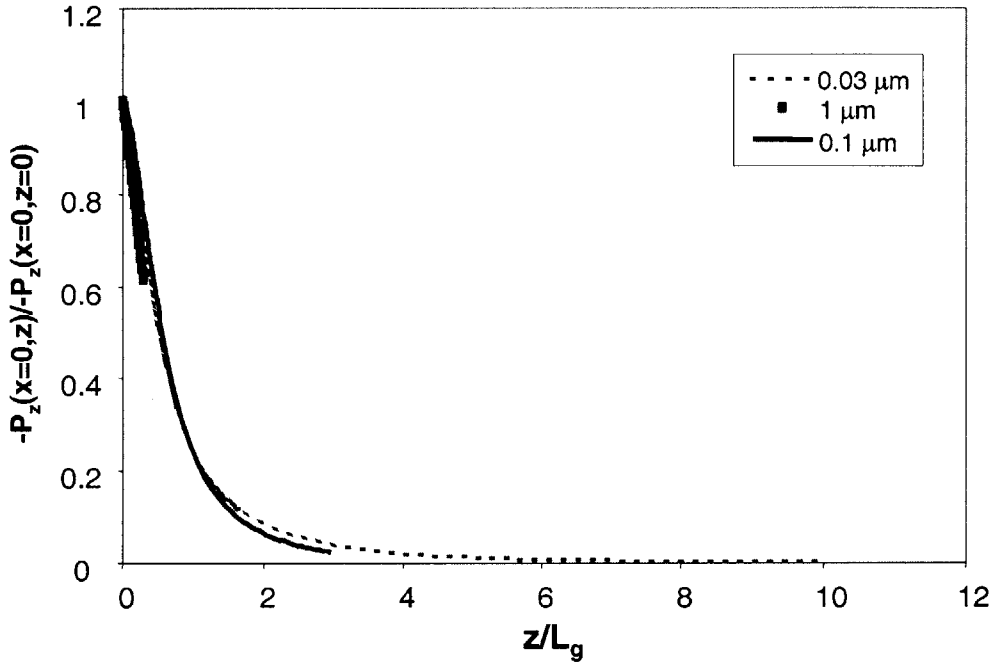

Fig. 5.6: Calculated polarization vector in the direction perpendicular to the gate, $-P_z$, at center of the gate as a function of the depth in the semiconductor scaled by L_g for the layer structure of Fig. 2.2 and gate lengths of 0.03, 0.1 and 1 μm and a gate orientation parallel to [011].

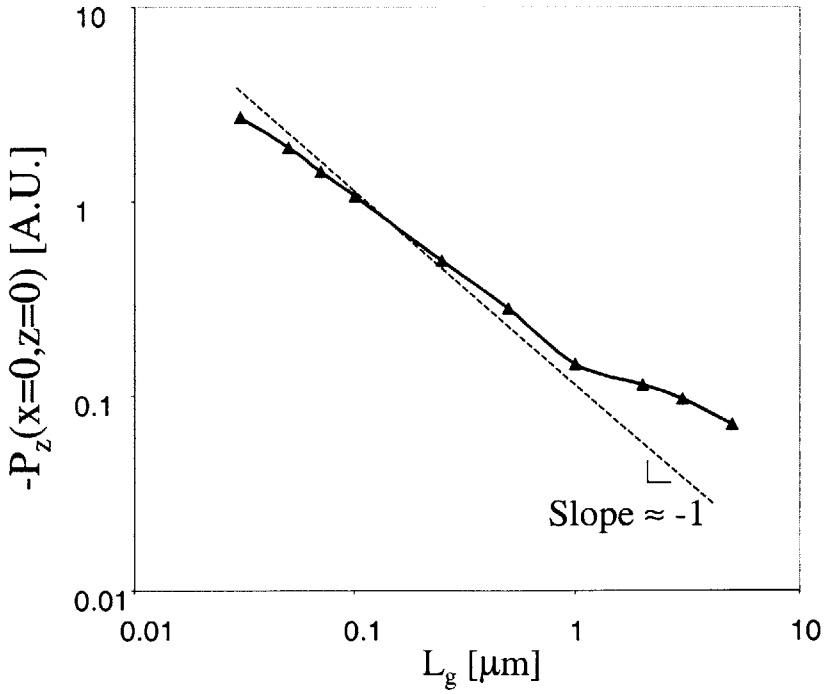

Fig. 5.7: $-P_z$ at the gate-insulator interface at center of the gate, $-P_z(x=0,z=0)$, calculated by ABAQUS as a function of L_g for the layer structure of Fig. 2.2 and a gate orientation parallel to [011]. The guideline is a line with a slope of –1.

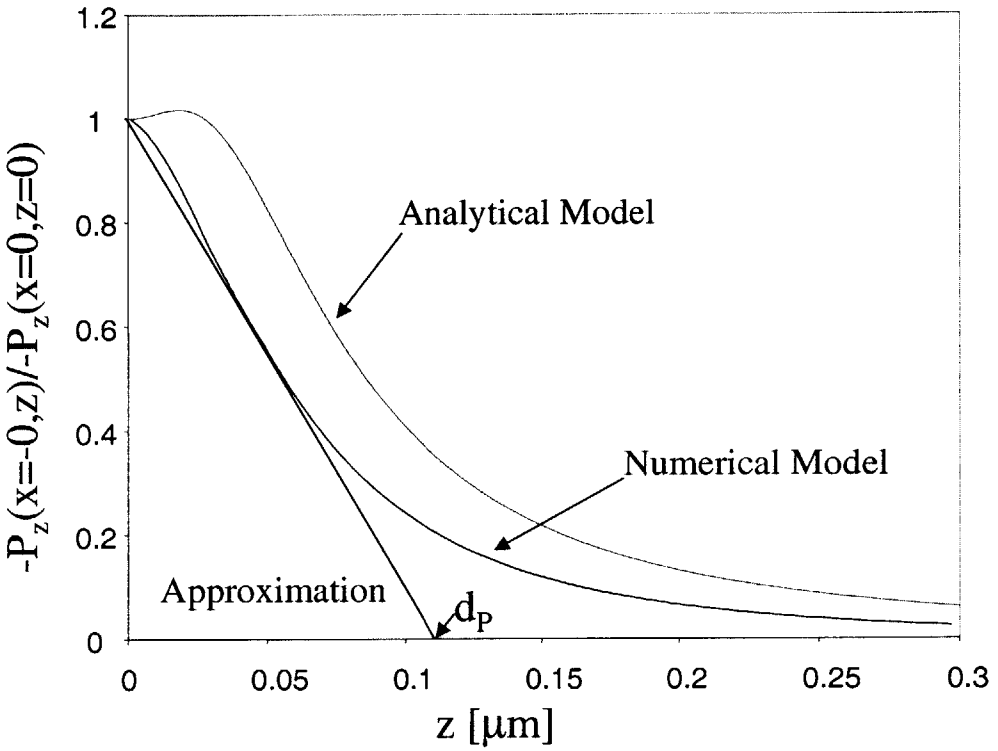

Fig. 5.8: Comparison of $-P_z(x=0,z)$ normalized by $-P_z(x=0,z=0)$ calculated by the simple analytical model from Blech and Meieran [62] to the one calculated by ABAQUS, for a gate length of 0.1 μm. The piezoelectric constants of the semiconductor are constant in this structure. The approximation of the depth profile used in 5.2.2.a is also shown.

Fig. 5.8 compares the two methods of calculating $-P_z(x=0,z)$ normalized by $-P_z(x=0,z=0)$. Here, the piezoelectric constants were assumed constant throughout the heterostructure. It can be seen that $-P_z(x=0,z)$ decreases faster with depth in the numerical model when compared with the analytical model. This is caused by the thickness of the expanding Ti layer and the rigidity added by the layers on top of the expanding Ti layer.

The key results of the simple analytical model are consistent with the results of 2D numerical simulations. In the next section, ΔV_T is calculated using the depth profile of $-P_z$. The influence of the gate dimensions on ΔV_T is explained using equation [5.8], which brings insight on how the depth profile depends on the gate length.

5.2.2. Influence of the Gate

The gate stack influences the H-induced piezoelectric ΔV_T. Conventionally, Ti/Pt/Au gate stacks have been used. The Ti forms the Schottky contact, the Pt forms a barrier with the Au that is used to lower the gate resistance. Other gate structures were studied that used WSiN as a Schottky metal covered with Ti/Pt/Au. The amount of mechanical stress caused by the expanding Ti layer in the gate stack depends on all aspects of the gate design. Because the piezoelectric charge is proportional to the mechanical stress, ΔV_T changes with the gate design. This section discusses how the design of the gate stack affects the H-induced piezoelectric ΔV_T.

5.2.2.a. Gate Length

As shown in the previous chapters, the H-induced ΔV_T is highly dependent on the gate length. According to equation [2.21], ΔV_T is proportional to the first order to the combined thickness of the insulator and channel, and to the difference between the average of the polarization above the channel-buffer interface, $<-P_z>_{ins+chan}$, and the average of the polarization in the buffer, $<-P_z>_{buf}$.

Fig. 5.8 shows the $-P_z(x=0,z)$ normalized by $-P_z(x=0,z=0)$ as a function of depth into the semiconductor. It can be seen that $-P_z(x=0,z)$ decreases quickly with increasing depth near the gate-insulator interface. At a certain depth, the polarization depth, d_P, $-P_z(x=0,z)$ has become small compared to $-P_z(x=0,z=0)$ and $-P_z(x=0,z)$ decreases at a slower rate. To understand how ΔV_T depends on L_g, the depth profile of $-P_z(x=0)$ can be approximated as decreasing linearly with depth until $z=d_P$, after which it becomes negligible. This approximation is sketched in Fig. 5.8.

Fig. 5.9 shows the depth into the semiconductor at which $-P_z$ becomes negligible, d_P, as a function of the gate length, which is given by:

$$d_P = \frac{-P_z(x=0,z=0)}{\left.\frac{dP_z(x=0)}{dz}\right|_{z=0}} \qquad [5.9]$$

The mechanical expansion originates at the edge of the gate. With decreasing L_g, the origin of the stress moves closer to the center of the gate causing both the stress and the

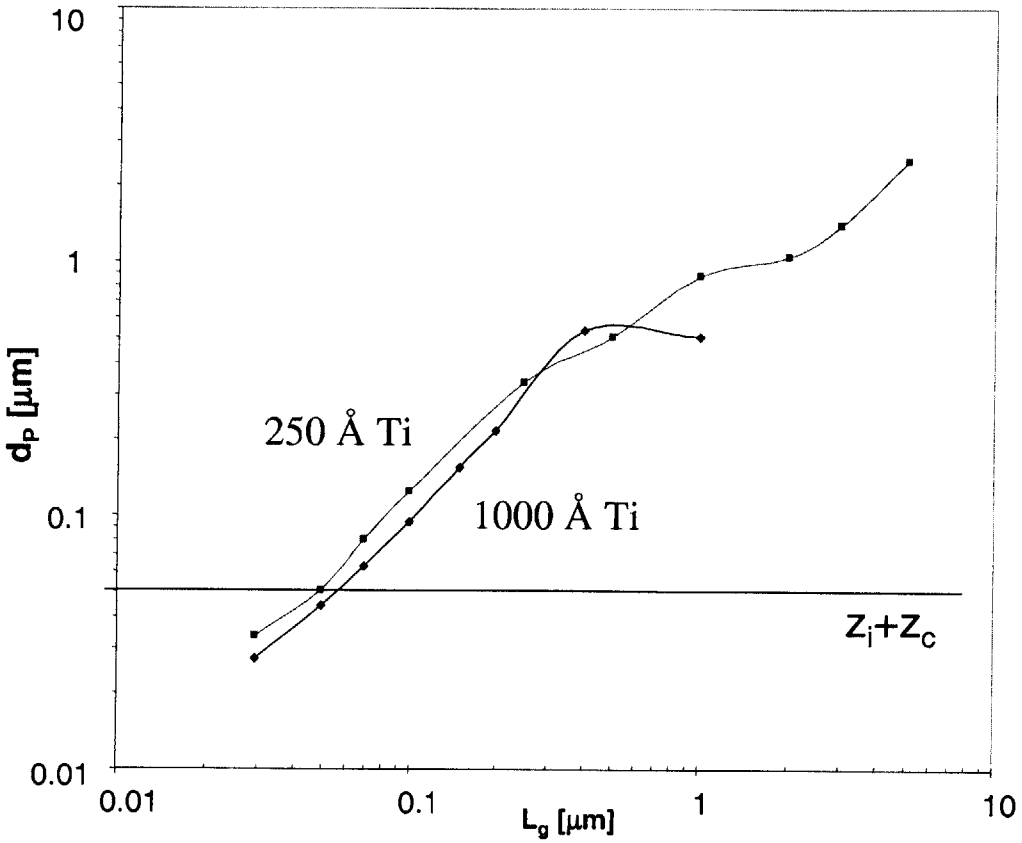

Fig. 5.9: Depth at which $-P_z$ becomes negligible, d_P, defined as $-P_z/dP_z/dz$ as a function of L_g calculated by ABAQUS for the layer structure of Fig. 2.2 and a gate orientation parallel to [011] with a Ti thickness of 250 Å and 1000 Å. z_i+z_c=500 Å is marked.

change in the stress at the center of the gate to increase significantly. Therefore, $-P_z(x=0,z=0)$ increases and d_P decreases with shortening gates. $-P_z(x=0,z=0)$ scales roughly with $1/L_g$ for thin Ti layers in the gate, which can be seen on Fig. 5.7. In consequence, d_P scales roughly with L_g, which can be seen on Fig. 5.9. Both these scaling rules are consistent with the simple analytical model (equation [5.4]), where the polarization is inversely proportional to L_g and the depth dependence scales with L_g.

Now ΔV_T is calculated using equation [2.23] and the approximation of the depth profile sketched in Fig. 5.8. In the following approximation, the differences in piezoelectric constants in the materials are ignored. With this approximation for $0<z<d_P$, $-P_z(x=0,z)$ can be written as:

$$-P_z(x=0,z) = -P_z(x=0,z=0)\times\left(1-\frac{z}{d_P}\right) \qquad [5.10]$$

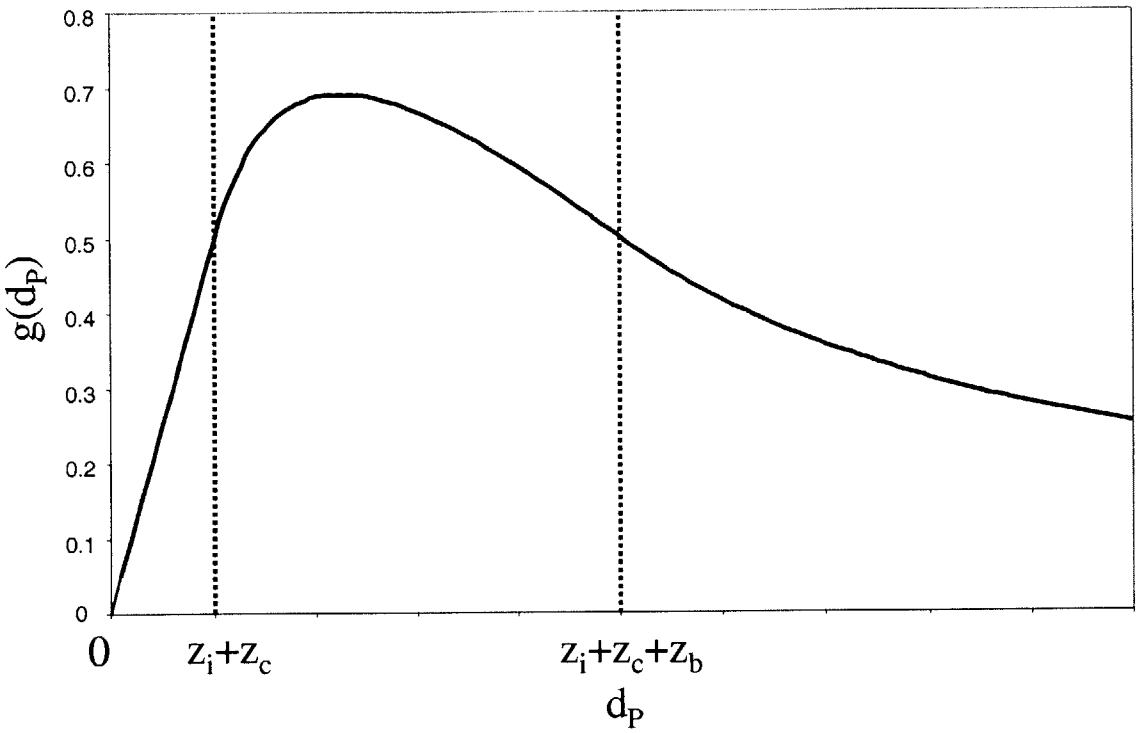

Fig. 5.10: $g(d_P)$, function how ΔV_T depends on d_P as a function. This is valid in the approximation that the piezoelectric material is constant throughout the heterostructure and that $-P_z(x=0)$ decreases linearly with increasing depth until $z=d_P$, and $-P_z(x=0,z>d_P)=0$.

Using equation 2.23, ΔV_T can be calculated as:

$$\Delta V_T \propto \frac{-P_z(x=0,z=0)}{z_i+z_c}\int_{z=0}^{z=\max(z_i+z_c,d_P)}\left(1-\frac{z}{d_P}\right)dz-\frac{-P_z(x=0,z=0)}{z_b}\int_{z=\max(z_i+z_c,d_P)}^{z=\max(z_i+z_c+z_b,d_P)}\left(1-\frac{z}{d_P}\right)dz \qquad [5.11]$$

this can be written as:

$$\Delta V_T \propto -P_z(x=0,z=0)\times g(d_P) \qquad [5.12]$$

Where $g(d_P)$ is a function of d_P, which has a different functionality dependent on the gate length and the dimensions of the heterostructure. Fig. 5.10 shows $g(d_P)$ as a function of d_P. In very short devices, when $d_P< z_i+z_c$, the approximation yields

$$g(d_P)=\frac{d_P}{2(z_i+z_c)} \qquad [5.13]$$

In this case, $<-P_z>_{ins+chan}$ scales proportionally with d_P and $-P_z(x=0,z=0)$, while $<-P_z>_{buf}$ is negligible compared to $<-P_z>_{ins+chan}$. When the HEMT shortens $-P_z(x=0,z=0)$ scales approximately inversely proportional with the gate length, while d_P scales approximately

proportional to the gate length. These two effects counter each other and ΔV_T increases very slowly with shortening gate length. When $z_i+z_c+z_b>d_P>z_i+z_c$:

$$g(d_P)=1-\frac{z_i+z_c}{2d_P}-\left(\frac{(d_P-(z_i+z_c))^2}{2d_P z_b}\right) \qquad [5.14]$$

ΔV_T is proportional to $-P_z(x=0,z=0)$ ($\propto 1/L_g$) and to a factor that changes slowly with d_P, as can be seen in Fig. 5.10. Therefore, to the first order, in this regime, ΔV_T scales inversely with L_g. Here, $<-P_z>_{buf}$ is small compared to $<-P_z>_{ins+chan}$, therefore ΔV_T is positive. For long HEMTs, $d_P>z_i+z_c+z_b$ and

$$g(d_P)=\frac{z_i+z_c+z_b}{2d_P} \qquad [5.15]$$

ΔV_T still scales with $-P_z(x=0,z=0)$ and $1/d_P$. Therefore, ΔV_T scales with $1/L_g^2$. d_P has little effect on $<-P_z>_{ins+chan}$. But, $<-P_z>_{buf}$ is of comparable magnitude to $<-P_z>_{ins+chan}$. $-P_z$ remains almost constant within the active device, except for the different material properties in the layers. $<-P_z>_{ins}$, $<-P_z>_{chan}$, and $<-P_z>_{buf}$ would almost be equal if not for the lower piezoelectric constant of the material in the channel. Therefore, at a certain long gate length $<-P_z>_{ins+chan}$ becomes lower than $<-P_z>_{buff}$ and the H-induced ΔV_T becomes negative. In these devices, ΔV_T is highly dependent on the thickness of the insulator and channel and their material properties. As $-P_z(x=0,z=0)$ scales inversely proportional to L_g, which can be seen on Fig. 5.7, ΔV_T still decreases with increasing L_g.

Fig. 5.11, which shows ΔV_T and $-P_z(x=0,z=0)$ vs. L_g scaled so that both ΔV_T and $-P_z(x=0,z=0)$ are equal at 0.1 μm. ΔV_T depends on the value of $-P_z(x=0,z=0)$ and the rate at which $-P_z(x=0,z)$ decreases with depth into the semiconductor, as discussed above. In devices significantly smaller than 70 nm, d_P is smaller than z_i+z_c and ΔV_T is positive and changes little with gate length. At short gate lengths, longer than 70 nm and shorter than 200 nm, d_P is larger than z_i+z_c. In this case, $<-P_z>_{ins+chan}$ changes slowly with d_P as seen in Fig. 5.11 and scales proportionally to $-P_z(x=0,z=0)$. ΔV_T is positive and scales with $1/L_g$. In long devices, d_P is significantly larger than z_i+z_c. Here, ΔV_T becomes negative and depends mostly on the details of the heterostructure.

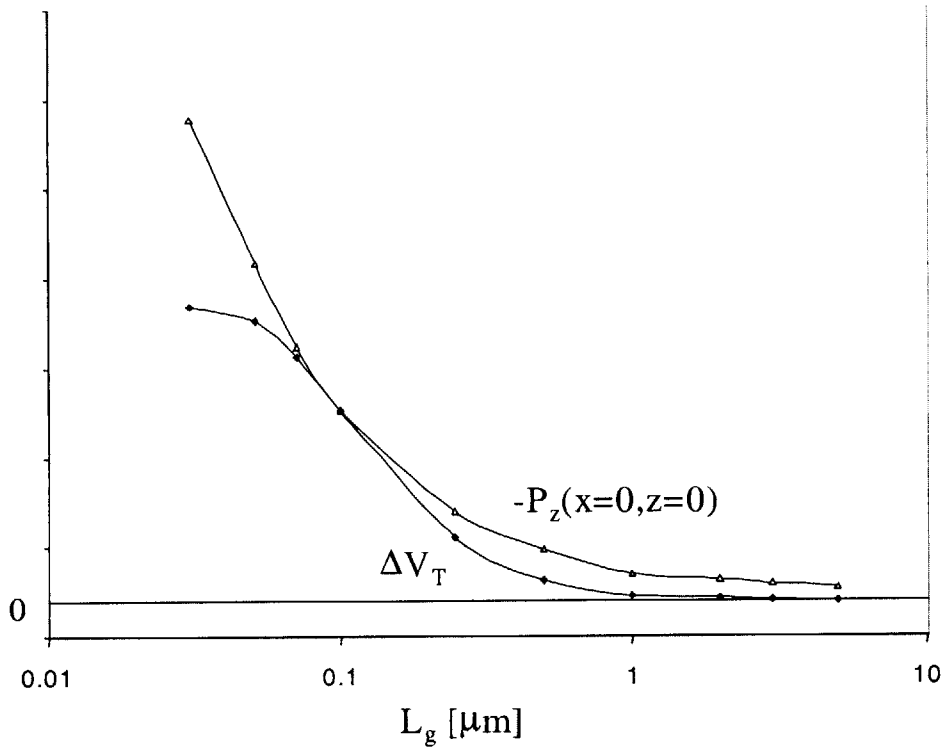

Fig. 5.11: $-P_z$ at the gate-insulator interface at center of the gate, $-P_z(x=0,z=0)$, calculated by ABAQUS and the resulting ΔV_T as a function of L_g for the layer structure of Fig. 2.2 and a gate orientation parallel to [011]. The values of ΔV_T and $-P_z(0)$ are scaled such that they are equal for a L_g of 0.1 μm.

5.2.2.b. Gate stack

The other layers of the gate stack also affect the stress in the semiconductor. A non-expanding layer underneath the expanding TiH_x absorbs the mechanical stress and decreases the polarization at the gate-insulator interface. Placing a non-expanding layer under the Ti layer is a very efficient method to reduce the H-induced ΔV_T in short devices, when the gate length is smaller than the thickness of this non-expanding layer. In long HEMTs, the H-induced ΔV_T is only slightly reduced by the presence of the non-expanding layer. This layer can be a WSiN layer, as has been discussed in Chapter 3, or a thick non-expanding Ti layer, as has been presented in Chapter 4.

The ratio of the thickness of the non-expanding layer, t, over the gate length, L_g, plays an important role. According to the simple analytical model, $-P_z$ at the gate insulator interface is given by substituting z=t in equation [5.4]:

$$-P_z(x=0,z=0)=\frac{4F(1+\nu)\mu d_{14}}{L_g \pi E}\left[(1-\nu)\left(\frac{1}{\frac{1}{4}+\left(\frac{t}{L_g}\right)^2}\right)+(3-4\nu)\frac{\left(\frac{t}{L_g}\right)^2}{\left(\frac{1}{4}+\left(\frac{t}{L_g}\right)^2\right)^2}\right] \quad [5.16]$$

When the thickness of the non-expanding layer is larger than the gate length, $t/L_g >> 0.5$, this can be approximated as:

$$-P_z(x=0,z=0)\approx\frac{4F(1+\nu)\mu d_{14}}{\pi E}(4-5\nu)\frac{L_g}{t^2} \quad [5.17]$$

Therefore $-P_z(x=0,z=0)$ scales with L_g/t^2 in stead of $1/L_g$ and $g(d_P)$ scales with L_g for short gate lengths. Since ΔV_T scales with $-P_z(x=0,z=0)$ and $g(d_P)$, it scales with L_g^2/t^2 in short devices. Here, ΔV_T becomes smaller when the gate length becomes shorter, which can be seen in Fig. 3.7. A thicker non-expanding layer underneath the Ti layer reduces ΔV_T dramatically in short HEMTs. In long HEMTs, equation [5.17] is not valid. Therefore, $-P_z(x=0,z=0)$ and the H-induced ΔV_T decrease slowly when t increases.

The layers on top of the Ti layer also affect the stress that is induced in the semiconductor. The higher the rigidity of these layers, the more the mechanical stress is reduced in the underlying semiconductor. Thicker layers or materials with a higher Young Modulus increase the rigidity. The reduced stress decreases the H-induced ΔV_T in short devices. In long devices the effect on the H-induced ΔV_T is lower. The L_g at which ΔV_T changes sign becomes shorter with increasing rigidity, because the rigidity increases d_P. This has been shown in Figs. 2.12 and 2.13, which show the change in H-induced ΔV_T when the Au layer on top of the gate stack thickens, or a nitride layer covering the gate stack is added.

5.2.2.c. Ti thickness

The thickness of the Ti in the gate stack impacts the stress in the semiconductor, and thus, the H-induced ΔV_T. Formation of the TiH_x layer only occurs in the top 200 Å of the Ti layer, as has been shown in Chapter 4. If the Ti layer is thinned below 200 Å, the

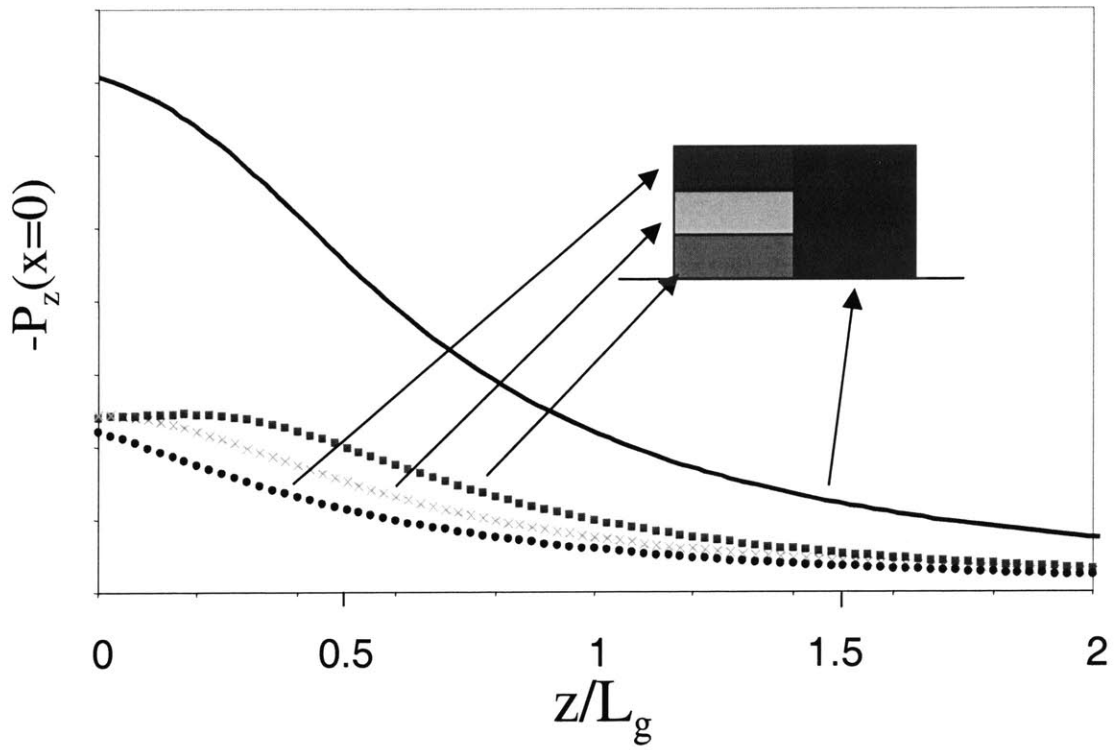

Fig. 5.12: Calculated polarization vector in the direction perpendicular to the gate, $-P_z$, at center of the gate as a function of the depth in the semiconductor induced by thin expanding layers at different heights in the gate stack and their superposition according to the model of Blech and Meieran [62].

stress in the semiconductor decreases proportionately. Thickening the Ti layer above 200 Å decreases the stress in the semiconductor because the expanding TiH_x layer is separated from the semiconductor by the non-expanding Ti layer.

The simple analytic model developed in 5.2.1.a holds for a very thin layer, but a real gate has a finite thickness. To the first order, the stress in the semiconductor results from the superposition of the stress induced by several thin layers stacked upon each other. A layer located further away from the semiconductor contributes to $-P_z(x=0,z)$ in a manner similar to the one shown in Fig. 5.5, but shifted to the left by the thickness of the underlying metal layer scaled by L_g. This can be seen in Fig. 5.12, which shows $-P_z(x=0,z)$ induced by thin layers at different distances from the semiconductor. If the thin layer is further away from the semiconductor, it induces a lower $-P_z(x=0,z=0)$, except when the thin layer is still very close to the gate-insulator interface. As a consequence, the stress distribution integrated over the full thickness of the gate decreases at a faster rate with increasing depth into the semiconductor.

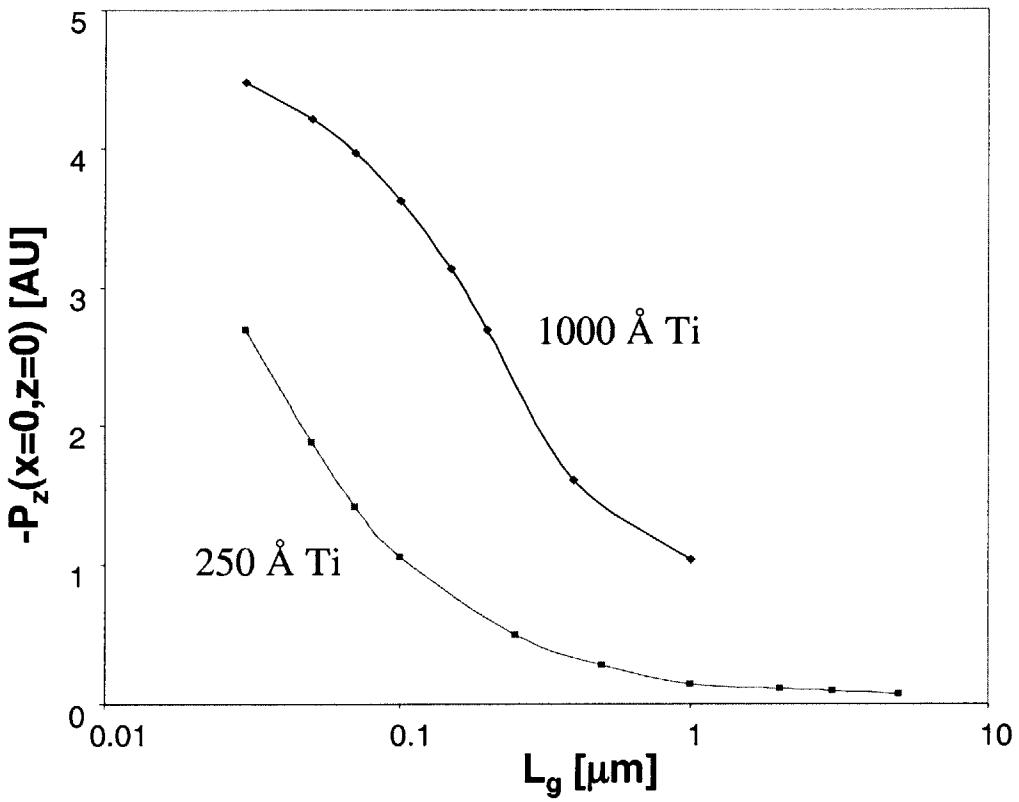

Fig. 5.13: $-P_z$ at the center of the gate at the gate-insulator interface, $-P_z(x=0,z=0)$, vs. L_g for the layer structure of Fig. 2.2 and a gate orientation parallel to [011] with a Ti thickness of 250 Å and 1000 Å.

$-P_z(x=0,z)$ is approximately proportional to the thickness of the expanding layer for thin layers. For thicker layers, the stress exerted by the upper layers on the top of the semiconductor is reduced significantly, as can be seen in Fig. 5.12. The rate at which this stress decreases with increasing depth scales inversely with L_g. Therefore, in short devices with thick expanding layers $-P_z(x=0,z=0)$ is not linearly proportional to the thickness of the expanding layer anymore, because the top part of the thick expanding layer does not induce as much stress in the semiconductor as the lower parts.

The calculations with ABAQUS show that $-P_z(x=0,z=0)$ and d_P depend on the thickness of the expanding Ti layer. Fig. 5.9 shows that d_P decreases slightly with an increasing thickness of the Ti. Fig. 5.13 shows $P_z(x=0,z=0)$ vs. L_g for HEMTs with a thickness of the expanding Ti layer of 250 Å and 1000 Å. Similar to the analytical model, a thicker layer causes the rate at which the stress decreases with depth to increase and $-P_z(x=0,z=0)$ stops scaling proportionally with thickness at shorter gate lengths. The findings of Figs. 5.9 and 5.13 are consistent with this simple analytical model.

Fig. 4.12 shows the calculated ΔV_T for an expanding layer thickness of 250 Å and 1000 Å. Because $-P_z(x=0,z=0)$ increases less than proportionally with thickness in shorter gates, ΔV_T decreases with decreasing gate length. In short devices, d_P is larger than z_i+z_c, but still small. Therefore, ΔV_T is proportional to $-P_z(x=0,z=0)$, which is significantly higher for devices with a thicker expanding layer, as can be seen on Fig. 5.13. For long devices, the heterostructure controls ΔV_T, though the magnitude of ΔV_T still scales with $-P_z(x=0,z=0)$.

5.2.3. Influence of the heterostructure

The design of the heterostructure affects how much V_T shifts for a given mechanical stress. Equation [2.21] states that to the first order the H-induced ΔV_T is proportional to the combined thickness of the insulator and channel, and to the difference between the average of $-P_z$ above the bottom of the channel, $\langle -P_z \rangle_{ins+chan}$ and the average in the buffer, $\langle -P_z \rangle_{buf}$. Both factors depend on the active device structure.

5.2.3.a. Insulator and Channel

The H-induced ΔV_T is to the first order linearly proportional to the combined thickness of insulator and channel. Thinning these layers has a proportional effect on ΔV_T. The material properties of the semiconductor set the piezoelectric polarization. The presence of material with a lower piezoelectric constant lowers $\langle -P_z \rangle$, and thus, the H-induced ΔV_T. An etch stop above the InAlAs insulator with a low piezoelectric constant, such as InP, reduces $\langle -P_z \rangle_{ins}$ significantly. This lowers the H-induced ΔV_T for devices of all gate lengths, as can be seen in Fig. 3.6.

The piezoelectric constant of InGaAs is lower than that of InAlAs, causing $\langle -P_z \rangle_{chan}$ to be smaller than $\langle -P_z \rangle_{ins}$ for all gate lengths. The average of $-P_z$ above the channel is given by:

$$\langle -P_z \rangle_{ins+chan} = \frac{z_i}{z_i + z_c} \langle -P_z \rangle_{ins} + \frac{z_c}{z_i + z_c} \langle -P_z \rangle_{chan} \qquad [5.18]$$

For short gate lengths, $-dP_z/dz$ is very high, therefore $<-P_z>_{ins+chan}$ is set by the value of $-P_z$ at the top of the InAlAs insulator and the ratio of z_i and z_c does not affect the H-induced ΔV_T much. For long devices, $-dP_z/dz$ is very small and according to equation [5.5], $<-P_z>_{ins+chan}$ decreases when z_c/z_i increases. As long as z_i+z_c remains constant, $<-P_z>_{buf}$ remains constant. When z_c/z_i increases, ΔV_T becomes more negative. This causes ΔV_T to flip signs at a shorter L_g.

5.2.3.b. Buffer

The H-induced ΔV_T is proportional to $<-P_z>_{ins+chan}-<-P_z>_{buf}$. In short HEMTs, $-dP_z/dz$ is so high that $<-P_z>_{buf}$ is negligible compared to $<-P_z>_{ins+chan}$. Therefore, the buffer has little effect on the H-induced ΔV_T. On the other hand, in long devices $<-P_z>_{buf}$ is of the same magnitude as $<-P_z>_{ins+chan}$. When the buffer is thinned $<-P_z>_{buf}$ increases because $-P_z$ decreases with increasing depth. Therefore, ΔV_T becomes more negative and changes sign at a shorter gate length. When the piezoelectric constant in the buffer is lowered, $<-P_z>_{buf}$ decreases and ΔV_T becomes more positive.

The influence of the buffer depends on the Fermi-level at the buffer-substrate interface. Fermi-level pinning has been observed at the buffer-substrate interface between InP and InGaAs, grown with MBE [50] and OMVPE [51]. In MOCVD grown material, the Fermi-level might not be pinned because of the improved interface quality caused by the etch-back before growth. The long HEMTs in Fig. 1.3 are fabricated using MBE, so the Fermi-level should be pinned at the buffer-substrate interface. The devices presented in Chapters 3 and 4 are grown with MOCVD, so the Fermi-level might not be pinned. The devices are not long enough to see the sign of ΔV_T change at a certain gate length, which would show if the Fermi-level is pinned or not.

5.3. Mitigating the H-induced piezoelectric effect

The H-induced ΔV_T can be mitigated through the design of the gate stack and the heterostructure. Engineering the gate is the most practical solution, since the device performance is highly dependent on the design of the active layers. But, some features in the heterostructure can help mitigate the H-induced ΔV_T without affecting the electrical characteristics.

Placing the gate parallel to [001] or removing the Ti layer in the gate eliminates the H-induced piezoelectric ΔV_T. These methods are not practical because of fabrication issues. The most practical way to reduce the H-induced ΔV_T is to separate the expanding TiH_x layer from the semiconductor where the piezoelectric charge is induced. This can be accomplished by putting a WSiN layer underneath the Ti layer as presented in Chapter 3, or by using a thick Ti layer as discussed in Chapter 4. The reduction of ΔV_T depends on the ratio of the thickness of the non-expanding layer to the gate length. With longer HEMTs, a thicker, non-expanding layer has to be used. WSiN underneath the Ti layer has additional benefits for device reliability and manufacturability [41]. By using WSiN as a Schottky metal, an InP etch stop layer can be used to improve the process control of V_T. WSiN is also thermally more stable than Ti. Using a thick Ti layer enables the use of the conventional Ti/Pt/Au gate stack. A thicker gate stack increases the gate resistance, limiting the practical reduction of the H-induced ΔV_T. It should be possible for most devices to use this technique to reduce the H-induced ΔV_T below 13 mV, which is the standard deviation of the V_T for different devices on a wafer.

If separating the TiH_x from the semiconductor reduces ΔV_T insufficiently, introducing InP in the insulator or channel can help. In future generations of HEMTs, as the channel and insulator thin [2], the H-induced ΔV_T should also be reduced. For longer devices, thinning the buffer reduces this reliability concern.

5.4. Summary

The model for the H-induced piezoelectric ΔV_T presented in Chapter 2 has several limitations that hinder quantitative modeling. But, the qualitative results are in excellent agreement with experimental observations. The 1D electrostatics model that is used to compute ΔV_T is found to be sufficient because the 2D effects do not affect the results of the model in the [011] orientation and the model may overestimate the H-induced shift in the $[01\bar{1}]$ orientation.

The model explains how the H-induced ΔV_T depends on the different aspects of device design. In short devices the H-induced ΔV_T is approximately proportional to the maximum polarization in the insulator. In longer devices, the H-induced ΔV_T is set by the heterostructure and the depth distribution of the polarization at the center of the gate. The structure of the gate affects the mechanical stress distribution in the semiconductor. Which sets the piezoelectric polarization in the semiconductor. By separating the expanding Ti layer or by making the gate more rigid, the stress in the semiconductor is reduced. This reduces ΔV_T significantly in short HEMTs and less in devices with a long gate length. The heterostructure controls how much the piezoelectric charge shifts ΔV_T. ΔV_T is proportional to the combined thickness of the channel and insulator. When the ratio of the channel thickness to the insulator thickness increases or the buffer thins, ΔV_T becomes more negative in the [011] orientation.

The H-induced ΔV_T can be eliminated by removing the Ti layer out of the gate stack or by orienting the gate parallel to [001]. But technological reasons make these solutions impractical. The most practical solution is to separate the expanding Ti layer from the semiconductor with a non-expanding layer. This can be done using a thick Ti layer, since only the top layer forms TiH_x or by putting a thick WSiN layer under the gate. The required thickness of the non-expanding layer is proportional to the gate length. Thinning the channel and insulator, or using a material with a low piezoelectric constant above the buffer-channel interface can help mitigate the H-induced ΔV_T.

Chapter 6

Conclusions

This chapter summarizes the important findings of this thesis. First, the development of the model for the H-induced ΔV_T is presented. This model helps understand how the H-induced ΔV_T depends on the gate structure and the heterostructure. The most important findings are summarized later. The chapter continues with proposals for practical device level solutions to the H-induced piezoelectric ΔV_T and finishes with some suggestions for future work.

6.1 The H-induced piezoelectric ΔV_T and its model

Blanchard presented the physical degradation mechanisms behind the H-induced ΔV_T in InP HEMTs. Two degradation mechanisms existed. One mechanism causes a small, negative ΔV_T, independent of the gate length and gate orientation. This thesis did not study this degradation because the shift is small and has no reported dependence on device design. A second H-induced ΔV_T mechanism has been observed to induce large shifts up to 150 mV highly dependent on gate length and orientation. This mechanism is caused by the absorption of H by formation of TiH_x in the Ti layer in the gate stack. This reaction is aided by the Pt layer which helps split the molecular H_2 into H. The formation of TiH_x causes an expansion of the Ti layer, which exerts a mechanical stress in the semiconductor. Since the material is piezoelectric, a polarization charge is induced,

which shifts V_T. The main goal of this thesis was to construct a detailed model of this mechanism that would allow the development of device level solutions to this problem.

A two-dimensional finite element mechanical simulation tool, ABAQUS, was used to calculate the mechanical stress in the semiconductor that is caused by an expanded Ti layer. This mechanical stress is then used to calculate the piezoelectric polarization charge in the semiconductor. The H-induced ΔV_T is subsequently calculated using a 1D electrostatics model at the center of the gate. In this model, the H-induced ΔV_T is to the first order proportional to the depth of the inversion layer, and to the difference between the average of $-P_z$ above the bottom of the channel, $\langle -P_z \rangle_{ins+chan}$ and the average in the buffer, $\langle -P_z \rangle_{buf}$.

This model was used to investigate how ΔV_T depends on the different aspects of device design. Where possible, the theoretical results of the model were tested experimentally on devices, supplied by industrial partners. The following section summarizes how the design of the gate structure influences the stress in the semiconductor and thus the H-induced ΔV_T.

6.1.1 Impact of gate design

The gate orientation influences the piezoelectric polarization in the semiconductor. On a (100) surface, a gate orientation parallel to [001], there is no ΔV_T. However, devices with a gate orientation parallel to [011] or [01$\bar{1}$], which are the gate orientations that are used. A 90° shift in gate orientation, switches the sign of ΔV_T.

The gate stack sets the mechanical stress in the semiconductor. The polarization at the gate-insulator interface scales inversely with gate length, while the penetration depth of the polarization scales with gate length. This implies that, except for very short gate lengths, ΔV_T scales inversely with gate length and is positive for devices in the [011] gate orientation. In long devices, ΔV_T is mainly controlled by the heterostructure, and becomes negative, decreasing when the gate becomes longer. This is consistent with the experimentally observed ΔV_T from Fig. 1.3.

When WSiN is used as the Schottky gate, this thick non-expanding layer separates the TiH_x layer from the semiconductor. This reduces the stress proportionally to the ratio of the thickness of the non-expanding layer to the gate length. This causes the piezoelectric ΔV_T to be reduced significantly in very short devices. This was experimentally verified using InP HEMTs fabricated by NTT.

The model predicts that a thick Ti layer would induce a very large piezoelectric ΔV_T in short devices. Experimental observations on InP HEMTs, fabricated at NTT, showed very small ΔV_T, similar to the degradation observed in InP HEMTs with a WSiN Schottky gate. This was explained by the diffusion mechanism of H in TiH_x. H diffuses in Ti, using the same interstitials it occupies in TiH_x. Therefore TiH_x acts as a diffusion barrier for H and TiH_x only forms in the top 200 Å of the Ti layer. Auger Electron Spectroscopy measurements verified this experimentally. Therefore, the non-reacting Ti underneath the TiH_x layer separates it from the semiconductor and reduces ΔV_T, similar to the WSiN layer.

6.1.2 Impact of heterostructure design

The heterostructure influences how much V_T shifts for a certain polarization charge. ΔV_T is proportional to the combined thickness of insulator and channel, and as those are becoming thinner in future HEMT generations [2], the H-induced ΔV_T should reduce as well.

The heterostructure plays a very important role in setting ΔV_T in long devices. In devices with a gate orientation parallel to [011], ΔV_T becomes more negative when the thickness of the channel increases compared to the insulator thickness or, when the buffer is thinned. Using a material with a low piezoelectric constant in the channel or insulator, reduces ΔV_T.

Some HEMTs were experimentally observed to be insensitive to H. The physical understanding behind the small H-induced ΔV_T in these devices leads to several device level solutions to the H-induced ΔV_T.

6.2 Device level solutions

The H-induced ΔV_T depends strongly on the device design. Shifts of a few hundred mV have been experimentally observed. But, the experimental observations of Chapters 3 and 4 have shown that ΔV_T can be reduced significantly.

The design of the gate stack and the heterostructure can mitigate the H-induced piezoelectric effect. The most practical solution is to engineering the gate to reduce stress in the semiconductor, since design of the heterostructure influences device performance. Some characteristics of the active device can also help reduce the H-induced ΔV_T.

Fabrication issues hinder elimination of the H-induced piezoelectric ΔV_T by placing the gate parallel to [001] or all together removing the Ti layer in the gate. The most practical way to reduce the H-induced ΔV_T is to reduce the stress in the semiconductor by separating the expanding TiH_x layer from the semiconductor using a WSiN layer, or any other suitable metal, underneath the Ti layer. Using WSiN as a Schottky gate has added reliability benefits. The reduction of the stress is proportional to the ratio of the WSiN thickness to the gate length. Since a thicker gate stack increases the gate resistance, the practical reduction of the H-induced ΔV_T is limited. When the gate becomes too thick it starts affecting device performance. The H-induced ΔV_T can be reduced below a workable value for most devices by increasing the thickness of the non-expanding layer below the Ti layer. If not, introducing InP in the insulator or channel can help. The roadmap of future HEMT technology predicts that the channel and insulator become thinner [2], thereby reducing the H-induced ΔV_T. In long devices, this reliability issue can be reduced by thinning the buffer.

6.3 Suggestions for future work

As a result of this thesis, the effects of H on the V_T of InP HEMTs are well understood and device level solutions have been proposed. H has been observed to degrade other device figures of merit, but these effects are relatively small. The small H-induced increase in parasitic resistance is very small compared to other degradation of the parasitic resistance that has been observed [4], while the concurrent increase in off-state breakdown voltage [37] is beneficial to the device. However, some questions are still unsolved. A second degradation mechanism that was identified in a few of the InP HEMTs with a thick Ti layer in the gate from Chapter 4 is still not well understood. It was linked to a processing issue, so it might not be very interesting to study since it might not be present in well designed devices. There is great uncertainty about the exact details of the formation of TiH_x. It would be interesting to have a better measurement of the exact TiH_x profile and the amount of expansion.

The influence of other atmospheric conditions on HEMTs have not been studied systematically. The influence of moisture at higher temperature definitely warrants a systematic study. The chemistry of III-V semiconductors and the gate stack has been shown to be reactive with a wide set of elements [4]. The influence of air on InP HEMTs would also be an interesting study, since air contains elements that have proven to affect InP HEMTs, such as H and F. While, it is unlikely that all degradation that has been seen in air [4] can be explained by reactions with H and F or the other elements that have been studied extensively.

There are plenty of other reliability issues with InP HEMTs that warrant systematic study. The thermal stability of the gate and its effects are not well understood. Some designs use Pt/Ti/Pt/Au gates in which the lowest layer of Pt is thermally driven into the insulator [63]. The lower Ti layer itself is also known to sink into the InAlAs layer [4]. The combination of bias, atmosphere and a gate sunk into the insulator could create serious reliability problems.

I think it is crucial for the HEMT technology to place a higher emphasis on reliability instead of developing new designs to keep improving performance. Even the most basic building blocks of the HEMT technology, such as the ohmic contacts and the Ti/Pt/Au gate are prone to degradation. Despite this, few groups publish about the development of

reliable ohmic contacts and gates. The evolution of the material systems that are used in HEMTs is too fast for reliability concerns to be systematically studied. Several reports about reliable devices show high reliability under well-chosen conditions of bias, atmosphere and burn-in conditions. There is great value in reporting high reliability under a given set of conditions. But by establishing the conditions at which reliability breaks down, further improvements can be made. A greater effort on resolving the reliability issues instead of trying to gain a new device performance record is necessary should HEMTs gain their potential.

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