Gain Compensated Sample and Hold

by

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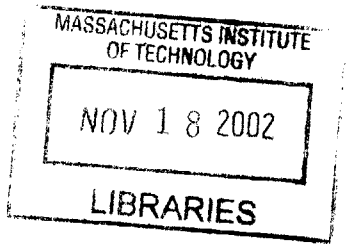

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Abstract

Modern scaled CMOS processes present challenges to the design of analog and mixed signal systems. Lower output resistance, reduced power supply voltage, increased threshold variation and gate leakage all make effective analog design more difficult. The design of high gain op-amps is one analog design challenge made more difficult by the continued scaling of CMOS. Low gain op-amps create errors in sample and holds and gain stages that limit the performance of analog and mixed signal systems. We propose the development of a circuit technique that reduces the gain error in gain stages and in sample and holds. The effective gain of the op-amp will be consequently enhanced by this technique. The proposed technique involves using a prediction of a desired output to aid an op-amp in settling more accurately. The design and fabrication of a sample and hold using the technique validates the utility of the technique.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

Modern scaled CMOS processes have been optimized for digital circuits. Process advances such as lower power supplies and shorter gate lengths which lead to lower power, faster digital circuits may also lead to higher power, lower performance analog circuits. Although the higher f_Ts of scaled devices can be used to increase analog performance, other process characteristics such at increased gate leakage, subthreshold leakage and threshold mismatch along with lower power supplies all make analog design more difficult.

The trend toward decreasing transistor length and supply voltage make the design of high gain opamps with large output swing very difficult. Low frequency opamp gain fundamental limits the accuracy of mixed signal systems such as analog to digital converters. The objective of this work is to develop a gain compensation technique that will reduce the detrimental effect of low opamp gain on the accuracy of switched capacitor circuits.

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1.1 Thesis Objectives

The focus of this work is on the development of a gain compensation technique. Specifically a finite gain compensated sample and hold is designed. The sample and hold is designed in a way such that it is compatible with lower supply voltages. The

effect of the gain compensation is seen by comparing the gain error of the sample and hold to what it would be in a traditional sample and hold using the same opamp.

1.2 Thesis Motivation

The persistent advance of CMOS process technology which has enabled unprecedented performance advancement of digital integrated circuits has also created many new challenges in the design of analog integrated circuits. Analog designers have been able to overcome the challenges of modern CMOS technology in order to take advantage of its inherent advancement. As we continue to scale CMOS this will become more and more difficult.

One of the most important design challenges posed by CMOS scaling is the design of high gain operation amplifiers (opamps). Opamps are essential analog building blocks. Analog blocks in integrated systems be they switched capacitor or continuous time circuits are limited by the performance of the opamps that they contain. Often the gain of the opamp will limit the accuracy of the analog system and the opamp's bandwidth will limit its speed. One specific example is the pipeline analog to digital converter. The gain of opamps contained in the input sample and hold as well as the pipeline stages will directly limit its accuracy.

Two aspects of CMOS scaling are increasing the difficulty of designing high gain opamps: smaller gate length and reduced supply voltage.

The ever shrinking gate length of modern CMOS devices is the heart of CMOS scaling. It enables faster smaller digital circuits. It also lowers the output resistance (r_o) of a transistor. Since the $g_m \times r_o$ product of a transistor fundamentally limits the gain of any amplifier, scaled devices will produce lower gain opamps. This effect can potentially be negated by using longer than minimum length devices in a design. Unfortunately a transistor's speed (f_T) is inversely proportional to its length. If you wish to take advantage of a scaled technology's increased high frequency capability you must use a small gate length. Also Buss shows in[2] that the output resistance of a modern digital device does not increase significantly with increasing length. Digital

devices below .25μm need to be doped with a pocket implant in order to control DIBL. This implant significantly reduces output resistance at longer channel lengths. For a 10μm device the early voltage of a device with a pocket implant is seven times lower than a device without the pocket implant.

Reduced supply voltages are both a feature and requirement of scaling. Using a lower supply voltage enables lower power consumption in digital circuits, but it is also a requirement of using scaled devices. In order to maintain gate control over very small devices it is required that one uses a very thin gate oxide. A low supply voltage must be used in order not to damage this oxide or cause break down in the channel. Unfortunately in analog circuits a lower supply voltage usually leads to higher power for a similarly performing circuit. This occurs because a lower supply voltage leads to a lower output swing. The signal to noise ratio decreases as the maximum amplitude of the output signal decreases. In order to maintain the signal to noise ratio capacitor sizes must be increased to reduce $\frac{kT}{C}$ noise. The power consumption of the circuit must be increased if one wishes to drive the larger capacitors at the same speed as the original circuit.

In order to achieve reasonable gain in an amplifier designed in a scaled technology it is often necessary to cascode transistors. A cascoded topology using a reduced supply voltage suffers from drastically reduced voltage swing. Reduced voltage swing translates directly into a lower signal to noise ratio. The only way to compensate for this is by decreasing the noise in the circuit. This requires an increase in power consumption.

If one uses cascoding only in amplifier stages before the output stage the output signal swing will not be reduced, but as supply voltage continues to decrease it will become increasingly difficult to keep any cascoded transistors in saturation. When the supply voltage is not large enough to enable cascoded designs designers will have to use other techniques in order to make high gain opamps using scaled devices.

This work attempts to address the problem of low opamp gain in scaled CMOS. A new gain compensation technique is proposed which compensates for low opamp gain. This technique is applicable to a large class of switched capacitor circuits. Any

switched capacitor circuits using sample and holds or gain stages can benefit from the proposed technique. Unlike other techniques, the proposed technique does not limit the speed of the circuit to which it is applied. The utility of the technique is tested through its implementation in a sample and hold.

1.3 Thesis Organization

This thesis will begin with a discussion of gain compensation techniques in chapter 2. The basic theory of gain compensation, previous gain compensation techniques as well as the proposed technique will be covered. The third chapter will cover opamp design. Some general comment will be made and the opamp used in the finite gain compensated sample and hold will be described in detail. The fourth chapter contains a discussion of other issues involved in the design of the sample and hold. The fifth chapter contains simulation results and a discussion of them. The layout of the sample and hold is described in the sixth chapter. Measurement technique is in the seventh chapter. Finally, conclusions are made in the eighth chapter.

Chapter 2

Gain Compensation Techniques

Gain Enhancement techniques counteract the negative effect that low gain opamps have on circuit performance

2.1 Gain Enhancement Theory

Any opamp with a gain less than infinity will create a gain error when used in a sample and hold or gain stage. This can been seen in figure 2-1. In the case of an opamp in unity gain feedback the output will always be less than the input by the output value divided by the gain of the opamp.

More exactly the output will follow the input in the following way

$$V_{out} = \frac{1}{1 + \frac{1}{A_o}} V_{in} \cong (1 - \epsilon) V_{in} \tag{2.1}$$

It can be see from this equation that the gain error is approximately

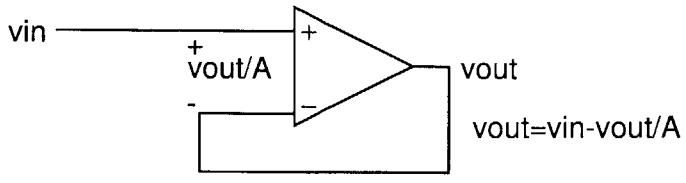

Figure 2-1: Gain Error of Unity Gain Buffer

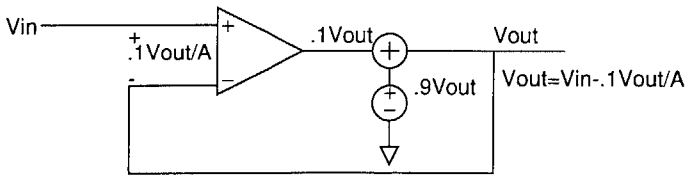

Figure 2-2: Gain enhanced unity gain buffer

$$\epsilon = \frac{1}{A_o} \tag{2.2}$$

In general the output of an opamp in feedback in the inverting configuration will follow the input by

$$V_{out} = -\beta(\frac{1}{1+\frac{1+\beta}{A}})V_{in} \cong -\beta(1-\epsilon)V_{in} \tag{2.3}$$

Where β is the ideal gain. The gain error will be approximately the inverse of the loop gain, $L(s)$.

$$\epsilon = \frac{1+\beta}{A} = \frac{1}{Af} = \frac{1}{L(s)} \tag{2.4}$$

The loop gain $L(s)$ is the product of the open loop gain A and the feedback factor f.

2.2 Gain Compensation

Most gain compensation techniques have the same principle of operation. They use a prediction of the an opamp's output to enable the opamp to settle more accurately. This technique is demonstrated in figure 2-2 for the case of the unity gain buffer

Before the unity gain buffer is evaluated a prediction of the output voltage that is 90% of the final value is generated. This predicted value is summed with the output of the opamp to produce the final output value. The input voltage to the opamp is smaller than in the case of a regular unity gain buffer because the output of the

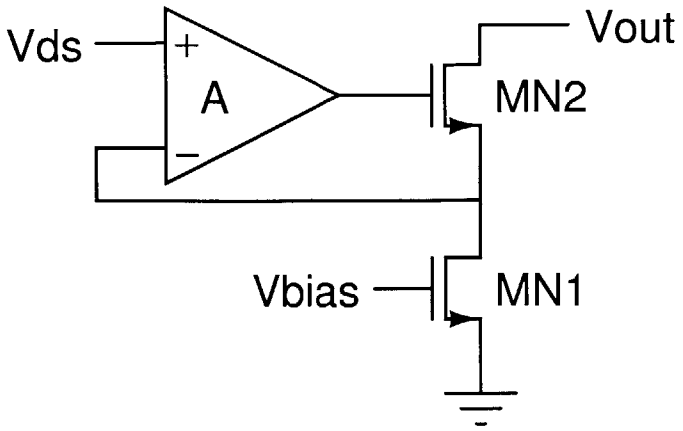

Figure 2-3: Regulated Cascode

opamp itself is smaller. The error voltage is decreased by the same amount as the output of the opamp.

$$\epsilon_E = \frac{.1}{A_o} \tag{2.5}$$

The effective gain of the opamp is increased since the error voltage is reduced.

$$A_E \cong \frac{1}{\epsilon_E} = 10 \cdot A \tag{2.6}$$

2.3 Previously Proposed Techniques

The challenge of designing high gain opamps has lead to the development of many gain compensation techniques. The regulated cascode[1] , an extension of traditional opamp design enhances the inherent gain of the opamp. Yu's [11] technique involved the use of an auxiliary amplifier to increase the gain of a single amplifier. Haug's technique [5] enhanced gain by cancelling an opamp's input voltage. Nagaraj's [9] and Larson's[8] techniques used a prediction of the output to enhance gain. Huang's [10] [6] [7] techniques provide gain compensation without significantly sacrificing speed.

The regulated cascode shown in figure 2-3 increases the gain of an opamp by increasing the output resistance of a cascode. The output resistance is

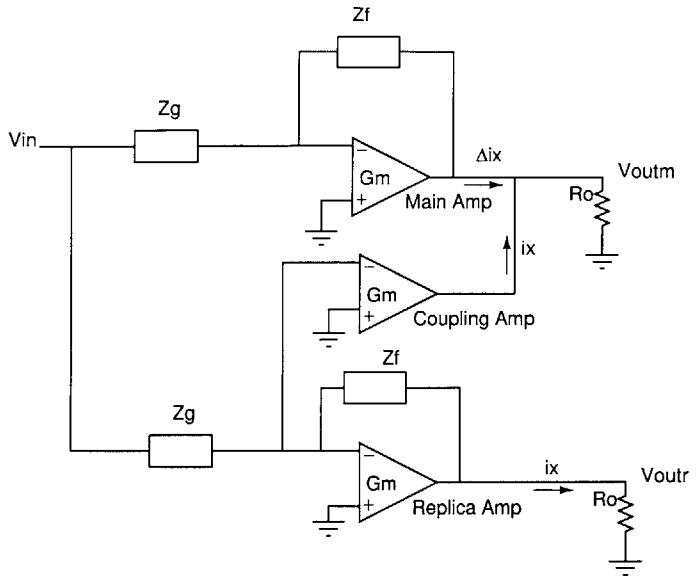

Figure 2-4: Gain compensation technique using a replica amplifier

$$R_o = A \cdot g_m \cdot r_{o2} \cdot r_{o1} \tag{2.7}$$

The opamp keeps the drain to source voltage of MN1 constant so the output resistance is increased.

Yu's technique involves using a replica amp to increase the effective gain of a single amp. The same input is fed to both amplifiers. The replica amp puts the current i_x into its output resistance needed for the stage to reach close to final value. The coupling amp injects this current into the main output resistance. The main amp then only needs to provide a small amount of current Δi_x. The input voltage on the main needed to support this smaller amount of current is

$$V_{errorE} = \frac{\Delta i_x}{g_m} \tag{2.8}$$

This voltage is much smaller that what would be required without the gain compensation

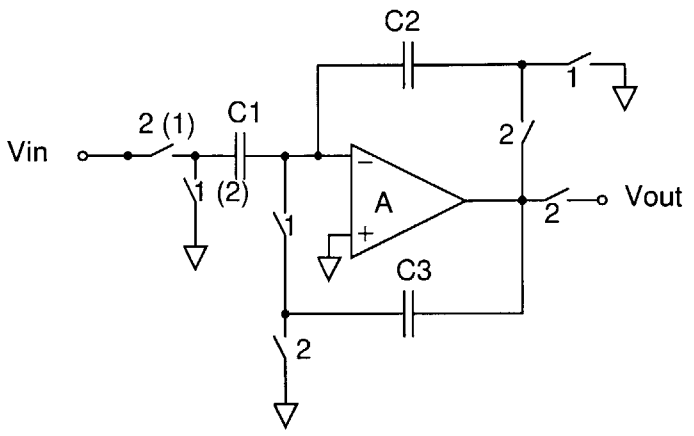

Figure 2-5: SC amplifier with input voltage cancellation gain enhancement

$$V_{error} = \frac{i_x}{g_m} \tag{2.9}$$

This gain error ideally will be reduced by a factor equal to the loop gain of the replica amp.

$$\epsilon_i = \frac{1+\beta^2}{A_o} \tag{2.10}$$

In reality the amount of gain compensation is limited by the matching between the output resistances of the two amplifiers.

$$\epsilon_r = \frac{1+\beta}{A_o}\frac{\Delta r_o}{r_o} \tag{2.11}$$

This gain compensation scheme slows down the settling of the opamp by approximately 30% because the two amplifiers must settle simultaneously.

Haug's technique(figure 2-3) enhances gain by cancelling the input voltage of the opamp. The amplifier in figure 2-3 is inverting if the phases outside the parentheses are used and non-inverting if the phases inside the parentheses are used. Taking the non-inverting case, during the first phase C_1 samples the input. The desired output is reached within the gain error during the second phase as C_1's charge is transferred to C_2. The output voltage remains on the opamp's output and input voltage needed

to produce this output remains on the input as the next phase one starts. During this next phase one, C_1 samples the difference between the input and the input voltage of the opamp. As the amplifier enters the second phase two the input voltage and the offset voltage of the opamp are cancelled and the final output value is reached. Enough charge is transferred to C_2 so that the voltage across it is

$$V_{C_2} = V_{in} + \frac{V_{in}}{L(s)} \tag{2.12}$$

This is enough voltage to raise the output to V_{in} because the left side of C_2 is at

$$-\frac{Vin}{L(s)} \tag{2.13}$$

Where L(s) is the loop gain. This assumes that the input voltage does not change during the circuit's operation. The final output value follows the input by

$$V_{out} = \beta(\frac{1}{1 + \frac{1+\beta}{A_o}})V_{in} \cong \beta(1-\epsilon)V_{in} \tag{2.14}$$

The gain error is therefore

$$\epsilon = \frac{1 + \frac{C_1}{C_2}}{A_o^2} \tag{2.15}$$

For the case of a unity gain buffer the gain will be enhanced by a factor equal to the gain of the opamp divided by two. The gain compensation capability of this technique depends on the input not changing much between two successive phase ones. If the input changes the circuit will not cancel the correct input to the opamp. This places a severe limitation on the allowed input frequency range. If the input frequency reaches 25% of the clock frequency all of the gain compensation is lost [5]

Nagaraj [9] and Larson [8] designed very similar circuits that enhance gain by predicting the output of the gain stage. Nagaraj's circuit (figure 2-6) consists of two inverting stages that operate on opposite clock phases. During the first phase a prediction of the output is created and the opamp input voltage needed to support this predicted value is sampled on Ci. During the second phase the voltage at node

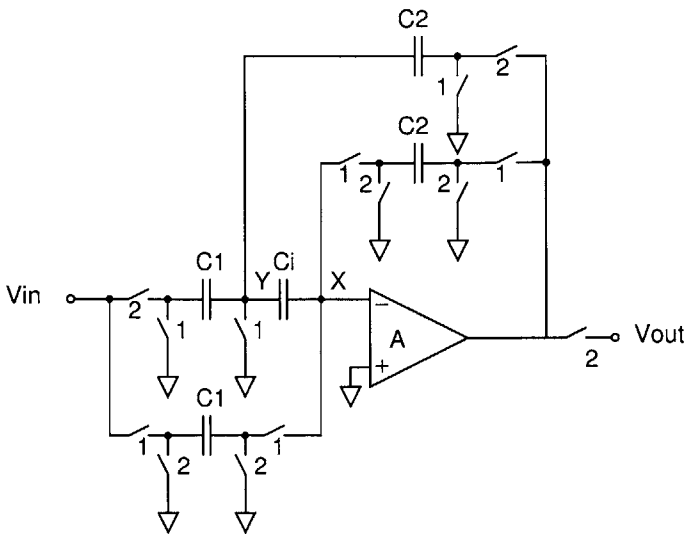

Figure 2-6: Nagaraj's Predictive Gain Compensation Circuit

Y does not have to move much for the output to reach its final value because the voltage across Ci is keeping the voltage of node X where it needs to be. The voltage at node Y is the gain error of the circuit. Since this voltage will be much less that the voltage at node X the gain error is reduced. If the input to the circuit is the same during phase one and two the gain error is the square of the inverse of the loop gain:

$$\epsilon = \frac{1 + \frac{C_1}{C_2}^2}{A_o} \tag{2.16}$$

If the inputs are not the same during phase one and two the gain error will increase because Ci will not hold the value needed to keep node Y from changing. The gain error will be

$$\epsilon = \frac{1 + \frac{C_1}{C_2}}{A_o^2} X((1 + \frac{C_1}{C_2} + \frac{C_i}{C_2})V_{out}(n) - \frac{C_i}{C_2}V_{out}(n-1)) \tag{2.17}$$

$V_{out}(n-1)$ is the output during phase one and V_{out} is the output during phase two. As in Haug's circuit the circuit's performance will be reduced as the input frequency rises. The effect will not be as bad as in Haug's circuit because the input only needs to be constant for two phases rather than four.

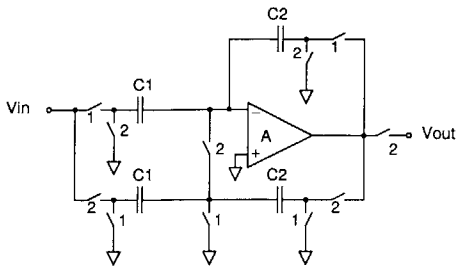

Figure 2-7: Larson's Predictive Gain Compensation Circuit

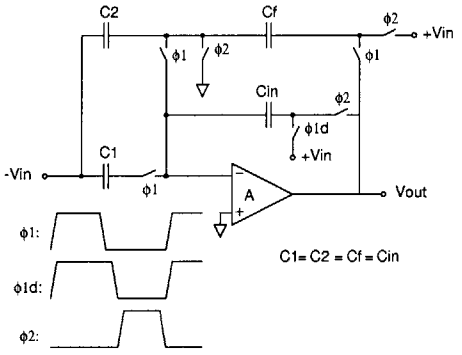

Figure 2-8: Huang's Finite Gain Compensated Track and Hold

Larson's [8] circuit is very similar to Nagaraj's except for the fact that the upper C1 and C2 provide the function that Ci did in Nagaraj's circuit.

Huang [10] [6] [7] designed two track-and-hold circuits which provide gain compensation for input frequencies up to half the sampling rate.

The first track-and-hold compensates for low gain by sampling the gain error on C_{in}. During ϕ_1 C_2 and C_f form an inverting buffer. C_1 cancels the charge sent to the summing point by C_{in} thereby eliminating the effect of the $+V_{in}$ applied to C_{in} on the output. Also during ϕ_1 the gain error and offset are sampled on Cin.

$$v_{cin} = v_{in} - V_{off} + \frac{v_{in}}{A} \tag{2.18}$$

As ϕ_2 goes high the right side of C_{in} is switched to the output node and the output voltage becomes.

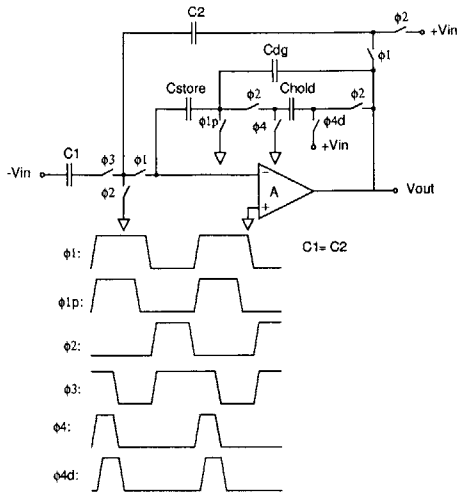

Figure 2-9: Huang's Improved Finite Gain Compensated Track and Hold

$$v_{out} = V_{off} - \frac{v_{out}}{A} + v_{cin} = v_{in}(1 + \frac{1}{A}) - \frac{v_{out}}{A} \tag{2.19}$$

The offset and gain error stored on C_{in} cancel the amplifier's offset and gain error. In fact the gain error is not completely cancelled. The gain compensation increases the effective gain by the loop gain during ϕ_1. Since the three capacitors are connected to the input the feedback factor is $\frac{1}{4}$ and the loop gain is $\frac{A}{4}$. The noise gain from the input to the output of the opamp is consequently 4 during ϕ_1. During ϕ_2 C_f and C_2 are precharged to a value close to what they will see during the next ϕ_1 period. This limits opamp slewing and improves settling time.

Huang's improved track-and-hold produces a similar result as his original proposal, but in a more complicated way. In this circuit the gain error is sampled on C_{store} during ϕ_1. C_{store} is then place in series with C_{hold} and the gain error is cancelled. A third phase has been added to this circuit in order to reduce the capacitance connected to the input of the opamp during settling and to cancel the gain error at DC. A large input capacitance will load the output of the opamp and slow settling. In this circuit when ϕ_4 goes low the capacitors are disconnected from the input and the circuit is allowed to settle. Also when ϕ_4 goes low the circuit stops tracking the input and settles on an unchanging value. This allows C_{store} to capture the gain error of the

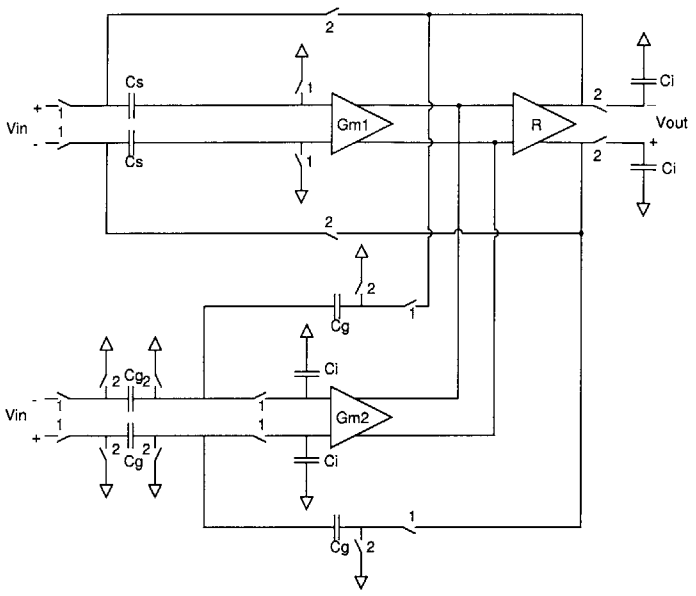

Figure 2-10: Gain Enhanced Sample and Hold

opamp at DC. This gain error more closely approximates the actual gain error than an error derived from the gain at a higher frequency.

2.4 The Proposed Technique

The gain compensation technique is used in the sample and hold in figure 2-3. The sample and hold consists of a traditional sample and hold in its main path and inverting gain stage in its prediction path. The inverting gain stage is fed the inversion of the input during phase1. At the same time the sample and hold is fed the input. The inverting gain stage produces a prediction of the output value during phase 1 while the input is sampled on Cs. Assuming all of the Cg capacitors were cleared in the previous phase the predicted output value is accurate to within the gain error of the prediction path. The Ci capacitors hold the input on the auxiliary inputs during phase 2 so that Gm2 provides most of the current needed to reach the final output value. Gm1 needs to only to provide enough current to move the output from the predicted output to the final output value. In this way the input to Gm1 and

consequently the sample and hold's gain error is very small. Also during phase 2 the capacitors in the predictive path are cleared. The output will follow the input by

$$\frac{V_{out}}{V_{in}} = \frac{1+\frac{3}{A_o}}{1+\frac{3}{A_o}+(\frac{2}{A_o})^2} > \frac{1}{1+\frac{2}{A_o^2}} \tag{2.20}$$

The resulting gain error of the sample and hold is the product of the gain errors of the main and predictive paths.

$$\epsilon < \frac{2}{A_o^2} \tag{2.21}$$

The gain error is reduced by a factor equal to the loop gain of the predictive path. The effective gain of the opamp is product of the loop gain of the main and predictive paths. Assuming that the main and predictive paths have the same gain. The effective gain will be increased by a factor equal to the gain of the opamp divided by two.

$$A_{eff} = \frac{1}{\epsilon} = \frac{A_o^2}{2} \tag{2.22}$$

The gain compensation technique does not significantly limit the allowed frequency range of the input. A regular switched capacitor sample and hold needs two phases to complete its operation. In only one of these phases is the opamp used. The sampling occurs on the first phase and the evaluation on the second phase. In the same way the inverting configuration only needs the opamp for one of two phases. In the first phase its capacitors are cleared and in the second phase it samples the input and evaluates. This allows us to stagger the operation of the main and predictive paths in such a way that they sample the input at the same time, but use the opamp at different times. The fact that the two paths sample the input at the same time ensures that as in a regular sample and hold the input can have a frequency up to half of the clock frequency. Also because the basic operation of the sample and hold is not changed, the sample and hold will not take longer to settle. Unlike Yu's technique only one amplifier is settling at a time. The predictive path does not slow down the settling

of the main path.

In fact the performance of the circuit will be somewhat dependent on the frequency of the input. Since the sample and hold can sample the input faster than the inverting gain stage they will not be sampling the exact same value. Making the inverting gain stage settle very quickly can minimize this effect. This is possible because the predictive path does not have to drive as large a load as the main path.

Mismatches between the two paths will not severely limit the gain compensation. Unlike Yu's implementation the proposed technique does not use two separate opamps but rather two transconducting stages and a common output resistance. In this way output resistance mismatch does not limit the compensation.

The input referred offset will also be decreased by the compensation. The gain compensation technique is very similar to the offset cancellation technique created by Vittoz[3]. The offset is therefore decreased in the same way. The final offset is

$$V_{off} = \frac{V_{off1}A_o + V_{off2}A_o}{(1+A_o)(1+\frac{A_o}{2})} \cong \frac{V_{off1} + V_{off2}}{\frac{A_o}{2}} \tag{2.23}$$

The gain compensation reduces the offset by the loop gain of the predictive path. This is the same as in the standard auxiliary input offset cancellation technique[3]. The offset will be twice what you would get from the standard technique because the predictive path is in the inverting configuration rather than in unity gain configuration.

2.5 Advantages of the Proposed Technique

The proposed technique has an inherent speed advantage over all other previously proposed techniques. All of the techniques proposed before Huang's have predictive and evaluative circuits that sample on different phases. This naturally limits the speed that the circuit can work at. Haung's circuit avoids this limitation, but still has a limited speed of operation. The input used in the evaluation phase is sampled on a capacitor that is connected to the opamp. Therefore the speed at which the circuit samples is limited by the settling time of the opamp. This settling time could be quite

long because the opamp is in feedback with a feedback factor of $\frac{1}{4}$. In the proposed technique the sampling for the evaluation phase is done with respect to ground. This is a very fast operation which does not limit the opamp's sampling rate. While the input is sampled to ground the opamp is settling to the predicted output value. It is not critical that the opamp settles fully during the phase because only a prediction of the output is produced on the final precise output. One advantage that Huang's technique has over the proposed technique is that it does not require any extra inputs. Therefore is consumes less power. The proposed technique's power consumption can be minimized by scaling the auxiliary inputs and the capacitors used in the inverting buffer.

Chapter 3

Op-Amp Design

Gain Enhancement techniques counteract the negative effect that low gain opamps have on circuit performance

3.1 Op-Amp Design Overview

A two stage op-amp topology was chosen to demonstrate the proposed gain compensation technique so that the sample and hold would be portable to low supply voltage technologies. The two-stage topology has the largest output voltage swing of any topology. The output swings of the major topologies are summarized in table 3.1

A large output swing ensures that a circuit has an acceptable dynamic range even as the power supply voltage is scaled. The first stage of a two stage amplifier can optionally be cascoded. In a cascoded two stage the first stage consists of a five transistor stack. The designer can reduce the voltage needed to saturate these transistors

Opamp	Swing
Two Stage	$2V_{dd}$-$2V_{ds,sat}$
Folded Cascode	$2V_{dd}$-$8V_{ds,sat}$-$4V_{margin}$
Current Mirror	$2V_{dd}$-$8V_{ds,sat}$-$4V_{margin}$
Telescopic	$2V_{dd}$-$10V_{ds,sat}$-$6V_{margin}$

Table 3.1: Output swing of different opamp architectures.

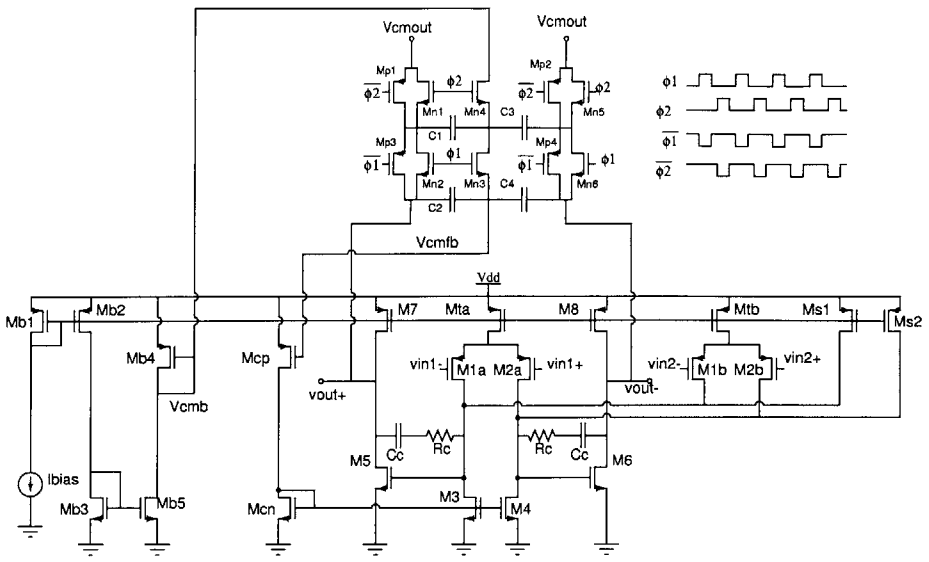

Figure 3-1: Two Stage Four Input Op-Amp

by biasing them in weak inversion. Eventually a minimum V_{ds} of approximately 100mV per device is reached. This limits a cascoded topology to power supplies of at least a half a volt. Also a topology which forces all the transistors to operate in weak inversion limits the designer's options and could lead to unacceptable mismatches. A non cascoded topology allows for minimum voltage supply operation. The proposed sample and hold is designed using a basic non-cascoded two-stage op-amp. The details of the opamp are described in the rest of the chapter. The op-amp schematic is seen in figure 3-1. Notice that is has two sets of inputs in order to allow it to be used in the proposed sample and hold.

3.2 Two Stage Opamp

The opamp as seen in Figure 3-1 is a standard two stage opamp with Miller compensation. The only way it differs from a basic opamp is that it has an extra input pair and extra tail current source. The extra input pair requires that the first stage NMOS load must have double the width in order to handle the doubled current.

The opamp was designed to settle quickly, but not necessarily to have the maxi-

mum possible DC gain. This was done so that the utility of the gain compensation technique could be shown. The settling time constant of the opamp under feedback is:

$$\tau = \frac{f}{\omega_u} = \frac{1}{\omega_u}\frac{C_f + C_s + Ci}{C_f} \tag{3.1}$$

Were ω_u is the unity gain frequency, f is the feedback factor and C_f, C_s, Ci are the feedback capacitor, the sampling capacitor and the capacitor at the opamp input respectively.

The transistors are operated with a large amount of current to prevent slewing and to produce a maximum unity gain frequency. Assuming a dominate pole system, the unity gain frequency is given by:

$$\omega_u = \omega_{p1} \times A = \frac{g_{m1}}{C_c} \tag{3.2}$$

The transconductance of the input pair is maximized by using wide devices and a large bias current. The compensation capacitor is set at the smallest value possible while maintaining an acceptable phase margin.

As can be seen in Figure 3.2 NMOS's in the second stage were also made wide in order to achieve high transconductances. This was done in order to produce a large DC gain for a given unity gain frequency and to push the non-dominant pole to a high frequency.

$$A = g_{m1} \times g_{m5} \times (ro3//r_{o1}) \times (r_{o5}//r_{o7}) \tag{3.3}$$

The length's of the NMOS first stage load and the PMOS second stage load were many times the minimum in order to increase their output resistance. The lengths of the tail current sources were fairly long also. This guaranteed an acceptable Common Mode Rejection Ratio.

The sizing of the input and load transistors in the first stage also created favorable noise performance. The input transistors were made wide and short so that the input referred noise would be divided by their high transconductance. The load transistors were designed with longer lengths so that there low transconductance reflected less

Transistor	Length(μm)	Width(μm)
Mta,Mtb	50	.9
M1a,M2a,M1b,M2b	75	.18
M3,M4	175	.72
M5,M6	100	.18
M7,M8	50	.9
Ms1,Ms2	1.25	1.26
Mcp	1.5	.18
Mcn	1.88	.18
Mb1,Mb2	2.5	.18
Mb3	2.88	.18
Mb4	.5	.18
Mb5	2.5	.18
Mp1-4	1	.36
Mn1-6	1	.36

Component	Design Value
C1-4	50fF
Cc	1.4pF
Rc	360Ω
Ibias	35μA

Table 3.2: Opamp design values.

noise into the circuit. In addition to sizing, noise performance was improved by the choice of PMOS input transistors. PMOS transistors suffer from less flicker noise than NMOS transistors.

3.3 Compensation

Proper compensation is necessary to ensure the stability of an opamp in a sample and hold. In the case of the two stage configuration, a pole splitting capacitor C_c provides the needed unity gain stability. The compensation capacitor uses the Miller effect to increase the loading on the first stage and move the dominate pole to lower

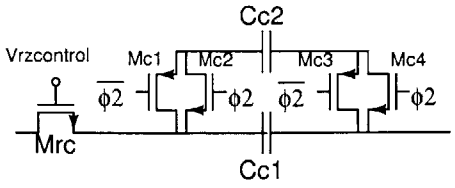

Figure 3-2: Variable Compensation

Transistor	Length(μm)	Width(μm)
Mc1,Mc3	10	.18
Mc2,Mc4	10	.18
Mrc	6.25	.18

Component	Design Value
Cc1	.4pF
Cc	1pF

Table 3.3: Compensation design values.

frequency. The frequency of the dominate pole is given by:

$$\omega_{p1} = \frac{1}{g_{m5}(r_{o7}//r_{o5})C_c(r_{o3}//r_{o1})} \tag{3.4}$$

The compensation capacitor also reduces the output resistance of the opamp at high frequency thereby pushing the second pole out to higher frequency. It is given by

$$\omega_{p2} = \frac{g_{m5}}{C_l} \tag{3.5}$$

In order to achieve unity gain stability and acceptable settling characteristics the unity gain frequency must occur before the second pole. The compensation capacitor must be chosen to ensure this.

Unfortunately the compensation capacitor creates a feedforward path which introduces a right half plane zero. This zero hurts the opamp's phase margin. The nulling resistor R_z moves this zero to the left half plane where it will increase rather than decrease the phase margin.

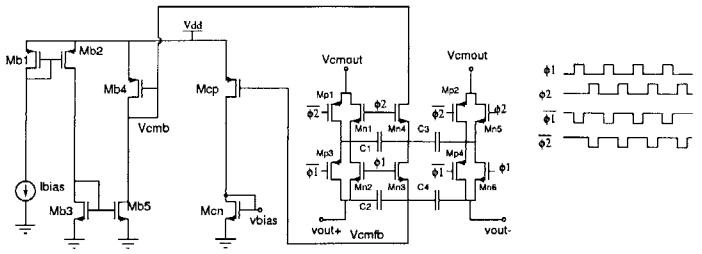

Figure 3-3: Common Mode Feedback

The actual compensation circuit that is used is shown in Figure 3-2. A transistor biased in the triode region, Mrc is used as R_z instead of a resistor. This was done so that the resistance matches $\frac{1}{g_{m5}}$ over process and temperature variation and so that the resistance value can be tuned with an external voltage. The compensation capacitor is made up of two capacitors in parallel. C_{c1} provides compensation during phase 1 and the parallel combination of C_{c1} and C_{c2} provide the compensation during phase 2. A smaller capacitor is needed during phase 1 because during phase 1 the sample and hold's load is not connected. The opamp sees a smaller load during phase 1 so the unity gain frequency can be higher. This allows the opamp to settle faster. Since the opamp sees a feedback factor of $\frac{1}{2}$ during phase 1 it needs to have a higher unity gain frequency if it is to match its settling time in phase 2.

3.4 Common Mode Feedback

3.4.1 Switched Capacitor Common Mode Feedback

The opamp's common mode feed back circuit(figure 3-3 is a standard switched capacitor implementation. The ideal common mode output voltage, V_{cmout}, is placed on the drains of Mn1 and Mn5. The expected value of the voltage needed be the circuit to produce a stable common mode voltage (V_{cmb}) is placed at the drain of Mn4. The output voltages are compared to the desired common mode and the circuit's bias is adjusted accordingly.

The sizes of the capacitors and the switches are chosen so that the switches' charge

injection does not create too large of a common mode transient in the circuit. They were also sized to ensure that the circuit settled quickly and used a minimum amount of area. Transistors Mcp and Mcn mirror the output of the common mode feedback circuit to the bias of the first stage load. These were sized to prevent common mode instability.

The common mode feedback control was fed into the NMOS loads rather than the PMOS tail transistors for two reasons: the ground node usually has less noise to couple into the common mode loop than the power supply and the opamp's two tail transistors would complicate a common mode loop which contains them.

3.4.2 Startup Conditions

All two stage opamps exhibit a common mode startup condition when used in unity gain feed back. If the output starts at the power rail the input will be forced to the rail. The output of the first stage will be at ground. When the inputs are at the rail the source of the input pair is forced to the rail and the tail transistors are cut off. Since no current flows in first stage the output of the first stage will stay at the ground rail even as the gates of the NMOS load transistors are brought to ground by the common mode feedback circuit. The circuit will stay in this locked up position as long as the it is not significantly perturbed.

In order to prevent the continuation of the startup condition transistors Ms1 and Ms2 were added to the circuit. When the output of the first stage goes to ground they inject a small amount of current into the NMOS load. This current raises the drain voltages of the NMOSs and pushes the circuit out of its locked state. The common mode feedback circuit then brings the common mode to the desired level. Ms1 and Ms2 were designed long and narrow so that they would conduct a very small amount of current during normal operation

3.4.3 Stability of Common Mode Loop

An opamp can suffer from common mode instability even if its differential loop is stable. The common mode loop contains the same poles and the zero as the differential loop as well as two zeros and two poles introduced by the current mirror in the common mode circuit. The current mirror also adds gain to the common mode loop.

The zero produced by transistor Mcp created the most problems for common mode stability. This zero is at:

$$\omega_{z,cp} = \frac{g_{m,cp}}{C_{gd,cp}} \tag{3.6}$$

In order to push this right half plane zero well beyond the crossover frequency it is essential to minimize the area and transconductance of Mcp. Minimizing $g_{m,cp}$ also minimizes the gain of the common mode loop.

$$A_{cm} = \frac{g_{m,cp}}{g_{m,cn}} \times g_{m3} \times r_{o3} \times g_{m5} \times r_{o5}//r_{o7} \tag{3.7}$$

A pole is introduced by $C_{gs,cp}$. Minimizing the area of Mcp also pushes this pole to higher frequency. Transistors M3 and M4 introduce both a pole and a zero into the common mode loop. The zero is at

$$\omega_{z,3} = \frac{g_{m,3}}{C_{gd,3}} \tag{3.8}$$

This is pushed to higher frequency by ensuring that the tranconductance of M3,4 is not too small nor the area too large .The pole is at

$$\omega_{p,3} = \frac{g_{m,cn}}{C_{gs,3}} \tag{3.9}$$

This pole can be pushed out past the unity gain frequency by limiting the area of M3,4 and by increasing the transconductance of Mcn. The limitation on the area of M3,4 limited the length of these transistors. Unfortunately the limited length increased their transconductances. This adversely effected pole and zero placement as well as increasing gain.

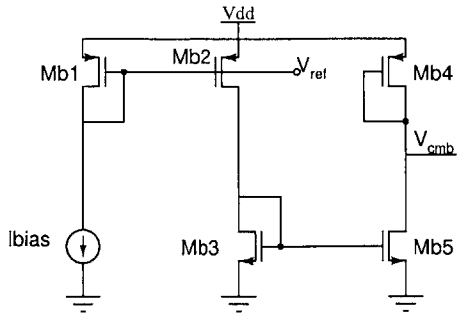

Figure 3-4: Bias Circuit

Transistor	Length(μm)	Width(μm)
Mb1,Mb2	2.5	.18
Mb3	2.88	.18
Mb4	.5	.18
Mb5	2.5	.18

Table 3.4: Bias design values.

3.5 Bias Circuit

The bias circuit shown in 3-4 is a standard circuit. Mb1 receives an off chip current and creates the voltage bias for the tail current sources and for the second stage of the amplifier. Mb2-5 transform the bias voltage into voltage expected by the common mode feedback circuit (V_{cmb}). This is the voltage expected at the gate of Mcp when the outputs are at a stable common mode. The sizes of Mb2-5 were adjusted for common mode stability reasons, as was previously mentioned, and were adjusted so that the common mode output would be about half way between the rails when V_{cmout} is half way between the rails. The common mode can be adjusted by changing V_{cmout} so the sizes of Mb2-5 are not critical for the determination of the common output voltage.

Chapter 4

Finite Gain Compensated Sample and Hold

The design of the sample and hold involves three issues: capacitor sizing, switch sizing and switch clocking

4.1 Capacitor Sizing

The sampling capacitors and feedback capacitors all match the 2pF output capacitor chosen to ensure that $\frac{kT}{C}$ noise in the sample and hold is consistent with approximately 12 bit performance. The capacitors at the auxiliary inputs are chosen large enough

Transistor	Length(μm)	Width(μm)
M1n,M1p,M2n,M2p,M3n,M3p,M4n,M4p	10	.18
M1c,M2c	6	.18
Mi1n,Mi1p,Mi2n,Mi2p	10	.18
Mon,Mop	10	.18

Component	Design Value
Ci	400fF
Cs,Cg,Cf	2pF

Table 4.1: Sample and Hold design values.

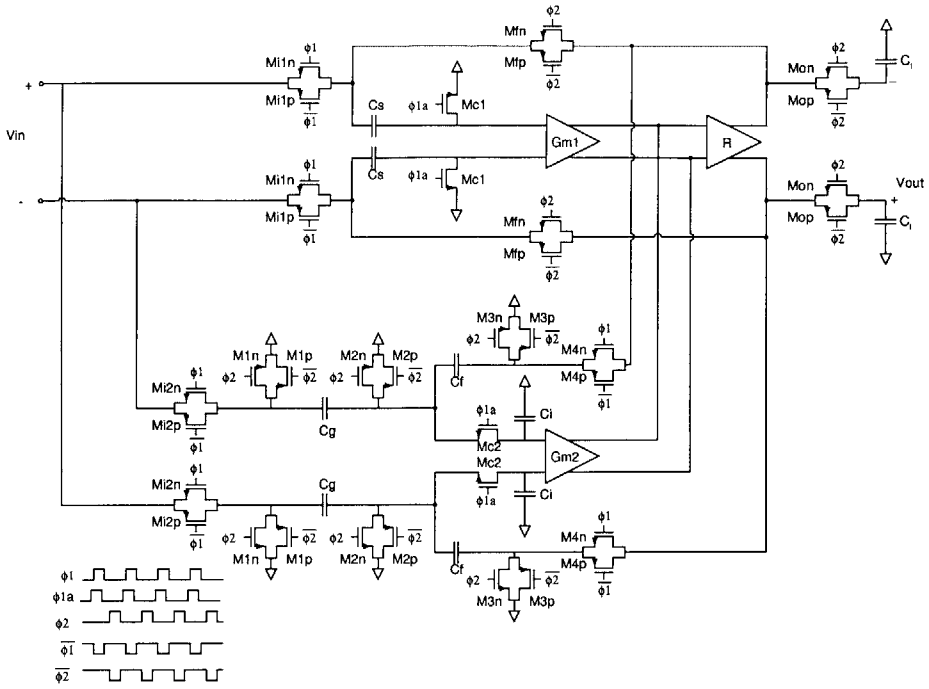

Figure 4-1: Finite Gain Compensated Sample and Hold

so that the charge injection does not corrupt their stored value, but small enough that they do not create stability problems, decrease the feedback factor significantly or load the output too much. The feedback factor is given by

$$f = \frac{C_f}{C_f + C_s + Ci} \tag{4.1}$$

The settling time constant is

$$\tau = \frac{f}{\omega_u} = \frac{1}{\omega_u} \frac{C_f + C_s + Ci}{C_f} \tag{4.2}$$

The smaller the feedback factor the longer time the opamp will take to settle. A smaller feedback factor also leads to less gain compensation since the amount of gain compensation is given by:

$$A_{comp} \approx A_0 \times f \tag{4.3}$$

4.2 Switch Sizing

Only Mc1 and Mc2 have critical sizing constraints. They need to be small so that the charge that they inject on to the sampling capacitors does not create unacceptable errors. The charge injection of these two sets of switches will not be completely common mode because the amount of charge that is injected by each switch depends on how the input voltage affects the impedance of the input switches (Mi1's and Mi2's). Since Vin+ and Vin- will not be the same the input switches will have differing impedances. The input switches are made as large complementary switches in order to minimize their on resistances. When the input switches have low on resistances they have low differential on resistance and therefore the differential charge injection produced by Mc1 and Mc2 will be minimized. If Mc1 and Mc2 are too small they will have too large of an on resistance. This large resistance will prevent the inputs from settling on the sampling capacitors quick enough. A large switch resistance of Mc2 also has the potential of creating a pole with Ci which appears before the crossover frequency in the loop gain transfer function. This can cause instability. All of the rest of the switches are designed to be large complementary switches so that their on resistances do not negatively effect the circuit.

4.3 Clocking of Switches

As is seen in Figure 4-1 Mc1 and Mc2 are clocked so that they open before the input switches. This reduces the amount of differential charge injection on the sampling capacitors. The input switches(Mi1's and Mi2's) naturally produce much more differential charge injection than Mc1 and Mc2 do because they are directly connected to the input. The input affects the V_{ds} of the input switch transistors and therefore affects the charge held in their channels. Mc1 and Mc2 open before the input switches and lock the charge on the sampling capacitors. When the input switches open their injected charge cannot change the total amount of charge on the sampling capacitors.

Chapter 5

Simulation Results

In this chapter simulation results are presented for the gain compensated sample and hold and for the opamp used in this sample and hold. HSPICE was used as the simulation tool. The simulations were used to verify the gain compensation technique and to optimize the circuit's performance. The simulations were completed using the transistor models of the TSMC .18μm CMOS process contained in the CMC design kit.

5.1 Opamp Simulations

The Opamp simulations reveal that the opamp functions at high speed and is stable under all feedback conditions. The opamp drew a lot of current so that it would settle quickly and to ensure that this settling was not limited by slewing. The opamp's performance in summarized in Table 5.1. The opamp operates in two different modes. During phase one the opamp has a 1.3pF load and a 1pF compensation capacitor. During phase two is has a 2.6pF load and a 1.4pF compensation capacitor. It can be seen in the table that the opamp has a larger unity gain frequency during phase one due to the smaller load and compensation capacitor. This was done so that the feedback factor of 1/2 during phase one would not cause the settling time to be significantly longer than during phase two. The opamp's frequency domain magnitude and phase response are seen for phase one in figure 5-2 and for phase two in figure

	Units	Phase 1 (Cl=1.3pF)	Phase 2 (Cl=2.6pF)
DC gain	(dB)	52	52
Unity gain frequency	Mhz	450	520
Phase Margin	degrees	67	80

Table 5.1: Summary of Opamp performance

5-1.

5.2 Sample and Hold Simulations

The Sample and Hold simulation shows that the gain compensation technique decreases the gain error and increases the effective gain by as much as 10dB . The simulated step response of the sample and hold is seen in Figure 5-3. The close up version of this figure seen in Figure 5-4 shows the operation of the gain compensated sample and hold. During phase one the output comes to within the gain error of the opamp of the input. During phase two the output draws much closer to the input. The spikes in the output are due to charge injected by opening switches on to the circuit's capacitors.

Figure 5-5 shows the effective gain of the sample and hold for different inputs. The line titled 'Not Gain Compensated' shows the effective gain after phase one. The line titled 'Gain Compensated' shows the effective gain after phase two. For low input voltages the increase in effective gain due to gain compensation is clearly seen. As the input voltages get higher the gain of both the uncompensated and compensated cases decrease. This is due to the fact that the increased input pushes the output transistors of the opamp toward the triode region and decreases their output resistance.

5.3 Common Mode Loop

One inherent difficulty in the design of fully differential two-stage opamps is ensuring common mode stability. The common mode loop was simulated rigourously to ensure

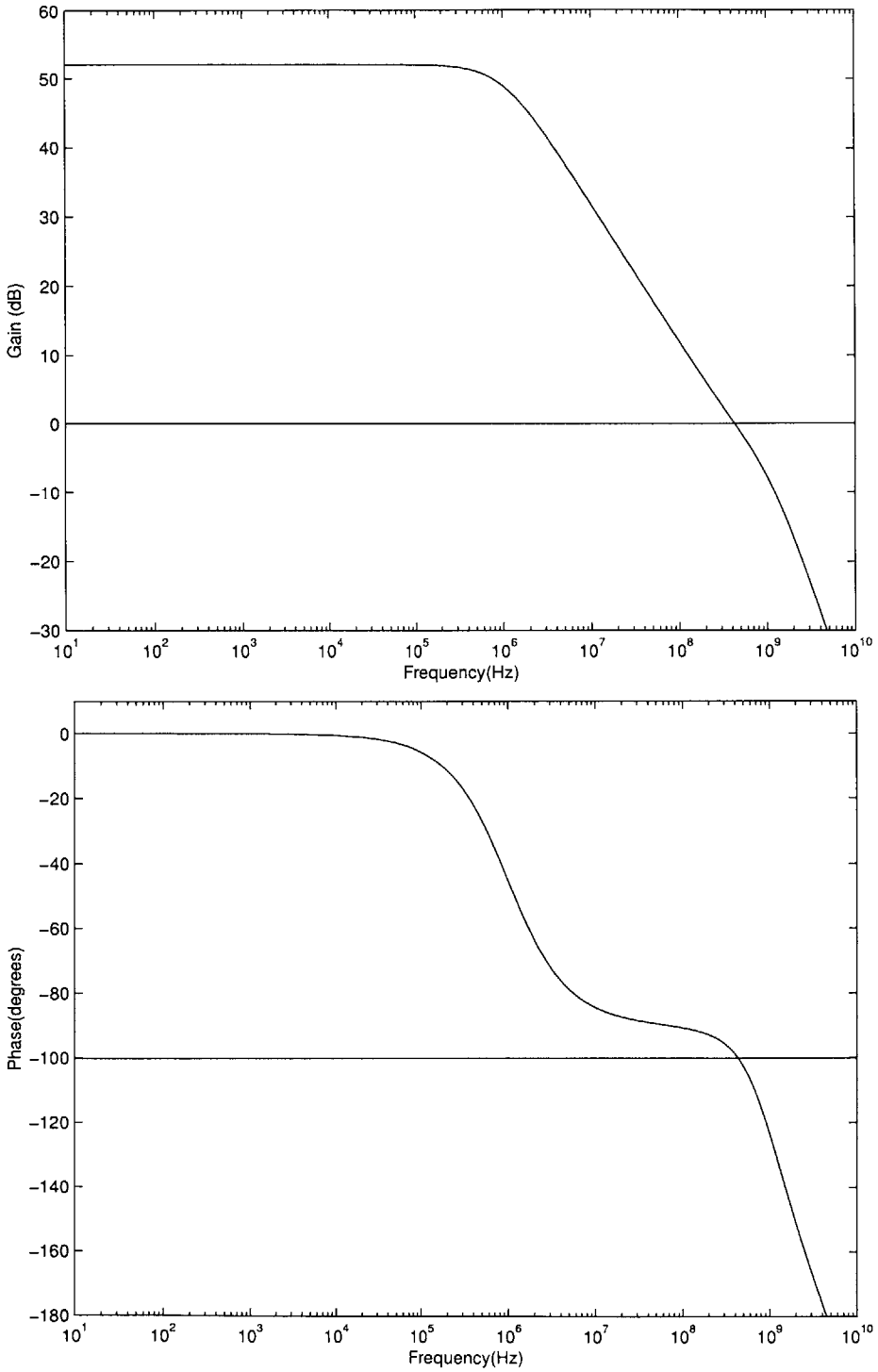

Figure 5-1: Opamp frequency domain magnitude and phase response with phase 2 load of 2.6pF

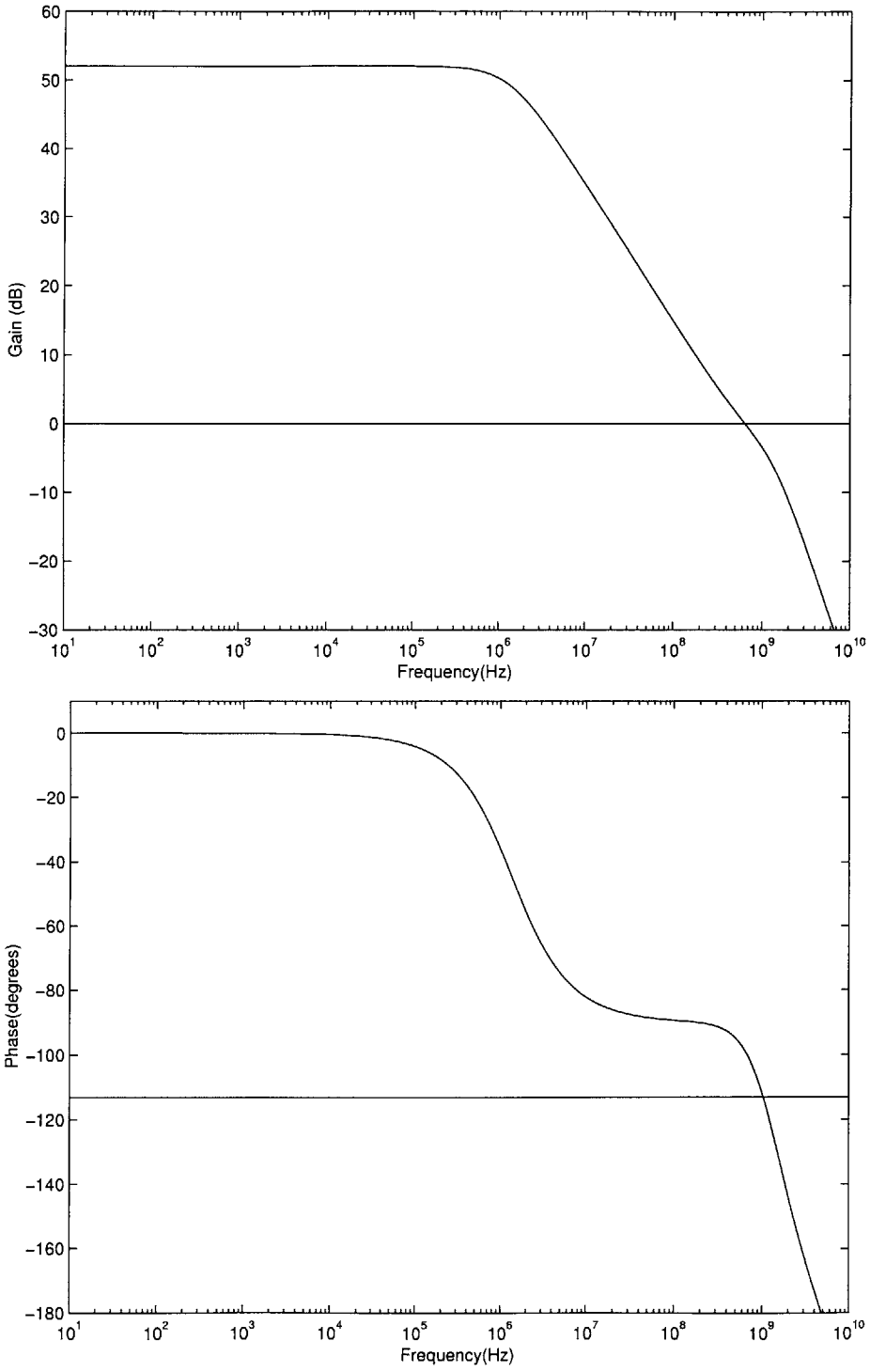

Figure 5-2: Opamp frequency domain magnitude and phase response with phase 1 load of 1.3pF

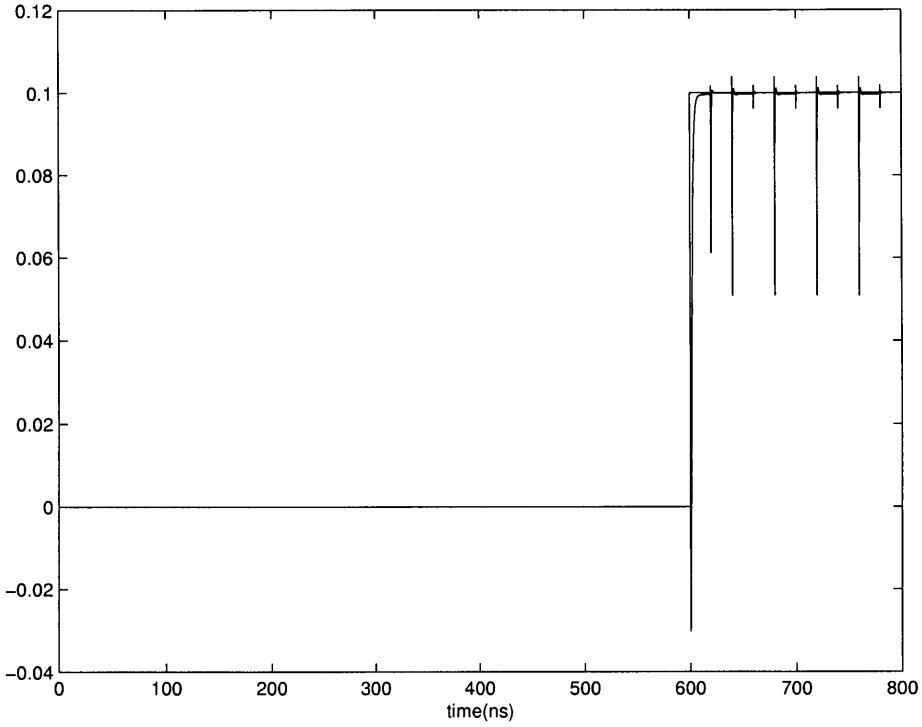

Figure 5-3: Sample and hold step response for .1V input

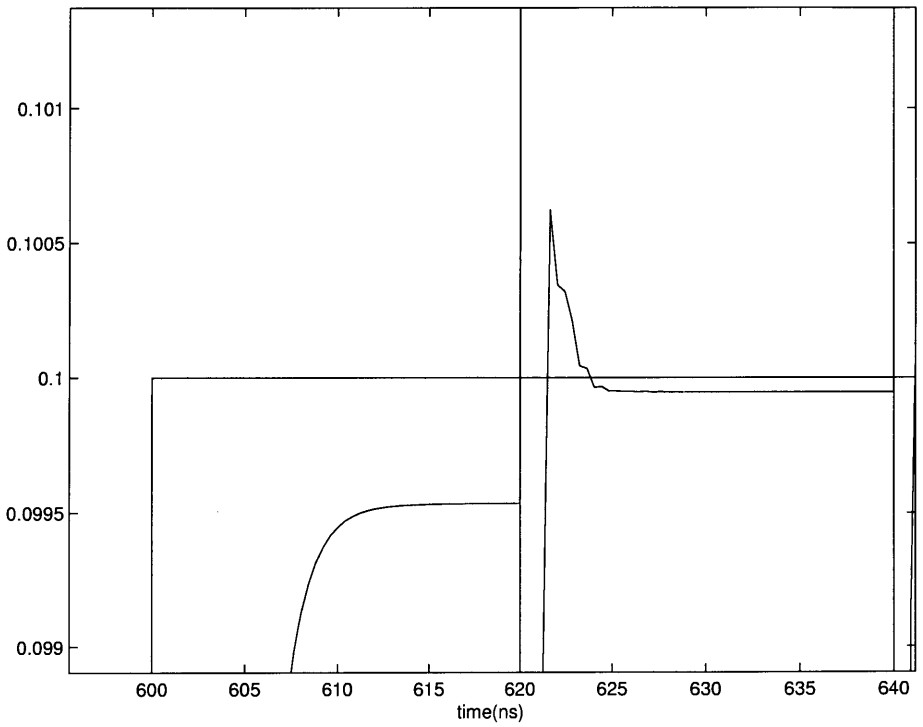

Figure 5-4: Close up of sample and hold step response for .1V input

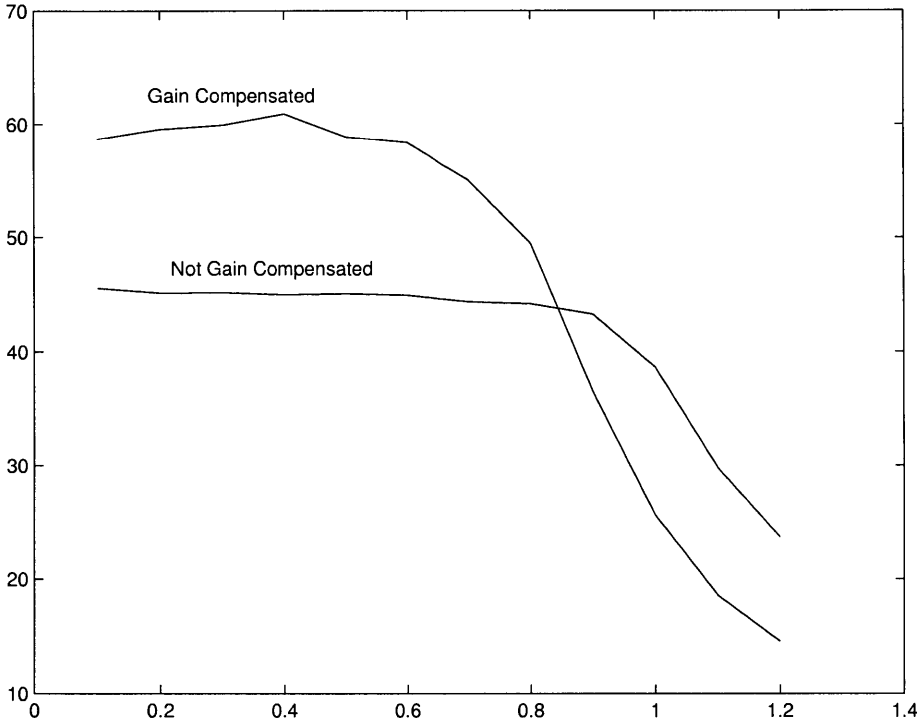

Figure 5-5: Effective Gain of the Sample and hold for different inputs

stability. Figure 5-7 shows the frequency domain magnitude and phase response of the common mode loop during phase one and Figure 5-6 shows it during phase two. In both cases the common mode loop has over 50 degrees of phase margin.

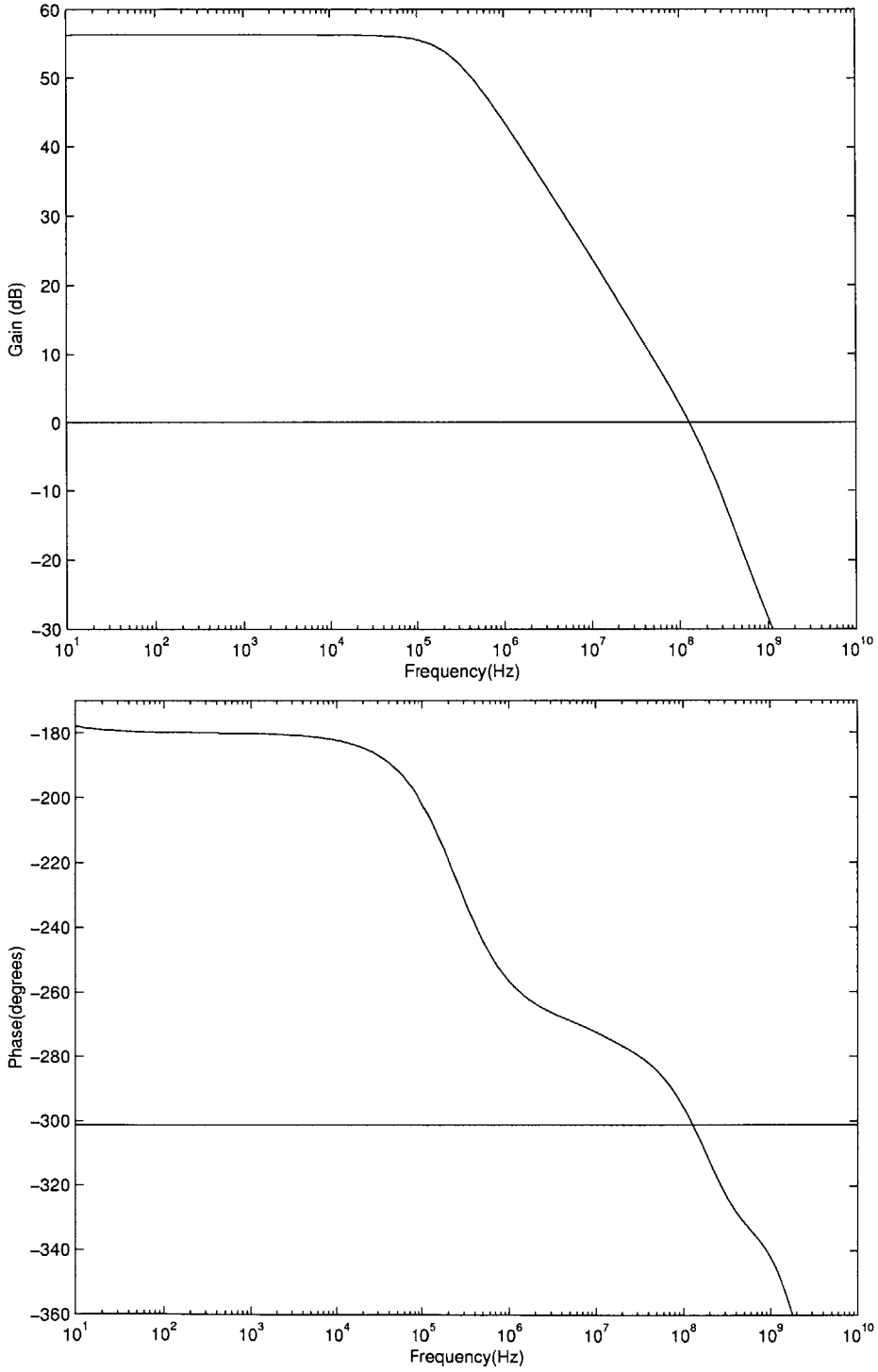

Figure 5-6: Common Mode Loop Transfer Function during Phase 2

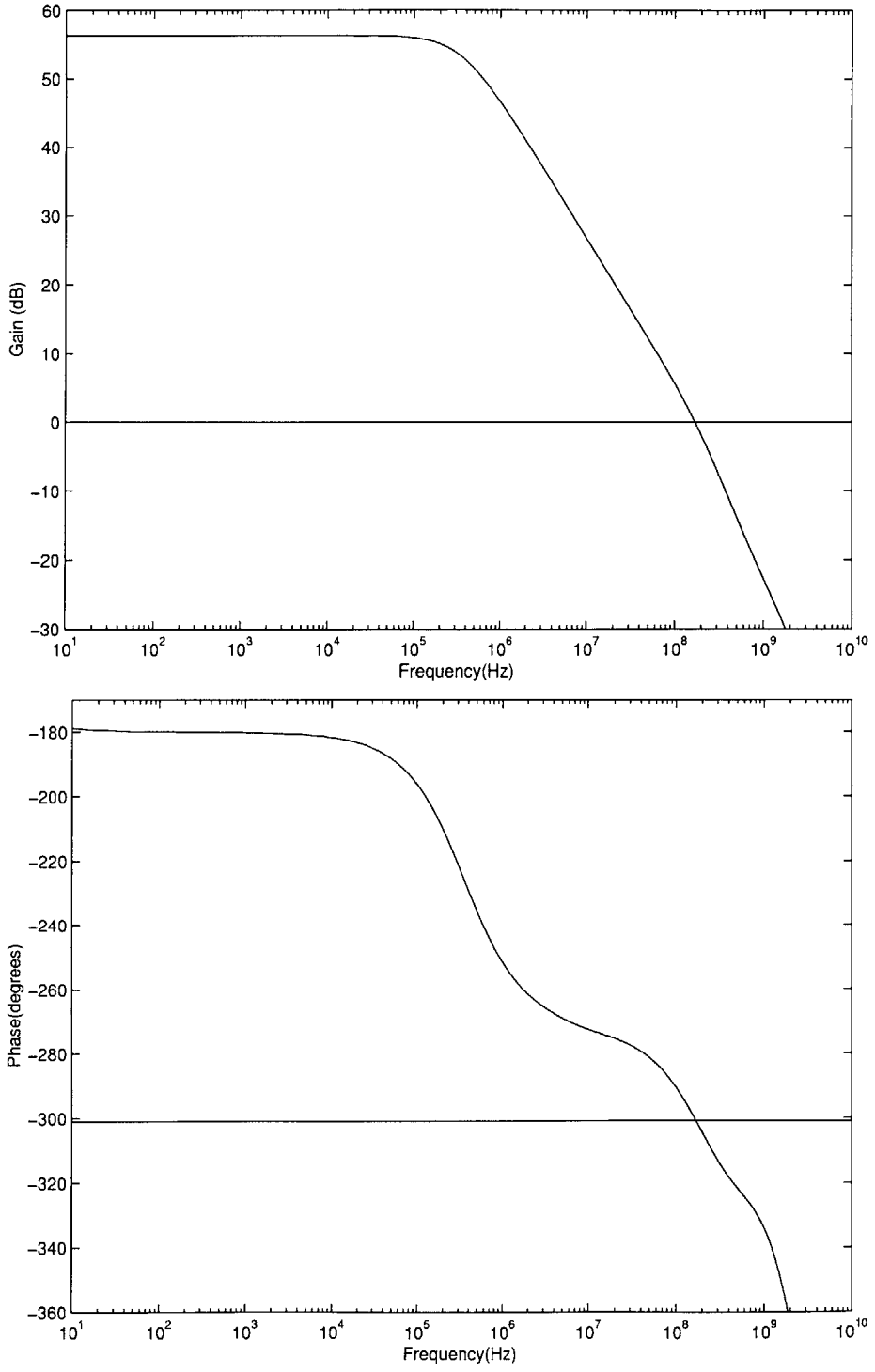

Figure 5-7: Common Mode Loop Transfer Function during Phase 1

Chapter 6

Layout

The test chip was fabricated in TSMC's .18um. A picture of the Layout in shown in Figure 6-1. This picture contains all of the active parts of the circuit, but leaves out all of the metal and polysilicon shapes that were added to meet CMP density requirements. In the actual circuit all of the empty space in filled with all levels of metal and polysilicon. This is seen in the die photo of the chip show in Figure 6-2.

The test chip contains two independent circuits. On the top of the layout is the gain enhanced sample and hold. Below the sample and hold lies a copy of the opamp used in the sample and hold. This opamp copy contains an extra input pair like the opamp in the sample and hold.

The entire layout is 10 times larger than the simulated circuit. The transistor are 10 times wider and the capacitors have 10 times more area. The transistor in the compensation circuit produces a resistance 10 times smaller than that used in simulation. This was all done so that the circuit could drive a large off chip capacitance. The actual circuit drives a 20pF load rather than the 2pF load driven in simulation.

6.1 Layout Topology

The sample and hold was laid out in a symmetric fashion in order to increase common mode rejection and reduce the effects of mismatches. The entire layout is a mirror image around a horizontal line which intersects the middle of the opamp. The tail

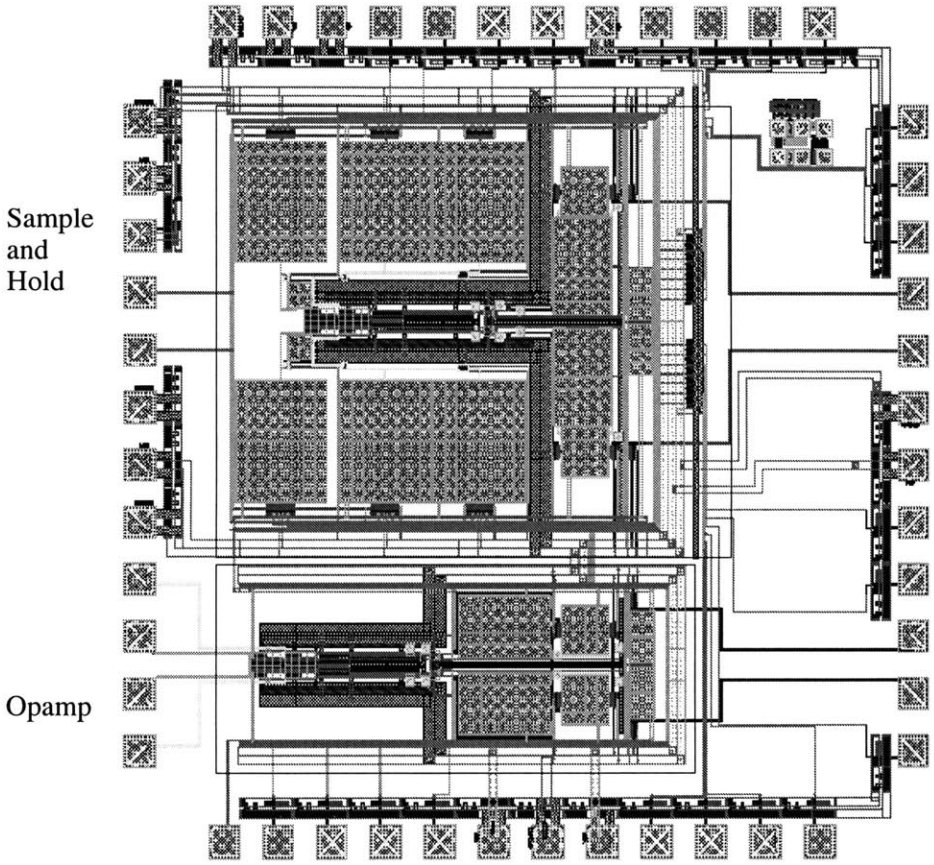

Figure 6-1: Test Chip Layout without Metal Fill

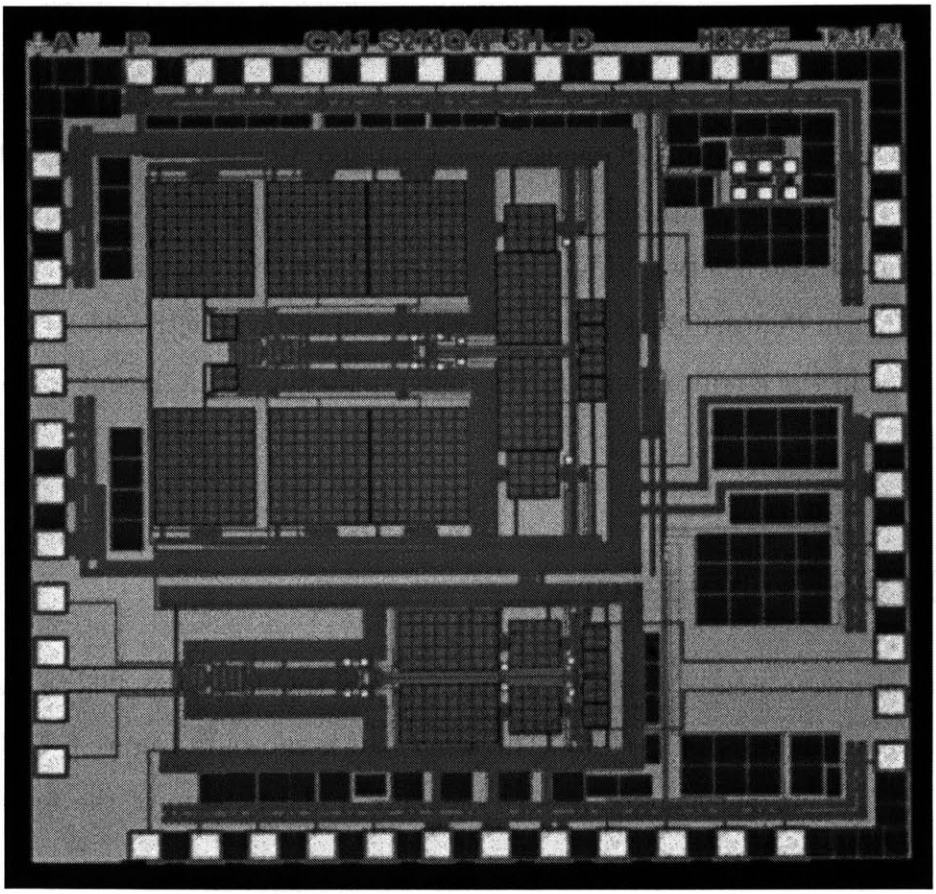

Figure 6-2: Test Chip Die Photo

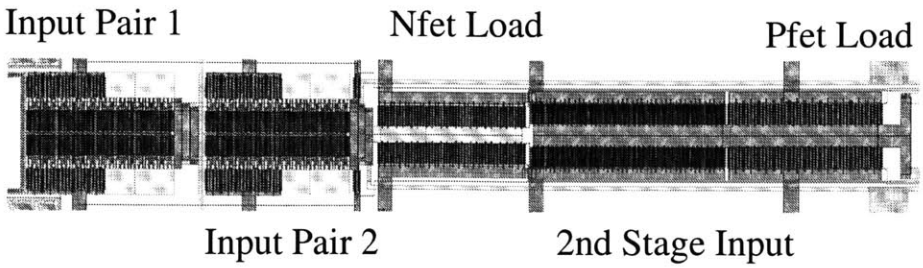

Figure 6-3: Opamp Layout

current sources and all of the bias transistors were divided in two and one piece was added to each side of the mirror image. The Common Mode Feedback circuit is also symmetric. It has two complementary switches and two capacitors on both sides of the centerline. It also has two NMOS switches straddling the centerline. The Layout of the amplifier in Figure 6-3 provides a closer view of the symmetric design. Many of the DC nodes in the circuit extend to the top and bottom of the layout and connect at its end.

6.2 MOS Transistors

The input pairs were created using a common centroid topology [4, p.435] to maximize the circuits matching characteristics. The input pair is shown in Figure 6-4. The two halves of the tail current source are seen on the top and bottom of the figure. The input pair lies in the middle. Half of each of the two input transistors lie on the top half and bottom half of the figure. There fingers are interdigitated in the following pattern : d_1-s-d_2-s-d_1-s-d_2-s-d_1 ... / d_2-s-d_1-s-d_2-s-d_1-s-d_2...

6.3 Capacitors

All of the capacitors in the circuit consist of stacks of metal from M1 to M6. M1, M3, M5 are one plate of the capacitor and M2, M4 and M6 are the other plate of the capacitor. This was done in order to achieve high capacitance density. Without this

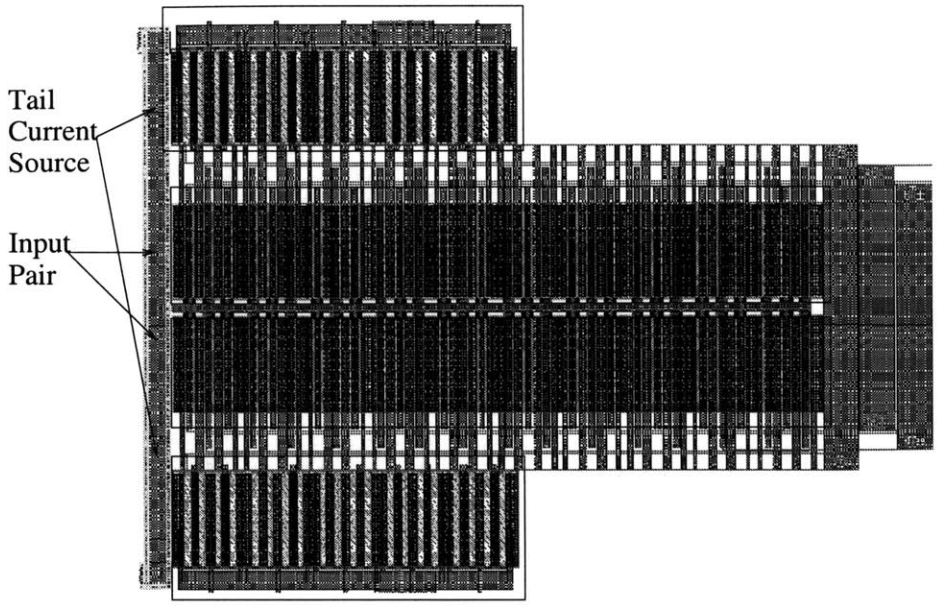

Figure 6-4: Input Pair Layout

stacked configuration the six 20pF capacitors in the sample and hold never would have fit on the chip. N type diffusion was placed under all of the capacitors and grounded off chip. This diffusion shields the capacitors from the noisy substrate.

The layout of one 20pF capacitor is seen in Figure 6-5. One can see in this figure that the capacitor is made up of many unit capacitors. Each unit capacitor is 35um on a side. The CMP process specifies this as the maximum allowable length of metal.

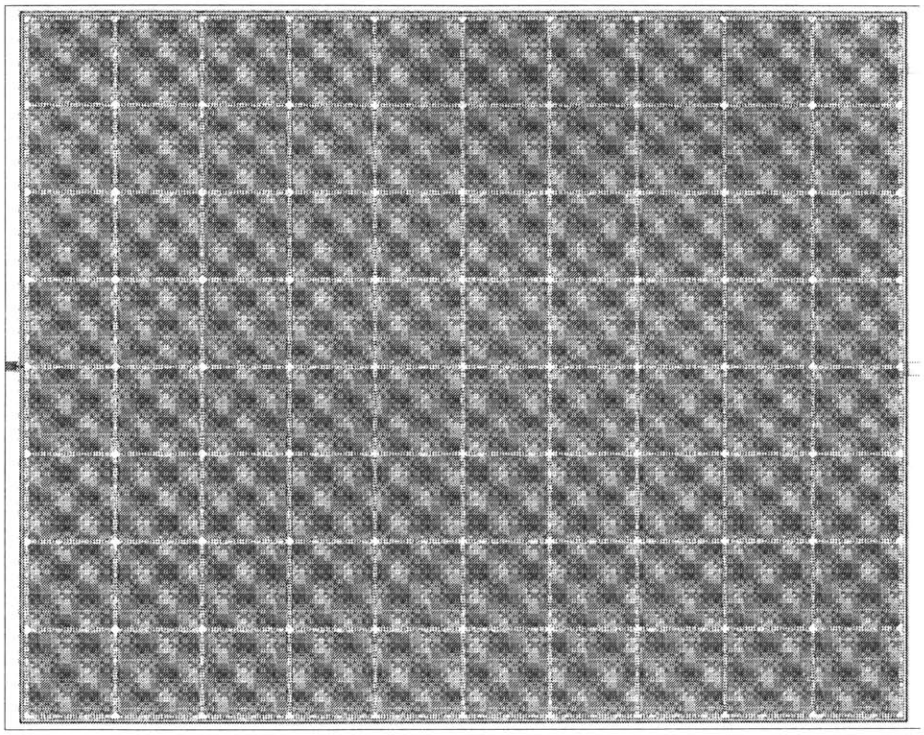

Figure 6-5: 20pF Capacitor

Chapter 7

Measurement Technique

7.1 Measurement Setup

The measurement setup consists of an HP54542A Digital Oscilloscope and a test board. The chip is soldered to the board and the two inputs and two outputs of the sample and hold are connected through BNC cables or active probes to the oscilloscope. The oscilloscope is controlled by a PC running National Instruments LabView Software connected to the oscilloscope via a GP-IB cable. Up to 16000 points at a time of data is captured from the oscilloscope by the PC. A sinusoidal dither signal is created by a HP 8656B signal generator and added to the inputs. This allows measurement averaging to produce a more accurate measurement than the 6 to 7 bits produced by the oscilloscope. The total measurement accuracy is defined by:

$$N_{bits,total} = N_{bits,oscilloscope} + \sqrt[4]{N_{samples}} \tag{7.1}$$

The sample and hold's clocks are generated on the board from a sinusoid produced by a Agilent 8644B signal generator. The separate opamp on chip was also tested using the oscilloscope. A sinusoid generated by a signal generator is transformed into differential signal and routed into the opamp inputs. The differential output signal is plotted vs the input signal. Measuring the slope of this plot near the zero crossing provides the opamp gain. This technique succeeds even when the output is clipped.

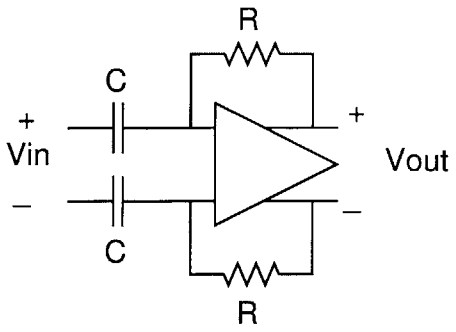

Figure 7-1: Offset cancellation test circuit

At higher frequency the gain of the opamp reduces and it is necessary to cancel its offset before an accurate gain measurement can be taken. Figure 7-1 shows the offset cancellation circuit.

7.2 PC Board Design

Figure 7-2 shows the layout of the PC test board. The top right corner contains the clock generation circuit. Below that lies the current and voltage references. Beneath the references are the sample and hold and opamp outputs. The sample and hold inputs are on the left side of the board. The opamp inputs are on the bottom of the board. The board schematics of the clock generation circuit, the references, the input and outputs and the voltage supply inputs are in Figures 7-3 , 7-4 , 7-5 , 7-6

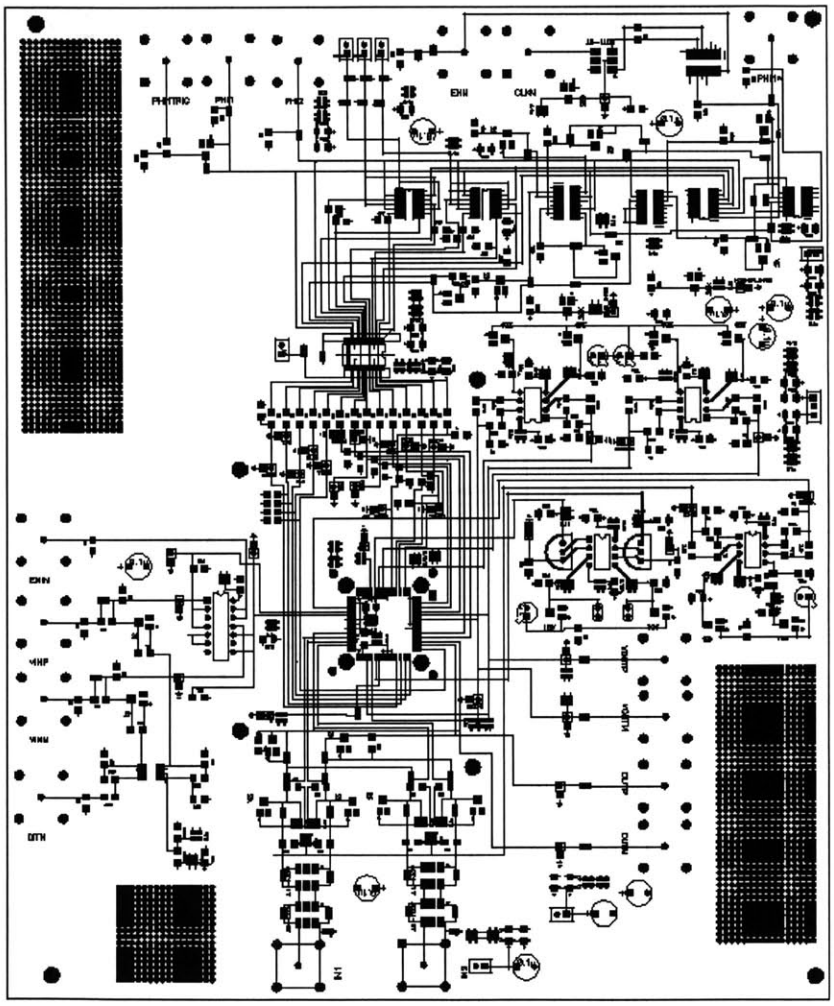

Figure 7-2: Test Board Layout

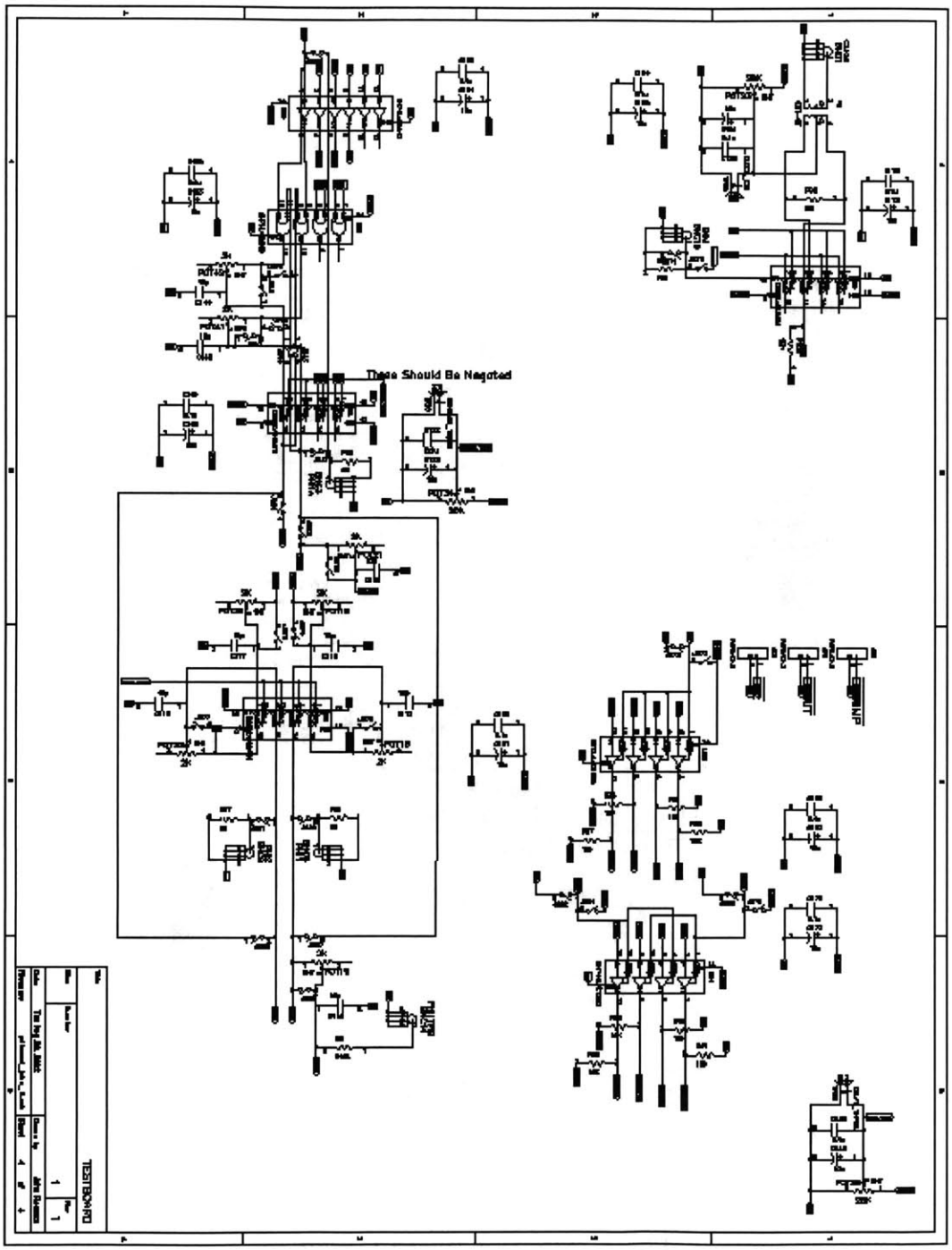

Figure 7-3: Schematic of clock generation circuit

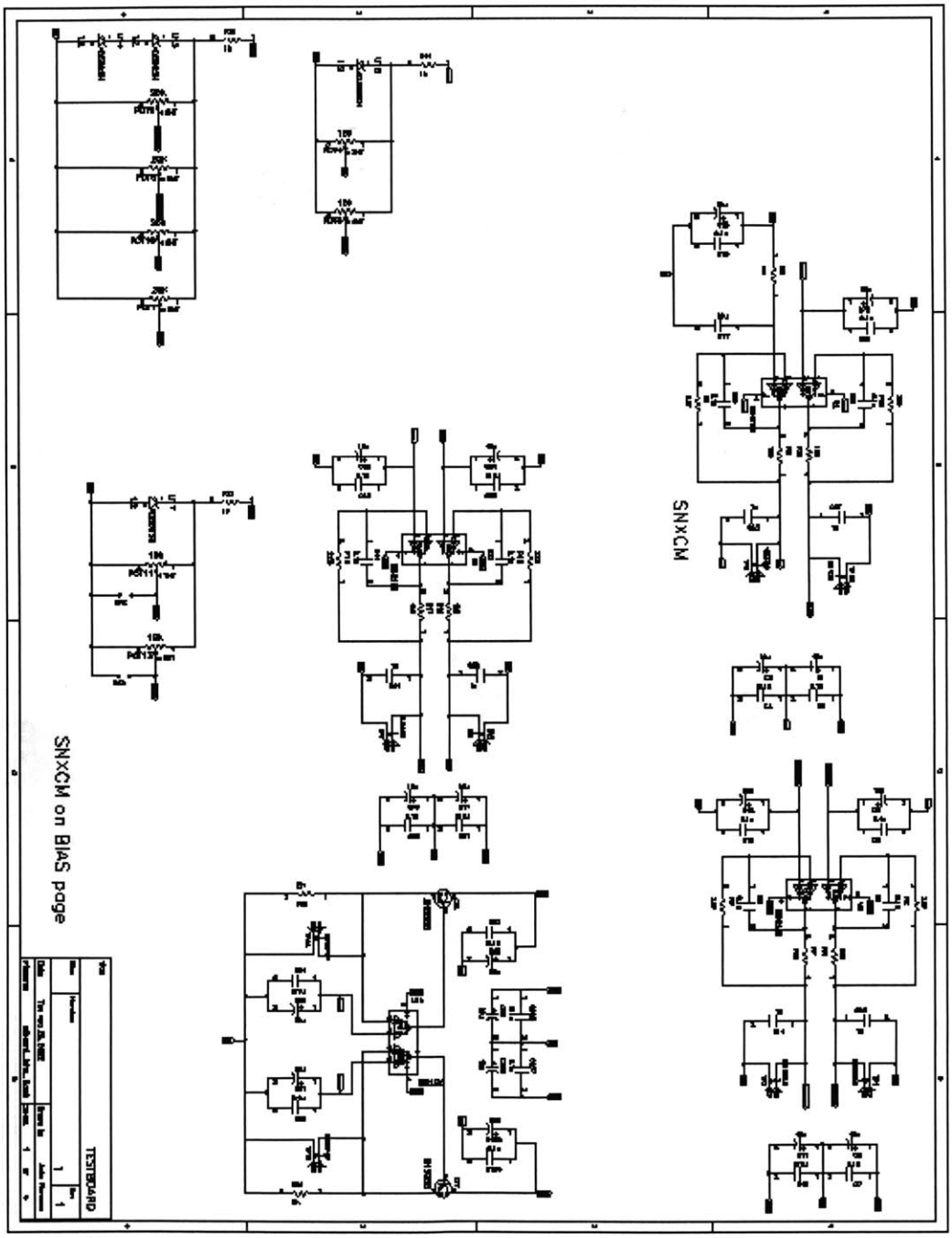

Figure 7-4: Schematic of voltage and current references

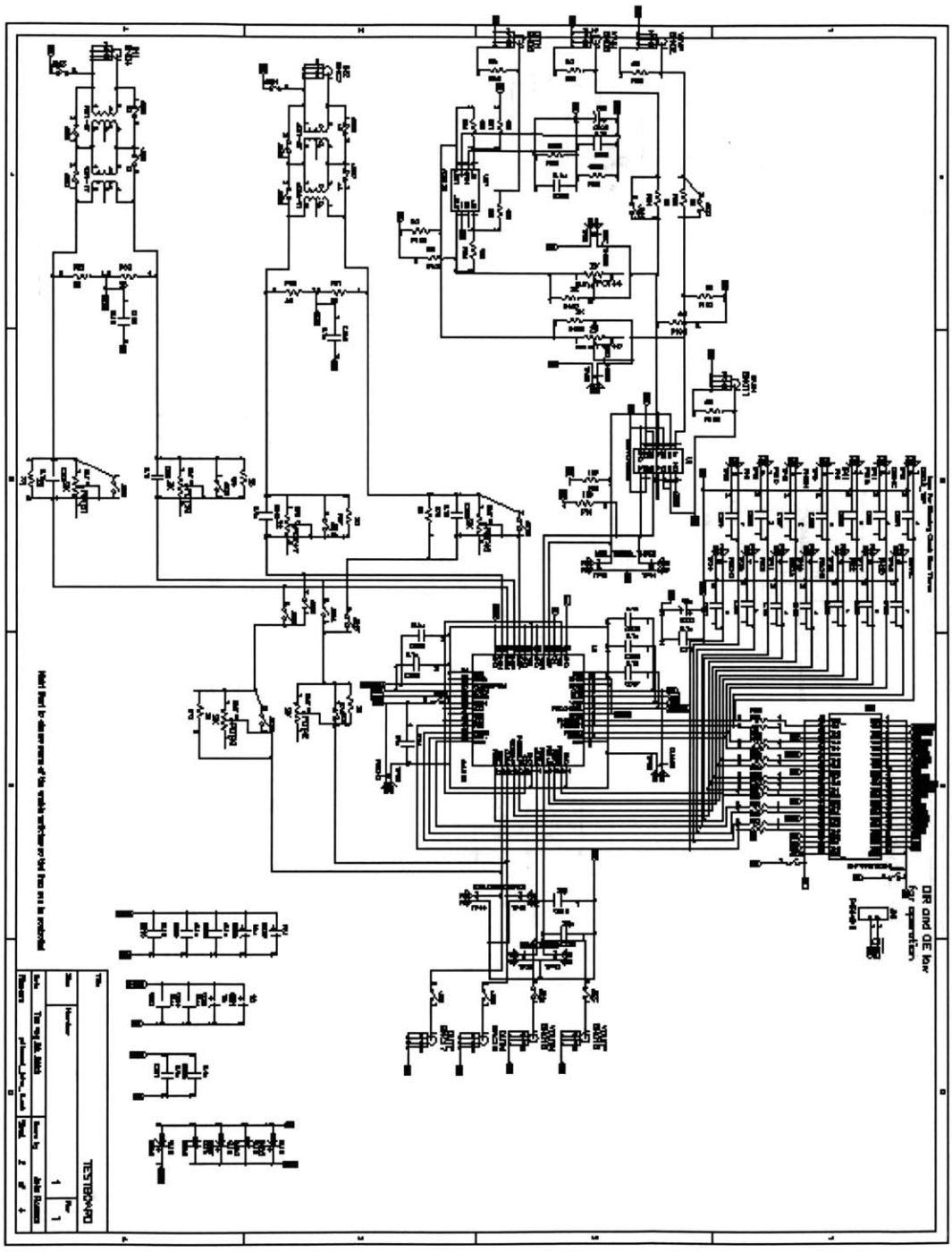

Figure 7-5: Schematic of chip inputs and outputs

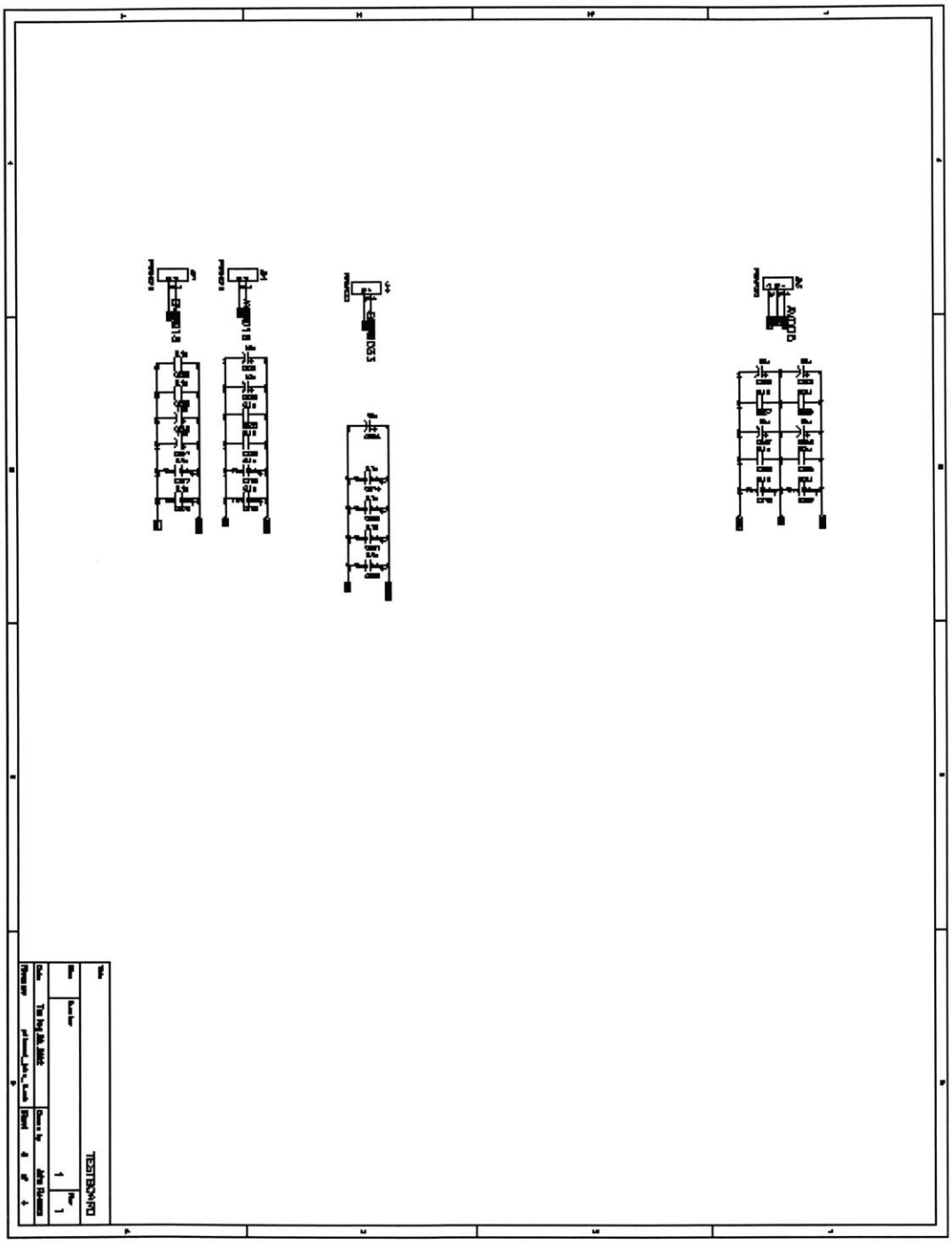

Figure 7-6: Schematic of voltage jacks and decoupling

Chapter 8

Conclusion

A new finite gain compensation technique was proposed and validated through the design and fabrication of a sample and hold. This technique adds a predictive path to a sample and hold through the use of an opamp with auxiliary inputs. A prediction of the output is derived from a parallel sample of the input. This prediction aids the sample and hold in settling more accurately. Unlike previous gain compensation techniques the proposed technique does not slow the operation of the sample and hold.

The proposed gain compensation technique has been validated through simulation. Testing of the sample and hold has shown it to be operational. Accurate measurements of its accuracy will provide final validation of the proposed technique.

The proposed technique is easily extended to pipeline analog to digital converters. Finite gain compensation is one way to counteract the deleterious effects of CMOS scaling on analog circuit performance.

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