Multi-connection Vias for Printed Circuit Boards

by

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MASSACHUSETTS INSTITUTE OF TECHONOLOGY

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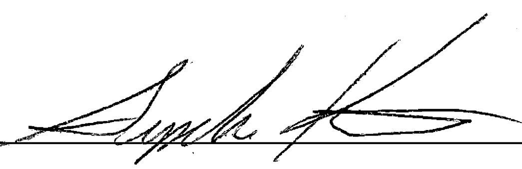
Signature of Author: 

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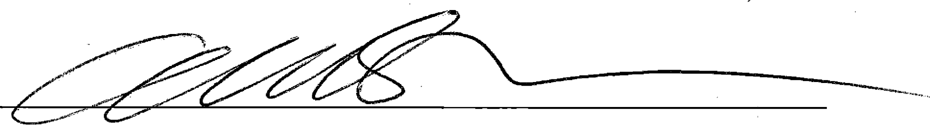
Certified by: 

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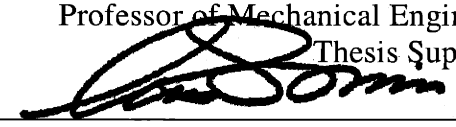
Accepted by: 

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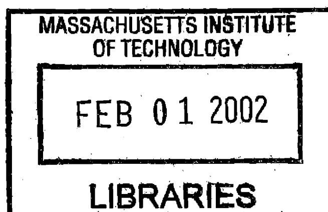
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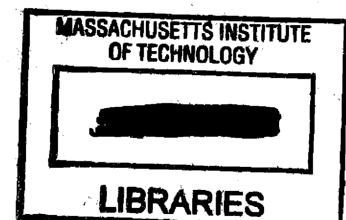
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Doctor of Philosophy in Mechanical Engineering

ABSTRACT

As the performance of digital electronic components improves, maintaining the integrity of high-frequency signals through circuit boards becomes increasingly challenging. The dimensions and material parameters of in-plane circuit board features, such as striplines, microstrips and co-planar waveguides are tuned to control signal impedance. Conventional multi-layer vertical interconnects, which connect between board layers, are not impedance matched to the in-plane signal traces. Multi-connection vias, developed in this thesis, provide a method for matching the impedance of vertical and in-plane features by forming co-cylindrical waveguides. Solutions from a high-frequency full-wave solver provide insight into field interactions within multi-connection vias; and results from these simulations and signal integrity experiments indicate impedance "tuneability" by adjusting the multi-connection via dimensions. The results also suggest that features can be impedance-matched independent of via diameter.

Multi-connection vias are formed by creating distinct conductor paths within cylindrical plated through-holes. The thesis explores several alternative manufacturing methods for fabricating these features. A specialized broaching machine and carbide-insert broaches were used to manufacture multi-connection vias for signal integrity experiments. Models of the broach tool and cutting force simulations resulted in several iterations of the broach design.

Broaching multi-connection vias is challenging due to the small diameters and high aspect ratios of plated through-holes, as well as the unique copper-epoxy/resin material. Since the broaching process prefers larger plated through-holes to permit larger broach tools, a new method was developed to analyze the cumulative connection density of multi-connection via arrays.

Multi-connection vias provide fertile ground for the development of corollary electronic products. Simulations for connector launches indicate that via impedance control can extend to board-mounted devices and connectors. Products that may benefit from multi-connection vias include by-pass capacitors, IC packages, test probes and pogo pins.

The thesis presents a roadmap for commercializing multi-connection vias. Elements of the roadmap include the integration of new signal routability constraints in CAD/CAM software, manufacturing processes, machine tool design, board testing, and durability.

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1 Introduction

Electrical connections between layers of multi-layer printed circuit boards (PCB) have traditionally been accomplished by drilled and plated through holes (PTHs). This process makes one connection from the top of the board to the bottom and to all the layers in between, as shown in Figure 1-1. Early in the history of PCBs, dividing this circular barrel of copper into multi-connections was proposed to improve density but was never seriously pursued. This thesis focuses on the potentials and processes of dividing PTHs, extending benefits beyond improved density to enhanced electrical signal performance.

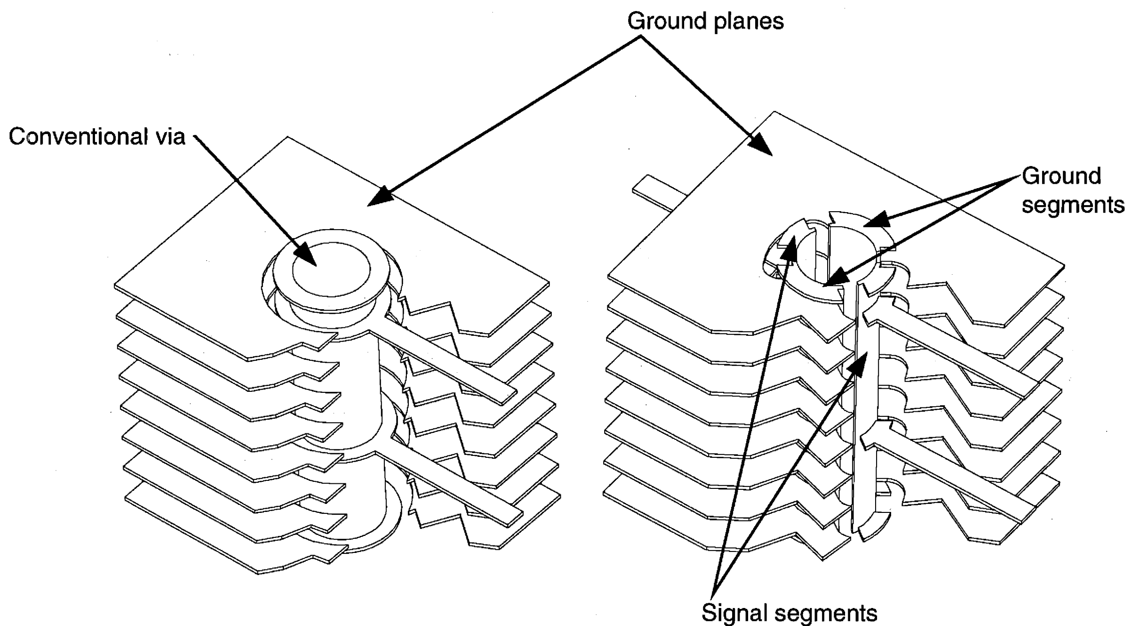

Figure 1-1: Plated through hole (left) and multi-connection via (right).

The fundamental contribution of this thesis is the development of manufacturing processes, geometry, and routing methods for multi-connection vias (MCVs). The resulting experimentation and simulation offers the potential for completely changing the routing rules for high speed signal traces in PCBs. Theory, backed with experimental work, for the manufacturing capabilities is produced and used to derive the theoretical performance enhancements to connection density and signal integrity. Device and connector launch to the PCB represents a major discontinuity in the signal path, concepts for multi-connection via

launch are developed and simulated. Product concepts for connectors and devices, including potential via-mount technology (VMT) device applications are proposed.

The establishment of a multi-connection via offers the signal functionality of a co-cylindrical waveguide that provides impedance control through the layer interconnect. This type of impedance control is not possible with standard via technologies, including more advanced structures like micro vias. This thesis provides basic design rules for these structures. The final major contribution of the thesis is the development of a roadmap to commercializing the multi-connection via.

The remainder of this chapter will give the background for this work and provides reference to past work conducted on this subject.

1.1 Background

The PCB was first developed in the 1940's by Dr. Paul Eisler using etched conductors on an insulator [Stewart]. As early as 1903, however, Albert Parker Hansen proposed laying metallic lines on an insulating medium to provide a much more efficient means of interconnecting vacuum tubes and other devices. By the 1950's PCB's, were standard in consumer and commercial applications, and by the late 1950's interconnection density demands pushed the development of double-sided boards. The double sided boards did not really take off until the late 1960's when copper hole-plating was developed, allowing the drilled holes to be plated (called vias) and providing interconnection between the top and bottom layers. Multi-layer PCBs were now possible, and by the mid 1980's accounted for the majority of US circuit board production [Flatt]. Today trace widths and spacing as small as 25μm are possible. Boards over 100 layers can be manufactured, as can drilled vias as small as 130μm supporting aspect ratios (hole length to diameter) as high as 20:1.

Over the past ten years, electronic device performance has increased by decreasing the path distance between transistors and decreasing transistor size. Today general digital device packages supporting frequencies as high as one GHz are available. On the other hand, the size and scale of the PCB has not changed significantly; as a result, the distance between device packages has remained relatively constant. For example, the standard AT motherboard for the 8088 processor of 1979 is the same size as the AT motherboard today. This lack of relative scaling has meant that the bandwidth of the PCB has not increased proportionally. The

bandwidth demands on future PCBs are such that the high frequency design issues can no longer be ignored.

PCB performance limitations are demonstrated in signal integrity phenomena like ringing, reflections, ground bounce, and crosstalk. These limitations are driven by signal rise times and board clock frequency. As the board clock frequency exceeds 100 MHz, PCB traces start looking more like high-speed signal transmission lines than D.C. electrical circuits. For a good overview of these phenomenon applied to high-speed circuit design see Johnson and Graham, [Johnson and Graham].

The board clock waveform of Figure 1-2 contains higher frequency harmonics than just the fundamental 150Mhz sine-wave. A rule of thumb for designing a transmission channel to pass this waveform with acceptable distortion is to design to the knee frequency ([Johnson and Martin] and [Harper]), which is where the signal energy drops off a significant amount, approximated by:

$$f_{knee} = \frac{K}{T_{rise}} \tag{1-1}$$

(where K=0.35 to 0.50)

For example, a PCB with a clock of 150MHz may require a rise time of 0.4ns, yielding a knee frequency on the order of 1.5GHz (the design-to frequency). That is approximately a 92mm wavelength in a standard PCB, approaching the device to device distance.

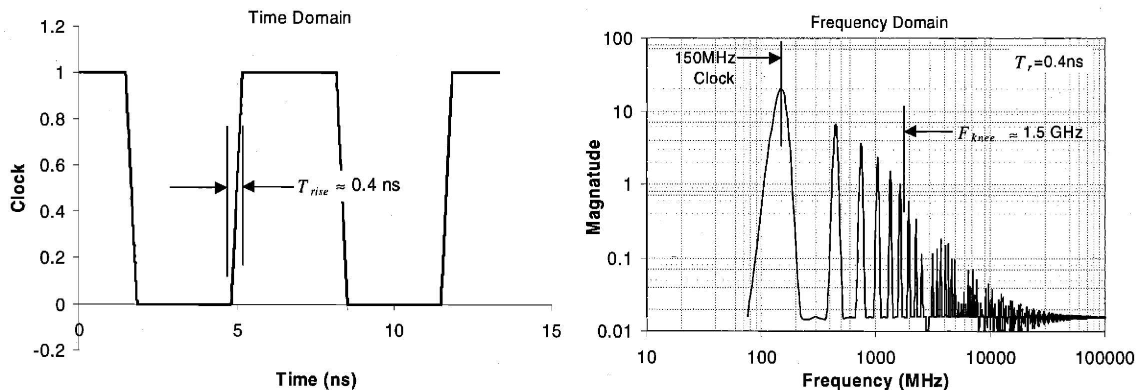

Figure 1-2: Time and frequency characteristic of a typical 150MHz clock.

Today's commodity computer motherboard operates at about 100MHz, while telecommunications and high performance systems use device to board frequencies an order of magnitude higher. According to the Semiconductor Industry Association (SIA) high

performance systems will see chip-to-board clock speeds in the GHz range by early next decade, see Table 1-1 [The National Technology Roadmap for Semiconductors]. To support these current and future performance demands, circuit board designers need to leverage all the design, analysis, and manufacturing tools available to them.

Table 1-1: SIA roadmap for high-performance chips.

Year	Smallest feature (μm)	On Chip clock (MHz)	Chip-to-board clock, peripheral bus (MHz)	Chip-to-board clock, high performance (MHz)	Chip to package pins/balls (connections)
1997	0.25	750	250	750	1450
1999	0.18	1250	480	1200	2000
2001	0.15	1500	785	1400	2400
2003	0.13	2100	885	1600	3000
2006	0.10	3500	1035	2000	4000
2009	0.07	6000	1285	2500	5400
2012	0.05	10000	1540	3000	7300

The PCB is essentially a complex set of signal interconnections created from a menu of standard features. The size, scale, and performance characteristics of these features are fundamentally limited by their manufacturing processes, most of which are standard in the industry. Functionally, the PCB interconnection features classify into three areas: on-layer, layer-to-layer, and board-to-device. The following sections introduce these areas.

1.1.1 On-layer interconnections (traces)

Photo-masked board traces are etched onto copper-clad dielectric substrates, such as fiberglass (FR4), to make on-layer interconnections. High frequency PC board design relies on the control of line width, line spacing, layer thickness, and dielectric properties. The basic structures used for building on-layer circuits for single-ended (Figure 1-3) and differential (Figure 1-4) signals provide protection against crosstalk, impedance mismatch and signal reflections. Developments in on-layer interconnection design include intelligent CAD tools, new materials, and features such as microcoaxial constructions, [Schieber].

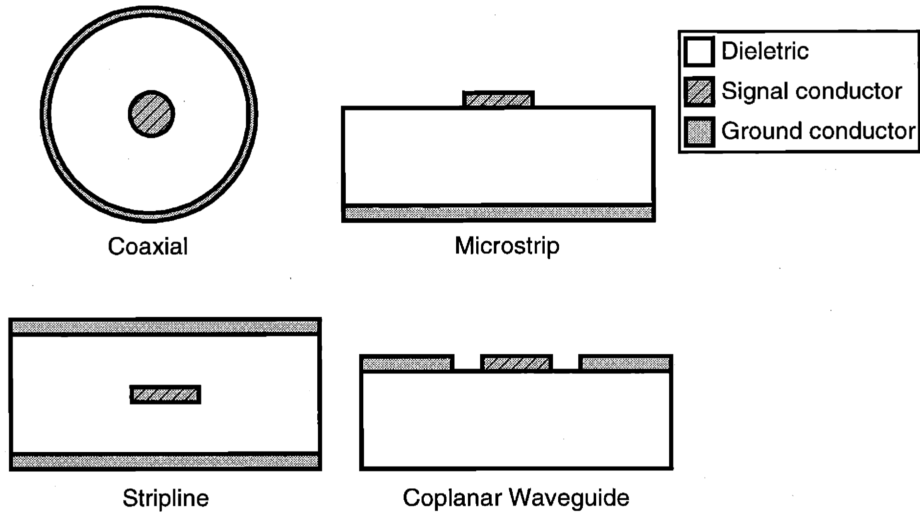

Figure 1-3: Signal ended impedance matched structures.

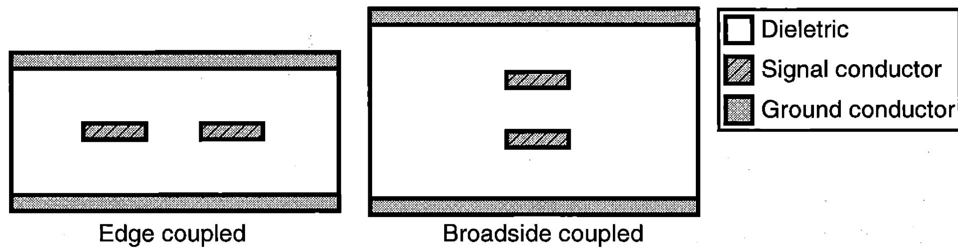

Figure 1-4: Differential structures

Typically, the trace impedance in a PCB is fixed to a 50Ω or similar standard that all devices, boards, and connectors are held to. The control of trace etching in PCB manufacturing (see Appendix A for a detail description of the PCB manufacturing process) is such that PCB impedance cannot be precisely controlled by simple design rules. It is therefore necessary, in the case of high frequency PCBs, for the board designer to specify the nominal trace widths and spacing, nominal layer thickness, and the exact desired impedance. The board manufacturer must then use a combination of simulation, empirical data, and trial and error to adjust trace widths and dielectric thickness to meet the impedance requirements. The overall board thickness is then adjusted to meet the design specifications with a take up layer, often in the center of the board.

1.1.2 Layer-to-layer interconnections (vias)

The plated through hole (via) has been the mainstay of layer-to-layer interconnection since the inception of double-sided and multi-layer boards [Flatt]. Originally vias served dual purposes,

providing layer-to-layer interconnect and through-hole component mount. The growth of surface mount component technology since the middle 1980s has, with the exception of backplane connectors and other large devices, since relegated the via to a single function of layer-to-layer interconnection. The need for high-speed PC boards and higher densities has pushed drilled via technology to limits in size and form, including blind and buried via combinations, as illustrated in Figure 1-5.

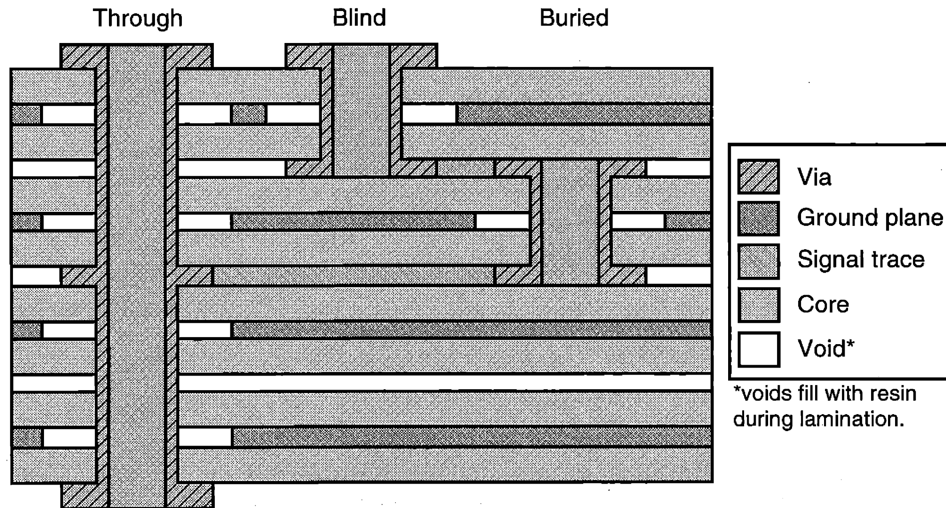

Figure 1-5: Section of conventional drilled and plated vias.

In addition to drilled and plated vias, developments in "buildup technologies" such as microfilled vias, photo-via redistribution, and sheet buildup, have increased performance significantly, [Fitts] and [Holden]. Most of these technologies rely on thinner layers and use chemical etching (photo-defined vias), laser ablation, or plasma etching technologies to drill holes and connect PC board layers. Figure 1-6 illustrates micro-vias. Because they must be manufactured from the outer surface (often out of non-woven aramid reinforced layers ([Jawitz]) or unreinforced dielectric), the micro-vias can only be on the outer traces unless subsequent layers are built on top of the constructed panel. Each layer adds significant processing cost. Via depth is limited greatly because the plating chemistry cannot flow through small blind holes in the same manner as through-hole vias. Similar limitations exist for laser ablated and co-deposition vias.

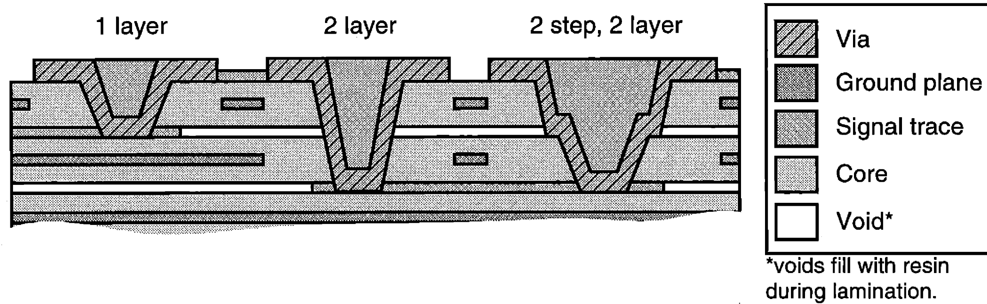

Figure 1-6: Section of micro-vias.

Both the signal and density performance of micro-vias are very good in comparison to drilled vias. There are still discontinuities in the signal path, because the ground plane is disrupted. However, because the scale is so small, this problem is minimal, especially when only going through one layer (which breaks the continuous ground path). Micro-vias find best application when the number of layers is very small or where density is extreme, such as in μBGA (micro ball grid array) escapement. As an added benefit, micro-vias can be placed directly in a surface mount pad.

In the final analysis, drilled and plated vias provide best coverage where the number of layers between traces that need to be connected is high. In contrast, micro-vias function more as on- and off-ramps to the vertical highways that conventional vias represent.

1.1.3 Board-to-device interconnection

Device-to-board or board-to-board interconnections must meet the signal performance requirements of the SIA chip-to-board roadmap, Table 1-1. Often this connection between the device and the PCB, the "board launch," is a dominant source of high frequency discontinuity. The most popular board launch technologies currently used for devices are surface mount (including ball grid arrays), and through-hole-solder. Connectors employ the same technologies and add edge-card, through-hole-pressfit, and pressure mount board-launch.

One of the oldest types of board launch technologies is the through-hole soldered connection, shown in Figure 1-7. This type of connection was used on single sided PCB's before the advent of multi-layer boards in the late 1960's. Assemblies can be processed through conventional wave solder systems. Manufacturing tolerances are taken up by the solder in the hole, making these types of connectors easier to manufacture.

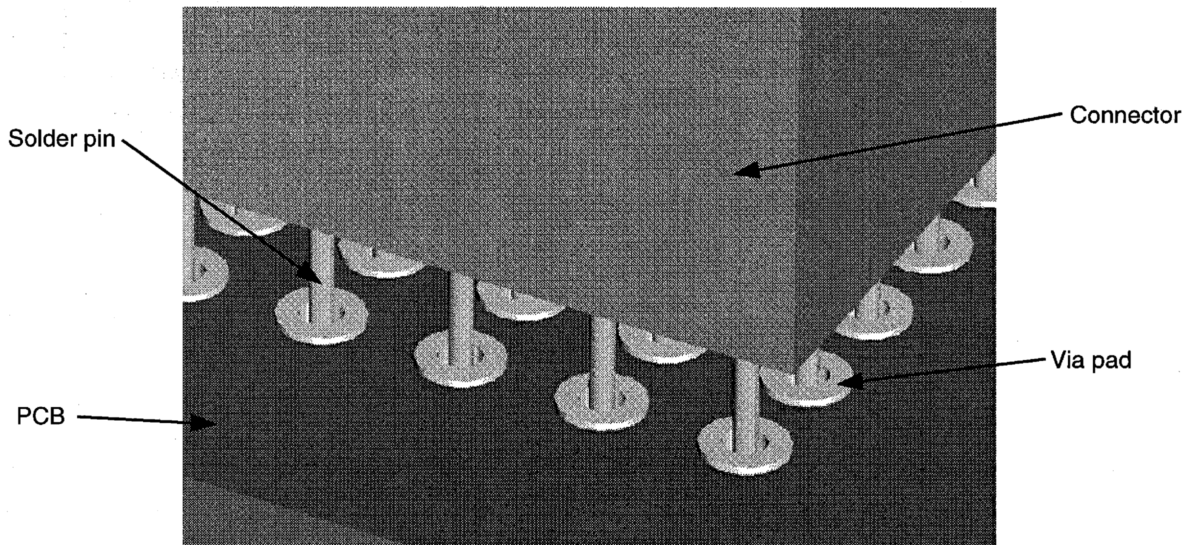

Figure 1-7: Through hole soldered connector.

In the manufacture of larger PCBs such as backplanes, wave solder processing of connectors is not desirable. The development of the pressfit connector, Figure 1-8, addresses this by making the connection using a compliant pin. The connection is maintained by the mechanical forces from the partially collapsed pin in the via.

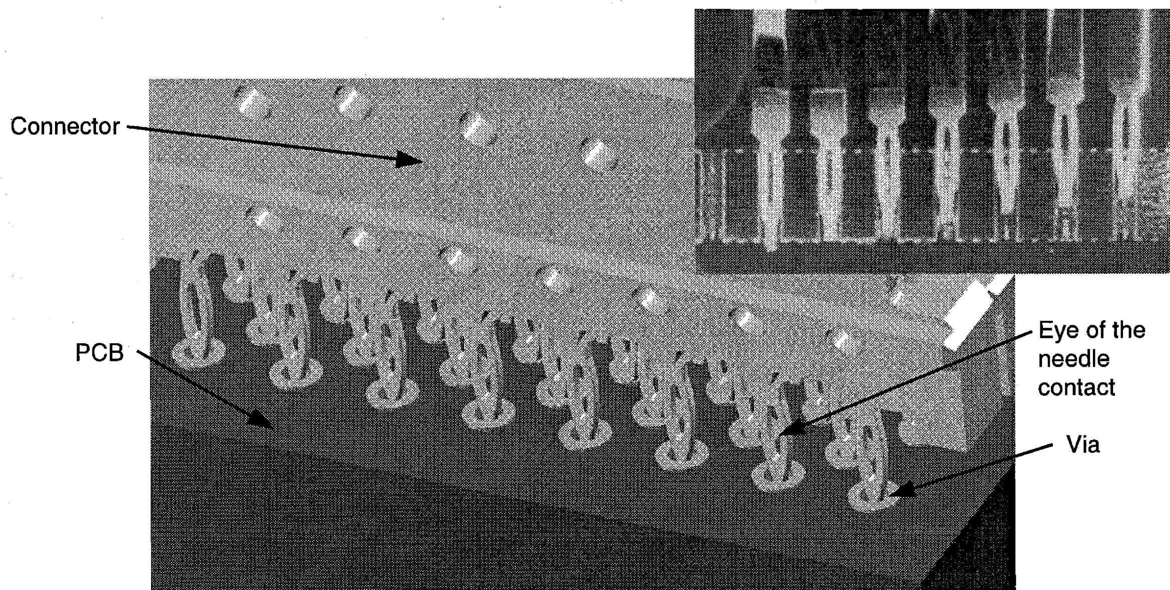

Figure 1-8: Pressfit connector.

The edge card connector uses gold plated surface pads on the edge of the PCB as one side of the connector, Figure 1-9. Edge card connectors are desirable from a cost standpoint because there

is only one piece to the connector. Ground planes may follow the conductor right up to the pad resulting in very good electrical performance. From a density standpoint they are limited to two conductor columns and only on the edge of the board, thereby limiting them to relatively low signal count connections.

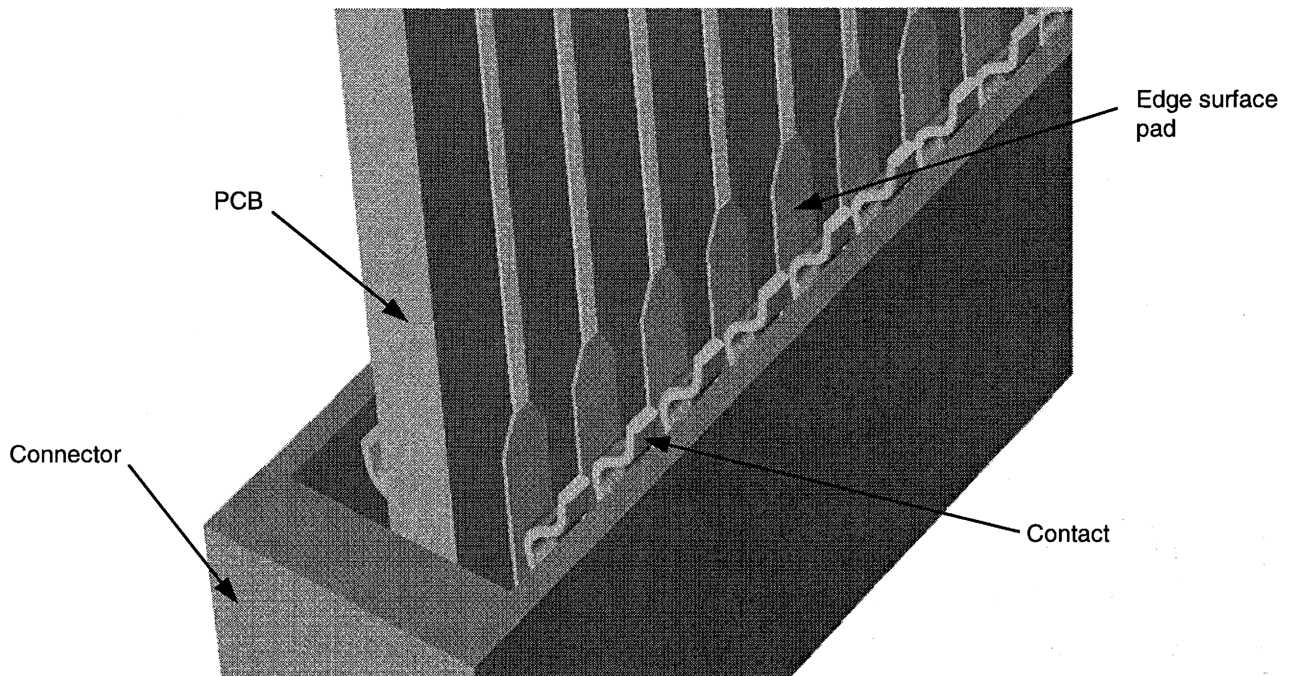

Figure 1-9: Edge card connector.

While surface mount devices are well established surface mount connectors have had limited development, Figure 1-10. This is partly due to the relative reliability of surface mount to other technologies. As the push for high speed-higher density-connectors continues, they are gaining acceptance.

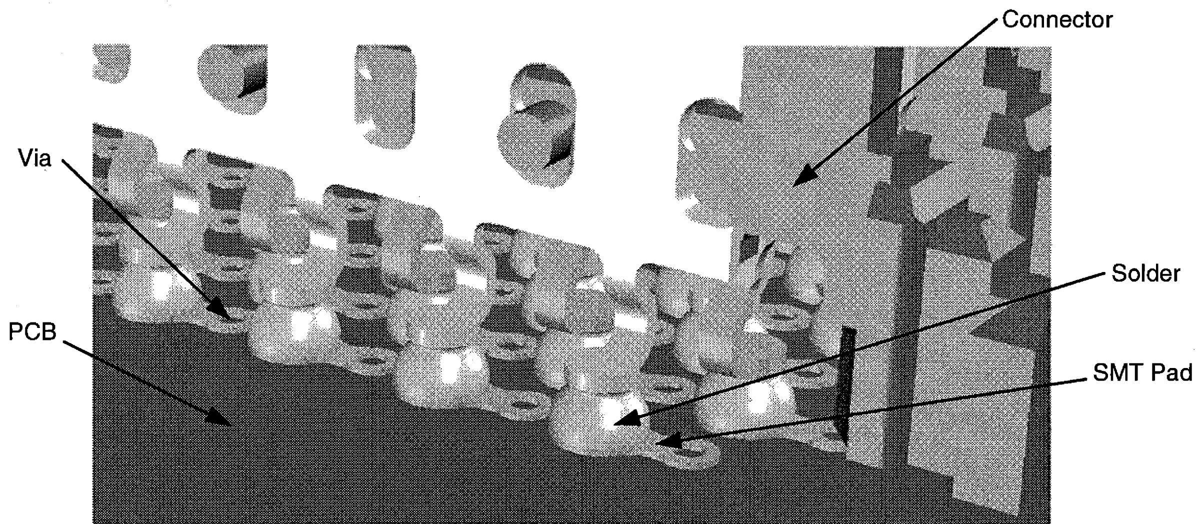

Figure 1-10: Surface mount connector.

1.1.4 Overview of PCB design and manufacturing

Multi-layer PCB design and manufacturing involves a complex set of steps and an extraordinary number of specialties. The fact that custom boards can be ordered and built quickly, in spite of this complexity, can be attributed to the competitive nature of the electronics industry and utilization of the tools and processes described below.

1.1.4.1 CAD/CAM tools

The first step in the design of a PCB is to take the desired schematic and route the PCB traces and layers. Most CAD packages today combine the schematic layout and the board layout into one associative package, ranging in price from $1K to $15K (in 1999 US dollars). The routing of the traces on the board are usually run by autorouting algorithms that use a rules-based system to place the traces [Dally]. Some of the more advanced packages optimize for signal performance, e.g. running differential lines.

Once the board is designed, the data is transferred to a computer aided manufacturing (CAM) package that generates the layer films and drill files. The drill files provide the numerical control (NC) data used by specialized PCB drilling equipment.

1.1.4.2 Lamination processes

Once all the designed layers and films are generated, the board manufacturer develops and etches the PCB layers. These layers are laminated with fiberglass and epoxy resin (for information on other materials, [Jawitz]). The laminate is then drilled for vias, plated, and etched for outer traces. A detailed treatment of the lamination process is provided in Appendix A.

1.2 Prior work

Creating multiple conduction paths within PCB vias was first disclosed in 1968 by IBM [Reinhart]. The disclosure suggests broaching as a manufacturing process, and the possibility that these paths reduce impedance discontinuity and increase density. Furthermore, the formed slots might be useful for registration of connectors and larger diameter holes improved plating. No development work is alluded to or subsequently published.

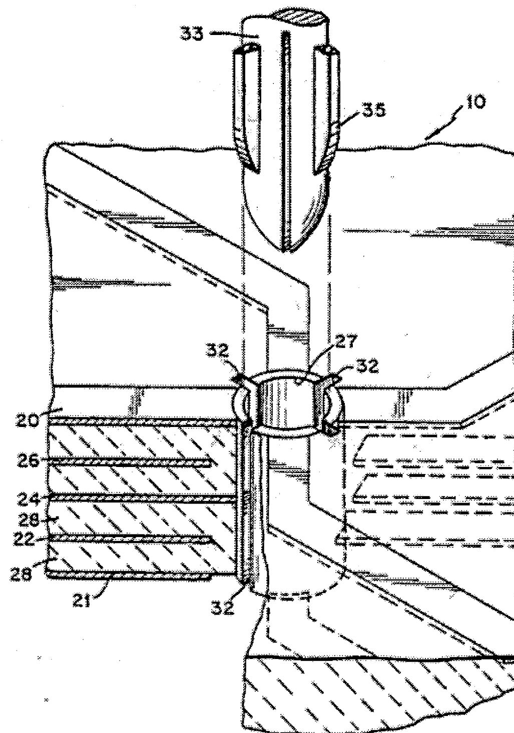

Figure 1-11: Cross section of coaxial via structure [Reinhart].

In 1973, a coaxial via structure was proposed, Figure 1-12, that require inner layers to have large plated holes [Dougherty]. Primary or larger holes would be drilled and plated in sub-panels then assembled together to form a thicker panel. This is the same process that is

employed to build buried vias, except that the vias are aligned forming an epoxy filled via. Because the holes would be larger, they were suitable to introduce discontinuities into the plating of the hole before the sub-panels were laminated. There are no discussions of how these separations are made. The inner hole is now drilled coaxial in the epoxy and plated as a standard via would be. No subsequent development or work beyond patent filing is published.

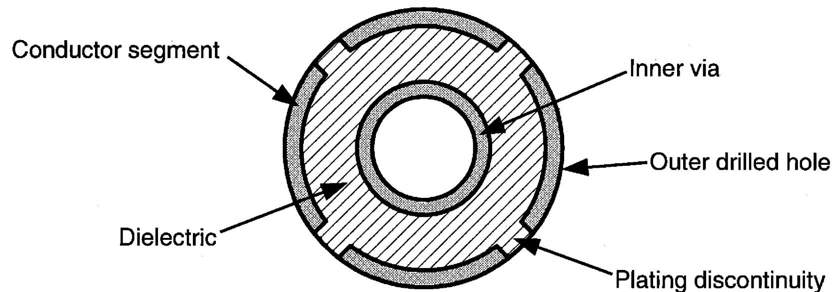

Figure 1-12: Cross-section of coaxial via structure [Dougherty].

Using multi-connection vias for large switch arrays was proposed in 1984 [Milosiu] to connect horizontal to vertical PCB layer traces placing solid pins into two conductor vias. Arranged in a rectangular array, each via could switch a connection on by placing a connector in it. The proposed via structures, shown in Figure 1-13, were low aspect ratio and manufactured by standard masking and plating processes. The connector is described as a pin that connects the two halves of the hole together, much like a banana plug would.

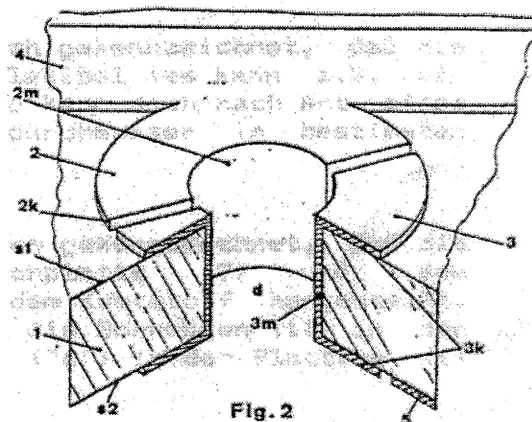

Figure 1-13: Switch-via, German patent DE 3422094 A1 [Milosiu].

In 1991, multi-connection vias, referred to as “bifurcated” plated through holes (BTH), were again proposed [Barnhouse]. Increased density and better routability were cited as benefits. Potential manufacturing processes included masking and etching followed by material removal

with water, laser, or conventional cutting tools. Experimental boards were developed with 0.04" diameter vias. Soldered connectors were proposed and developed for two connection pins cut from FR4 PCB stock. Devices that connect to the PCB were also proposed using multi-connection vias to compete with dual-inline packages. Concerns about processing include cost, thermal failure potentials, and wave solderability.

In addition to the work presented above, two other's are worth mentioning: layer interconnection manipulation by [Akihiro] and bypass capacitor mounting inside the PCB by [Lenkisch]. Therefore, from the literature and industry search, multi-connection vias were conceived around the same time that multi-layer printed circuit boards were being developed. Very little development, beyond proposal, was executed or published on the subject. The available material suggests a thorough exploration of benefits, applications, and manufacturing processes has never been performed.

1.3 Summary

All prior work suggests greater density and better signal performance is possible by splitting the conductor in the via. There is, however, no experimental or theoretical evidence to support this directly. This chapter has made the case for the future demands of high frequency circuits. It outlines the interaction of different elements in and connecting to the PCB. Maintaining the integrity of signals as they pass to the board and between layers in the board represents a major performance bottleneck to current and future electronics.

2 Overview

This thesis focuses around two problems of PCB layer and device interconnection: signal performance and density. As device operating frequencies or clock rise times increase, signal integrity is more difficult to maintain. The high frequency models of transmission theory best describe this phenomenon. The signal quality suffers when the impedance of the transmission structure changes, resulting in parasitic wave reflections and in some cases resonation. A secondary related effect is crosstalk, which relates to the electro-magnetic interference (EMI) between circuit structures.

Similar to coaxial type structures show in Figure 1-3, the basic high-frequency electrical circuit structure requires three elements: a signal conductor path, a return or ground conductor path, and an isolating dielectric. The configuration of these elements determines the impedance of the structure at each point in the path. Consider the analogy of water flowing in a channel that abruptly changes size and how energy is dissipated in the resulting back flows and eddies. This is the same in high frequency signals. When a change in path structure changes impedance, some of the signal energy is reflected due to the discontinuity. This is what happens in a PCB when connections are required between layers, (i.e., vias).

A fundamental rule in high frequency design is to eliminate or minimize the number of layer changes in the signal path [Dally]. It is hypothesized that structures analogous to stripline and coaxial structures will inherently have better signal performance. Considering available manufacturing technologies and functional requirements of having a constant signal, ground, and dielectric structure through the vertical interconnection; this mismatch of impedance in the path can be addressed by changing the structure of the via. This is the primary focus of this research. By placing and controlling the geometry of signal, ground, and dielectric structures in the signal-path transition between layers, this discontinuity can be minimized or wholly eliminated.

Density is a secondary, yet important, concern in this research because the PCB layer-to-layer interconnection is a significant factor in board layout density. The development of any new layer-to-layer interconnection structure must take density into account. It is, of course, desirable to improve board density in addition to increasing signal performance. While the two are not necessarily mutually inclusive, it would be unacceptable to have large density decreases to gain

better signal performance in all but a few cases. In order to monitor how a proposed new structure will affect board density, normalizing factors are developed allowing for equitable comparisons. Prior work by other groups suggests that merely splitting the via into multiple connections will increase density. While it stands to reason that creating richer three-dimensional structures will inherently have greater density, this is an oversimplification. In fact, in some configurations, density is worse because routing is not taken into account. What is developed here is a theoretical model that uses routing as a normalizing factor, allowing for proper comparison of different structure densities.

New board layer-to-layer interconnection structures and proposed manufacturing methods are developed in this thesis to address both of these concerns. Experimentation is used to verify some of the proposed manufacturing processes, and both simulation and experimentation are used to verify signal performance of the new structures.

Many processes for manufacturing multi-connection vias are considered in this thesis, including: waterjet cutting, broaching, laser machining, EDM, ultrasonic machining, and etching processes. Because the scope of this research is confined, only the process of broaching and wire-EDM was taken to the experimental level. Manufacturing process selection and optimization is not the central focus of the thesis, thus the first successful process was developed to a proof of concept level, and all other processes were treated on a survey level. This approach allows the remainder of the thesis to focus on the design and performance aspects of multi-connection vias.

With these new elements in the PCB design toolbox, corollary design opportunities arise. The final part of this research considers some of these opportunities. While the design of the via itself has many possibilities, the design of devices that connect to the via may provide even greater benefits. Developed are concepts for both connectors and devices that connect to the PCB. As with the layer interconnection device and connector, performance is compared using simulation and experimentation.

Thesis outline

The flow of this thesis follows the same basic logic illustrated in Figure 2-1. The next two chapters address the "why" or the justification for this work with a focus on signal performance and density to provide a roadmap of what these two performance parameters are sensitive to. A discussion of the manufacturing processes that could be employed follows. Finally, design

applications are explored, including PCB layer connection, board connector, and device connection. The thesis concludes with an outline of the future research required for production, focused on the signal performance design tools, manufacturing process development, and product design.

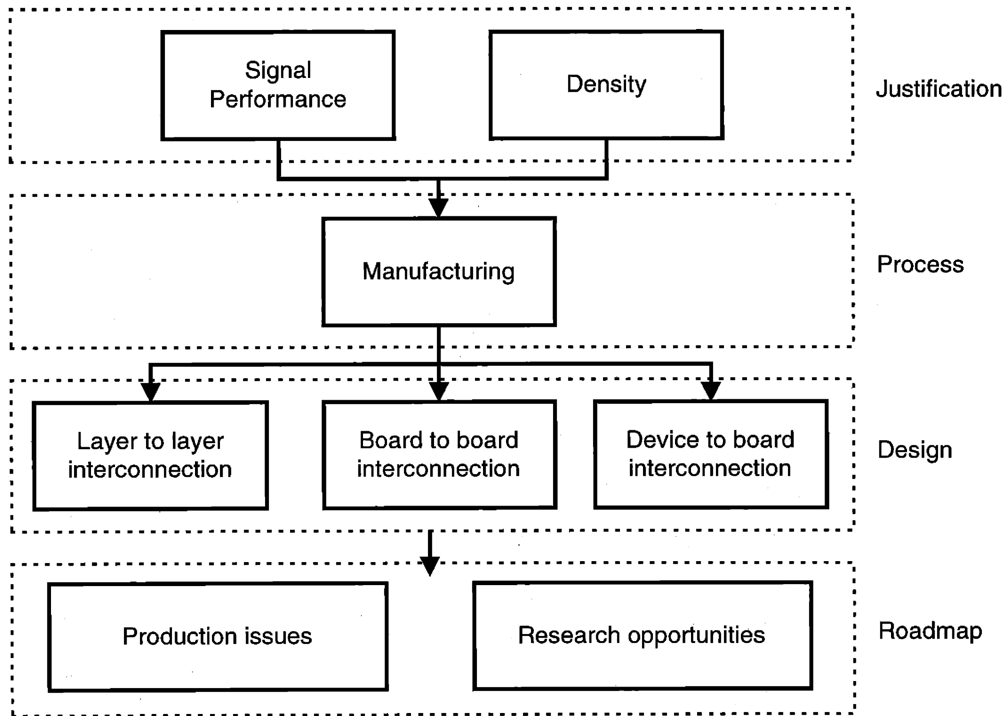

Figure 2-1: Flow of thesis.

While it is impossible to fully explore all the possibilities in this thesis, development of this new element in the PCB interconnection toolbox offers designers valuable opportunities not yet considered. These design opportunities will present themselves in cases where board launch is critical from a signal performance and/or density standpoint. More importantly, however, is the development of methodologies for measuring and comparing new designs.

3 Electrical signal performance

This chapter compares the proposed via structures to conventional structures for signal performance required for supporting the signal bandwidth of current and future devices. According to industry expectations for future demands on PCB performance (shown below in Figure 3-1), PCB frequencies and clock-rise-times will have to increase more than two-fold over the next ten years. The primary concern for the high-frequency board designer is the integrity of the signal as it traverses through the circuit. The vehicles for this transmission are impedance-controlled structures, as those discussed in Section 1.1.1.

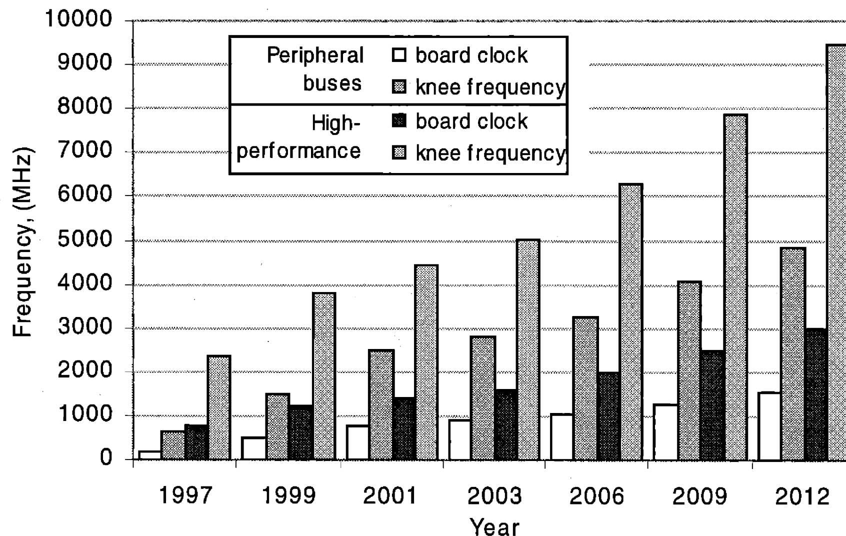

Figure 3-1: Design frequency as a function of clock speed, with SIA data from Table 1-1 (assumes 80/20 clock).

If a signal line is perfectly impedance matched, the signal will see no transitions that provide points of energy loss. The only losses in a perfectly matched straight signal path are those from the dielectric, which are length-of-trace dependent, i.e. attenuation. Attenuation is a significant problem in larger PCBs, like backplanes, where the trace lengths are long compared to the wavelength of the signal.

When there are impedance discontinuities in the line, additional energy is lost and the signal is weakened. The conservation of energy causes this lost energy to have several effects on the circuit. First, part of the signal is reflected back towards the source. This reflection can show up as noise on the lines. If two impedance mismatches are set at a distance approximately an

integer multiple of a quarter the wavelength, the reflections will resonate between them. A common case is that of short unterminated lines (stubs), where the signal goes to the end of a line that connects to nothing, causing all the signal energy to be reflected.

Second, if the line is not fully controlled (i.e., completely bound by ground structures) within the range of other signal carrying lines, EMI will result. EMI reduces the energy of the signal, and these free energy waves cause or induce crosstalk to other circuits. Crosstalk is the induced signal from the electromagnetic field surrounding a signal line, which can also occur from the board to the device above the board and show up as noise on a nearby victim signal lines. Devices have maximum noise budgets which they will safely tolerate before erratic behavior occurs. See Appendix B for a more detailed explanation of high frequency signal propagation.

This chapter looks at the transmitted and reflected energies of multi-connection vias by running a series of simulations and presenting experimental data that reduces the simulation work to practice. It further compares the two sets of data, simulation and experimental, for correlation. Both layer-to-layer interconnection and device or connector launch are considered. In all cases, conventional technology benchmarks are included for comparison.

3.1 Simulation

A three-dimensional full-wave finite element method (FEM) is employed to fully understand the high-frequency signal flow through these new structures. This is necessary because a two-dimensional solution would neglect important ground plane interactions and would not provide complete field visualization. The method employed is a frequency domain solver that provides information like S-parameters (scattering parameters) of the input and output ports and single frequency (sinusoidal) field plots. The solutions are swept from 500MHz to 5GHz to illustrate the frequency-dependent effects in a range that includes today's and future devices.

To perform a comparative study of the multi-connection via structures, a benchmark case that represents a standard via pair is established and shown in Figure 3-2. This single-ended signal line employs a 0.559mm signal and ground vias placed 1.5mm apart. The PCB is 1mm thick. All other structures which carry single-ended signals are compared to this benchmark structure. The virtual test apparatus is a 50Ω microstrip running to a 50Ω PCB trace, to the via, and back out the same structure. The PCB structure is comprised of four ground planes and dielectric (FR4) sized large enough to ensure that fields die down before reaching the outer limits. All the simulations conducted use lossy dielectrics. The dimensions of the virtual apparatus are the

same for all tested structures. The simulation results in a two-port S-parameter matrix embedded in the test apparatus.

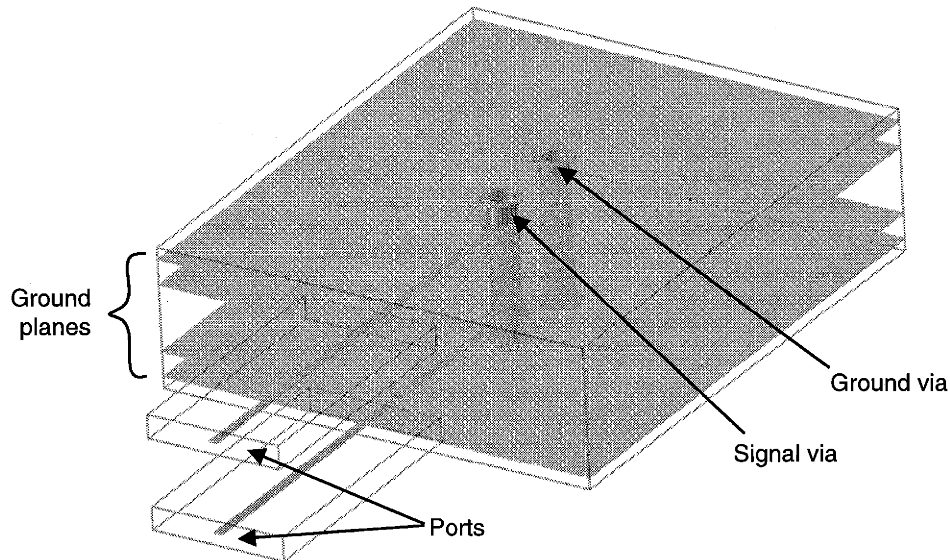

Figure 3-2: Single ended standard via pair.

The basic geometry of the single-ended test, shown in Figure 3-3, is parametrically varied to characterize the effects of each parameter on single-ended signals propagating through a multi-connection via. Three cases are explored. First, the ground and signal trace sizes are kept the same, the via diameter is held at 0.559mm, and the gap is varied. Second, the gap is held constant while the signal arc length is varied, and third, the gap is held constant while the signal arc length is varied with a 1.0mm diameter via.

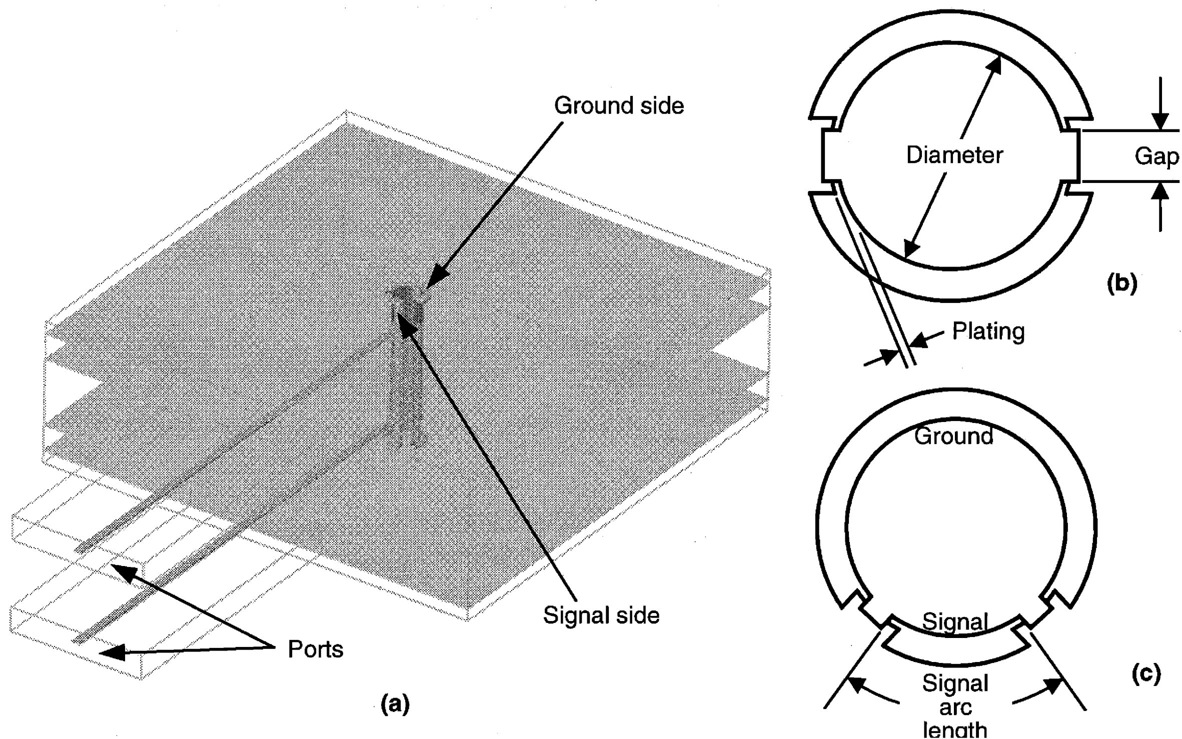

Figure 3-3: (a) Single-ended multi-connection via test structures (b) horizontally split via geometry (c) non-symmetrically split via geometry.

The goal of this set of simulations is to illustrate and prove that multi-connection vias are inherently impedance tunable. Standard vias, on the other hand, do not have definable impedance. The parameters are varied in a manner to show sensitivities, and the results are presented for reflected and transmitted energies. For visualization purposes, electric field plots illustrate the interaction of the elements.

3.1.1 Single ended via structures

The first circuit structures of concern are single-ended vias. They represent the simplest routing constructions, where the signal runs between ground return structures. The only difference in a differential signal is that the return path is a discrete conductor equal and opposite to the other conductor. The ground in a differential signal acts as a drain for leakage caused by symmetry imperfections. Due to stability issues with the solver only single-ended models were run. This is acceptable because single-ended results will map into differential structures well enough for the scope of this research, such that solution trends will be identical for both cases.

3.1.1.1 Affects of varying the gap on reflections and transmissions

The width of cut in the plating or the gap (shown in Figure 3-3) is the first parameter varied while keeping the diameter at 0.559mm and the cut symmetric between signal and ground. When the gap increases, the signal conductor-arc length decreases, as does the ground conductor due to symmetry. The gap is where the closest coupling between the signal and ground occurs; thus, it is likely that varying this gap will have a significant effect on reflections and transmission.

The de-embedded reflected power, plotted in Figure 3-4, shows that the reflections drop off to near zero as the gap is widened. It is expected, however, that if the gap were further widened, (requiring a larger diameter via) the reflected power would eventually increase.

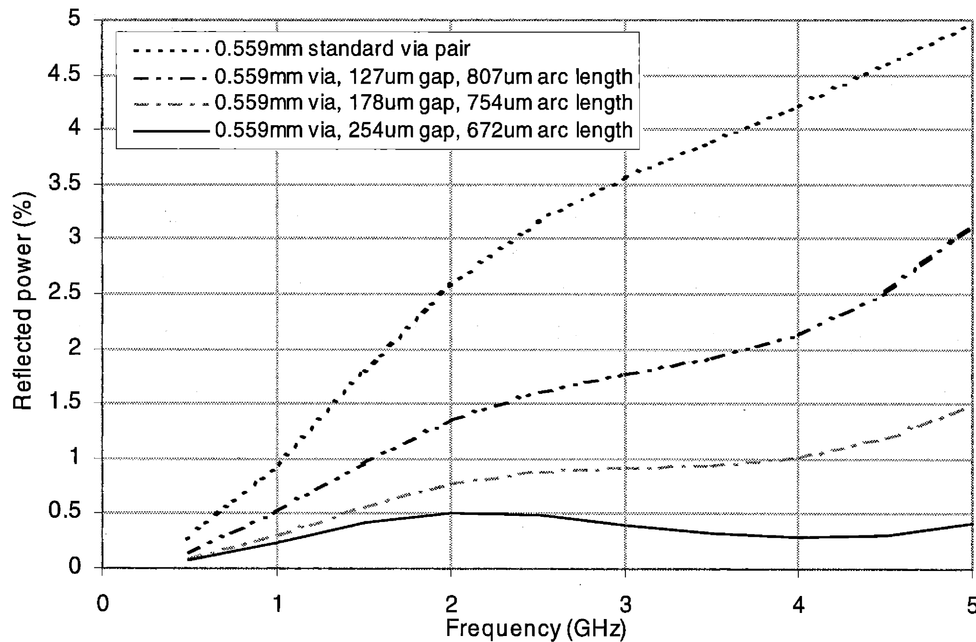

Figure 3-4: Reflected power, comparing gap widths for 0.559mm vias.

The energy that is reflected in the conventional via increases at a greater rate than that of multi-connection vias, thus the benefits of the new structure is greater at higher frequencies. In the best-tuned case, the reflected energy is negligible across the frequency range. It is suspected that the second order wave on all of the curves is due to reflections from the stubs at the end of the vias. This indicates the stub reflections begin to dominate above the 5GHz point by the increase in the upward slope for this particular stub length.

The transmission, plotted in Figure 3-5, is consistent with the reflections. The decrease in reflected power increases the transmitted power proportionally. This is an important interaction to watch, because it is possible to decrease both the reflections and the transmission, often occurring where losses (EMI) are high (and provides a sanity check on simulations). It is important to note that even the best case (254μm gap) has a decreasing transmission slope not equal to the reflection slope, because EMI and conductor losses for all structures do not directly show up on either port, but do attenuate the signal. The field containment with a larger gap will also be less and thereby increasing the EMI losses. This attenuation increases with frequency.

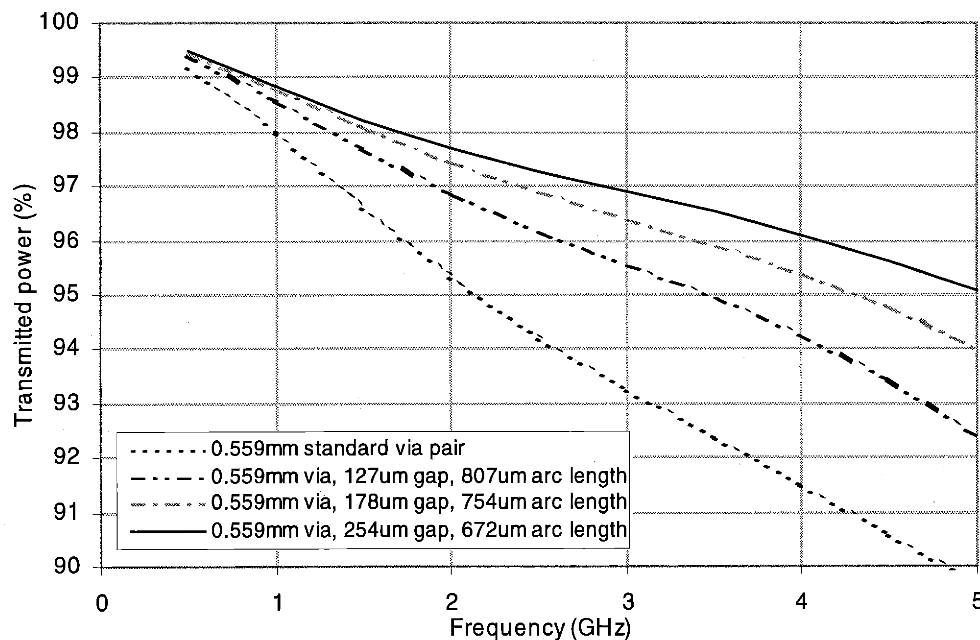

Figure 3-5: Transmitted power, comparing gap widths for 0.559mm vias.

3.1.1.2 Affects of varying the conductor ratio on reflections and transmissions

Figure 3-6 shows that varying the signal conductor size tunes the via circuit better than varying the gap and keeping the ground and signal symmetric. In this case, as the signal arc-length decreases below 520μm, the reflections begin to increase at higher frequencies. This implies that these via structures are inherently tunable to the circuit. Conventional plated-through vias can attain performance gains by decreasing the size and increasing the ground clearance, both of which are difficult to achieve. In the end, conventional vias cannot truly cross over a tuned point.

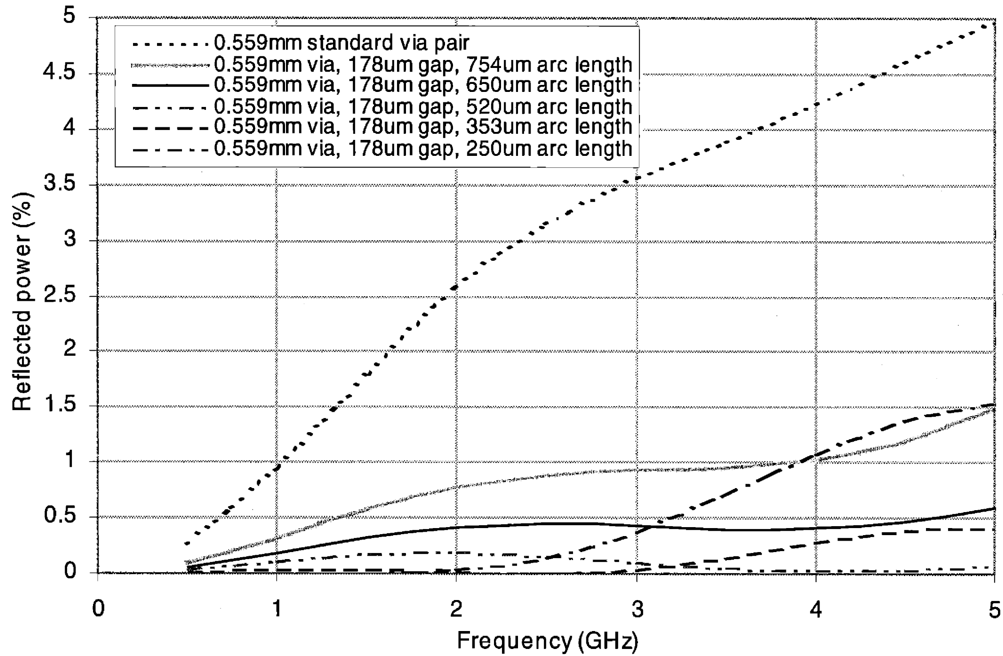

Figure 3-6: Reflected power, comparing conductor ratios for 0.559mm vias.

In Figure 3-7, transmission characteristics follow the reflections as expected. The 5GHz transmission of the best case via is 95.5%. This is half a percent better than the 254μm gap case shown in Figure 3-5, which is exactly equal to the reflected power of that via (note, that it is assumed that relative accuracy of the solver is very high). This illustrates how well these results follow the conservation of energy laws. The remaining loss is attenuation and EMI.

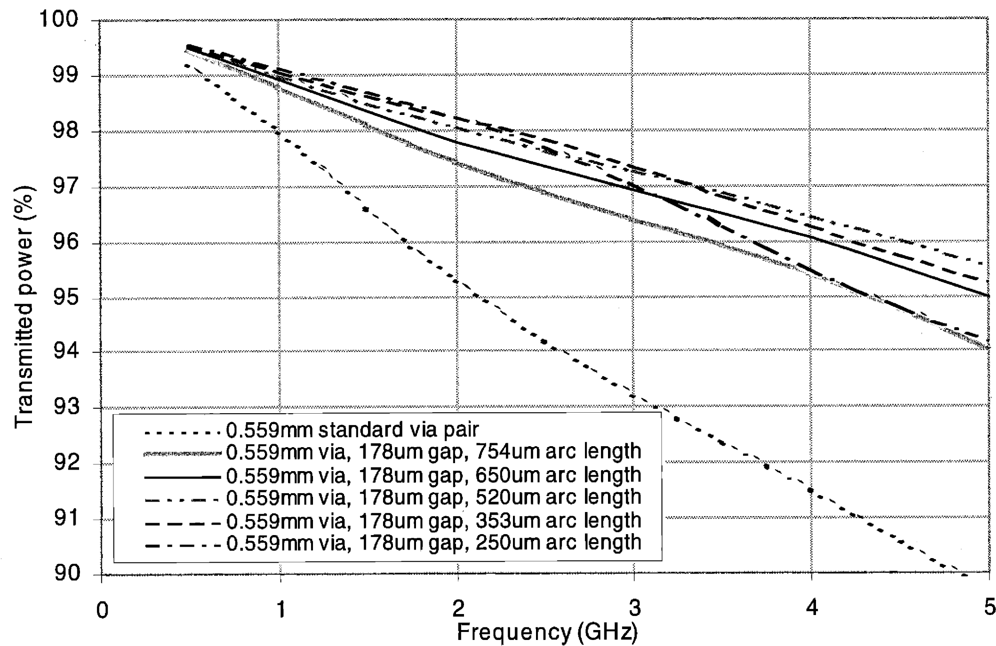

Figure 3-7: Transmitted power, comparing conductor ratios for 0.559mm vias.

3.1.1.3 Affects of varying the via diameter on reflections and transmissions

Increasing the via diameter traditionally increases the reflections and decreases the transmission, thus indicating sensitivity to diameter. However, as shown in Figure 3-8, reducing the signal arc length reduces the reflection down to the same range as the smaller multi-connection via. As with previous cases the transmission (Figure 3-9) follows conservation laws well. Thus, the larger multi-connection via is as tunable as the smaller diameter multi-connection via. This is very significant. It means larger diameter vias, which are easier to manufacture, employ better impedance control than the smallest standard via. In other words, reflections and transmission in standard vias are highly sensitive to via diameter, while impedance-tuned multi-connection vias are not.

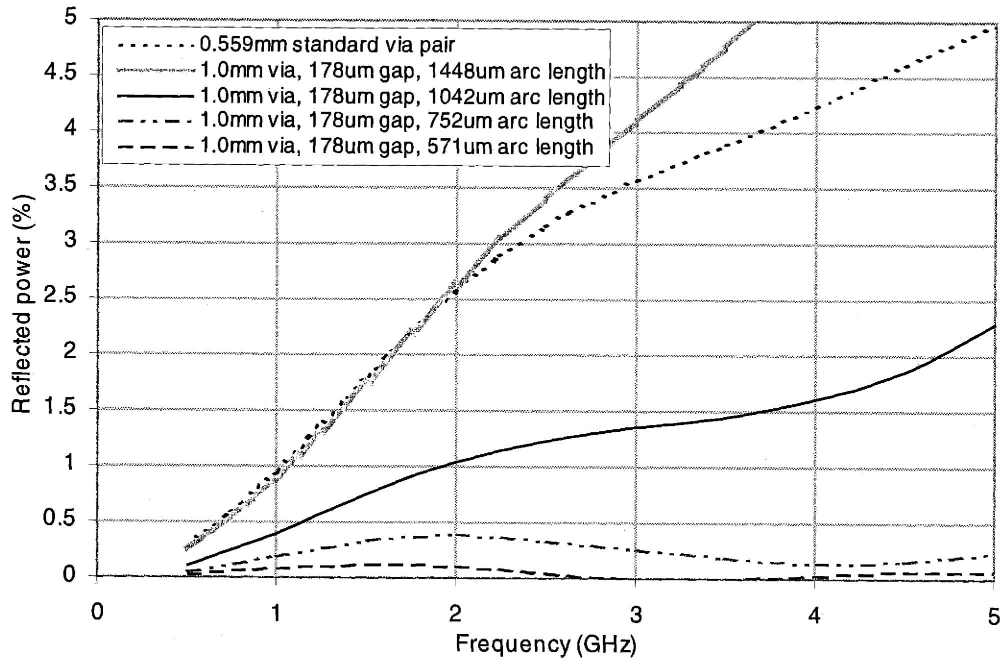

Figure 3-8: Reflected power, comparing conductor ratios for 1mm vias.

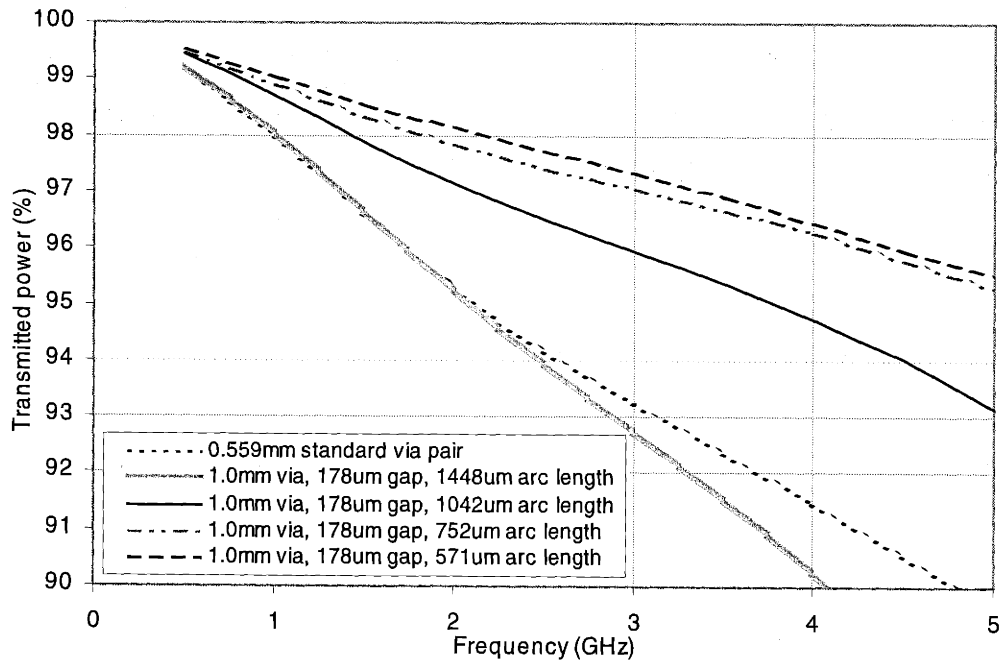

Figure 3-9: Transmitted power, comparing conductor ratios for 1mm vias.

3.1.1.4 Electric and magnetic fields

This section presents field plots for the structures discussed above. They are all shown at 5GHz to represent the worst-case field effects. Both the standard benchmark via and the 571μm signal arc length 1.0mm-diameter via are shown. The large multi-connection via represents the most likely candidate for initial development, because larger vias are split more easily. The smaller, 0.559mm-diameter case has similar field plots to the 1.0mm case. Field plots are on two-dimensional planes, all of which are in directions that have the highest field intensity. Both the magnetic (H-field) and the electrical (E-field) fields are plotted in all cases.

First, consider the standard 0.559mm-diameter via pair sectioned through the signal path and shown in Figure 3-10. There is little or no field inside the via, except at the very ends, where EMI broadcast occurs. The electrical field emanates radially around the signal via and toward the ground planes, as shown in Figure 3-11. While the electric field shows no interaction with the ground via, the magnetic field does. This is primarily because the electric field is strong at the surface of the signal conductor and distributes to ground structures (both ground planes and via) as widely as possible. Thus, distribution of electrical field on the ground structures decays rapidly with distance. Magnetic fields, on the other hand, concentrate where the current flow is strong, thus verifying that the ground via does function as a current return.

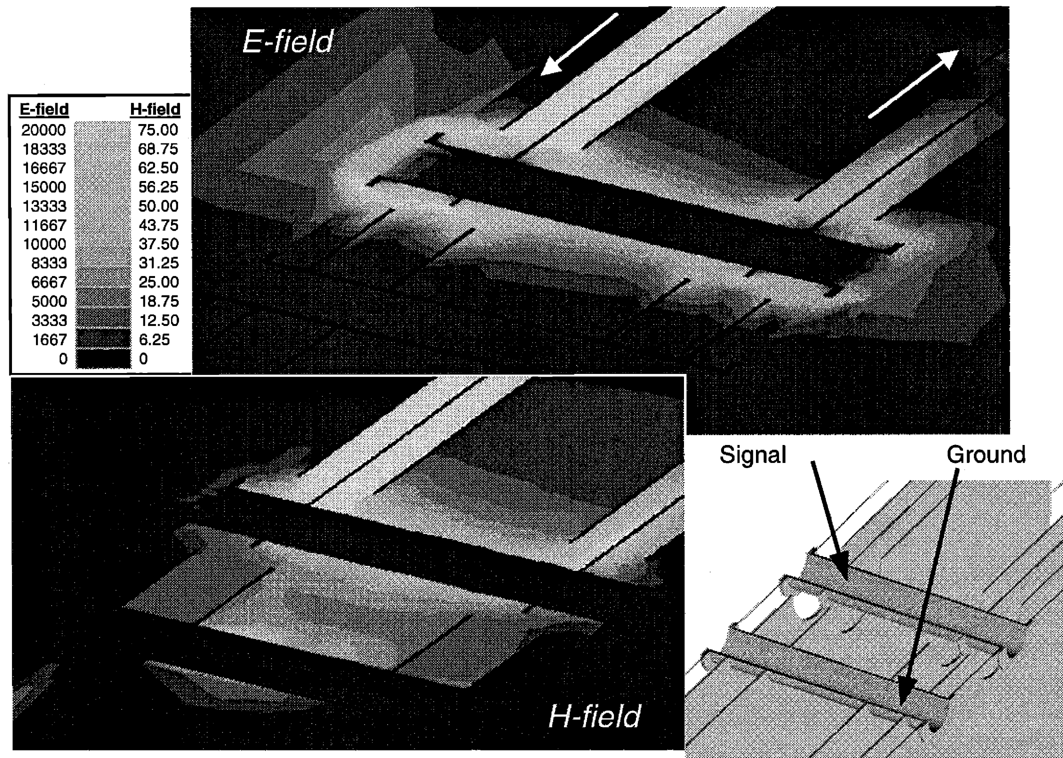

Figure 3-10: Electric field at 5GHz for standard 0.559mm via pair, sectioned through signal path.

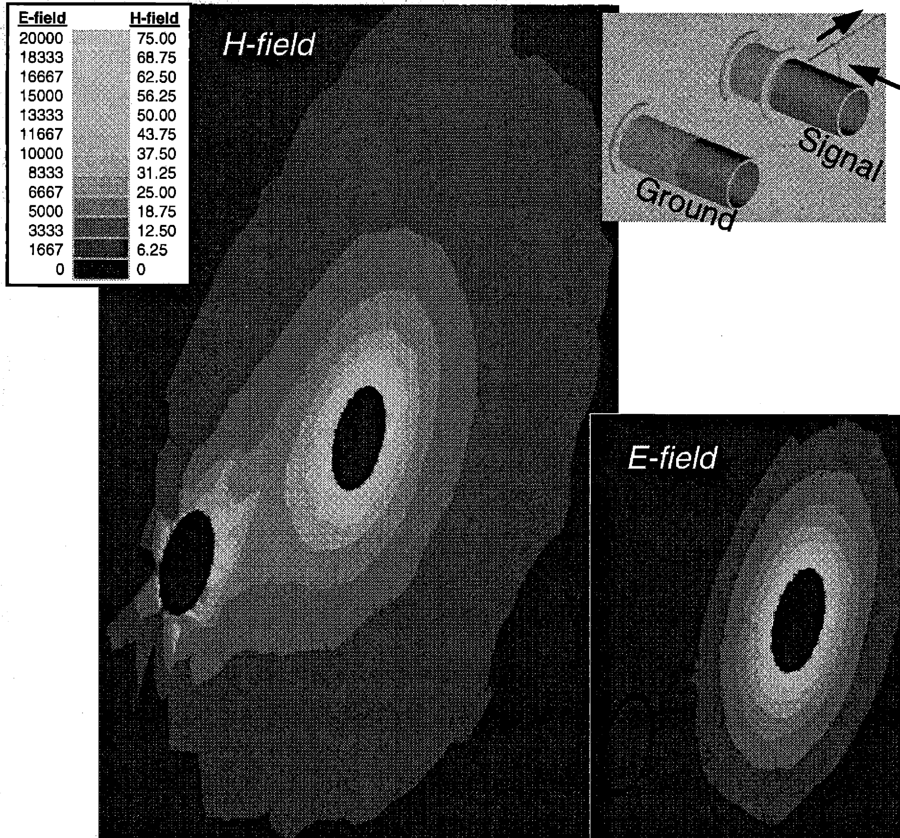

Figure 3-11: Electric field at 5GHz for standard 0.559mm via pair, sectioned normal to vias.

In regions of high field strength, there are opportunities for inducing signals (crosstalk) to circuitry and devices that pass through the field in and above the board. It is important to understand that crosstalk occurs with both magnetic and electric fields, because both are forms of field energy. The only difference is that electric fields couple capacitively and magnetic fields couple inductively. Figure 3-12 shows high field strength in regions above, below, and between the vias. Note that the magnetic field does not broadcast EMI above or below the board like the electric field does. The field distribution not only indicates potential crosstalk issues to traces routed nearby, but also poor field control in the transition between layers.

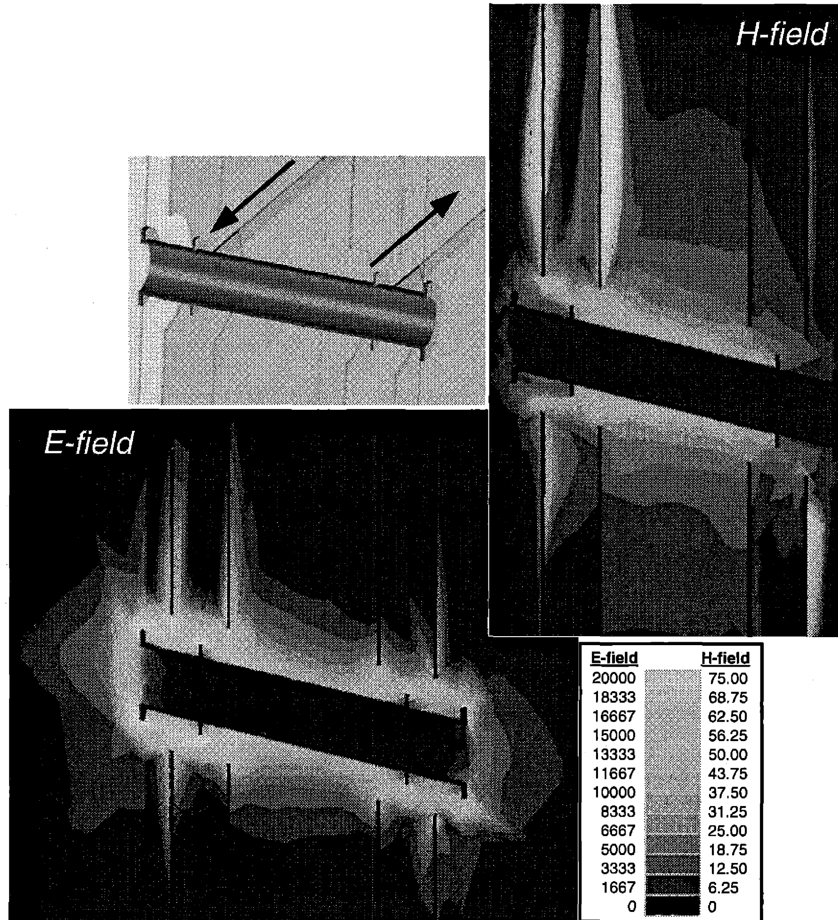

Figure 3-12: Electric field at 5GHz for symmetric 254μm wide split 0.559mm via, sectioned normal to signal path.

In the case of multi-connection vias, the field is much better controlled between the signal side and ground side of the via, as shown in Figure 3-13. For these structures, the return path is closely coupled to the ground side. Figure 3-14 shows how the maximum field strength is in the gap for both electric and magnetic fields, which helps explain why the results of the parametric simulation study are sensitive to the gap, see Figure 3-4.

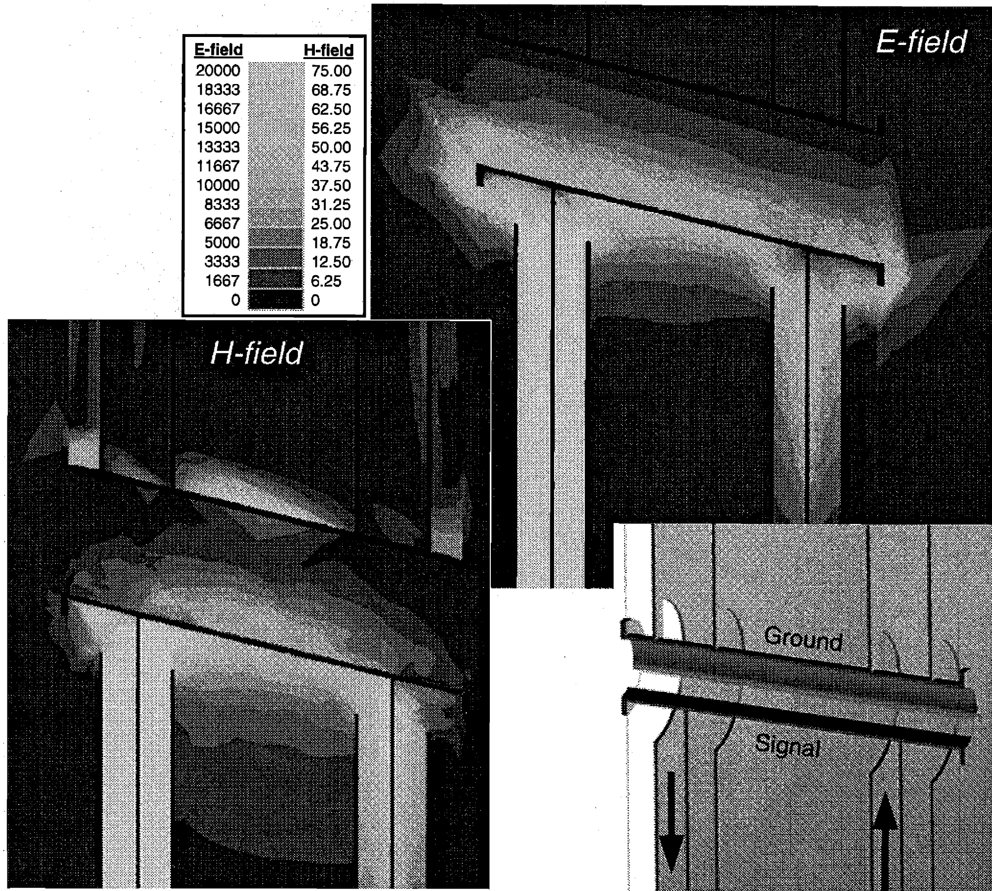

Figure 3-13: Electric field at 5GHz for standard 0.559mm via pair, sectioned through signal path.

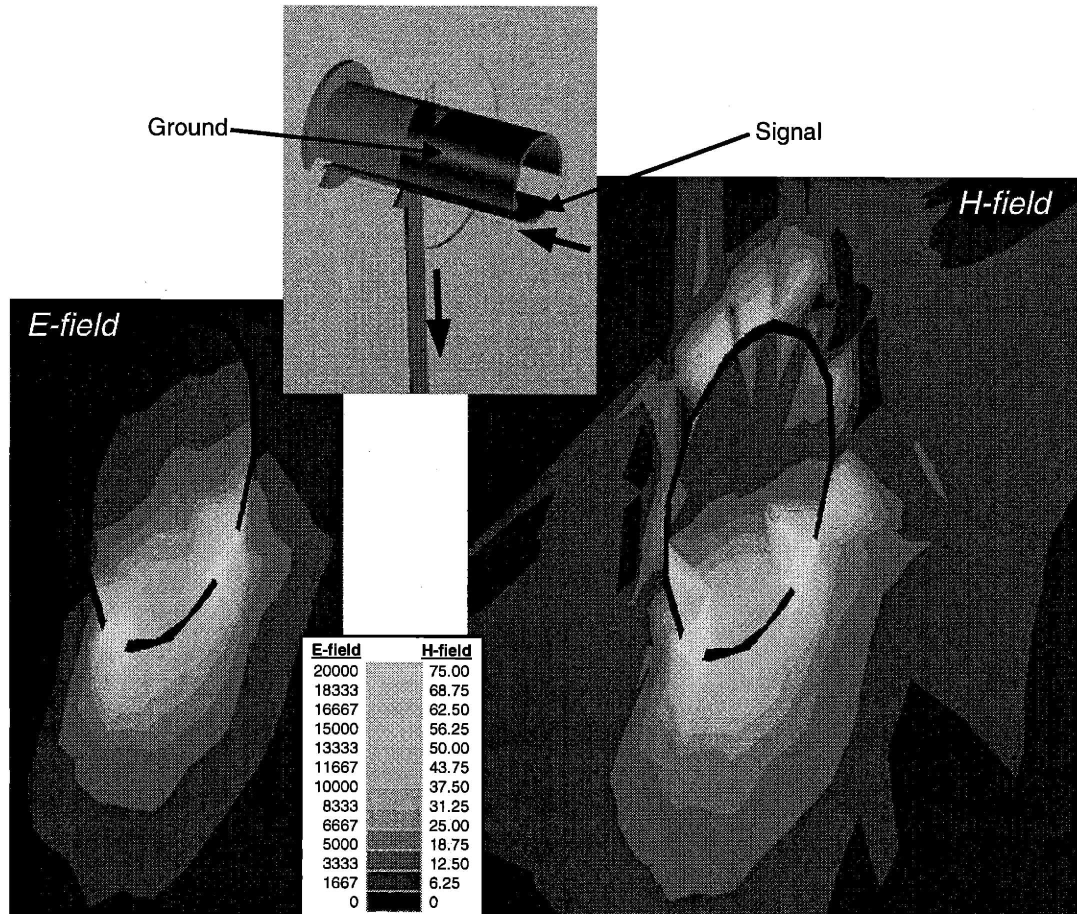

Figure 3-14: Electric field at 5GHz for symmetric 254μm wide split 0.559mm via, sectioned normal to via.

Cross-section comparisons of the different via structures (as shown in Figure 3-15) illustrate how field size and intensity are controlled with the multi-connection via structure. There is essentially no electrical field strength and very little magnetic field on the outside of the ground segment. This supports conclusions in Section 4.2.1 regarding routablilty near the ground side of multi-connection vias. Figure 3-15 shows that the overall field containment for the multi-connection via is much better than the conventional case, yielding less potential crosstalk. There is also an efficiency of space by providing a path for some of the field to resolve inside the via, as opposed to the conventional case.

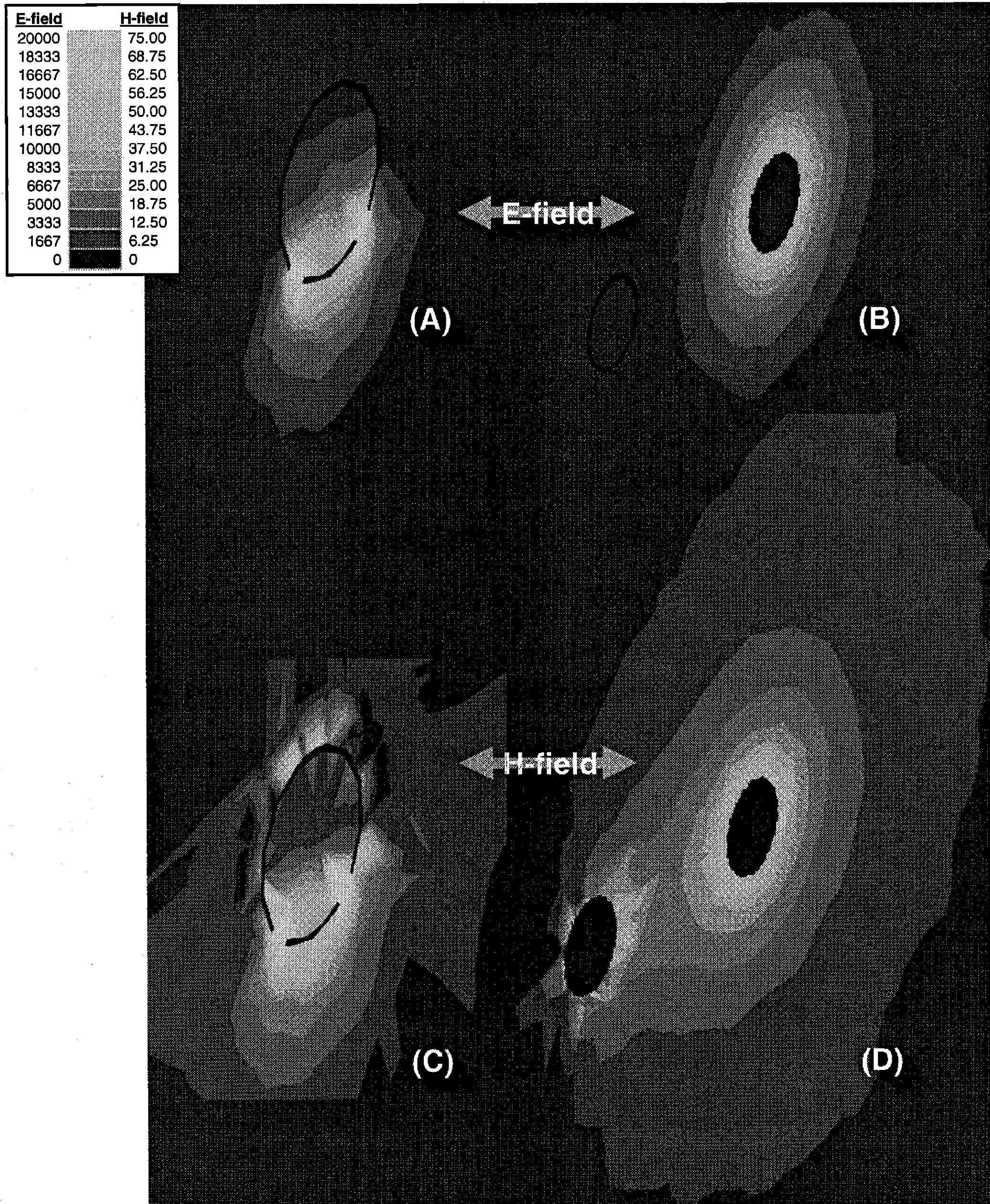

Figure 3-15: At 5GHz, 1.0mm diameter via with 571μm signal arc length, 178μm gap, (A) and (C); 0.559mm diameter via pair, (B) and (D).

3.1.2 Board launch

The launch of a device or a connector into the board is one of the potential areas of development for multi-connection vias. Signal field control between the ground and signal conductors is not handled well in the transition from connector or device into the PCB. To evaluate the potential performance gains, this section compares two launch cases, one for a two-contact pressfit

connector and one for a multi-connection via (there are other conventional launch structures, such as SMT (surface mount technology), which could be compared here too but are not do to limitations of scope). The two-contact pressfit connector is similar to commercially available high-end back-plane connectors. Figure 3-16 shows a simplified simulation model with one signal pair (the real connector has hundreds of mated pairs). Here, the via size is 0.559mm and the spacing between signal and ground vias is 1.33mm. This case provides the benchmark for comparison to the multi-connection via launch described below.

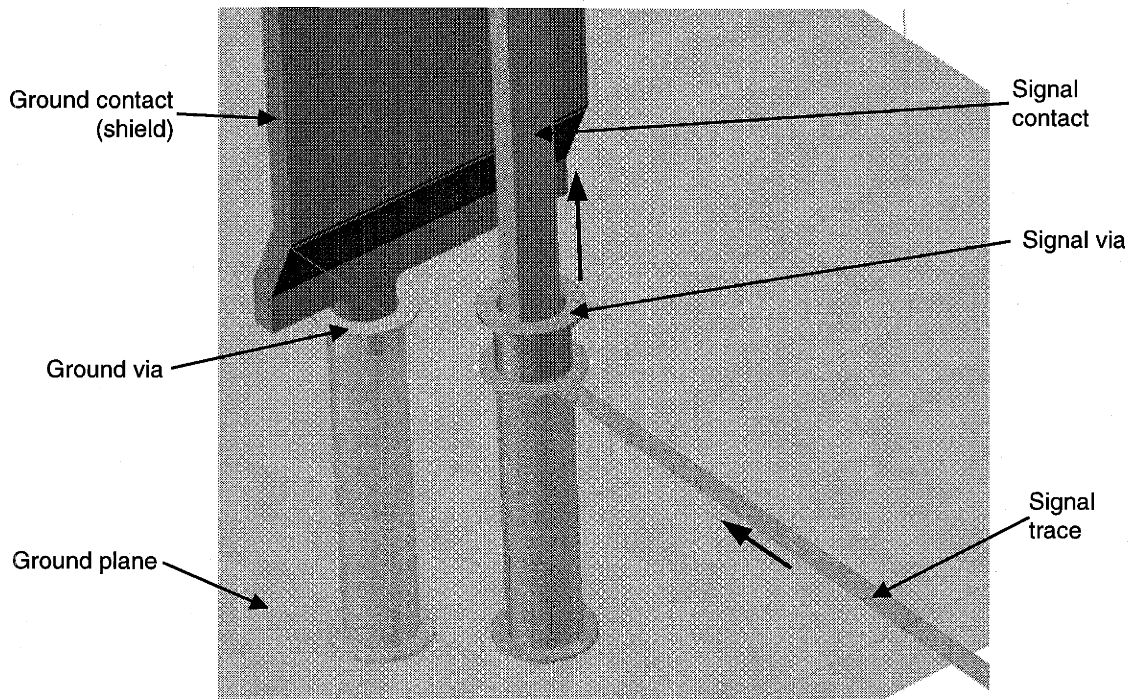

Figure 3-16: Conventional pressfit launch (2mm x 1.75mm pitch x 0.559mm diameter vias).

As shown in Figure 3-17, a 1.5mm diameter is used for the multi-connection via test case. At this scale, the via is easily manufactured and provides plenty of space for a pair of contacts. The signal arc length is set to 540μm and the gap is 254μm. These dimensions were selected based on the design experience from the via simulation studies, to provide a good impedance match to the connector and the PCB trace. In both cases, a signal is launched into the PCB (stripline) and exits on the connector (microstrip), each matched to 50Ω. The PCB dielectric is FR4 and the connector is LCP (liquid crystal polymer) plastic. Both port solutions (S-parameters) and field plots are presented.

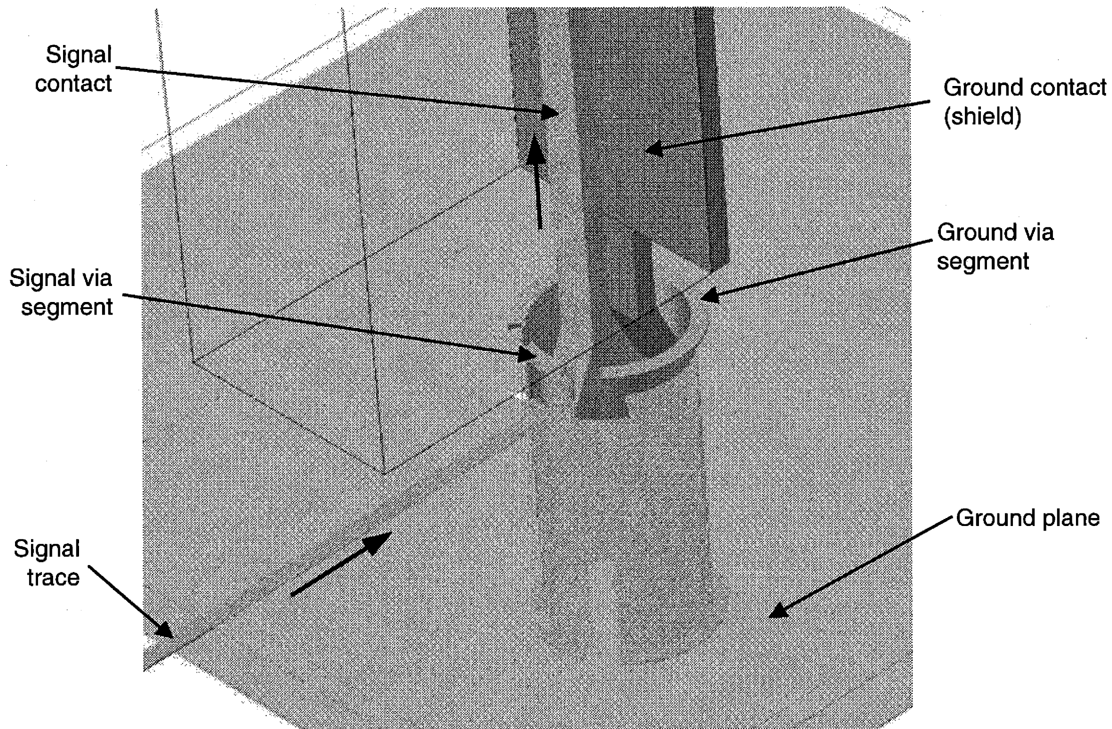

Figure 3-17: Multi-connection via launch (1.5mm diameter via).

3.1.2.1 Reflections and transmissions

As with the via-only cases the port solutions yield S-parameters, which provide reflected power plots (Figure 3-18). This conventional pressfit connector is rated for 4-6% reflection (voltage magnitude) at a 200ps rise time, which corresponds to a knee frequency of approximately 1.5GHz. The reflections for the conventional case have this same order of magnitude considering that broadband reflection is an accumulation of the reflections up to a frequency for which the excitation energy is considered low, i.e. knee frequency. In other words the excitation energy decreases with frequency for fixed rise-time reflections. Therefore, considering this level of acceptable reflection, the multi-connection via launch supports much lower rise times.

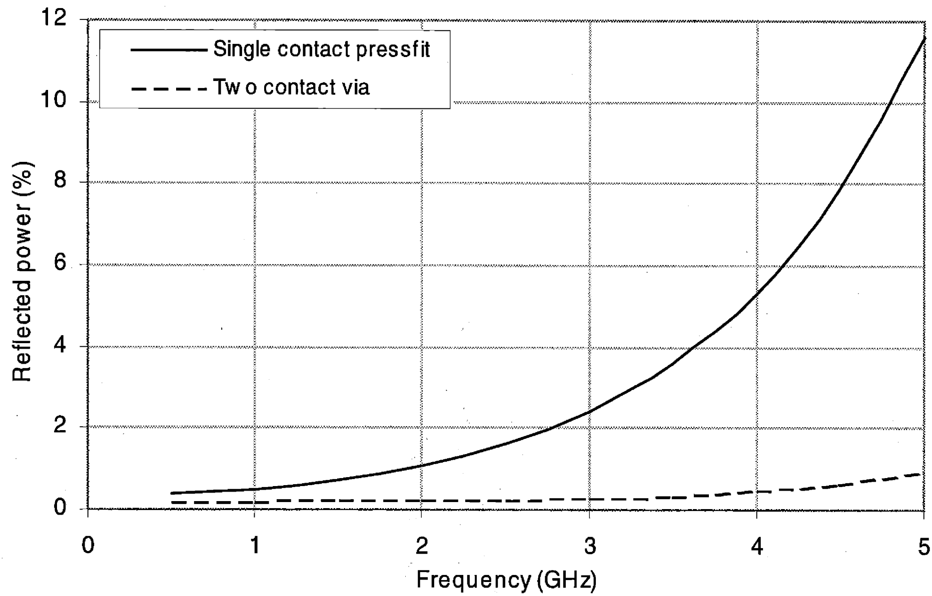

Figure 3-18: Reflected power comparing multi-connection launch to conventional pressfit launch.

The transmitted power is plotted in Figure 3-19. The drop off in the transmitted energy is not as favorable, because the transmitted power of the multi-connection launch at 2.5GHz is the same as that of the conventional technology at 1.5GHz. Therefore, if the transmission is the criteria for acceptable performance, this multi-connection launch would support rise times on the order of 180ps. Decoupling the effects of the reflected energy and transmission line attenuation, provides resolution to these differences. By driving the reflected energy to near zero levels puts the transmissions loss burden squarely on the shoulders of the dielectric materials. Therefore, the impedance-tuned multi-connection via launch can support reflectionless signals up to the range tested here (5GHz), assuming the via stub length is as modeled or shorter. If transmitted strength is not strong enough at this frequency, the only degree of freedom to manipulate is the dielectric material properties.

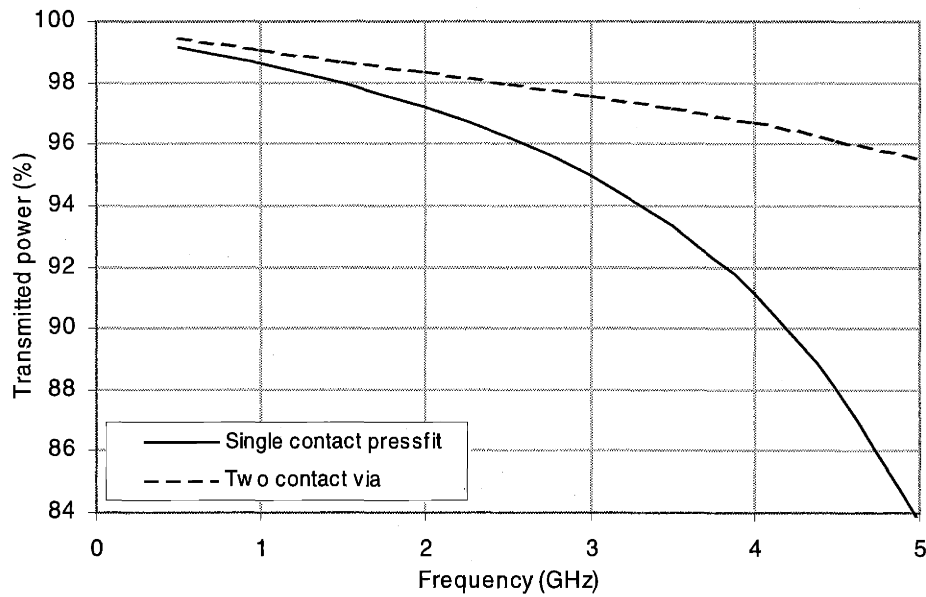

Figure 3-19: Transmitted power comparing multi-connection launch to conventional pressfit launch.

3.1.2.2 Electric and magnetic fields

Field plots for both simulated launches are created for both electrical and magnetic fields. As shown in Figure 3-20, the section normal to the via through the signal trace is similar to that of the conventional vias in the prior section. Where the electric field is strong locally about the signal conductor and the magnetic field is strong between the ground via and signal via.

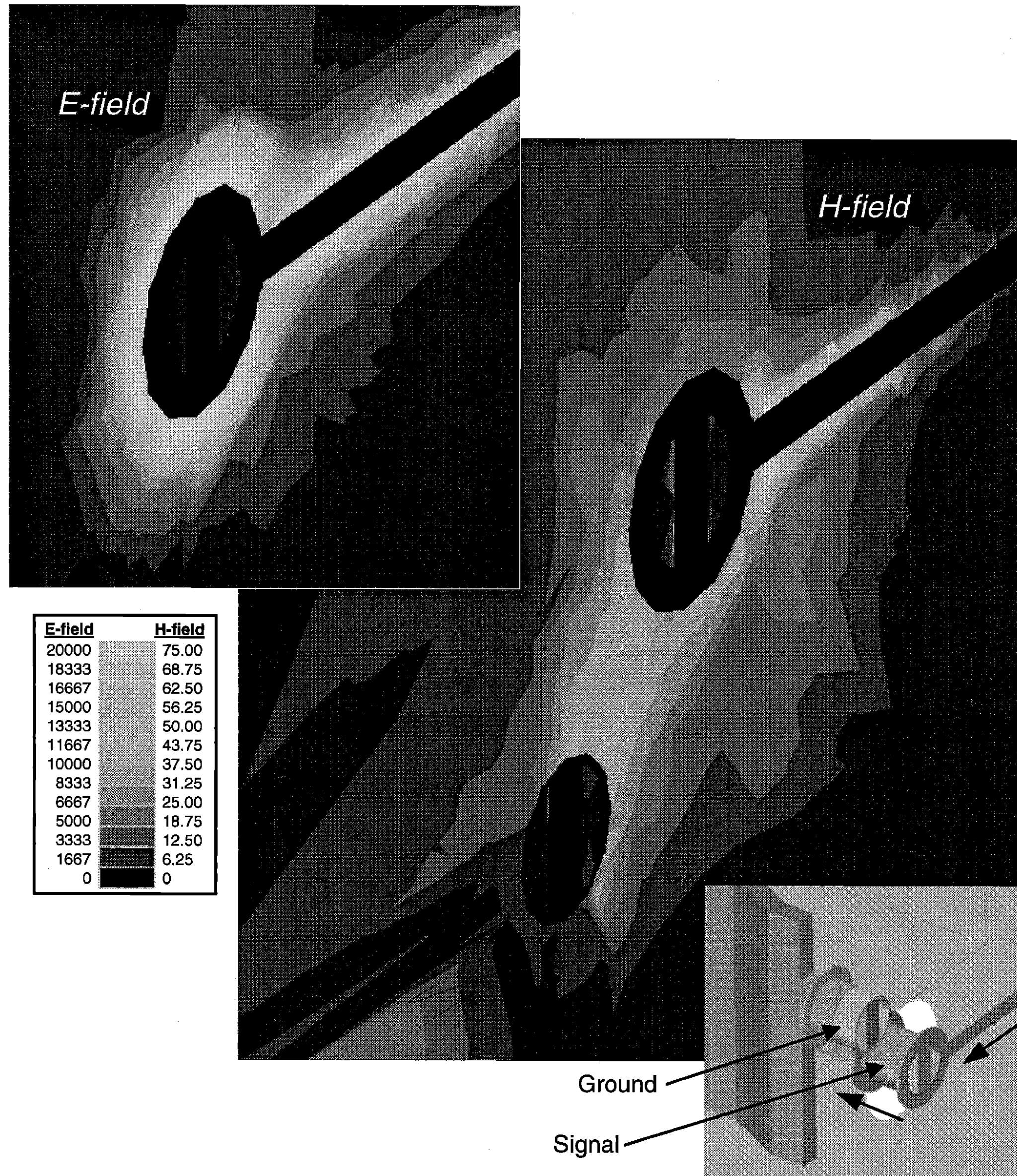

Figure 3-20: Electrical and magnetic fields at 5GHz for conventional connector launch, sectioned normal to via.

Taking a section through the signal path, shown in Figure 3-21, illustrates the discontinuity at that transition. Notice how the magnet field follows the contact into the via, indicating that the current flows to the inside of the via. Because high frequency signal travel on the surface of conductors the current must travel back out of the top the via.

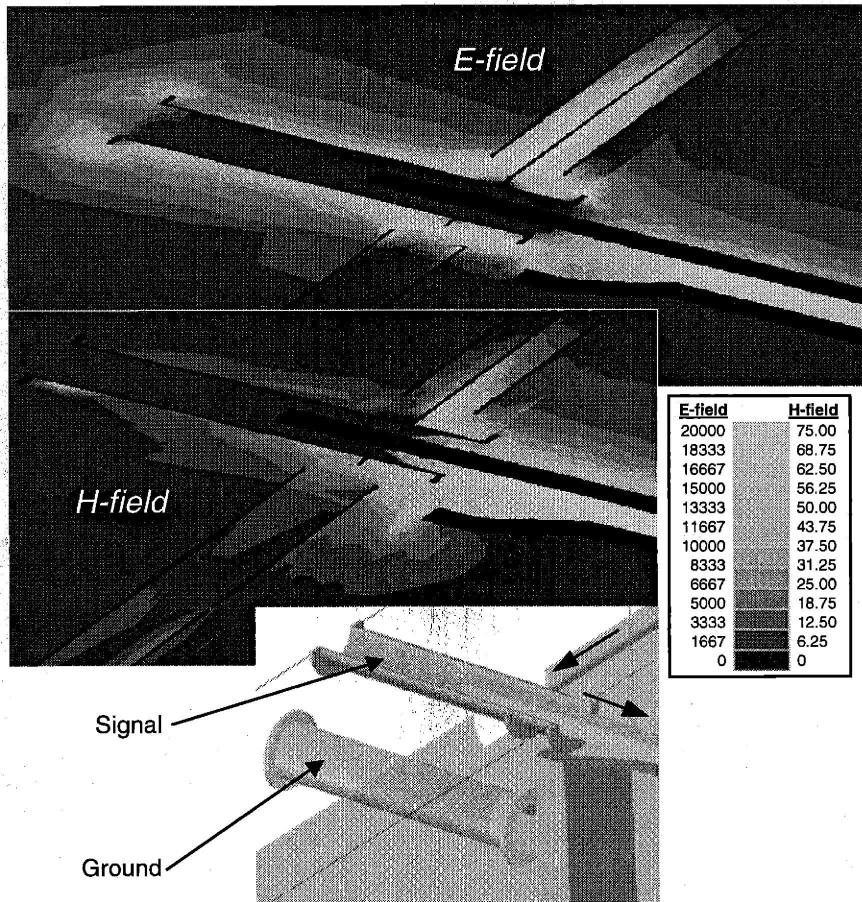

Figure 3-21: Electrical and magnetic fields at 5GHz for conventional connector launch, sectioned through signal path.

Compare these interactions with that of the multi-connection via launch, shown in Figure 3-22 and Figure 3-23. The current flowing into the inside surface of the via has a direct path to the signal conductor in the PCB. Also, note how the field almost completely resolves inside the via. Because all fields require space to travel, using the space inside the via provides for more efficient use of the PCB. Hence, because the layout of connectors occurs in tightly packed arrays opportunities for crosstalk are reduced.

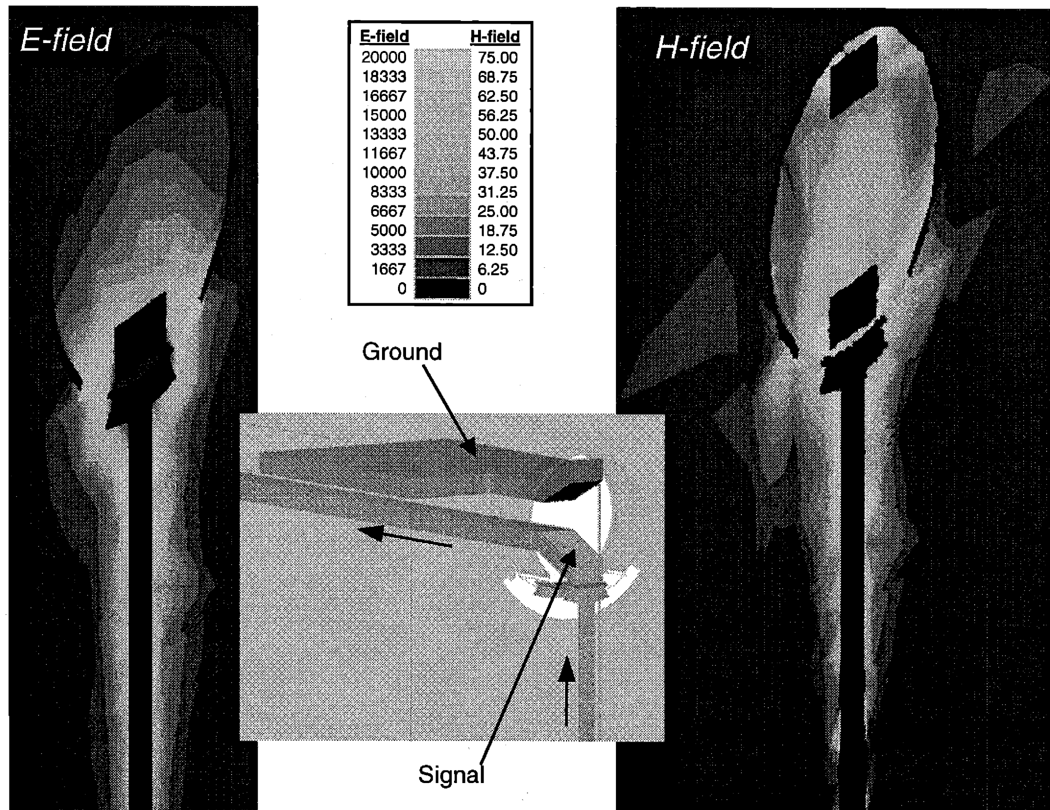

Figure 3-22: Electrical and magnetic fields at 5GHz multi-connection via connection launch, sectioned normal to via.

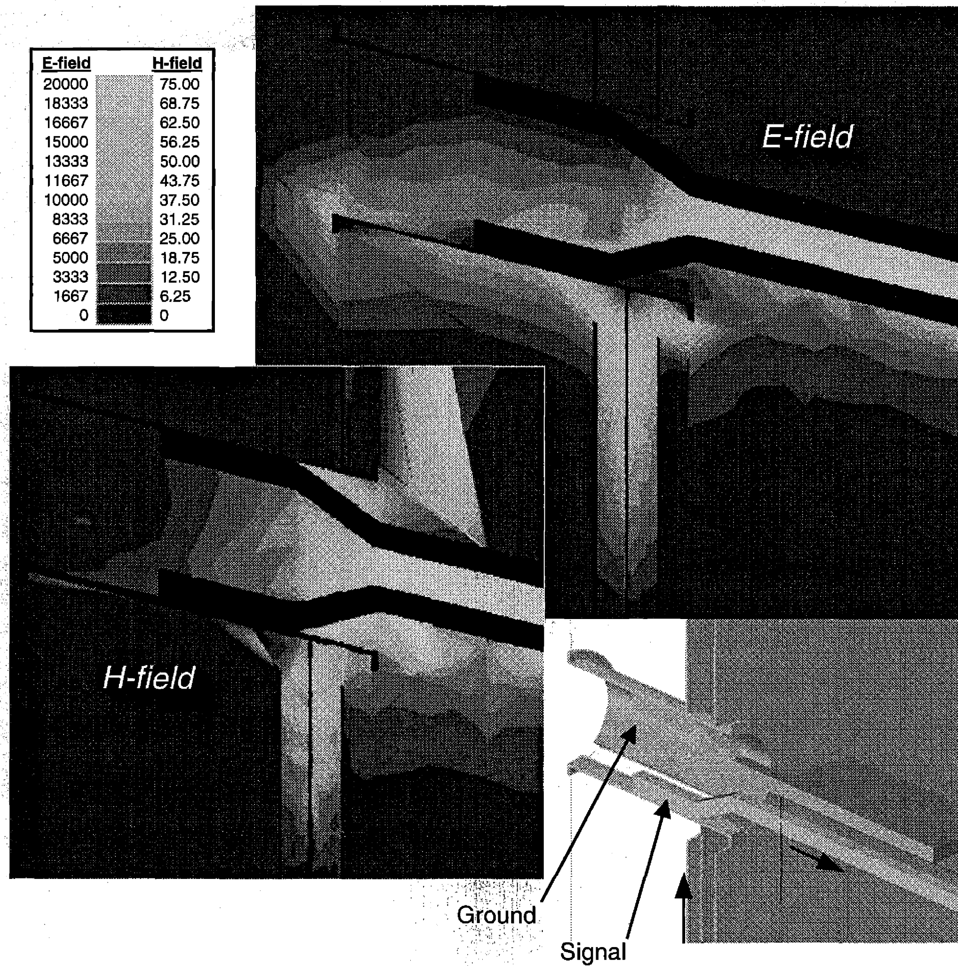

Figure 3-23: Electrical and magnetic fields at 5GHz multi-connection via connection launch, sectioned through signal path.

3.2 Experimentation

The experimentation goals are to verify the simulation results and demonstrate that the performance gains can be reduced to practice. The test PCB, shown in Figure 3-24, provided 38 single-ended and differential via combinations, along with six benchmark cases. It was a 3.2mm-thick, 12 layer board (four internal signal layers) using glass/epoxy (FR4) dielectric. All stripline circuits were configured at 50Ω±10%. All split vias were 1.5mm finished diameter, permitting use of the same tooling for all holes. Conventional benchmark vias were 0.33mm in diameter. Tests were conducted using a Textronix 11801B (w/SD24 sampling heads) TDR (Time Domain Reflectometer).

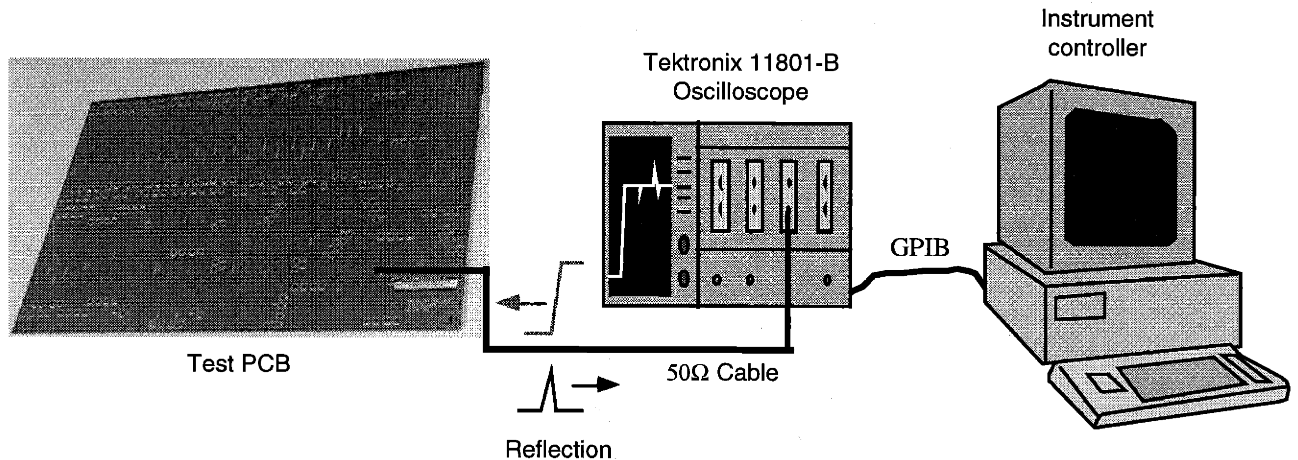

Figure 3-24: Test setup.

Experimental work results are in the time domain, while the simulations are in the frequency domain. This discrepancy imposes a problem in getting exact correlation between the two. It is possible to convert the experimental data into the frequency domain using FFT, but different energy inputs in the excitation mechanisms still prevent exact correlation. In the simulation case, the input energy is the same at each frequency, coming from the sinusoidal wave inputs. While the TDR uses a sloped-step input, in the time domain (100ps rise-time, in this case), such that energy decreases with frequency. This problem is compounded by the signal launch into the test board using SMA connectors, which act as low pass filters on the signal.

There are a couple solutions to this problem, first to characterize the input waveform at the via in the frequency domain and compensate for the difference, and second to use a network analyzer instead of a TDR to experiment in the frequency domain directly and de-embed the test from the test structure. Both of these solutions require a significant amount of experimental work to fully characterize and calibrate the launch into the test. In addition, the launch from the instrumentation into the PCB has inferior high frequency characteristics as compared to the structure under test. Therefore, it was deemed acceptable to keep the two sets of data in different domains and provide a qualitative trend comparison. In the end, this approach provides more than adequate information for deriving strong conclusions.

The results are broken into two areas: signal-ended and differential. Data is normalized for temporal errors and average input and output impedance variations. These impedance variations are due, for the most part, to slight manufacturing errors. All the data is windowed from the

input trace, through the via, and out the output trace, such that the test probe launch and exit are not shown.

3.2.1 Signal ended vias

While higher-frequency PCB differential signal pairing shows the greatest performance promise, especially for long traces, single-ended signals still represent the majority of circuitry today. Hence, all the simulation work was conducted on signal-ended structures. The primary concern is correlating to the simulations, as discussed above. The single-ended vias of the test board are shown in Figure 3-25, where (A) and (B) show the cases that provide correlation to the simulations. In these cases, the gap, arc length, and layer combinations are varied.

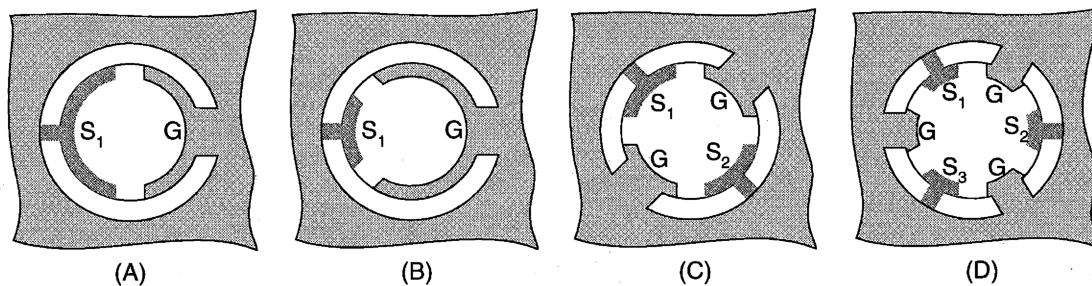

Figure 3-25: Single-end via structures tested

For connection cases (A) and (B) the layer connections are kept the same (signal layers 1 to 4) and the signal arc length is varied. The TDR reflection amplitude is plotted in Figure 3-26 for all cases including the benchmark via. Because all the tested multi-connection vias are the same diameter, the only variable here is the arc length. As shown in Section 3.1.1.3 a large via with a wide signal conductor arc length has worse performance than the smaller diameter benchmark via. As the arc length is decreased, the reflection reduces to near zero (0.31mm case) and then the reflection increases again (0.19mm case). It is interesting to note that in digital electronics vias, are capacitive in nature (i.e., yielded negative broadband reflection), while the over compensated multi-connection via here is inductive.

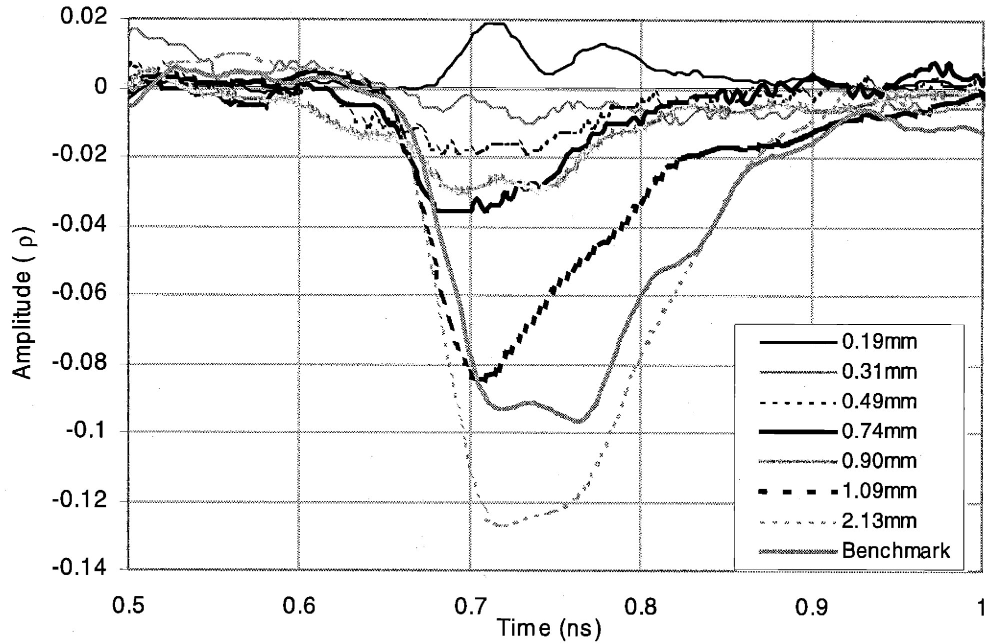

Figure 3-26: Reflection amplitude for various signal conductor arc lengths connecting layers 1 to 4 in 1.5mm-diameter vias.

Table 3-1 presents the peak values and areas under the curves shown in Figure 3-25 to enable a quantitative comparison. The peak value correlates more closely to the high frequency content reflection, while the area under the curve corresponds to the lower frequency band of the data.

Table 3-1: Reflections and energy for layers 1 to 4 in 1.5mm-diameter vias

Signal conductor arc length	Reflection amplitude	Reflection area (s)
0.19mm	2.0%	1.79E-12
0.31mm	1.0%	1.98E-12
0.49mm	2.2%	2.25E-12
0.74mm	3.6%	3.35E-12
0.90mm	3.0%	4.84E-12
1.09mm	8.4%	10.6E-12
2.13mm	12.7%	17.4E-12
Benchmark	9.7%	15.8E-12

Figure 3-27 shows reflections for various signal conductors with arc lengths connecting layers 1 to 2. While the data in this case is not as thorough as that in the prior case, there is clear

performance improvement in going from a 2.1mm to a 0.9mm arc length. It is reasonable to assume that tests of arc lengths close to 0.3mm would bring this structure to a more tuned state. The stub, however, limits the ability achieve a completely reflectionless transition.

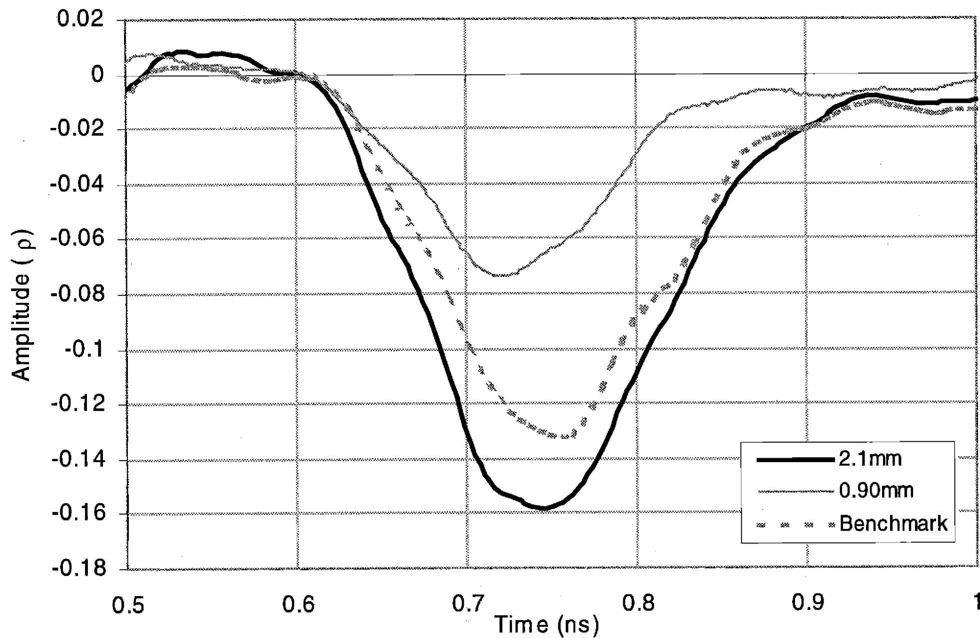

Figure 3-27: Reflections for various signal conductors with arc lengths connecting layers 1 to 2 in 1.5mm diameter vias.

Table 3-2 presents reflections and energy for layers 1 to 2, as shown in Figure 3-26. A comparison of these values with the values in Table 3-1 reveals increased reflection across the board. Comparing the peak reflected amplitude between the two layer cases for the 0.90mm and 2.13mm arc length yields 4.4% and 3.2% increase in reflection respectively, with a 3.6% increase for the benchmark vias. This difference represents the contribution from the stub reflection. While it is difficult to draw firm conclusions from this small amount of data, it appears to confirm the speculation that the better the impedance control of the stub the greater the amount of reflected energy returned to the signal. Where as the poor impedance control of the conventional via actually helps to attenuate the stub reflection.

Table 3-2: Reflections and energy for layers 1 to 2 in 1.5mm diameter vias.

Signal conductor arc length	Reflection amplitude	Reflection area (s)
0.90mm	7.36%	1.06E-11
2.13mm	15.86%	2.68E-11
Benchmark	13.25%	2.25E-11

This is shown further in Figure 3-28 and Table 3-3, where the sensitivity to stub effects is demonstrated by changing the layer combinations, while holding all other variables constant. Since this case was for the 0.90mm arc length via, which is not the best-tuned configuration, a portion of the reflection is due to the impedance mismatch. If all these were, the peak amplitudes would reduce by approximately 3%, resulting in just the stub reflections. In addition, observe how the waveform of the benchmark via is similar to that of the corresponding multi-connection via for both layers 1 to 2 and 1 to 4. When stub lengths are equal, characteristic higher frequency reflected waves ride the main curve with the same form.

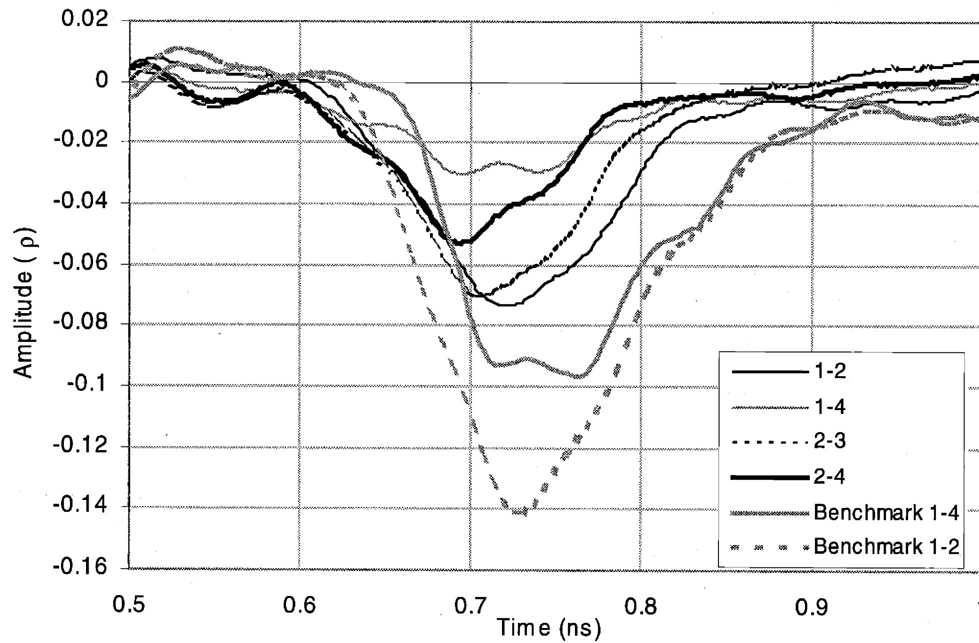

Figure 3-28: Reflections with different layer combinations with arc lengths of 0.90mm in 1.5mm-diameter vias.

Table 3-3: Reflections and energy for different layer combinations in 1.5mm-diameter vias.

Signal conductor arc length	Connected layers	Reflection amplitude	Reflection area (s)
0.90mm	1-4	3.03%	4.84E-12
0.90mm	2-4	5.30%	6.19E-12
0.90mm	2-3	7.00%	7.51E-12
0.90mm	1-2	7.36%	1.06E-11
Benchmark	1-4	9.65%	1.58E-11
Benchmark	1-2	14.12%	2.12E-11

3.2.2 Differential vias

The differential cases that were tested are shown in Figure 3-29, as follows:

A. single pair,
B. single pair with drain,
C. single pair with drain,
D. two pairs,
E. three pairs, and
F. two pairs with drains.

This section focuses on one set of tests for reflection, case (C), where the layer combinations are varied and results are provided in Figure 3-30 and Table 3-4. Like the single-ended results, comparing the same layer combinations to the benchmark shows that the multi-connection differential via has significantly better performance. The resource limitations, of this research, did not provide for optimization of the differential case, but it is reasonable to expect that they are as tunable as the single-ended vias. This implies that if the stub lengths are short, the reflections can be reduced to near zero.

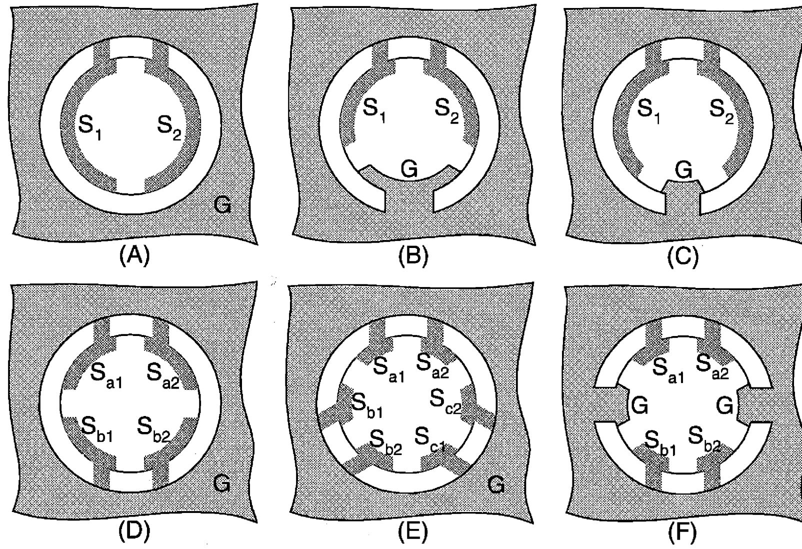

Figure 3-29: Differential via structures tested

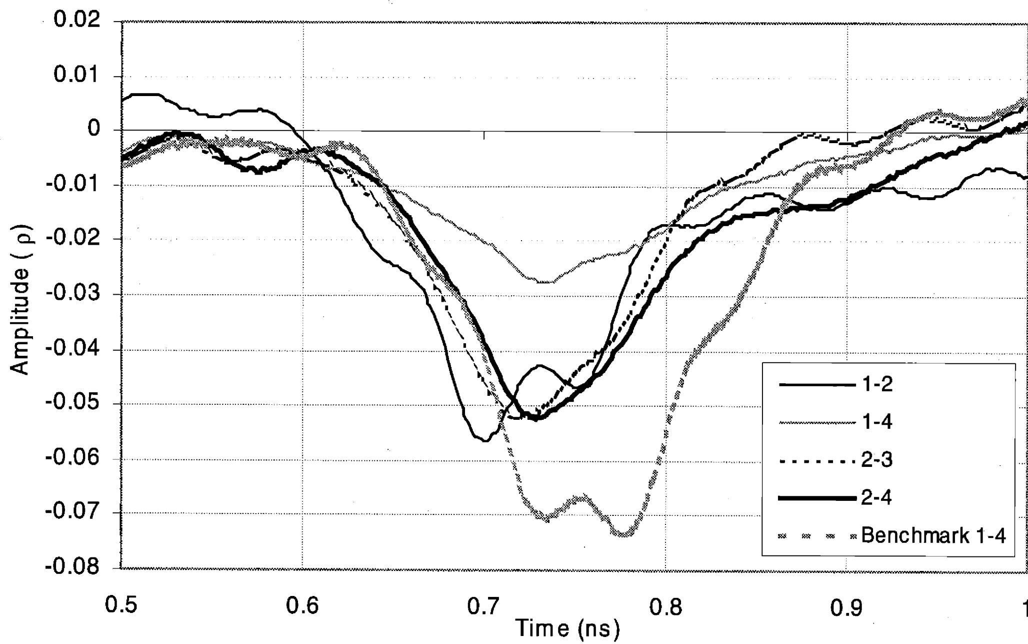

Figure 3-30: Differential structures (two pairs and two grounds) with 0.53mm signal arc lengths.

Table 3-4: Reflections and energy for differential structures.

Signal conductor arc lengths	Connected layers	Reflection amplitude	Reflection area (s)
0.53mm	1-2	5.66%	9.4E-12
0.53mm	2-4	5.24%	7.9E-12
0.53mm	1-4	2.76%	4.35E-12
0.53mm	2-3	5.22%	6.29E-12
Benchmark	1-4	7.34%	10.0E-12

Figure 3-31 plots crosstalk amplitude for several layer combinations. Plots show both case D and E in Figure 3-29, neither of which have ground segments in the via. Measured crosstalk in cases with grounds in the via were below the instrumentation resolution, i.e. less than 0.1 percentage. Therefore, multiple connection pairs should never be run in the same via without isolating ground segments.

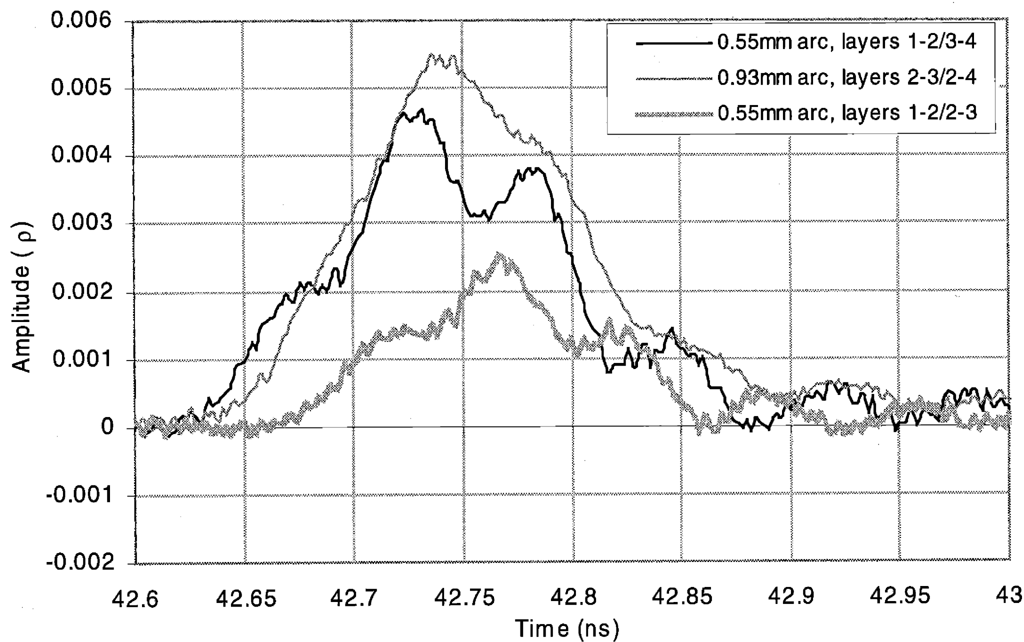

Figure 3-31: Crosstalk in differential structures.

3.3 Summary

This chapter has confirmed the fundamental hypothesis that multi-connection vias, properly tuned, provide impedance control in the transition of signals between layers in the PCB. This

confirmation extends to the launch of external signals into the PCB. Both experimental and simulation results agree that the signal arc length and gap to ground structure determine the impedance match. While the via diameter is independent of the attainable performance. Once the impedance of the via is matched to the trace and connector launch the stub reflection dominates, thus manufacturing processes which eliminate the stub need to be considered.

One final note on dielectric materials. In the drive for higher speed signals, board manufactures are beginning to replace conventional PCB dielectrics with lower loss materials. This prevents signal degradation over long traces, and has the added benefit to multi-connection vias of increasing the transmission. One advantage of the older higher loss dielectric material, however, is the filtering effect on high frequency noise. Thus, lower loss dielectric PCBs are less tolerant to reflections, making an even greater case for impedance matched multi-connection vias.

4 Connection density

If multi-connection vias provide significant increase in signal performance over existing technologies, yet cause the overall circuit size to increase, their applications would be few, limited to cases where performance is the only criteria. The opposite case may also be true, such that a system requires low signal performance (i.e., low frequency) but density criteria is extremely high. The trend for most of electronics, however, is clear – smaller and faster. To make circuits smaller, devices must be placed closer together and be more integrated. This means more signals have to be routed in a smaller space. One way to increase the number of devices in a given space is to decrease their size and add layers. However, with more layers added to a board, more vertical interconnections are required. In tall buildings, the elevator shaft can consume a surprisingly large portion of the building. In the same way, vias, the vertical interconnects of the PCB, can consume a great deal of the routing space.

Do multi-connection vias then improve the situation or make it worse? To answer this question, via density must first be defined. In some cases, such as devices and connectors, vias are arranged in arrays, where the area density may be limited by the via size and spacing. If the routing space is not limited, there is no reason to be concerned with via density. Therefore, to legitimately compare the number of vertical interconnections per unit area (density), a limiting-case situation (i.e., a fully routed array) must be assumed.

The first section of this chapter develops a model for "routability" that determines how the space between vias in an array is used and how all the necessary interconnections are made. This model provides a normalizing factor to use in comparing density of any through-hole type via, regardless of size or number of connections. The intention here is to provide a tool for making high-level comparisons of different via geometry.

4.1 Via routability

When comparing the density of split vias, one must consider the problem of running traces to a multi-connection via. This is different from standard plated through holes that only support one connection. One approach for measuring and comparing density considers routability as the effective trace pitch [Johnson and Graham].

$$P_{effective} = \frac{P_{via}}{N_{tracks}} \quad (4\text{-}1)$$

The number of tracks (N_{tracks}) is the number of traces between vias (see Figure 4-1). This assumes the number of vias limits the board density, or the board is completely covered with vias on a pitch (P_{via}). Therefore, the number of vias and the number of traces between them limit the effective trace pitch. In other words, the more traces between vias and the smaller the via pitch, the greater the routing density. This relationship is one relative measure of routability for standard vias.

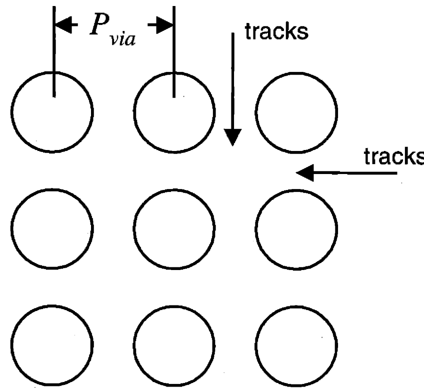

Figure 4-1: Symmetrical array of vias

The effective trace pitch is not a sufficient density model for comparing multi-connection vias, because it does not consider the number of layers and the number of traces that have to connect to a via. Another model, developed here and applied to multi-connection vias, is to consider the density of layer-to-layer interconnections with respect to traces available for routing. Routability (R) can be defined as a function of: the number of traces that fit in the tracks in each direction (T_x and T_y), the number of LLIs per via (N_c), the number of signal layers in the PCB (L), and the array of vias requiring routing (A_x by A_y), see Figure 4-2. To clarify, the space between vias, where traces are run, is called the routing channel; and the number of traces in the channel is the number of tracks. Using these parameters, a more effective measure of R can be derived, which is a relative measure of the feasibility of routing an array of vias on a PCB. First, the following assumptions are made:

1. Traces are run in only one direction per layer (either x or y).
2. Traces connect to the array from all directions. In other words, traces run from the outside-in and from both sides (in the direction defined by assumption 1).
3. Every other LLI is a ground connection to ensure the design is electrically balanced.

4. The array is uniformly spaced and rectangular in shape.
5. Each via in the array has the same number of LLIs (i.e., N_c is constant).

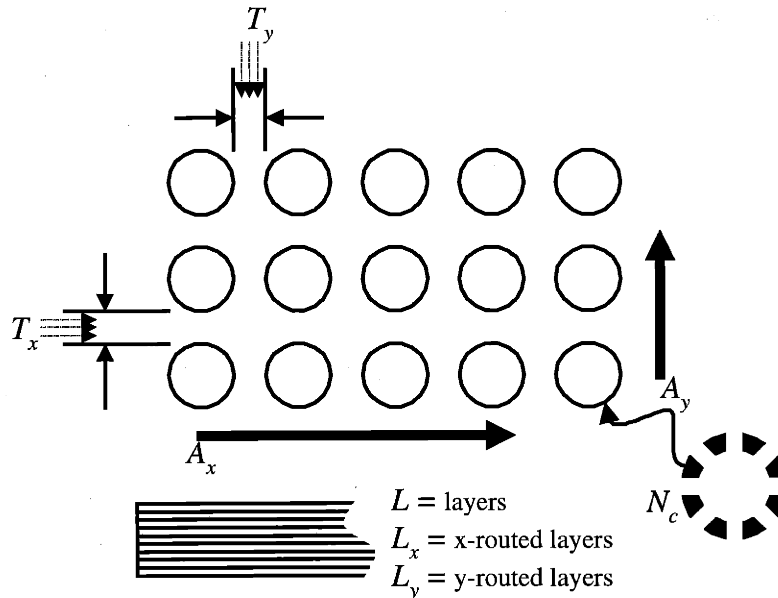

Figure 4-2: Via array and variables for routing

The total number of vias that have to be routed is then $A_x A_y$. Now considering assumption three, the number of signal connections per via that have to be routed is:

$$\frac{Signals}{via} = \frac{N_c}{2} \tag{4-2}$$

This implies that if there are 50 interconnections in the array, 25 will be ground and 25 will be signal. The total number of real signal LLIs that are created by the array is then:

$$\frac{A_x A_y N_c}{2} \tag{4-3}$$

The number of traces that can be run between vias (tracks) in x and y directions defines the number of connections that can be made in that direction per layer. In accordance with assumption two, there are $2T_x$ and $2T_y$ connections that can be made in each routing channel per layer, one connection from each side. The total number of traces available for routing equals:

$$2T_x A_y L_x + 2T_y A_x L_y \tag{4-4}$$

where: L_x = number of signal layers routed in the x-direction
L_y = number of signal layers routed in the y-direction

A fully routable array would then have the same number of signal LLIs as number of available traces. This is possible because assumptions four and five don't allow for cases of irregular arrays. While this simplification ignores the potential benefits or problems that will occur in individual design cases, it eliminates unnecessary complexity from the model. Routability can now be defined as the ratio of the available routing space (4-4) to required routing space (4-3).

$$R = \frac{4(T_x A_y L_x + T_y A_x L_y)}{A_x A_y N_c} \tag{4-5}$$

A routability index equal to one represents a fully-routed array, where every available LLI has one trace that can reach it and no extra space for other traces. If R is less than one, the array is not fully routable, and if R is greater than one, there will be extra free traces in the channels. A further simplification would be to assume the number of signal layers is even, with half of the layers routed in the x-direction and half in the y-direction:

$$R = \frac{2L(T_x A_y + T_y A_x)}{A_x A_y N_c} \tag{4-6}$$

Consider an array of vias that is 10 by 10 on a four-signal layer PCB. In Figure 4-3, routability is plotted versus the number of LLIs per via with different track spacing. As expected, routability decreases as the number of LLIs per via increases, and routability increases as the number of tracks between vias increases.

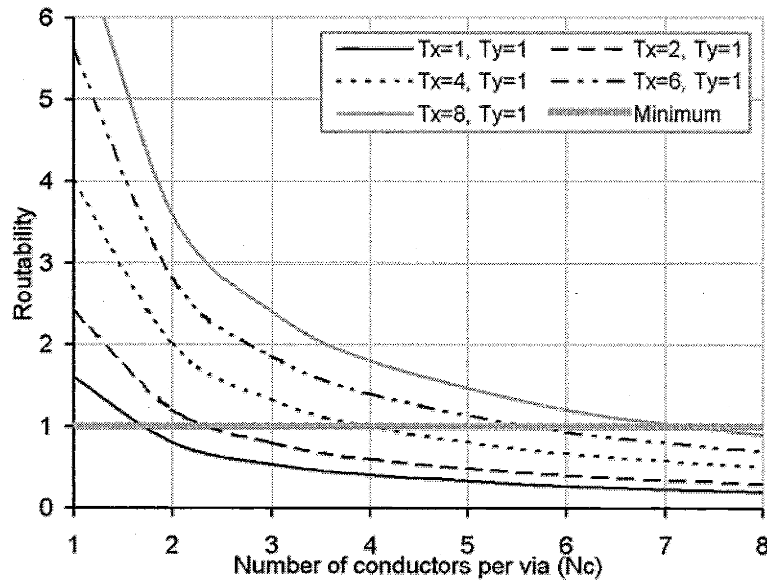

Figure 4-3: Routability index for 10 by 10 via array on a four-signal layer board for various track configurations.

The routability index is intended to provide a relative comparison of via types and track spacing. It gives the designer rules of thumb for a specific PCB design considering the number of layers, via type, and via spacing. The index can be applied to density comparisons, as described in the next section. Of particular interest is the application to connectors.

This routability model is not intended as a complete design tool. The assumptions used to derive the model cannot accommodate optimizations possible in PCB designs, including:

- removal of unused signal pads,
- non-uniform arrays,
- non-uniform via spacing,
- blind and buried vias,
- differential signals,
- via clustering (see Section 4.2.1), and
- radial coordinate arrays.

4.2 Via density

One potential benefit of multi-connection vias is the increase in LLI interconnection density. Comparing density requires considering all factors involved in sizing a via, including finished-hole size, plating thickness, drill errors, spaces between vias, trace sizes, trace spacing, and keep outs. These parameters are illustrated in Figure 4-4.

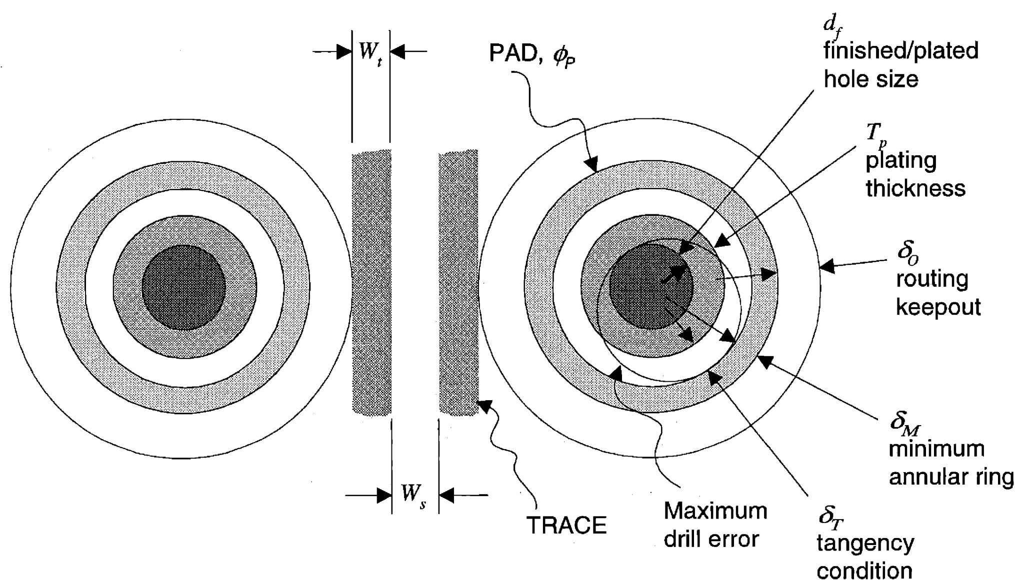

Figure 4-4: Via size, pad size, trace size and trace spacing.

The via pad provides the connection between layer traces and via barrels. Surface pads can also function as solder points for through-hole devices. The diameter of the pad must be sufficient to allow for manufacturing flaws such as true position, fixturing, thermal, layer stack up, and drill wander errors, such that the drill does not break out of the pad. Pad size is represented as follows:

$$\phi_P = d_f + 2(T_p + \delta_T) + 2\delta_M \tag{4-7}$$

Tangency condition, δ_T, is the maximum error that the drilled hole can have from the specification. This error is presented as the sum of the hole diameter tolerance and the hole alignment allowance, [Johnson and Graham]. Experimental data provides both error terms (δ_T and T_p) for small drilled vias, resulting in an expected error for inner layer pads of 131μm and 105μm for outer layer pads, [Braunstein].

Drill error and runout are presented here as constant values for small drilled vias. Because multi-connection vias require much larger holes, these errors will decrease significantly. The error is related to the aspect ratio relationship between hole diameter (d_{drill}) and board thickness (t_{PCB}). Assuming that the deflection of the drill will be that of a fixed/free beam, this error has the following form:

$$DrillError = K\frac{t_{PCB}^3}{d_{drill}^4} \tag{4-8}$$

The constant, K, is a function of the drill bit material, geometry, and drill side forces possible. Development of the drill error factor requires a volume of experimental work not inline with the goals of this research. Therefore, fix drill error values from Braunstein are used. This approach is conservative because the data comes from smaller drills.

It is now possible to define signal connection density in terms of the geometry in each direction:

$$\rho_{VIA_x} = \frac{1}{2(\phi_P + \delta_O) + W_t T_x + W_s(T_x - 1)} \tag{4-9}$$

$$\rho_{VIA_y} = \frac{1}{2(\phi_P + \delta_O) + W_t T_y + W_s(T_y - 1)} \tag{4-10}$$

The number of LLIs per via is N_c, giving total connection density as:

$$\rho_c = N_c \rho_{VIA_x} \rho_{VIA_y} \tag{4-11}$$

Plotting the total connection density versus the number of connections per via (Figure 4-5) yields density which decreases with a larger number of tracks. However, the crossover point from the standard via to the multi-connection via occurs at a lower number of connections per via when the number of tracks is increased. Therefore, in cases where higher via spacing is required, multi-connection vias become more advantageous.

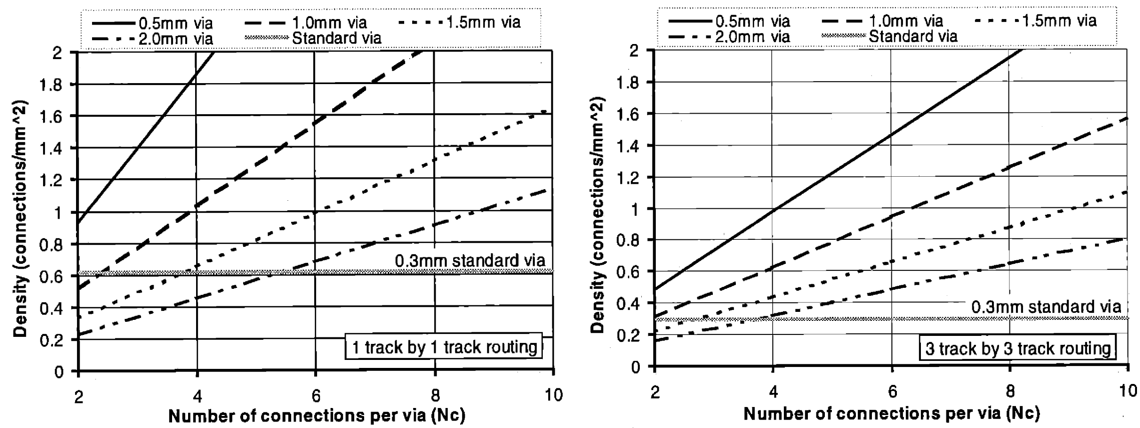

Figure 4-5: Connection density versus the number of splits per via for 1- and 3-track PCB.

With density defined, it is possible to add routability considerations (from Section 4.1) to the model. This allows for the maintenance of a prescribed level of routability for each via geometry compared, and maximizes density for the defined array arrangement and size. To integrate with density model it is first necessary to assume some proportional relationship between the number of tracks in each direction:

$$K_t = \frac{T_y}{T_x} \tag{4-12}$$

Solving equation (4-5) for the number of tracks in x gives:

$$T_x = \frac{A_x A_y N_c R}{4K_t(A_y L_x + A_x L_y)} \tag{4-13}$$

Putting this into equation (4-11) requires layer and array size information to compare density from a routability standpoint. For a valid comparison, the same connection-array size is required, not the same via array size. For example, a 10-by-10 array of single-connection vias maps into an array of 5-by-5 four-connection vias, both yielding 100 LLIs. The relationship between the via array and the connection array is:

$$A_x^{'} = A_x\sqrt{N_c} \text{ and } A_y^{'} = A_y\sqrt{N_c} \quad (4\text{-}14)$$

By holding $A_x^{'}$ and $A_y^{'}$ constant, it is now possible to compare single- and multi-connection vias. Figure 4-6 shows lines of constant routability for a 10-by-10 connection array and 4 signal layer PCB. Unlike Figure 4-5, where routability is not considered, the density gains begin to drop off as the number of connections per via increases. This drop off occurs because a higher number of connections to a via requires more space for routing that via.

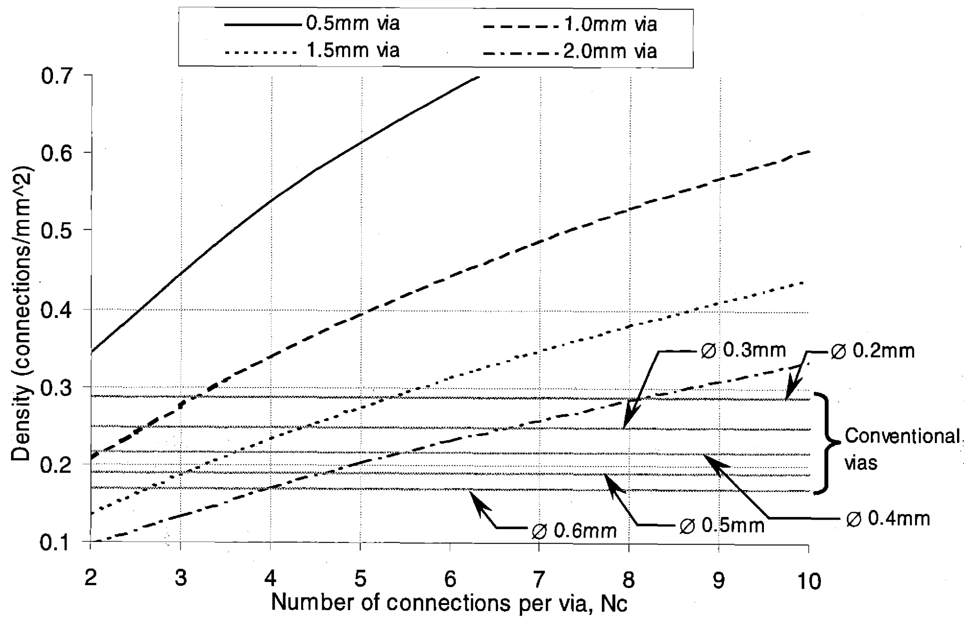

Figure 4-6: Effective connection density for 10-by-10 connection array and 4 signal layer PCB.

One final consideration is required to make this analysis complete. The data shown in Figure 4-6 gives the number of traces routed in a channel between vias at a given R. This is not, however, a continuous function and must have integer values of traces within channels. Applying this integer constraint to the T_x and T_y, for the same case above, illustrates the non-linear transitions between trace numbers, Figure 4-7. These curves no longer represent lines of constant routability (R=1 for this case), but lines of minimum routability (R≥1 for this case).

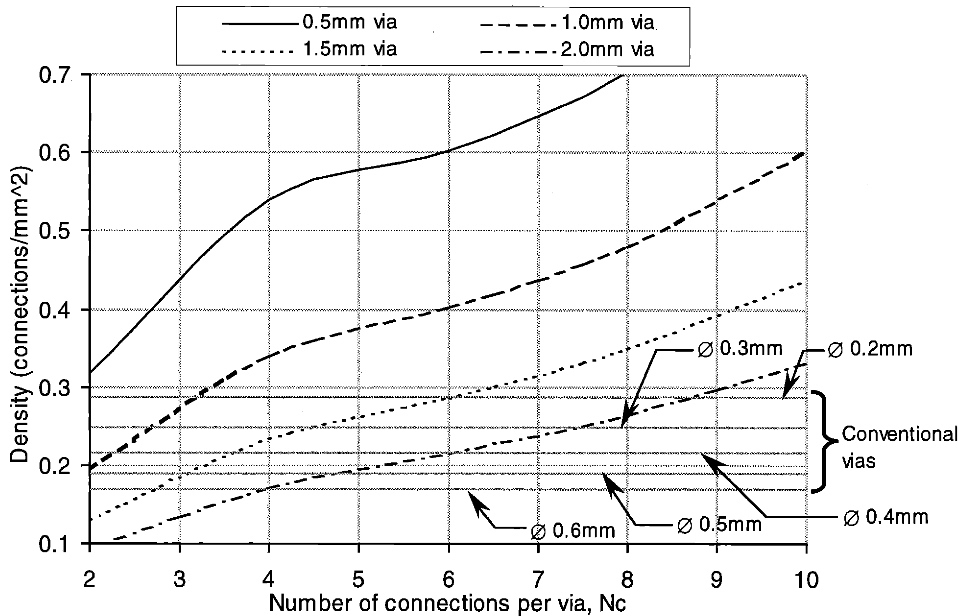

Figure 4-7: Effective connection density with integer trace values in routing channels; for 10-by-10 connection array and 4 signal layer PCB.

Concluding, from this analysis, multi-connection vias offer density benefits over conventional drilled vias when manufactured at a small enough scale. This scale is on the order of 1.5 to 3 times the size of conventional drilled vias. The manufacturing and scale of multi-connection vias is discussed in Chapter 4. It is important to note that this analysis neglects possible design optimizations that could take advantage of the special geometry of multi-connection vias. The next section presents some concepts in this area.

4.2.1 Clusters

The density comparisons in the section above all assume vias are on an evenly-spaced grid as shown in Figure 4-2. While this may be a good first-order comparison, even greater benefit may be gained by considering the unique geometry of multi-connection vias and exploring electric field issues.

Figure 4-8 shows a two-connection via clustered in pairs. Routing channels pass on either side of the clusters. Ground vias are placed next to each other with zero trace spacing between them. Because there is no need for the keep-out zone between the ground sides of the vias (δ_O from Figure 4-4), connection density increases.

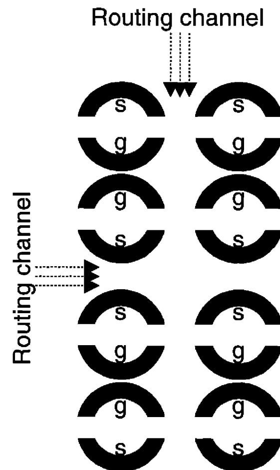

Figure 4-8: Two-connection cluster

One electrical form that particularly benefits from multi-connection vias is the differential pair. In its simplest form, two connections transmit signals in opposed phase. Because a perfectly balanced differential pair is not possible, it is desirable to have a ground drain close to the pair. Figure 4-9 illustrates clusters of three three-connection vias, each representing a differential pair and ground drain. As in the previous example, the ground sides of the vias are placed next to each other in a zero trace condition and no keep-out zone is necessary.

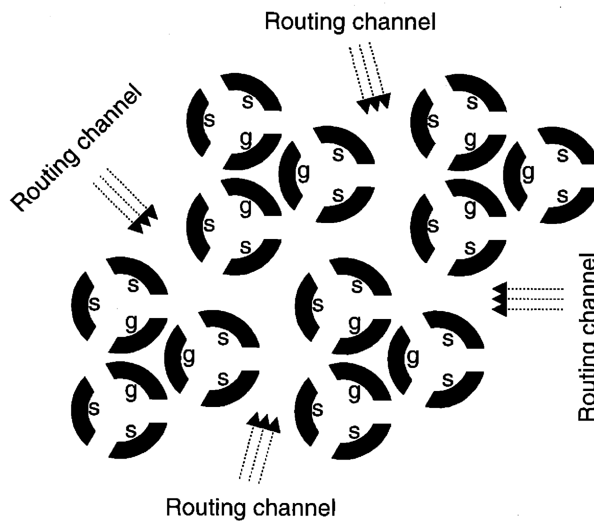

Figure 4-9: Three-connection cluster

The third example, shown in Figure 4-10, is a simple grid arrangement of four-connection vias. Placing grounds next to each other in a repeating pattern provides higher densities than the assumptions in the density model developed in the prior section allow.

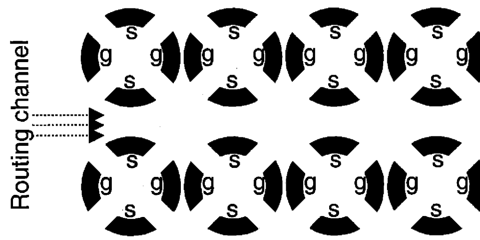

Figure 4-10: Four-connection cluster

As demonstrated by these three examples, the possibilities for multi-connection via arrangements are numerous. A final consideration in routing multi-connection vias is clearance around the via structure. As shown in Figure 4-11, the gap between the signal side and the trace is much larger than that of the ground side, primarily due to the ground plane clearance. This clearance requires traces on the layers above and below the ground plane to not be routed in the clearance areas, thereby avoiding potential impedance mismatch in the trace and minimizing crosstalk from the signal via. On the via ground side, the ground plane is uninterrupted, because there is little or no field on this side. Therefore, clearance on the ground side is set to just outside the minimum annular ring requirement.

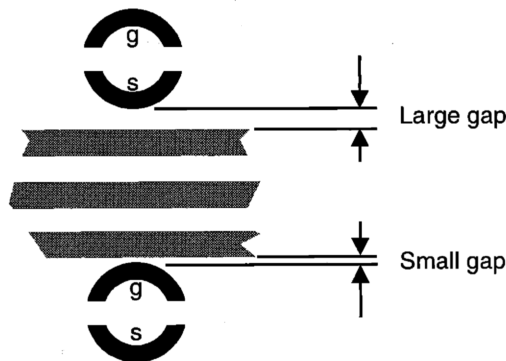

Figure 4-11: Routing clearances relative to signal and ground sides of vias.

4.2.2 Micro vias

It is difficult to compare micro-via density to standard or multi-connection vias, primarily because micro-vias are essentially very short blind vias. They represent a new paradigm to PCB design that breaks via function into two categories, large and small number of interconnected layers. Micro-vias provide the minor roadways for connecting local traffic, while conventional

through-hole vias represent the major throughways. The two technologies are complimentary, therefore it is not appropriate to directly compare them from a density standpoint.

4.3 Maximum number of connections

The final thing to consider in the scaling of multi-connection vias is the physical limitation to the number of splits. The electrical impedance required will determine the relationship between the radial copper length, l_{cu}, and the width of cut, t_w, see Figure 4-12. Future work requires the development of formula similar to those used in stripline and microstrip impedance calculations. For the purposes of this preliminary comparison, it is assumed that the two lengths are equal. Values of the following formula are plotted in Figure 4-13 for a 130μm, 250μm and 500μm wide gaps.

$$N_c = \tfrac{1}{2}\pi \frac{1}{\sin^{-1}\left(\dfrac{t_w}{d_{tool}}\right)} \tag{4-15}$$

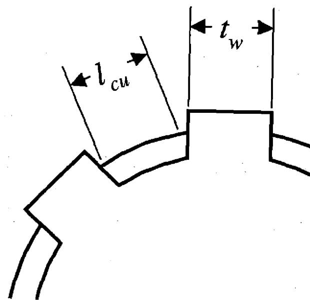

Figure 4-12: Copper and cut radial lengths.

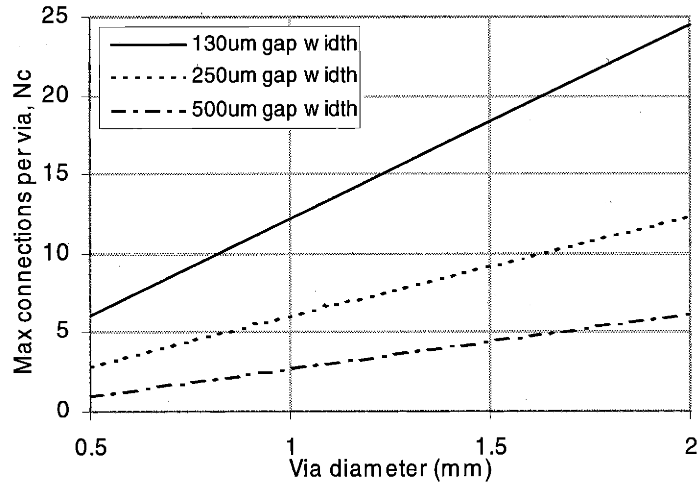

Figure 4-13: Maximum number of splits possible per via size.

Applying this model to the density comparison completed in Figure 4-7 bounds the results. Figure 4-14 applies the density limitations due to gap width (t_w) to the same case. Because the gap width is limited by the manufacturing process capability, these limits represent manufacturability limits. Therefore, below the manufacturability lines and above the conventional via lines represents the region of produceable higher density using multi-connection vias. Manufacturing limits, including aspect ratio, also determines the minimum diameter produceable for the particular case. Therefore the via diameters bound the left side of the region.

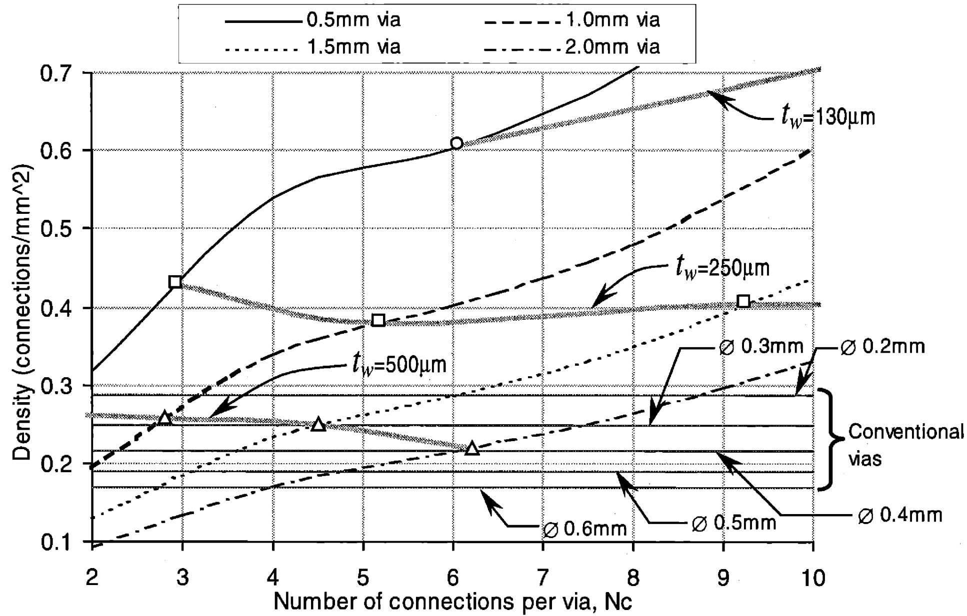

Figure 4-14: Density for different via sizes, with manufacturing limits, based on Figure 4-7.

4.4 Connector density

For the most part, board-to-board interconnect density can be compared using the same analysis applied to layer interconnects. Array design is an even greater factor with connectors than with vias, because connectors form natural arrays. Thus, the analysis developed above is particularly applicable to connectors.

4.5 Summary

This chapter explores the impact of changing via geometry on the density LLIs in the PCB. Development of the "routability" concept provides a theoretical model for routing feasibility. The density model presented measures the LLIs per unit area. Applying the routability model to the density model allows for density comparisons of different via geometry. Because routability is very sensitive to array size and the number of routing layers, every design case is different. Thus, density increases over conventional drilled and plated vias are possible only when proper design criteria are met; otherwise density is the same or lower. In general, multi-connection vias require more routing channel spacing or more layers to support a higher number of connections per via.

5 Manufacturing of multi-connection vias

For this thesis, two manufacturing processes were used to produce multi-connection vias, broaching and wire electrical discharge machining (EDM). Some other processes may prove better in the long run and are investigated in Section 9.3. Broaching and wire EDM were explored to a level that satisfied the needs of the performance experimentation and provided proof of concept. Broached vias provided all the electrical test data necessary to validate signal performance expectations. Experiments in EDM provided only a proof of concept and utilized conventional wire EDM process.

This chapter focuses primarily on the theoretical and experimental developments of broaching multi-connection vias. The cutting physics and tool design are considered in some depth. In addition, some simple experimentation of multi-connection vias produced using standard wire EDM equipment is presented.

5.1 Broaching

Broaching is a very old cutting process that depends on a progressive tool, which makes successively deeper cuts in a work piece, as shown in Figure 5-1. In fact, broaching is often employed instead of reaming for long accurate holes, [Oberg et al.]. At the same time, the material removal rates can be extremely high, due to the number of cutting edges that can be in contact with the work piece at one time. The cutter profile is dependent on the shape of the tool, which can allow cuts not easily produced using any other method. For this reason, broaching is well suited to the irregular shape of the multi-connection via, which was recognized when multi-connection vias were originally proposed in 1968, [Reinhart].

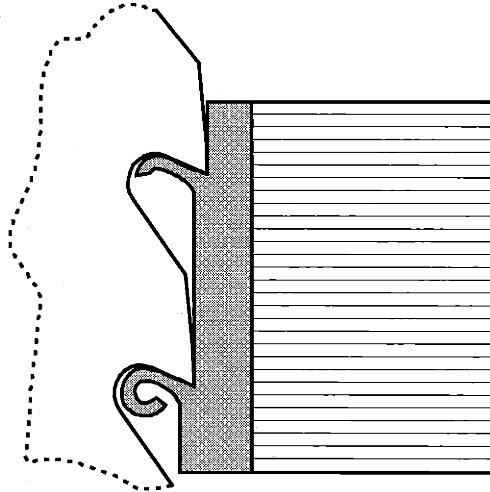

Figure 5-1: Broaching.

The basic cutting action of the broach is similar to that of a band-saw where the material is carried through the work piece by the tooth profile. Unlike the saw, the stagger of the teeth determines the cut depth. The tool is usually guided on the entry side and sometimes on the exit side, and is either pushed or pulled through the work piece. While broaching can be applied to cutting material from the edge like sawing, a very common application is changing hole shapes. A good example is that of broaching a square hole from a round starter hole.

Creating multi-connection vias by broaching presents a unique set of challenges, due to the material and scale. Broaching applications that scale down to the diameter of a drilled and plated via are not common. Consequently, no commercial tooling is available for this operation. The second interesting problem is the unique composite material make up of the PCB plated through-hole. The tool must first cut soft, ductile copper then brittle, fibrous, glass/epoxy composite, as Figure 5-2 illustrates. No published data was found on broaching such a composite combination at any scale.

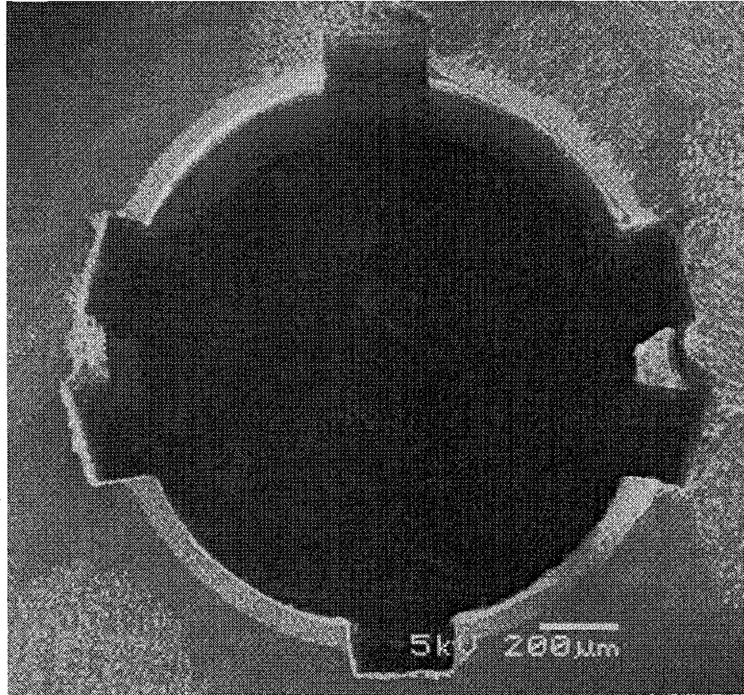

Figure 5-2: Sectioned SEM (Scanning Electron Microscope) of broached via.

Developing the broaching process for this application is similar to the development of conventional material broaching, [Kalpajian]. Both require consideration of all the relevant parameters, which can be broken into independent variables:

- tool material, coating and condition,
- tool geometry, surface finish and sharpness,
- work piece materials and condition,
- cut speed and depth,
- cutting fluid use,
- machine tool stiffness, damping, etc., and
- PCB thickness.

And dependant variables:

- types of chips produced,
- chip storage,
- energy dissipated,
- maximum cutting force,
- thermal issues in the chip and the tool,
- tool wear and failure, and
- surface finish and fiber disruption.

This section explores some of these parameters and provides models for scaling. First, the forces generated in cutting are considered, including rate-dependant effects. A discussion on chip storage follows, which offers important information on via diameters and produceable aspect ratios. The section concludes with a discussion of prototypes developed for this thesis.

5.1.1 Cutting forces

The first step to understanding broach mechanics is discerning force balance. Figure 5-3 shows the "shear-angle solution" originally presented for metal cutting in the 1940's, [Ernst and Merchant]. The basic assertion is that the shear angle will adjust to minimize the cutting force. In other words, the shear angle represents a plane into the page, which matches the maximum shear stress plane. The shear stress is given by:

$$\tau_s = \frac{F_s \sin(\phi)}{w \cdot t_0} = \frac{F_s}{A_s} \tag{5-1}$$

w is the width of the cut and A_s is the shear area. The shear angle (ϕ) is given as a function of the rake (α) and the mean friction angle (β, note: $\beta = \tan^{-1}(\mu)$, where μ is the friction factor). Using the geometric relationships to solve for the cutting force and differentiating with respect to ϕ, yields the minimum cutting force configuration as:

$$2\phi + \beta - \alpha = \frac{\pi}{2} \tag{5-2}$$

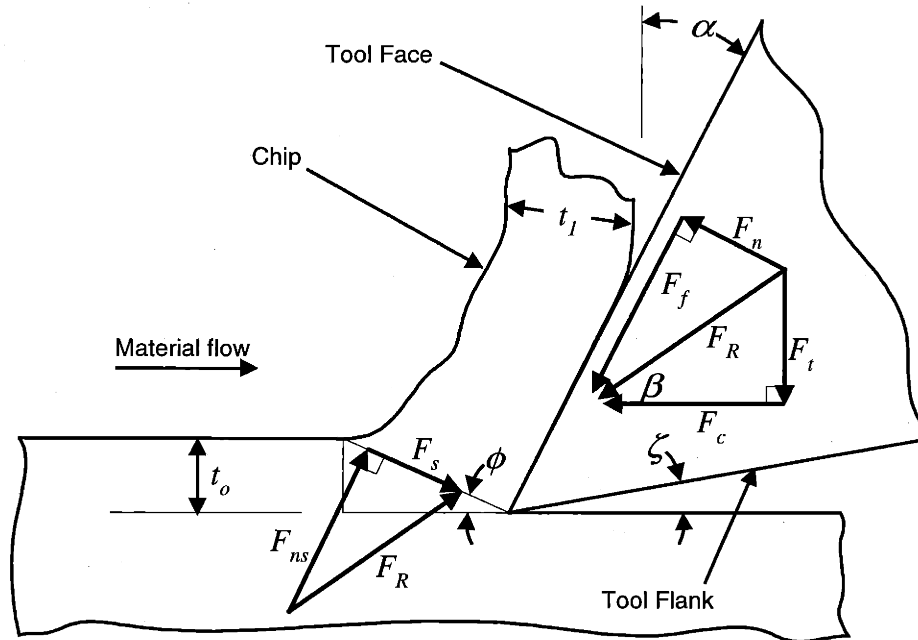

Figure 5-3: Forces in the shear plane

Later work ([Lee and Shaffer]) attempted to apply plasticity theory to orthogonal metal cutting, yielding the following:

$$\phi + \beta - \alpha = \frac{\pi}{4} \tag{5-3}$$

These two theories assume that the cutting edge is perfectly sharp and that the friction model is simply dynamic friction. A more complete model of the cutting tip and friction are illustrated in Figure 5-4, [Boothroyd]. The plowing affect is due to the round tip of the cutting edge, yielding a larger deformation zone than the straight shear plane in Figure 5-3. The static and dynamic zones on the tooth face correspond to a constant shear and constant coefficient of dynamic friction respectively.

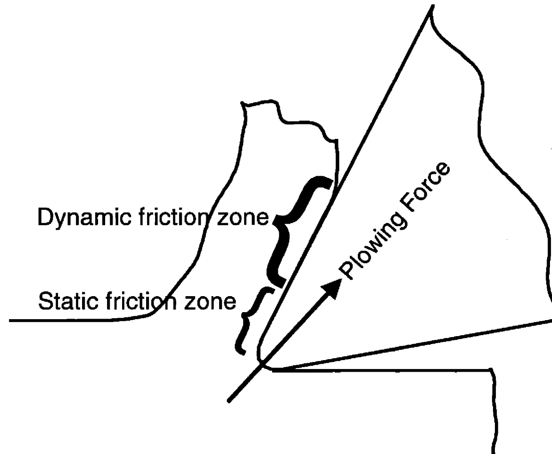

Figure 5-4: Plowing force.

For the purpose of this work, empirical data from Boothroyd is used for the copper cutting force calculation. As for fiberglass-reinforced core (FR4) cutting, no data was found to address shear angle versus mean friction angle. However, there have been discussions documented and experimental work performed on composite drilling, ([Chandrasekharan et al.] and [Di llio et al.]). Fiber orientation further complicates matters. While the broach will always see those fibers perpendicular to the cutting direction, the in-plane orientation varies. For now, the slope between $(\beta - \alpha)$ and ϕ is assumed to follow the Ernst and Merchant assumption:

$$\phi + \beta - \alpha = \frac{\pi}{4}$$

It then follows (from Figure 5-3) that the cutting force on the tooth is:

$$F_c = \frac{\tau_s w t_0 \cos(\beta - \alpha)}{\sin(\phi)\cos(\beta + \phi - \alpha)} \tag{5-4}$$

5.1.2 Chip side loads

The broach cuts on the side of the tooth as well as the primary cutting edge. Therefore, the cutting model must include this effect as well. Figure 5-5 shows the side shear region of a chip being removed by broaching. It is assumed that the side shear area is the triangular section bounded by the tooth rake (α), the primary shear plane (ϕ), and the material plane from the previous cut. This assumption yields the following relationship:

$$F_{side} = \tau_s t_0^2 \left(\frac{1}{\sin(\alpha)} + \frac{1}{\cos(\phi)} \right) \tag{5-5}$$

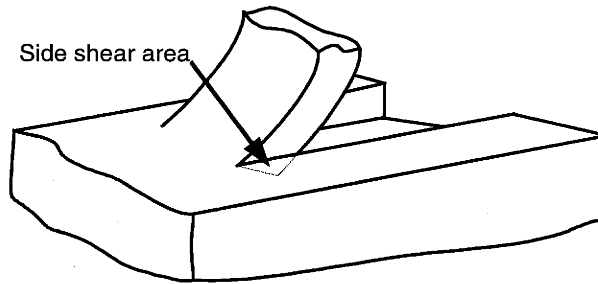

Figure 5-5: Side shear area

The final force to consider is the broach dragging force through the slot. These are essentially side flank loads at the work-piece/tool interface. Because the side of the tooth is also cutting material, it is desirable to incorporate relieved side flanks into the tool, as shown in Figure 5-6. However, the tools used in this work are small and fragile, such that drafted side flanks are not feasible as they are in larger commercial tools. Eventually, it may be possible to manufacture very small broaches that use this design to reduce total cutting force.

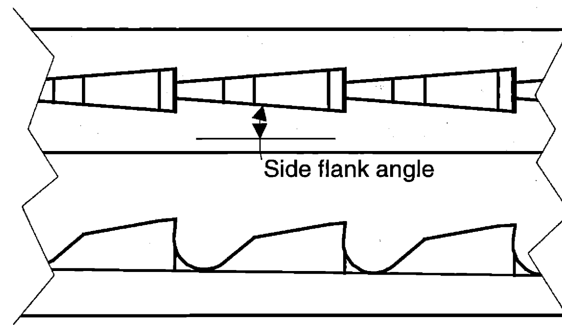

Figure 5-6: Broach teeth with side flanks.

If the tool is totally captured by the slot and the chip is not flowing along the side flank, the models presented in the previous section would not be valid. Because the side flanks are straight, it stands to reason that the side load friction is purely a function of the tooth area engaged and some shear stress at the interface. The side area of the tooth engaged in the slot is a function of the tooth profile, the cut depth, and the broach position during the operation. Approximating the side shear stress is, however, a bit more difficult.

Consider the two extreme cases of material properties, extremely brittle and extremely ductile. With extremely brittle material, very small side loads would be expected, and the shear zone will be very narrow or have little or no plastic deformation. Conversely, with very ductile materials, the shear stress is expected to approach the shear strength. Assuming the side shear

equals the shear strength (i.e., the ductile case for these materials) results in the following relationships:

$$F_{drag} = 2 \cdot A_t \tau_{co}\text{, when } t_{co} \geq d_{cut}$$
$$F_{drag} = 2 \cdot A_t \left[\frac{t_{co}}{d_{cut}} \tau_{co} + \frac{d_{cut} - t_{co}}{d_{cut}} \tau_{Fr4} \right]\text{, when } t_{co} < d_{cut} \tag{5-6}$$

The area (A_t) is the side area of the tooth in the slot. When the tooth is just cutting copper, only the copper shear stress is used. Once the tooth enters the fiberglass, the ratio of the tooth in copper versus fiberglass (Fr4) is calculated with the thickness of the copper plating (t_{co}) and the depth of cut (d_{cut}). This relationship is used to evaluate the equivalent shear stress.

Lastly, the quality of the cutting edge needs to be quantified. As discussed above, tool sharpness can increase or decrease the plowing force. In addition, Boothroyd pointed out that flank friction is the most significant factor, [Boothroyd]. Flank smoothness can be addressed by adjusting the friction factor based on experimentation. For this research, using published friction factors and adjusting for tool/cutting edge quality separately provides a sufficient model. These conditions combined with equations (5-4), (5-5), and (5-6) give:

$$F_{cut} = \frac{F_c + F_{side} + F_{drag}}{K_q} \tag{5-7}$$

While this model is not a perfect representation of the cutting physics, specifically ignoring rate-dependant effects, it does provide a sound first-order representation to use in designing broaches for this thesis. To utilize the cutting model, the formulas were programmed into an algorithm to simulate the entire cutting action. In the following section, one design case is presented against experimentation data.

5.1.3 Experimentation

To apply the model, a test broach was constructed and test samples of FR4, 110 copper and plated PCB vias were prepared. The test samples were all 3mm thick and the test vias were all 1.5mm in diameter. A test fixture was fabricated to hold the 1mm pitch carbide broach, and the samples were tested in an Instron (see Figure 5-7). The simulation used the same tooth geometry as the tool tested.

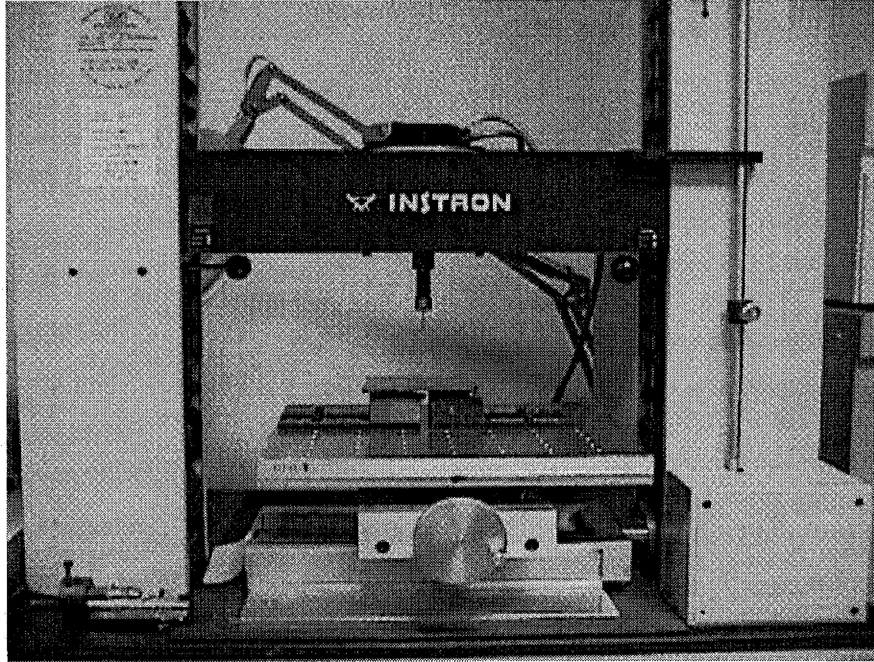

Figure 5-7: Instron setup.

Figure 5-8 shows a plot of cutting solid copper plate, including model simulation results for three different tool quality factors. The increasing slope of the simulation model is due to the model's drag force, which increases as the broach drives deeper into the cut. The later portion of the data appears to correlates best to the simulation at a quality factor a little higher than 25%.

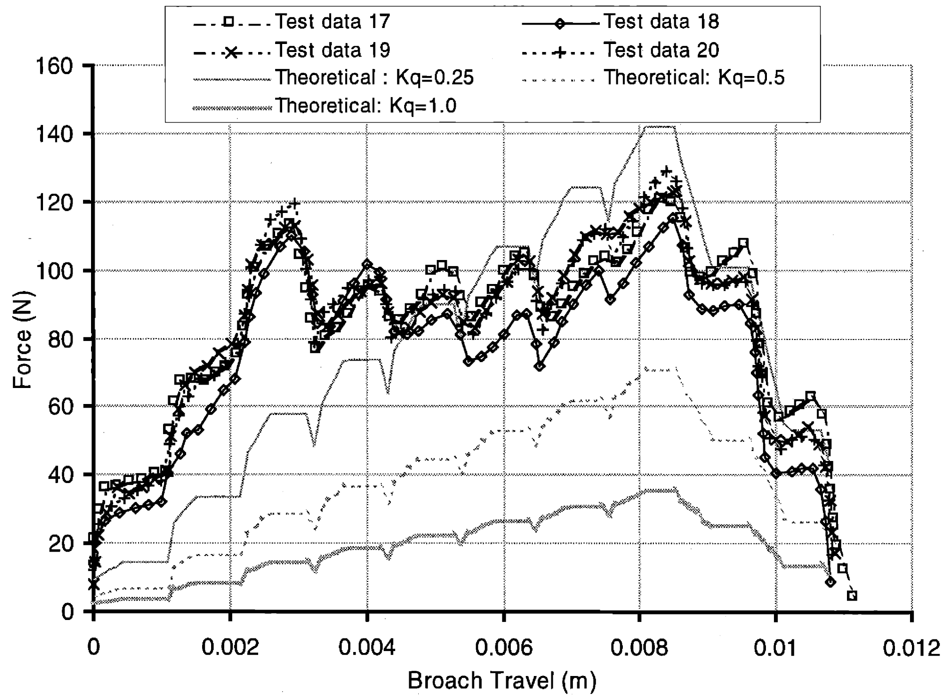

Figure 5-8: Broaching just copper (110).

The second experimental case cuts pure FR4. As shown in Figure 5-8, the FR4 case appears to have a high initial load like the copper case. Because the same tool was used for all experiments, it is possible that the first tooth of the progression had a lower quality cutting edge or that the tool tolerances made the first cut deeper than the actual progression. This would explain why after that tooth exits, the force drops significantly. The FR4 case also seems to correlate best to a quality factor greater than 25%. The slope of the simulation appears to be greater than that of the experimental data, indicating that the drag model assumptions are too great. The data for the glass/resin composite cutting is much more erratic than that of the copper; this is easily explained by the intermittent nature of the glass fibers.

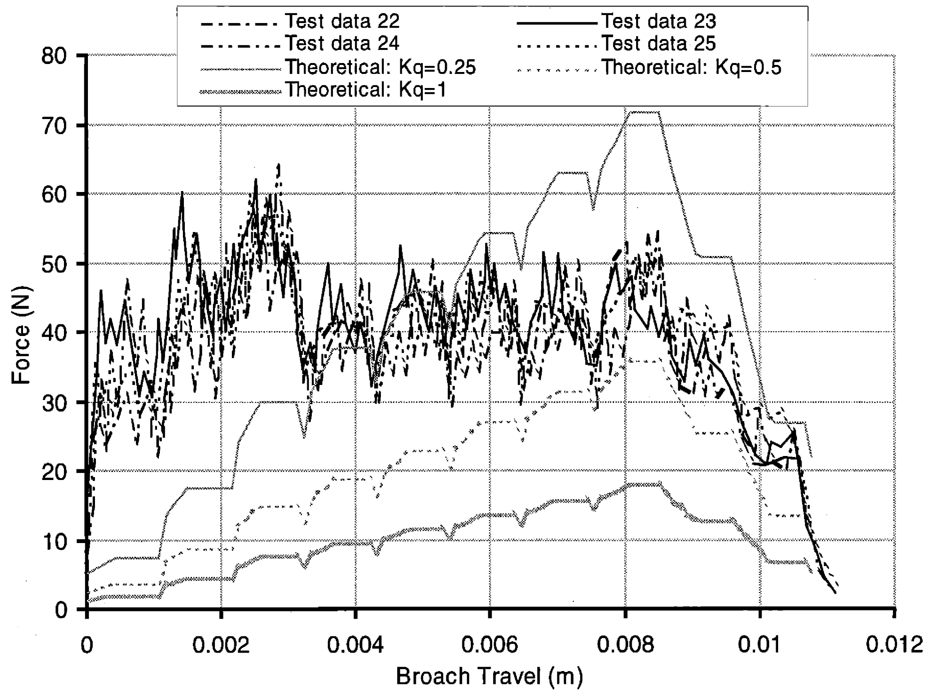

Figure 5-9: Broaching just fiberglass (Fr4).

Real PCB vias transition from plated barrel to fiberglass, which is the final experiment. In this case, two plated vias are tested against the model, and the test results are plotted in Figure 5-9. The simulation accounts for the plated barrel/fiberglass transition by transitioning the material properties at the prescribed plating depth. As with the prior cases, the first tooth of the tool has a much higher load. Thus, the maximum cutting force that the tool sees is caused by the first tooth (third peak), where as the simulation has a maximum force at the exit of the third to last tooth.

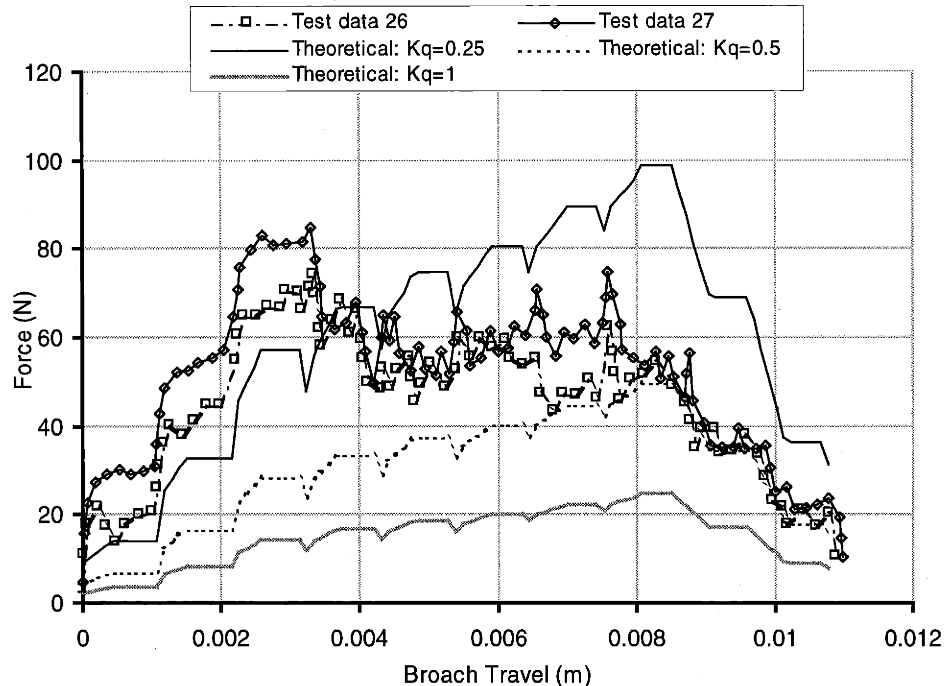

Figure 5-10: Broaching copper plated hole through FR4 PCB.

There are some important observations to draw from this data. If the tooth pitch is not matched well to the thickness of the PCB, the forces will spike at the transition between teeth, which may affect the life of the tool. On the other hand, cutting the copper/dielectric composite damps out the force spikes seen when cutting the pure fiber/resin composite. The more teeth engaged at a time, the higher the force; therefore, if this tool were used in a 4mm-thick board, the peak force would increase by one more tooth or to approximately 90 to 100N.

5.1.4 Cutting speed

In general, metal cutting speed does not apply to the cutting force theories covered in the previous sections. Cutting rate is, however, very important from a thermal standpoint. Obviously, applying the same amount of energy in a shorter period will generate higher temperature. This can affect tool life, surface finish and, under extreme conditions, cutting force. It is reasonable to speculate that there may be more rate dependence in the cutting force for glass/epoxy composite than for copper. In order to investigate this, several measurements were taken at different cutting rates and plotted in Figure 5-11. It can be seen that within the test equipment range of operations, there is no discernable rate dependence to cutting.

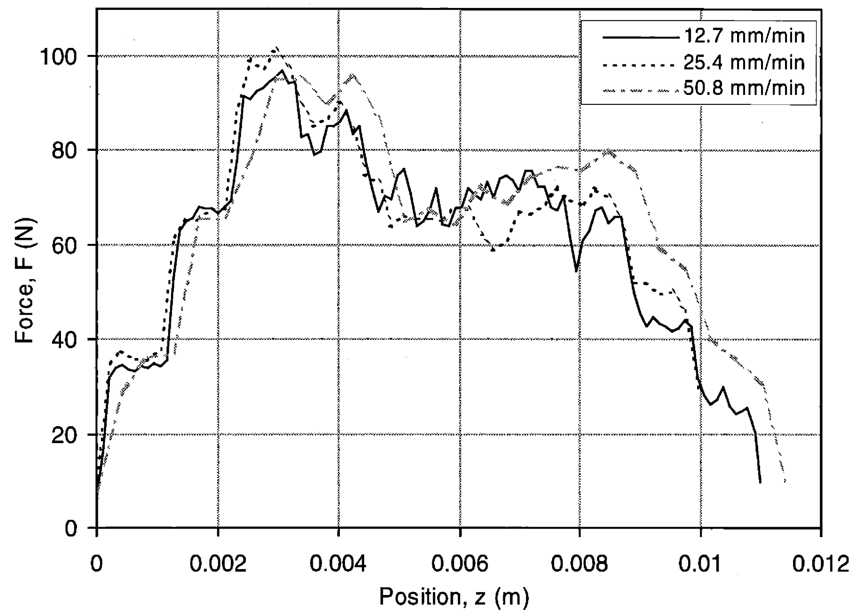

Figure 5-11: Position versus force for different cutting rates.

For process development, it is desirable to understand the rate limitations of broaching vias. The cost, and consequently commercial viability, of the process ties to these limitations. If for example, the limitation is thermal, a liquid or gas coolant can be used. Liquid coolant offers the added benefit of lubricating the cutting, thereby reducing the heat and force from friction. Low friction coating will also reduce the heat up of the tool.

5.1.5 Chip storage

As the broach removes material from the side of the via barrel, the material must accumulate in the tool until it exits the opposite side. This storage space is called the gullet, see Figure 5-12. The storage space is a fundamental limitation to broaching, because all the material removed must be carried all the way through the via barrel.

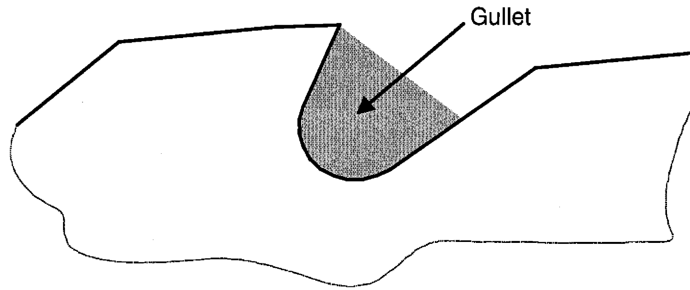

Figure 5-12: Broach gullet for chip storage.

The chip is stored with a packing efficiency that is a measure of the percent of material versus air filling the chamber. If the packing ratio is approaching or surpassing unity, the forces will rise rapidly, causing a failure of the tool, the PCB, or both. Figure 5-13 shows a failed broach with too little storage for cut material. The cut fiberglass/epoxy composite packed so tightly that the fibrous particles fused together, generating forces high enough to shatter the carbide teeth.

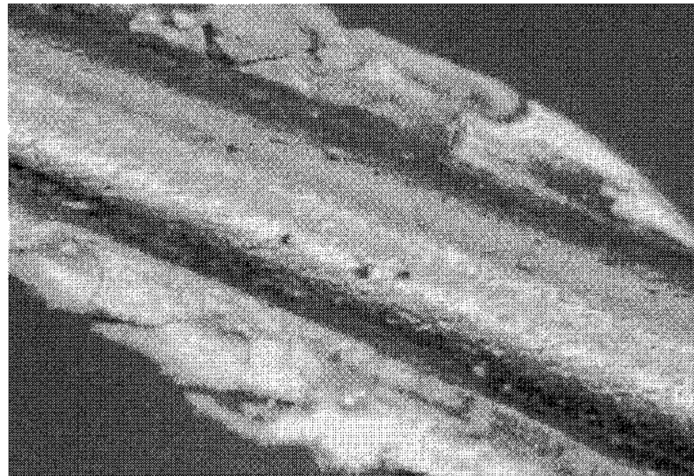

Figure 5-13: Results of overloading broach.

Packing efficiency depends on the shape of the chip, [Kaczmarek]. There is no published data for the packing ratio of cut fiberglass/epoxy composite. While the copper chip curls, the composite chip has a brittle fibrous form, and is, therefore, expected to pack differently. To completely understand packing capability for fiberglass, a thorough design of experiments would be required, which is beyond the scope of this research. Based on the tools tested, however, packing ratios of at least 60% are feasible.

The amount of material that is carried by each tooth is a function of the depth of cut (t_0), the width of cut (t_w), and the thickness of the PCB (t_{pcb}), as follows:

$$V_c = t_0 t_w t_{pcb} \tag{5-8}$$

The gullet geometry, shown in Figure 5-13, determines the amount of storage available and has the form:

$$V_s = A_{gullet} t_w \tag{5-9}$$

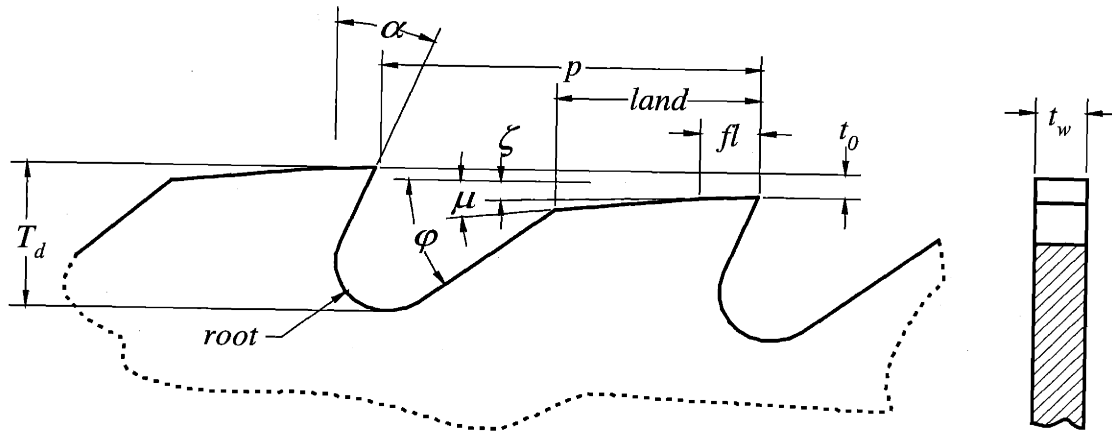

Figure 5-14: Broach geometry

The gullet depth is limited by the via diameter, (i.e., gullet depth cannot be more than the diameter of the broach and there must be enough material left to keep the tool robust). Figure 5-15 shows the difference between double-sided and single-sided tools, with respect to gullet depth. As illustrated, the minimum hole that can be broached is smaller for single-sided tools. An option for making a double-sided tool more robust is to stagger the teeth, as shown in Figure 5-16.

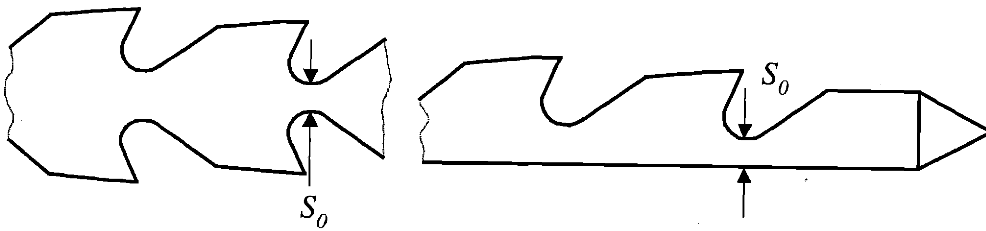

Figure 5-15: Double-sided and single-sided broaches.

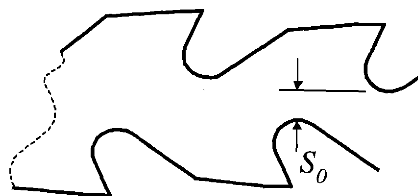

Figure 5-16: Staggered double-sided broach.

Two other factors affect available chip storage, tooth length (land size) and tooth pitch. Strength and robustness of the tool necessitates adequate tooth length. If the aspect ratio of the storage space to the storage depth was long, the chip will accumulate at the root, not using the extra space. Therefore, packing efficiency is the ratio of the amount of available storage (V_s) and the amount of material carried by each tooth (V_c).

$$\eta_p = \frac{V_s}{V_c} \tag{5-10}$$

or

$$\eta_p = \frac{A_{gullet}}{t_0 t_{pcb}} \tag{5-11}$$

Note that the broach thickness drops out. Summing the three areas shown in Figure 5-17 can approximate the gullet storage area (A_{gullet}). This approach applies as long as the aspect ratio is relatively low.

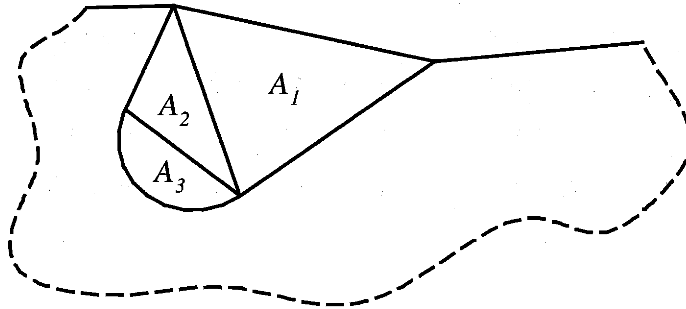

Figure 5-17: Calculating gullet area.

The goal of this analysis is to understand the size and scale limits of a broached via. To accomplish this, some simplifications must be made. First, a single-sided broach tool is used, because it can cut smaller holes than a double-sided tool. The smaller holes are possible because the single-sided tool throat (S_0) is greater for a given tool diameter when compared to a double-sided broach. Therefore, the throat thickness for the first tooth, shown in Figure 5-18, provides a size-limiting feature. Second two broach tool cases are considered a two–piece broach tool (i.e., an insert in a tool holder) and a monolithic broach tool. If S_0 is too small, there will not be enough material to support the insert. Finally, for the sake of simplicity, a minimum of twice the insert thickness, $2t_w$, will be required for the two-piece tool and t_w for the monolithic tool. Using the geometry of the two-piece tool, the throat thickness follows:

$$S_0 = \frac{1}{2} d_{tool} + t_0 - T_d + \frac{1}{2}\sqrt{d_{tool}^2 - t_w^2} \quad (5\text{-}12)$$

And for the monolithic tool:

$$S_0 = d_{tool} + t_0 - T_d \quad (5\text{-}13)$$

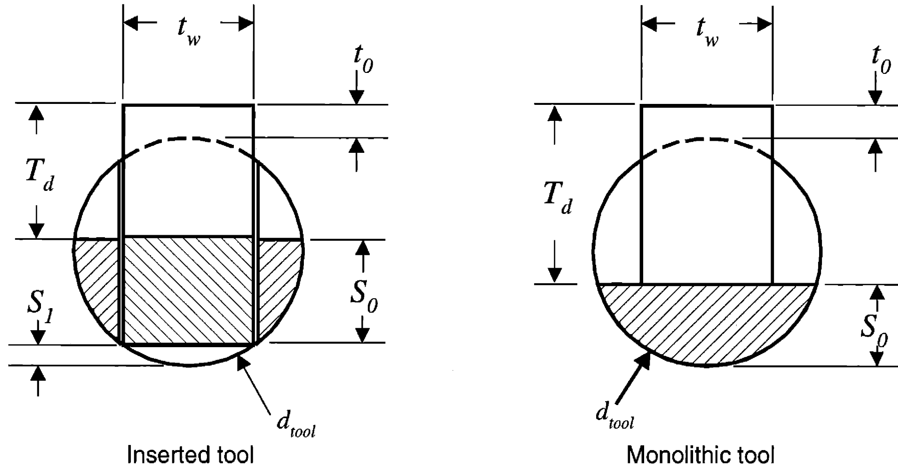

Figure 5-18: Front view section on first tooth.

The throat thickness formulations can now be used to explain size scaling, based on manufacturability. There is a correlation between the via diameter and board thickness, often referred to as the via aspect ratio. As the boards get thicker, the quantity of material accumulated in the gullet of the broach tooth increases, requiring a greater gullet volume. To tie this together, the geometric relationship of the tooth profile needs to be solved for the tooth depth. The tooth geometry must be optimized based on the via geometry and materials, while considering the cutting physics. Based on the limited experimentation, discussed in the prior sections, a first-order approximation is made using the following assumptions.

1. The cut depth, t_0, is limited by manufacturing tolerances assumed to be 13μm,
2. The packing efficiency, η_p, is set to 60%,
3. $T_d = \frac{1}{2} P$,
4. $land = \frac{1}{3} P$,
5. $root = \frac{1}{2} T_d$,
6. The flank and land have the same angle (set to 5°),

7. Rake angle, α, is zero,
8. Gullet angle, φ, is 35°, and
9. Tooth width, t_w, is 0.25mm.

Using these assumptions, the throat size, S_O, can be found for an inserted tool (as shown in Figure 5-19) and for a monolithic tool (as shown in Figure 5-20). Plotting the assumed value for minimum size provides a manufacturability bound. It is interesting to note that the ability to broach is relatively insensitive to board thickness. Holes as small as 1.1mm (using an inserted tool) and 0.7mm (using a monolithic tool) can be broached in a 12mm-thick board. These findings indicate applicability in backplane designs.

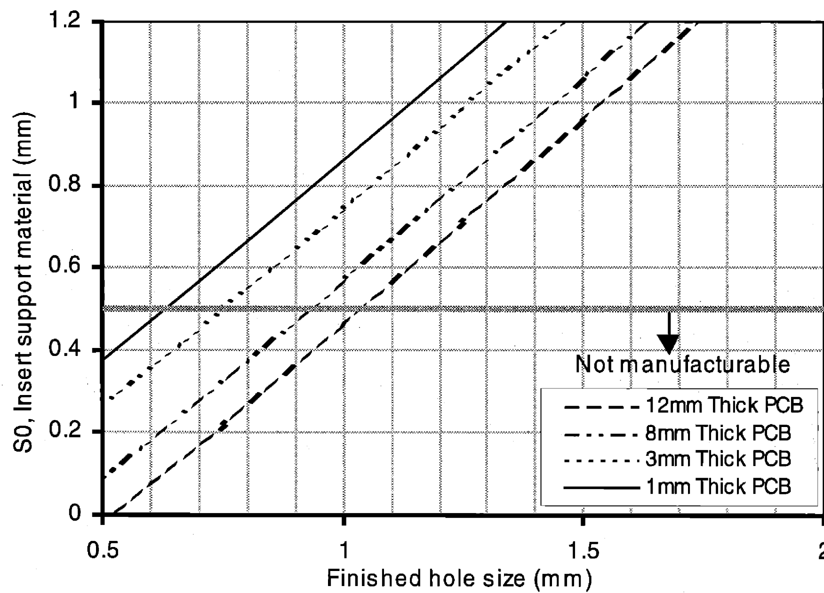

Figure 5-19: Manufactureability using inserted single-sided broach.

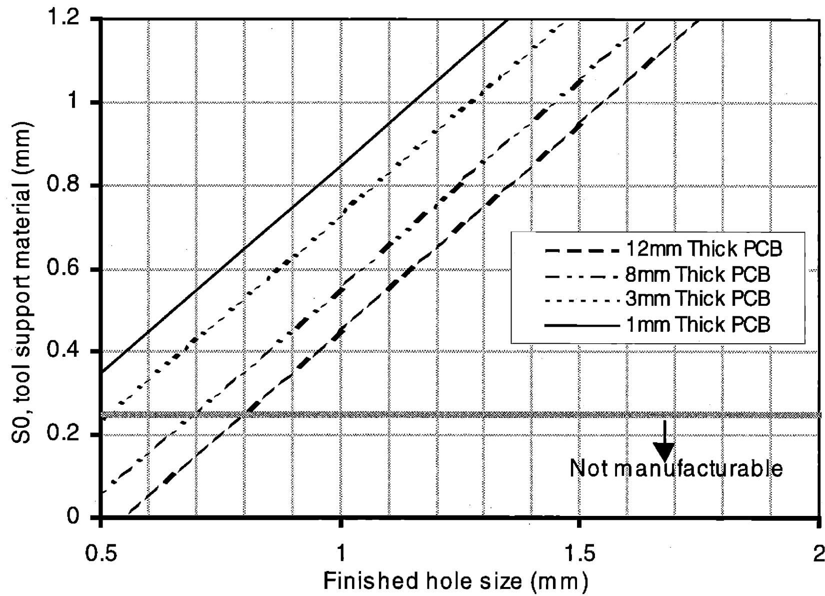

Figure 5-20: Manufactureability using monolithic single-sided broach.

Using the crossover levels from these figures allows for plotting of the aspect ratio (the board thickness to via diameter), Figure 5-21. Because the copper-plated via barrel has constant thickness, regardless of hole diameter, these curves have steep slopes. These results function as scaling rules for the two designs. For example, the monolithic tool can support aspect ratios higher than 15 for vias over 0.8mm in diameter. Thus, for large vias there is little limitation to board thickness.

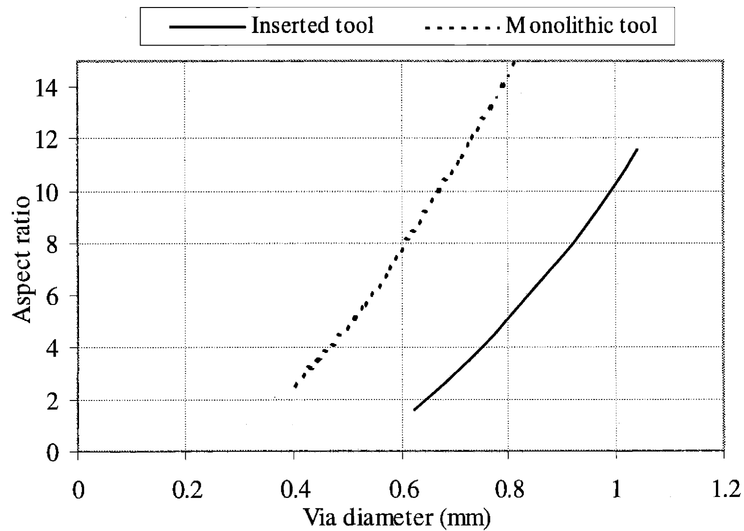

Figure 5-21: Broachable aspect ratio versus via diameter.

5.1.6 Prototyping

Several prototype tools were built to further explore the process, provide proof of concept, and prepare the force data used in refining the tooling model. The early experiments made it clear that the tool needed support on both the top and bottom of the PCB. This requirement drove the design of a manual broaching machine. In addition, the process of clearing chips from the broach teeth upon exit was addressed. The resulting multi-connection vias had very good form, but showed evidence of internal fiber damage. The following sections address each of these subjects.

5.1.6.1 Tool

Developing the prototype tool for this thesis took several iterations. It was first decided that a monolithic tool would be far too difficult to prototype. This decision was acceptable because scaling is not a priority for the initial phase, and an inserted tool was therefore developed. The simulation results revealed that the via diameter was not a factor in the via signal performance. This made it reasonable to select a larger diameter via, 1.5mm, for prototyping. This allows for improved process control, observation, and significantly easier tool prototyping.

In all cases, the inserts were manufactured from a solid block of carbide using wire EDM. A 0.25mm-diameter wire was used to first cut the broach profile from the block and then slice out the inserts, as shown in Figure 5-22. This process produced many inserts relatively quickly (total burn time per insert was less than 15minutes). Several iterations on the insert design were required.

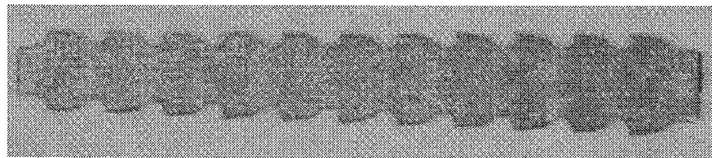

Figure 5-22: Carbide insert.

The first tool holder built was a simple round shaft with a slit down the middle, see Figure 5-23. The slit was produced with a slitting saw. The insert was then epoxied into the tool holder, and excess epoxy was removed by bead blasting. The epoxy proved adequate for prototyping purposes, but for production, an inserted tool would most likely require a silver solder process. Silver soldering such a small tool demands careful process control and complex fixturing. For

the prototype, an optical-comparitor was used to center the insert in the tool holder before the epoxy was cured, thereby eliminating any need for a fixture.

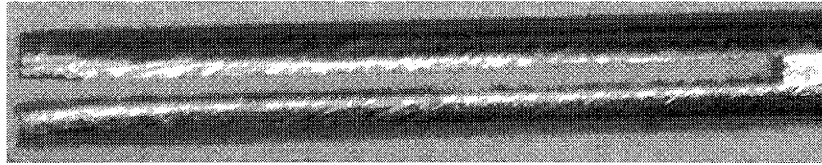

Figure 5-23: Front split tool holder.

This first tool revealed some problems. Because the tool holder was cut from the front, the cutting forces on the insert tended to spread the split. This spread would eventually break the bond and shatter the insert. Also, because the broach gullet was completely incased, the chips packed into the slot and had to be tediously picked out.

To address these problems, the tool was redesigned. As shown in Figure 5-24, the tool holder slit was moved from the front to the middle of the tool to eliminate opportunities for separation. In addition, the tool was relieved on both sides to the bottom of the gullet (see Figure 5-25) so the chip is no longer held on three sides. This relief was first produced by grinding, but later tools were relieved by wire EDM. The grinding was possible because the earlier tool had a constant diameter and could be fixtured with a small cantilever. Later tools had larger diameter bodies, allowing for a universal collet size for all tool diameters, but prohibited grinding of the relief.

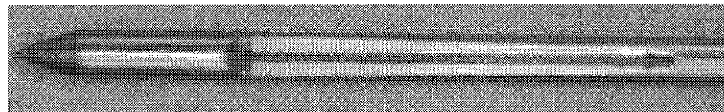

Figure 5-24: Center slotted tool holder.

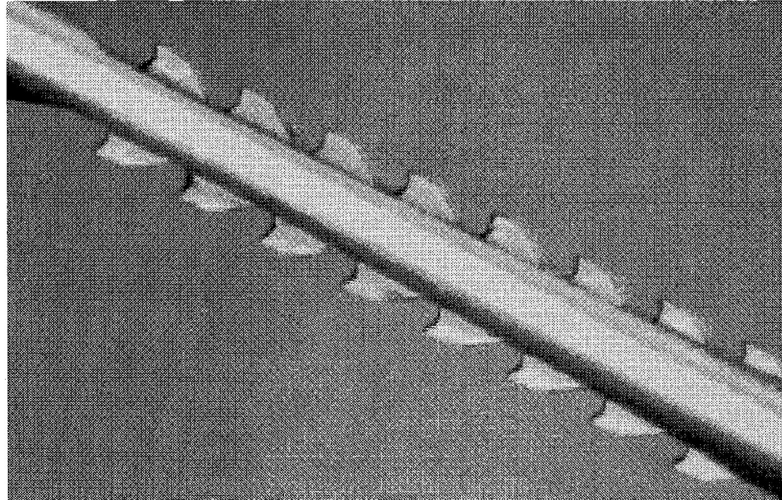

Figure 5-25: Prototype tool with relieved tool holder.

Some inserts were coated with Titanium Nitride (TiN), Titanium Carbonitride (TiCN), and Tungsten Carbide/Carbon (WC/C). No formal coating experimentation was conducted in this research; however, an optimal coating is expected to reduce the cutting force, increase tool life, and assist in chip shedding.

5.1.6.2 Manual Prototype machine

Initially, vias were broached by holding the broach in a Bridgeport milling machine and locking the head from rotating. The PCB was supported on two sides close to the hole. After all the broach teeth exited the backside, the collet was loosened and the tool was allow to fall through completely. It was possible to drop the tool through the vias because the early tool holders had a constant body diameter. This very slow process was necessary because there is no mechanism to keep the PCB held down, or to strip the tool from the PCB. Furthermore, the broach gullets could not be pulled back through the slot before being cleaned.

To scale the process for the larger number of holes required for the electrical performance test, a manual machine was designed. The machine needed to clamp the PCB tightly and guide the broach through the via. The upper guide was designed with special consideration for smaller tools, to prevent thinner broaches from buckling above the PCB. The lower guide was designed as a backing tool to support the work piece as close to the broach as possible and minimize breakout damage.

The machine, illustrated in Figure 5-26, allowed the PCB to float on ball transfers, which simplified the machine design significantly. A grid is bonded to the table surface to provide orientation reference. The trade-off for machine simplicity is increased operating complexity. Ideally, the PCB would be held in a frame with X- and Y-stacked linear bearings.

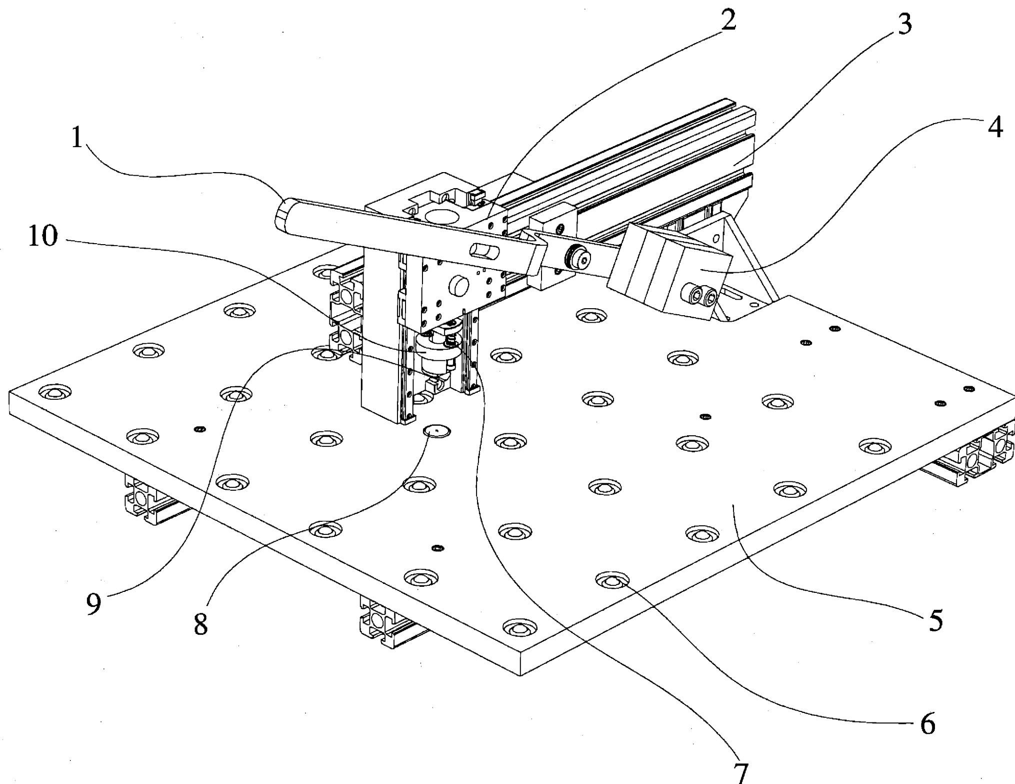

Figure 5-26: Manual split-via machine.

The head mechanism uses a counter-weighted lever, balanced to make the head neutral. Force is transferred to the head by a cam follower, shown in Figure 5-27. This force drives a carriage that houses the rotating portion of the head and a locking mechanism to prevent rotation once the desired cut angle is set. The tool guide is on a spring-loaded set of linear bearings that provides both the clamping force and the means of stripping the tool from the board on removal.

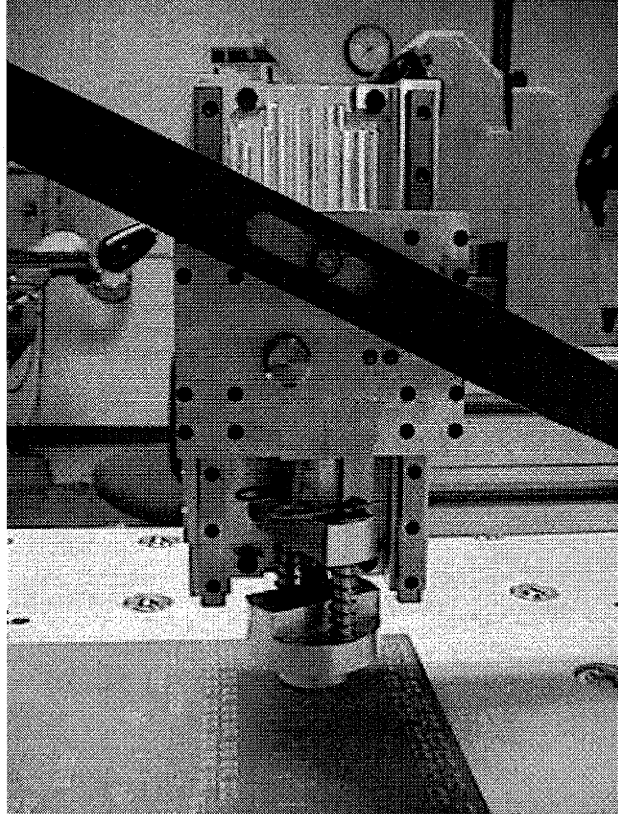

Figure 5-27: Manual broaching machine carriage assembly.

Removing the spring-loaded guide and the PCB leaves just the exposed broach, allowing for orientation of the lower tool. This allows the operator to rotate the lower tool-guide until it aligns with the broach. Upon replacing the spring-loaded guide and the PCB, the exposed broach tip guides the alignment to the via hole. Before driving the broach through the via, the PCB is oriented to the grid. After cutting and before withdrawing the tool back through the board, the teeth are cleaned by manual brushing. In the following section, an automated chip clearing mechanism is presented.

5.1.6.3 Chip clearing

When the broach emerges from the backside of the PCB, the tooth gullets carry the chips, as shown in Figure 5-28. If the broach is now removed by reversing the direction, the copper and fiberglass debris will be pulled up through the slot, which can wedge copper between via traces and cause shorts, as Figure 5-29 illustrates. Therefore, it is necessary to clean the broach before pulling it back through the PCB.

Figure 5-28: Broach tooth with copper load.

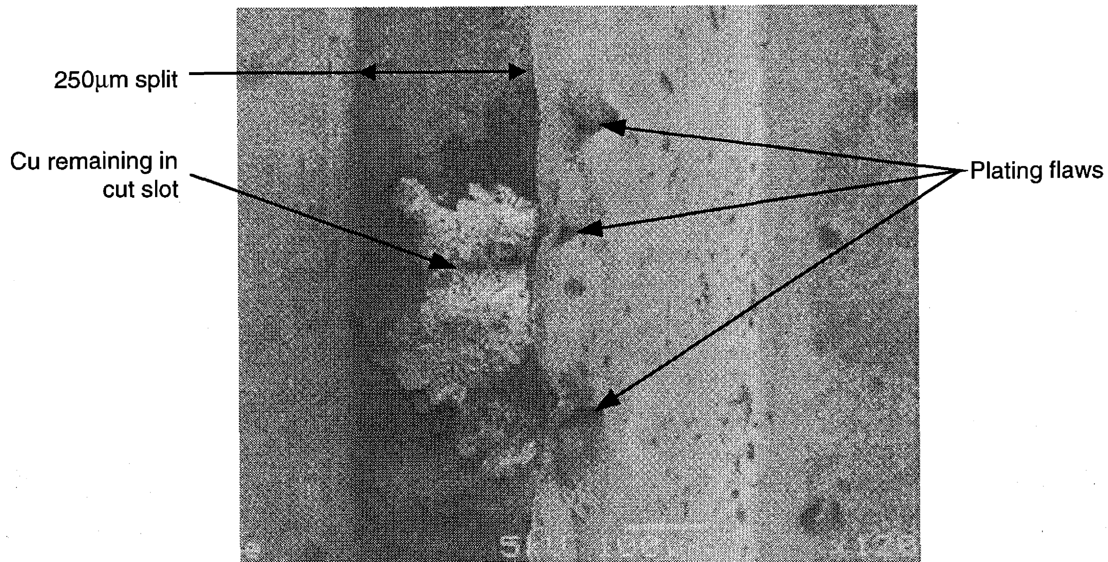

Figure 5-29: SEM of copper pulled back up through the slot.

As discussed in the prior section, broach cleaning can be accomplished with manual brushing. In the long-run, this cleaning needs to be automated to support production. Several experiments were conducted to determine what cleaning methods could be employed. Experiments with high-pressure air proved insufficient, while high-pressure water (with and without entrained particles) worked very well. A water-based system was prototyped, as illustrated in Figure 5-30.

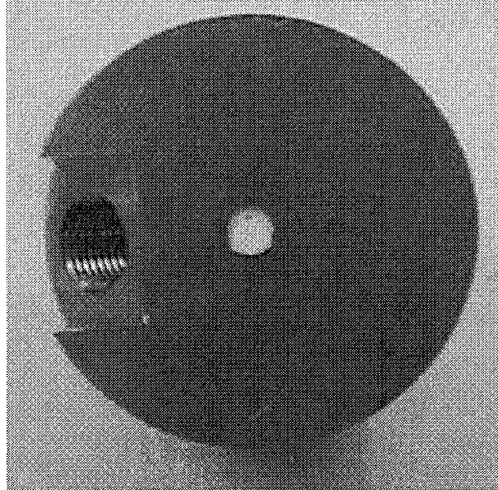

Figure 5-30: Broach cleaning nozzle.

5.1.6.4 Fiber damage

One common problem with cutting fiberglass composites is a damage zone in the cut region. Because the direction of the broaching action is normal to the layers, internal bending stresses cause localized delamination. In tests conducted, the delamination region is very clear (see microscope photo in Figure 5-31). The photo shows much larger delamination zones on the left side than on the right side of the via. This via was split with a two-sided cutting tool, and the teeth on the left were not as sharp as those on the right. In production, tool quality would likely be held more consistent than was possible for these experiments. The photo also illustrates that tool sharpness will have to be monitored during operation to minimize the damage zone.

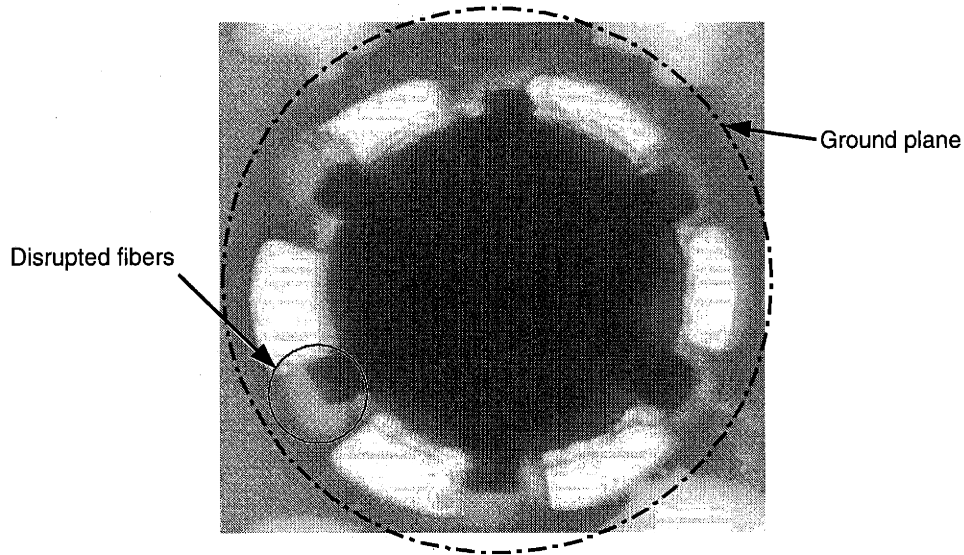

Figure 5-31: Fiber/matrix damage from broaching

From a routing perspective, this delamination region should be avoided. If ground plane routing rules are followed, (i.e., no routing under the ground plane clearance region), all the splits in the figure would be acceptable because delamination keep out zone is smaller than the ground plane clearance. The life issues discussed in Section 9.6 are of a greater concern as moisture and thermal cycling interact over time with the damage zone.

5.1.7 Broaching conclusions

It has been demonstrated that broaching multi-connection vias is feasible in small volumes. The tools tested are for 1.5mm-diameter vias and were design using conventional cutting force models. Ultimately, a more thorough design of experiments needs to be conducted. This process would require hundreds of precision experiments to develop a complete design model, theoretically resulting in tables or a program that would provide the exact broach design for given parameters. Because of variations in PCB plating, the via diameter will vary significantly, requiring the broach geometry to be selected after the board is manufactured. This development would require much larger resources and time than allotted for this research.

The scaling study – based on broach geometry and chip storage – showed that broach diameters below 500μm appear to be feasible for monolithic tools. This study indicated the inserted tools produced in this thesis will not scale as well as its monolithic counterparts. A manual broaching machine was designed, built, and used to manufacture multi-connection vias for electrical signal testing. While the design minimized fiber damage, there was still evidence that internal fibers

are damaged. This damage zone should be considered a routing keep-out area. Broach cleaning is a significant problem that was partially addressed with some experimentation. The proposed solution is a high-pressure water nozzle trained on the tool as it exits the via. If the tool is not fully cleaned, copper chips can be pulled back through the via causing shorts.

5.2 EDM

EDM is a process that is typically used in cutting hard tool materials. The process uses electrical discharges (arcs) between the work piece and the electrode that erode the work piece by melting or vaporizing (ablating) the material. The dielectric, which is usually mineral oil and in some cases distilled/deionized water or kerosene ([Kalpatikan]), functions to control the arc, flush the eroded material (swarf), and control temperature. There are two basic forms of EDM, sinking and wire. In sinking, an electrode with the inverse of the features desired is sunk into the work piece, creating a negative of the electrode surface. With wire EDM, a small diameter wire is continuously fed through the part to create simple and complex profiles. With four-axis wire EDM systems, complex three dimensional profile shapes can be created.

Because of the lack of contact between the electrode and the workpiece, and thus no forces to distort either one, provides tight tolerance control. The material removal rate is a direct function of the amount of energy dissipated. The size, geometry, materials and spark area of the electrode and the part, determines the energy consumption. Typically, EDM has relatively slow rates, generally limiting it to hard material tool and die cutting. While softer materials can be cut by this process, the costs are prohibitive compared to more conventional processes. Additionally, while high energy densities result in high material-removal-rates, surface finish suffers. The rough surface is undesirable in tooling but not as important for multi-connection vias.

In the case of the plated via it is only necessary to remove the thickness of the conductor in the barrel (usually less than 38μm). Figure 5-32 illustrates how using a round wire electrode cuts the plating while leaving the glass/resin core unaffected. Because the current must pass through two conductors, the spark stops once the plating is removed. This, of course, assumes that there is proper dielectric fluid flow to cool the region. Unlike other processes, which require the disruption of matrix and fibers, EDM has the potential to avoid damage in the split region. Therefore, the only fiber disruption would come from the original drilling operation.

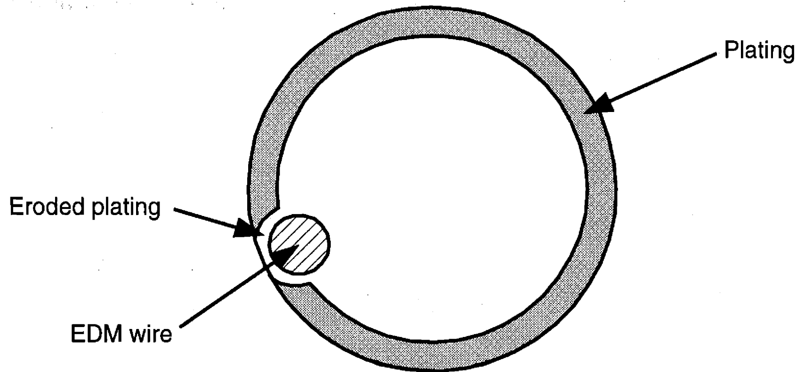

Figure 5-32: Schematic of wire EDM cutting of a via.

In experiments conducted on a test PCB, using standard-wire EDM equipment (shown in Figure 5-33), there is no visible composite edge burning, while the cut characteristic is as expected. The experimental cut rate was 360μm/s for a 3.175mm-thick PCB. Therefore, the cut time for 80μm-thick plating is approximately 220ms per split, without any rate optimization. Factors that can be varied for rate controls include: pulse frequency (typically 50-500kHz), voltage (typically 50-300V) and current (0.1-500A).

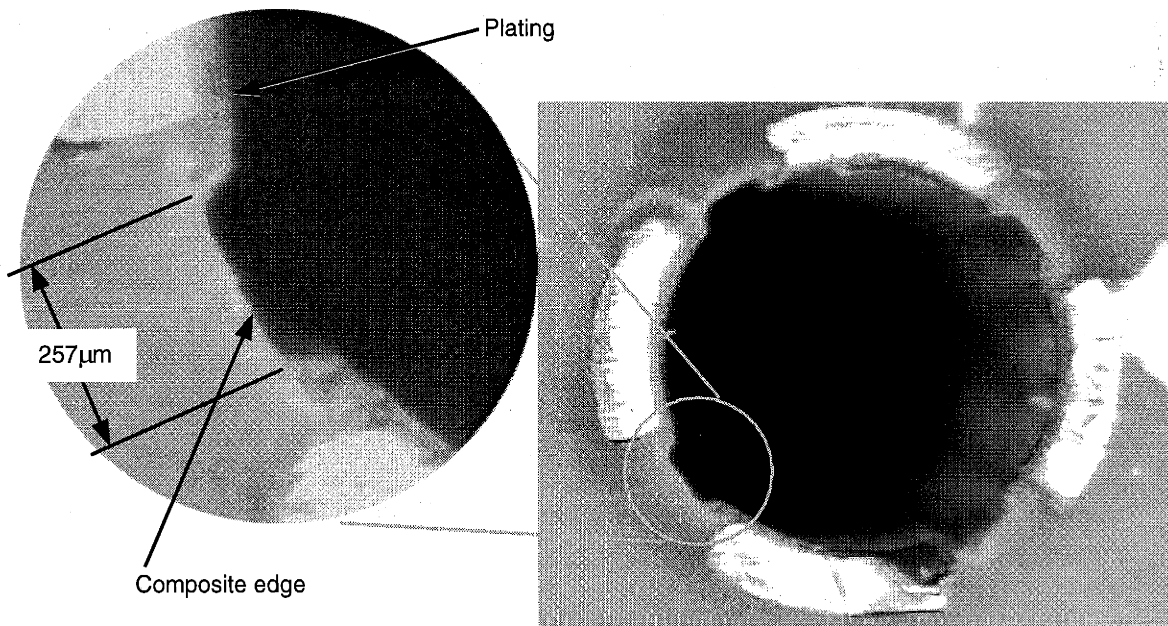

Figure 5-33: 1.5mm diameter, 80μm-thick plated via segmented by 254μm diameter wire.

Soldering the ground connection to all the traces provided the via grounding for this set of experiments. The development of production equipment would have to deal with this and other

limitations of standard-wire EDM equipment. Section 9.3.2 elaborates on some of these limitations and offers possible solutions.

5.3 Summary

Two processes were shown to produce multi-connection vias: broaching and wire EDM. Broached via manufacturing was explored in greater detail than wire EDM. The broach profile design was developed using basic cutting physics. Future design work will require a significant increase in resources to develop the experiments necessary for an accurate design model. Scaling rules for broach designs were developed to determine what via sizes and aspect ratios are appropriate for broaching. Broach tool prototypes and a manual manufacturing system were build and evaluated.

6 Multi-connection vias for layer-to-layer interconnect (LLI)

This is the first of three chapters that consider the design of products resulting from multi-connection via technology. The via itself, as a vertical signal routing feature, is the primary product, for example see Figure 6-1. All other products derive from the via design. This chapter builds on the knowledge gained from the signal integrity, density and manufacturing chapters to layout the design and uses of multi-connection vias. It is not possible to have via pads that are the same as conventional vias; thus, the pad design on each type of layer is presented. Non-vertically cut vias along with routing benefits are explored. Finally, multi-connection via routing provides unique challenges to the board layout; these challenges are introduced.

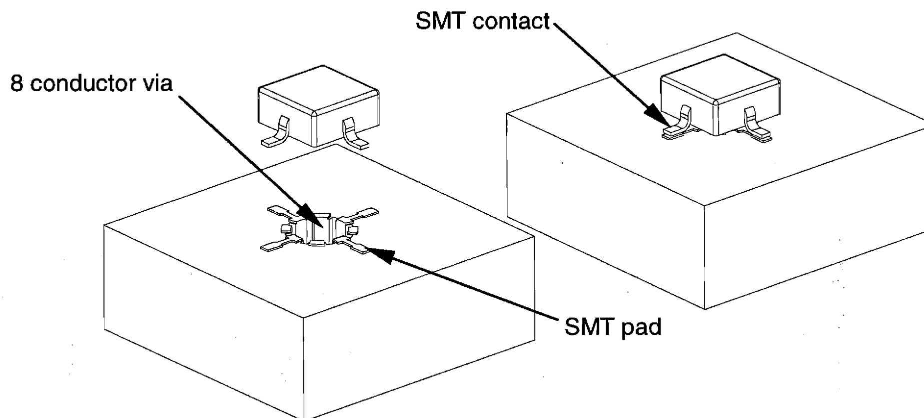

Figure 6-1: Surface mount device with split via for high signal speed routing.

6.1 Design of via section

The via barrel cross-section is the primary governor of signal performance. Designers only have control over the signal conductor arc length, the ground conductor arc length, and the gap width. The via diameter has a lower bound determined by the thickness of the board, such that the aspect ratio (board thickness to diameter) is supported by both the drilling and via splitting processes. There is effectively no upper limit to the drill diameter, and as shown in Section 3.1.1.3, the via can be tuned regardless of diameter.

With these parameters in mind, the cross-section of the barrel can be sized to meet performance and routing requirements. A good first-order approximation of the via cross-section impedance can be calculated by assuming that the diameter is large and using co-planar waveguide formulas, see Appendix C. For single-ended systems, the co-planar waveguide formulas result

in impedance relations, as shown in Figure 6-2. A more precise calculation of the section impedance can be found by using two-dimensional finite element methods. Knowing the impedance of the via cross-section, however, provides only a partial picture of the desired goal. This is because one-to-one impedance matching of the via to the board trace does not always give the lowest reflection and highest transmission. The lumped effect of the 90° transition from the trace to the via pushes the desired via impedance to a somewhat higher value.

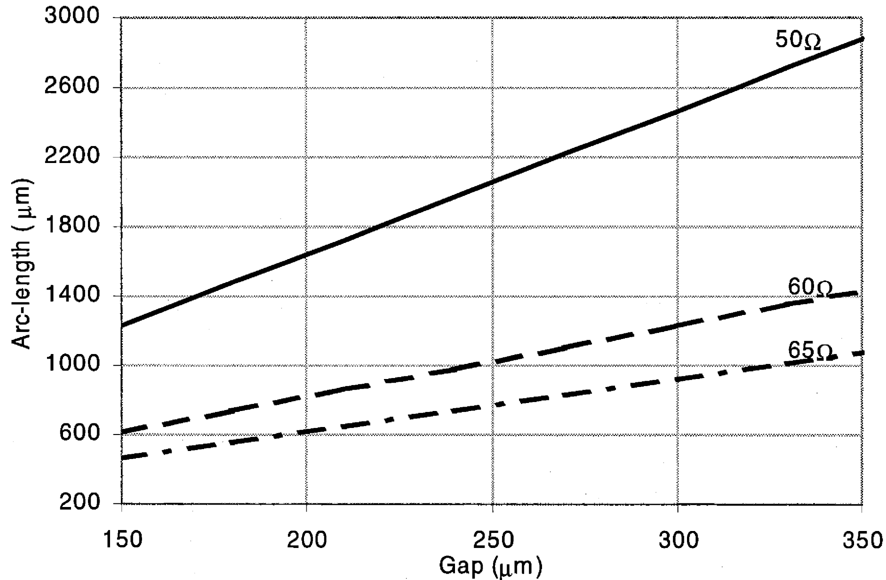

Figure 6-2: Co-planer waveguide assumption.

While these cross-sectional analysis approaches provide basic design rules, they do not provide the full solution available from a complete three-dimensional model. Three-dimensional models, such as those discussed in Section 3.1, incorporate the ground plane interaction, the stub affects, and the trace to via transition. It is not feasible, without significant future development, to model and optimize for reflection/transmission for every via in a large multi-layer PC board. One possible solution is to model a proto-typical via for a particular board lay-up to provide a general configuration for all vias of that size in that board. This is particularly well suited for boards that are standardized on single-ended or differential signals, with every via limited to one connection set. The one-connection set limit maintains a constant diameter for all multi-connection vias on the board. This solution has the added benefit of reducing tooling requirements for some of the proposed via production processes.

While from a routing standpoint limiting to one set of single-ended/ground, differential pair or differential pair/ground per via is desirable, multiple connection sets can also be created using multi-connection via technology. In situations where density is a priority and/or there is a pattern of vias (such as vias with connectors, BGAs or surface-mount device escapement), more than one connection set may be acceptable. Figure 6-3 illustrates some multi-connection single-ended and differential via sections. These vias function like the vertical superhighways of the PC board, where the on- and off-ramps can only come in at specified angles.

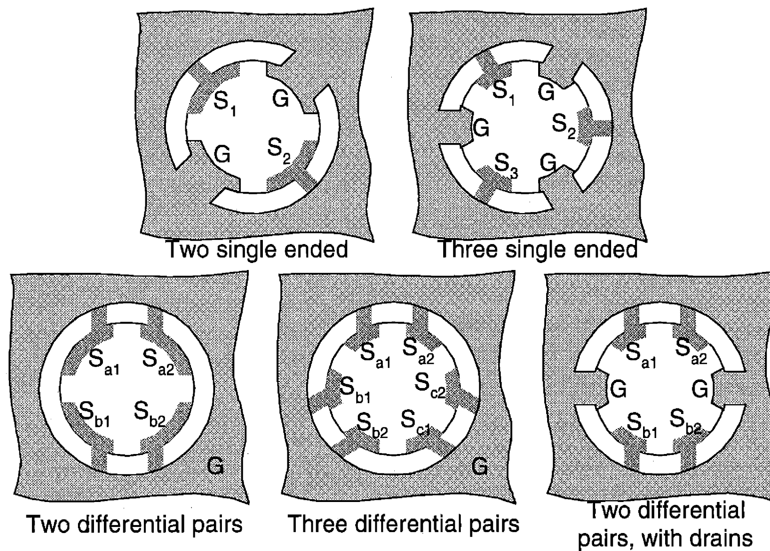

Figure 6-3: Examples of multiple set single ended and differential pairs.

In an ideal differential pair the field resolves between the pair without need for ground return. Manufacturing and material flaws, however, cause stray signals. Placing a ground structure parallel to the single pair provides a drain for these stray signals. As the experimentation in Section 3.2.2 illustrates, without a drain between multi-differential pair sets there is crosstalk. Therefore, the two cases without drains in Figure 6-3 should never be considered.

6.2 Pad design

As illustrated in Figure 6-4, there are two fundamental approaches to the design of the pad, parallel and radial splits. While both approaches can be produced with equal ease, the parallel split provides greater arc length for traces to connect to. This offers important flexibility, considering the difficulty in routing from a specific direction to the via.

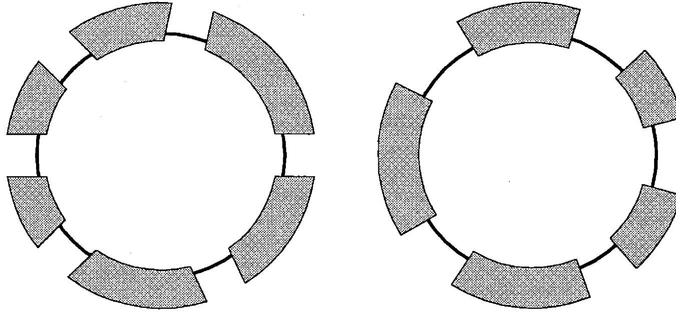

Figure 6-4: Parallel versus radial splits.

The gap size in the pad has to be larger than that of the split in the barrel. This requirement addresses the drill error from the actual pad location, as shown in Figure 6-5. As discussed in Section 4.2, the drill errors for smaller vias are on the order of 131μm. Thus, in a worst-case scenario, the pad gap would have to be 262μm wider than the barrel split (note, the errors for larger holes are less because the larger drill bits have greater stiffness). This width of gap causes the pad to decrease to an unacceptable size for smaller vias. If the barrel splitting operation were allowed to cut into the pad, as shown in Figure 6-6, the pad gap would only have to be large enough to prevent the two sides from shorting out at the maximum error condition or:

$$\frac{\delta_g}{2} + \frac{\delta_p}{2} > \phi_p \tag{6-1}$$

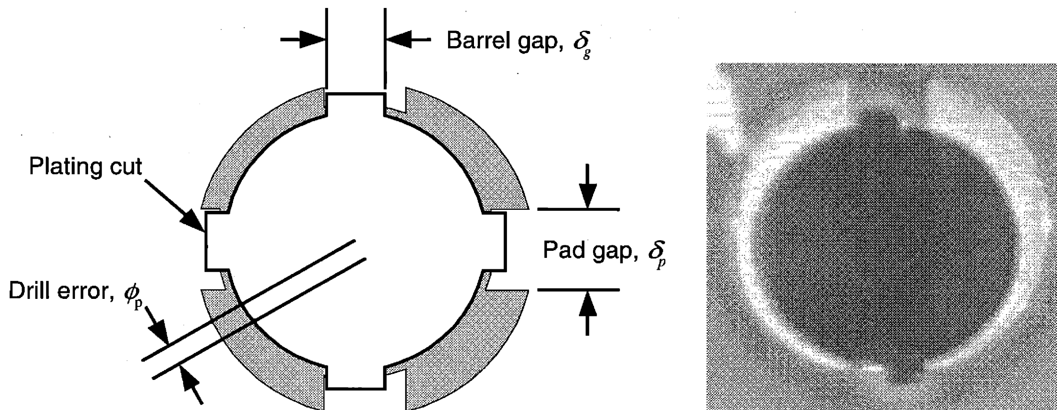

Figure 6-5: Error buildup.

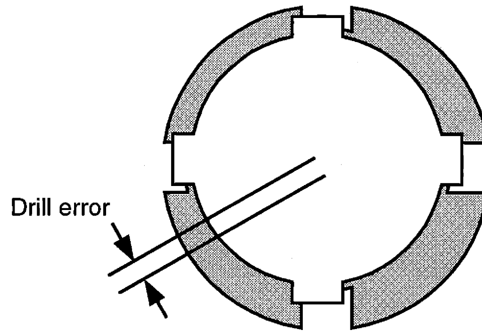

Figure 6-6: Allowing overlap between cut and pad.

Having established the desired outcome, the actual pad layer etching needs to be defined. Figure 6-7 shows the pad for a four-contact via. While the design of the pad center is not critical, because it is drilled away in subsequent operations. It is shown here completely separated with an inner radius to encourage drill centering. Traditionally, the signal pad design has been the same on all signal layers, but the necessity of high-speed signals forces the removal of all non-functional pads. Figure 6-8 illustrates the pad stack for a single conductor shielded via, where signal layers without connections have no pad. Once drilled, plated, and split, the pad stack looks like the example in Figure 6-9.

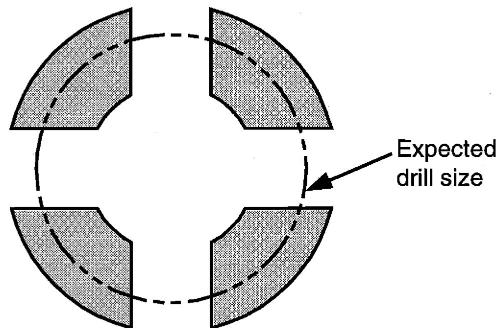

Figure 6-7: Pad before drilling and plating.

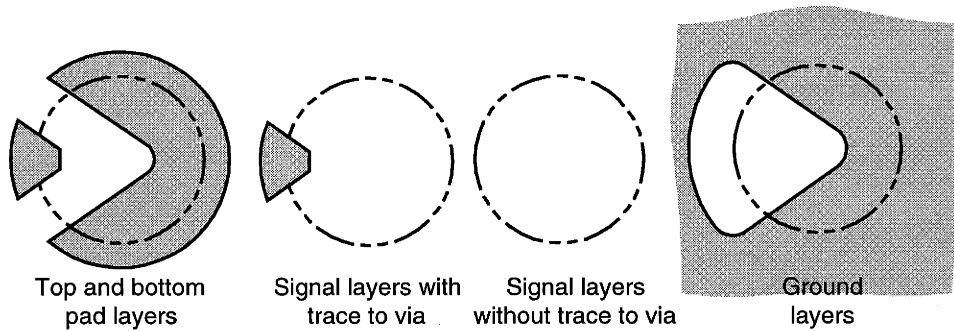

Figure 6-8: Pad stack design before drill/plate.

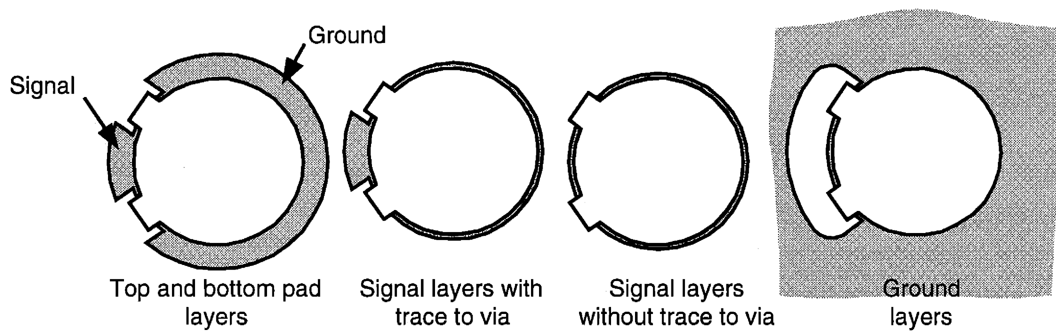

Figure 6-9: Pad stack design after drill/plate.

The design of the ground layer is very important for maximum routing space. The keep-out zone is essentially the ground clearance area around the signal conductor. This allows traces to be run very close to the via on all other sides, as discussed in Section 4.2.1. If a ground via is to receive a soldered connecting pin the ground plane design needs to provide reduced connection area to the via, thereby reducing the heat transfer from the via to the ground planes.

This development is based, in part, on the experience of the simulations and experiments in Chapter 3. The pad and ground plane design can be further optimized for signal performance by conducting focused simulations.

6.3 Non-vertical opportunities

All the concepts presented so far show vertical or axial splits, which were proposed as early as 1968 [Reinhart]. This section considers the design opportunities available through non-vertical separation in the via plating. Figure 6-10 illustrates a proposed horizontal or radial split that can be used on its own or in conjunction with axial splits in a via. The radial split is electrically similar to blind and buried vias without the additional process expense. Some processes

proposed in Section 9.3 can produce this type of feature. It was not possible in the timeframe of this research to reduce this to practice. Therefore, this discussion is purely conceptual.

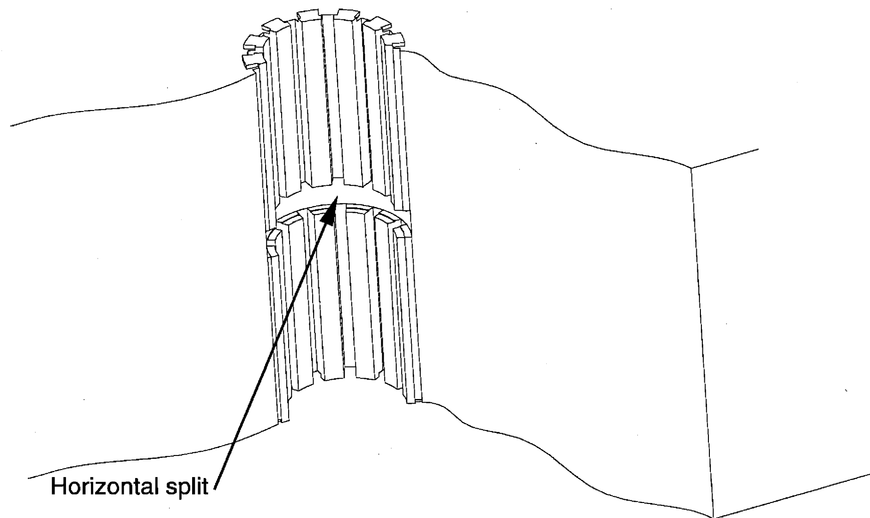

Figure 6-10: Two-dimensional split via

In addition to increased layer-to-layer routing, horizontally-split vias can significantly reduce reflections caused by unused via extensions. Some board manufactures get this benefit by counter boring out the unused end of the via (Figure 6-11). Counter-boring has the advantage of using conventional drilling equipment. However, not all PCB drills can do controlled-depth drilling. In horizontally-split vias, each level operates as a separate set of connections, thereby improving space usage over counter-boring.

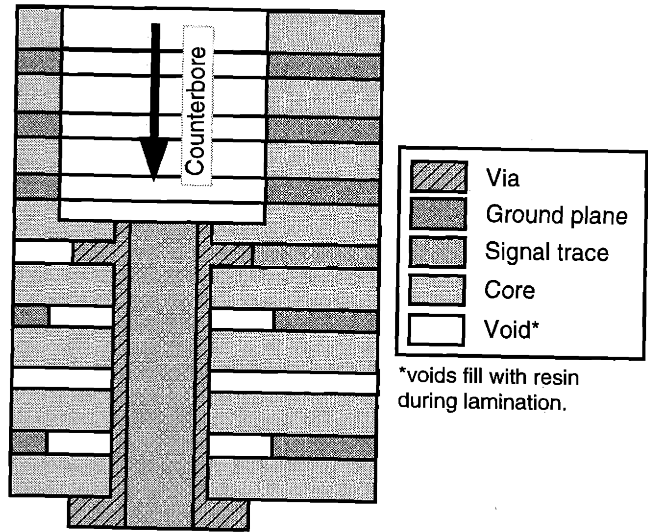

Figure 6-11: Section of conventional via with stub counter-bored.

A further permutation on this theme requires a complete shift in the manufacturing goals from "splitting vias" to creating traces on the inside of the via cylindrical surfaces. Vertical- and horizontal-split vias now become a subset of the "in-via trace" (IVT), illustrated in Figure 6-12. The IVTs shown represent the best performance geometry possible using the paradigm of a drilled and plated hole, because they virtually eliminate via reflections, stub affects, and out of board EMI (see Appendix B). Another benefit of this geometry is the ease of routing. As with conventional vias, the IVTs can be routed from any direction and simply rotate to meet the trace.

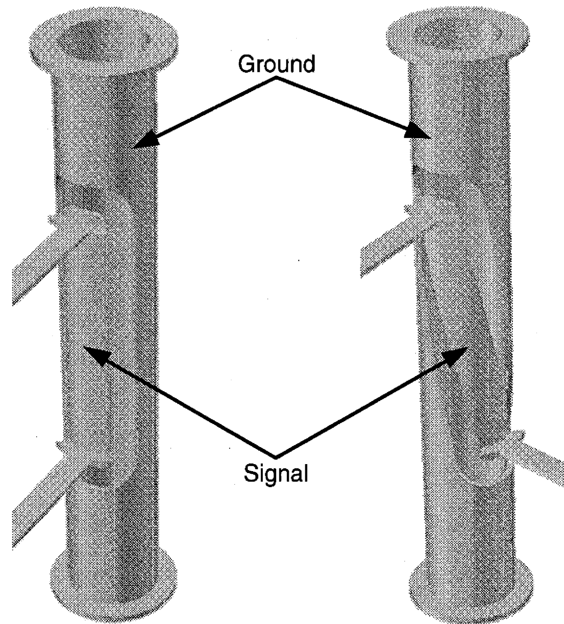

Figure 6-12: In-via trace, vertical (left) and off angle (right).

6.3.1 Buried and blind

Like standard single-connection vias, multi-connection-vias can be setup in blind and buried configurations, see Figure 6-13. Fabricating separate panels then laminating them together creates a single board with vias sandwiched inside. While expensive, this is an accepted practice for high-performance PCBs. In addition to all the electrical benefits of counter-bored or horizontally-split vias, buried and blind vias do not disrupt the routing space above or below the via.

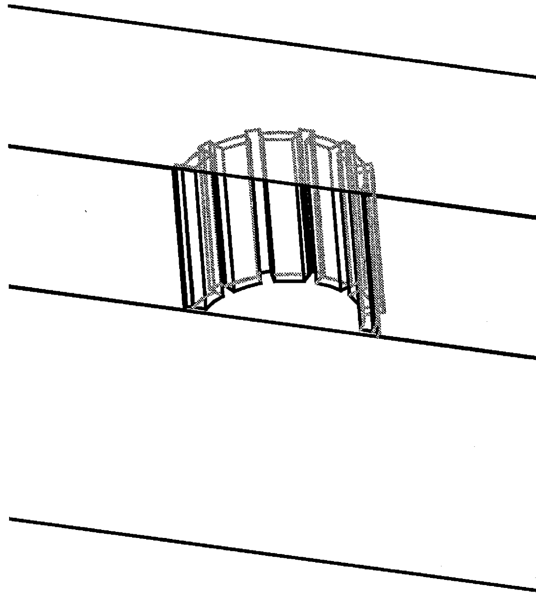

Figure 6-13: Buried multi-connection via.

For multi-connection vias, the panel laminating process has the added benefit of filling the via with resin. This addresses the durability concerns of having disrupted fibers by sealing the via. Dielectric change would require the design of the cross-section to change somewhat.

6.4 Routing considerations

Conventional vias allow traces to enter and exit from any angle, making routing straightforward. Typical PCB layout software automatically routes traces from devices through vias. Except for the case of IVTs, multi-connection vias add an additional element of complexity because they must be routed from one side only. Figure 6-14 illustrates some examples. While the angle of the signal segment can be adjusted, entry and exit layers must approach the via from the same direction. This limitation can be even more difficult with multiple connection sets. Differential pair sets will naturally approach from the same side on each layer.

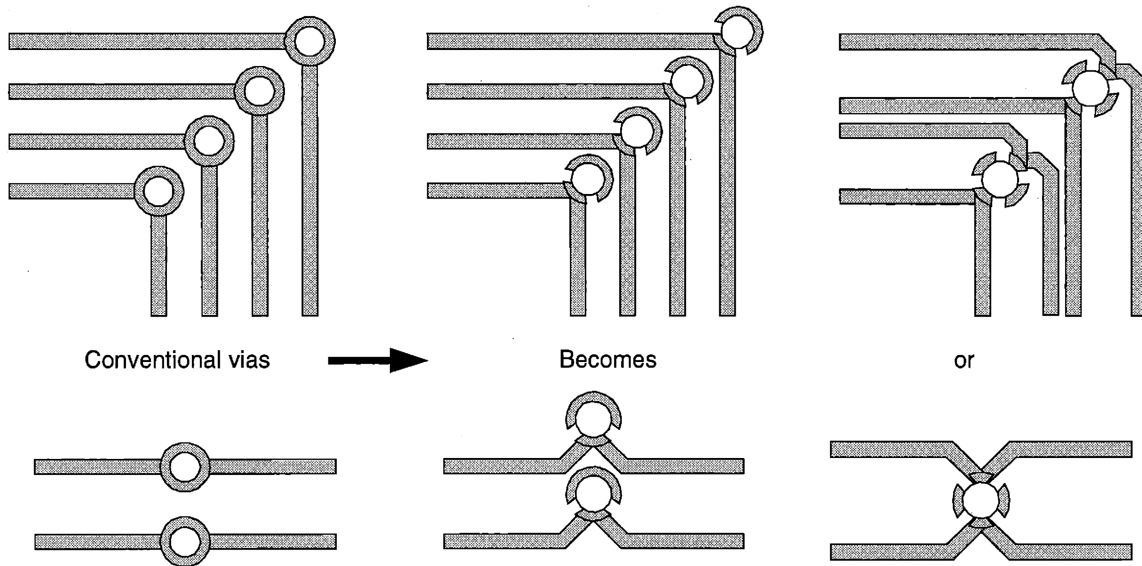

Figure 6-14: Examples of the how routing has change.

In cases where regular via patterns and split angles are established, such as in connectors; routing methods can be designed as a repeating pattern. This discussion intends to merely describe the problem. The solution is a much larger project than can be reasonably developed here. It is clear, however, that if multi-connection vias are to be used by board designers, layout CAD software will need to automate this part of the routing process.

6.5 Benefits of multi-connection vias in PCBs

The electrical signal performance analyses indicates that the general design rule of minimizing layer changes for high-speed traces is not necessary for multi-connection vias. Assuming, the design minimizes the via stubs. Properly impedance matched vias have been shown to eliminate reflections up to 5GHz and support 100ps rise times. Eliminating this design constraint allows signal trace paths to change layers in areas of congestion. Potential payback derives from reducing the number of layers required to maintain the conventional design rule. Eliminating this design constraint is of particular interest to larger high performance boards where long trace signal attenuation is significant. To prove this hypothesis, experimentation and modeling still need to be conducted.

The main problems with long traces are signal attenuation and degradation. The dielectric constant and loss tangent, and EMI losses in the signal path drive the attenuation, all of which increase with frequency. Most high-frequency traces must pass through one or two vias at the being and end of the trace. By using multi-connection vias for these layer changes, the EMI

losses in the signal path reduce. Signal degradation is a result of both reflections from discontinuities and crosstalk from EMI sources. These in-board EMI sources are often from nearby vias. Multi-connection vias have been shown to reduce EMI when compared to conventional vias. Thus, it is postulated that a long trace passing by many vias will gain less crosstalk noise if those vias are impedance controlled.

Vertically-split, multi-connection vias provide the best signal performance when run from the upper-most layer to the bottom-most layer, primarily because the stub affects are eliminated. Consequently, in cases where no stub elimination processes are employed (i.e. horizontal splitting, counter-boring, blind/buried vias or IVT), multi-connection vias provide a near-reflectionless signal channel from the top of the board to the bottom. In situations where stub elimination processes are employed, near-reflectionless routing can be obtain between any set of layers.

Therefore, the argument in favor of multi-connection vias is connected to minimizing the free energy (EMI) in the board and the reduction of the signal path mismatches. Eliminating EMI from the via increases the transmitted energy in that path. At the same time, the free energy, in the form of magnetic and electrical fields, is not available to drive crosstalk in adjacent signal paths.

6.6 Summary

This chapter explored the detail design of multi-connection vias purely as a LLI. The cross-section design was presented from a signal performance and density standpoint. The design of the layer pad was explored considering tolerance issues. Pad stack designs were discussed and exemplified. Non-vertical design possibilities, the concept of an IVT, and the benefits of blind and buried vias were presented. Finally, the particular complexity and benefits of routing multi-connection vias was introduced.

7 Board launch design for multi-connection vias

While the prior chapter explored the design of the multi-connection via itself, this chapter expands to the secondary via function of connecting devices to the circuit board. Board launch is defined as the electrical connecting element between the device or connector and the PCB. Concepts that use the via to provide this launch in both pressfit and solder-tail applications are discussed in Chapter 8. As simulations in Section 3.1.2 demonstrate, multi-connection vias offer a unique opportunity for improving board launch performance by controlling the field through the launch transition.

This chapter explores the design of this type of board launch. A contact design case-study was conducted, and the study details are discussed in the following sections. Resulting multi-connection launch concepts are explored using this contact design. In addition, a shielded via concept with only one connection in the via is addressed. These concepts are intended as a starting point for further consideration in the following chapter.

7.1 Contact types

Early in the history of the printed circuit, PCBs were one sided, where the devices and connectors had pins that passed through holes and soldered to pads. This practice continued with two-sided and multi-layer boards with one change, the plated barrel. Connections are still soldered in this fashion, using wave solder machines to solder the entire board in mass. When multi-connection vias were originally proposed, connections were described as soldered in this same fashion, see Section 1.2.

The main challenge in soldering connectors to multi-connection vias is keeping the solder from bridging the small gap between via splits, especially in smaller vias. If the connection is prepared with a solder paste or plated with solder, and placed in a reflow oven, this problem may be eliminated.

Wave solder machines cause other undesirable problems in connector processing and for boards with SMT devices. One side of the board is completely brought in contact with a wave of solder, limiting the placement of connectors and devices on the opposite side of the board. These problems have driven the development of the compliant pin or pressfit connection for connector

design. The pressfit connections are solder free and rely on mechanical forces to maintain connection and retain the connector.

Like the via, pressfit-type contacts are usually plated with tin-lead (solder). A gold plated connection is not necessary here, because the press-in forces are high enough to yield the material in the contact zone. In the case of separable connections, which need to be able to mate and unmate hundreds or even thousands of times, gold plating is required on both surfaces. It is possible, due its larger diameter, to use a multi-connection via for a separable interface. This option requires both the contact and PCB to have gold plating. Plating gold on PCBs is a common process (edge-card connectors rely on it), but adds significant manufacturing cost, which have to be offset by the benefits.

7.2 Contact design case study

A test contact that connects to a multi-connection via was designed for this research, see Figure 7-1. The test contact was intended to facilitate electrical testing, mechanical reliability testing, and connector mockup. Its design considered the contact and beam forces required; and it was constructed from a progressive stamping tool, shown in Figure 7-2.

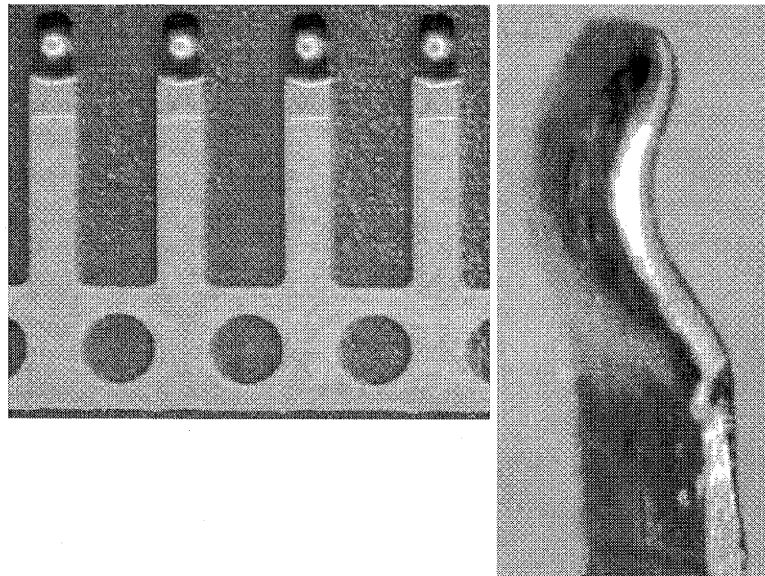

Figure 7-1: Stamped test contact.

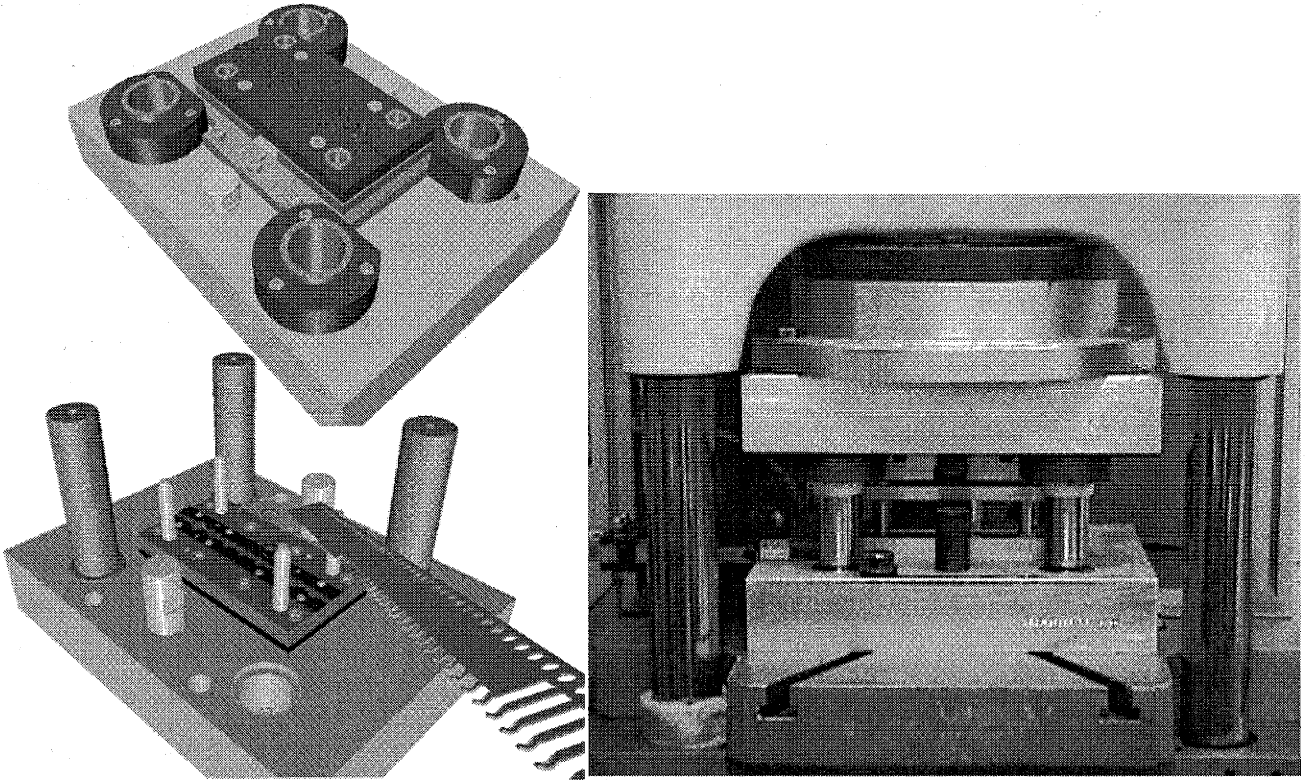

Figure 7-2: Die used to manufacture test contact.

Connector contact forces are critical to the reliability of the electrical connection. The contact pressure must be high enough to keep the contact points sealed from the atmosphere, [Dally]. Contact stresses required for a typical connector with a gold-on-gold interface are on the order of 1.0 to 1.4GPas. Figure 7-3 illustrates the contact geometry of this interface with a spherical contact on the inside of a cylindrical barrel. The stress were calculated using Hertzian contact stress formulas for curved surfaces, [Slocum].

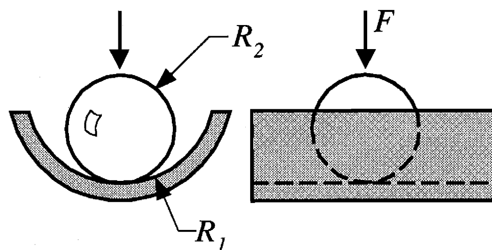

Figure 7-3: Sphere on inside of cylinder.

To generate this force the contact typically employs an elastic member, often beam elements, preloaded against the contact surface. Beam cross-section and length design determine the contact force from the displacement at insertion. Because the scale of these components and

features is so small, the geometry tolerances must be considered in order to meet the force requirements without yielding the beam. Gage thickness also requires that plating is accounted for in the beam section, as shown in Figure 7-4. Nickel is plated under the gold to prevent copper diffusion through the gold, reduce gold thickness, and increase wear properties, [Brush Wellman]. A composite beam model is used to calculate the cross-section moment of inertia, [Beer and Johnston].

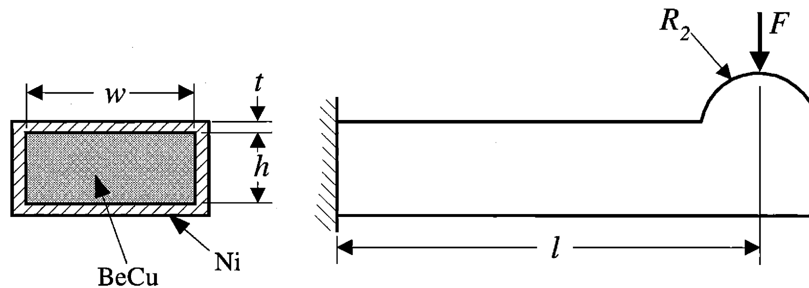

Figure 7-4: Beam geometry.

The resulting contact design fits into the 1.5mm-diameter via of the test PCB (from Section 3.2) to provide a two-contact board launch. If the pitch is 3mm by 2.6mm (allowing for one- and two-track routing channels), the signal density is on the same scale as commercially-available 2mm pitch connectors (on the order of 0.25 connections per mm^2).

7.3 Multi-connection launch concepts

To develop commercial devices and connectors that take advantage of this type of contact, the launch geometry must be defined. This section explores some concepts for two-, three- and four-conductor vias, while expanding on the contact geometry developed in the last section. Most of the concepts presented can function as permanent or separable interfaces. The intention is to illustrate some of the possible permutations, which can easily be the subject of many more detailed analyses.

The simplest derivative is to have two connections in one hole. The two connections can either be a signal and a ground, or a differential pair. Figure 7-5 illustrates a two-connection launch using a pressfit connection. The contact surfaces are the inside of the cylinder and the spherical surface of the conductor led. Reinhart and Barnhouse proposed another permutation, a solder-in connection, which is the multi-connection version of the through-hole soldered launch.

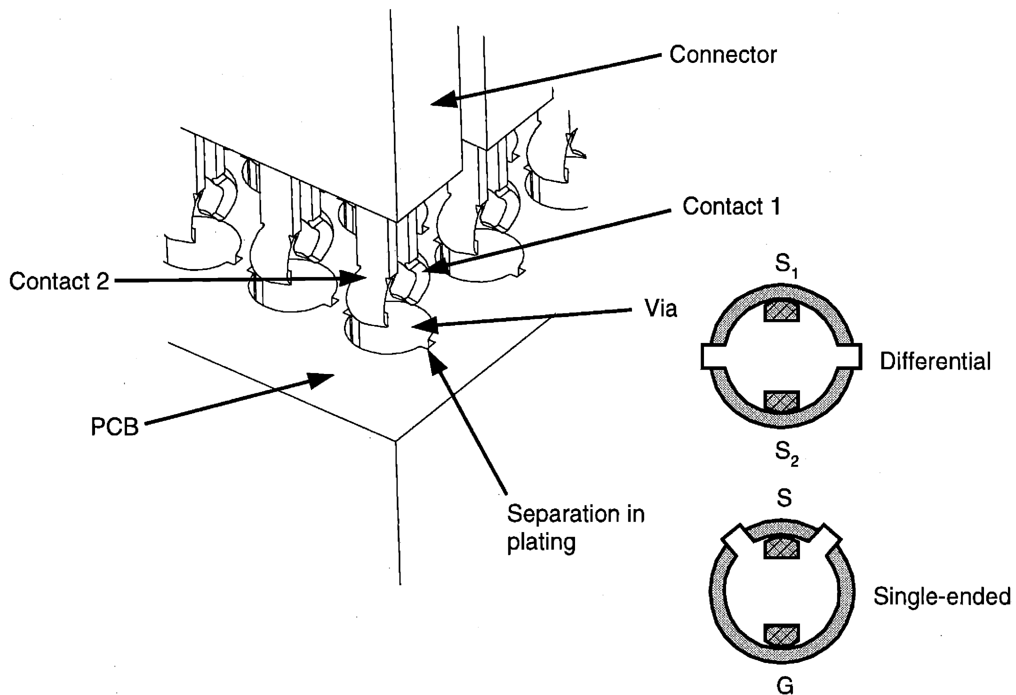

Figure 7-5: Two contact press-fit.

For differential connections, it is desirable to have a ground structure close to the differential pair. Usually referred to as a drain, this ground structure provides return to stray signals due to imperfections in the differential pair. Figure 7-6 shows a concept with connector elements that provide the three connections required for a good differential pair. As before, a pressfit connector is illustrated but a soldered-in connector is also possible.

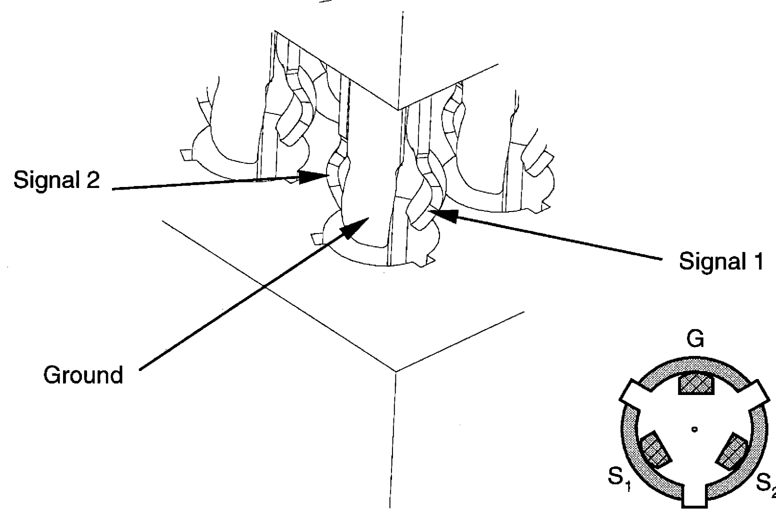

Figure 7-6: Three conductor modular connector.

Scaling the number of connections to four per hole provides for two single-ended signals and two ground segments separating them. Figure 7-7 shows a single ground contact that makes connections to two opposite segments of the via, separating the two signals. The advantage of this design is an inherent manufacturability of the connector due to the symmetry. Figure 7-8 is a variation on this configuration using surface mount connections for the signals. This hybrid incorporates known connector technologies, namely eye-of-the-needle pressfit and SMT, with a multi-connection via. The advantage here may be acceptance. Another variation on this design would be to replace the SMT contacts with pressure-mount pads. The pressfit contact provides the required retention force.

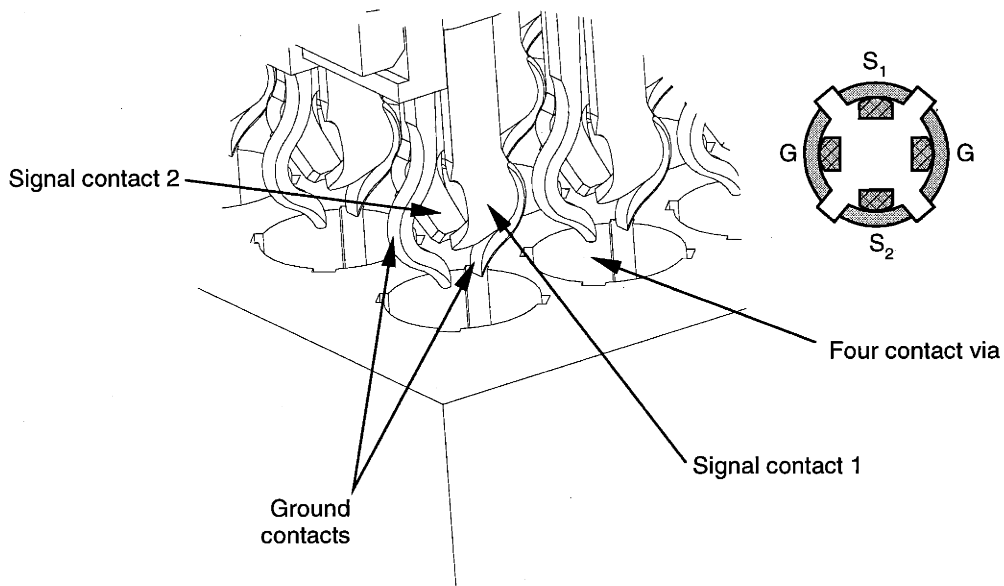

Figure 7-7: Two pairs shielded connection details.

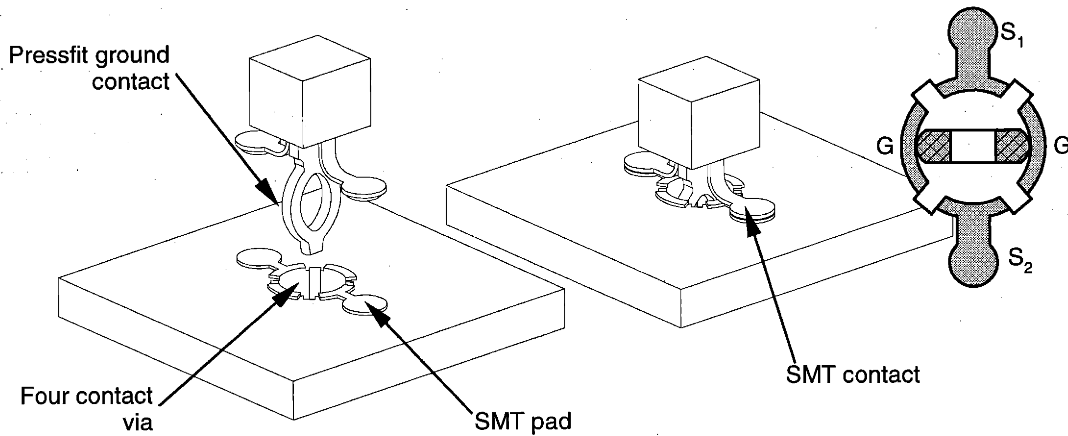

Figure 7-8: Pressfit and surface mount (SMT) hybrid connector.

7.4 Shielded via launch

One way to use the multi-connection via technology without changing connector design is with the shielded via concept, shown in Figure 7-9. While not as optimum for ground loop as concepts described in the previous section, a shielded via provides some performance gains. The main benefit is that it only requires a change in board routing to overcome the limitations of trace-to-via connection. The trace would only be required to connect to one of the two via signal

sides. Ground plane design would also have to accommodate ground connections, which provide a secondary benefit of a wider routing channel. As discussed in Section 4.2.1, the single traces can be run very close to the via ground sides, effectively widening the routing channel. In general, a pressfit-type connection is more conducive to this concept; but if a process for masking inside the hole over the ground elements was possible, then a soldered connector would be possible too.

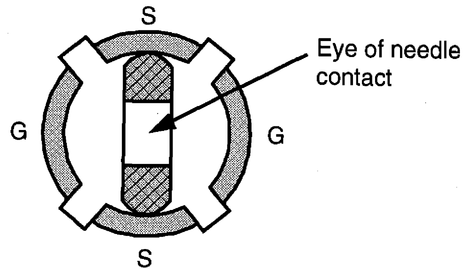

Figure 7-9: Single contact shielded via.

7.5 Summary

This chapter explored board launch design using multi-connection vias. Pressfit, soldered and SMT connection types were configured in two-, three- and four-contact concepts, as was a shielded via that utilizes conventional contact design. The design of a stamped contact and beam was presented. Both differential and signal-ended launches were evaluated and confirmed possible.

8 Multi-connection vias for connectors and devices

The last two chapters provide the basic building blocks for the development of countless permutations of connectors and devices. The application of multi-connection vias to the board launch offers potential signal performance and density gains for existing devices. This chapter presents concepts in different areas of application to illustrate some of the possible design avenues. Within the scope of this research, concepts are presented on the highest level, leaving details to future development.

Concepts covering connectors focus primarily on large array board-to-board interconnection, due to scope limitations not due to any inherent limitation of the technology. Bypass capacitors offer a unique opportunity for reduced inductance path and broad design options that go beyond retrofitted devices. While the bypass capacitor represents a small-scale device, the final concept of an IC package offers a larger scale example.

8.1 Connector concepts

Connector levels are categorized by the electronics industry, depending on how far a connection is from an actual device. Table 8-1 lists these level categories. This section focuses primarily on level-3 connectors, but does not preclude the development of non-level 3 connectors with multi-connection via launch. Launch concepts from the last chapter apply to both parallel and right angle level-3 connectors. Concepts for pogo pins and circuit board test probes are also developed.

Table 8-1: Connector levels.

Level	
1	Device (IC to package)
2	Package to board
3	Board to board
4	I/O (outside of box)

8.1.1 Parallel board concepts

Parallel board connectors find most common use in mezzanine boards and parallel daughter cards. While these connectors usually fall under level 3, using them for multi-chip modules (MCMs) technically raises them to level 2. Figure 8-1 shows a two-contact parallel-board

connector, which uses the PCB as a separable interface on one side and a permanent interface on the other. This design reduces part count, the number of actual connections in series and the stack height when compared to two piece connector designs like the one shown in Figure 8-2. A two piece connector design eliminates the need for gold on the PCB, and reduces a process step for most boards. The optimum configuration is provided by setting up the contact pairs with single-end signals (one ground and one signal) for both of these connectors. While feasible, configuring the design as a differential pair neglects stray signals from imperfections in the pair, and causes crosstalk.

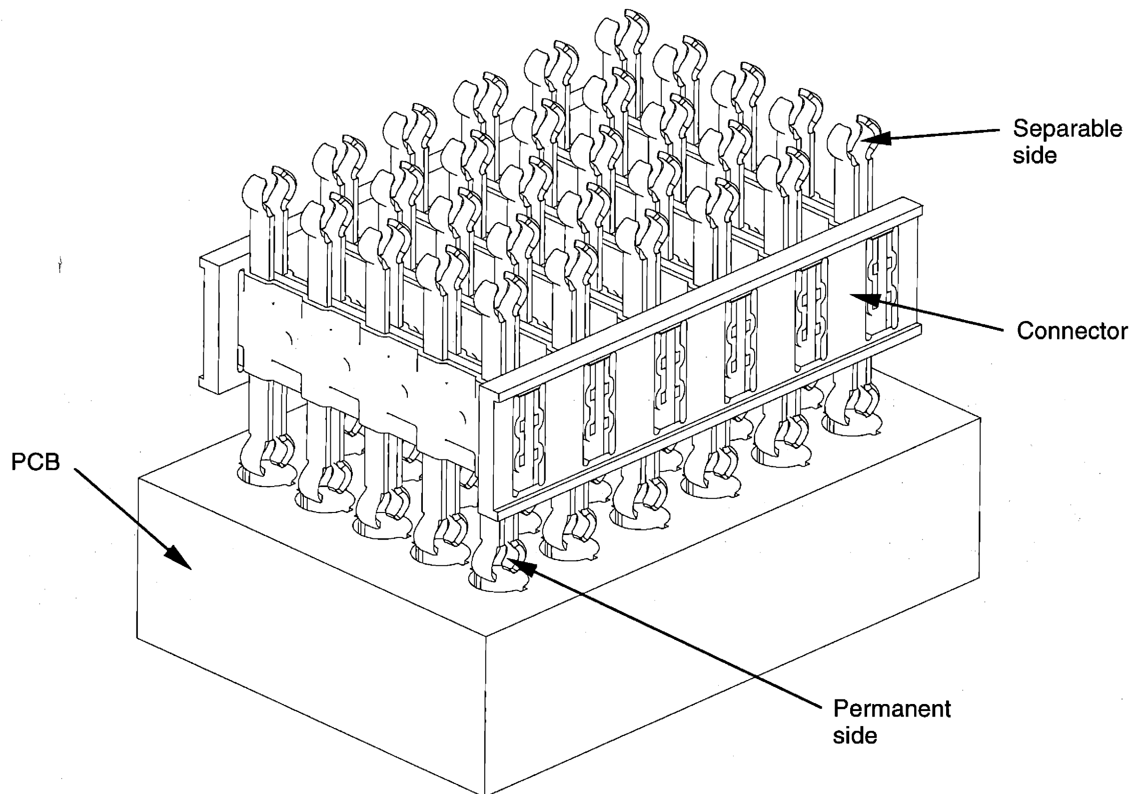

Figure 8-1: Two-contact pair single piece connector

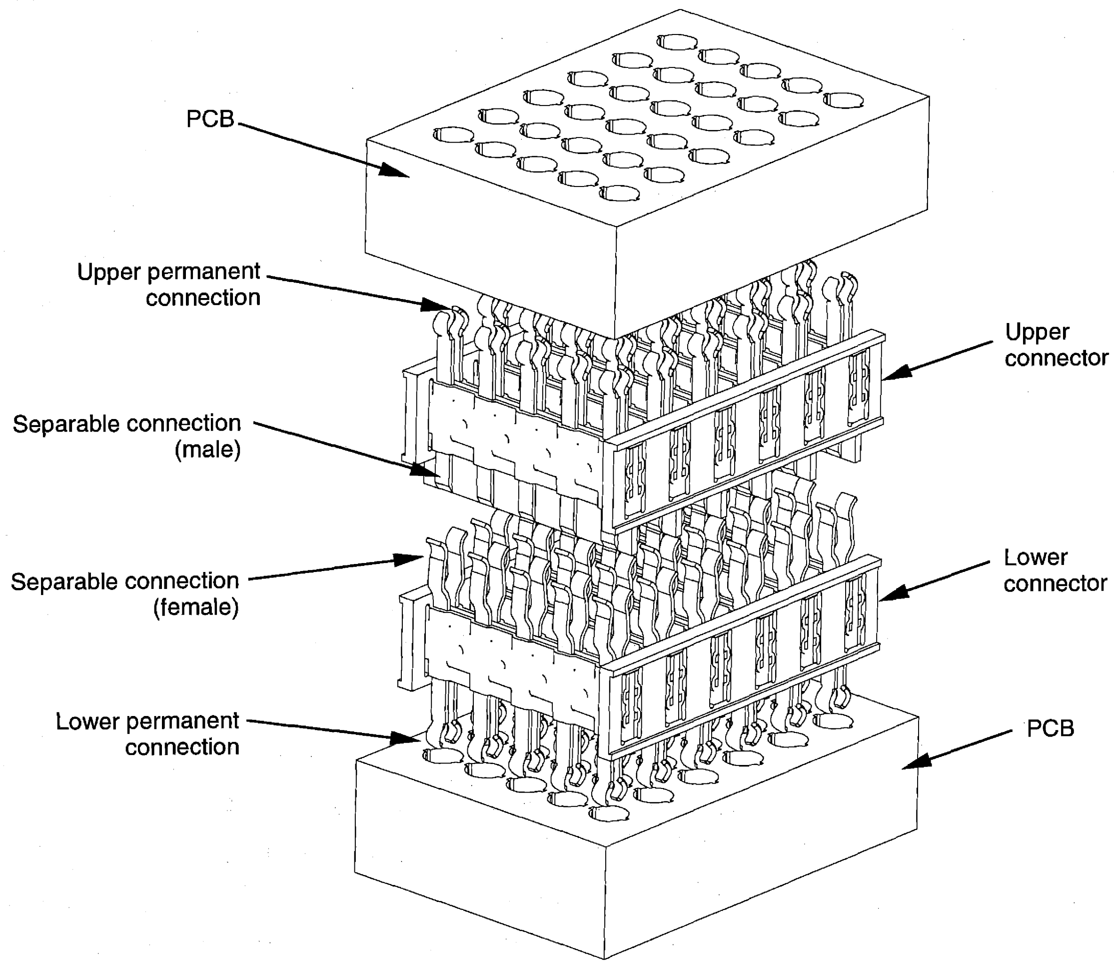

Figure 8-2: Two contact pair split-hole separable connector.

To address the need for a ground drain in the differential pair, the modular design of Figure 8-3 allows for three contact differential modules. This creates a differential pair without the crosstalk issues of the previous design. The modularity of the design allows for the mixing of differential and single-ended signals along with power and ground. Each insert-molded module snaps into the carrier in any desired pattern. While this design is embodied as a single piece connector, a two-piece design that incorporates a separable interface is possible.

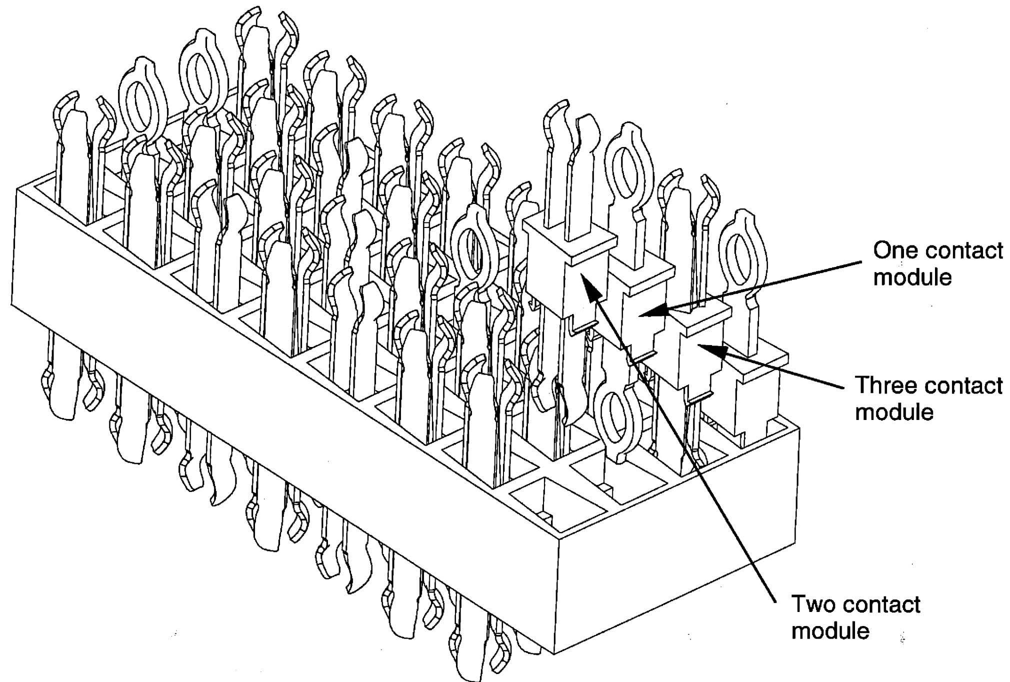

Figure 8-3: Modular connector with one-, two- and three-contact parallel-board connectors.

Adding a fourth contact to each connection set, as shown in Figure 8-4, results in design symmetry that fosters manufacturability. The four-contact design supports either dual single-ended signals or a differential signal by providing two ground segments and contacts per set. This design also adds a protective guide to the separable side of this one-piece connector, which minimizes contact damage during handling.

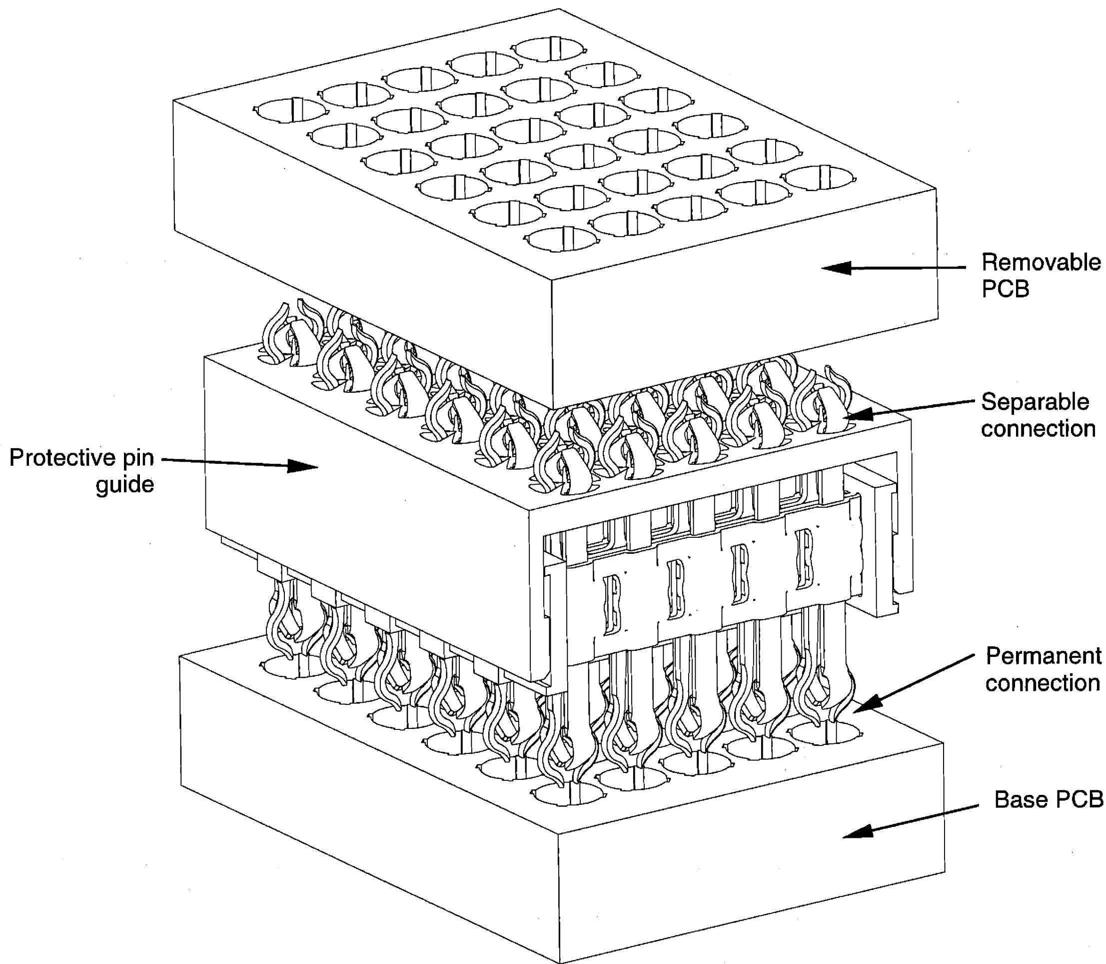

Figure 8-4: Two-pair parallel-board connector.

8.1.2 Right-angle connector concepts

The right-angle backplane/daughter card configuration employed by most large-scale digital systems allows for high volumetric density and ease of service in the cabinet. Connectors that support these systems require high performance and mechanical robustness. Applying a multi-connection via launch to a right-angle connector, as shown in Figure 8-5, puts the separable interface in the backplane vias. For many system designers, robustness and repair concerns will override the added cost of a two-piece derivative, like the one shown in Figure 8-6. As with the parallel board concepts, two contacts per via offer the best configuration for single-ended signals. A right-angle differential connector with three contacts per via lacks manufacturing feasibility. Adding separate ground contacts with their own vias intermittently between signal pairs provides the required drain, thus allowing for a differential design.

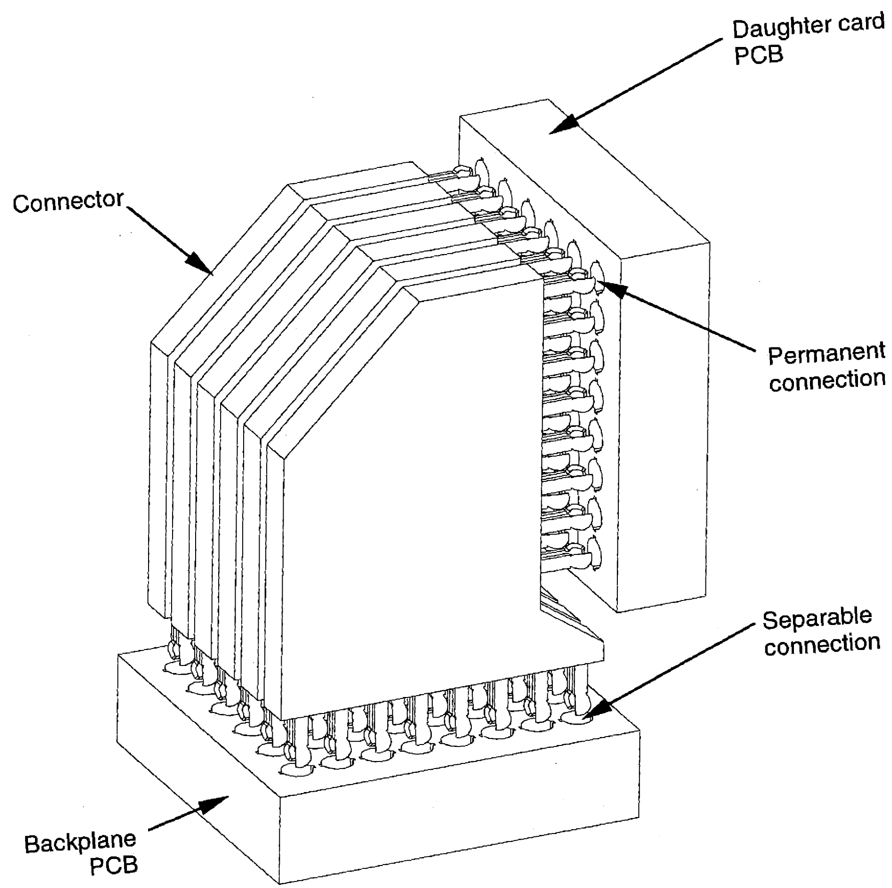

Figure 8-5: Two-contact right-angle single piece connector.

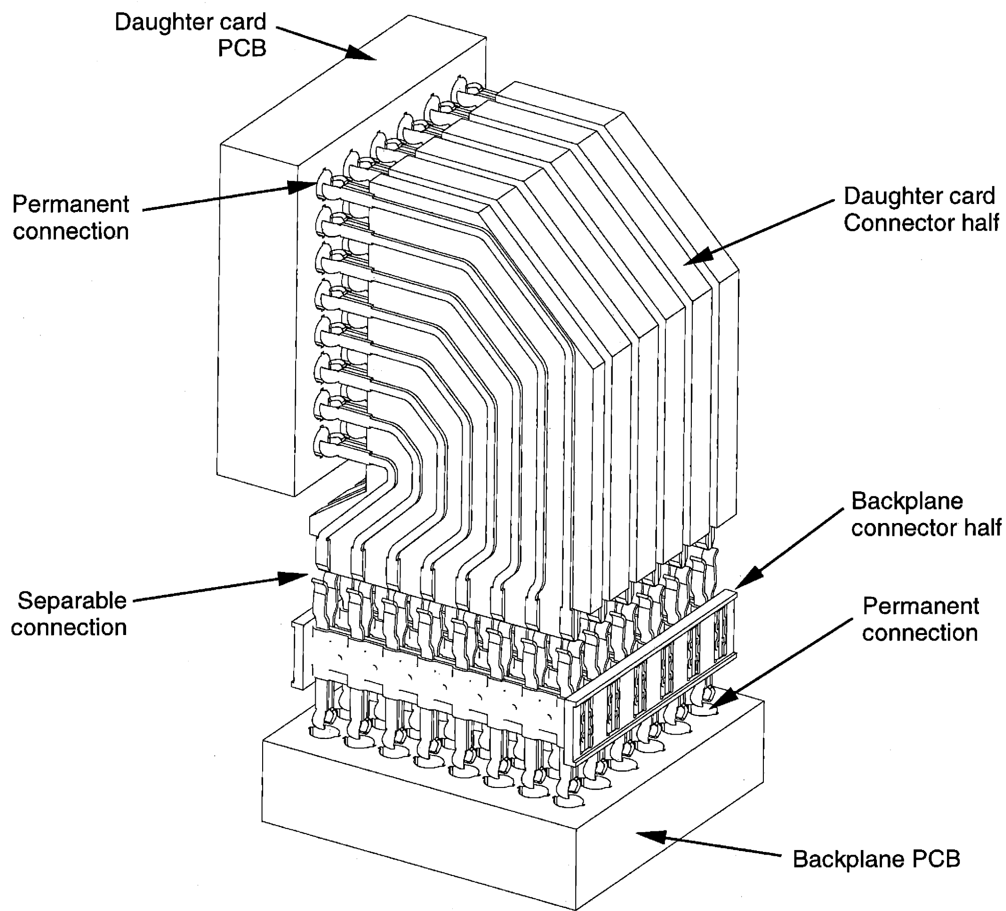

Figure 8-6: Two-contact right angle separable connector (with exposed internals).

The concepts presented for both right-angle and parallel-board connectors only touch the surface of connector design employing multi-connection vias. They also reveal problems that need resolution before commercialization, including but not limited to the following.

- A mechanism must be designed to protect the fragile contacts during handling.
- The development of a two point of contact design is needed. Because, two points of contact are required for many connector designs, all the designs presented herein connect to the via with only one contact point per connection.
- A design that prevents the contact leads from touching each other during insertion.

Addressing these and other problems in the connector design details requires a great deal of design and experimentation, well beyond the range of this research.

8.1.3 Pogo pins

Pogo or spring pins, shown in Figure 8-8, find use in both PCB and semiconductor testing applications. In PCB test, pin arrays ("bed of nails") provide connections to vias and pads for pre-assembly board testing. Semiconductor test heads rely on the ability to connect tester probe-cards to channel cards, requiring high cycle, density and performance connection which spring pin contacts provide. These spring-loaded pins contact the test board on gold-plated pads. In the case of semiconductor tests, both frequency and density push the limits of this technology, [Chiu]. Because semiconductor testers check devices, the electronics in the testers run at the device frequencies, which are significantly higher than the typical PCB speeds discussed in Chapter 3.

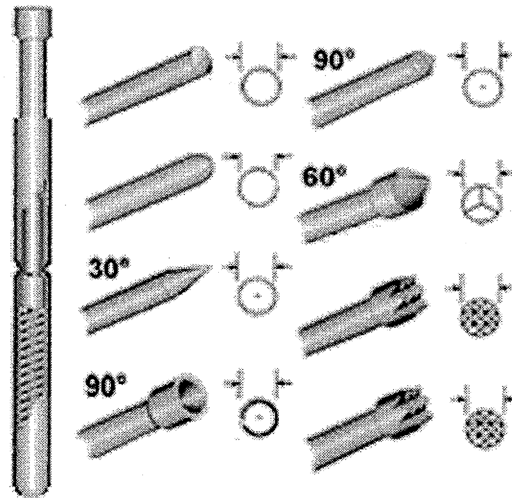

Figure 8-7: Spring pogo pin with various tip styles.

Applying the benefits of multi-connection vias to the design of pogo pins expands the system performance envelope. The two-contact configuration shown in Figure 8-8 functions as a co-axial launch. This arrangement offers superior impedance control over the pad and via geometry of conventional pogo pins, because the connection is impedance matched all the way to the via, where as conventional pogo pins have a mismatch at the board launch.

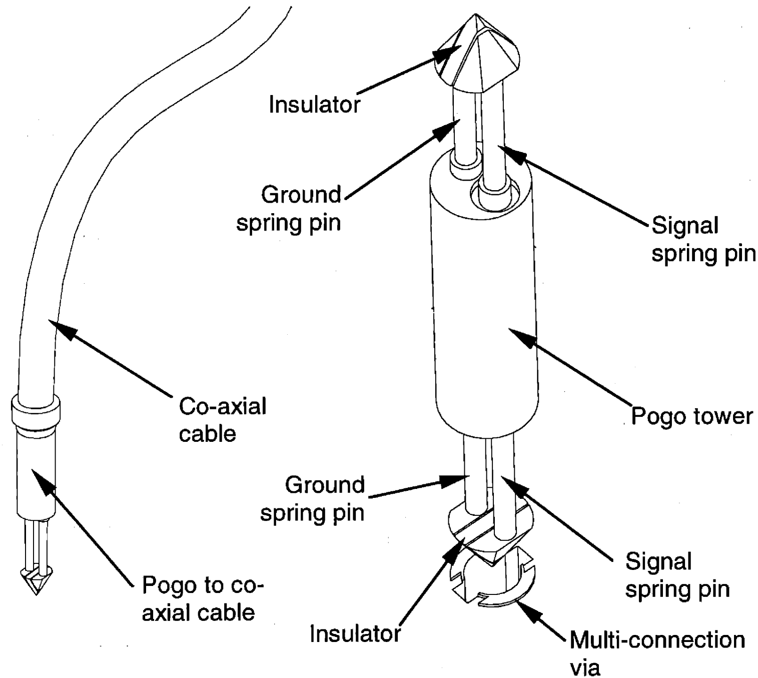

Figure 8-8: Multi-connection via spring pogo pin tower and co-axial cable.

Beyond signal performance and density requirements, the testing of PCBs, which employ multi-connection vias, necessitates the development of these designs.

8.1.4 PCB test probes

Co-axial cable connections to PCBs offer another potential application for multi-connection vias. These SMA, SMB and SMC (Sub-Miniature A, B and C) connectors, see Figure 8-9, find applications in RF circuits and high-performance PCB tests. For testing devices, the device under test (DUT) attaches to the PCB traces that connect to these coaxial launches. For many testing applications, such as the ones in this thesis, the DUT has better performance than this connector does. This performance degradation is the same as for any connector to the PCB, i.e. the impedance mismatch in the connection to inner traces relying on conventional vias. This research has shown the possibility of achieving launches with virtually no reflection using multi-connection vias. Thus, Figure 8-10 illustrates one potential design solution, where pressure contacts provide connection to each side of the via. The splits in the via align with features on the connector to guarantee orientation.

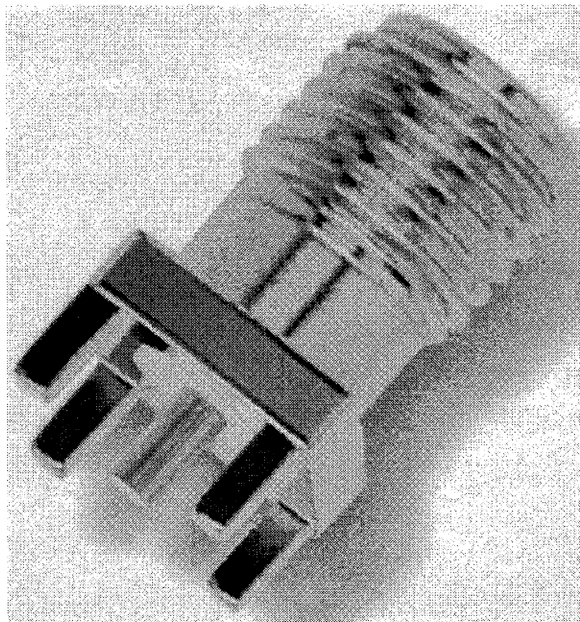

Figure 8-9: SMA.

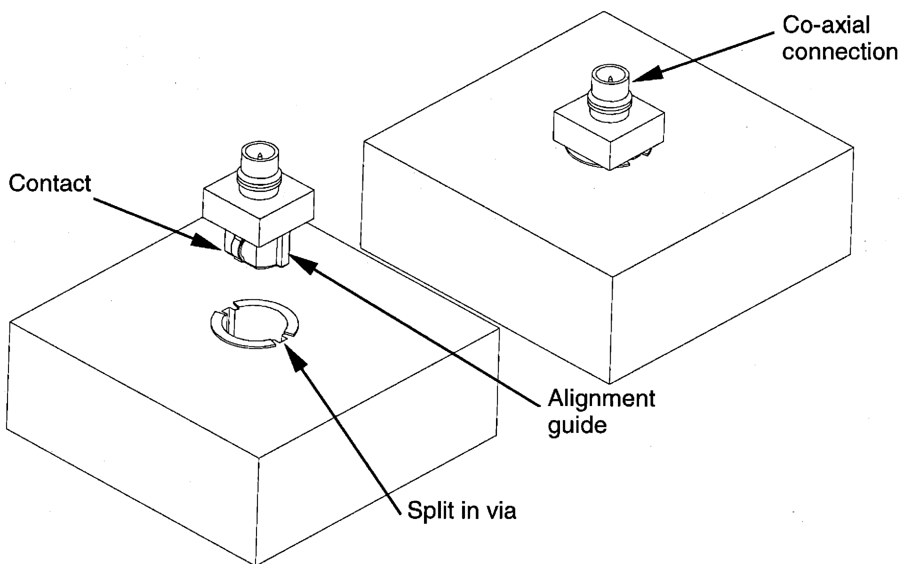

Figure 8-10: Split-via coaxial connector launch.

8.2 Bypass capacitors

The typical power portion of a high-speed electric circuit requires a power-to-ground plane design that both distributes power to all logic devices and provides stable reference voltage for digital signals. Bypass capacitors filter out noise from this circuit. Typically, designers use a rule of one bypass capacitor for every power input to a device. SMT-type devices represent the majority of bypass capacitors used. Lead inductance causes the effectiveness of bypass

capacitors to drop off at higher frequencies [Johnson and Graham]. The frequency at which inductance begins to dominate is given by:

$$F_{bp} = \frac{X_{\max}}{2\pi L_{C2}} \tag{8-1}$$

Where: X_{max} = maximum impedance, in Ω's.
L_{C2} = series lead inductance in Henry's.

Figure 8-11 shows a typical SMT bypass capacitor with routing structure. The lead length from the power and ground planes determines the lead inductance. The shorter the lead, the lower the inductance will be, and consequently, the higher the frequency of operation. In the following sections, multi-connection vias are applied to this problem in several different ways.

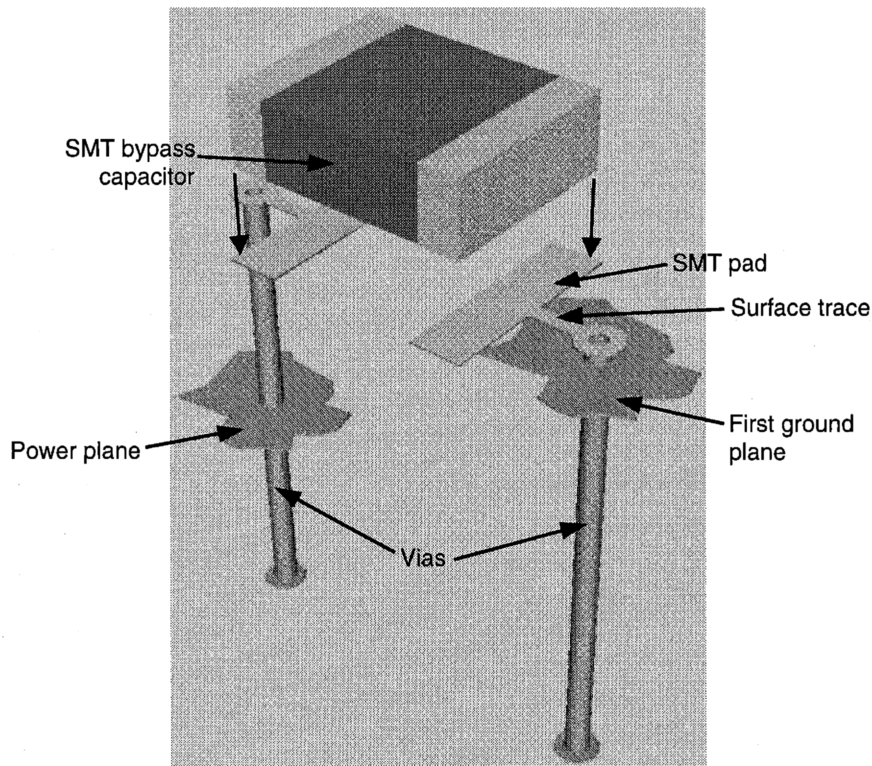

Figure 8-11: SMT bypass capacitor with surface traces and routing vias.

8.2.1 SMT capacitor routing

The most direct application of multi-connection vias to the bypass capacitor does not change the design of the SMT package, but utilizes the new via geometry for routing only. Placing the via directly below the device, as shown in Figure 8-12, reduces the inductance loop to only the surface trace. Because the via itself offers an impedance-controlled structure, the inductance

caused by the conventional via configuration does not apply. Approaching the problem in this manner offers a superior solution than using micro-vias because power planes most often locate in the middle of the PCB, where micro vias cannot easily reach.

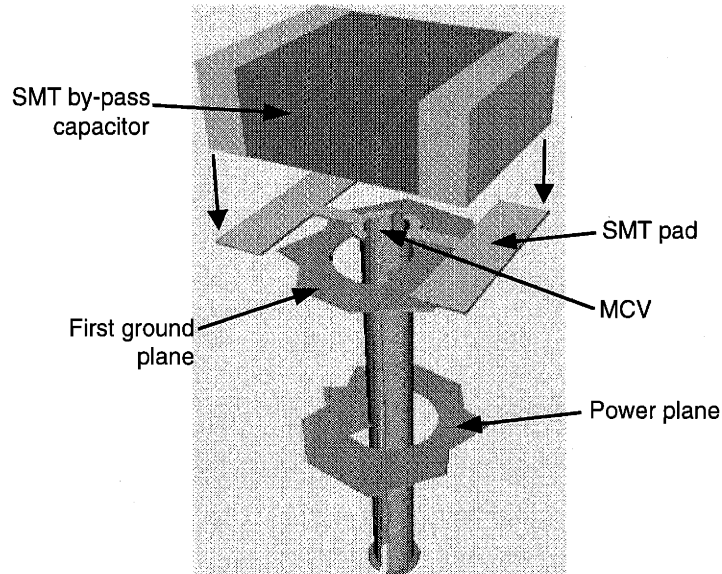

Figure 8-12: Bypass cap with multi-connection via for routing.

8.2.2 Via-mount technology (VMT) capacitor

The next level of approach to the bypass capacitor problem involves placing the device directly inside the via, which creates a whole new class of VMT devices analogous to SMT. This new class eliminates surface traces altogether and reduces lead inductance significantly. Figure 8-13 shows the proposed device and installation. Tabs on the body of the capacitor mesh with the broached split to provide orientation. Contacts on the side of the capacitor function like press-fit connectors. This setup does not preclude creating a design with soldered connections.

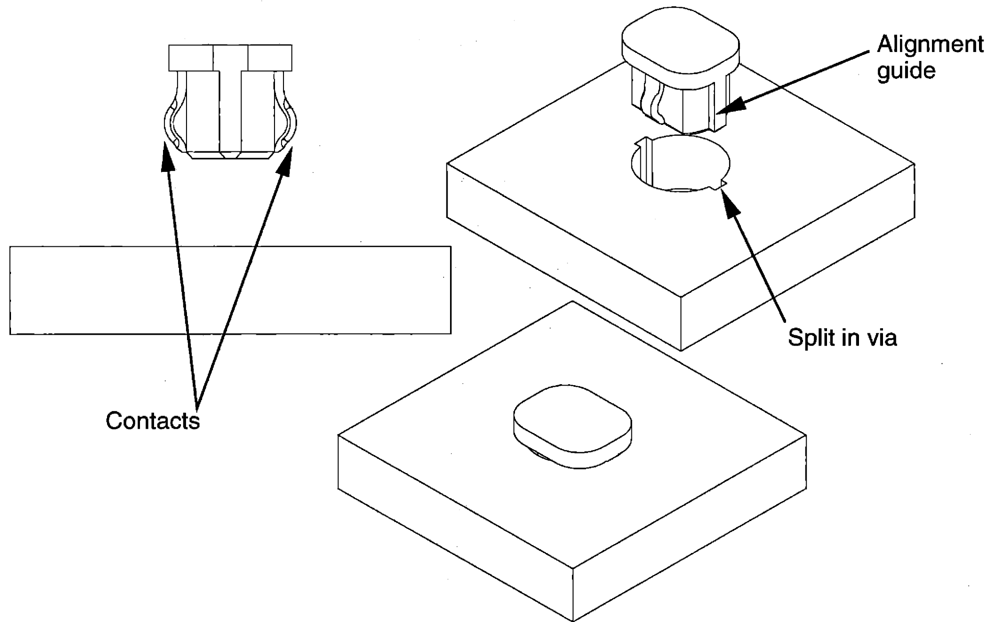

Figure 8-13: VMT bypass capacitor.

Lenkisch proposes a similar device in which two vias are connected by milling a slot between them, [Lenkisch]. Solder provides the connecting mechanism between the device and the via. From a signal performance standpoint, this design offers the same performance benefits of the VMT capacitor.

8.2.3 Via based capacitor

For the final bypass-capacitor concept, consider a multi-connection via as a capacitor by itself. By connecting one side to power and the other to ground the via functions effectively as a two plate capacitor. As a first order estimate of its effectiveness, consider only the area at the split as a parallel plate capacitor, shown in Figure 8-14. Capacitance for a pair of plates is ([Giancoli]):

$$C = K\varepsilon_0 \frac{Area}{gap} = K\varepsilon_0 \frac{2t_p h}{gap} \qquad (8\text{-}2)$$

where: K = dielectric constant

$$\varepsilon_0 = 8.85 \cdot 10^{-12} \frac{C^2}{Nm}$$

Unfortunately, the area is very small, and depending on the splitting process, the gap is relatively large. At the same time integrating the device into the PCB directly, the inductance problems of the SMT device do not apply.

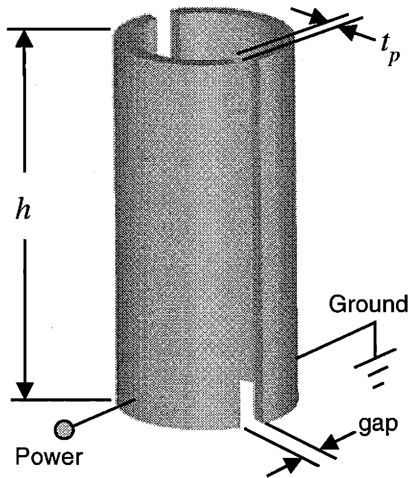

Figure 8-14: Single split-via bypass capacitor.

Since air has a very low dielectric constant (1.006), potting the via with a high dielectric constant material improves the capacitance proportionally. Some capacitors use materials with dielectric constants ranging from 1000 to 10000 [Johnson and Graham]. Applying some of these materials inside the via yields the capacitance values shown in Figure 8-15. Even with the thicker PCB, a high dielectric constant and narrow gaps (t_w) render low capacitance values. Most bypass capacitors function in the 10-to-1000μF range, putting these designs off by several orders of magnitude. Completely discounting further development, however, neglects potential gains from more splits per via, higher dielectric constant materials, smaller split gaps, and un-modeled capacitive benefits. Therefore, the potential cost savings and lower inductance benefits warrant consideration of this technology beyond this thesis.

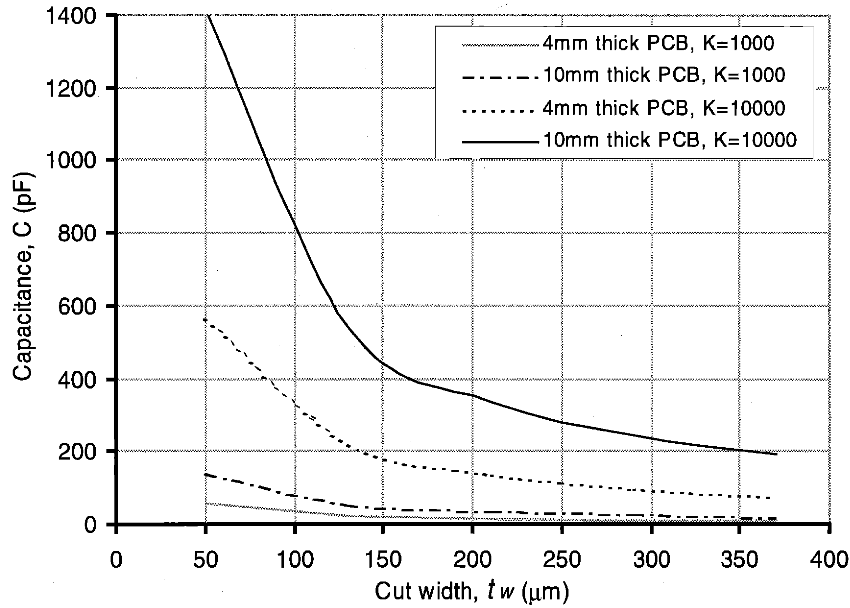

Figure 8-15: Multi-connection via capacitor model assuming one split and 40μm plating.

8.3 Integrated circuit device VMT

Applying the VMT to higher IO (input/output) devices, as shown in Figure 8-16, takes the VMT to another level. In this design, both vertical and horizontal plating separations create a large number of connections. The design shows multiple ICs in a single package. A single chip design offers another permutation by allowing for a higher number of connections per device. Depending on the manufacturing technology employed, non-round vias (most likely rectangular) may integrate better with the chip IO. The benefits of this type of configuration include improved launch performance, low profile, and density. The design challenges include heat management, device-to-contact connection and general acceptance.

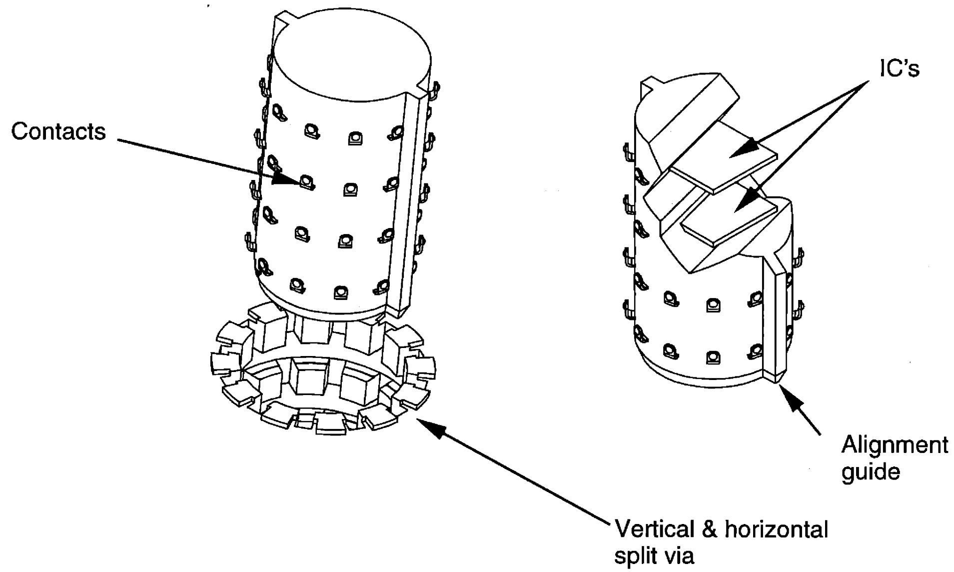

Figure 8-16: VMT IC package.

8.4 Summary

This chapter explores some key areas of the design space created by multi-connection vias and launch. The investigation intends to explore different design opportunities on a purely conceptual level. Consequently, the designs do not necessarily imply commercially-viable products. Concepts proposed range from connector designs, to VMT devices inserted into the PCB, to a fully integrated bypass capacitor design.

9 Production roadmap and research opportunities

To the casual observer, adding a simple new feature to the via of the PCB does not add significant complexity to the design and manufacture of the board. Design changes to the pad do not stretch beyond the capabilities of current lithography processing. Therefore, the only addition is a simple hole-splitting machine that adds a step to the end of the process, without really disrupting it. However, there are many more opportunities and challenges that have to be met before this technology can be made widely available. The intention of this chapter is to present these opportunities and challenges, and provide a basic roadmap to establishing the commercial viability of multi-connection vias.

The map starts at the via design, moves through the process of via manufacturing, and finally to board testing (see Figure 9-1). The coverage of via manufacturing goes beyond those processes developed for experimental work in Section 3.2. The first topic considered is the design of the via section itself.

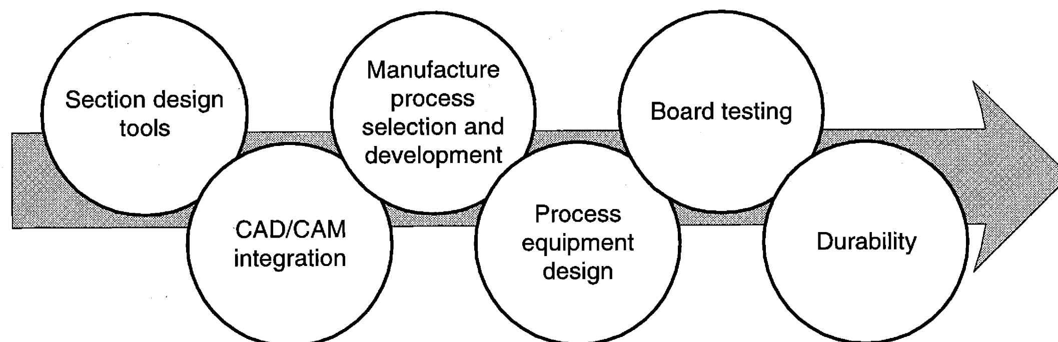

Figure 9-1: Production roadmap.

9.1 Design tool

Before using multi-connection vias, the board designer needs to know what geometry will provide the least reflection and the best transmission, while minimizing the via EMI inside the board. Section 6.1 develops the via section design based on the simulation and experimental experience of this research. To select the design parameters that provide optimum signal performance without trial and error for individual cases, the designer needs a design tool based on the signal physics.

The first-order solution to the impedance problem, presented in Section 6.1, takes the co-planer waveguide formulas and assumes the radius is large for both single-ended and differential signals, see Figure 9-2 and Figure 9-3. While it may prove feasible to develop a closed-form solution that solves this structure's impedance, a numerical solution to the 2-D problem can provide a very fast, flexible solution.

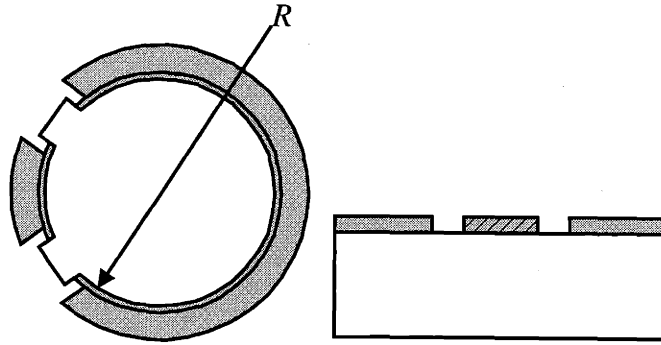

Figure 9-2: Single-ended co-cylindrical and co-planer waveguides.

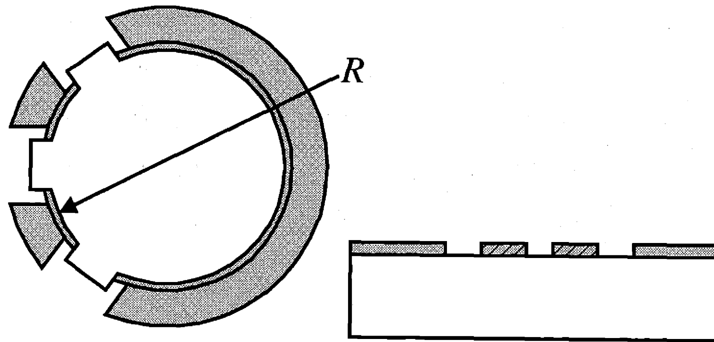

Figure 9-3: Differential co-cylindrical and co-planer waveguides.

Because of the lumped affects of the transition, matching impedance does not always provide the lowest reflection. The section solution, also, does not take into account the ground plane structure. Considering these structures, in the model, more properly characterizes the performance. The overall geometry in three dimensions is too complex to contemplate, at this point, a closed form solution where the desired outcome is a relation for input impedance:

$$Z = f(d_f, T_p, T_w, X_g, X_p, \varepsilon_{r,board}, \varepsilon_{r,via}) \quad (9\text{-}1)$$

where: d_f = finished diameter
T_p = plating thickness
T_w = the gap
X_g = clearance in the ground plane
X_p = ground plane spacing

$\varepsilon_{r,board}$ = dielectric constant of the PCB

$\varepsilon_{r,board}$ = dielectric constant inside the via

A full-wave solution using finite element methods can deal with this problem. This type of simulation, however, does not provide a good design tool. It requires substantial computational power to solve the problem, and more importantly, its solution cannot be factored for the design variable required (i.e., cannot be optimized for a particular impedance). Using simulation to develop equations that fit the data within a given range requires many simulations. The results, however, yield formulas that solve each case quickly. Integrating these formulas into the CAD tools used for board design is critical to the success of multi-connection vias.

Another application for these formulas lies in integration with the board manufacturing process. Sampling the fabricated boards for critical dimensions that are difficult to precisely control, obtains information required for more accurate impedance matching. In fact, board manufactures, currently, compensate the laminate thickness to dial-in the desired impedance due to variations in the line widths after etching. This compensation changes the ground plane spacing. These samples can also provide the finished hole-size and the plating thickness in the via. Using this information, the processing equipment can compensate the multi-connection via gap and signal arc-length parameters.

9.2 CAD/CAM integration

The design tools proposed above provide the CAD tool with information required to layout the via. The pad and ground plane design follows the section at each layer intersection. The trace direction determines the orientation of the via segment. At the same time, the traces require routing with the special orientation needs of multi-connection vias.

Current CAD software is not prepared to meet these geometry requirements, nor are specialized pad stacks available with most design packages, see Figure 9-4. IVT configurations pose an even greater challenge to CAD software. Routing multiple traces and grounds to the same via often violates design rules enforced by the CAD system. CAD software development needs to address these deficiencies.

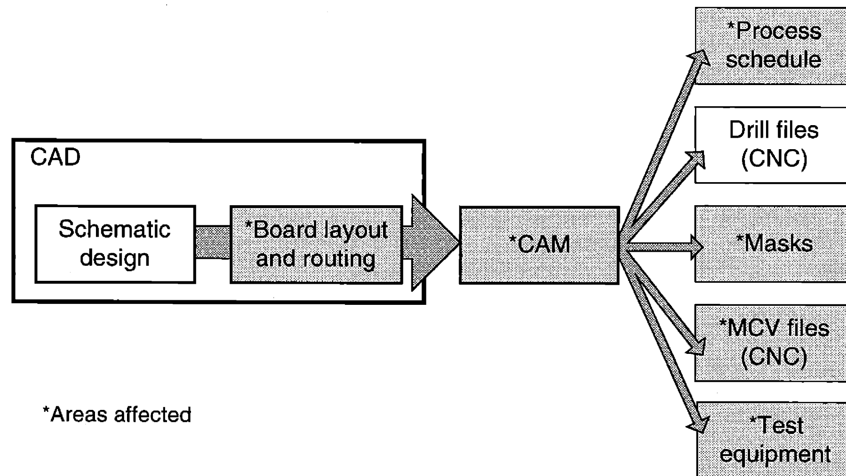

Figure 9-4: Changes to CAD/CAM.

Auto-routing these new vias represents the most important part of the PCB layout software. Algorithms tied into the design schematic automatically route traces. They use the design rules to determine how to run traces and were to put vias. While often requiring significant intervention from the designer, auto-routing has become an indispensable tool; without it, PCB routing using this new technology becomes prohibitively complex.

CAD systems typically define the desired geometry on each layer and the size of the plated-through hole. This functionality would have to be extended to include geometry information on the inside of the hole. In addition to the drill diameter, the CAM package must handle the in-via geometry generation, and generate NC data to drive the new production equipment according to process requirements.

In summary, the viability of multi-connection vias as a PCB feature lies in the ability to design them into the layout. The CAD software currently used to layout PCB designs must be modified to work with these vias. The routing tools need to assist in the uniquely complex task of making the vertical traces. Finally, the CAM software output must integrate with the hole-splitting production equipment as well as other affected downstream processes.

9.3 Developing the manufacturing process

Resource and scope limitations reduced the processes explored up to an experimental level to those that provided the path of least resistance. The implementation of a manual broaching machine and development of cutter designs provided acceptable levels of resources and scaling for electrical experimentation. In addition, access to wire EDM equipment provided an

opportunity to do some simple experimentation with this process. Both processes require significant development before commercialization.

Ultimately the process selected for production must consider other possible options and accommodate customizations. This section explores some candidate processes configured to work within the constraints of multi-connection vias.

9.3.1 Broach tool design

The development of broaching for this thesis discussed in Section 5.1, focused primarily on prototype tools. Looking toward future production, the broach tool design requires further consideration. As a consumable in the multi-connection via manufacturing process, the tool contributes significantly to the overall process cost. Broach tool manufacturing must take advantage of potential production volumes, while supporting diverse configurations.

Broach tool design requires careful consideration of all the design parameters and tool manufacturing processes. The main variables include hole diameter, cut width, plating thickness and cut depth. Design models can be developed to optimize tooth profiles for each configuration case. Optimization will help meet the functional requirements of smaller holes and higher aspect ratios, while maintaining tool robustness. Models and experiments from this research provide a starting point for the tooth profile design, but do not offer the complete optimization attainable through large-scale experimentation.

The tool manufacturing process, also, presents limits to the tool profile. Some of the process options include grinding, wire EDM, and powder metallurgy (PM). The process selection requires flexibility to accommodate the main design variables while keeping the economics in mind. For example, the tooling costs of PM may outweigh the potential production volumes and lower per-tool cost. Another important conclusion derived from experiments suggests the quality of the cutting edge factors greatly in the tool performance. Consequently, adding a final grinding step and applying low friction tool coatings improves performance.

Process selection depends on the answer to the important question of whether to use a monolithic or an inserted tool design. Inserted tools have the advantage of placing the hardest and most expensive material, such as carbide or ceramic, only at the cutting edge. On the other hand, monolithic tools, similar to the one shown in Figure 9-5, have the potential of scaling to smaller diameter higher aspect ratio vias.

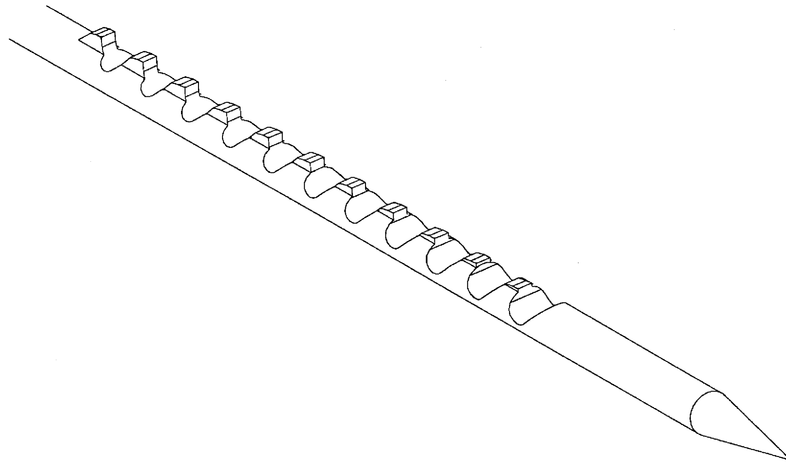

Figure 9-5: One sided broach monolithic tool.

Selection and development of the broach manufacturing process requires consideration of all functional needs for both the tool design and the process. Flexibility and cost represent the primary drivers.

9.3.2 EDM

One of the most promising processes for manufacturing multi-connection vias is EDM. Currently, it is feasible to make small quantities of multi-connection vias using standard EDM equipment. This section builds on the experimental work conducted in Section 5.2 to explore EDM development for the special requirements of multi-connection vias. Full production necessitates modifications to the process.

Typical wire EDM equipment reliably provides for the "threading" of wire through starter holes. First, the exact via center is found using a vision or mechanical centering system, as discussed in Section 9.4.1. The wire is annealed, stretched and broken on the fly, creating a straight tapered start. The straightened wire goes through the starter hole guided by water jets.

For multi-connection vias, some sort of a grounding mechanism, such as the clamps shown in Figure 9-6, provides ground to each via during processing. This is typically not a problem in cutting blocks of metal, because the conductivity of the entire work-piece allows for one grounding connection. In the case of the PC board, however, most vias do not connect to a common ground. In addition to grounding, the conductive clamp assists in guiding the wire during threading, thereby speeding up this process. The machine tool design incorporates interchangeable top and bottom clamping tools to deal with the varying via diameters. Once

through the hole and clamp, the take-up pulleys (B) grab the wire. As with conventional wire EDM, the wire stays straight due to tension.

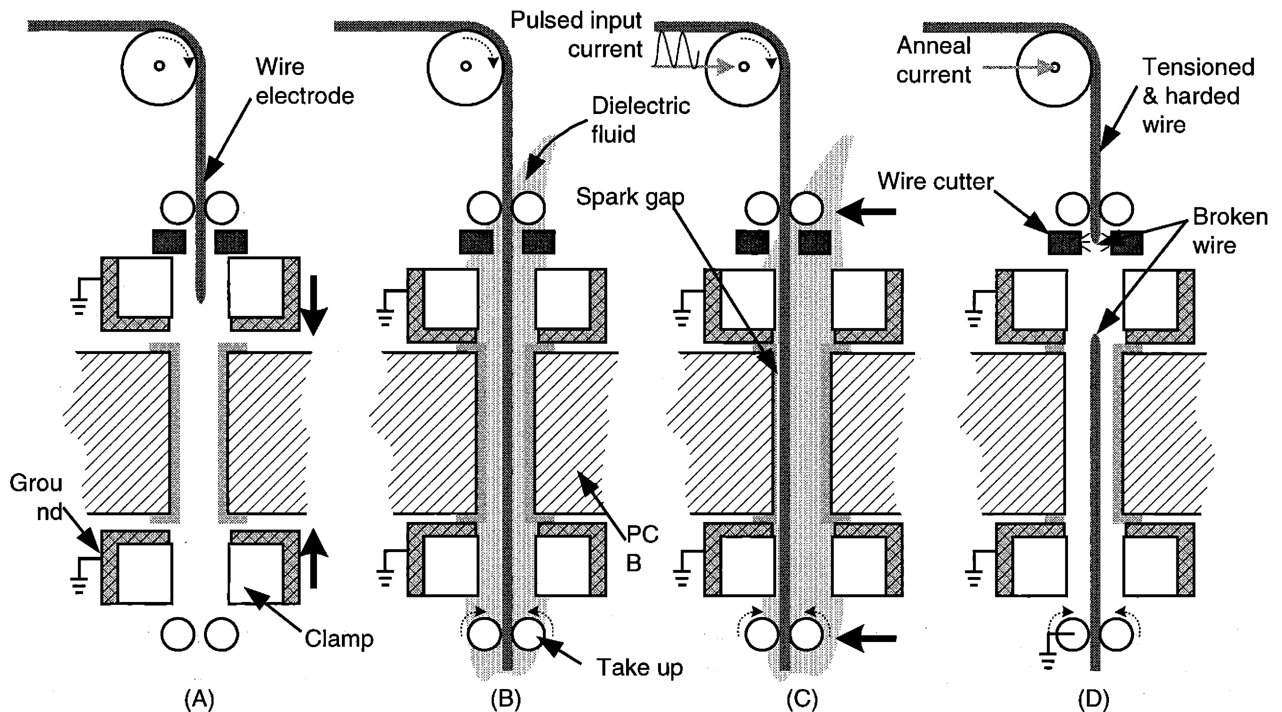

Figure 9-6: Modified wired EDM process.

Once the wire is held on both sides, an input current is applied and the via barrel is burned in the desired direction (C). During this time, dielectric fluid flows through the via hole. After cutting that via, the wire is broken and removed from the hole. While an annealing current is passing from the lower pulley to the upper pulley, the wire is broken above the clamp (D). This process straightens the wire between the cut point and the upper pulley to facilitate threading of the next via. This threading time takes as long as one minute for commercial-wire EDM machines. The threading time, combined with the cutting and indexing times, determine the per-via rate, which represents the main cost factor.

The nature of the PC board may require non-conventional approaches to optimize the rate. A possible approach is illustrated in Figure 9-7. Once the via is clamped and grounded (A), the rotating electrode drives through the plating (B) until the plating is eroded away (C). The electrode then retracts. Because both the work-piece and electrode erode, the end of the electrode tapers, requiring it to extend further with each pass. Providing a wire-straightening

system permits the use of spooled wire electrode stock, instead of requiring electrodes in precut rod form.

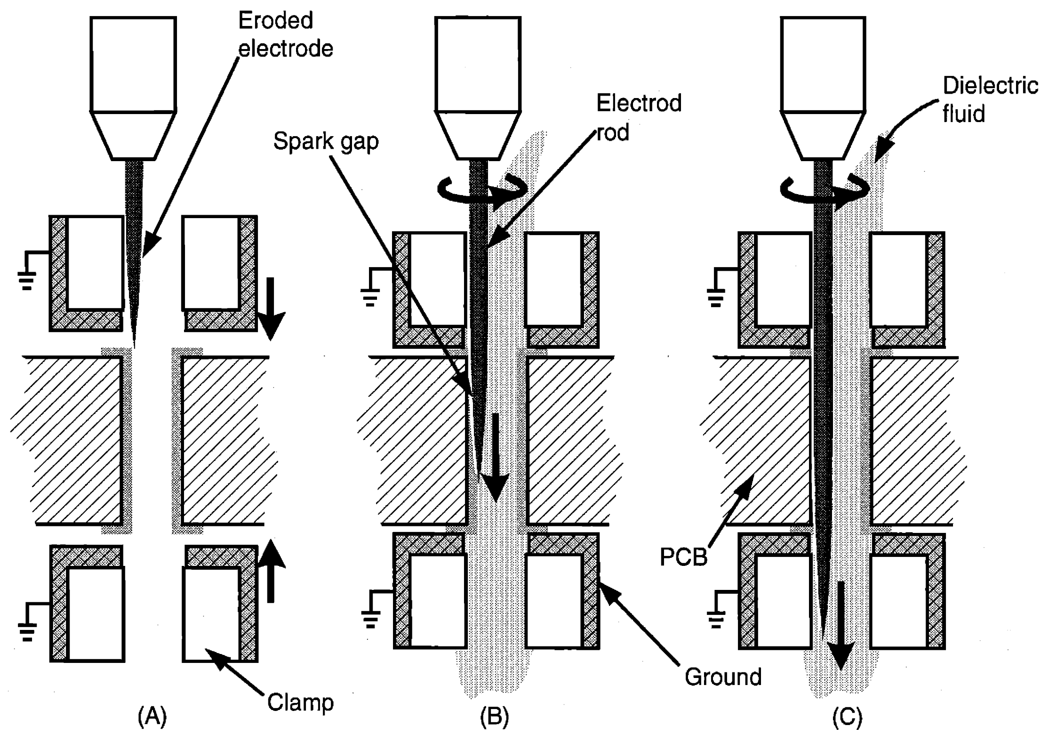

Figure 9-7: Wire rod EDM process.

Both of these types of wire EDM systems limit the via geometry to vertical conductor strips. Delivering electrode and dielectric to a point location inside the via barrel plating removes conductor only in the selected regions. The process concept shown in Figure 9-8 allows for the manufacture of IVTs, such as those shown in Figure 6-12. Inside the via, the ceramic guide directs the arc to a point and etches cylindrical traces in only the regions desired. Like the previous concept, grounding clamp blocks provide the via ground connection. The electrode material must be soft enough to permit the sharp bend required for smaller vias, which ultimately limits the process to relatively large holes. The cutting time can suffer, because the material removal rate is a function of the energy density and the arc area is limited to the area at the end of the wire. At the same time, the total volume of material removed decreases when compare to complete vertical separations. In addition, the change over time between vias reduces.

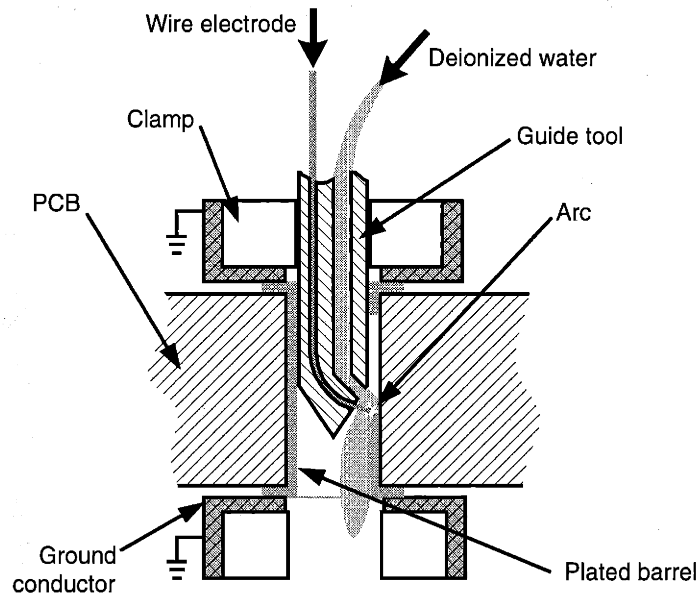

Figure 9-8: Selective EDM or EDM milling.

One problem with using EDM to remove plating on fiberglass surfaces is the un-machined material (Figure 9-9). The epoxy etch-back process used after drilling the via compounds this problem, because it increases roughness on the via walls. Assuming the electrode has a long enough dwell period and the spark gap is large enough, the electrical connection will break between segments. With the selective EDM process described above, the focused material removal leaves less residual copper. The bits of metal left in the dielectric change the signal characteristics. One solution to this problem inserts the splitting process before the copper etch-back step (after step shown in Figure A-9) so the residual copper etches away.

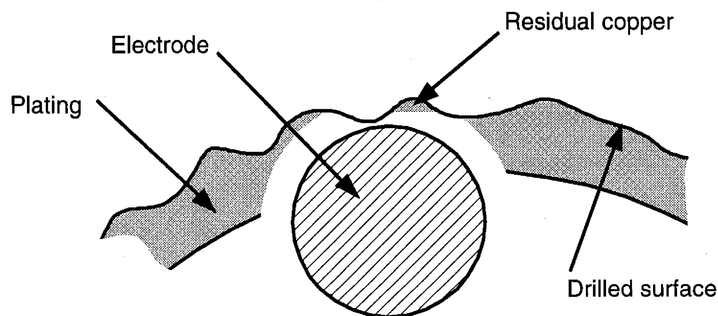

Figure 9-9: Residual copper in surface roughness.

Aside from chemical etching processes (Section 9.3.3), EDM manufacture of multi-connection vias provides the unique benefit of removing just the conductor material, thereby preserving the

fiber/resin dielectric. The benefits include: reduced routing keep-out zones, eliminated crack propagation, reduced potential copper migration, and reduced moisture absorption. After overcoming both the residual copper and rate issues, EDM provides a very flexible and scalable manufacturing option.

9.3.3 Chemical etching

Multi-connection via etching requires features in the etch resist on the inside surfaces of the via barrel. Some advantages may be gained by integrating steps to prepare the vias for copper etching into the PCB manufacturing process. The primary advantage may be the elimination of epoxy/fiber damage. However, potential problems include process chemical seepage into fiber walls and handling PCB surfaces during fragile stages. For a general overview of the PCB manufacturing process, refer to Appendix A.

Cutting the etch resist, as shown in Figure 9-10, separates the individual conductor elements by etching away the copper in the cut areas. Cutting or breaking the etch resist employs any of the same processes proposed/developed for cutting the entire barrel. By cutting just the etch resist, however, no fiberglass is disrupted. For example, using a broach to cut just past the etch resist and barely enter the copper plating. For EDM, this process provides the added benefit of etching away the residual copper in the surface roughness.

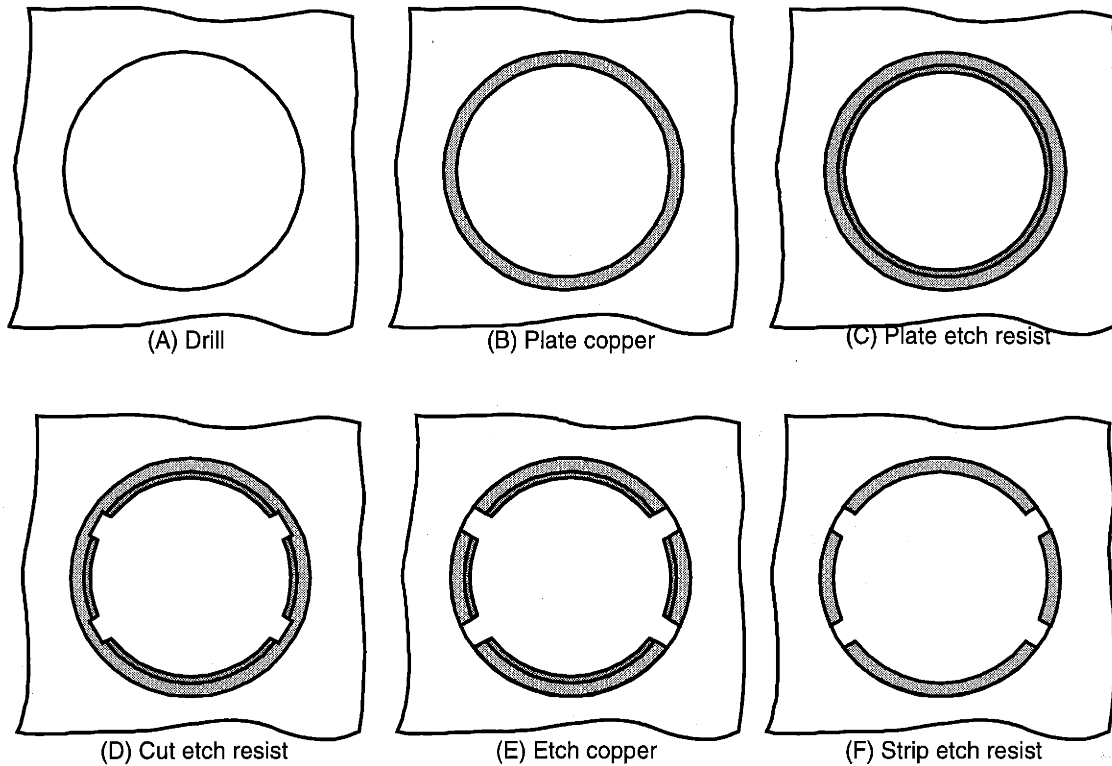

Figure 9-10: Process steps for etched via separations.

As shown in Figure 9-11, another option at this point in the process is to force an etch resist polymer material through a die, creating small passageways along the via surface. These passageways permit the etch chemicals to remove the copper in that region. The etch resistant polymer selected has a low melting point to enable polymer removal with relatively low temperatures.

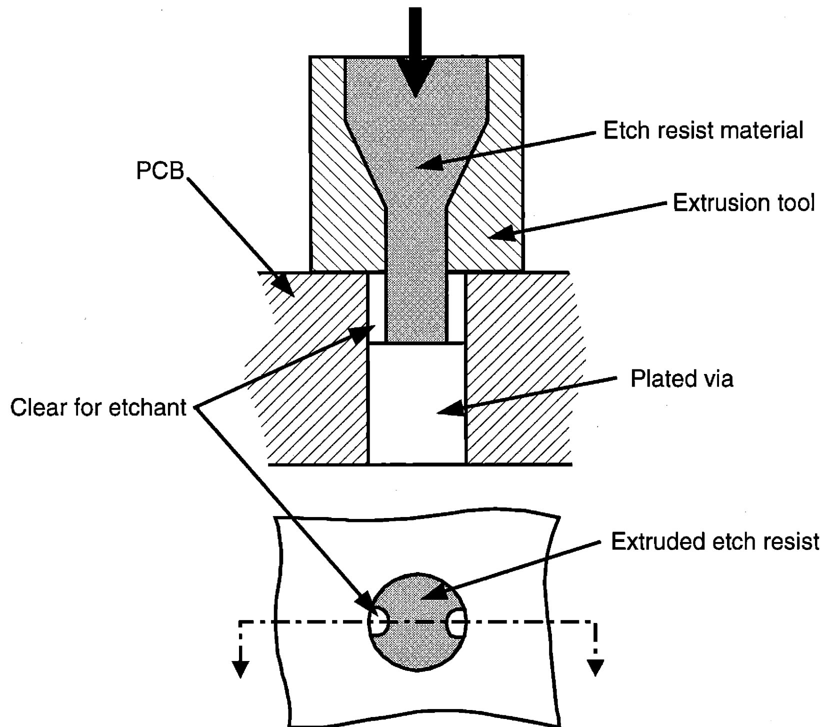

Figure 9-11: Extruded in-via etch resist mask.

A variation on this theme places prefabricated plugs in the via prior to etching. The plugs are recycled or reused after the process. They are taller than the hole, and thereby able to process different thickness boards. Because both concepts restrict the passageway through which the etching chemicals flow, the relative size of the via is large.

Moving further up in the PCB fabrication process just before the copper electroplate step provides an inverse opportunity. Using inkjet technologies, like the spray nozzle shown in Figure 9-12, to travel inside the via, precise marks can be made on the areas to be etched. Because of the polymer-based chemistry of the plating resist, the process can derive directly from inkjet technology. After several steps, the treated areas become copper barrel separations. This type of process offers the flexibility required to create the in-via traces described in Section 6.3.

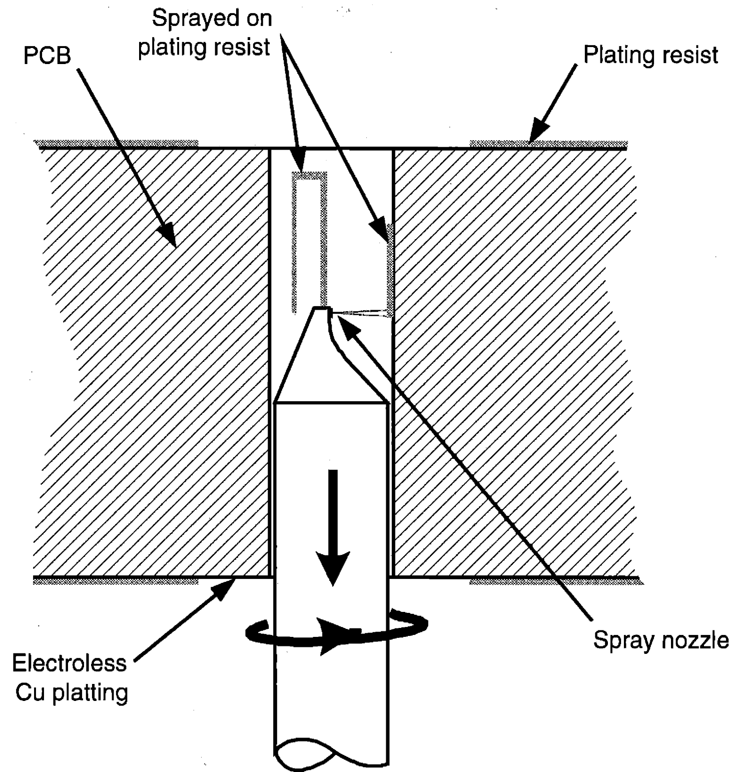

Figure 9-12: Inkjet print plating resist via.

Various concepts are presented for manipulating the etch- or plating-resist to create multi-connection vias during the etch cycle. Development of these processes requires changes to well established material flows, and adds significant expense and risk over end-of-process copper removal. Process chemical flow on exposed fiber edges poses uncertain risks, which requires additional exploration for all PCB matrix materials.

9.3.4 Laser machining

This section considers laser beam machining (LBM) for manufacturing multi-connection vias. LBM is a mature industrial process used for cutting virtually all engineering materials. For example, 1500+ Watt CO_2 lasers cut mild steels more than 14mm thick in industrial applications, [Powell].

9.3.4.1 Laser cutting mechanism

All laser-cutting systems concentrate light energy of a particular wavelength onto the cut surface. The cutting process in all cases is thermal, but the effect on the cut material varies. The

cutting process separates into four basic mechanisms: fusion, sublimation, chemical decomposition, and thermal shock.

There are two types of fusion cutting: inert- and reactive-gas. Most laser cutting systems use the flow of gas to control the cutting process, as indicated in Figure 9-13. In inert-gas systems, the material heats to a melting point and erodes out using high-pressure inert gas. This gives good kerf control and surface finish. The cutting process can accelerate using oxidizing gas or reactive-gas-assisted cutting. In this case, the base material burns and provides heat to the cutting process. This higher rate diminishes dimensional accuracy and surface finish.

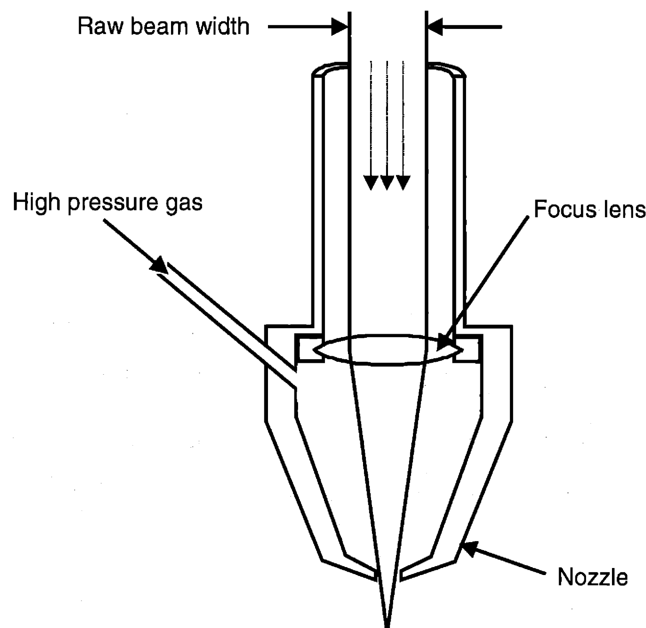

Figure 9-13: Cutting laser nozzle cross section.

With high enough energy densities, the material vaporizes or sublimates. The sublimation process depends on the ratio of the energy density to the vaporization temperature and the heat of vaporization. In fusion-cutting operations, some of the material also sublimates. The chemical decomposition mechanism burns the material, i.e. breaking of the chemical bonds, such as in laser paper cutting. Reactive gas cutting, described above, does not fall under this category because the main cutting mechanism is still melting and material flow out of the kerf. Base material oxidation that occurs in reactive gas cutting adds heat to accelerate the cutting process.

The fourth mechanism applies to glass cutting. It creates intense localized thermal gradients to crack the glass, making a zero-width cut. For PCB applications, both fusion and chemical decomposition are relevant.

9.3.4.2 Material affects on LBM

The material properties that affect laser machining include:

- hardness,
- tensile strength,
- shear strength,
- melting/vaporization temperature,
- latent heat of fusion/vaporization,
- reflectivity, and
- thermal conductivity.

The composite makeup of the PCB via consists of 40µm-thick copper on a glass-fiber/epoxy substrate (other less common materials are also used). The process only needs to separate the electrical connection by cutting a minimal amount of the dielectric. In typical industrial applications, different materials employ different laser configurations and wavelengths.

Copper is particularly difficult to cut with some lasers because of its high thermal conductivity and high reflectivity. The high reflectivity requires either surface treatments to increase the energy absorption or a laser that provides wavelengths not reflected by the copper, such as Neodinium: Yttrium-Aluminum-Garnet (Nd:YAG), solid-state laser. If the cutting operation occurs at the end of the PCB fabrication process, the tin-lead plating will lower the reflectivity, see Table 9-1. In some cases, however, the via requires gold plating, which is highly reflective.

Table 9-1: Material properties [Powell].

Material	Absorptivity to CO_2 laser (%)	Thermal conductivity (W/m/K)	Melting point		Heat generated during oxidation (KJ/mol)	Products
			(K)	(°C)		
Copper	1.0-2.0	385	1356	1083	160	CuO
Gold	0.5-1.0	296	1340	1067	-	-
Tin	[a]16.0	65	505	232	581	SnO_2
Lead	[a]4.5	35	600	327	1670	PbO_2

[a]Estimated.

The damage zone, created by cutting past the copper into the composite, changes based on material thickness, feed rate, and laser power. The damage zone increases with feed rate on the entry side and decreases on the exit side, while the higher power densities have smaller overall damage zones [Chryssolouris]. In general, moving faster decreases the damage zone. CO_2 lasers, usually used for cutting composites, have power ranges from 300W to 2kW. Micrograph studies show that the glass fibers melt in the cut zone and the resin matrix recedes away from the cut [Tagliaferri et al.]. The depth of recession or damage changes as a function of fiber orientation. The matrix around the fibers perpendicular to the cut zone recedes the greatest. Matrix recession in PCBs represents a particular problem because the matrix provides protection from moisture. The burned resin (char) forms conductive compounds, including pure carbon. Selecting a working gas and adding a secondary cleaning operation may minimize or eliminate this problem.

By-products from matrix chemical decomposition represent another problem with laser machining of composites. Gases released contain CO, CO_2, and low-molecular organic compounds [Powell]. In addition, aramid/epoxy (a combination sometimes used in PCB construction) produces large quantities of hydrogen cyanide.

9.3.4.3 Laser sources

While there are many types of lasers: solid-state, gas, dye, chemical, semiconductor, and free electron [Svelto]; those most commonly used in industrial material cutting are CO_2 gas and Nd:YAG lasers. Their common use is primarily due to low cost and sufficient power for cutting engineering materials. In addition to these two laser types, excimer lasers, common in micro-machining applications, are considered. CO_2 lasers have a 10.6μm wavelength, generated from exciting a gas mixture, and are used to commercially cut copper up to 4mm thick [Powell]. To

accomplish this cut thickness, the copper surfaces require low reflectivity coatings. However, the coatings only solve the problem on the surface, because on the inside, the molten pool of copper has the high reflectivity, which reduces the maximum cut thickness.

Nd:YAG lasers are generally better suited for cutting copper because the wavelength is 1.06μm, a length where copper better absorbs light. These solid-state lasers use either a high-powered flashlamp or a laser diode to excite a crystal. The light from Nd:YAG lasers has transparency to glass, which allows for use of cheaper, higher-quality glass optics; as opposed to the CO_2 lasers, which require zinc selenide or gallium arsenide lenses. Figure 9-14 shows the optics geometry. CO_2 lasers operate at higher power levels than Nd:YAG lasers, up to 5000W and 1000W, respectively.

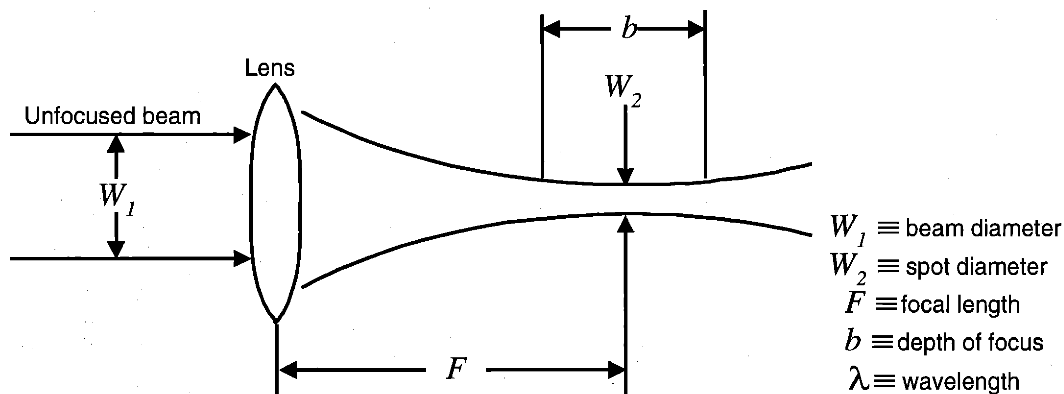

Figure 9-14: Laser focusing system.

One solution to the power discrepancy is to pulse the laser light. The pulsing allows for much higher peak powers, on the order of 10kW for Nd:YAG lasers. The pulsed laser yields smaller kerfs and smoother cuts, because the energy density is higher on a smaller area. It also provides another set of control parameters, namely frequency and on/off ratios [Powell]. Increasing energy density pushes the cutting mechanism more toward sublimation than fusion. A new class of lasers, called femto-second lasers, creates such short (on the order of 200fs), high-powered pulses that the surrounding ablated material has no time to conduct any heat. These lasers virtually eliminate the heat-affected zone.

The excimer laser is another type of gas molecule laser that is important to address. Excimer lasers transition from one molecular state (excited dimer state) to another (ground). The gases used by this laser are rare gas atoms in an excited state combined with F or Cl, together producing wavelengths in the deep UV range, see Table 9-2 [Svelto]. At these wavelengths,

features can be produced at one half the size of those produced by Nd:YAG lasers. The material removal process is ablation, due to the high energy densities. Most commercial excimer lasers operate in a 150W average power range. Lasers with average power exceeding 1000W are being developed [Borisov et al.].

Table 9-2: Wavelengths of excimer lasers.

Laser type	Wavelength (nm)
ArF	193
KrF	248
XeCl	308
XeF	351

Excimer lasers developed for commercial applications include photolithography, photoablation, photodeposition, contact cleaning, planarisation or surface processing [Godard et al.], micromachining [Tabat et al.], and aerospace alloy processing [Scott and Henry]. For multi-connection vias, the spot diameter and the focus depth determine the kerf and depth of cut. The spot diameter is defined by:

$$W_2 = \frac{8\lambda F}{\pi W_1} \tag{9-2}$$

The depth of focus, which determines the board thickness, is:

$$b = \frac{8\lambda}{\pi}\left(\frac{F}{W_1}\right)^2 \tag{9-3}$$

The parametric signal study in Chapter 3 shows that kerf widths smaller than 200µm are desirable. Further, the density study in Chapter 4 illustrates benefits of thinner separations. Plotting the spot diameter for different focus depths (see Figure 9-15) shows that CO_2 laser spot diameters are too large for this application. Nd:YAG lasers support diameters below 200µm and excimer lasers below 100µm, for even the thickest PCB. It is, however, uncertain if either type of laser can produce the power required to make such deep cuts.

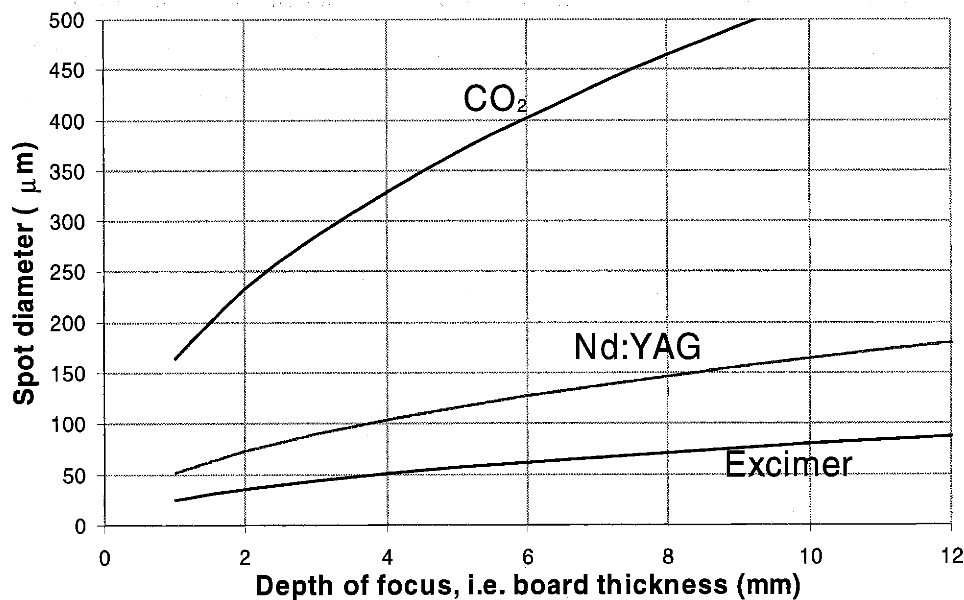

Figure 9-15: Spot diameter versus depth of focus for CO_2, Nd:YAG, and Excimer lasers.

One approach to reduce the power requirements is to change the incidence angle during the cutting operation, as shown in Figure 9-16. This process is better categorized as laser etching than cutting, because most of the operation occurs on the via wall. For high-aspect-ratio vias, lasers can operate from both sides of the hole, thereby requiring only half the depth of operation.

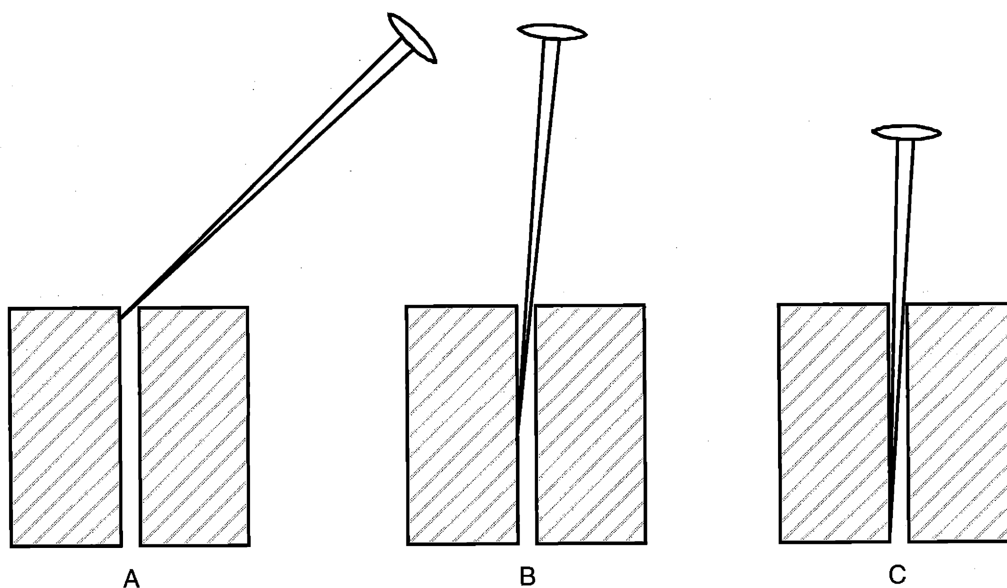

Figure 9-16: Variable incident angle laser cutting.

Because the angle of incidence varies, the spot size and shape continuously changes. The cutting rate also varies continuously to compensate. While this is potentially better than trying to cut parallel to the via, these compensations may prove impractical. As shown in Figure 9-17, an approach that could solve this problem places a 45° mirror inside the via from the opposite side of the board to provide constant normal incidence. The normal incidence on the barrel surface allows for very small spot diameters, and consequently, higher energy densities. Gas flows from the backside of the via parallel to the mirror support. The type of gas can be a significant factor in cutting rates [Scott and Henry].

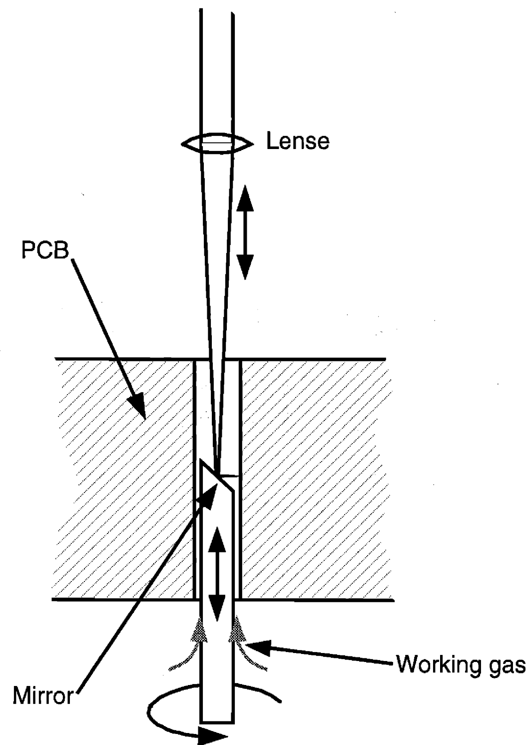

Figure 9-17: Backside mirror provides constant normal incidence.

One potential problem with this configuration is the mirror's close proximity to the cutting point. The beam has high energy densities very near its focal point, which could damage the mirror surface. Overcoming this problem offers the potential of producing IVT geometry.

9.3.4.4 Laser cutting rate

Cutting rates depend on specific parameter settings. Published data, as shown in Table 9-3, give a general idea of the rates to expect. Information about laser pulse power, pulse duration, and

gas jet velocity are critical to the achievable cutting rate [van Dijk]. Developments of these parameters often follow trial and error experimentation. Analytic cutting rate models have been developed for metal cutting, [Chryssolouris] and [Schuöcker]; and thermal models for composites, [Tagliaferri, et al.].

Table 9-3: Cutting performance for various materials and configurations.

Material	Laser		Cutting Gas	Thickness (mm)	Cutting speed (mm/s)	Kerf (mm)
	Type	Average Power (Watt)				
[1]Glass/resin	CO_2	500	-	1.6	250	-
[2]Glass/epoxy	CO_2	1000	-	5	33.3	0.5
[1]Copper	Nd:YAG	200	-	1.5	0.58	-
[1]Copper	Nd:YAG	300	-	1.5	3.33	-
[1]Copper	Nd:YAG	300	-	4	1.08	-
[3]Copper	Nd:YAG	120 ([a]4000)	Oxygen	3	0.83	0.2
[1]Copper	CO_2	500	Oxygen	0.6	8.3	-
[3]Gold	Nd:YAG	190 ([a]10000)	Oxygen	3	.25	0.35
[2]Mild Steel	Nd:YAG	150	-	1.5	3.83	0.6
[2]Mild Steel	CO_2	250	-	0.5	10.6	-
[1]Steel	Nd:YAG	300	-	5	1.5	-
[1]Lead	CO_2	500	-	3	60	-

Sources: [1][Belforte and Morris], [2][Chryssolouris], and [3][van Dijk].
[a]Pulse power.

The depth of cut, shown in Figure 9-18, requires some assumptions for plating thickness and safety margin. Plating thickness varies from as little as 10µm to more than 50µm. An assumed safety margin of 40µm results in a cut depth of 60 to 90µm. Cutting rates scale directly with board thickness, and are therefore kept as independent variables. Based on the data in Table 9-3, a 1000W-pulsed Nd:YAG laser (the upper limit for commercial Nd:YAG lasers) cuts 4mm thick copper at a rate of 3.6mm/s. Assuming the machine tool supports up to 3g's of acceleration and the laser enters the cut at maximum speed (in this case, speed is limited by acceleration), the cutting time falls between 4 and 5ms.

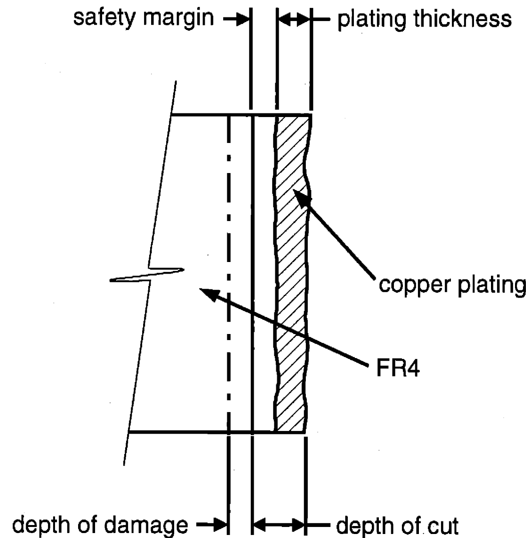

Figure 9-18: Cross section of cut.

9.3.4.5 Laser machining conclusions

Industry generally uses CO_2 lasers for composites, tin and lead; and Nd:YAG lasers for copper and gold. It is possible to use a CO_2 laser for splitting vias with tin-lead plating, but at the risk of board thickness and large gaps. If a design requires gold plating for a connector application, the Nd:YAG and excimer lasers offer the only options. In addition, Nd:YAG and excimer have kerf sizes more than ten times smaller than CO_2 lasers within the range required for split vias (less than 200μm). With limited published data on the performance of Nd:YAG or excimer lasers in cutting composites, fundamental research on this cutting process is necessary, along with research on cutting across the copper composite transition.

The best potential electrical configuration derives from the ability to cut normal to the surface of the via, i.e. laser etching. This concept provides flexibility in terms of via diameter, hole depth, hole shape and routing patterns. The main challenge is to find a mirror material and configuration that can support the high energy densities.

9.3.5 Milling

One way to address the limitation of a purely vertical, separated conductor is to slot mill the via horizontally at a particular level, as shown in Figure 9-19. This approach can also be applied to non-vertically split vias. In some high-performance applications, PCB vias are counter bored after plating to remove the unused conductor ends. This step eliminates the stub effect, high-

frequency ringing that occurs in non-terminated conductors. Milling offers this same benefit. In addition, it provides a density benefit by allowing for sets of connections at different levels. A third milling advantage comes from the ability to operate from just one side, where as counter boring requires work from two sides and consequently, two setups.

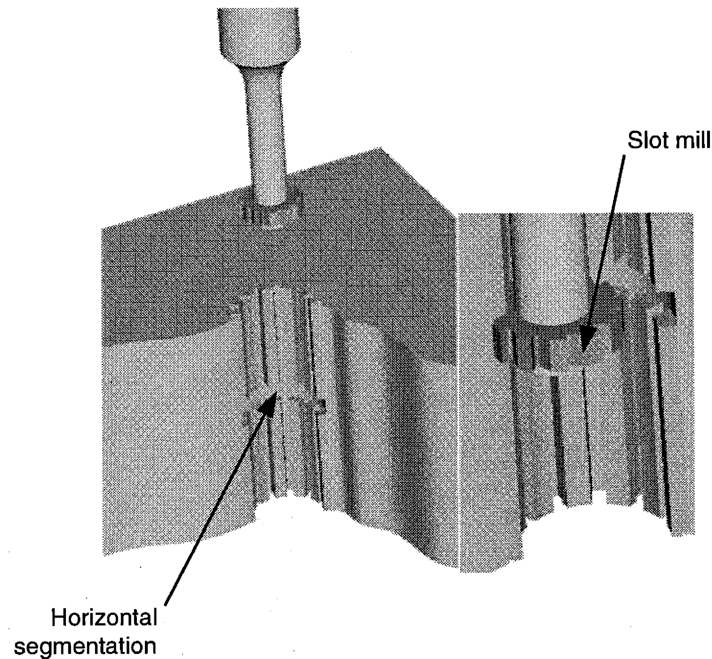

Figure 9-19: Two-dimensional via splitting.

A rotary slot cutting tool is placed in the via. Once positioned, the cut is made by circularly interpolating the high-speed tool. Aside from the cutting fluid pumped into the via to prevent the cutter from clogging and true position finding, the cutting operation is within the capabilities of standard PCB drilling equipment.

Because of the constant plating thickness, regardless of via diameter, a small tool can cut large vias, with a limitation of hole depth. The tool shank determines the depth limit. The shank diameter is smaller than the cutter diameter, which is smaller than the via diameter, thereby compounding the problem. Therefore, the process requires either low aspect ratio vias or setup from both sides.

9.3.6 Ultrasonic machining

L. Balamuth first patented ultrasonic machining in 1945. Its development has focused mostly on materials that are difficult to machine [Rozenberg et al.]. Conceptually, ultrasonic machining is

simply a grinding process that typically sinks a tool into the work material. Because of the overlap with EDM capability, ultrasonic machining is less common.

9.3.6.1 Ultrasonic cutting mechanism

A typical ultrasonic machining application, illustrated in Figure 9-20, feeds an abrasive fluid between the tool and the work piece. The tool is vibrated at frequencies in the ultrasonic range (i.e., frequencies above the range of human hearing, >16kHz). As the tool wears into the work piece, it feeds down to the desired depth. The working fluid and the applied force determine the gap between the two pieces. Both the work piece and the tool abrade, requiring tool replacement or sharpening for final cuts.

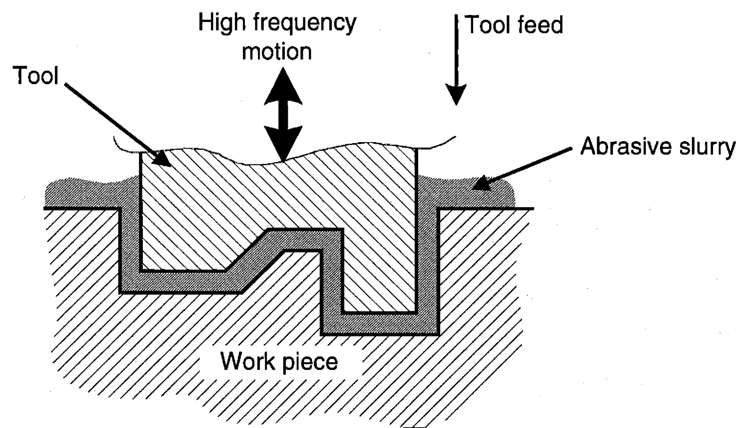

Figure 9-20: Fundamentals of ultrasonic machining.

Figure 9-21 shows a typical arrangement of an ultrasonic machine tool. The transducer or generator utilizes either magnetostrictive or piezo-electric mechanisms suspended with fluid or flexure bearings. The oscillations transmit to the tool through the acoustic head, which is a displacement amplifier. The amplifier design is critical to the development of proper waveforms, [Pandey and Shan]. Two approaches exist for getting the abrasive fluid to the work-piece/tool interface: submerging the piece in a liquid/abrasive powder mixture, or spraying an abrasive slurry.

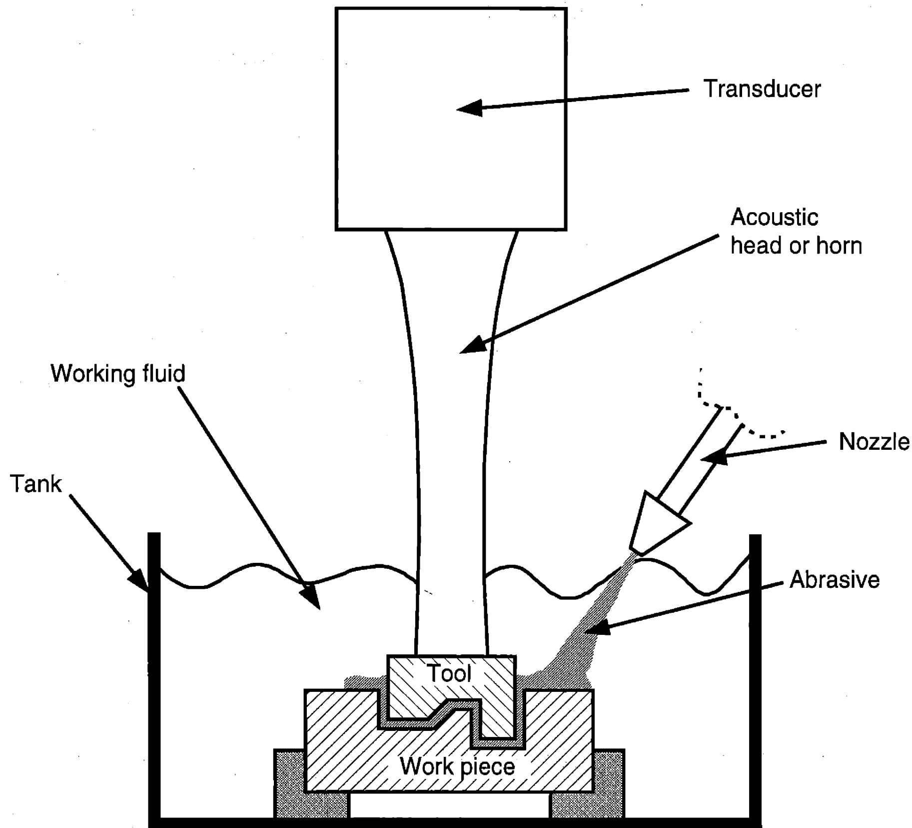

Figure 9-21: Typical machine configuration.

Holding the feed force constant maintains an even abrasive cutting-force distribution. Force-based feed makes springs, counter weights, pneumatic and force feedback servo-control best suited for ultrasonic machining. For the case of PCB vias, characterizing the cutting force by experimentation and using rate-controlled feed may prove most efficient. Both the required cutting force and the rate vary based on the liquid media and the abrasive grits, which range from 200 to 2000 grit.

An example of plated via cutting is shown in Figure 9-22. This cutting requires the tool to provide a large enough clearance between the shank and the plated barrel to prevent erosion in undesired locations. Ramping the tool as shown in the figure increases the surface contact area and, in turn, increases the cutting rate. This technique requires a minimum angle setting to achieve a tolerable radial deflection.

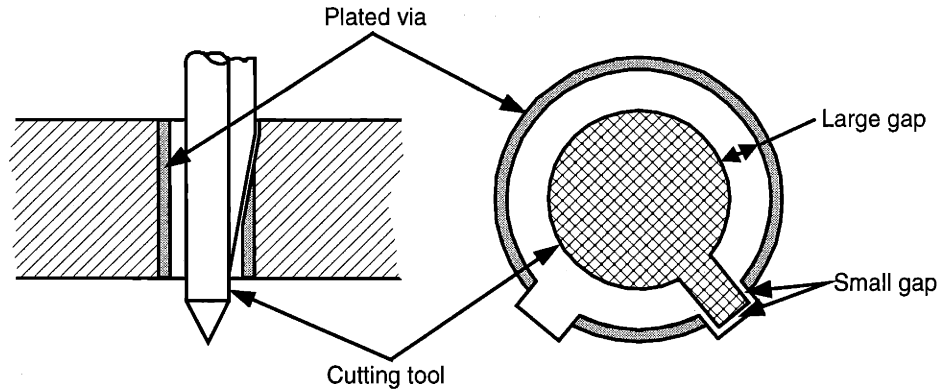

Figure 9-22: Cutting of plated barrel.

9.3.6.2 Materials and ultrasonic machining

The cutting mechanism for ultrasonic machining is either ductile or brittle, depending on the material being cut [Pandey and Shan]. Traditionally ultrasonic machining has been used to cut very hard materials, because its process is expensive and softer materials have less expensive options. While no data was available on cutting PCB with ultrasonic machining, Table 9-4 provides cutting rate data for various other materials to offer some feeling for the rates.

Table 9-4: Relative cutting rates of different materials [Rozenberg et al.].

Material	*Cutting rate (mm^3/min)
Brass	2.2
Tungsten	1.6
Titanium	1.35
Steel (Rc=62)	1.3
KE672 Steel (Rc=66)	4.7
Chrome Steel	4.7

*16.3kHz at 12.4μm amplitude with a boron carbide tool.

If the PCB cutting rate is similar to that of brass (2.2 mm^3/min), then the assumptions detailed in Section 9.3.4.4 make some rough estimating possible. For a 3mm thick PCB, each via split would take approximately 20 and 30ms.

9.3.6.3 Ultrasonic machining conclusions

While ultrasonic machining of multi-connection vias theoretically offers acceptable cutting rates, geometric constraints prohibit a conventional configuration. The long slender tools required for cutting small-diameter, high-aspect-ratio holes change the dynamics of the cutting motion that finds no parallel example in available literature. Unlike broaching, the tool cannot use the via as a guide. As a result, deflections of the tool tip pose the additional problem of unwanted cutting. Clearly, this process for multi-connection via manufacturing requires significant development and experimentation just to examine feasibility.

9.3.7 Abrasive water-jet cutting

Abrasive water-jet (AWJ) equipment accelerates a mixture of high-pressure water and abrasive material (e.g., silica, garnet or aluminum oxide) through an orifice to cut hard and soft materials. The basic cutting mechanism is erosion. Figure 9-23 illustrates a typical water-jet cutter nozzle. Recent development of high-pressure water pump technology, able to produce over 250Mpa, has made this process feasible. Most commercially available systems create kerfs larger than 700μm.

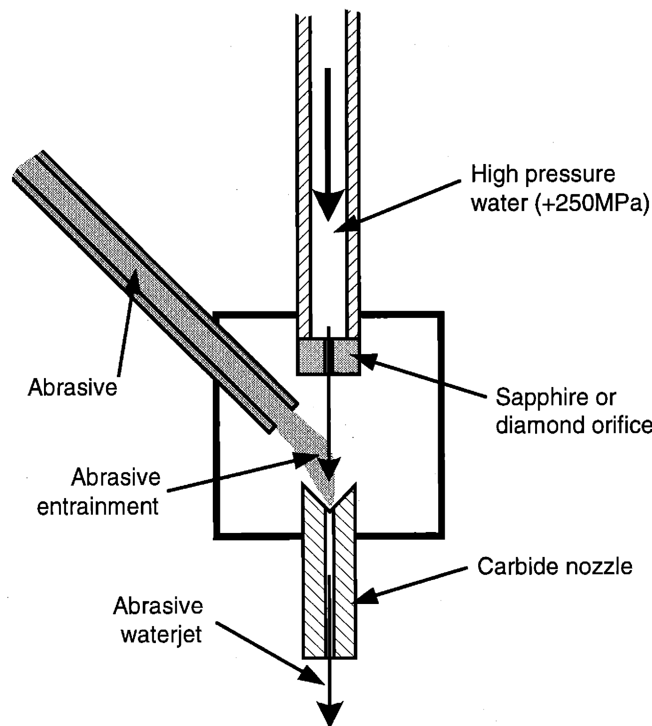

Figure 9-23: Functional elements of an AWJ system.

Applying this technology to multi-connection via manufacturing offers several advantages:

- high cutting rates,
- no direct hardware contact around the via (aside from holding the whole PCB),
- single-sided machine tool,
- one process for all materials, and
- applicability to thick boards.

ABJ, however, does apply a localized force on the material, which can cause breakout problems with fiberglass composites. Kerf size represents the chief problem with this process. Without some process redesign, only very large vias can be produced.

Because cut width represents a primary impedance-tuning variable, cutting mechanism resolution on this parameter needs to be smaller than the smallest cut width. Barring this limitation, AWJ offers an attractive process for multi-connection vias. Therefore, feasibility assessment on this process requires an in-depth review of the fundamental physical limitations associated with the mechanism that determines the jet diameter.

9.3.8 Summary of manufacturing process selection

This survey of potential manufacturing processes covers broaching, EDM, chemical etching, laser machining, milling, ultrasonic machining, and AWJ. The selection and development of candidate processes requires a thorough analysis of all the functional requirements, some of which include:

- development cost,
- capital equipment cost,
- production rate,
- operating cost (including consumables),
- geometry generation capabilities (vertical, horizontal and IVT),
- control and scale of feature parameters (via diameter, gap width and aspect ratio),
- fiber damage, and
- acceptability (current process disruption).

The experiments and theoretical developments in this thesis provide data for broaching and wire EDM. Consideration of other processes requires further research and experimentation. Ideally,

the selected process will incrementally scale to cover all the geometry demands, and ultimately result in the highest performance via structures.

9.4 Split via machine tool

The electrical experimentation associated with via broaching required the design of a manual-broaching machine, see Section 5.1.6.2 for details. Similarly, high-speed production demands the integration of the same manual functions into a high-speed machine tool, pictured in Figure 9-24. Most of the processes proposed in the prior section operate one via at a time; thus the layout of the machine tool is conceptually similar for each process.

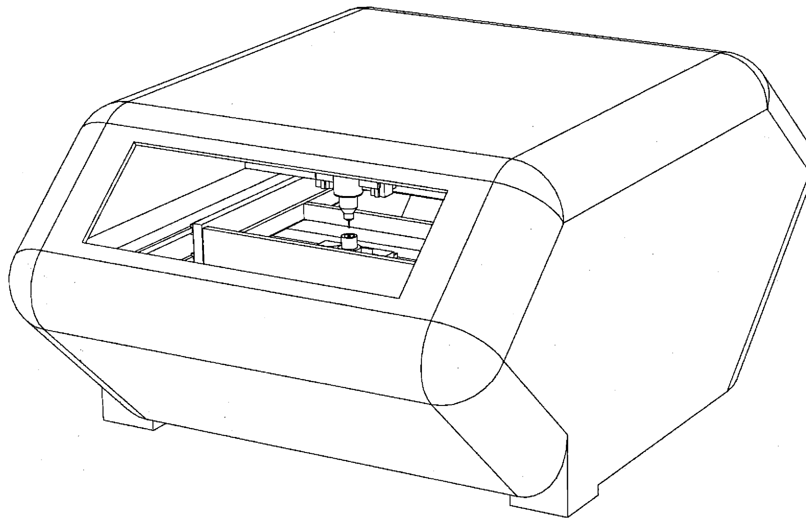

Figure 9-24: Multi-connection-via machine tool concept.

Because the proposed technologies manufacture vias one at a time, the system requires X-Y positioning to locate the hole in the PCB. The axes locations govern the size and function of the machine. Figure 9-25 illustrates one possible configuration that holds the PCB in a fixture containing the system Y-axis. The two X-axes shown hold the upper and lower tools, and are calibrated to remain aligned. This configuration allows for a narrow machine, similar to PCB drilling, which promotes a side-by-side factory layout. In addition, the bridge structure that supports the tooling is short and stiff. Placing both X- and Y-axes on the PCB side of the structure fixes the positions of the upper and lower tools, eliminates one or two sets of axes, and keeps the process stationary. The other extreme puts both X- and Y-axes on the tool side, providing the smallest machine footprint, smallest moving mass, and simpler PCB fixturing. Ultimately the selected process will determine the need for the lower tool, without which the machine simplifies significantly.

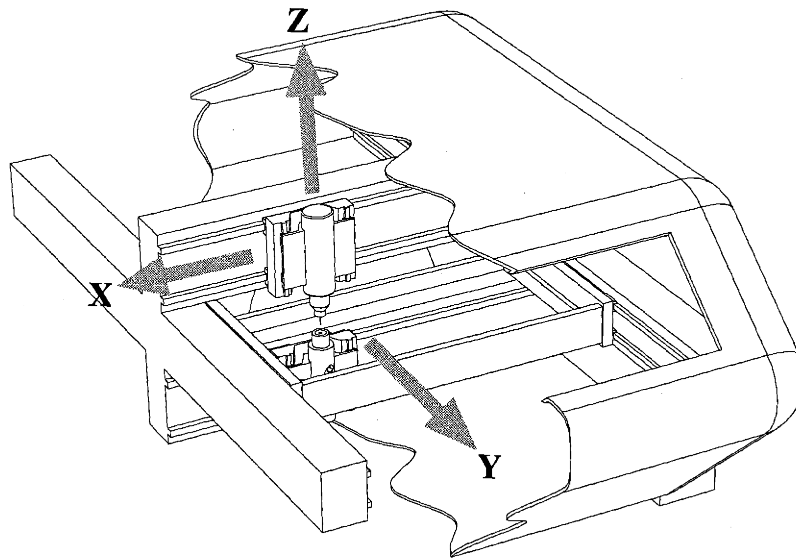

Figure 9-25: Machine tool, break out view.

9.4.1 Tool-to-via true position errors

The absolute location of the via relative to the PCB artwork is subject to errors in PCB manufacturing. Inner-layer features have 3σ errors of 131μm, [Braunstein]. The contribution due to drill error is 34% of the total, but the multi-connection via diameter has a significantly larger size (4-10 times). Thus, it stands to reason that the real drill error contributes less, generating a total 3σ errors less than 131μm.

Using the tip of the tool as a location error sensor requires the machine tool to compensate during insertion, as shown in Figure 9-26. With this information and the maximum true-position error of the vias, the minimum tool-diameter is calculated to be 0.262mm. Thus, the conical tip of the tool enters the via hole without hitting the top of the PCB, even with the highest possible true position error.

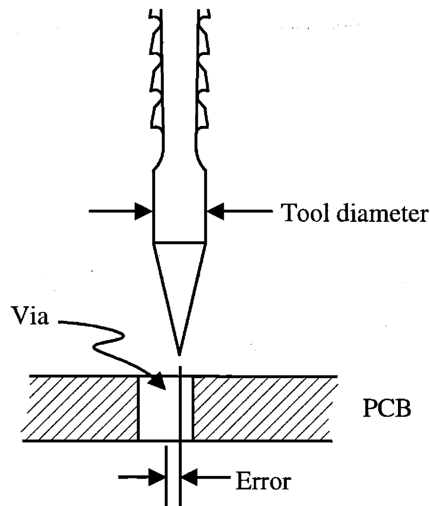

Figure 9-26: Tool misalignment.

With the tool and hole misaligned, the machine tool senses the error and compensates the upper and lower tool, as shown in Figure 9-27. After fully centering the cutting tool, the lower tool is raised to clamp the PCB. Translating the mechanical signal back to the control system requires an electromechanical scheme, as addressed by the following two concepts.

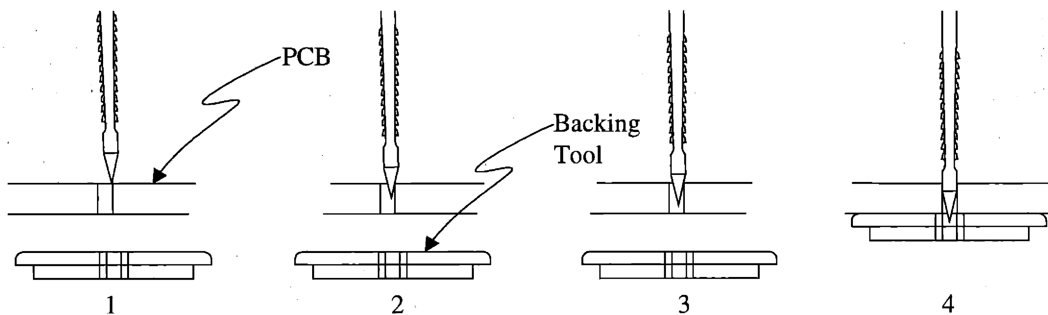

Figure 9-27: Broach to hold misalignment.

The first concept uses linear force feedback. Figure 9-28 shows how the forces in the tool are translated to the tool holder, where force sensors feedback to the positioning control system. The controller works to minimize the force on each sensor as the tool moves in the downward direction, controlling the decent such that the displacement forces stay below a pre-determined safe value. One problem with this approach is the long distance between the tip of the tool and the force sensors. This distance causes the force to translate into moments.

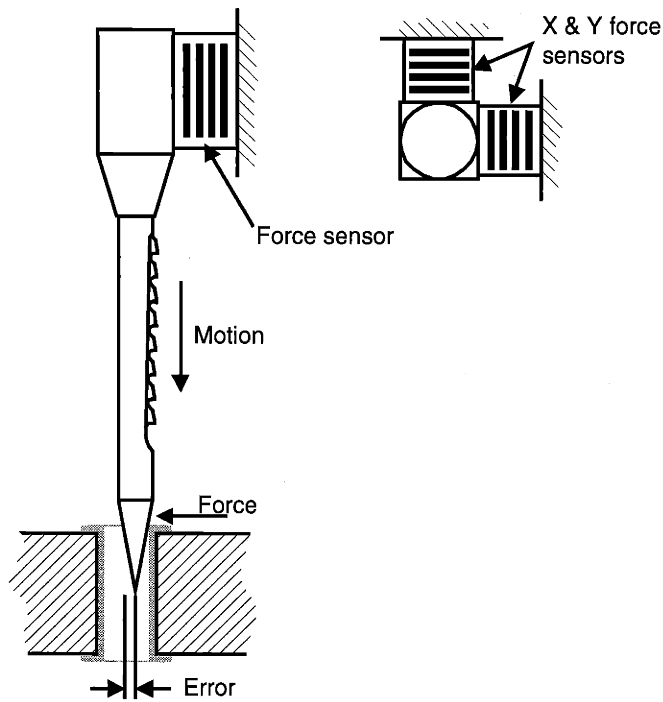

Figure 9-28: Force measuring displacement system design.

The second concept uses linear displacement sensors, as shown in Figure 9-29. True position errors cause angular displacements of the tool tip. These errors translate through the tool showing up as linear displacements in the sensors. The control system compensates inversely to the sensed displacement. This configuration also allows for error amplification. The downward motion controller ties in to limit the maximum error allowed before continuing.

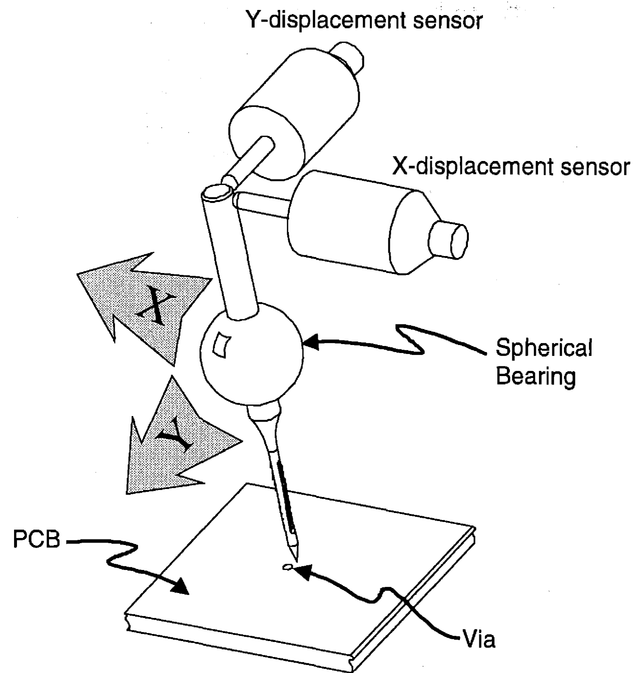

Figure 9-29: Angular displacement design.

The sensor requires control system response times to be very fast. Tool usage, mass, stiffness, and friction can each limit response time. Figure 9-30 shows a non-contact approach that scans ahead of the tools to locate the hole center before the tool enters. This approach de-couples the tool from the sensing function, allowing for higher rates. The downside comes in using a wet process, which disrupts the optics.

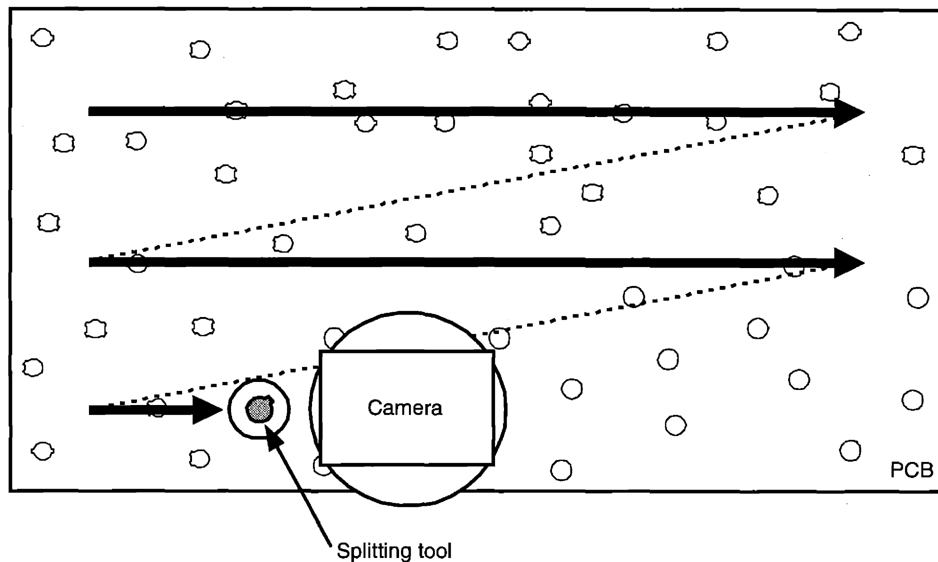

Figure 9-30: Vision scanning

9.4.2 Summary of machine tool design

Cost drivers in the machine tool design include the number of axes, the process, and the maximum PCB size. Determining the need for a lower tool governs the number and size of axes. Each axis is estimated to add about $30-50K (in 1999 US dollars) to the machine tool sale price. Different process technologies (e.g., laser, EDM, ultrasonic, etc.) have different cost levels. PCB drilling machines control cost by ganging multiple drill stations together to share controls, structure and axes. Localized position correction required for multi-connection via manufacturing makes sharing axes difficult, if not impossible. Ganging subsystems, especially core process technologies, presents cost-saving options. For example, one laser source can provide light to multiple stations, or one dielectric processing system used for multiple wire EDM heads.

9.5 Board testing

PCB manufacturing employs inspection at different points in the process. On the roadmap to commercialization, multi-connection vias affect every inspection point. Internal panel inspection, prior to board lamination, must incorporate a check of the special pad designs for the multi-connection via. After fabrication and via splitting, a PCB bed of nails tests the board for shorts and opens. These testers probe at the pads and vias using conventional pogo pins. The pogo pins that contact the multi-connection vias must be retrofitted with multi-connection via pogo pins, such as those discussed in Section 8.1.3. After all the components are attached, PCBs are again checked using testers such as the one shown in Figure 9-31. This tester also requires fixture retrofitting with multi-connection pogo pins.

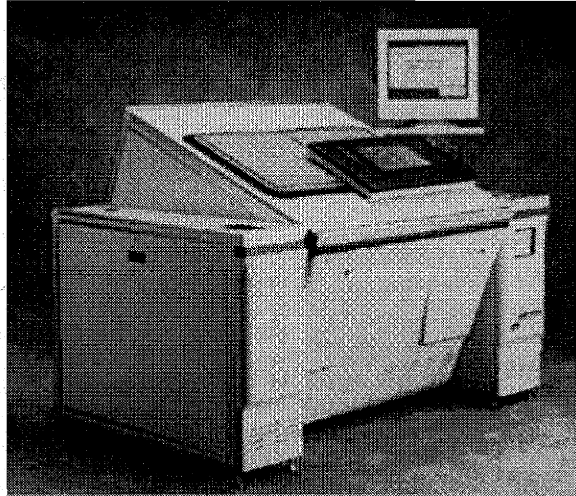

Figure 9-31: Teradyne Spectrum™ 8800 PCB tester.

9.6 Potential durability problems

The PCB operational environment varies widely from very clean laboratory conditions to very harsh industrial settings. Since the circuit board is the interconnection between devices, it must be the strongest link in the failure chain. One of the largest threats to the viability of multi-connection vias is potential failure due to environmental factors. Removing the copper inside the via barrel exposes the fiber/resin edge to the environment, providing opportunities for moisture and chemical attack, crack propagation and possible copper molecule migration.

9.6.1 Fiber/matrix damage

Force-based cutting technologies (like broaching, milling, AWJ, and to a lesser extent, ultrasonic machining) all cause some amount of localized de-lamination, as the broach experience showed, see Figure 5-31. Applying the cutting force normal to the laminate, as shown in Figure 9-32, causes the fibers to bend and the matrix to fail locally. Using a backing tool on the exit side minimizes fiber break out from the bottom, but does not fully solve the problem. The free edge of a composite structure is often the source of de-lamination because of the stress condition [Pagano].

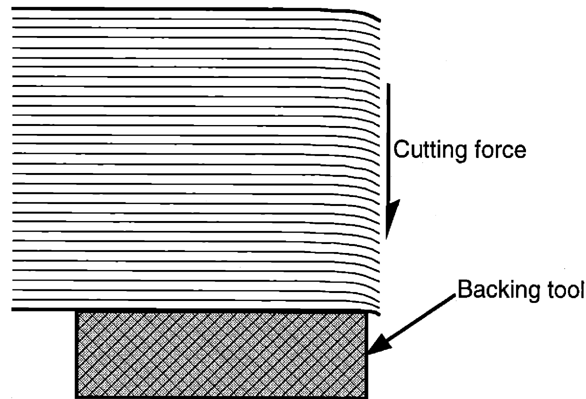

Figure 9-32: Cutting forces on fiber/matrix.

Laser machining can also damage the matrix thermally, as shown in Figure 9-18. The thermal damage forms both a matrix recession away from the cut and resin charring. The char is of particular concern. If the carbon content of the char is high, it significantly changes the dielectric and conductive nature of the matrix. Using shorter, higher-powered pulses to shorten the heat transfer time can minimize this damage.

Any exposed fiberglass edges can permit moisture to enter the fiberglass structure and raise the potential for moisture-induced damage. From cycle to cycle, this damage occurs as debondings at the fiber-matrix interface [Reifsnider]. Full water submersion experimentation shows that fiberglass that was impact damaged showed an average of 10% damage zone growth [Butts et al.]. In cases where the process itself does not damage the fiber/matrix, i.e. build up and EDM, there is still a potential problem with the exposed fiber edge. In all cases, the potential life reduction caused by the disrupted regions needs to be understood, and if necessary, addressed.

9.6.2 Testing

Conducting both thermal cycle and electrical bias tests on sample boards will help define the extent of the exposed fiber problem. The thermal cycle test samples sectioned and compared with non-cycle test samples, exposes crack growth problems. Adding an electrical current bias to the circuit promotes copper migration in susceptible regions. Careful monitoring of resistance between via segments as a function of time indicates board life susceptibility to copper migration. Fiber damage levels can be compared using broach and EDM-produced multi-connection vias.

9.6.3 Sealing

Sealing the via with a polymer offers an obvious solution to crack growth and copper migration. Producing only panel laminated buried and blind vias inherently solves the sealing problem, because the resin naturally migrates during lamination. A secondary sealing operation offers the same benefit for through vias. The process could be integrated with the same machine tool, inline with the splitting operation, be run on a separate machine, or be added in a process batch fashion. Since the via does not require filling to seal, a thin coating of epoxy, UV-cured or thermal-set polymer sprayed on the wall would suffice. This approach allows press-fit contacts to wipe away the polymer during insertion. Filling the via with a semi-cured silicone gel can also support press-fit connections.

9.6.4 Summary of durability issues

Durability of the multi-connection via in the PCB remains an uncertainty in this research. Manufacturing methods employed and proposed all have different degrees of fiber exposure in the separation region. Anecdotal evidence suggests that crack growth and/or copper migration pose a serious risk to the long term viability of the board. Both testing methods for determining the extent of the problem and sealing methods proposed in this section need further exploration.

9.7 Summary

This chapter develops a roadmap for multi-connection via commercialization. The purpose is to pose questions for future development. The map plots from the design stage, through manufacturing, and into testing. Along the way, It identifies research opportunities in via design, CAD/CAM development, manufacturing process, board test and durability.

10 Conclusions

This chapter presents a synopsis of the main contributions in this thesis, a brief summary of major themes covered in the chapters, and conclusions. It closes with recommendations for future work.

10.1 Thesis summary and contributions

The context of this research derives from current and future performance demands on printed circuit boards, in the areas of both signal integrity and connection density. Industry data clearly shows that future performance needs outstrip today's capabilities. Connecting the layers in a multi-layer PCB represents the primary focus for this thesis.

The PCB provides signal impedance control within the layer plane, but this control breaks down when signals change layers using conventional plated-through holes. The thesis has demonstrated, through simulation and experimentation, that multi-connection vias provide full impedance control when transitioning between signal layers. This key contribution fundamentally changes routing rules for high speed signal traces, allowing for layer changes without concern of signal degradation. An essential conclusion drawn from the data shows that signal performance of the co-cylindrical wave-guide structure is completely independent of diameter, which opposes conventional via rules.

The thesis also demonstrates that the same performance benefits carry over to a PCB's connector and device launches, providing an impedance-controlled structure throughout the transition. With this in mind, new concepts for multi-connection via launch, connectors, and devices are presented. The thesis also proposes a new class of VMT devices that integrates the device into the PCB and improves signal performance.

A second area of improved performance is connection density. In this thesis, density is defined with a routability model. The model demonstrates the density improvement multi-connection vias achieve over conventional technology. A manufactureability model uses the manufacturing process constraints to bound results of the density analysis.

To construct multi-connection vias in PCBs for signal experiments, a broach process was developed for segmenting plated-through holes. Simulations of the broaching process, based on

conventional cutting force models, provided a method for designing broach tools. Measuring actual cutting forces while broaching multi-connection vias verified the simulations. A specialized machine was designed and built for broaching the experimental PCBs.

The thesis also presents methods for designing multi-connection vias. The methods cover the design of via cross-sections for single-ended and differential signals, optimum configurations for impedance control, and pad design. The pad design accounts for tolerance issues and ground plane layout. Another important result is the IVT geometry design, which offers the highest potential signal and density performance possible within the confines of a cylindrically plated conductor, while improving routability (see Table 10-1 for comparison with other technologies). Furthermore, the concept of a shielded via offers improved performance to connectors and devices without requiring design changes.

Table 10-1: LLI technology comparison.

Design options	Functional requirements				
	Impedance control	No stubs	Board launch	Full height connection	High density
Through-hole via			x	x	
Blind/buried		x			x
Counter-bored		x	x		
Micro-vias	x*	x			x
Multi-connection vias	x		x	x	x
Blind/buried MCVs	x	x			x
Counter-bored	x	x	x	x	x
IVT	x	x	x	x	x

*With only one layer change.

A roadmap to commercializing multi-connection vias is the final contribution of this thesis. It identifies the major areas of research and development required to achieve a commercially-viable process, including problems and proposed solutions covering design, manufacturing, and testing.

This research stemmed from a concept for a new connector that would integrate tightly with the PCB. It has evolved into a path for developing both a new manufacturing process and a new PCB feature, namely the multi-connection via – a new structure, which offers impedance control for signals passing from layer-to-layer, something that was not previously possible.

10.2 Future work

The roadmap laid out in Chapter 9 details many topics for future work. Before progressing further along the roadmap, however, a clear model of the economic factors is necessary to determine priorities. That said, the development of IVTs likely presents the most interesting challenge and the greatest promise for overall performance gain.

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Appendix A
Multi-layer PCB manufacturing

This section provides a basic overview of multi-layer printed circuit board (PCB) manufacturing. The proposed processes for making multi-connection vias is integrated into different points of the standard PCB manufacturing process described herein.

Multi-layer PCB manufacturing begins with inner core layer processing. Cores are comprised of fully-cured resin/fiber laminates that are clad with copper on both sides, as shown in Figure A-1. Traditional core materials are glass/epoxy (FR4). In a drive for lower dielectric constants and small dielectric loss tangents, other core materials are under development and seeing some commercial use. While the processes vary somewhat for different materials, they are fundamentally similar to the process described below.

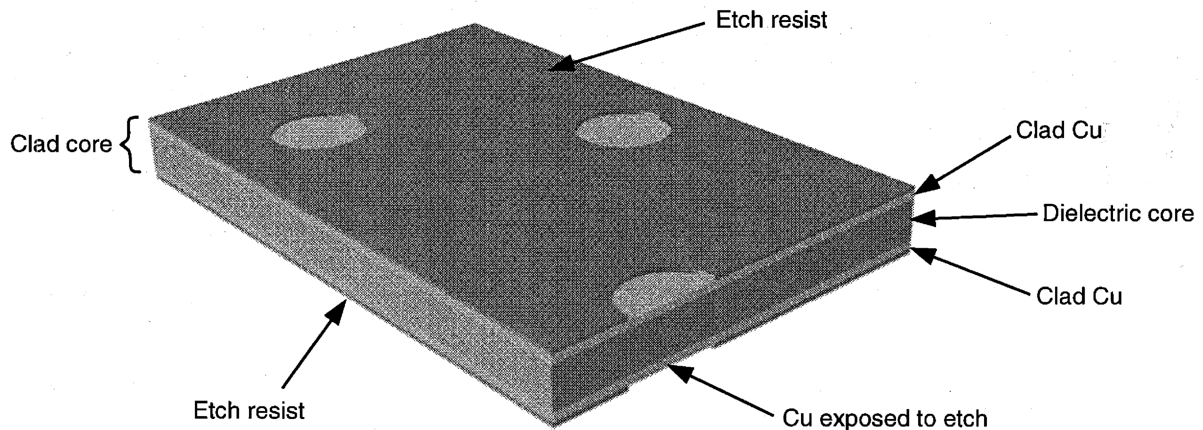

Figure A-1: Copper-clad inner core with developed etch resist.

The core's copper clad surface is coated with a photosensitive etch resist film. (Screen-printed resist films are available, but they are typically used in older processing). The resist is then exposed to UV light through a film master, typically with one-to-one optical scaling. This step polymerizes the exposed resist, thereby allowing the unexposed coating to be washed away. The copper in the exposed regions is then etched away leaving the desired circuit structure. This type of core processing is performed in Develop-Etch-Strip (DES) lines, as shown in Figure A-2.

Figure A-2: Develop Etch Strip (DES) line.

Once the cores are processed in the DES line, they are stacked intermittently with prepreg (partially-cured resin pre-impregnated fibers). The prepeg forms the dielectric material between the cores and serves as the bonding material. Figure A-3 shows the stack before lamination. The outer-most surfaces of the laminate book must be uninterrupted copper, i.e. not etched. This is accomplished by not processing one side of the outer two cores (called cap sheet) or by placing layers of copper foil (called foil lamination) on the outer layers, as shown.

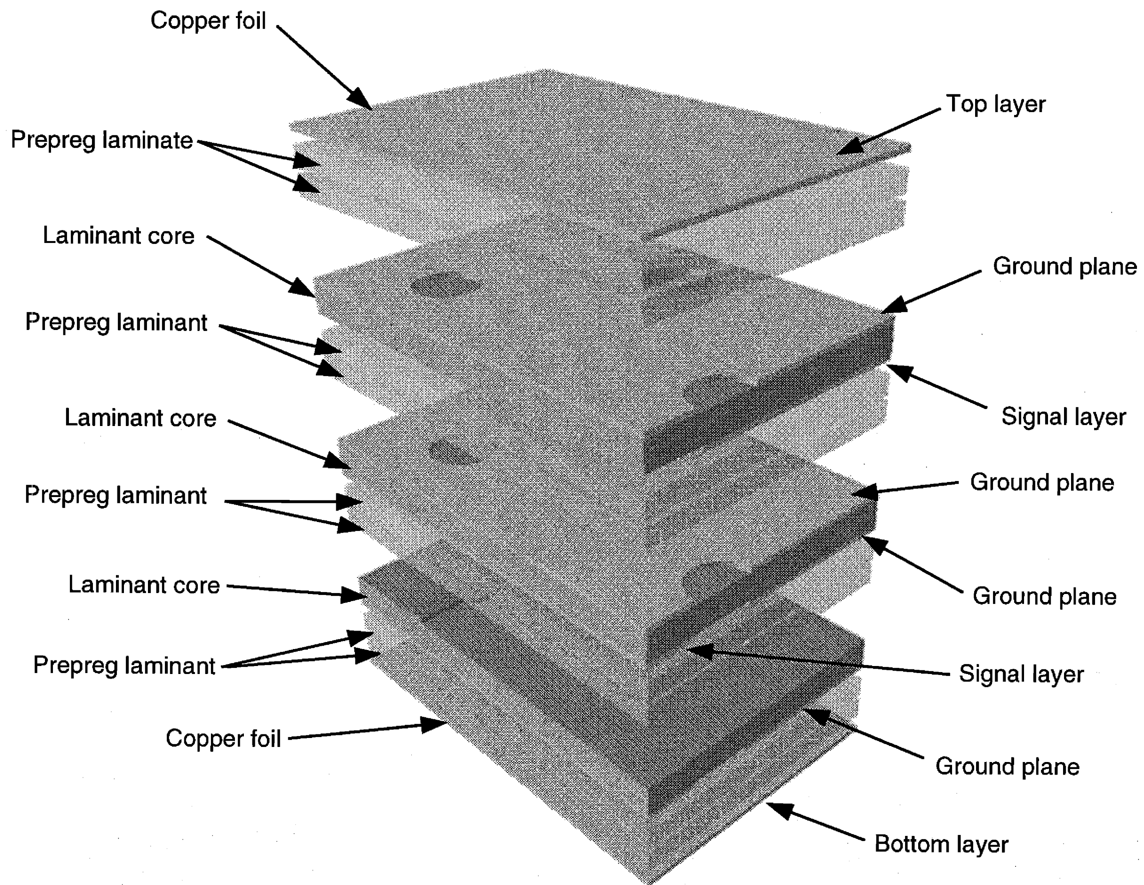

Figure A-3: Complete stack before lamination.

The laminates are cured with heat under high pressure, and then drilled on special printed circuit board drilling machines, see Figure A-4. The resulting holes provide the conductor pathways, vias, for interconnecting the layers. After drilling, a de-smearing or epoxy etch-back process is usually used to clean off any resin that remains on the conductors. The etch back process also improves the copper plate anchoring, [Jawitz]. Notice how a ground via has been drilled in a location where the ground planes do not have the clearance which signal vias have. In cases where devices are soldered into ground vias, a spoked pad may be used to limit the heat transfer between the via and the ground plane for better solderability.

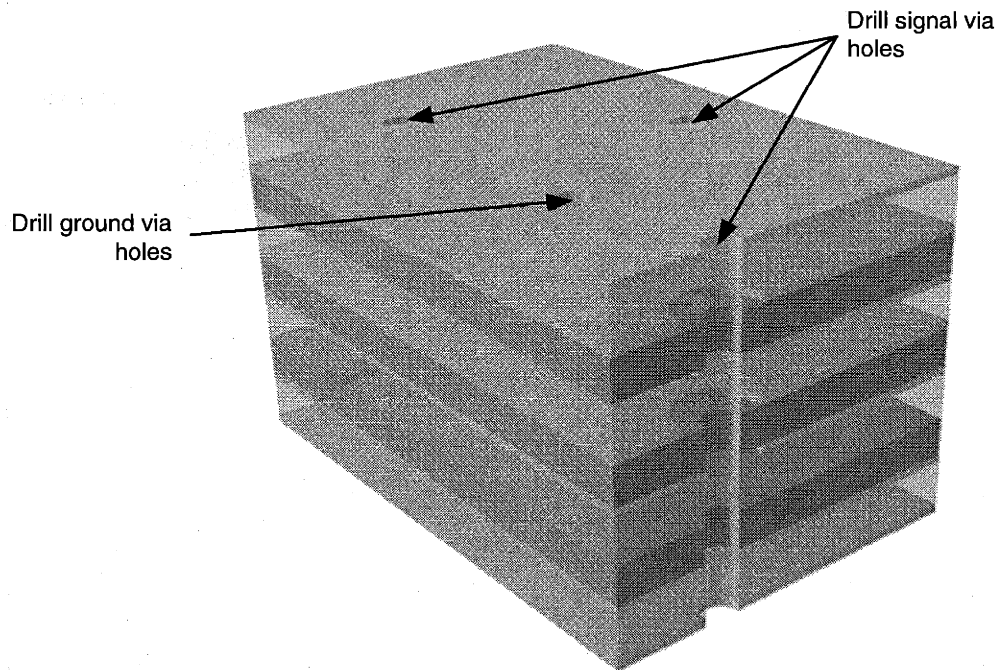

Figure A-4: After lamination and drilling.

The panels are exposed to a tin/palladium catalyst that sensitizes all the exposed surfaces allowing for copper deposition using an electroless plating process. All exposed surfaces gain a 1.25 to 4μm-thick copper coating, making them all connected electrically, see Figure A-5. This coating seeds the surfaces and allows for future electroplating steps, which require all surfaces to be conductive.

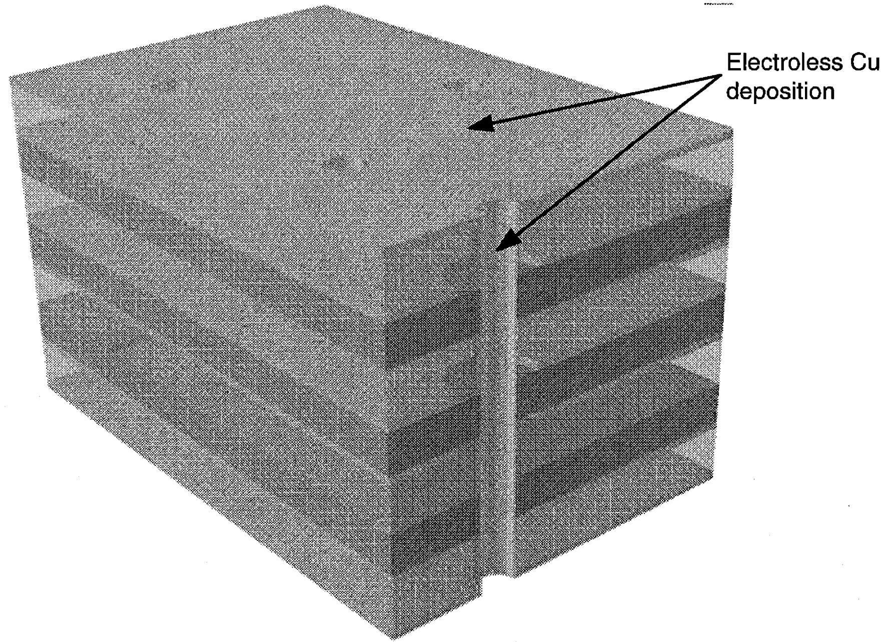

Figure A-5: Electroless copper plating (seeding).

To prepare for the electroplating steps, another photosensitive resist layer is applied using a lithography process. This process leaves the outer traces and via pads exposed, as shown in Figure A-6. These exposed areas are then plated using an electroplating process, in Figure A-7. This final build up of copper adds approximately 25 to 40μm thick.

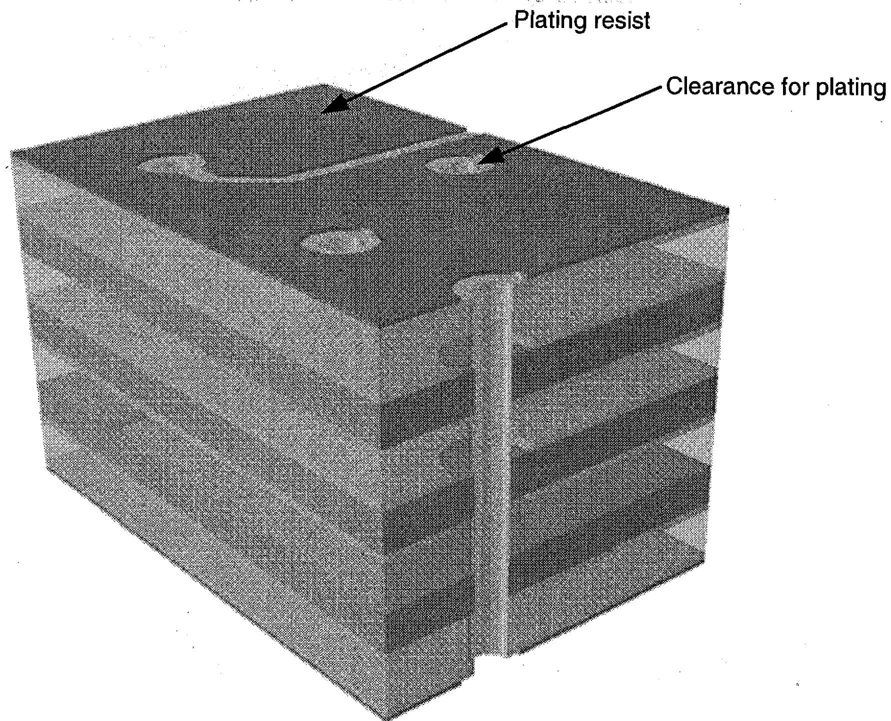

Figure A-6: Resist application.

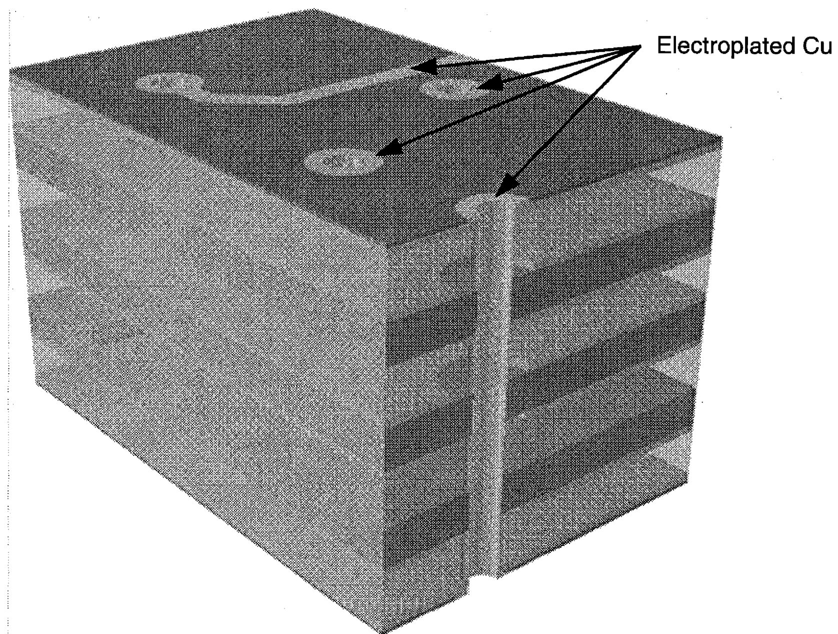

Figure A-7: Copper electroplate

Before excess copper can be etched away, all exposed copper surfaces are plated with tin or tin/lead (see Figure A-8) to establish a resist barrier. The remaining photosensitive resist is then removed and the exposed copper is etched away (as shown in Figure A-9 and Figure A-10,

respectively), leaving just the desired conductor structures. The tin/lead etch resist can now be removed (if desired) as shown in Figure A-11.

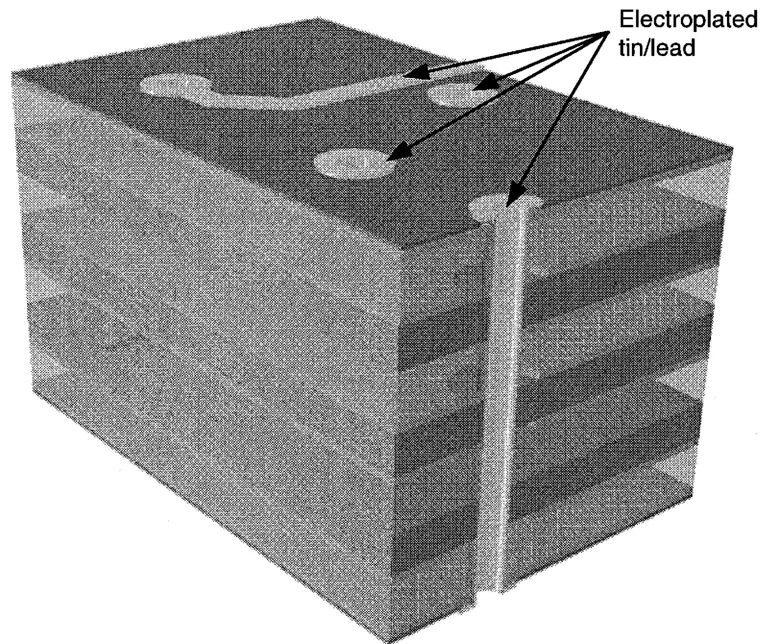

Figure A-8: Tin/lead etch resist.

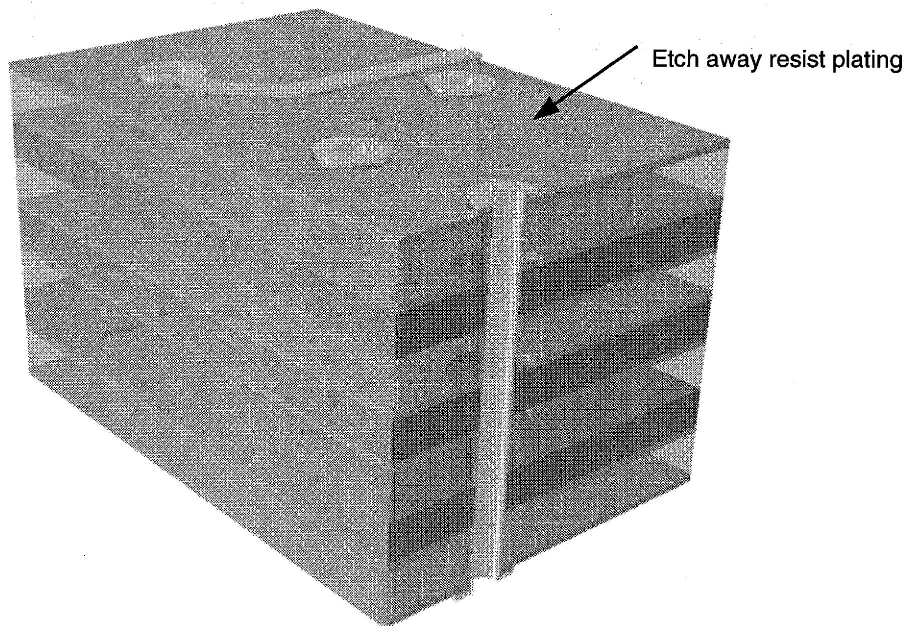

Figure A-9: Strip resist

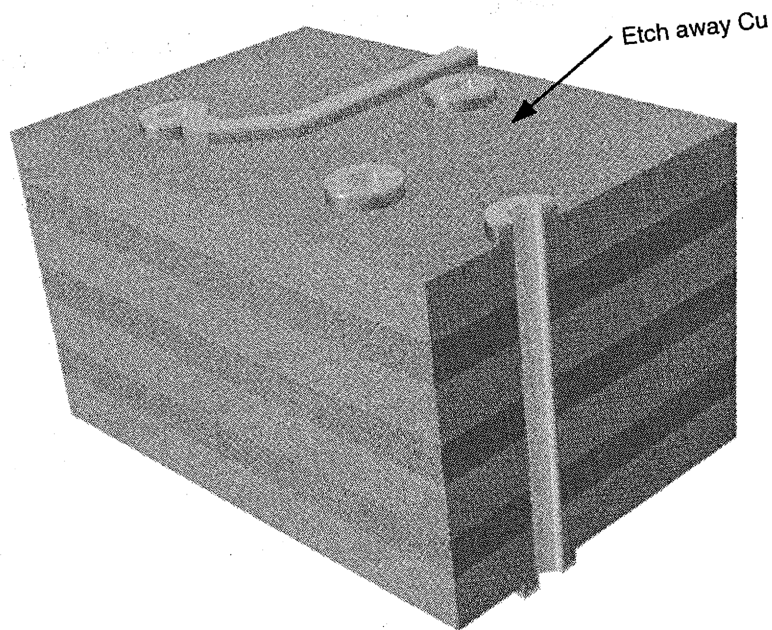

Figure A-10: Copper etch.

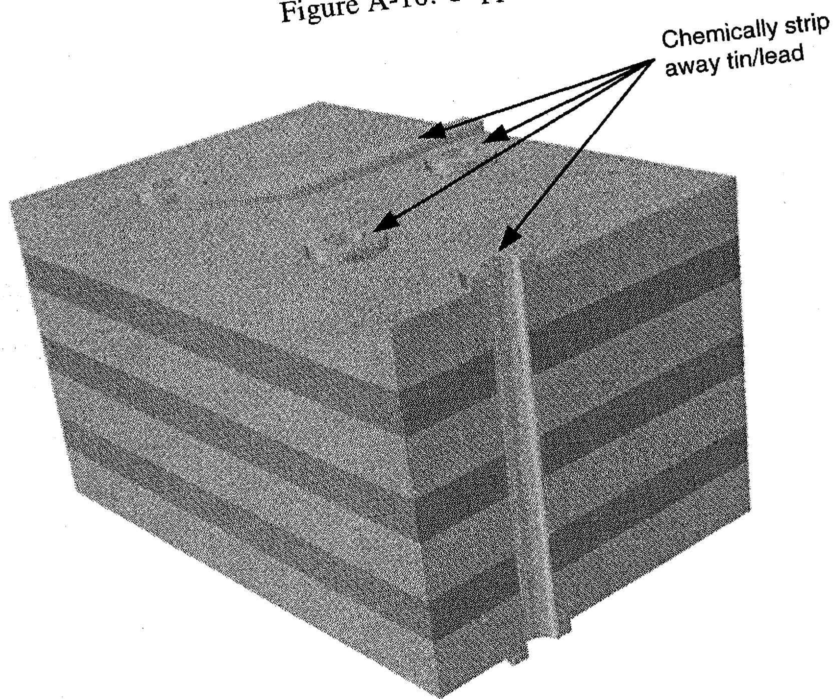

Figure A-11: Strip tin/lead.

The final step in finishing the multi-layer PCB and preparing for assembly is screening on a polymer solder mask, as shown in Figure A-12. The solder mask protects the outer traces and controls solder flows. In addition, it isolates areas that need further plating - typically requiring tin/lead plating to prevent corrosion and promote solder adhesion. In cases of separable

connection features, such as edge card connectors, gold plating is used to facilitate better conduction. These features are usually plated in two layers, using nickel with hard gold alloy (electroplate) or soft gold alloy (immersion plate).

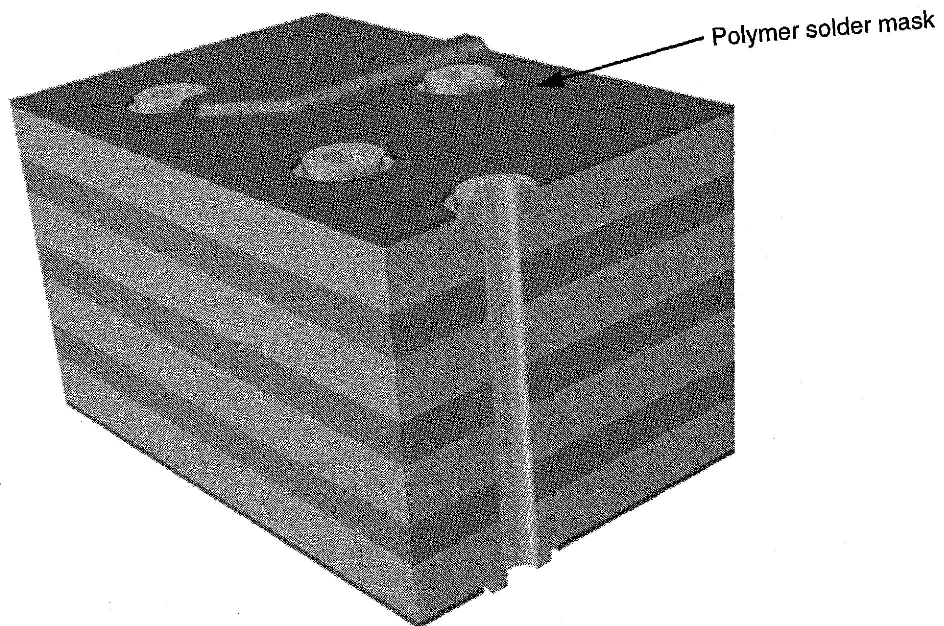

Figure A-12: Solder mask.

There are some final finishing steps like silk screening and routing that are not relevant to this project, and consequently, not discussed. For more information on these processes see [Flatt], [Dally] and [Coombs].

Appendix B

Understanding high frequency signal propagation

Keeping in mind that this thesis is intended for a mechanical design and manufacturing audience, it is desirable to provide a clear explanation of how high-frequency (HF) signals interact in circuit conductors. HF circuits behave very differently than the low-frequency circuits with which most mechanical engineers are familiar. "The higher the frequency, the greater the likelihood of a radiated coupling path; the lower the frequency, the greater the likelihood of a conducted coupling path." [Montrose]. In other words, HF signals take paths of least impedance, not the least resistance paths of low-frequency signals. In this section, the relationship between the geometry parameters is explored on a qualitative level of transmission line theory. A good qualitative introduction to HF signal physics is also given by [King et al.]. This introduction provides the foundation required to interpret the results of the presented simulation and experimental data. In order to simplify the visualization of these relationships, a physical analogy is developed.

Electrical signals can be visualized as fluid flowing in open canals, where the fluid represents the electrical wave and the canal represents the electrical conductor. Imagine water suddenly released from sluices into an empty canal system. The wave front of water passing through the system is very similar to a HF electromagnetic wave pulse. It should be noted that the analogy is an imperfect one, but is selected in this context for its ease of visualization. To take this analogy a step closer to real HF signal function, visualize a system of completely enclosed, fluid-filled tubes (or even solid bars of material) with acoustic waves passing through them.

HF circuit elements can therefore be mapped to canal features that provide similar functionality. The primary element of the HF circuit is an impedance-controlled transmission-line structure, such as those presented in Figure 1-3 and Figure 1-4. The important thing to understand is that the fields travel through the dielectric between the surfaces of the conductors. In a simple and uniform canal, as shown in Figure B-1, the canal width corresponds to the circuit impedance, and fluid energy losses map to dielectric losses. In this simple structure, as in a transmission line of uniform cross-section, a wave front would pass through without reflecting waves back towards the source, and system losses would cause energy leaving the structure to be lower than energy coming in.

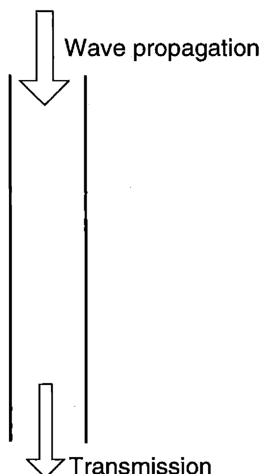

Figure B-1: Ideal transmission element: a straight, constant-section, continuous canal.

Before going forward, it is important to understand one item in the circuit designer's toolbox, the scattering parameter (S-parameter). In general, HF circuit designers are most concerned with the strength and quality of the signal being transmitted by the structure. Parameterizing the energy flux at circuit reference points (ports) for a given frequency is very advantageous for understanding this transmission. While there are different types of parameters, the S-parameter is most often used. S-parameters describe transmission element energy interactions in the frequency domain (i.e., S-parameters are computed or measured at one frequency). It is important to note that digital signals are almost never single frequency or perfectly sinusoidal. S-parameters are useful only when swept up through the maximum frequency bandwidth of the circuit. Interactions and losses are often frequency dependent, so S-parameters help by decomposition to illustrate these dependencies. For more information on S-parameters, see [Balabanian and Bickart] or [Nibler].

A typical two-port element has the interactions shown in Figure B-2 and defined by the following equation:

$$[S]=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{B-1}$$

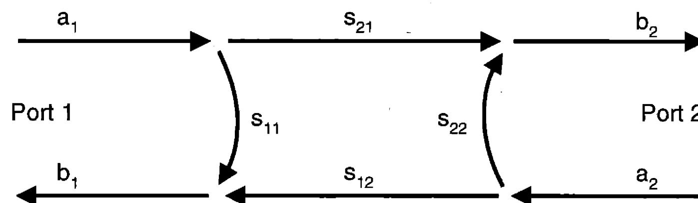

Figure B-2: Two port transmission element.

The port vector values, a_i and b_i, are defined as the incident wave amplitude and "reflected" wave amplitude, respectively. The relationship between the port vectors is:

$$\vec{b} = [S]\vec{a} \tag{B-2}$$

The magnitude of the vector has units of $\sqrt{VI}$ (where V is voltage and I is current). Therefore, $\left|\vec{a_i}\right|^2$ is the excitation RMS power at the ith port and $\left|\vec{b_i}\right|^2$ is the transmitted (or reflected) field RMS power at the ith port [Ansoft].

By relating some elementary canal features to HF structures, more complex structures can be described. First consider an impedance mismatch. As stated before, the canal width correlates to the transmission line impedance. Figure B-3 shows how the abrupt narrowing of a canal causes some of the wave to reflect back toward the source and reduces the transmitted wave energy. This is exactly what happens in impedance mismatched circuits, and is represented by an increase in the S_{11} parameter and a decrease in the S_{21} parameter. The increase and decrease effects, are greater at higher frequencies.

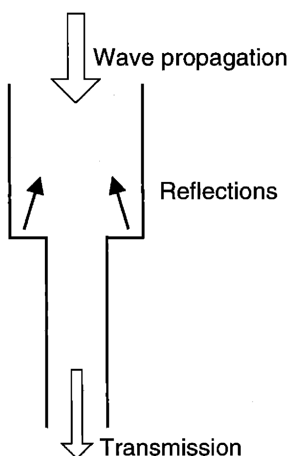

Figure B-3: Impedance mismatch: step change in canal section.

Now consider a discontinuous ground structure, such as a coaxial cable with a finite hole cut in the ground. This is a source of electromagnetic interference (EMI) to the environment. In the canal analogy, it can be thought of as a short break or porosity in the wall, as shown in Figure B-4. While it can be argued that a better analogy would be a flexible or elastic wall that absorbs energy as the wave pulse passes, a leak may be easier to visualize. The result is what is important. First, escaped fluid can flow into nearby canals causing new wave pulses in those canals. This corresponds directly to crosstalk, where noise in victim lines is generated by EMI leakage from neighboring sources (the offending source). Victim lines are more susceptible to crosstalk when they too are porous, a condition called reduced immunity [Montrose]. An additional leak result is the loss of energy from the wave front, which shows up in the two-port S-matrix as a decrease in the transmission term S_{12}, and depending on the severity of the leak, as some reflection.

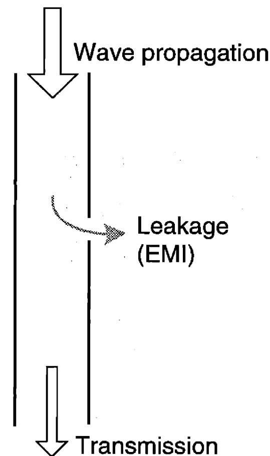

Figure B-4: Discontinuity in ground structure: an opening in the canal wall.

The next transmission feature is a "stub". Figure B-5 shows a branch that is short, narrow (on the scale of the circuit) and ends abruptly. This is equivalent to a short, un-terminated line (i.e., any extension of a conductor that does not make a complete circuit, and is short compared to the wavelength). When the wave comes to the intersection, it splits proportional to the path size ratios. This spilt effectively decreases the line impedance causing the first reflection back to the source. Once the wave reaches the end of the stub, all of the wave energy in the stub returns to the intersection. Here, it sends waves both back to the source and down the transmitted side; and because it is out of phase with the desired wavefront, it shows up as noise. If the stub length, L, is a multiple of one-quarter the wavelength of the signal, standing waves can be set up in the excitation or input signal (this is not, however, fully possible in this canal analogy with just one

wave front). Stubs do interesting things to transmissions and reflections, depending on the tuning of the stub. It is possible to have the stub reflection out of phase and almost equal in magnitude to the initial reflection at the split for a particular frequency (and typically at more than just one frequency of actual signal spectrum). The net result is a cancellation of the reflected energy (i.e., $S_{11} \rightarrow 0$). The nature of digital signals are, however, much broader in band, making it impossible to truly tune stubs.

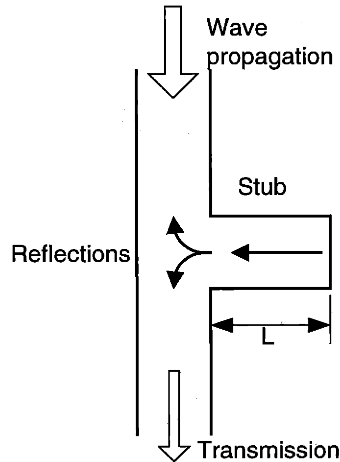

Figure B-5: Stub: a short terminating canal branch.

Stubs are often modeled as lumped elements, zero length devices made up of resistors, capacitors and inductors. As the size of the stub increases relative to the frequency, lumped parameter assumptions fall apart and features have to be modeled as distributed. An example of a simple stub is a 90° turn in a trace, this is why in circuit board trace designs it is very undesirable to make sharp turns, where as 45° or even rounded corners reduce or eliminate these stub reflections. In the canal model, lumped elements can be represented as small short reductions in the path, as shown in Figure B-6.

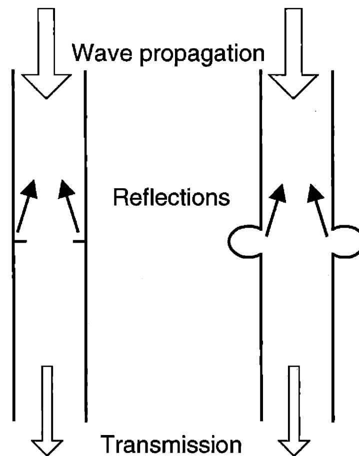

Figure B-6: Lumped element: very short obstruction or expansion in fluid path.

Having established all the basic elements, via structures can now be visualized using this canal analogy. First, consider a standard drilled and plated through-hole, as shown in Figure B-7. The signal wave is launched through an impedance-matched trace into the via, which has higher impedance (or a wider canal) than the input trace. The connection between the via and trace is at a right angle, which can cause reflection from the stub effect. As the wave transmits down the via, it periodically leaks through the dielectric layers because the ground plane structure is intermittent. Each leak causes reduced signal strength and reflection. The signal then exits the via and travels down another trace on a different layer at a sharp right angle. This trace impedance matches the original trace, which is a mismatch from the via, causing another reflection. In addition, the via extends above and below the traces, causing stub effects. Because the end of the via is not shielded, there is a strong EMI leakage into the environment, which broadcasts like an antenna to other devices.

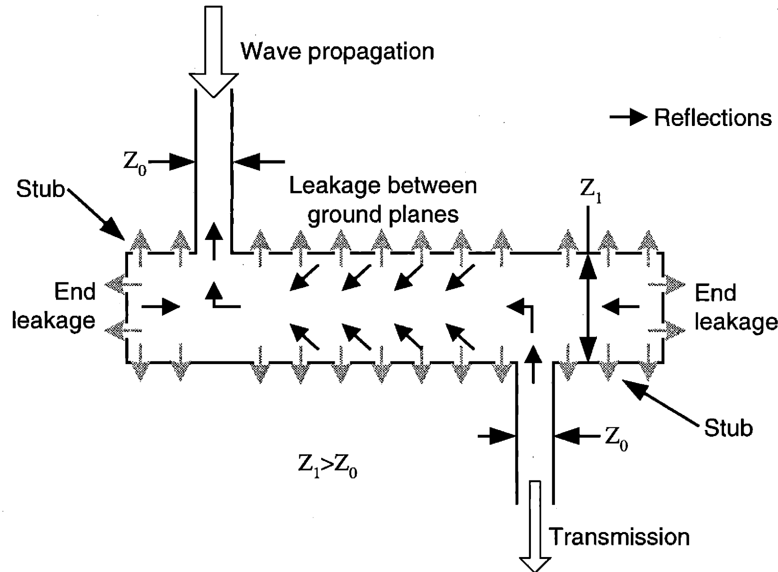

Figure B-7: Canal analogy applied to a conventional plated via.

Applying this same descriptive analysis to impedance controlled multi-connection vias helps to explain why their performance is better. In Figure B-8, a vertically-split via is modeled as a series of intersecting canals. Unlike the previous case, the impedance (or canal width) of the via is very close to that of the signal launching into it, thereby reducing or eliminating any resulting mismatch reflections. Because the via structure is not a completely enclosed waveguide, there is leakage at the gap. This leakage is continuous along the length of the via (as opposed to intermittent with the standard via), which reduces reflections from abrupt flow changes. In addition, the amount of leakage is significantly less, as shown on the field plots in Section 3.1.1.4. As with the standard via case, however, this system has end leakage and stub effects from the extension of the via above and below the two traces.

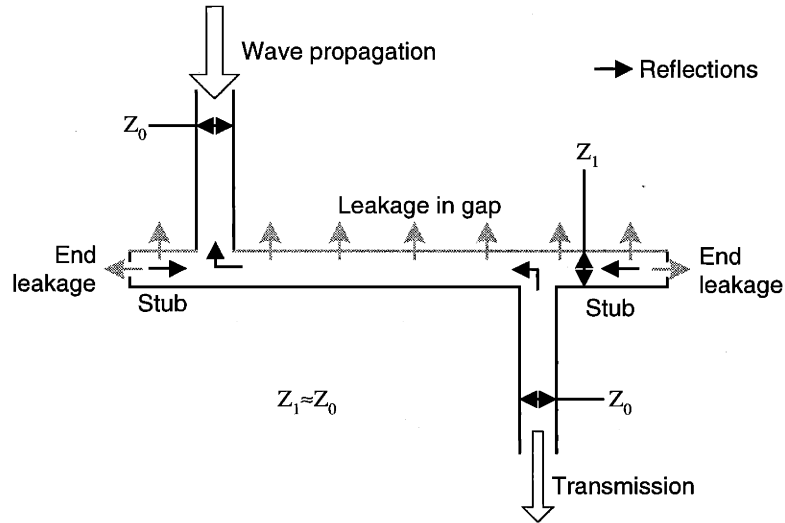

Figure B-8: Canal analogy applied to real impedance controlled via.

If the process can be developed (such as those in Section 6.3) to selectively remove plating in the via, the stubs can be eliminated, as shown in Figure B-9. By removing the stubs, the ends of the signal conductor can be shielded to eliminate via leakage above and below the PCB. Leakage would then be limited to the gap. This resulting structure represents the best achievable transmission and reflection from the co-cylindrical waveguide structure of a split or multi-connection via.

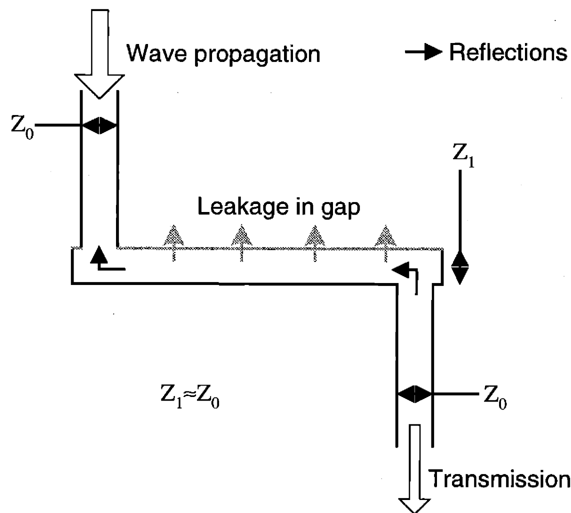

Figure B-9: In via trace.

The canal analogy has shown how different features of the via structure affect signal performance, and how changes to this structure can improve or eliminate some of the identified

problems. The analogy also explains why these systems have complex relationships with frequency.

Appendix C

Co-planer wave guide equations

Co-planer waveguide equations are relevant to multi-connection vias because they represent the impedance case were the via diameter is very large. This representation provides a glimpse at how the development of co-cylindrical waveguide equations would develop. The simplest co-planer waveguide case is the single-ended, infinite wide ground-conductor, and infinite thick substrate case, as depicted in Figure C-1. In fact, this case represents the large diameter co-cylindrical waveguide well, because the grounds connect together and the substrate is in the plane of the board making it very thick.

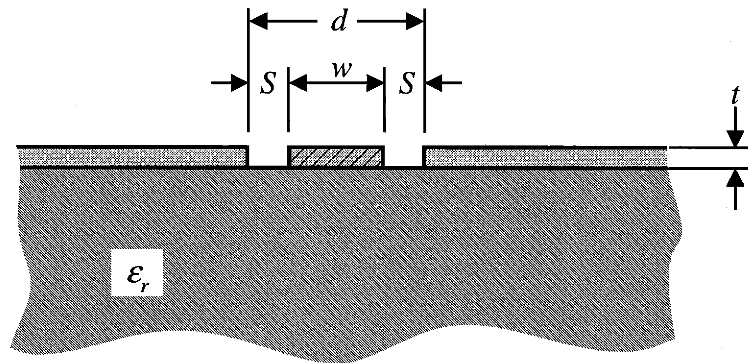

Figure C-1: Infinite wide ground, infinite thick substrate co-planer waveguide.

The general approach to this analysis is to use a conformal imaging method [Hoffmann]. Results of this method are presented below. The complete first order elliptical integral (*K(k)*) of the modulus *w/d* (equals *k*) as:

$$Z_L = \frac{Z_{L0}}{\sqrt{\varepsilon_{r,eff}}} = \frac{\eta_0 K\left(\sqrt{1-k^2}\right)}{4\sqrt{\varepsilon_{r,eff}} \cdot K(k)} \qquad \text{(C-1)}$$

In this case the thickness, *t*, is considered to be infinitely thin. η_0 is the permeability of free space (120π). The dielectric constant is averaged between the substrate and the air, yielding an effective dielectric constant:

$$\varepsilon_{r,eff} = \frac{(\varepsilon_r + 1)}{2} \tag{C-2}$$

By dividing the bounds, the formulation can be fit into two, more useful cases. The first case is when 0<*w/d*≤0.173 or $\eta_0 \leq Z_{L0} < \infty$:

$$Z_{L0} = \frac{\eta_0}{2} \ln\left(2\sqrt{\frac{d}{w}}\right) \tag{C-3}$$

Solving for modulus gives:

$$\frac{w}{d} = 4e^{-2Z_{L0}\frac{\eta_0}{\pi}} \tag{C-4}$$

And for 0.173≤*w/d*≤1 or $0 < Z_{L0} \leq \eta_0/2$:

$$Z_{L0} = \frac{\pi\eta_0}{4}\left[\ln(2) + 2\tanh^{-1}\left(\sqrt{\frac{w}{d}}\right)\right]^{-1} \tag{C-5}$$

Solving for modulus yields:

$$\frac{w}{d} = \left[\tanh\left(\frac{\pi\eta_0}{8Z_{L0}} - \frac{\ln(2)}{2}\right)\right]^2 \tag{C-6}$$

In addition to [Hoffmann] there are collections of various transmission elements in [Wadell].