Very-High-Frequency Low-Voltage Power Delivery

by

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Abstract

Power conversion for the myriad low-voltage electronic circuits in use today, including portable electronic devices, digital electronics, sensors and communication circuits, is becoming increasingly challenging due to the desire for lower voltages, higher conversion ratios and higher bandwidth. Future computation systems also pose a major challenge in energy delivery that is difficult to meet with existing devices and design strategies. To reduce interconnect bottlenecks and enable more flexible energy utilization, it is desired to deliver power across interconnects at high voltage and low current with on- or over-die transformation to low voltage and high current, while providing localized voltage regulation in numerous zones.

This thesis introduces elements for hybrid GaN-Si dc-dc power converters operating at very high frequencies (VHF, 30-300 MHz) for low-voltage applications. Contributions include development of a new VHF frequency multiplier inverter suitable for step-down power conversion, and a Si CMOS switched-capacitor step-down rectifier. These are applied to develop a prototype GaN-Si hybrid dc-dc converter operating at 50 MHz. Additionally, this thesis exploits these elements to propose an ac power delivery architecture for low-voltage electronics in which power is delivered across the interconnect to the load at VHF ac, with local on-die transformation and rectification to dc. With the proposed technologies and emerging passives, it is predicted that the ac power delivery system can achieve over 90 % efficiency with greater than 1 W/mm^2 power density and 5:1 voltage conversion ratio. A prototype system has been designed and fabricated using a TSMC 0.25 μm CMOS process to validate the concept. It operates at 50 MHz with output power of 4 W. The prototype converter has 8:1 voltage conversion ratio with input voltage of 20 V and output voltage of 2.5 V. To the author's best knowledge, this is the first ac power delivery architecture for low-voltage electronics ever built and tested.

Thesis Supervisor: David J. Perreault
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We have lots of memorable moments together and I am very happy to be with you. I love you.

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Chapter 1

Introduction

INTEGRATED low-voltage power delivery is drawing increased attention due to both the expanding personal electronics market and the increasing performance demands of computer systems. In addition, as the required supply voltages falls and the current demands rise, future computation systems pose a major challenge in energy delivery that is difficult to meet with existing devices and design strategies. Delivering large current over interconnects does not just cause efficiency problems, but also results in many other challenges, such as thermal management, voltage regulation, power density, interconnect (pin) bottlenecks and cost. To reduce interconnect bottlenecks and enable more flexible computation and energy utilization, it is desired to deliver power across the interconnect to the chip at high voltage and low current with on- or over-die transformation to low voltage and high current. This work presents elements for hybrid GaN-Si dc-dc power converters operating at very high frequencies (VHF, 30-300 MHz) for low-voltage applications, which include development of a new VHF frequency multiplier inverter suitable for step-down power conversion, and a Si CMOS switched-capacitor step-down rectifier. These are applied to develop a prototype GaN-Si hybrid dc-dc converter operating at 50 MHz. Additionally, this thesis exploits these elements to propose an ac power delivery architecture for low-voltage electronics in which power is delivered across the interconnect to the load at VHF ac,

with local on-die transformation and rectification to dc. With the ac power delivery architecture, voltage transformation can be achieved on die with an integrated matching network which only requires inductors and capacitors (no coupled magnetics are required).

1.1 Motivation

Currently, about 2% of the US electricity production is spent in powering computing infrastructure. This figure is about two times increase over the consumption from five years ago, and future projections are for a similar exponential increase, unless energy demands for power delivery and cooling are curbed. This overall demand for increased system level power is coupled with acute challenges in chip level power delivery and heat removal. For example, according to the International Technology Roadmap for Semiconductors (ITRS) 2011, the current drawn by high performance microprocessors is over 150 A now and will be increased to over 200 A by 2020 (Fig. 1-1). Fig. 1-2 shows the power delivery structure for voltage regulator and processors. From the Intel Voltage Regulator Module (VRM) Design Guidelines [2] [3], Fig. 1-3 shows the Intel processor platform power delivery impedance model example based on the current Intel processors' design requirement. Even with the 0.8mΩ board parasitic resistance, the interconnect causes over 10% of power loss. And this did not even consider the much higher conduction loss from the interconnect on the silicon.

Not only the number of transistors on integrated circuits doubles every 18 months as predicted by Moore's law, Fig. 1-4 shows that the Intel CPU pin count also grew exponentially over years. Moreover, power delivery competes with computation and signal communication for precious interconnect resources of wiring and interconnect pads, about 2/3 of the total pins in the package are used for power and grounds nowadays [4], and this requirement increases with higher current.

Chip power has increased greatly, and is effectively at or near the air cooling

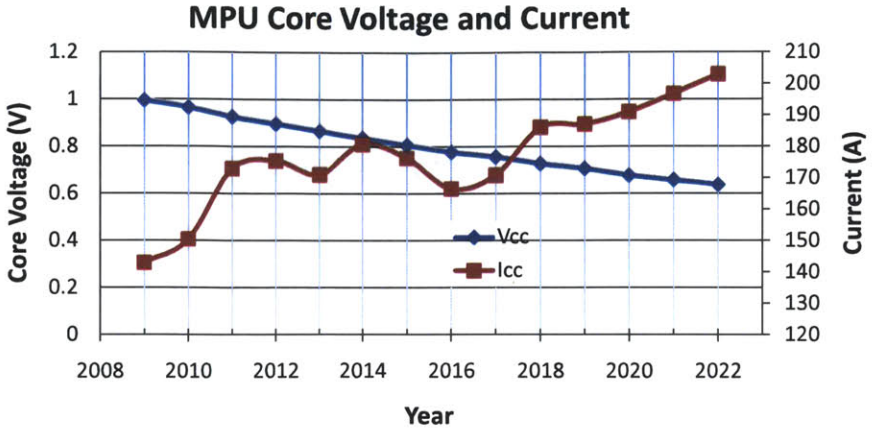


Figure 1-1: International Technology Roadmap for Semiconductors (ITRS) 2011. *http://www.itrs.net/Links/2011ITRS/Home2011.htm*

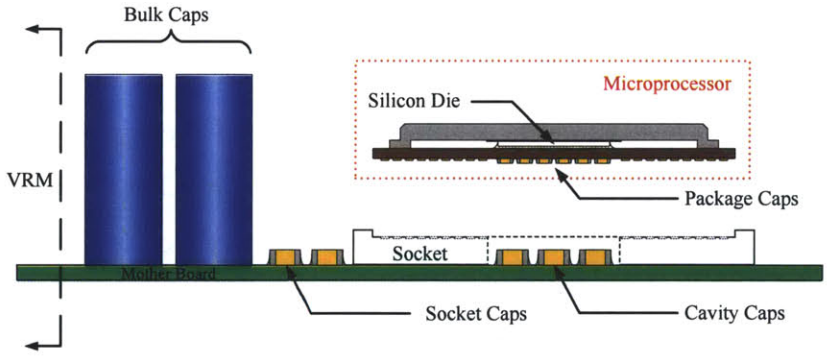


Figure 1-2: Current power delivery structure for voltage regulator and processor.

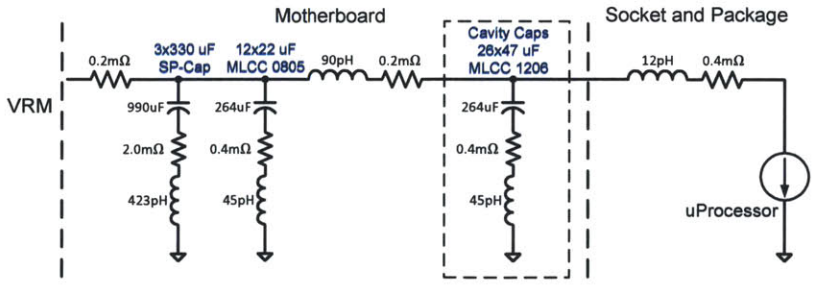


Figure 1-3: Intel processor platform power delivery impedance model path.

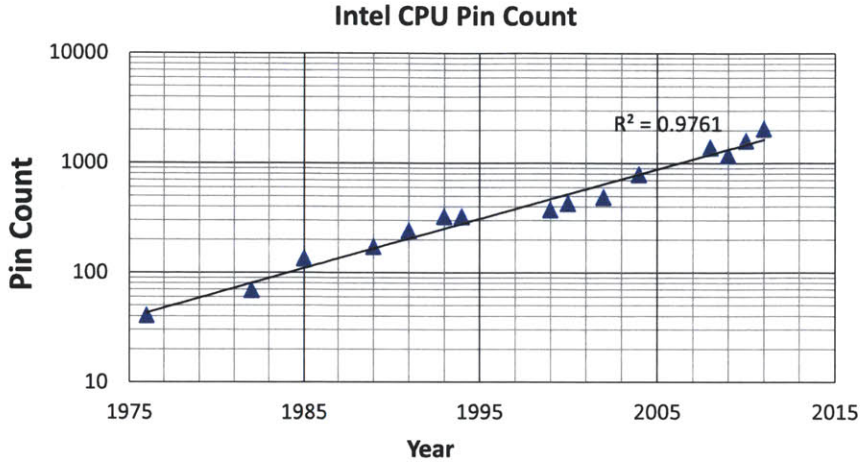


Figure 1-4: Intel CPU pin count history.

limit of approximately 100 W/cm^2 [5]. The need to deliver increasing current and achieve higher performance (including communications on and off die) limit represents a major challenge in CMOS scaling and IC packaging. This overall demand for increased system level power is coupled with acute challenges in chip level power delivery and heat removal. the ITRS projects as much as a factor of two increase in current, wider operating ranges and tighter voltage tolerance requirements, each of which strains the power delivery and management system. Likewise, the continued anticipated rise in operating frequency (about 8% average annual growth rate, limited mainly by power management tradeoffs) demands faster power supply transient response, which becomes increasingly untenable with the current off-chip regulation methodology. Also, the trend towards increasing functional diversity and computation with larger numbers of cores creates a desire for regulation and adaptation of voltages locally on-chip.

In order to reduce the interconnect loss and ease the limitations on pin count challenge, it is desired to deliver power across interconnects at high voltage and low current with on- or over-die transformation to low voltage and high current, which providing localized voltage regulation in numerous zones. In doing this, voltage con-

version ratios from 4:1 to more than 12:1, power conversion densities from 1 W/mm^2 to above 10 W/mm^2, and efficiencies to be greater than 90% are desired for local on-die conversion depending on system type.

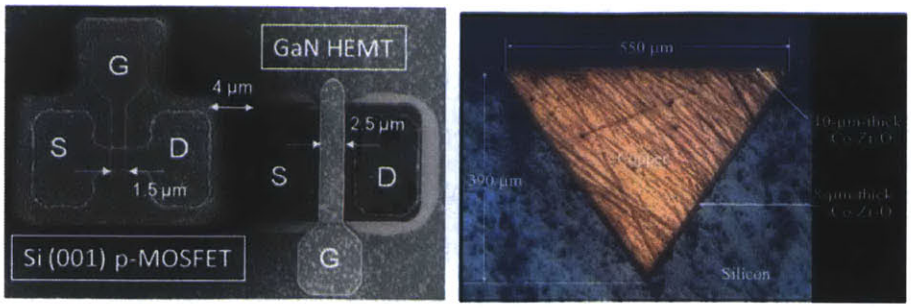
These needs have not been met by any proposed conversion systems to date [6, 7, 8, 9]. Existing integrated converter approaches are only sufficiently power dense and efficient for small conversion ratios (e.g., 2:1). Meeting the necessary conversion, power density, and efficiency targets requires power converter switching frequencies at many tens of megahertz and above, based on energy storage density considerations. On-chip Si transistor designs are capable of either efficient high-frequency switching speed or high blocking voltage, but not both. New approaches to power converter and delivery need to be developed to break this trade-off.

Equally important are challenges associated with powering the myriad low-voltage electronic circuits in use today, including portable electronic devices, digital electronics, sensors and communication circuits among many items. These applications all require delivery of power at very low voltages (e.g., 0.5 - 3.3 V), often from much higher input voltages (e.g., $\geq$5 V). The size and cost of the power conversion electronics (dc-dc converters) for these applications are important, limits overall system design. There is thus an evident need for advances in power conversion at low output voltages.

1.2 VHF Low-Voltage Power Delivery

1.2.1 Introduction

To overcome the barriers, we propose to develop conversion architectures and topologies based around use of both GaN power devices and Si CMOS transistors. These devices may be integrated monolithically or used together in a hybrid fashion. GaN power devices offer high blocking voltage, fast switching, and low loss at high voltage while Si CMOS devices offer high speed and low loss at low voltages. We will de-



(a) GaN on Si (MIT) (b) V-groove Inductor (Dartmouth)

Figure 1-5: Integrated GaN power device with CMOS (photo courtesy, Prof.Palacios, MIT) and low loss inductor for VHF operation and 3D integration (photo courtesy, Prof.C.Sullivan, Dartmouth).

velop power delivery architectures that leverage these device characteristics to provide power delivery solutions having unprecedented performance. This work leverages advances in GaN-on-Si power devices (Fig. 1-5(a)) and emerging magnetic component technologies [10] (Fig. 1-5(b)).

Fig. 5-1 shows the three major blocks of a dc-dc converter: inverter stage, transformation stage and rectification stage. A conventional buck converter has no transformation stage, so the inverting and rectifying devices each see both high current and high voltage, making this approach unattractive for high-conversion-ratio on-die dc-dc converters. And for high-conversion-ratio buck dc-dc converter, the PWM control requires very small duty ratios, which also brings great challenges for control circuitries. Topologies with a transformation stage (e.g. coupled-inductor buck, flyback, etc.) can operate using only low-voltage rectifier devices, which may be operated at very high switching frequencies ($\geq$ 30 MHz). However, these topologies require coupled magnetics (or transformers) which are not readily realized on die. Moreover, the inverter devices still operate high voltage, such that very high operating frequencies cannot be achieved with conventional topologies and devices. Magnetics based large-conversion-ratio dc-dc converters integrated on die in CMOS thus represents a major challenge. (Not considered here are switched-capacitor circuits [6] [7] and mixed capacitor-inductor circuits [11, 12, 13], which may represent excellent

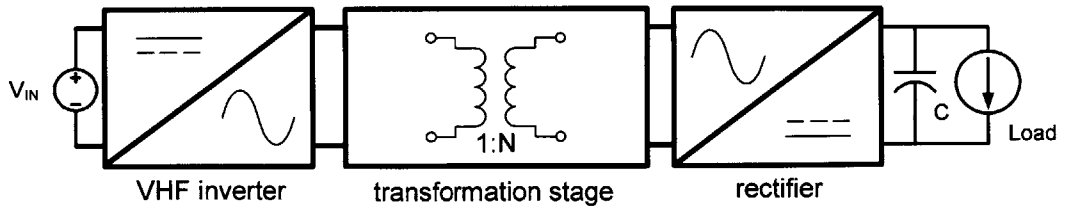


Figure 1-6: General architecture of a dc-dc converter.

opportunity, but as yet have not proven themselves at high conversion ratio.)

1.2.2 VHF Dc-dc Conversion

To obtain VHF dc-dc conversion with high step-down ratio, very high-frequency step-down circuit blocks are preferred for the major stages in a dc-dc converter. In this thesis, the novel frequency multiplier inverter and switched-capacitor rectifier are first presented for step-down power conversions. The normal high-frequency resonant inverters, such as class-E power amplifiers [14, 15, 16, 17] have step-up voltage conversion ratio from the input dc voltage to the ac output voltage, which is not suitable for voltage step-down applications. The new frequency multiplier inverter in this work does not just provide a step-down voltage conversion ratio, but also provides frequency multiplication. The individual device in the inverter only needs to be switched at half of the output frequency and switching loss can be reduced. Conventional half-bridge rectifiers also have the step-up voltage ratio from the input fundamental ac voltage to the dc output voltage. In this work, a switched-capacitor rectifier is proposed to provide a step-down voltage conversion for the converter. Coupled with a current-drive source, low-loss and high step-down rectification is realized. Implementation in CMOS with appropriate controls results in a design suitable for low-voltage very-high-frequency conversion.

The matching network transformation stage, the GaN frequency multiplier and the low-voltage integrated CMOS switched-capacitor rectifier can be combined to create a complete dc-dc converter. The proposed converter structure is shown in

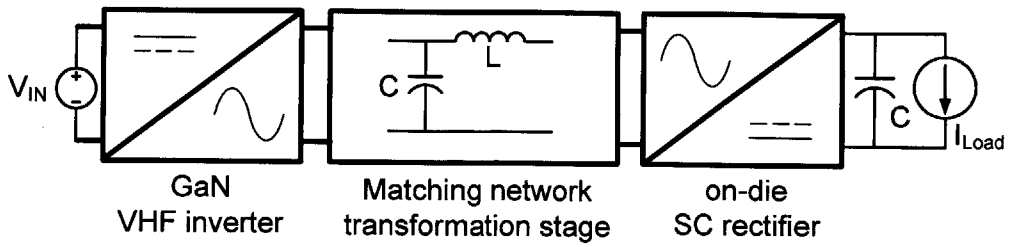


Figure 1-7: Proposed high power density high step-down ratio dc-dc converter architecture.

Fig. 5-7. The frequency multiplier inverter and the switched-capacitor rectifier both provide voltage step-down conversion ratio to reduce the burden in the matching network transformation stage. The matching network transformation stage provides high power-density voltage conversion and separates the rectifier stage from the high input voltage. In this case, high-speed high-voltage GaN device can be used in the high voltage inverter stage and high-speed low-voltage CMOS devices can be used in the rectifier stage. The GaN frequency multiplier converts the high input dc voltage into VHF ac output with a step-down conversion ratio, and then the matching network isolates the high-voltage input from the low-voltage load and provides additional step-down voltage conversion. Lastly, the switched-capacitor rectifier converts the rf ac power back to dc output for the load, while providing further voltage step down. With the possible GaN-on-Si technology, this architecture can also provide a fully integrated dc-dc converter solution for low-voltage applications.

1.2.3 Ac Power Delivery

To reduce interconnect bottlenecks and enable more flexible computation and energy utilization, it is desired to deliver power across the interconnect to the chip at high voltage and low current with on- or over-die transformation to low voltage and high current. With a remote inverter stage, our proposed GaN-Si converter architecture with matching network transformation stage can provide desired characteristics described above. Fig. 1-8 shows the ac power delivery architecture. This power delivery architecture leverages high-voltage power devices (which may be off die) and

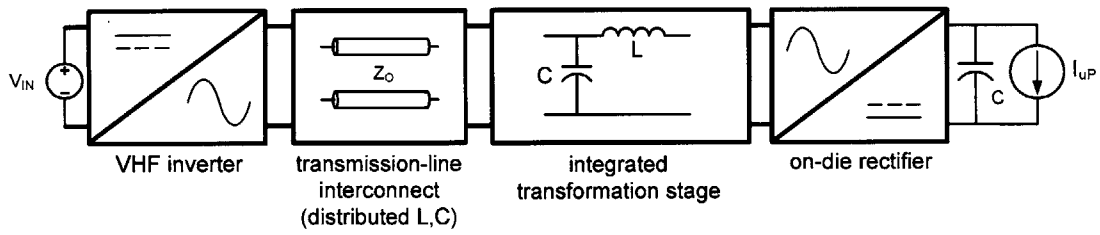


Figure 1-8: Ac power delivery architecture.

low-voltage integrated Si CMOS devices. It takes advantage of a transformation stage using integrated inductors to provide integrated power delivery.

GaN devices can be used in the high-frequency inverter stage to convert high-voltage dc input to a high-voltage and low-current ac output; and this high-voltage low-current ac power is delivered across the interconnect. On or over the die, matching network transformation stage transforms this high-voltage ac power into low-voltage ac power. Lastly, the low-voltage CMOS rectification stage converts the high-frequency low-voltage ac power back to low-voltage dc output for application use. A version of this general ac power delivery idea has been proposed before [18], but without any enabling means of realizing the high-frequency on-die magnetic transformers that would be required. Furthermore, no experimental result of this kind of structure has ever been published. This thesis presents a detailed investigation of the achievable performance of such a system within currently available technology, along with a trade-off comparison among different implementation options. Polyphase ac power delivery is also considered. Analysis reveals that such a system is feasible, and that polyphase RF power delivery is advantageous.

1.3 Thesis Contributions

There are four major contributions of this thesis. The first is design, analysis and implementation of a new frequency multiplier inverter suitable for efficient operation at very high frequencies (VHF) for step-down conversion. The normal high-frequency

resonant inverters, such as class-E power inverters [14, 15, 16, 17] have step-up voltage conversion ratio from the input dc voltage to the ac output voltage, which is not suitable for voltage step-down applications. This new inverter has an output frequency of twice the individual device switching frequency and provides a 3:2 step-down voltage conversion ratio. The lower switching frequency in the inverter provides lower switching loss and extends the lower output power limit due to the device output capacitance. The step-down conversion ratio in the inverter can reduce the burden for the transformation stage in the converter and improve the performance for high step-down ratio converters. Both the experimental and simulation result from the 50 MHz prototype implemented with GaN-on-Si transistors demonstrates the high performance and wider output power range of this frequency multiplier compared to conventional resonant inverter topologies.

The second main contribution of this thesis is the design and implementation of the new CMOS switched-capacitor rectifier. The SC rectifier only requires low-voltage devices and the flying devices can be self-driven, greatly simplifying gate drive considerations for VHF operation. The multi-step structure of this SC rectifier is well-suited to implementation in low-voltage CMOS, and can provide multiple times higher voltage step-down ratios compared to conventional bridge rectifiers. High step-down ratio power converters can benefit from the high step-down voltage conversion ratio of the SC rectifier and achieve better performance. A 50 MHz full-bridge SC rectifier IC implemented in a TSMC 0.25 μm process is presented that validates the concept and demonstrates the feasibility of VHF CMOS synchronous rectification.

The third contrition of this thesis is the development of a hybrid GaN-Si step-down dc-dc converter architecture capable of operating at VHF frequencies. The hybrid GaN-Si dc-dc converter consists of a VHF GaN frequency multiplier inverter stage, a transformation stage and a switched-capacitor rectifier stage. With transformation stage - implemented with a matching network, the low-voltage rectifier stage can be separated from the high input voltage such that the high-voltage inverter stage does

not need to carry the high output current and the low-voltage rectifier stage does not need to see the high inverter voltage. The GaN-on-Si power devices in the inverter can be fabricated either on the same silicon die with the integrated magnetics and low-voltage CMOS rectifier to make a fully integrated dc-dc converter or on a different substrate but whole system is co-packaged together. The proposed dc-dc converter architecture is suitable for low-voltage portable electronics and applications where high power density and high voltage conversion ratio are desired. The hybrid GaN-Si dc-dc converter prototype was designed, built and tested with discrete GaN devices and integrated CMOS SC rectifiers. The system operates at 50 MHz to provide 8:1 voltage conversion ratio and 4 W of output power. The input dc voltage is 20 V and the output dc voltage is 2.5 V.

The last contribution of the thesis is an investigation of a very high frequency ac power delivery architecture for microprocessors and other low-voltage digital ICs. With remote inverters, high-voltage low-current ac power can be delivered across the interconnect into the silicon die. And integrated matching network and CMOS low-voltage rectifier converts the high-voltage ac into low-voltage dc for application use. With the proposed ac power delivery architecture, one can reduce the interconnect loss and pin-count burden that limits many modern digital devices. The integrated matching network and low-voltage CMOS rectifier can achieve over 90% efficiency with 6:1 voltage conversion ratio and over 1 W/mm^2 power density from the study based on 65nm CMOS process and emerging integrated thin film magnetics [10]. In addition, multi-phase VHF ac systems are also explored and developed to provide higher power density and better performance for the system. An integrated circuit (IC) prototype was designed and fabricated in a TSMC 0.25 μm CMOS process to validate the feasibility of the ac power delivery system. The prototype provides 8:1 voltage conversion ratio (20 V_{peak} ac input to 2.5 V dc output) and 4 W of output power with switching frequency of 50 MHz. To the author's best knowledge, this is the first power converter with ac power delivery architecture ever built and tested.

1.4 Thesis Organization

The thesis is divided into 7 chapters, including this introductory chapter. Chapter 2 overviews some possible architectures for very-high-frequency (VHF) high voltage conversion ratio power converters, including their design trade-offs and limitations.

Chapter 3 overviews some inverter architectures and proposes the frequency multiplier inverter for step-down power converters. The design limitations of the classic resonant inverters are discussed. The detailed design analysis and advantages of the frequency multiplier are also described. This chapter also presents the 50 MHz frequency multiplier prototype with EPC discrete GaN devices. The power devices are switched at 25 MHz and the inverter output frequency is 50 MHz. The measurement shows 92.5 % efficiency for the 5 W frequency multiplier.

Chapter 4 discuss the limitations of the conventional bridge rectifier for step-down power conversion and presents a new switched-capacitor (SC) rectifier architecture. This chapter first shows the detail analysis of the operation of a two-step switched-capacitor rectifier and then expand this analysis for the general multi-step switched-capacitor rectifier architecture, including the driving scheme for the switched-capacitor rectifier. Furthermore, the design of a two-stage SC rectifier integrated circuit prototype built in TSMC 0.25 μm CMOS process is shown. This chapter concludes with the experimental result of the IC prototype operating at 50 MHz.

Chapter 5 demonstrates a complete hybrid GaN-Si dc-dc converter. Three different types of prototype designs are presented: GaN-Si dc-dc converter with half-bridge switched-capacitor rectifier, GaN-Si dc-dc converter with isolated full-bridge switched-capacitor rectifier and GaN-Si dc-dc converter with isolated conventional full-bridge rectifier. All systems are operated at 50 MHz with 5 W of output power. Detailed analyses and design trade-off among different systems are discussed. And measurement results are shown to verify the concept.

Chapter 6 introduces the ac power delivery architecture. With ac power deliv-

ery from remote inverters, high voltage and low current can be delivered across the interconnect into the microprocessors (or other digital IC) to save pin count and interconnect loss. This chapter also explores the multi-phase ac power systems. The design trade-offs for multi-phase matching networks for voltage transformation are also investigated and developed. Based on this investigation, we first show a 50 MHz discrete prototype to validate the high-frequency matching network and rectification. Next, we describe the design of a polyphase ac power delivery system incorporating an integrated circuit (IC) synchronous rectifier implemented in a TSMC 0.25 μm CMOS process. The chapter concludes with IC measurement results and the demonstration of the VHF ac power delivery architecture.

Lastly, chapter 7 summaries the contributions of the thesis and proposes some potential future directions for work on this topic.

Chapter 2

High Step-down Converters

Fig. 2-1 shows the schematic of the conventional buck converter. There is no transformation stage in the buck converter to provide additional voltage conversion (beyond that provided by the duty ratio of the pulse-width modulation). As a result, both of the power devices are required to block the high input voltage and carry the large output current. For large conversion ratios, this makes it difficult to utilize device characteristics advantageously. In addition, the narrow duty cycle in the buck converter limits its application for high step-down dc-dc conversion. For converters with large step-down conversion ratio, it is common to have a transformation stage (such as a transformer) in the converter to provide additional voltage conversion and better control. Furthermore, if isolation is provided, the transformer (and transformation ratio) can be used to separate the requirements of the high-voltage (inverter) stage and low-voltage (rectifier) stage; this enables one better to leverage the power device characteristics and provide better performance for the converters. For example, in order to utilize the high blocking voltage and fast switching characteristics provided by GaN devices, GaN devices can be used for inversion to block high-voltage but carry low current. On the other hand, we can leverage low-voltage CMOS devices for rectification for their high speed. There are numerous possible topologies that can obtain advantages using a combination of GaN and Si devices.

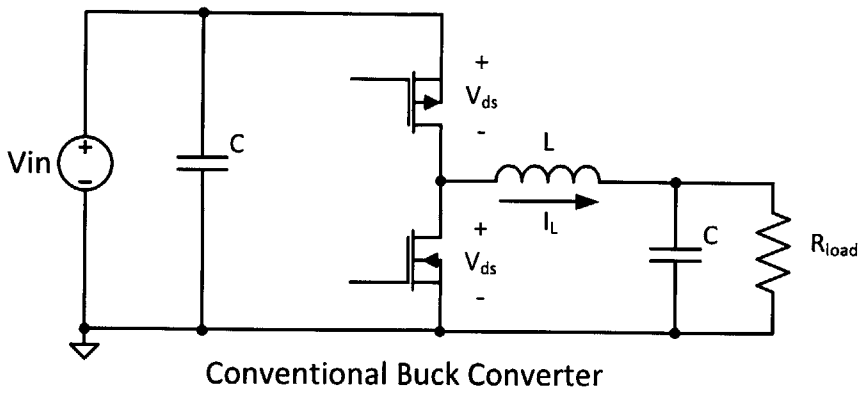


Figure 2-1: Conventional buck converter schematic.

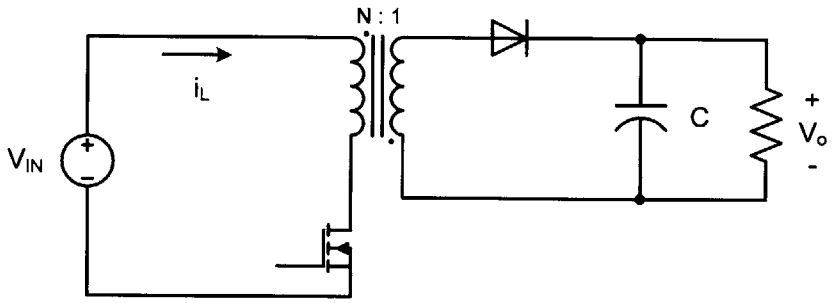


Figure 2-2: Flyback dc-dc converter schematic.

2.1 Flyback Converter

The flyback converter is used in both ac/dc and dc/dc conversion with galvanic isolation between the input and output(s). More precisely, the flyback converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage is transformed from primary to secondary with an additional advantage of isolation. The schematic of a flyback converter can be seen in Fig. 2-2. Although the two-winding magnetic device is represented using the same symbol as the transformer, unlike the ideal transformer, the magnetizing inductance is used to store energy, and current does not flow simultaneously in both windings of the flyback transformer.

The operation of the flyback converter can be seen in Fig. 2-3. The behavior of most transformer-isolated converters can be adequately understood by modeling the physical transformer with a simple equivalent circuit consisting of an ideal transformer

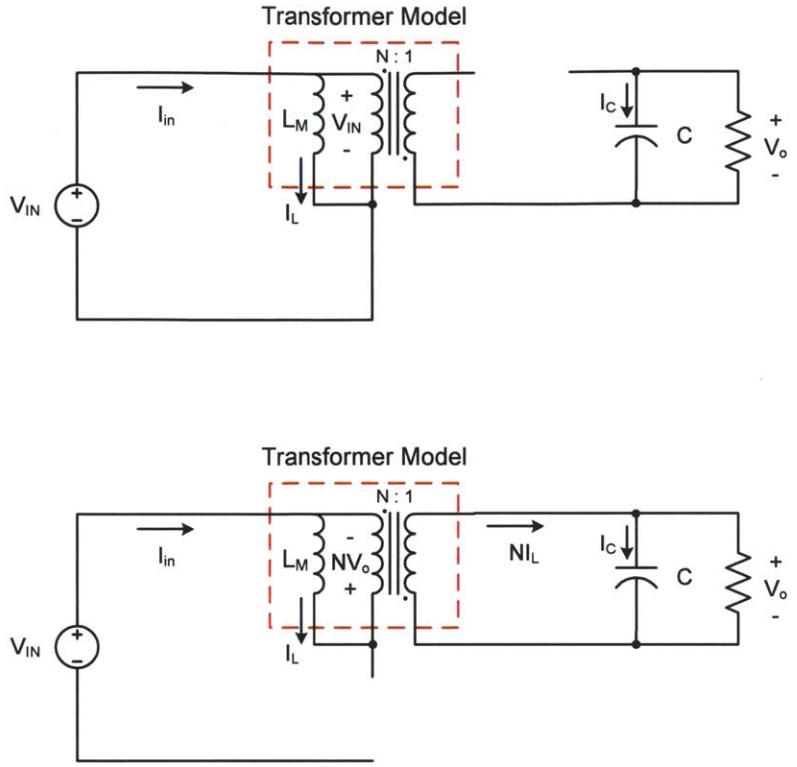


Figure 2-3: Flyback dc-dc converter operation.

in parallel with the magnetizing inductance. The magnetizing inductance must then follow all of the usual rules for inductors; in particular, volt-second balance must hold when the circuit operates in steady-state. This implies that the average voltage applied across every winding of the transformer must be zero. When the transistor is on, the energy from the input dc source is stored in the magnetizing inductor L_m. The diode is off and the voltage across the inductor is V_{IN}. When the transistor is off and the diode conducts, the energy stored in the magnetizing inductor is transfered to the output. The voltage across the inductor is NV_o and the current in the secondary side isNI_L (N is the turns ratio of the windings).

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields

$$< v_l >= D(V_{IN}) + (1 - D)(-NV_o) = 0 \tag{2.1}$$

Solution for the conversion ratio then leads to

$$\frac{V_o}{V_{IN}} = \frac{D}{N(1-D)} \tag{2.2}$$

With this extra freedom N in the conversion ratio equation, the limitation of the duty ratio for high conversion ratio can be reduced. In addition, the high-voltage input can be galvanically isolated from the low-voltage output. As a result, a hybrid flyback dc-dc converter is one way that one could leverage the characteristics of GaN devices (high-voltage at high speed) and CMOS devices (low voltage, high speed). Fig. 2-4 shows the schematic of such a hybrid GaN/Si converter.

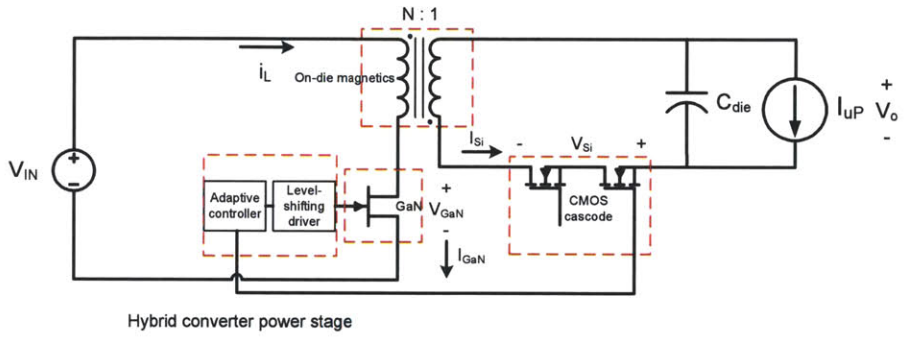


Figure 2-4: Hybrid flyback dc-dc converter schematic.

Consider the peak device voltage and current stresses one could ideally observe in such a topology:

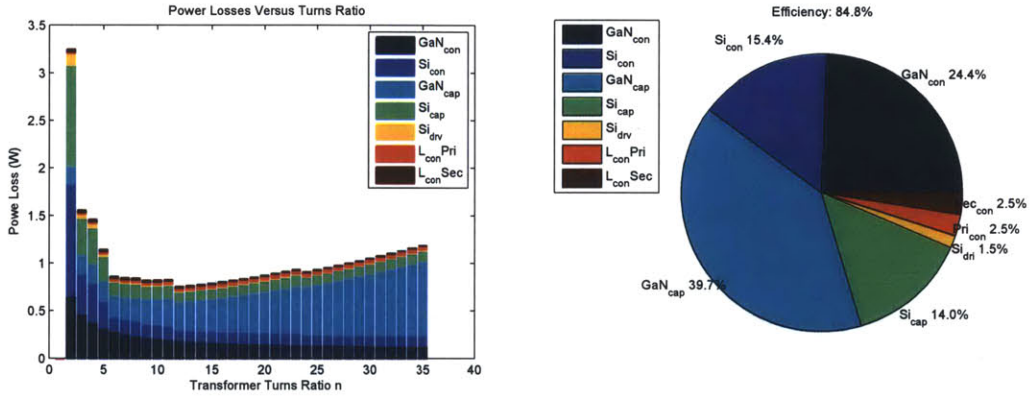
$$V_{GaN} = V_{IN} + NV_o; I_{GaN} = i_L \tag{2.3}$$

where N is the voltage conversion ratio in the transformer.

$$V_{Si} = V_{IN}/N + V_o; I_{Si} = Ni_L \tag{2.4}$$

From the above equations, one can see that the GaN device will block the large input voltage and N times the low output voltage, but it only carries the low input current. For the Si device, the cascoded pair of CMOS transistors together only need to block the low output voltage which is N times smaller than the input voltage, but it

carries N times the input current. In this case, the converter leverages the advantages of both devices. With given characteristics of both devices, we can further optimize the conversion ratio in the transformer to give the best performance in the converter. Fig. 2-5 shows a sample optimization for the flyback converter with 12 V input voltage and 1 V output voltage. The switching frequency is 100 MHz and output power is 5 W. The GaN device included in the optimization is commercialized CREE devices with V_{DSS} rating of 84 V. In addition, the optimization sweeps the Si process from 65 nm to 350 nm corresponding to different blocking voltages. And the Si CMOS device is also sized properly based on conduction loss and switching loss trade-off [19, 20, 21].



(a) Flyback Optimization Sweep

(b) Optimization result

Figure 2-5: Optimization for the flyback converter. GaN_{con} means the conduction loss in GaN device, Si_{con} is the conduction loss in the Si CMOS. GaN_{cap} and Si_{cap} are the capacitive loss for GaN device and Si CMOS respectively. Si_{drv} is the gate driver loss for the Si CMOS device. $L_{con}Pri$ and $L_{con}Sec$ are the winding loss for the transformer primary and secondary.

The optimization result shows that the optimal turns ratio for the transformer is 12:1 with magnetizing inductance of 36 nH. The blocking voltage of the GaN device is 24 V (a over-rated 84 V device CGH40035F was used since that was the lowest rating available at the time the optimization was undertaken). The Si CMOS device pair needs to block 2.0 V, which can be achieved by cascoding CMOS10SF IBM 65 nm devices [22]. In cascoded devices, we effectively connect a pair devices in series,

so on can achieve higher blocking voltage than with a single device (with a doubling of effective on-resistance). Importantly, the cascode pair can block two times higher voltage without changing the process, and normally the low-voltage process has better FOM (Ron·Qgd) and a higher switching speed than a single high-voltage device, making cascoding a good design choice in many instances. The optimized size for the Si NMOS device is 388000 μm. At an operating frequency of 100 MHz, a simulated efficiency of 84.8% is predicted, including the tapered gate driver loss for the Si NMOS device and estimated winding loss in the transformer based on the models for thin-film magnetics developed at Dartmouth (unit magnetizing inductance is 1 nH/mm, dc resistance is 0.91 mΩ/mm and the ac resistance is 3.82 mΩ/mm @100 MHz) [23]. Although the above result is very promising, constructing a practical integrated transformer is very difficult and switching ringing due to the leakage inductance in the transformer would need to be taken care of in a real design. A snubber circuit can be used to clamp the magnitude of the leakage inductor ringings to a safe level that is within the peak voltage rating of the transistor. However, this is inefficient at very high frequency operation. Another possible way is to make a resonant converter to absorb the leakage inductance in the transformer into the circuit operation; this will be discussed in section 2.3.

2.2 Modified Tapped Inductor Converter

A Tapped Inductor (TI) converter shares similar characteristics with the flyback converter in balancing device voltage and current stresses effectively [24, 25, 26, 27, 28]. Nonetheless this approach has similar challenges regarding transformer leakage. Also, driving the high-side device can be challenging at VHF frequencies. A Modified Tapped Inductor(MTI) converter is proposed in here that seeks to address at least some of these challenges. Fig. 2-6 shows the schematic of the modified tapped inductor converter. In this converter, the peak device stresses are:

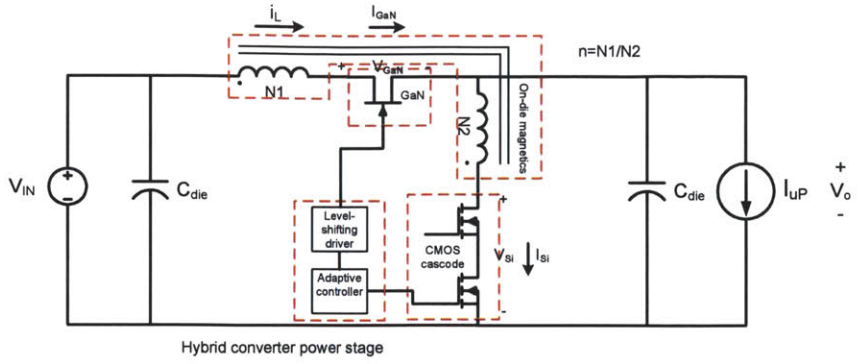


Figure 2-6: Modified tapped inductor converter schematic.

$$V_{GaN} = V_{IN} + (N_1/N_2 - 1)V_o; I_{GaN} = i_L \tag{2.5}$$

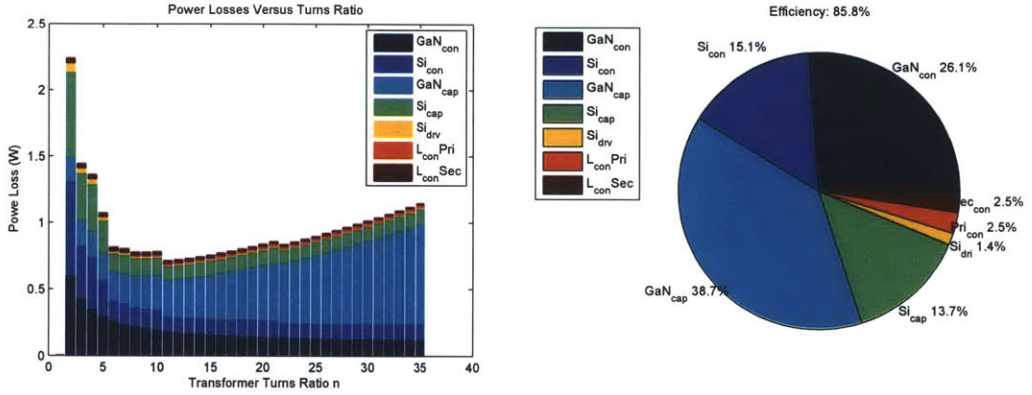
where n is the turns ratio of the tapped inductor.

$$V_{Si} = (V_{IN} - V_o)/(N_1/N_2); I_{Si} = ni_L \tag{2.6}$$

Similar to the flyback converter, the high-side GaN device blocks the large input voltage and the reflected output voltage from the the tapped inductor and carries low input current. The cascoded CMOS device pair in the low-side only needs to block the low output voltage and an additional function of the input voltage depending on the turns ratio in the tapped inductor. And the CMOS pair needs to carry n times of the input inductor current. The advantage of this modified tapped inductor converter is that the high-side GaN device is connected to the output DC node. This simplifies the gate driver design complexity of the high-side device since the control port of the device (the gate-source port) is not referenced to a flying node. And negative gate bias can be easily provided for the high-side GaN device if necessary (e.g., for a depletion mode device, or to reduce off-state leakage current). But this is limited to an output voltage which is greater than the negative bias of the high-side device. In terms of loss, the high-side device with a dc reference node can reduce the switching loss by preventing the well from floating. Since a level-shifting gate driver

is easy to implement in this case (dc level shifting rather than to a flying node), the gate drive requirements are considerably relaxed as compared to conventional TI converters. Also, in the case where an integrated Si device is used for the high-side transistor, an N-channel high-side device can be used to provide better performance, and well-capacitance losses for the high-side device are eliminated.

Again, a similar optimization process is used for the modified tapped inductor converter. The converter has input voltage of 12 V and 1 V output voltage. The switching frequency is 100MHz and output power is 5W. The optimization result is shown in Fig. 2-7.



(a) Modified Tapped Inductor Converter Optimization Sweep

(b) Optimization result

Figure 2-7: Optimization for the modified tapped inductor converter

The optimization result shows that the optimal turns ratio for the tapped inductor is 11:1 with magnetizing inductance of 33 nH. 100% current ripple ratio is used to achieve Zero-Voltage-Switching (ZVS) soft switching [29, 30, 31, 32, 33]. The blocking voltage of the GaN device is 23 V (an over-rated 84V device CGH40025F was used for the optimization since that was the lowest rating available at the time the analysis was undertaken). The Si CMOS device needs to block 2.0 V, which can be achieved by cascoding the CMOS10SF IBM 65nm devices. The optimized width for the Si NMOS device is 356000 μm. At operating frequency of 100 MHz, an idealized, simulated efficiency of 85.8% can be achieved, including the tapered gate driver loss for the

Si NMOS device and estimated winding loss in the inductor based on the magnetic models provided by Dartmouth.

The modified tapped inductor converter shows certain performance improvements compared to the flyback converter, but the ringing problems caused by the parasitics in the magnetics remain unsolved. A better topology is desired to better absorb parasitics in the converter and achieve better efficiency.

2.3 Multi-Resonant Modified Tapped Inductor Converter

The biggest challenge of the Modified Tapped Inductor converter is the magnetic design since the leakage inductance will cause series parasitic ringing when the switches are switching. This parasitic ringing will give high voltage/current stress for the devices and contributes to loss. A Multi-Resonant Modified Tapped-Inductor Buck Converter is proposed here to absorbed parasitics into the normal converter operation. This converter is related to others in the multi-resonant converter family [34].

The operation of the Multi-Resonant Modified Tapped-Inductor Buck Converter is similar to the Modified Tapped-Inductor Converter discussed above in section 2.2. Fig. 2-8 shows the schematic of the multi-resonant modified tapped-inductor buck converter. The leakage inductances in the tapped inductor are used as the resonant inductance to achieve ZVS. (An additional resonant inductor can be added in series with the device if necessary.) Also, the parasitic capacitance of the device is also absorbed as part of the resonant capacitance, and additional resonant capacitance can also be added in parallel with the devices as needed. Owing to the resonance between these elements, zero-voltage-switching is achieved, which reduces switching loss. But this does not come for free, since the devices will experience higher peak voltage and current stress during resonance.

Fig. 2-9 shows sample simulation waveforms of the multi-resonant modified tapped

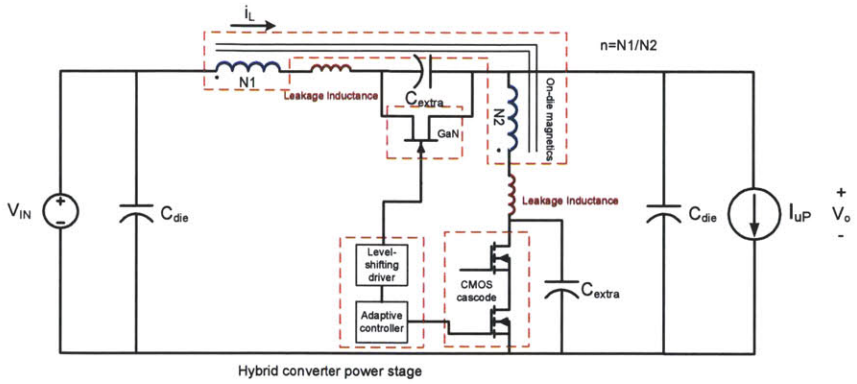


Figure 2-8: Multi-resonant modified tapped inductor converter schematic.

inductor converter with 1:1 transformer and 2:1 conversion ratio. Voltage waveforms are normalized to the input voltage to show device stress and drain-source current waveforms are also normalized to the output current. The simulation shows that the converter can achieve both zero-voltage switching (ZVS) and zero-current switching (ZCS) if the control timing and resonant components are chosen properly. But on the other hand, the normalized voltage and current waveforms also show that the devices will experience almost 2 times higher stress during resonance compared to traditional hard-switched converter topologies (under ideal conditions with no transformer leakage inductance). In order to further investigate this multi-resonant modified tapped inductor converter topology, a printed-circuit-board (PCB) prototype is built to verify the feasibility of the structure.

2.3.1 Prototype Experiment

A schematic of the prototype multi-resonant modified tapped-inductor buck converter is shown in Fig. 2-10. The input voltage of the converter is 3 V and the output voltage is 1.5 V. The switching frequency is 100 MHz and the output power is 0.5 W. Custom-made cascode devices were used for very-high-frequency operation [22]. The cascode devices were designed based on 3.3 V TSMC 0.35 μm process. The width of each device is 80000 μm, on resistance R_{on}=60 mΩ, gate capacitance C_{gs} is 65 pF

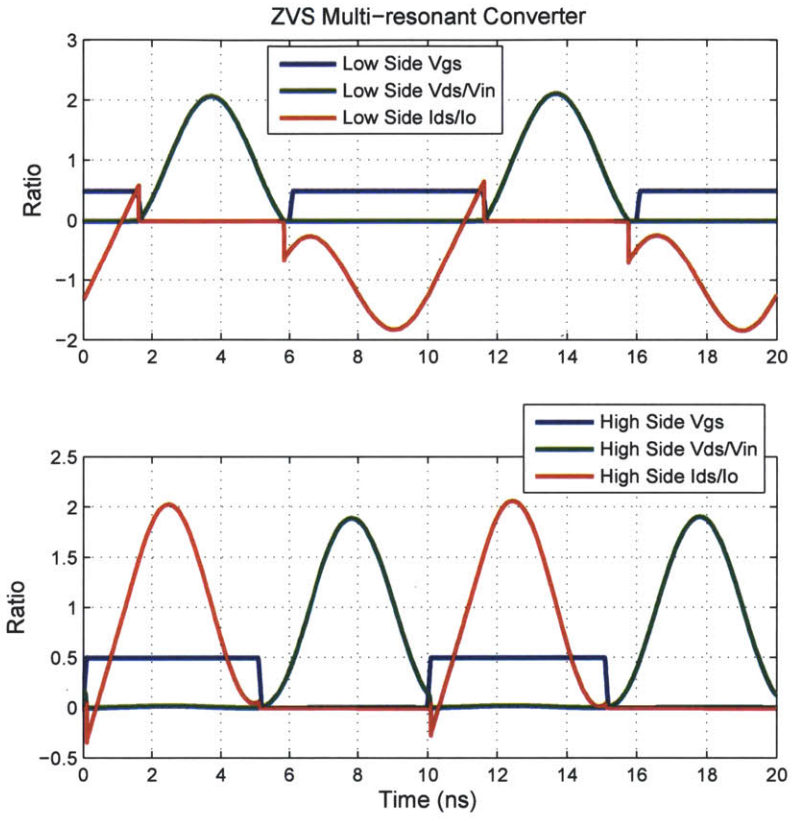


Figure 2-9: Sample simulated waveforms shows ZVS and ZCS transient in the multi-resonant modified tapped inductor converter. In the simulation, the input voltage is 6 V and the output voltage is 3 V. The output power of the converter is 3 W and the operating frequency is 100 MHz. The coupled inductor (transformer) has magnetizing inductance of 50 nH and leakage inductance of 2.5 nH. The shunt resonant capacitance across the cascoded devices is 110 pF.

and output capacitance C_{oss} is 47 pF. The built-in 7-stage gate driver has a taper factor of 4. The cascode device is designed to have 6.6 V breakdown voltage. A custom-made 1:1 transmission line transformer [35] is used to minimize the leakage inductance. This 4-turn transformer is made to have 35 nH magnetizing inductance for characteristic impedance matching and 4 nH leakage inductance for resonance (copper foil is used to reduce the ac resistance). The core is made of iron powder-17 material with a relative permeability of 4 (even though there is no core loss in air core transformer, which may provide better efficiency for VHF converters, it is not chosen for our design due to its weak coupling and relative large leakage inductance). Additional external 33 pF and 27 pF capacitors were added in parallel with the top and bottom power devices to resonate with the leakage inductance and achieve zero-voltage-switching. Additional 18 pF and 12 pF capacitances are added in parallel with the top cascode devices to obtain better voltage sharing between the cascoded devices. 1 ns overlap was added between the low-side gate signal and high-side gate signal to achieve better resonant operation.

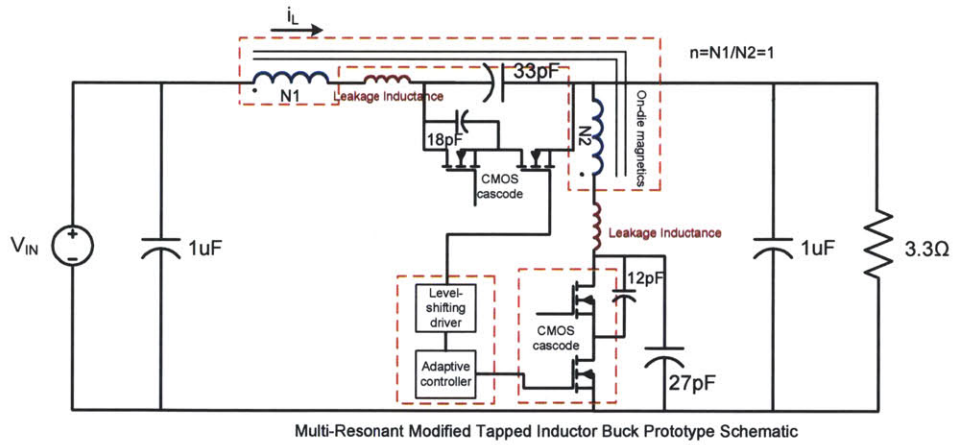


Figure 2-10: Multi-resonant modified tapped inductor buck converter prototype schematic.

A picture of the PCB prototype is shown in Fig. 2-11 and the measured waveforms are shown in Fig. 2-12. From the experiment waveforms, we can see that the ZVS is achieved for both devices at both turn-on and turn-off transition. In addition, the

measurement also shows that the cascoded devices share the blocking voltage evenly. The measured efficiency of the converter is 60 % since the power devices were not optimized for this application. (They were developed for another application, and were the only existing devices available that were suited for VHF power conversion at these frequencies and voltages. However, this prototype validated the multi-resonant modified tapped-inductor buck converter concept and prove the possibility to absorb the leakage inductance for resonant operation at VHF.

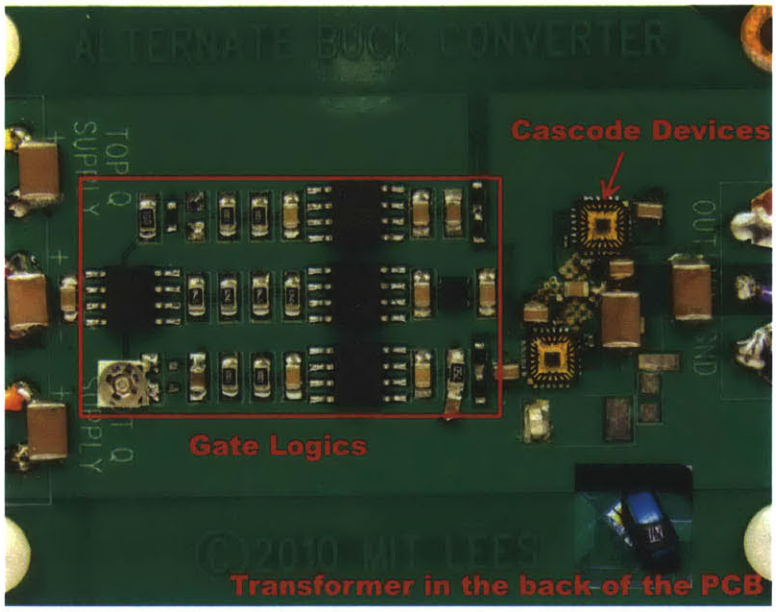


Figure 2-11: A picture of the multi-resonant modified tapped inductor buck converter prototype.

2.3.2 Summary

Even thought the experiment shows promising results, the multi-resonant modified tapped-inductor buck converter still faces several problems. First of all, the device stress does not scale linearly proportional to transformer turns ratio and conversion ratio. If a high conversion ratio is required, the low-side device will still have a voltage stress much higher than the output voltage. Higher transformer ratio can reduce the voltage stress for the low-side device and increase the voltage stress for the high-side

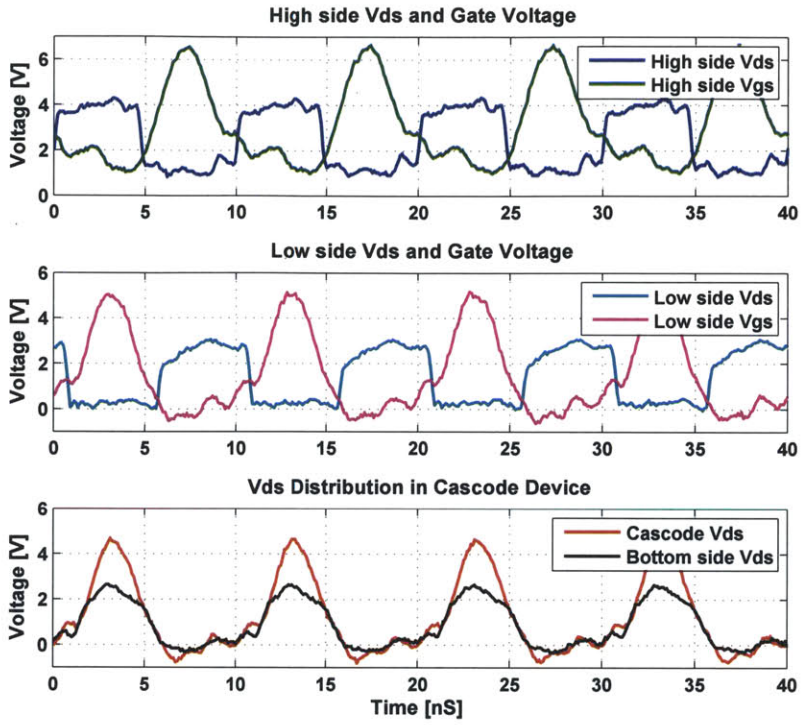


Figure 2-12: Measurement waveforms of the PCB prototype.

device. The impedance on both side of the transformer increases as the square of the transformer voltage conversion ratio. Since this is a resonant converter, the characteristic impedance of the resonant tank should be matched well with the converter. In addition, the resonant frequency should be at a certain fraction of the switching cycle to achieve ZVS/ZCS (or the resonant period should fit into the device on/off stage period). Given the top two conditions, the required inductance and capacitance in the resonant tank are set. This limits the design of the transformer since the minimum inductance is bounded by the leakage inductance in the transformer and the minimum capacitance is given by the parasitic capacitance in the device. In order to delivery more power, it requires relative lower characteristic impedance for the low-side resonant tanks, and hence has the possibility to lower the required leakage inductance to an unreasonably low level (simply increasing the capacitance to

Table 2.1: Multi-Resonant Converter Conversion Ratio Characteristic Summary

Variables	**Variation**	V_{out}	**Description**
Duty Ratio	↑	↑	Deliver more power to load
Load	↓	↑	Lower current, higher impedance
$L_{Highside_Resonant}$	↓	↑	smaller L, lower impedance in resonant tank
$L_{Lowside_Resonant}$	↓	↑	smaller L, lower impedance in resonant tank

Duty Ratio is for the high side device. When one variable is changing, all other variables remain constant.

lower the characteristic impedance will not work since it will also affect the resonant frequency). We normally assume that the leakage inductance is about 10% of the magnetizing inductance. This is a reasonable assumption in RF transformers, which are built with low permeability cores. As a result, in order to increase the impedance of the converter, we only can either reduce the power or increase the input voltage. Table 2.1 shows a summary of multi-resonant converter conversion ratio characteristics over other adjustable components in the converter. Some options are normally not available for a set industrial specifications. The Multi-resonant technique solves the parasitic ringing problem for VHF converter but with a high voltage stress for Si CMOS that may not be suitable for low-voltage power delivery in many cases.

2.4 Summary

In this chapter, we have described several possible architectures for VHF high-step-down power conversion. However, each different system has drawbacks. Both the flyback converter and tapped-inductor converter have the leakage inductance ringing problems at high-frequency. The conventional TI converter also has gate drive challenges. The multi-resonant modified tapped-inductor converter solves the leakage inductance ringing problem and the gate drive challenges, but it cannot scale suitably for high voltage conversion ratio applications. This thesis investigates techniques to overcome these problems and improve the three major stages (inverter stage, trans-

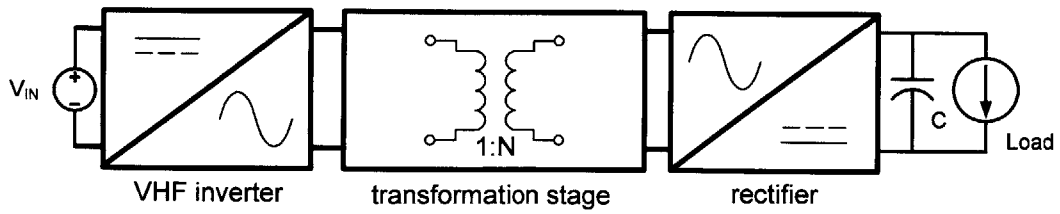


Figure 2-13: General architecture of a dc-dc converter.

formation stage and rectification stage shown in Fig. 5-1) in a dc-dc converter for high voltage conversion ratio low-voltage power conversion. Each of the improved blocks and the new power converter architecture will be described in detail in the following chapters.

Chapter 3

Frequency Multiplier Inverter

An inverter stage is the first stage of a dc-dc converter. It converts the dc power into ac power. Since the inverter is connected to the high-voltage input node in a step-down converter, we can leverage high-voltage low-current devices (such as GaN power devices) for inversion. However, there are several requirements for the inverter to be used for our applications. For step-down applications, step-down voltage conversion ratio from the dc input to the ac output fundamental is preferred to optimize the system performance. Moreover, In order to achieve high power density, small numerical values of passive components and wide control bandwidth, the switching frequency of the inverter needs to be pushed into very-high-frequency (VHF) range. In this case, zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) is preferred for the high-voltage inverter stage to reduce the switching loss. However, traditional resonant topologies useful at VHF, such as class E/F and class DE inverters [16] all show different limitations for the high-conversion-ratio low-voltage applications (e.g., step-up conversion ratio or device driving problems). In this chapter, we first overview several resonant inverter topologies and then propose a frequency multiplier inverter topology to provide step-down voltage conversion ratio and high performance at VHF for the high step-down applications.

3.1 Inverter Overview

Several inverters are reviewed here, and their application for high step-down ratio, low-voltage VHF converters is considered. The inverters considered include the conventional Class E inverter, Class DE inverter and Class DE inverter with Φ_2 network [36].

3.1.1 Class E Inverter

In the very-high-frequency range, Class E inverter is a widely favored candidate among all classes switching mode inverters due to its circuit simplicity , ease of design and ability to absorb device capacitance and provide ZVS at high frequencies. Fig. 3-1 shows a sample schematic of a class E inverter [14, 15, 37]. It only consists of a single transistor and a load network. L_{dc} is a high reactance input shunt-feed choke and C_r is the shunt resonant capacitance (If the frequencies are high enough, all of the C_r can be supplied by the transistor output capacitance. Otherwise, additional external capacitance can be added in parallel with the power device). L_r is the combination of the resonance inductance and filtering inductance and C_s is the filtering capacitance. In some applications, additional matching networks may be added between the output of the class E inverter and the load for impedance matching purpose. If these components are chosen properly, during the resonant cycle, class E does not just have zero-voltage-switching (ZVS) while the device is turned off, but also have zero-current-switching (ZCS) while the device is turned on since the derivative of the device drain-source voltage is zero during the switch turn-off time (ZdVS). As a result, the switching loss is minimized in the class E inverter and high performance can be achieved at VHF or even ultra-high-frequency (UHF). People have studied the class E inverter carefully over years due to its popularity, and there are many ways to obtain these design parameters [14, 38, 39, 40].

Even though class E inverter can provide good performance at VHF and UHF,

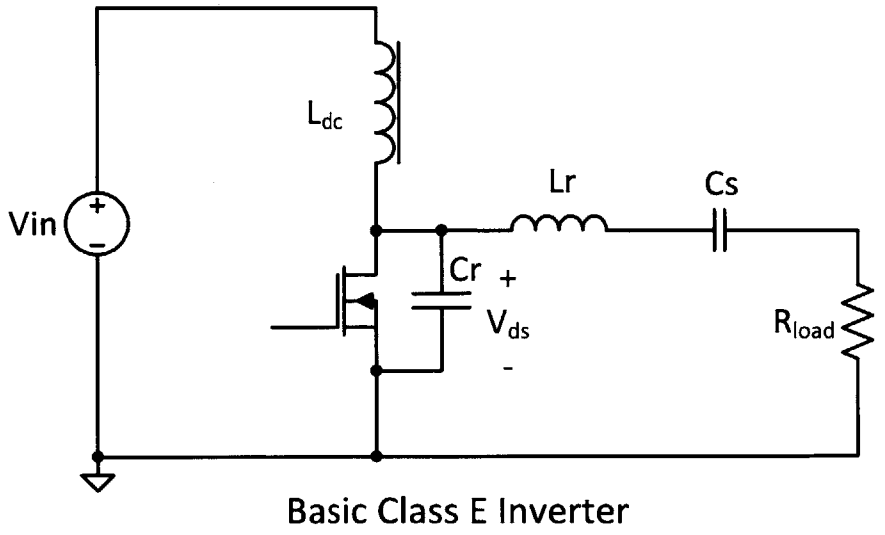


Figure 3-1: Sample schematic of a class E inverter.

it has several limitations for step-down low-voltage applications. From Sokal and Raab's paper [14, 38], the optimal design parameters can be obtained as follows:

$$L_r = \frac{QR}{\omega} \tag{3.1}$$

$$C_r = \frac{1}{\omega R(1+\pi^2/4)(\pi/2)} \approx \frac{1}{\omega R} \tag{3.2}$$

$$C_s = C_r(\frac{5.447}{Q})(1+\frac{1.42}{Q-2.08}) \tag{3.3}$$

R is the output resistance and Q is the loaded quality factor associated with the inductor in the resonant network. The Q is also corresponds to the damping of the system. The desired Q can be chosen freely, according to the design compromise to be made between harmonic content of the power delivered to the load and the efficiency. Higher Q gives less harmonic contents in the output but requires a larger numerical value of inductor and hence a larger parasitic resistance of the inductor, and hence reduce the efficiency of the inverter.

In addition, the output voltage can be given as

$$V_o = \frac{2}{\sqrt{1+\pi^2/4}} V_{in} \approx 1.074 V_{in} \tag{3.4}$$

and the output power can be delivered to the load is

$$P = V_o^2/R = \frac{2}{1+\pi^2/4} \frac{V_{in}^2}{R} \approx 0.577 \frac{V_{in}^2}{R} \tag{3.5}$$

If we substitute the output resistance R with C_r (3.2) in the output power equation (3.5), the output power can be expressed as

$$P = \pi \omega C_r V_{in}^2 \tag{3.6}$$

With the fixed power supply voltage V_{in} in the applications, the output power is directly proportional to the shunt capacitance C_r. As a result, the minimum output power of the class E inverter is limited by the switch output capacitance.

In addition, the peak drain voltage on the device in the class E is about $3.56 V_{in}$ and the maximum current in the device is

$$I_{max} = (1 + \sqrt{1+\pi^2/4}) I_{dc} \approx 2.86 I_{dc} = 2.86 \frac{P}{V_{in}} \tag{3.7}$$

With all these transistor limitations, an approximate maximum frequency of the class E inverter can be found for a given device from the output power equation (3.5) on the top is

$$f_{max} = \frac{I_{dc}}{2\pi^2 C_r V_{in}} = \frac{I_{max}}{C_r V_{in} 2\pi^2 (1+\sqrt{1+\pi^2/4})} \approx \frac{I_{max}}{56.5 C_r V_{in}} \tag{3.8}$$

As a result, with a given application (dc input voltage) and operation frequency, the minimum output power of the class E inverter is constrained by the device technology. And this also limits the class E performance for low-voltage low-power applications.

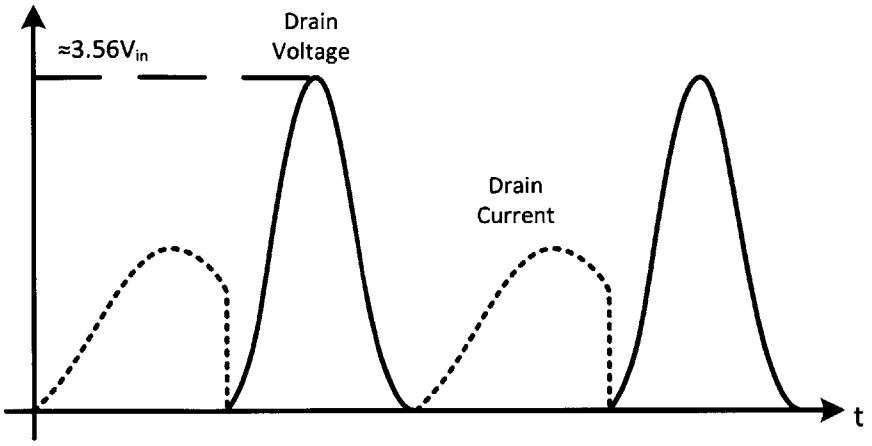


Figure 3-2: Sample waveforms of a class E operation.

Fig. 3-2 shows the switch voltage and current waveforms in a class E inverter. Besides the ZVS and ZdVS, a high voltage stress on the device is observed. The peak drain voltage on the device in the conventional class E inverter is about $3.56V_{in}$. If there is no transformation stage (such as matching network) in the output of the class E, the output voltage amplitude of the class E is about $1.074V_{in}$ based on the equation (3.4). So this gives a step-up conversion ratio between the dc input voltage to the peak ac fundamental of the output voltage in the class E inverter. This is not optimal for the step-down applications since it increases the burden of the following stages in the dc-dc converter to compensate this step-up conversion ratio.

3.1.2 Class DE Inverter

Class DE inverter is an improved version of the conventional Class D inverter [41]. As shown in Fig. 3-3, it is a two-switch topology in which the switches conduct during alternate half cycles. A series resonant tank converts the quasi-square voltage waveform into a sinusoidal load current. For the traditional class D inverter, the transistors operate with zero-current-switching (ZCS), turning on and off as the load current crosses zero. Although the class D does not have overlap loss due to switching, it still has the device output capacitance loss due to charging and discharging the

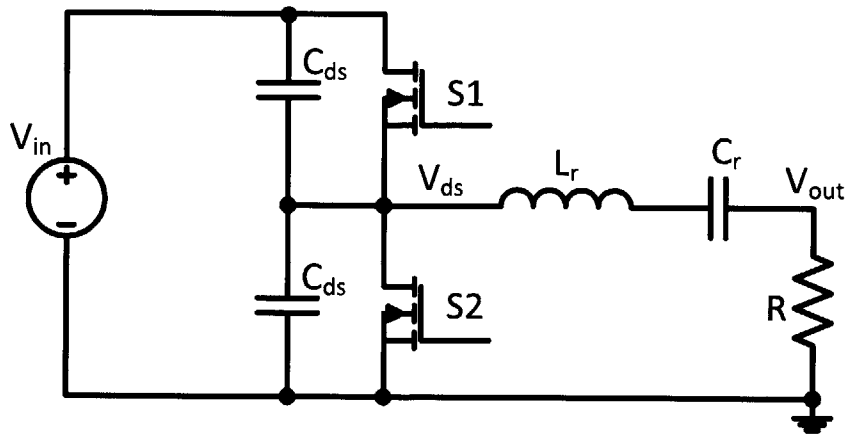


Figure 3-3: Simplified schematic of the class DE inverter.

capacitances at every switching transition; this can become a dominant loss at high frequencies.

Fig. 3-4 shows the operation of a half-bridge class DE inverter. Dead-time (dt) is added such that both switches are open during a period of commutation between switches. If we control this dead-time carefully, the output current charges or discharges the output capacitance of both devices and zero-voltage-switching (ZVS) can be achieved. In this case, the energy in the output capacitances in the switches can be recovered and delivered to the load. Moreover, the devices are also turned on at the zero current crossing point. In addition, similar to the class E inverter, the switches are also closed when the derivative of the voltage is equal to zero (ZdVS). This gives low sensitivity to the circuit parameters and switching time. The class DE topology has much lower peak voltage stress on the devices compare to the class E inverter since the peak voltage on the devices is only the input voltage V_{in}. Since the half-bridge output voltage switches between V_{in} and ground, the class DE has a voltage conversion ratio of $2/\pi$ from the dc input voltage to the ac fundamental voltage amplitude of the output, which is more suitable for step-down applications.

However, the class DE topology has two drawbacks that limit its use in VHF applications. First of all, the class DE inverter has two switches instead of one switch in the class E inverter. For optimal performance, N-channel transistors are

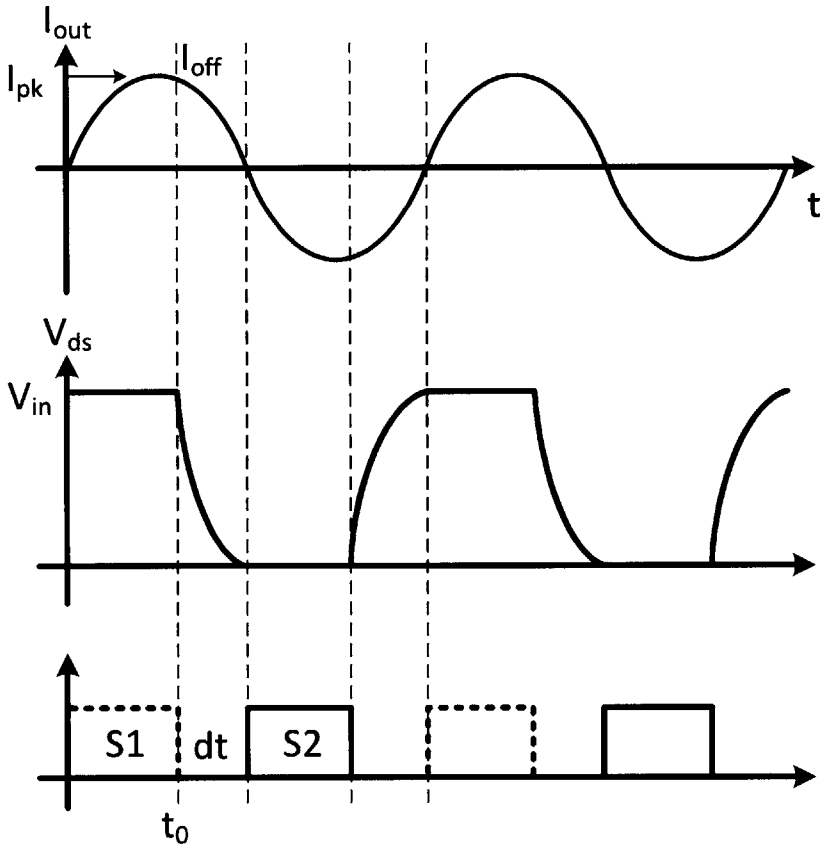


Figure 3-4: Sample waveforms of a class D operation.

normally used for both switches (owing to the relatively poor performance of P-channel transistors). As a result, a bootstrap gate driver is required for the top side device, and control commands must be level shifted to the flying reference node of the driver. In the bootstrap circuit, duty-cycle and on time is limited by the requirement to refresh the charge in the bootstrap capacitor. In VHF range, it is difficult to charge up the bootstrap capacitor if large power device is used. A big concern for the bootstrap circuit in VHF applications is the parasitic inductance in the driving loop. The parasitic inductance between the bootstrap capacitor and the device, coupled with capacitances from the gate to drain and ground of the flying switch can cause big voltage ringing at the source node of the power device during switching. This excessive voltage can damage the gate of the switches. Moreover, it is difficult to provide effective signal level shifting to the flying switch node, which has extreme common-mode noise on it.

The second limitation of the class DE inverter for VHF applications is the dead-time and turn-off current. In VHF operation, the dead-time period can be very short. In order to achieve the class DE operation (ZVS and ZdVS), the output capacitances of the switches need to be completely charged or discharged. If the power device size, output current and switching frequency are known, the required dead-time for the class DE operation can be calculated by solving the following equation:

$$\frac{I_{pk}}{\omega}(1-\cos\omega t_0) = Q = 2C_{ds}V_{in} \tag{3.9}$$

I_{pk} is the peak output current, C_{ds} is the drain-source capacitance of the device and t_0 is the time required to charge/discharge the device capacitance. If the dead-time is short and the device output capacitance is large, the devices need to turn off at very large current I_{off}:

$$I_{off} = I_{pk}\sin(\omega t_0) \tag{3.10}$$

For example, if the device output capacitance is 100 pF, and we would like to set the dead-time dt to be 2 ns for a 50 MHZ class DE inverter with input voltage of 20 V, the devices need to be turned off when the output current is 3.87 A. This relatively large turn-off current can induce considerable switching loss. In addition, with a low output current application, the choice of device size needs to be compromised to reduce the output capacitance to meet the ZVS requirement, and hence limits the inverter performance.

3.1.3 Class D inverter with Φ_2 network

In order to leverage the step-down voltage conversion ratio in the class D inverter, instead of using the output current to charge/discharge the device output capacitance to achieve ZVS, a Φ_2 network [42, 36] can be used. The Φ_2 resonant network is illustrated in Fig. 3-5. A Φ_2 network is a lower-order resonant network that provides impedance and waveforms shaping characteristics similar to those of a shorted quarter-wave transmission line. The resonant network acts to impose (approximate) half-wave voltage symmetry in the drain-source voltage waveform, yielding a quasi-trapezoidal drain-source voltage having a low peak value. For a single-switch inverter, the Φ_2 network gives a drain voltage of slightly over two times the input voltage V_{in} on the device. If the Φ_2 network is connected between the dc center-tapped voltage of the input and the switching node of the class DE inverter, the network can be leveraged to achieve zero-voltage-switching for the switches. Moreover, with the proper tuning, the network can obtain zero dv/dt across the switch at turn on, which is desirable for operating at frequencies in the VHF-UHF range.

To obtain the approximate shorted quarter-wavelength transmission line impedance characteristics, the Φ_2 network is tuned to have relatively high impedance (a pole) at the fundamental and the third harmonic and a low impedance (a zero) at the second harmonic. With a selected value of C_F, the rest of the component values can be calculated as [36]:

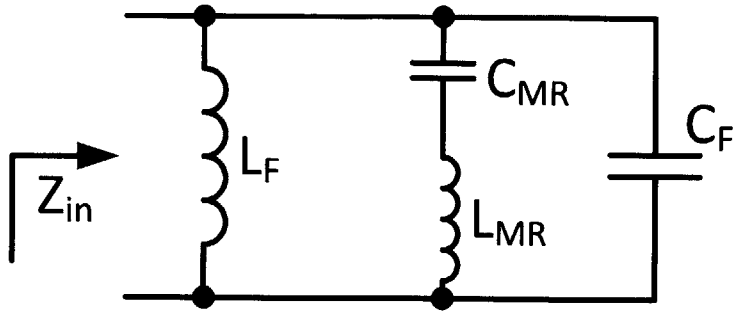


Figure 3-5: Schematic of the Φ_2 network. The input impedance Z_{in}, when when properly tuned, has relatively high impedance at the fundamental and the third harmonic and has low impedance at the second harmonic. This impedance characteristics of this network are similar to a shorted quarter wavelength transmission line.

$$L_F = \frac{1}{9\pi^2 f_S^2 C_F} \tag{3.11}$$

$$L_{MR} = \frac{4}{15\pi^2 f_2^2 C_F} \tag{3.12}$$

$$C_{MR} = \frac{15}{16} C_F \tag{3.13}$$

where f_S is the switching frequency/fundamental frequency and f_2 is the second harmonic frequency.

In order to verify the concept, a push-pull inverter with Φ_2 network is simulated. The schematic of the class D inverter with Φ_2 network is shown in Fig. 3-6. The Φ_2 network is connected between the inverter switching node and the half V_{in} node. The output capacitance of both switches are absorbed as C_F. The input voltage of the inverter is 20 V and the output power is 6 W with a ac peak voltage of 11 V. The operating frequency of the inverter is 50 MHz. The Φ_2 network impedance characteristics is shown in Fig. 3-7. With the properly chosen values of the components, the poles are placed in the fundamental (50 MHz) and the third harmonic (150 MHz), and the zero is placed in the second harmonic (100 MHz). The network appears inductive to the fundamental frequency.

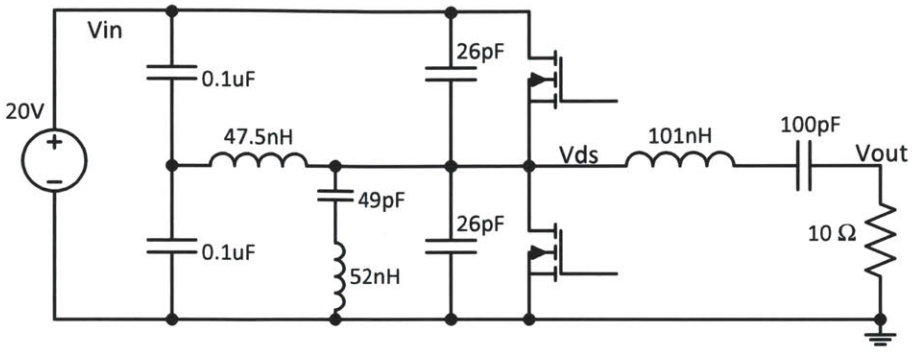


Figure 3-6: Schematic of the class D inverter with Φ_2 Network.

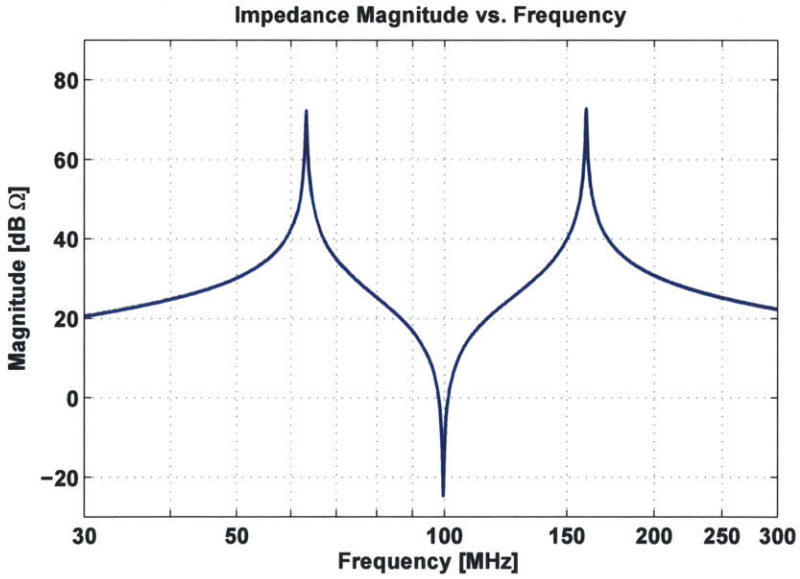


Figure 3-7: The Impedance characteristics of the Φ_2 network. The poles are in the fundamental frequency and the third harmonic and the zero is in the second harmonic. The network appears inductive to the fundamental frequency. L_F=47.5 nH, C_F=26x2 pF, L_{MR}=52 nH, C_{MR}=49 pF.

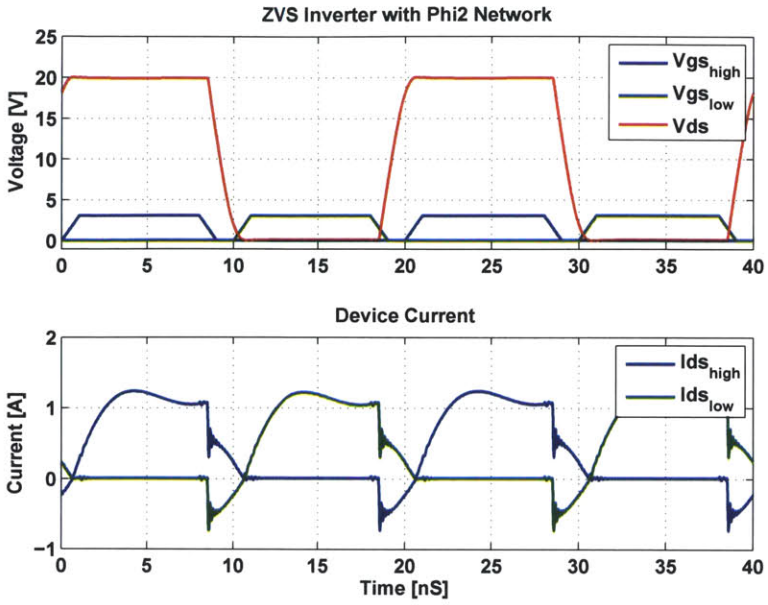


Figure 3-8: Simulated operation waveforms of the class D inverter with Φ_2 network. The input voltage of the inverter is 20 V and the output power is 6 W with a ac peak voltage of 11 V. The operating frequency of the inverter is 50 MHz. The schematic for simulation is shown in Fig. 3-6.

The simulated operating waveforms of this class D inverter with Φ_2 network are illustrated in Fig. 3-8. When both switches are off, the Φ_2 network resonates with the output capacitance of the switches and charges the drain voltage V_{ds} to two times of center tapped voltage, or V_{in}. In this case, ZVS and ZdVS can be achieved. Without using the output current to achieve ZVS, it reduces the constraint between the output current and the device size selection in the class DE inverter. But both switches are still turned off with high current, and large circulating current in the resonant network can reduce the performance of the inverter.

In certain cases, the Φ_2 network can be modified to shape the conduction current in the switches. Fig. 3-9 shows the schematics of a modified Φ_2 network class D inverter. The new inverter has the same structure but different component values in the resonant network. The new inverter has the same specifications as before. The input voltage of the inverter is 20 V and the output power is 6 W with a ac peak voltage of 11 V. The operating frequency of the inverter is 50 MHz. However, as

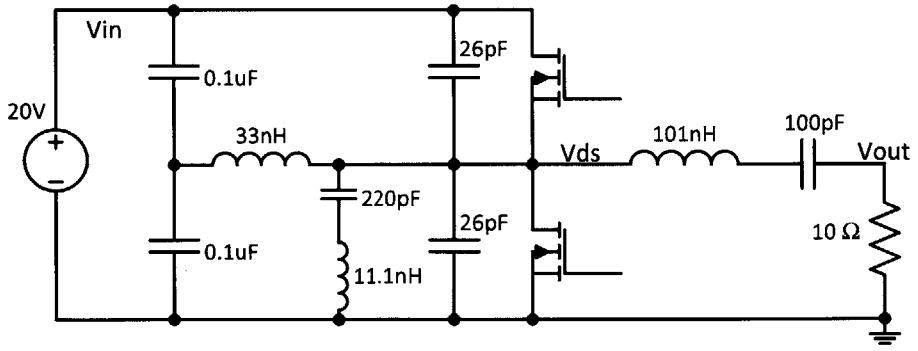


Figure 3-9: Schematic of the class D inverter with the modified Φ_2 network.

shown in Fig. 3-10, instead of putting the poles in the fundamental frequency and the third harmonic frequency, the poles are placed in the fundamental frequency and the fifth harmonic. The zero remains in the second harmonic frequency. With this new network, the inverter does not just achieve ZVS as before, but also has close to zero-current-switching at turn-off for the top-side switch. This can reduce the switching loss at high frequency and also have the potential to turn off the high-side device more easily.

Although the the modified Φ_2 network has the potential to reduce the switching loss and provide better performance, it is very difficult to tune the network to achieve zero-current-switching. And the network is not scalable and may not be able to provide the same characteristic in other setups. Furthermore, the difficulty of driving the top devices in the inverter at VHF is still unsolved.

3.1.4 Summary

In considering above resonant inverter topologies, they all have desirable performance at high frequencies but they also have key limitations. The Class E inverter is simple and efficient, but it has a step-up voltage conversion ratio and the output power is limited by the device output capacitance. These single-switch resonant inverters normally have step-up voltage conversion ratio and are more suitable for boost converters [43, 42, 44, 45, 46, 47]. Class DE inverter and Class D inverter with Φ_2 network both

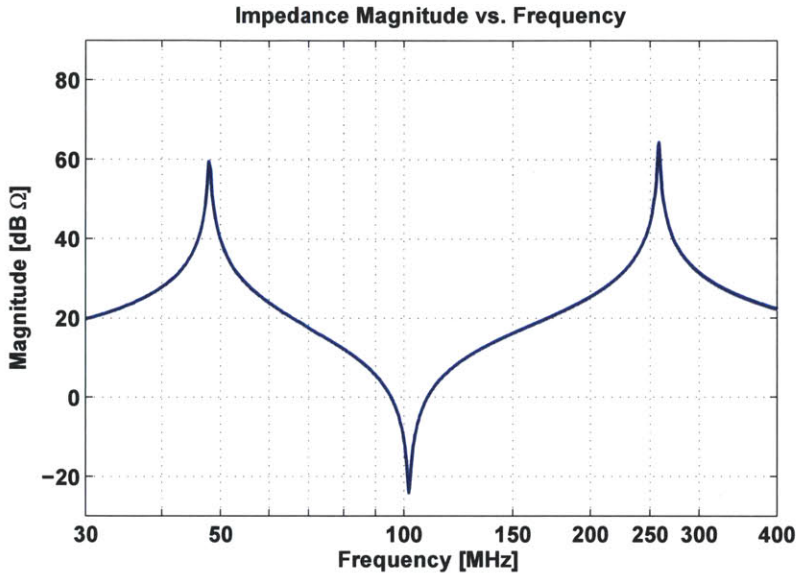


Figure 3-10: The impedance characteristics of the modified Φ_2 network. The poles are in the fundamental frequency and the fifth harmonic and the zero is in the second harmonic. L_F=33 nH, C_F=26x2 pF, L_{MR}=11.1 nH, C_{MR}=220 pF.

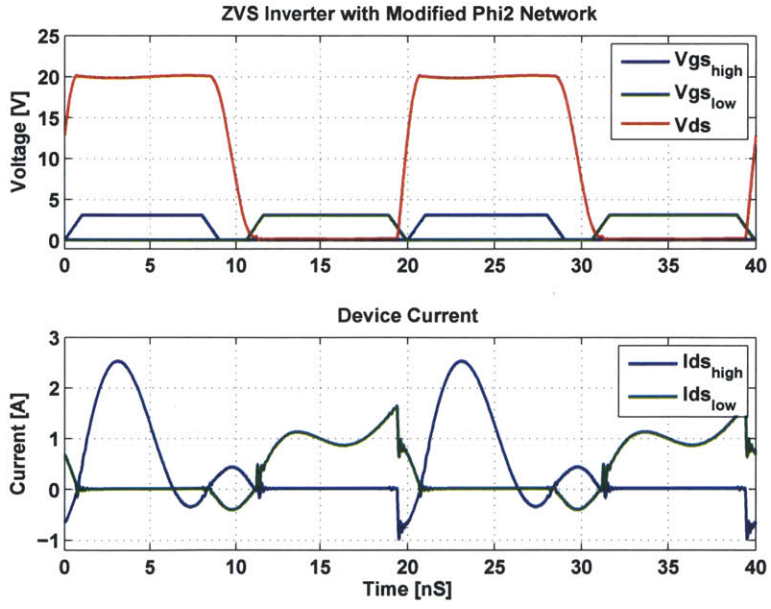


Figure 3-11: Simulated operation waveforms of the class D inverter with the modified Φ_2 network. The input voltage of the inverter is 20 V and the output power is 6 W with a ac peak voltage of 11 V. The operating frequency of the inverter is 50 MHz. The schematic for simulation is shown in Fig. 3-9.

give a step-down voltage conversion ratio, but the gate driver for the top-side switch is problematic at VHF, especially at higher voltages. In the next section, a frequency multiplier inverter will be presented to provide a better solution for step-down VHF applications.

3.2 Frequency Multiplier Inverter

As explained above, the conventional inverter topologies either have step-up conversion ratio or driving problems at VHF. In this section, a frequency multiplier inverter is proposed that has a both step-down voltage conversion ratio and high performance at VHF. Frequency multipliers have often been used when seeking extreme-high frequencies (e.g., approaching the f_T of the device) [48, 49], and class E frequency multipliers have been proposed and used, though these have inherently poor efficiency characteristics [50, 51, 52], such as much higher voltage and current stress on the device compared to the conventional class E inverter topology. Here we exploit frequency multiplication in a manner that enables high output frequency, voltage step down, and high efficiency to be attained.

Fig. 3-12 shows the schematic of the frequency multiplier circuit. It consists of two class E/F inverters (power amplifiers) [53] which are switched 180 degree out of phase. The frequency multiplier shares same of the advantages of class E/F inverters, such as easy driving (switch and gate driver referenced to ground) and high performance at VHF. The output of each class E/F inverter is coupled with a center-tapped inductor (or transformer) to cancel the fundamental content in the output. Owing to the series resonant tank, which is tuned to the second harmonic of the individual class E/F inverter switching frequency, the inverter only outputs the second harmonic content. In this case, the frequency of the ac output is twice that of the switching frequency in the class E/F inverters.

The simulated operation waveforms of the frequency multiplier is demonstrated

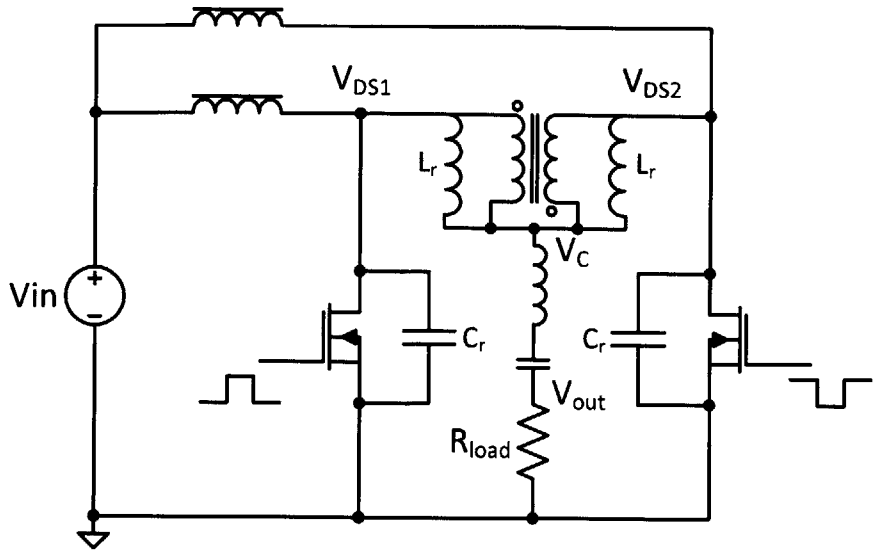


Figure 3-12: Schematic of the frequency multiplier inverter.

in Fig. 3-13. All the voltage waveforms are normalized to the input voltage to illustrate the voltage stress on the device and voltage conversion ratio. The drain voltage waveforms are similar to class E/F inverters and the peak drain voltage V_{DS} is about 3.2 times the input voltage. Once the drain voltages are combined and the fundamental contents are canceled at the center tapped node of the coupled inductor, the peak output voltage becomes approximately $0.5V_{DS}$ and it only contains the dc bias and even harmonics. After the series resonant tank, only the second harmonic voltage is delivered to the output. If we do a Fourier analysis of the center tapped voltage, we will have:

$$V_c(t) \approx V_{in} - \frac{2}{3}V_{in}\cos(2\omega t) - \frac{2}{15}V_{in}\cos(4\omega t) - ..... \tag{3.14}$$

Note that higher order terms in the expression must be even harmonics only and are cosine terms. By extracting the second harmonic term, the output voltage is given as:

$$V_o(t) = -\frac{2}{3}V_{in}\cos(2\omega t) \tag{3.15}$$

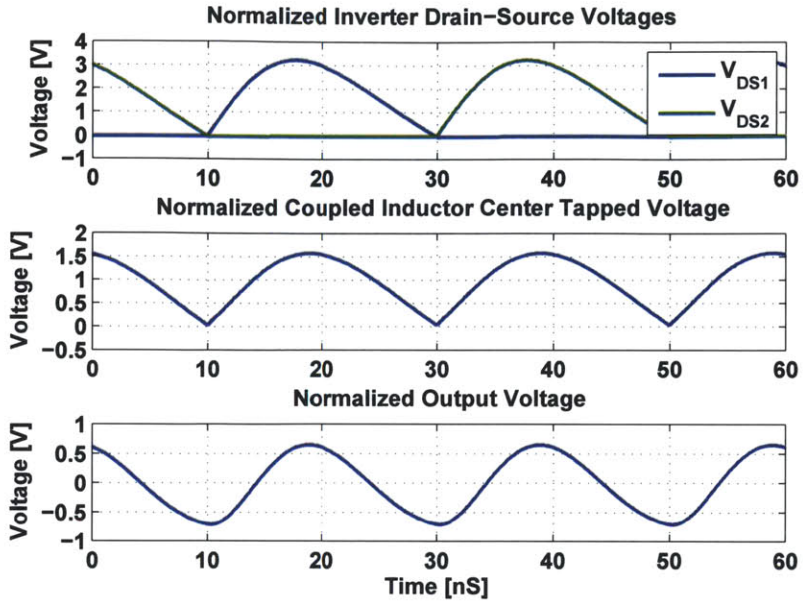


Figure 3-13: The simulated operation waveforms of the frequency multiplier. The voltage waveforms are normalized to the input voltage.

From the above output voltage equation, we can see that the proposed frequency multiplier gives a 2/3 voltage conversion ratio from the dc input voltage to the output ac output fundamental amplitude, providing a step-down characteristic. In addition, the switches only need to switch at half of the output frequency. This gives us two advantages. First, the inverter operates at half of the output frequency, so it has less switching loss and better performance. Second, the class E/F inverter can absorb larger shunt capacitance at lower switching frequencies according the previous equation (3.2). Since the minimum output power was limited by the device output capacitance in the class E inverter, switching the inverter in a lower speed can extend minimum output power range; this can be important for low-power applications.

There are several ways to further improve the frequency multiplier to have fewer components or a larger step-down voltage conversion ratio. Fig. 3-14 shows one improved version of the frequency multiplier inverter. First of all, the dc choke inductors from both of the class E/F amplifiers are combined together and connected

to the center tap of the coupled inductor. In this case, the choke inductor will carry twice of the dc current, but the ac current will be reduced by a factor of two with the same inductance. However, the ripple frequency of the ac current is doubled. The skin depth for copper is 9.2 μm @ 50 MHz and 13.0 μm @ 25MHz at room temperature. Typical choke inductors are skin depth limited at this frequency range. According to conduction loss equation, I^2R, the ac conduction loss is reduced in this configuration since the current amplitude is reduced by half and the resistance is only increased by $\sqrt{2}$. From the Steinmetz equation [54], the inductor core loss is $P_c = kf^{\alpha}B^{\beta}$, where f is the ac frequency, B is the peak magnetic field and k, α and β are core material parameters. When the current ripple is reduced by half, the magnetic field B is also reduced by half. However, when the frequency is doubled, we can have performance gain by using one choke inductor if $\alpha \leq \beta$. If $\alpha \geq \beta$, then there is higher core loss by going for the single choke inductor topology. But β is typically larger than α for high permeability materials which are used for choke inductors. As a result, it is a better approach to combine the choke inductors together from a performance perspective, as well as from a component-count perspective.

In addition, the resonant inductors from both the class E/F inverters can be absorbed into the magnetizing inductance of the transformer. Lastly, the switch output capacitances are used as the resonant capacitances (no external shunt capacitance to the devices) to reduce the RMS current in the switch and improve the efficiency.

Fig. 3-15 shows another version of the frequency multiplier inverter that provides an improved step-down voltage conversion ratio. In this topology, the two class E/F inverters are stacked at their dc inputs to provide an additional factor of one half in the input to output conversion ratio. However, two bypass capacitors are required to be connected in series with the transformer to block the dc offset. In this case, the transformer has a large resonant current, putting more components in this resonant current path, which will potentially increase the conduction loss and reduce the inverter performance. On the other hand, this is a possible approach if higher

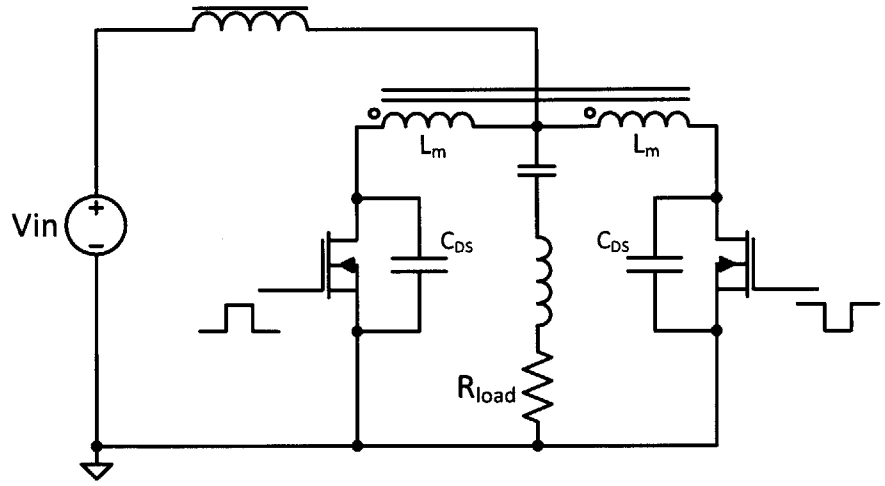


Figure 3-14: Schematic of the improved frequency multiplier inverter. The component count is greatly reduced by absorbing the resonant capacitance and inductance into the output capacitance of the device and magnetizing inductance of the transformer

step-down conversion ratio is desired.

3.3 50 MHZ PCB Prototype

Once the theory for this circuit was developed and the concept was verified in simulation, a prototype was designed and implemented with discrete components at an output frequency of 50 MHz to demonstrate the feasibility of the frequency multiplier inverter concept. Fig. 3-16 shows the schematic of the frequency multiplier PCB prototype and Fig. 3-17 shows the picture of the PCB prototype. (The detailed PCB schematic and layout are shown in Appendix A.1, the component types and constructions are shown in Table A.1.). The frequency multiplier inverter takes the 20 V dc input voltage and gives a 5 W of ac output power into an 50 Ω load resistor. The output ac frequency is 50 MHz and the inverter halves switch at 25 MHz with 50 % duty ratio. EPC 2012 200 V GaN power devices are used for the switches due to the low output capacitance and low parasitics packaging. The GaN devices have equivalent 100 pF output capacitance which provides the entirety of the shunt resonant capacitance. No external shunt capacitance is needed for resonance. A Fairchild

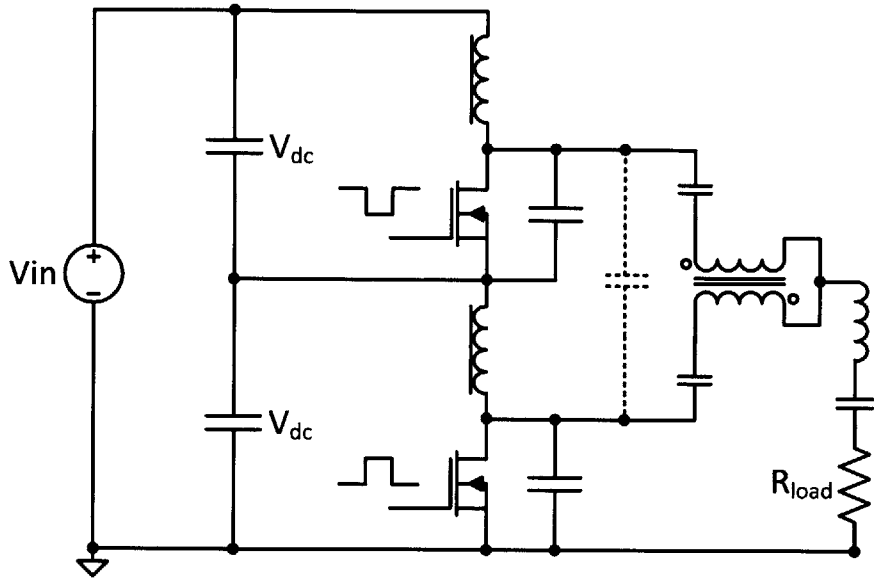


Figure 3-15: Schematic of the improved frequency multiplier inverter.

NC7WZ04 inverter is used for the gate driver of the GaN device (There are two inverters in the package and both of them are used to drive one GaN device). The dead-time between two gate drivers are controlled by the RC delay circuit before the gate driver. SRU3017 2.2 uH inductor is used for the dc choke inductor. The transformer is a 1:1 hand-wound transformer with a BLN1728-8A/94 iron powder core. The transformer is designed to have 92 nH magnetizing inductance for resonance with 3 turns of winding (AWG 28 wire, bifilar wound) and the leakage inductance is 25 nH. Since this is a resonant topology, the leakage inductance in the transformer only affects the output magnitude and will not cause excessive ringing to affect the operation. A matching network is added in the output to match to the 50 ohm load for efficiency measurement purposes. 130 nH Coilcraft MAXI air core inductor and 180 pF and 80 pF ATC RF capacitors are used for the output filter and matching network.

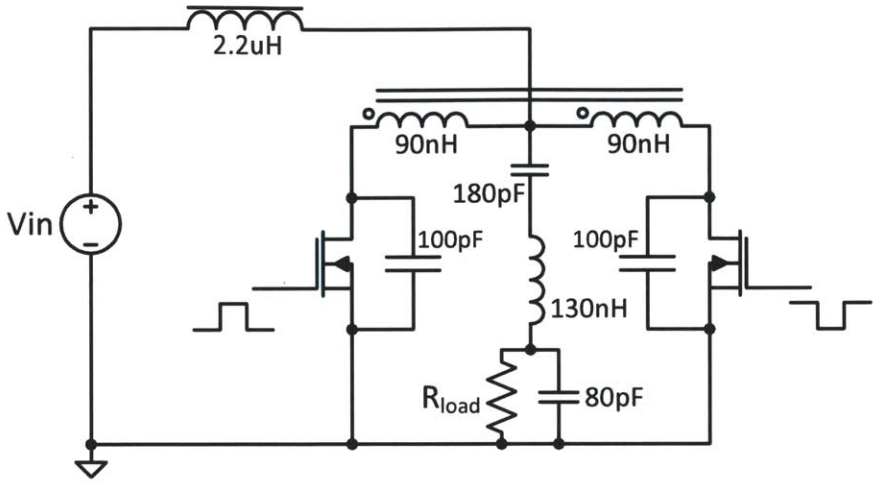


Figure 3-16: The Schematic of the frequency multiplier PCB prototype. The switches are EPC 2012 200 V GaN devices. The component types and constructions are shown in Table A.1.

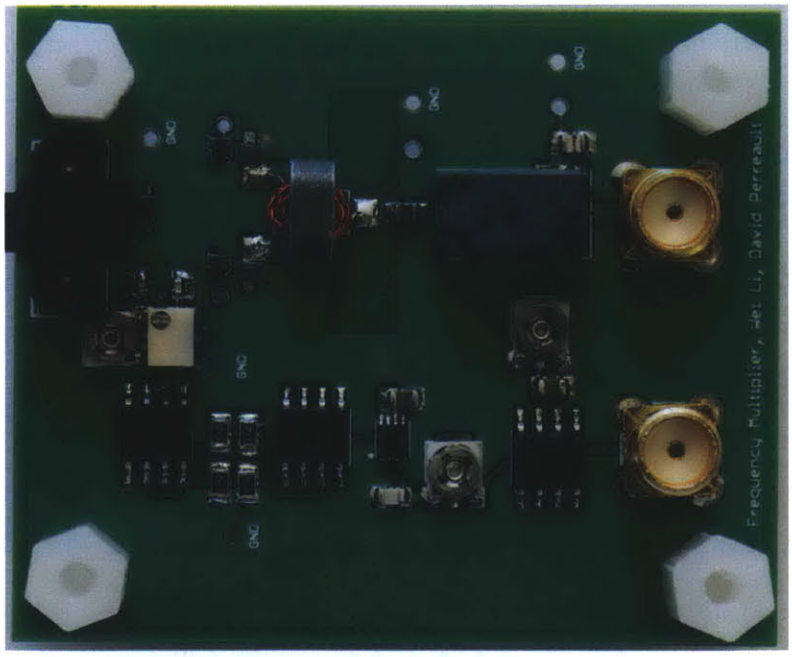


Figure 3-17: The picture of the frequency multiplier PCB prototype.

3.4 Experimental Results and Discussion

To measure the performance of the inverter, a 100 W, a 30 dB attenuator (Part #: 690-30-1, Meca Electronics Inc.) loaded with the input channel of a Tektronix TDS7254B oscilloscope, set to 50 Ω input impedance, was employed as a load for the inverter. The ac output power of the inverter was measured using a directional RF power meter (5010B, Bird Electronics Corp.). The measured waveforms of the inverter are shown in Fig. 3-18. We can see that the switches are switched at 25 MHz and the drain-source voltage is about 65 V with a 20 V dc input. The inverter output is a 22 V peak 50 MHz sinusoidal ac voltage. The output voltage is stepped up by 1.67 times to matching with the 50 Ω oscilloscope input impedance for measurement. A single 130 nH inductor is used for both the 75 nH matching network inductance and the 55 nH filtering inductance. The 2/3 step-down voltage conversion ratio cannot be directly measured here. But it will be shown in the full converter design in Chapter 5. At 5 W of output power, the measured inverter efficiency is 92.5 %, including the loss in the step-up matching network. Excluding this step up, it is estimated that the efficiency would be 94 %.

Fig. 3-19 shows the simulated efficiency of the frequency multiplier over a wide load range. The simulation setup is based on the component parameters used in the PCB prototype (such as EPC 2012 GaN device, Coilcraft air core inductor, ATC capacitor and measured hand-wound transformer data.). The efficiency simulation shows that the frequency multiplier can obtain high performance over the wide load range (inverter output power is varied by changing the load resistance and resonant inductance/transformer magnetizing inductance). With our prototype parameter setup, the inverter has a peak efficiency of 93.5 % at 7 W. The measured efficiency is also plotted in the graph to verify the accuracy of the simulation. And it illustrated that the simulation result matches with the experimental result very well. Since the inverter is switched at half of the required output frequency, the inverter can absorb larger device output capacitance into the resonant tank, and hence extend the output

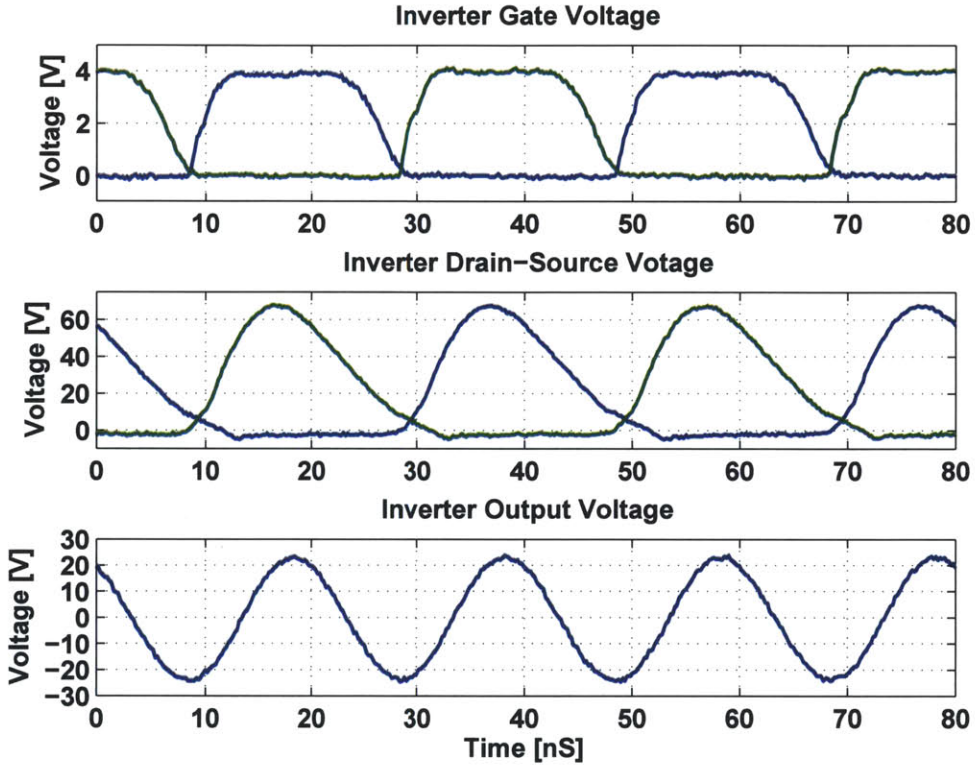


Figure 3-18: The measured operating waveforms in the frequency multiplier inverter PCB prototype. The switches are switched at 25 MHz and the drain-source voltage is about 65 V with a 20 V dc input. The inverter output is a 22 V peak 50 MHz sinusoidal ac voltage with 50 Ω load.

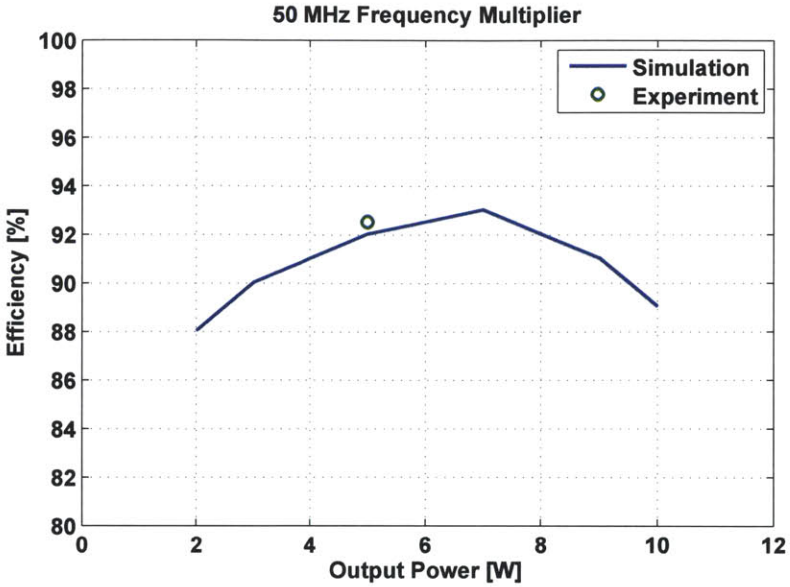


Figure 3-19: The simulated efficiency of the frequency multiplier over different load range. The simulation result is based on the component parameters used in the prototype. The output voltage is held constant at 13 V. The load resistance is varied from 42 Ω for 2 W of output power to 8.5 Ω for 10 W of output power.

power limit. With the same setup, the conventional class E topology has a minimum output power of 4 W while the frequency multiplier can reduce the output power limit by a factor of two. (It is noted that alternate versions of the class E inverter may have different limits in output power, such as the "second harmonic class E inverter" [50, 51, 52] or versions in which the input inductor is made resonant [40]).

3.5 Summary

This chapter reviews several resonant inverter topologies and analyzes the limitations of each topology for step-down applications. A frequency multiplier inverter topology is demonstrated to provide step-down conversion and high performance at VHF. A 50 MHz GaN frequency multiplier prototype was designed and built with discrete components. The prototype takes 20 V dc input voltage and delivers 5 W of ac output power with 92.5 % efficiency at 50 Ω load. With these advantages of the

frequency multiplier, it is suitable for VHF converters with high step-down voltage conversion ratio. In the next chapter, rectification for low-output-voltage VHF dc-dc converters will be explored.

Chapter 4

Switched-Capacitor Rectifier

This chapter presents a switched-capacitor rectifier that provides step down voltage conversion from an ac input voltage to a dc output. Coupled with a current-drive source, low-loss and high step-down rectification is realized. Implementation in CMOS with appropriate controls results in a design suitable for low-voltage very-high-frequency conversion. Applications include switched-capacitor rectification to convert high-frequency ac to a dc output and, combined with inversion and transformation, to dc-dc converters for low-voltage outputs. A two-step CMOS integrated full-bridge switched-capacitor rectifier is implemented in TSMC 0.25 μm CMOS technology for demonstration purposes. For an operation frequency of 50 MHz and an output voltage of 2.5 V, the peak efficiency of the rectifier is 81% at a power level of 4 W.

4.1 Rectifier Overview

As shown in Fig. 5-1, the rectification stage is one of the three major blocks in a dc-dc converter. At VHF, resonant rectifiers, such as class E rectifiers, are often used [42, 44, 46]. Resonant rectifiers can provide a significant step-down conversion ratio from the fundamental of their ac input to their dc output [55, 37, 22]. However,

these rectifiers usually require high-voltage devices, which are incompatible with low-voltage CMOS implementation. Moreover most such resonant rectifiers operate with diodes, making them undesirable for low-voltage outputs where diode drops are not acceptable from an efficiency perspective. (It should be noted that one exception to this is [22] which realized synchronous resonant rectification at VHF with cascoded CMOS devices, though this still required significant device voltage stress normalized to the output voltage.)

To realize rectification at VHF frequencies with conventional CMOS, one most frequently employs conventional half-bridge rectifiers. Unfortunately the conversion ratio of conventional half-bridge rectifiers for high-frequency rectification do not provide a desirable step down from the ac input voltage amplitude to the dc output voltage [56, 57]. This places a greater burden on the transformation stage to achieve a large step-down. This can be detrimental, as the percentage loss of a matching network (or other transformer) is often directly related to the voltage conversion ratio [1].

For example, consider the traditional half-bridge rectifier of Fig. 4-1 (which may be implemented with diodes or preferably with CMOS transistors acting as synchronous rectifiers). When driven from a current source, this rectifier provides a $\pi/2$ voltage conversion ratio from the fundamental component of the ac voltage to the output dc voltage ($V_{dc}/V_{ac,pk}$) (Fig. 4-1). This step up in voltage in the rectification stage has the effect of increasing the required conversion ratio of the other system portions in a step-down system. If the rectification stage can instead provide step-down characteristics, then the voltage transformation ratio in the transformation stage can be reduced while maintaining the same conversion ratio in the system as a whole, and hence improve the system performance. A full-bridge rectifier doubles the input voltage swing and gives a step-down voltage ratio of $\pi/4$. However, double-ended operation (such as enabled by transformer isolation) is required for the full-bridge rectifier. Therefore, a rectifier with higher step-down voltage conversion ratio for

single-ended operation is desired.

This chapter presents a voltage step-down rectifier with a switched-capacitor architecture suitable for integration on-die in CMOS. This rectifier has application to both dc-dc conversion and to ac power delivery [58] for low-voltage electronics. When coupled with an inverter and transformation stage as in Fig. 5-1, the rectifier provides a dc-dc converter having improved voltage transformation characteristics as compared to conventional converters. The inverter may be realized with high-voltage low-current devices (either on the same die as the rectifier or a different die) and the transformation stage may be realized with magnetics (transformers or matching network, etc.) realized on or off the rectifier die.

It should be noted that some kinds of switched-capacitor rectifiers have been previously explored in the context of low-frequency applications (e.g., [59, 60, 61, 62]), and multi-level converter structures such as those in [63] can be controlled to provide rectification. However, the approach presented here goes beyond existing techniques in that it is structured and controlled to provide large step-down rectification at very high frequencies (VHF) from current-driven (e.g., inductive) ac sources. To accomplish this, the proposed approach leverages the characteristics of on-die CMOS devices, utilizes self-drive of "flying" switches, and integrates key control and drive logic together with the power stage.

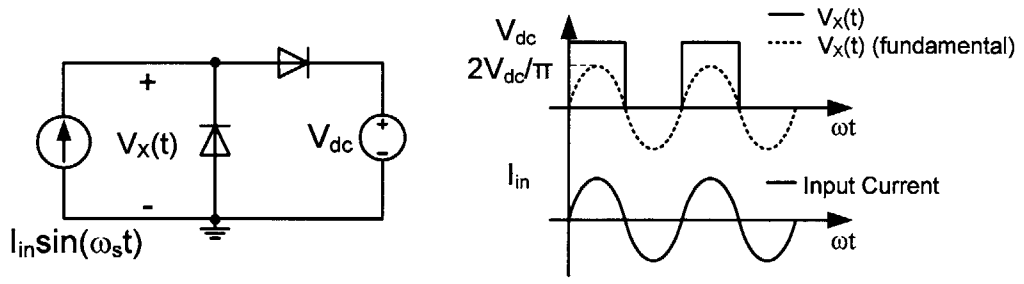


Figure 4-1: The half-bridge rectifier and its characteristics. When provided with a dc blocking capacitor at its input, this design can also be recognized as a "voltage doubler" rectifier.

4.2 Switched-capacitor Rectifier Architecture

Fig. 4-2 shows the general structure of the switched-capacitor (SC) rectifier. This rectifier is ideally driven from an inductive ac source, or an ac source that looks similar to a current source. Excepting the switches referenced to the top of the half bridges, the switches can be replaced by diodes. In steady-state, the voltages across all the capacitors are equal to the output voltage. In "diode operation", whether the capacitors are stacked in series or parallel by the operation of the switches depends on the ac-drive current direction. (With active devices, it is also possible to phase shift the rectifier switching with respect to the ac-drive current). In either case, the input voltage swing of the switched-capacitor rectifier is N times the output voltage for N "steps" (with N = 1 representing only a half-bridge). The switched-capacitor rectifier can provide a $\pi/(2N)$ step-down voltage conversion ratio from the fundamental component of the ac input voltage to the output dc voltage ($V_{dc}/V_{ac,pk}$). This increases the step down transformation in the rectification stage of a dc-dc or ac-dc power converter, and also minimizes the step down conversion ratio of a transformation stage in ac power delivery system to provide better performance.

To illustrate the operation of the system, a two-step switched-capacitor rectifier is presented here in detail. Fig. 4-3 shows a schematic of one version of the proposed switched-capacitor rectifier, with details of the gate drive illustrated in Fig. 4-4. Fig. 4-5 shows the switching pattern of the SC rectifier and Fig. 4-6 describes the theoretical switching and voltage waveforms for "diode rectification".

Control for "Diode rectification", providing a resistive effective input impedance of the rectifier at the switching frequency, is described as follows: When the input ac current is positive, switches labeled S_1 are closed and switches labeled S_2 are open. The capacitors C_1 and C_2 are connected such that positive current charges C_1. This current recharges C_2 during at least a portion of this state, and this current and the current in C_2 support the load current. Since the capacitors C_1 and C_2 both hold the same average voltage V_o in steady-state operation, the input voltage of the

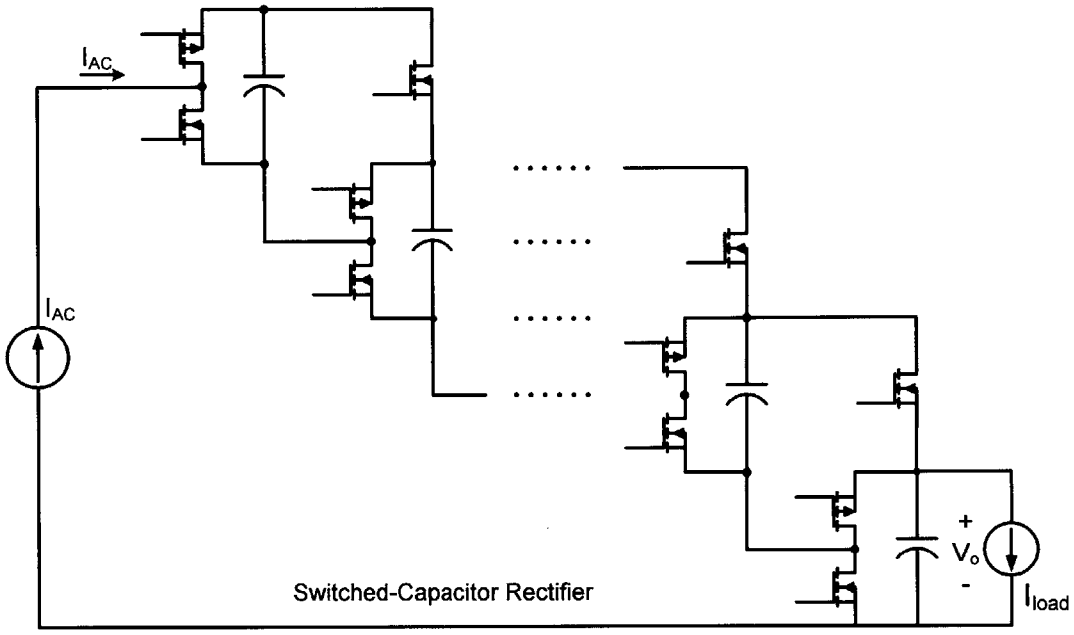


Figure 4-2: General schematic of a multi-step switched-capacitor rectifier.

SC rectifier is approximately $2V_o$ in this state. When the input current is negative, switches S_1 are opened and switches S_2 are closed. In this case, C_1 and C_2 are connected in parallel to support the load, and the input of the SC rectifier is shorted to the ground. As a result, the input voltage of the SC rectifier is 0 V. In this case, there is a $2V_o$ square-wave voltage swing at the input of the rectifier, thus providing a $V_{dc}/V_{in,fundamental} = 1/\frac{4}{\pi} = \frac{\pi}{4}$ fundamental peak ac-to-dc conversion, which results in step-down rectification. This design thus provides an additional factor of two in voltage step down as compared to a conventional half-bridge rectifier. Higher-stage versions of this switched-capacitor rectifier can provide higher step-down ratios, but require a higher device count and greater control complexity.

As can be seen from the switched-capacitor rectifier operation, each of the devices only need to block the low output voltage level. As a result, low-voltage CMOS devices rated for the converter output voltage can be used to provide fast switching speed. As device M3 has its control port referenced to the dc output voltage, level-shifting its control signal is straightforward, and it can be driven easily. The detailed

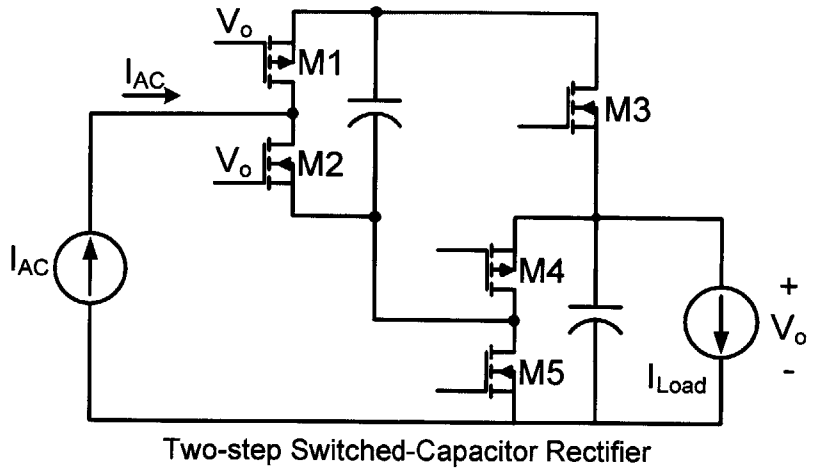


Figure 4-3: Sample schematic of a two-step CMOS switched-capacitor step-down rectifier. The drive and control structure is shown in Fig. 4-4. Note that in some cases a dc blocking capacitor (not shown) may be desired at the rectifier input; this does not change the rectification characteristics.

drive and control circuit for the SC rectifier is shown in Fig. 4-4. Flying capacitor C_1 can be used as a bootstrap capacitor to provide energy for the gate driver of M3. This eliminates the extra circuit that would otherwise be required to supply power for the gate driver of M3 and also minimizes the driver energy storage capacitance C_3. In addition, since M1, M2, M3 and M4 share the same control pattern, only a constant voltage is required to drive the gates of M1 and M2, while the V_X node can be controlled by switching M4 and M5 using ground-referenced logic and drivers. As a result, the first-stage devices M1 and M2 can be self-driven by the output voltage, as is also shown in Fig. 4-4.

In general, for a many-step rectifier, devices in the bridge of previous "step" can be driven by the positive voltage of the capacitor in the next "step". Furthermore, the devices referencing to the positive node of the flying capacitors can be driven by a dc voltage $N \times V_o$ (N is the level of the particular device) since their reference nodes are switching with the flying capacitors. This reduces the complexity of the driving scheme greatly. Only the devices in the last stage are required to be controlled and all other devices in the multi-level SC rectifier can be either self-driven or driven by dc voltages. The driving scheme of the multi-level SC rectifier is shown in Fig. 4-7.

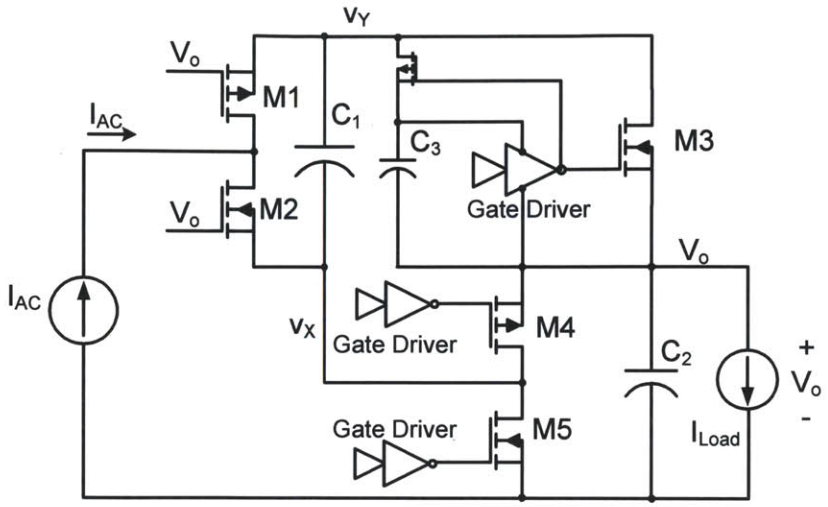


Figure 4-4: Control details of the switched-capacitor rectifier.

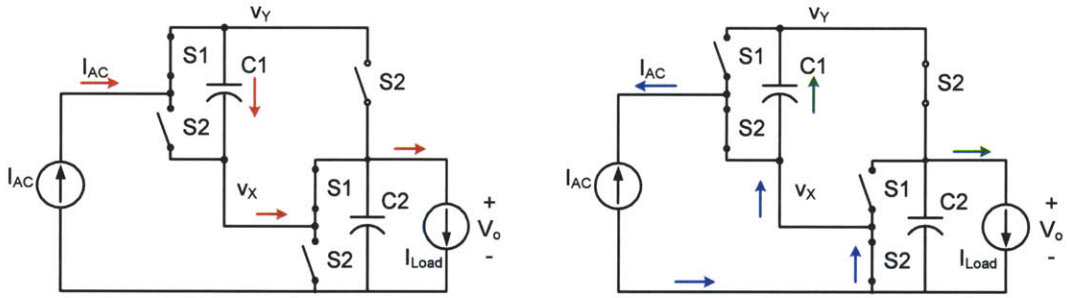


Figure 4-5: Switching patterns of the switched-capacitor rectifier.

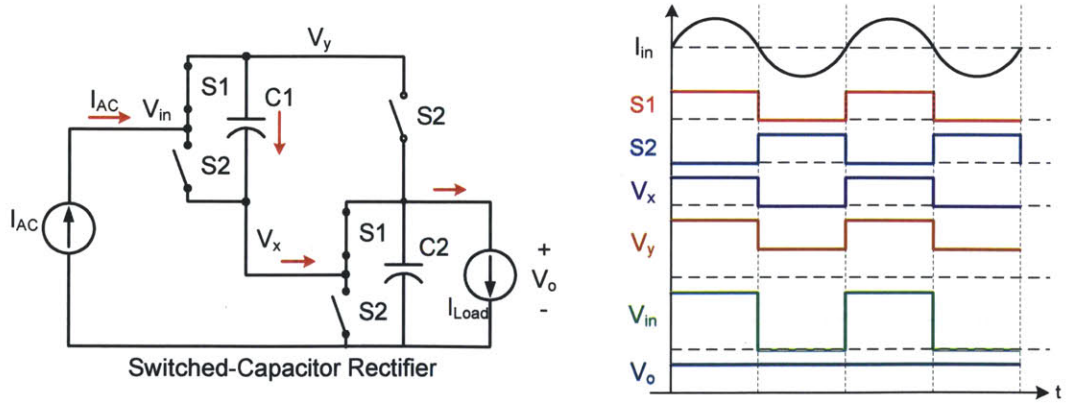


Figure 4-6: Switched-capacitor rectifier operating waveforms.

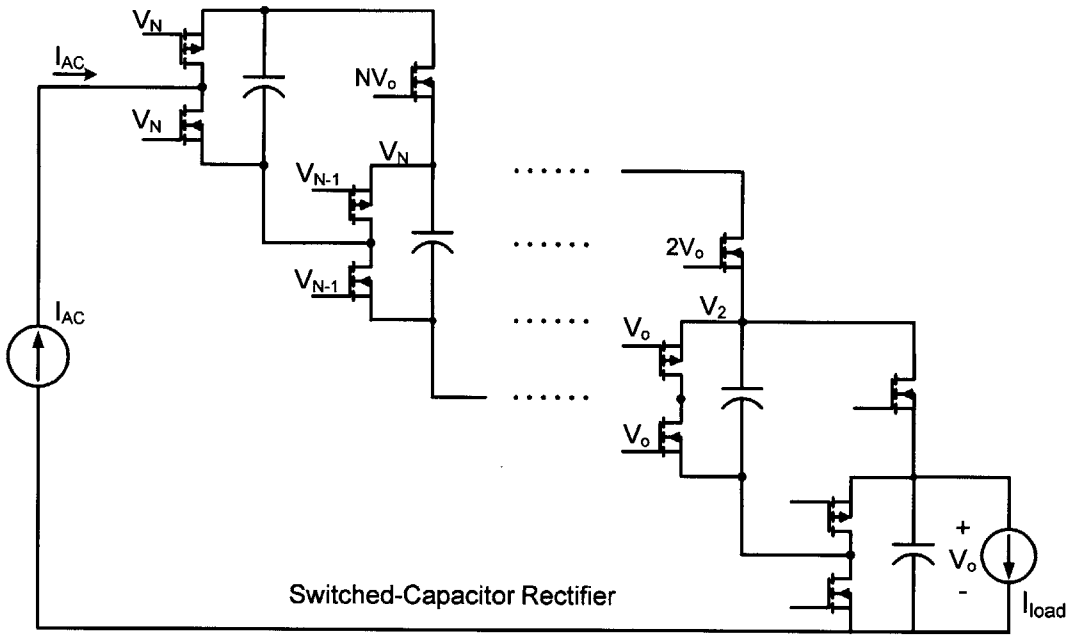


Figure 4-7: Self-driven scheme for the multi-level switched-capacitor rectifier circuit.

It will also be recognized that this rectifier can be driven in reverse to provide an inverter with a large step-up voltage conversion ratio. Implemented in this manner, one gets a large amplitude square wave output. A square-wave output is more crude than achievable with multi-level topologies such as a Marx inverter [64] or other multi-level inverters [63], but takes advantage of the self-driven nature of many of the switches in a CMOS implementation to provide a distinct performance advantage.

Similar to the full bridge rectifier, the SC rectifier can also be connected in a double-ended fashion to double its ac voltage and eliminate the dc offset across its input port. Fig. 4-8 shows the schematic of a double-ended SC rectifier structure. The double-ended SC rectifier has the same operation pattern as a single-ended SC rectifier. It just has two single-ended SC rectifiers operating 180° out of phase (polyphase versions are likewise possible). In the double-ended SC rectifier, the input voltage swing is $\pm NV_o$, so the step-down voltage conversion ratio is $\pi/(4N)$.

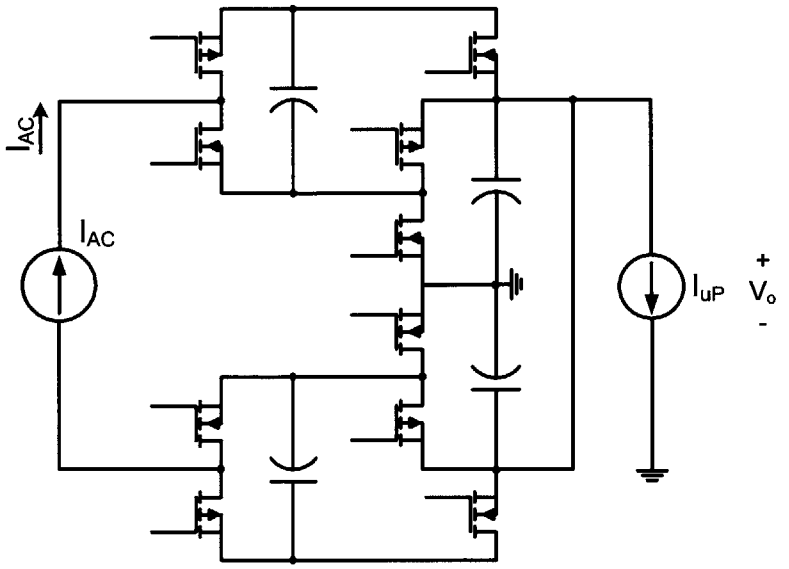


Figure 4-8: Schematic of a double-ended two-step switched-capacitor rectifier.

4.3 10 MHz Discrete Prototype

To further explore the functionality of the switched-capacitor rectifier and validate the concept, a two-step full-bridge switched-capacitor rectifier prototype was built with discrete components. The topology version tested is shown in Fig. 4-9 below. The discrete rectifier was designed for operation at a 10 MHz switching frequency and a 3 V output voltage with 2 W of output power. In order to simplify the control, diodes are used in the bridges. In addition, the output voltage polarities are inverted to yield an improved PCB layout. (This does not affect the underlying operation of the SC rectifier.) For testing purposes, the switched-capacitor rectifier prototype is driven from a RF power amplifier (10W1000, Amplifier Research), which is controlled by a function generator (33250A, Agilent Technologies).

BAT60A Infineon silicon schottky diodes were used for the diodes. Switches were Si1012R N-Channel silicon MOSFETs from Vishay and the drivers for the switches were NC7WZ04 TinyLogic inverter from Fairchild. Isolation is provided by a 1:1 hand-wound transformer with a BLN1728-8A/94 core. There are 6 turns of 30 AWG wire each in primary and secondary (bifilar wound to minimize the leakage inductance) on

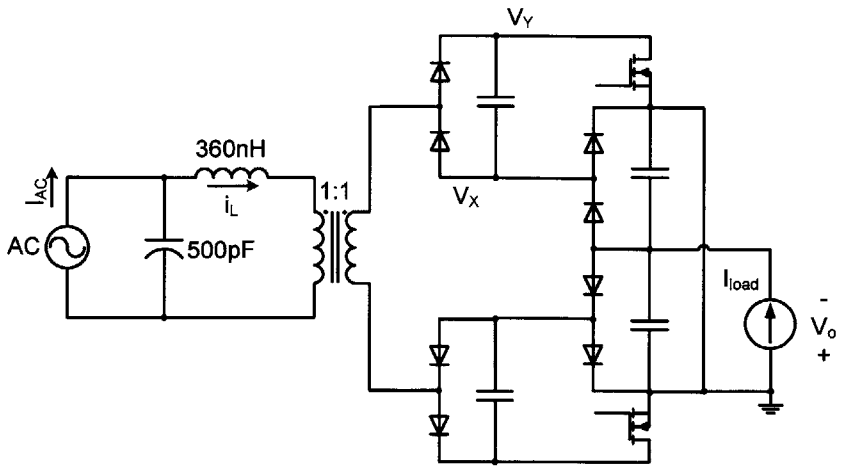


Figure 4-9: The schematic of a full-bridge two-step switched-capacitor rectifier prototype with discrete components.

the transformer providing magnetizing inductance L_m of 961 nH and leakage inductance L_l of 43 nH in both the primary and secondary. A 360 nH Coilcraft air core inductor and a 500 pF ATC capacitor are used to form a impedance matching network to match the input impedance of the SC rectifier to the 50 Ω output impedance of a power amplifier and to provide filtering of the rectifier input voltage harmonics. Fig. 4-10 shows a picture of the discrete SC rectifier prototype and Fig. 4-11 shows measured operating waveforms in the SC rectifier. Since the magnitude of the output voltage is 3 V (-3 V when the output node is referenced to ground), with isolation, the two-step SC rectifier in each half-bridge gives a square wave of $\pm V_o = \pm 3$ V in the input. So the peak-to-peak differential voltage of the square wave in the input of the full-bridge two-step switched-capacitor rectifier is $\pm 2V_o = \pm 6$ V. This successfully demonstrates that the half-bridge two-step SC rectifiers can provide the same input voltage swing as a conventional full-bridge rectifier, and a full-bridge two-step switched-capacitor rectifier can provide an input voltage swing twice as large as a conventional full-bridge rectifier.

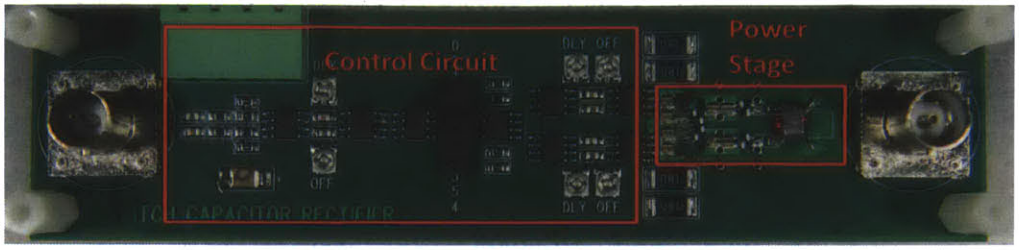


Figure 4-10: A photo of the discrete full-bridge two-step switched-capacitor rectifier prototype.

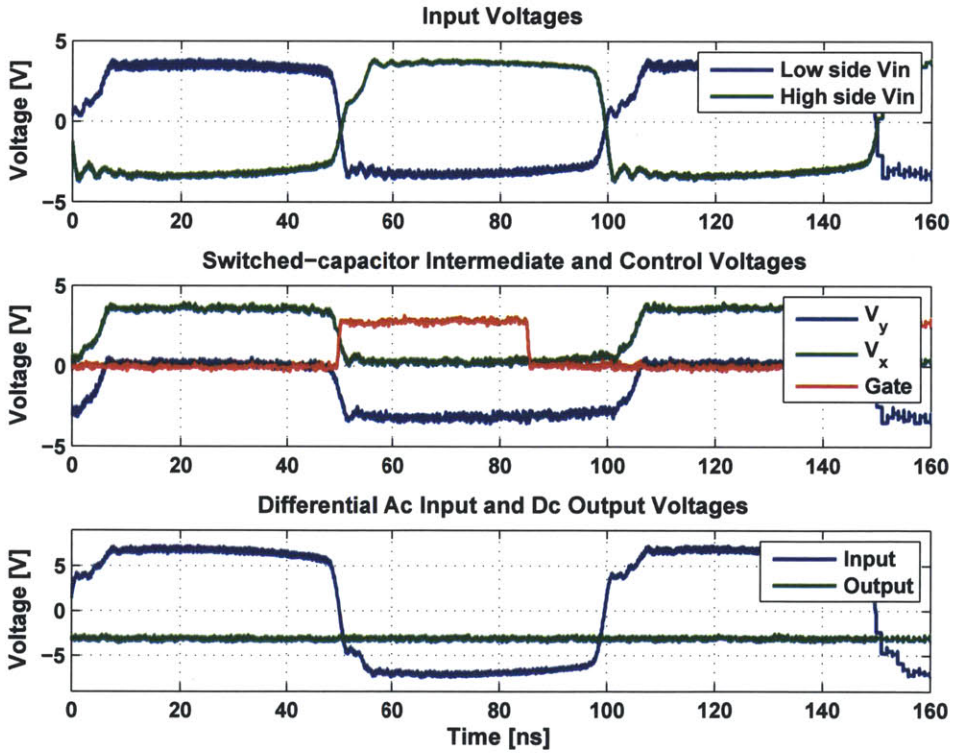


Figure 4-11: Measurement waveforms of the discrete SC rectifier prototype.

4.4 Integrated SC Rectifier Prototype

The prototype with discrete components validated the switched-capacitor rectifier concept. Based on this, an integrated version of the two-step switched-capacitor rectifier has been designed and fabricated in a TSMC 0.25 μm process to demonstrate the functionality and integration possibility of the SC rectifier. A 2.5 V output voltage was chosen based on the native operating voltage of the TSMC 0.25 μm process used for the prototype. (This process was selected to be able to validate the approach at relatively low cost. As described below, higher performance would be expected with finer line-width CMOS processes.) An operation frequency of 50 MHz was chosen to minimize the size of passive components while providing acceptable efficiency. (A finer-width processes would enable combinations of lower voltages, higher frequencies, and higher efficiencies based on CMOS scaling characteristics.) There are two single-ended switched-capacitor rectifiers on the chip, which can be configured into a double-ended rectifier. Each single-ended switched-capacitor rectifier has an output power rating of 2 W (4 W total for the full circuit). This power level could represent that of a small zone in a microprocessor, or that of an entire low-power digital IC.

4.4.1 Design Details

The device sizes for the rectifiers were optimized to balance the conduction loss and capacitive loss [20, 19, 21]. There are two major losses on the power devices. One is the conduction loss when the switch is on and the other is the capacitance switching loss. For a specific CMOS technology, by assuming the unit width on-resistance of the device to be R_0 $(\Omega \cdot m)$, the unit gate-source capacitance to be C_{GS0} $(nF \cdot m)$ and the unit device output capacitance to be C_{DS0} $(nF \cdot m)$, the losses can be calculated depending on the device width (w), switching frequency (f) and voltage (V_{dd}):

$$P_{con}(w) = I_{rms}^2 \frac{R_0}{w} \tag{4.1}$$

where I_{rms} is the rms current when the switch is on. The conduction loss is inverse proportional to the width of the device. When the device is wider, the on-resistance of the device is smaller, and hence the conduction lower is lower with the same rms current.

$$P_{cap}(w) = C_{GS0} w V_{dd}^2 f + C_{DS0} w V_{dd}^2 f \tag{4.2}$$

Only gate-source capacitance loss and device output capacitance loss are considered in here to simplify the optimization. The gate-drain capacitance (miller capacitor) is typically very small, (10 times smaller compared to the gate-source capacitance), and hence the loss is negligible. The capacitive loss in the device is proportional to the size of the device. When the device is wider, the capacitances of the device are larger, and hence the capacitive losses are larger.

The total loss in the power device is

$$P_{loss}(w) = I_{rms}^2 \frac{R_0}{w} + C_{GS0} w V_{dd}^2 f + C_{DS0} w V_{dd}^2 f \tag{4.3}$$

From this conduction loss and capacitive loss trade-off, the optimal device width can be calculated by letting the derivative of the loss equation respect to width w to be zero.

$$\partial P_{loss}(w)/\partial w = -I_{rms}^2 \frac{R_0}{w^2} + C_{GS0} V_{dd}^2 f + C_{DS0} V_{dd}^2 f = 0 \tag{4.4}$$

$$w_{opt} = \sqrt{\frac{I_{rms}^2 R_0}{C_{GS0} V_{dd}^2 f + C_{DS0} V_{dd}^2 f}} \tag{4.5}$$

(The Matlab Optimization code is shown in Appendix. B.1). The modeled loss distribution of the rectifier is shown in Fig. 4-12 and Table 4.1. A taper factor of 8 is chosen for the gate driver to balance the tapered gate driver loss and switching loss of the power devices [20] (Simulation is used to sweep the taper factor for the

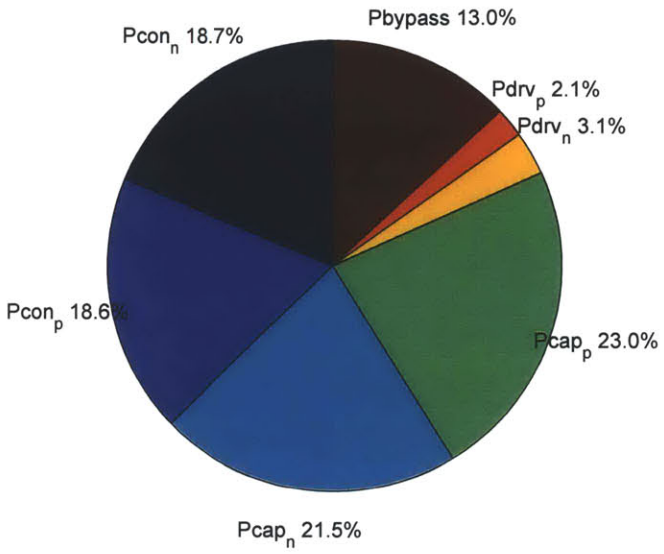


Figure 4-12: Figure shows the loss break down in the rectifier. $Pcon_n$ and $Pcon_p$ mean the conduction loss in NMOS device and PMOS device respectively, $Pcap_n$ and $Pcap_p$ are the capacitively loss for the NMOS device and PMOS device. $Pdrv_n$ and $Pdrv_p$ are the gate driver loss for the devices. P_{bypass} is the conduction loss on the ESR of the bypass capacitors. Optimization code is shown in Appendix. B.1). And the detailed loss values are shown is Table 4.1

gate driver with optimal power device sizes); a 6 stage driver was employed, starting with a first-stage driver. The detailed schematic of the 6-stage gate driver is shown in Fig. 4-13. In the rectifiers, the optimized width of each NMOS device is 23100 μm and the optimized width of the PMOS device is 48000 μm. The detailed device information is shown in Table 4.2.

In order to explore the proposed approach and compare it to other rectification architectures, conventional CMOS bridge rectifiers were also built on the same IC. There are a total of 6 half-bridge rectifiers integrated on the chip for testing flexibility, which can be reconfigured into 3 sets of individual full bridge rectifiers. Each full-bridge rectifier is optimized to handle 2 W of output power. Since the rectifier is driven by an inductive sinusoidal current source, soft-switched class D or DE operation can be achieved in the rectifiers if the control timing is adjusted carefully [41]. Fig. 4-

Table 4.1: Device Loss Summary

	Value
Power	2 W
Frequency	50 MHz
Output Voltage	2.5 V
$Pcon_n$	63.6 mW
$Pcon_p$	63.2 mW
$Pcap_n$	73.1 mW
$Pcap_p$	78.2 mW
$Pdrv_n$	7.1 mW
$Pdrv_n$	10.5 mW

This table shows the rectifier loss breakdown in the design. $Pcon_n$ and $Pcon_p$ mean the conduction loss in NMOS device and PMOS device respectively, $Pcap_n$ and $Pcap_p$ are the capacitively loss for the NMOS device and PMOS device. $Pdrv_n$ and $Pdrv_p$ are the gate driver loss for the devices.

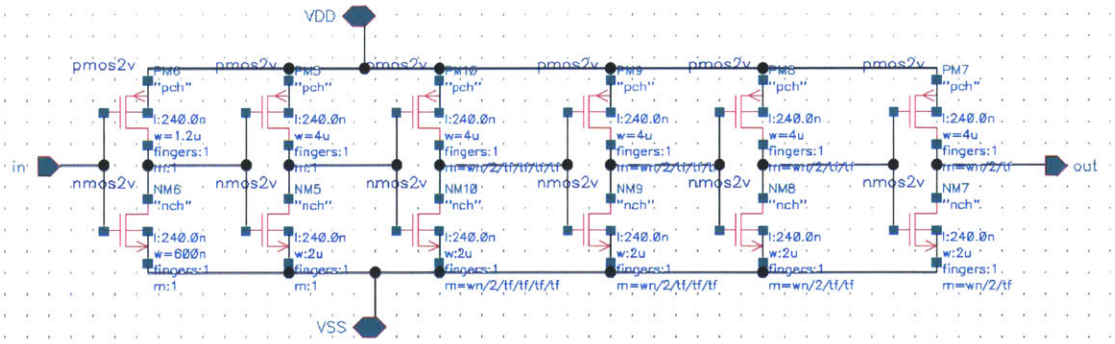


Figure 4-13: Detailed schematic of the gate driver. There are 6 stages with a taper factor of 8.

14 shows the simulated switching waveforms of the soft-switched rectifier. When the sinusoidal input current changes from negative to positive, the low-side NMOS can be turned off under a near-zero-current-switching condition. With the high-side PMOS remaining off, the positive input current can charge the drain-source capacitance of the NMOS and discharge the drain-source capacitance of the PMOS. If this dead-time period is controlled accurately, zero-voltage-switching can be achieved at the turn-on transition of the high-side PMOS. Similarly, the high-side PMOS can be turned off close to zero-current-switching condition when the input current is making the positive to negative transition. By controlling the dead-time, zero-voltage-switching can be achieved at the turn-on transition of the low-side NMOS. In this way, the energy stored in the output capacitance of the switches can be recycled and hence improve the performance of the rectifier. In this particular design, 1 nS fixed dead-time is used based on the sizes of the devices and input current level; this dead-time is also used in the switched-capacitor rectifier for the same purpose.

A simplified full-chip schematic is shown in Fig. 4-15. Only a single full-bridge rectifier and a single-ended switched-capacitor rectifier are shown in the schematic for simplicity. Synchronous rectification is controlled by two-stage voltage-controlled delay lines (due to the limited controllable delay range provided by the RC network). The first stage comprises coarse voltage-controlled delay lines, which gives a 2 nS to 11 nS adjustable delay range. Three of these coarse voltage-controlled delays are connected in series and a 2-bit ADC is used to select between the center tap delays. The second stage comprises a fine voltage-controlled delay lines, which only give a 1 nS adjustable delay range. With this stage, the timings of rectifiers can be fine tuned to achieved optimal performance. The schematic of the voltage-controlled delay line is shown in Fig. 4-16. The delay is controlled by the RC time constant between the inverters. The NMOS connected in series with the capacitor is used as voltage-controlled resistor. When the RC time constant is comparable to the switching frequency, the delay is highly nonlinearly dependent on the control voltage

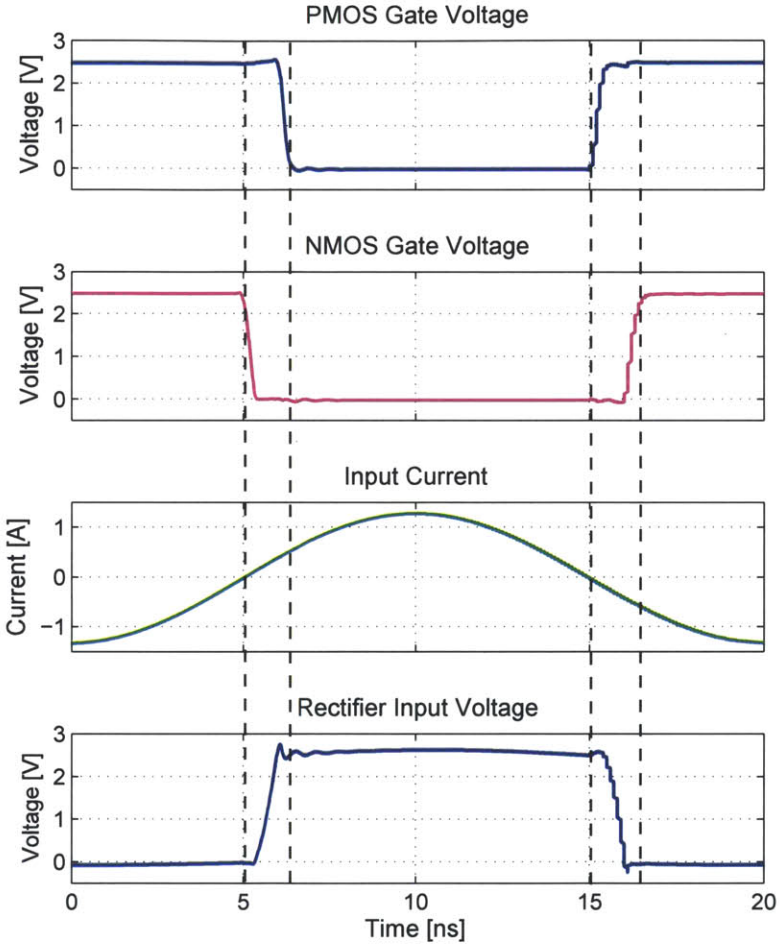


Figure 4-14: Simulated soft-switched class D rectifier switching waveforms. It shows that both devices can achieve zero-voltage turn-on and close to zero-current turn off. The output power is 2 W with output voltage of 2.5 V. The switching frequency is 50 MHz.

due to the nonlinearity in the inverter. As a result, a multi-stage system is required for long delays. Fig. 4-17 shows the detailed schematic of the multi-stage delay line for the fine tune control. Using additional MiM capacitor in the output of the inverter can better define the RC time constant and have better control linearity. However, large capacitors are required for long delays, and this is not economical in IC design due to the large sizes of the capacitors. The other way to control the delay is by controlling the current feeding into the inverter. Fig. 4-18 shows the detailed schematic of the multi-stage delay line for the coarse delay control. A PMOS is connected in series between the inverter and the power supply, by controlling the PMOS resistance, the current sinking by the inverter can be limited. Similar to the previous control method, the delay is highly nonlinearly dependent on the control voltage due to the nonlinearity of the MOS resistance control. It can provide a large delay in high Si density. And linearity is not required for the coarse control delay line.

In addition, a level shifting circuit is required to control the NMOS referenced to the output voltage in the switched-capacitor rectifier. The level shifter needs to convert the ground-referenced signal to an output-voltage-referenced signal. A capacitor-coupled level shifting circuit is used here and the schematic is shown in Fig. 4-19. The actual design schematic is shown in Fig. 4-20. Compared to resistive-loaded level shifting circuits, this capacitor coupled level shifter consumes no static power and has faster transition time (smaller RC time constant in the switching node). Furthermore, the level shifting is based on the output voltage instead of the 2.5 V logic supply voltage. In this case, the logic driven by the level shifter will never experience a voltage higher than the output voltage during the startup transient. As a result, only native 2.5 V MOSFETs are used in the circuit and no high-voltage devices are required. However, deep-n-well NMOS is required when the body substrate is not referenced to ground.

A 390 pF dc decoupling NMOS bypass capacitor is integrated for the output of

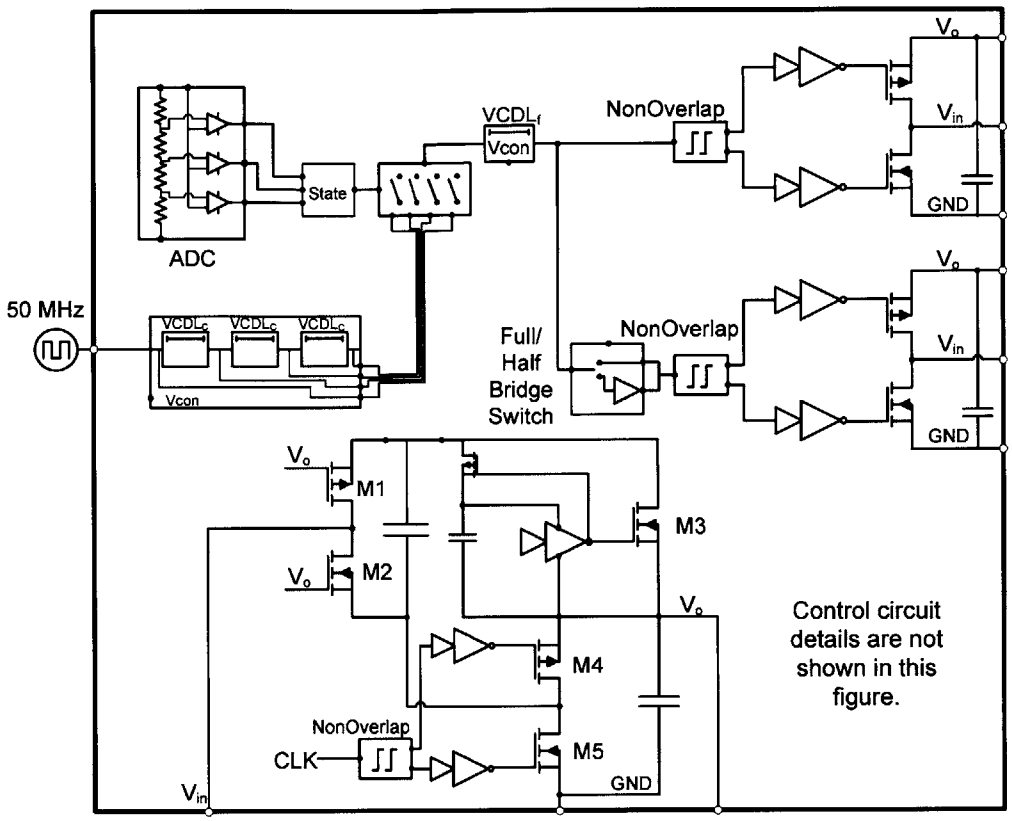


Figure 4-15: A simplified schematic of the chip. Control circuit details are not shown in the figure. In addition, only a single full-bridge rectifier and single-ended switched-capacitor rectifier are shown. $VCDL_c$ is the coarse control of the voltage-controlled delay line and $VCDL_f$ is the fine-tune control of the voltage-controlled delay line.

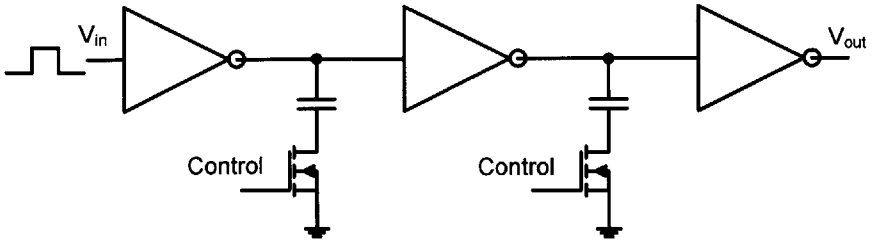


Figure 4-16: The schematic of the voltage-controlled delay line.

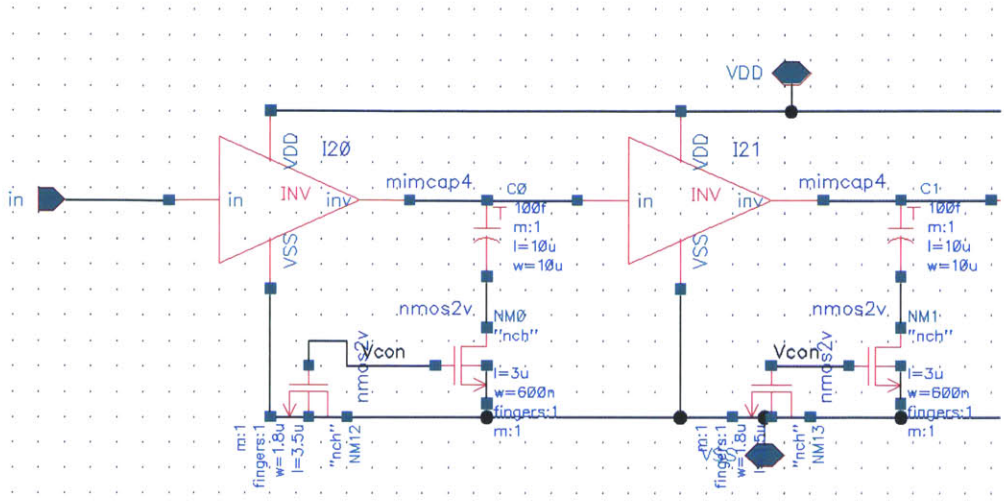


Figure 4-17: The detail schematic of the voltage-controlled delay line for fine tune control. 100 pF MiM capacitor is used to control the RC time constant. The resistance is controlled by the NMOS.There are 6 stages in the delay line and only two stages are shown here.

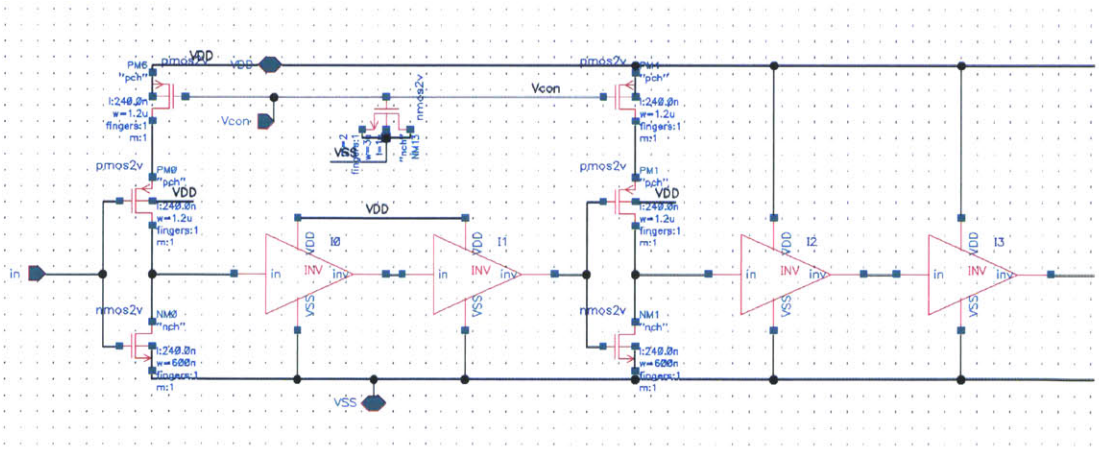


Figure 4-18: The detail schematic of the voltage-controlled delay line for coarse control. By controlling the resistance of the top PMOS (limiting the current in the inverter), rise time of the inverter can be controlled, and hence the delay is controlled. There are 6 stages in the delay line and only two stages are shown here.

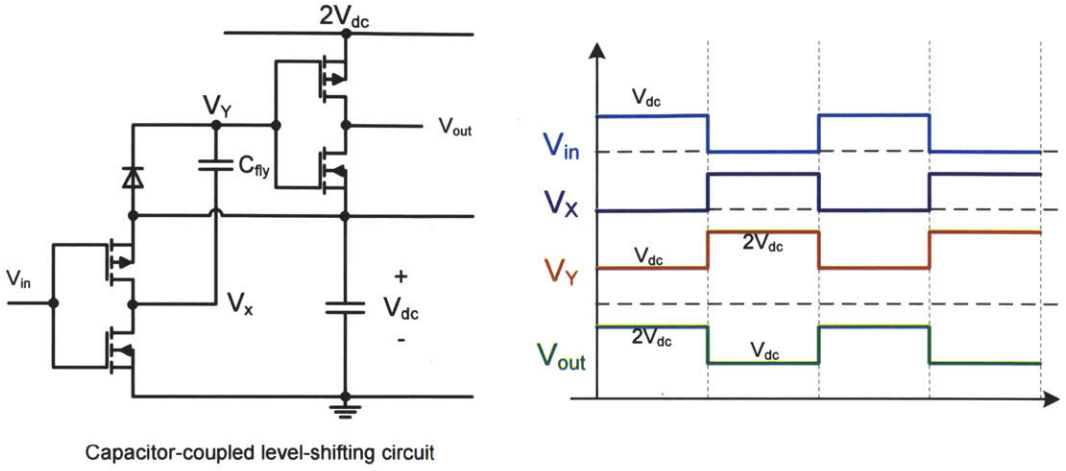


Figure 4-19: The schematic of the level shifting circuit.

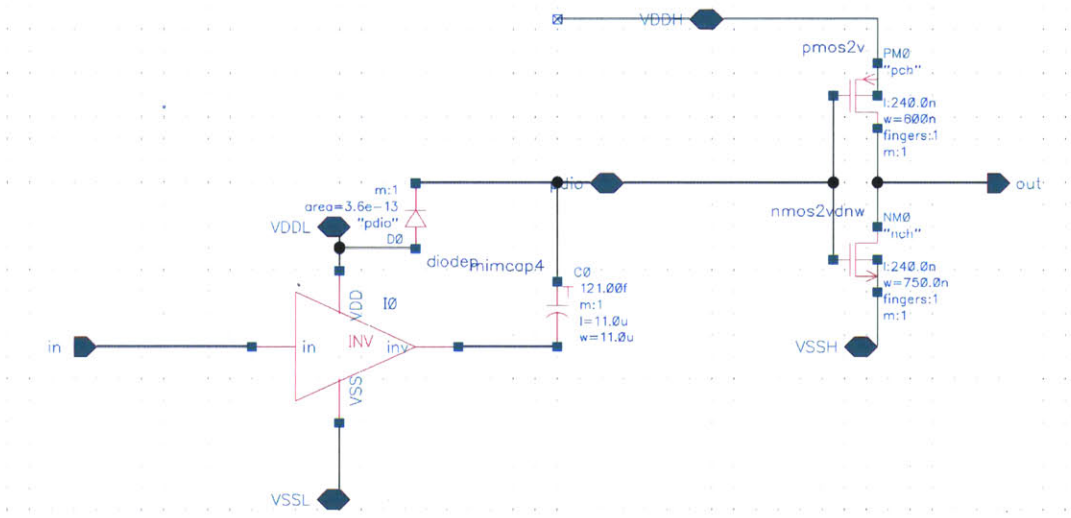


Figure 4-20: The detailed schematic of the level shifting circuit. A 121 fF MiM capacitor is used for the voltage shifting capacitor. The PMOS device in the output inverter stage is sized smaller intentionally to obtain higher threshold voltage for the output inverter.

switched-capacitor rectifier, and a 170 pF deep-n-well NMOS capacitor is integrated for the flying capacitor in the switched-capacitor rectifier. For each of the half-bridge rectifiers, a 280 pF dc decoupling NMOS capacitor is also integrated on die. These capacitors are used to prevent the devices from being damaged by excessive ringing due the package parasitics. These capacitors are over-sized to optimize the layout structure. For sufficient filtering, external 100 nF 0204 ceramic capacitors are also used.

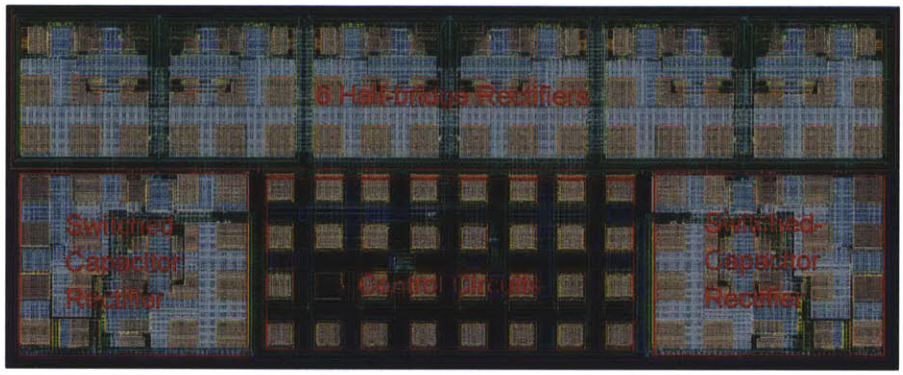
Table 4.2 shows the sizing details and area breakdown of the power MOSFETs and decoupling capacitors in both the switched-capacitor rectifier and conventional bridge rectifier. From the simulation, the switched-capacitor rectifier has 81% peak efficiency at 4 W of output power with switching frequency of 50 MHz and 2.5 V of dc output voltage. This efficiency includes all the logic and gate driver losses, the estimated interconnect loss on the layout and ESR loss on the external decoupling capacitors (60 mΩ ESR on the external 100nF 0204 ceramic capacitors contribute an estimated 13% of the total loss in the SC rectifier system). For the full-bridge rectifier system, the simulated peak efficiency is 87%. Even though the double-ended SC rectifier alone has a lower efficiency as compared to the full-bridge rectifier, its step-down ratio is two times higher. This reduces the burden on the transformation stage while maintaining the same system conversion ratio and gives a better overall system performance. The experimental result in the next section further verifies this conclusion.

To optimize the performance and minimize the parasitic effects in VHF, flip chip packaging is used. The layout and the picture of the die after solder ball bumping are shown in Fig. 4-21. The pad size is 200 μm square with a 350 μm pitch. The total chip size is 6600 μm x 2800 μm (A quarter of the chip is used for test pins).

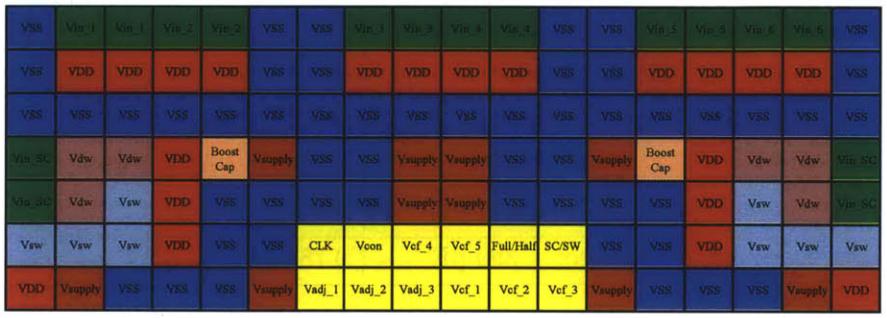
Table 4.2: IC Design Summary

	Devices	**Size**	**Area (mm^2)**	C_{gs} **(pF)**	C_{ds} **(pF)**	R_{on} **(Ω)**
SC	M1	48000 μm	0.085	92	45	85m
Rectifier	M2	23100 μm	0.046	52	23	46m
	M3	23100 μm	0.046	52	23	46m
	M4	48000 μm	0.085	92	45	85m
	M5	45000 μm	0.080	102	45	23m
	Flying capacitor	170 pF	0.33	-		
	Decoupling capacitor	390 pF	0.78	-		
	Efficiency	81%				
Bridge	NMOS device	23100 μm	0.046	52	23	46m
Rectifier	PMOS device	48000 μm	0.085	92	45	85m
	Decoupling capacitor	280 pF	0.51	-		
	Efficiency	87%				

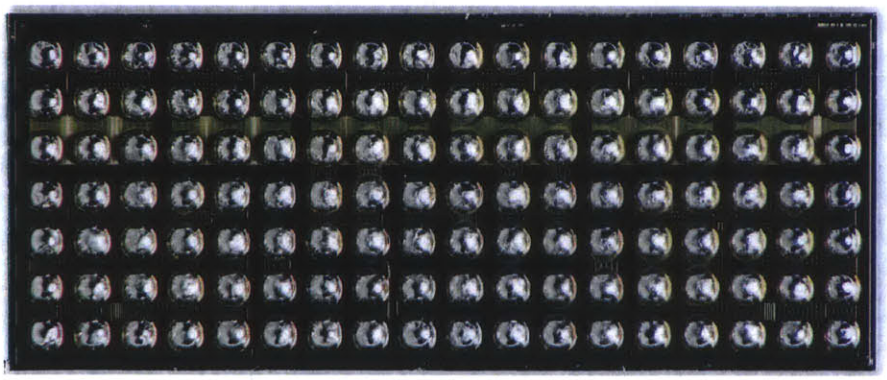
This table shows the detailed sizing for each power MOSFET in both the SC rectifier and bridge rectifier and the area breakdown in both designs. For the bridge rectifier, the design detail is for a single half-bridge rectifier only. There are total six of this half-bridge rectifier on the chip. Reference Fig. 4-4 for the SC rectifier device configuration.



(a) Layout of the rectifier chip



(b) Floorplan of the chip



(c) Flipchip bumping on the die

Figure 4-21: The layout of the rectifier chip as seen from the board side of the IC. The pads of the flip-chip IC are 200 μm square with a 350 μm pitch. The solder balls are 200 μm.

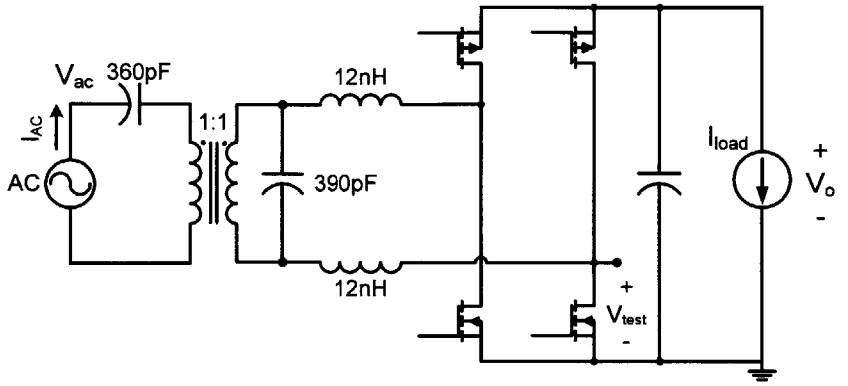
4.4.2 Experimental Results

In order to compare both the performance and operation of the proposed switched-capacitor rectifier and conventional bridge rectifier, two prototype boards were built for the rectifier circuit validation, one with the proposed rectifier and a second implementing a conventional full-bridge CMOS rectifier (The detail PCB schematic and layout are shown in Appendix. A.2, the component types and constructions are shown in Table A.2.). For testing purposes, the very-high-frequency (VHF) ac power is supplied by an RF power amplifier. Both systems have the same operation frequency of 50 MHz and 4 W of output power. The ac input voltages are 20 V (line-to-neutral) and output dc voltages are 2.5 V. As a result, the ac-to-dc voltage conversion ratio in the system is 8:1. Fig. 4-22(a) shows the schematic of the conventional full-bridge rectifier system. 390 pF ATC capacitors and two 12.5 nH Coilcraft Mini Spring air core inductors (A04T_L) were used to form a matching network with a 2π:1 voltage conversion ratio to match the input impedance of the SC rectifier to the 50 Ω output impedance of the power amplifier. Isolation and single-to-double-ended operation is provided by a 1:1 hand-wound transformer with a BLN1728-8A/94 core. There are 7 turns of each winding (30 AWG wire, bifilar wound) on the transformer providing a magnetizing inductance L_m of 1.2 uH and leakage inductance L_l of 30 nH. A 360 pF capacitor is connected in series of the primary side of the transformer for leakage inductance cancellation. The whole system provides an 8:1 voltage conversion ratio from the ac input voltage to the dc output voltage. Fig. 4-22(b) shows the schematic of the double-ended switched-capacitor rectifier system. 180 pF ATC capacitors and two 22 nH Coilcraft Midi Spring air core inductors (1812SMS-22N) were used to form a matching network with a π:1 voltage conversion ratio to match the input impedance of the rectifier to the output impedance of the power amplifier. Since the two-step SC rectifier has twice the step-down voltage conversion ratio as the conventional bridge rectifier, the voltage transformation ratio of the matching network is reduced by half that of the conventional bridge rectifier to achieve the same voltage conversion ratio

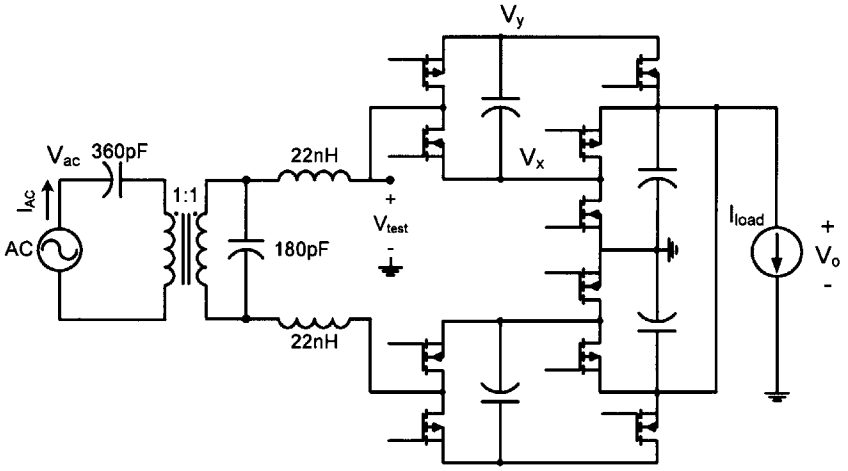
in the overall system. Again, transformer is used for isolation and single to double-ended operation. And a 360 pF capacitor is connected in series of the primary side of the transformer for leakage inductance cancellation.

Fig. 4-23 shows the picture of the SC rectifier system prototype; the conventional bridge rectifier system has the same PCB footprint. Fig. 4-24 shows the switched-capacitor rectifier operating waveforms. In the first step, the node V_x switches between ground and output voltage V_o. In the second step, the node V_y switches between V_o and 2 V_o. As a result, the input of the single-ended switched-capacitor rectifier switches between ground and twice the output voltage V_o, as shown in the center plot of the Fig. 4-24. A 20 V_{peak} ac input voltage waveform and ± 5 V ($2V_o$) voltage swing in the input of the double-ended switched-capacitor rectifier are shown in the bottom plot of Fig. 4-24.

Fig. 4-25 shows the experimental waveforms comparison of both rectifier prototypes. Both systems shown the same 50 MHz 20 V line-to-neutral ac input voltages and 2.5 V output voltages with 4 W of output power. The ground-referenced input of the SC rectifier shows ground to $2V_o$ swing as the input of the conventional rectifier only shows ground to V_o swing (The differential input swings are $\pm 2V_o$ and $\pm V_o$ respectively). The measured overall system efficiency is about 66% for the SC rectifier system, which matches with the calculated performance (estimated transformer efficiency is 90%, matching network efficiency is 93% with an inductor Q of 80 and the SC rectifier efficiency is approximately 81%). However, the overall system efficiency of the conventional full-bridge rectifier is about 63% due to the lower performance of the transformation stage (estimated transformer efficiency is 90%, matching network efficiency is 83% with an inductor Q of 56 and the rectifier efficiency is approximately 87%). (The inductor sizes are kept similar in this comparison; as a result, the inductor Q is different for different inductances). The measurement results confirm that the switched-capacitor rectifier reduces the burden of the matching network to provide high voltage step-down while improving overall system performance. In ad-



(a) Full-bridge rectifier schematic



(b) Double-ended SC rectifier schematic

Figure 4-22: Schematics of the rectifier prototypes. 50 MHz, 20 V ac input voltage, 2.5 V output voltage and 4 W of output power. Drive to the rectifiers in the experimental system is provided by an RF power amplifier. V_{test} is the rectifier input voltage swing measurement point. The component types and constructions are shown in Table A.2.

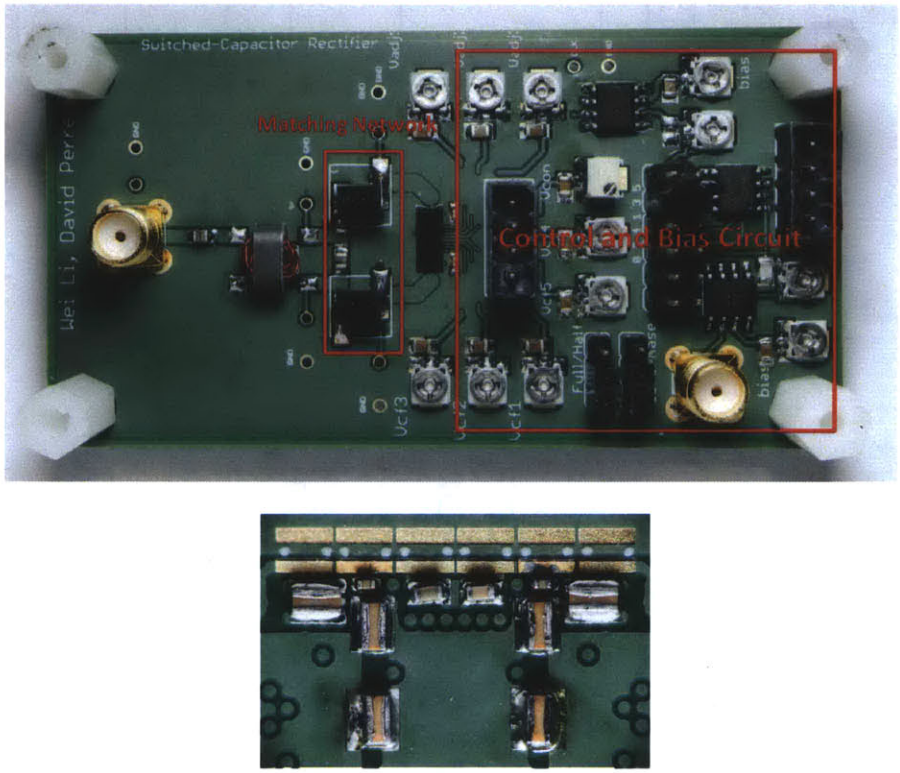


Figure 4-23: Pictures of the switched-capacitor rectifier prototype board. The black rectangle in the middle of the board is the rectifier IC. The lower figure shows the flying capacitors and decoupling capacitors in the back of the chip. They are two 10 nF 01005 capacitors, two 0.1 μF 0201 capacitors and six 0.1 μF 0402 capacitors.

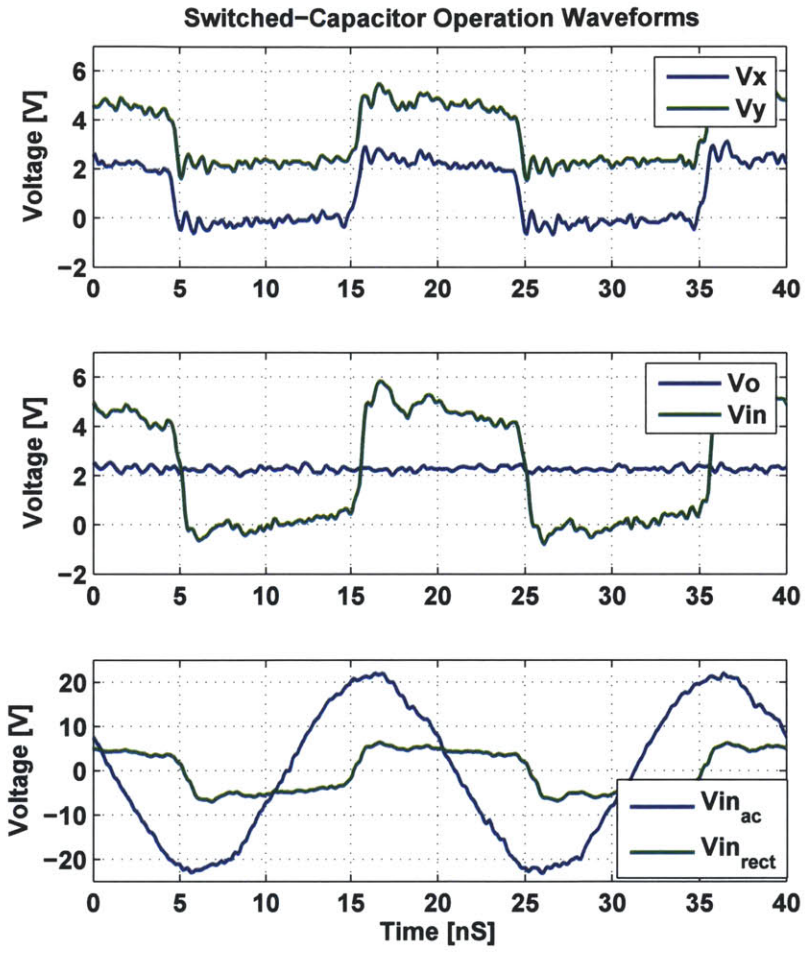


Figure 4-24: Experimental waveforms show the operation of the double-ended switched-capacitor rectifier.

dition, the ESR in the flying capacitors contributes a considerable amount of loss (approximately 13% of the total loss) in the switched-capacitor system due to the high RMS input current. Better capacitor technology (e.g., integrated trench capacitors or high-quality-factor discrete capacitors) with smaller ESR can further improve the SC rectifier efficiency.

4.4.3 Summary and Discussion

This section presents an integrated full bridge two-step switched-capacitor rectifier prototype and successfully demonstrated the concept. The two-step SC rectifier shows twice of step-down ratio compare to the conventional bridge rectifier. As a result, the transformation ratio required in the transformation stage can be reduced by a factor of two, and hence better overall system performance is presented.

Fig. 4-26 shows the two-step SC rectifier performance calculated for different CMOS processes and different operating frequencies (in each case making the output voltage the voltage of the core devices in the process). For comparison purposes, the calculated efficiencies of a conventional CMOS bridge rectifier are also presented. As illustrated, the SC rectifier can achieve much better performance if better CMOS technology is available. At a frequency of 50 MHz, the SC rectifier can achieve 92.5 % efficiency theoretically with the IBM 65 nm process, which is much better than the 81 % efficiency we tested with the TSMC 0.25 μm process. Furthermore, the calculation shows that the efficiency gap between the SC rectifier and bridge rectifier becomes smaller if better device technology is used, which favors the SC rectifier as it provides twice the step-down transformation. It may be concluded that for fine-line processes (as would be used in many applications), the SC rectifier system can achieve even better performance as compared to the bridge rectifier system, since the SC rectifiers provide double the step-down conversion ratio.

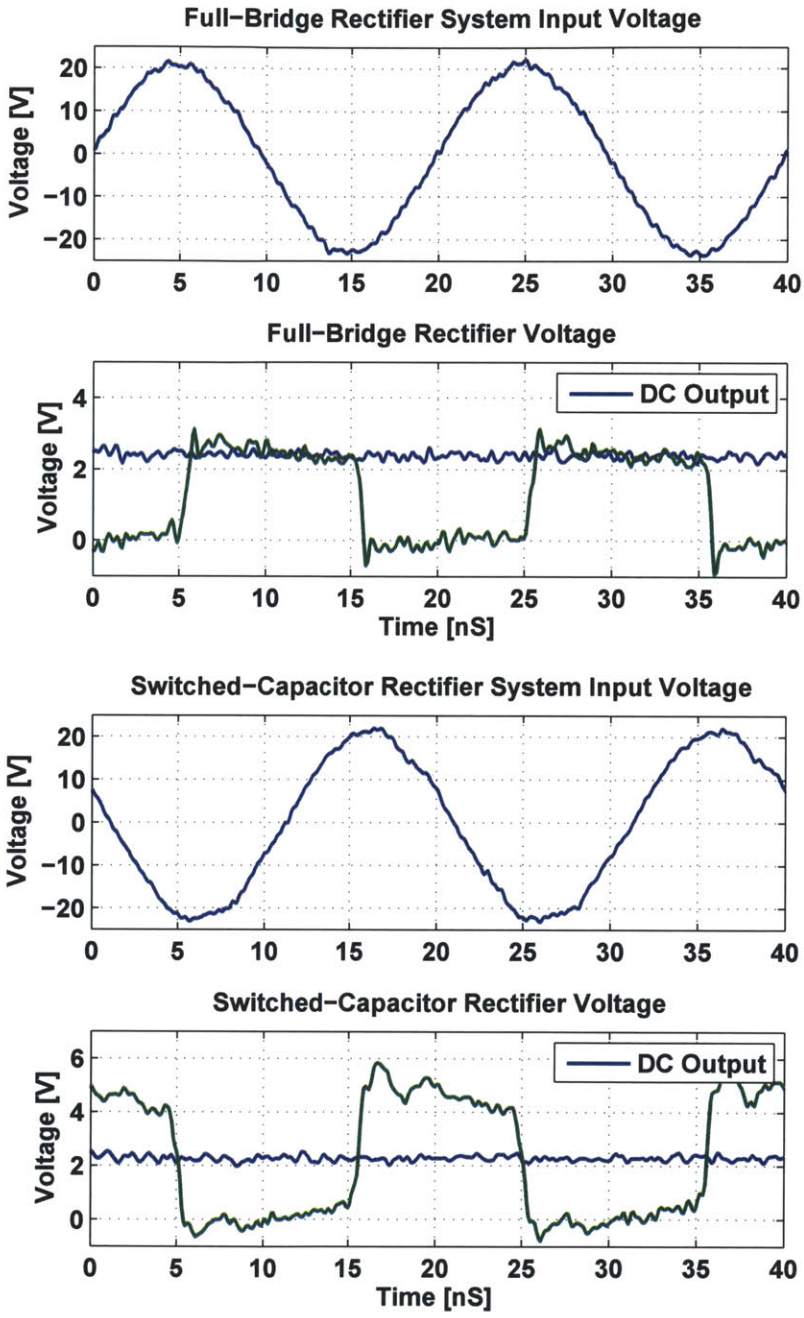


Figure 4-25: Experimental waveforms of the rectifier prototypes. Only one phase of the full-bridge rectifier input voltage is shown here, which is ground referenced. The other phase of the rectifier input voltage is simply shifted by a half cycle from the waveform shown here.

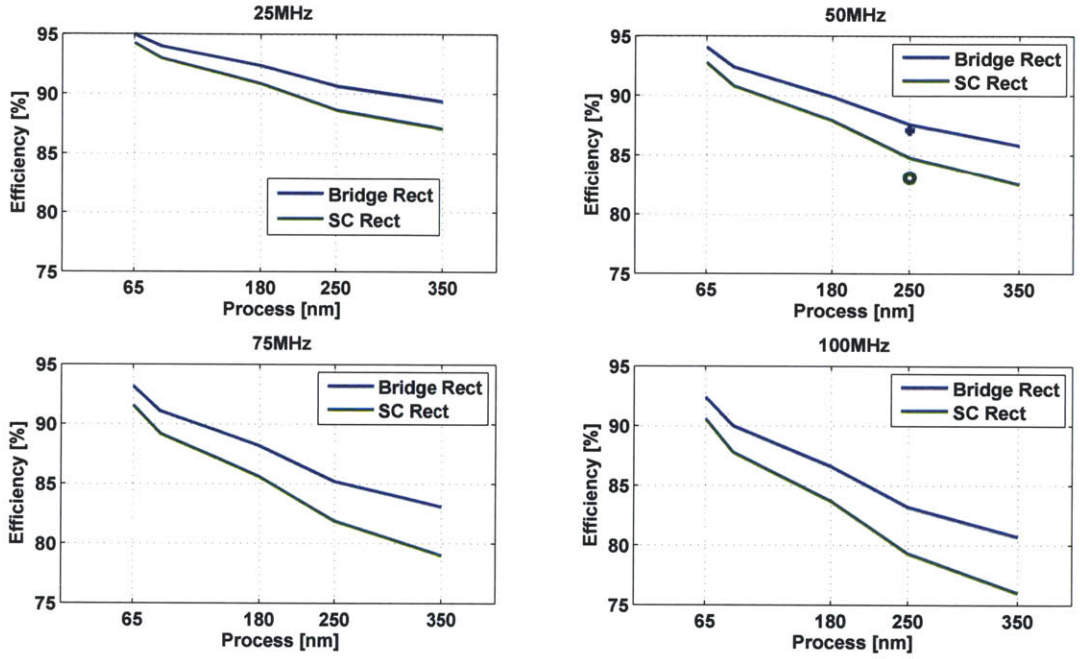


Figure 4-26: This figure shows the rectifiers performance scaling with CMOS processes. The calculation is based on the IBM CMOS technology. Both systems are full bridge CMOS synchronous rectifiers. And the SC rectifiers provide two times voltage step-down conversion ratio compare to the conventional bridge rectifiers. Experimental results are also plotted in the 50 MHz graph to verify the accuracy of the simulation.

4.5 Summary

This chapter presents a switched-capacitor rectifier architecture for very high-frequency synchronous rectification in low-voltage power electronics. By providing large step-down voltage conversion in the rectification stage, the burden in the transformation stage in a dc-dc converter or ac power delivery system is reduced, providing a better performance in the overall system. First, a discrete prototype operating at 10 MHz was designed and built to verify the concept. Following this, an integrated prototype operating at a 50 MHz switching frequency and 2.5 V output voltage was designed and fabricated in a TSMC 0.25 μm CMOS process to demonstrate the functionality and performance benefit of integration. The prototype shows the advantages of the SC rectifier and validates the self-driven scheme in the SC rectifier. The proposed switched-capacitor rectifier provides improved voltage transformation capabilities as compared to a conventional bridge rectifier, making it suitable for applications where high power density and high voltage conversion ratio are desired.

Chapter 5

Hybrid GaN-Si Dc-Dc Converter

In the previous chapters, a new frequency multiplier inverter and a new switched-capacitor rectifier were proposed for VHF step-down power conversion. A hybrid GaN-Si dc-dc converter architecture is presented in this chapter to leverage the advantages of both the inverter stage and rectifier stage for high-power-density step-down applications. The hybrid GaN-Si dc-dc converter prototype consists of a GaN-based frequency multiplier stage, a matching network transformation stage and an integrated switched-capacitor rectifier stage. The converter has an 8:1 voltage conversion ratio with a input voltage of 20 V and a output voltage of 2.5 V. The operating frequency of the converter is 50 MHz and the output power is 4 W. The design details are described in detail in the following sections.

5.1 Matching Network Transformation Stage

Fig. 5-1 shows the fundamental structure of a dc-dc converter. In order to leverage the characteristics of the high-voltage inverter stage and low-voltage rectifier stage, a transformation stage is required. The transformation stage does not just provide additional step-down voltage conversion ratio, but also isolates the high-voltage low-current input from the low-voltage high-current output. With a transformation stage,

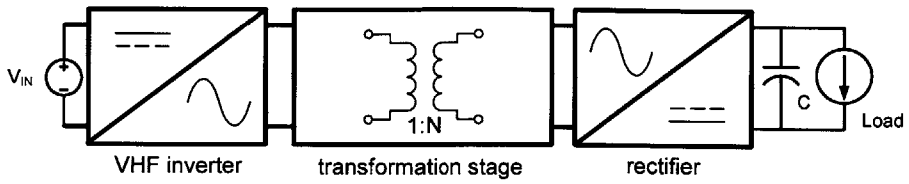


Figure 5-1: General architecture of a dc-dc converter.

the high-voltage high-speed devices (such as GaN devices) can be used for the inverter stage and low-voltage high-speed CMOS devices can be used in the rectification stage. Topologies with a transformation stage (e.g. coupled-inductor buck, flyback, etc.) can operate using only low-voltage rectifier devices. However, they require coupled magnetics (or transformers) which are not readily realized on die. Even though our proposed architecture is not limited to integrated applications only, we focus on implementations that lend themselves to partial or complete integration, especially of the transformation and rectification stages. (Other possible implementations will be readily apparent). Moreover, it is noted that in all such implementations, the inverter devices still must be both fast and high voltage, making this portion of the circuit unavailable in conventional CMOS processes.

An alternative to magnetic transformers for providing voltage transformation is the use of matching networks [65] or immittance conversion networks [66], which require only inductors and capacitors to realize. With the emergence of high-efficiency, high-power-density integrated inductors at very high frequencies (VHF), such as those developed in [10], an efficient integrated transformation stage starts to become practical. In [10], a Q of 66 at 100 MHz was reported, and integrated inductors having Q of over 100 are under development; these quality factors are sufficient for constructing high-efficiency matching networks [1].

5.1.1 Theory and Design

A matching network is a passive two-port circuit designed to provide narrow-band impedance and voltage transformation between the two ports. The fundamental

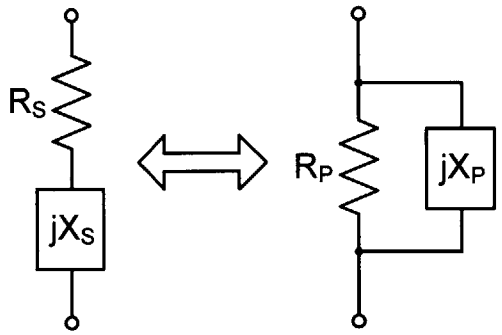


Figure 5-2: Series parallel impedance conversion.

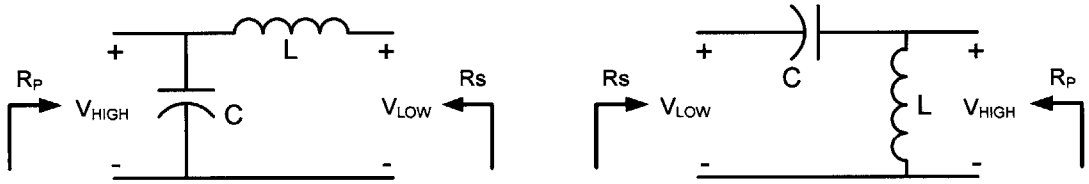


Figure 5-3: Basic matching network topologies.

operation of the matching network is based on the series and parallel RLC network conversion [67]. At a fixed frequency (or a very narrow frequency range near the resonant frequency), if we equate the impedances and quality factor Q of both the series and parallel networks, the series or parallel equivalent RC/LR network can be computed as (The equivalent circuits are shown in Fig. 5-2):

$$R_P = R_S(Q^2 + 1) \tag{5.1}$$

$$X_P = X_S(\frac{Q^2 + 1}{Q^2}) \tag{5.2}$$

where X is the imaginary part of the impedance and R is the real part of the impedance. Based on the above equations, the resistance loading the network, R can be stepped up with a series-to-parallel conversion, and can be stepped down with a parallel-to-series conversion.

In general, there are two basic lumped matching network topologies ("L-sections"). The left of Fig. 5-3 shows the low-pass single-stage L-section matching network and

the right shows the high-pass single-stage L-section matching network. The load impedance can be stepped up or down depending on which port is connected to the load and which is connected to the source. Other topologies such as T or Π matching network (which may be viewed as cascades of equivalent L sections) can also be used for impedance transformation. However, they invariably have lower efficiency than an equivalent L-section network [68] and thus are not considered here. The details of designing matching networks are well studied [68, 67] and are reviewed as follows: By ignoring the parasitic resistances in the passive components (input power is equal to output power), the resistance transformation ratio at the operating frequency can be described as

$$\frac{R_P}{R_S} = \frac{V_P^2}{V_S^2} \tag{5.3}$$

Based on previous equation (5.1), the matching network transformation quality factor can be expressed as

$$Q = \sqrt{\frac{R_P}{R_S} - 1} \tag{5.4}$$

for the series leg, the quality factor is

$$Q_S = \frac{|X_S|}{R_S} \tag{5.5}$$

and the shunt-leg quality factor is

$$Q_P = \frac{R_P}{|X_P|} \tag{5.6}$$

R_S is the matched series resistance; X_S is the series reactance; R_P is the matched shunt resistance and X_P is the shunt reactance. By letting all the quality factors be the same, $Q = Q_S = Q_P$, the matching network reactances can be picked to achieve the desired transformation ratio.

For our applications, only the step-down matching network is considered. So the

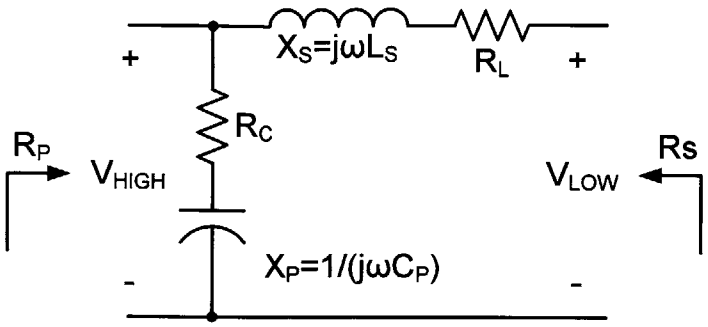


Figure 5-4: L-section step-down matching network with parasitic resistance shown.

series leg of the matching network will be connected to the input of the rectifier stage and the shunt leg of the matching network will be connected to the output of the inverter stage. For communication applications, both inductors and capacitors can be used for the series and shunt reactances. But only an inductor is considered for the series leg in our matching network due to the need for filtering of the rectifier voltage harmonics, which arise from the switched mode operation of the rectifier. The high harmonic contents from the rectifier operation can be filtered out by the matching network and a real impedance load can be provided to the inverter stage by the matching network to optimize the performance.

The matching network efficiency can be estimated by calculating the currents flowing through inductor equivalent resistance R_L and capacitor equivalent resistance R_C [1]. The parasitic resistance in the L-section step-down matching network is shown in Fig. 5-4. When $Q/Q_L << 1$ and $Q/Q_C << 1$, where Q_L is the inductor quality factor and Q_C is the capacitor quality factor, the matching network efficiency can be approximated as

$$\eta \approx 1 - \frac{Q}{|Q_L|} - \frac{Q}{|Q_C|} \tag{5.7}$$

Since the performance of the matching network is proportional to the transformation quality factor Q, multistage matching networks can be used to achieve better performance at the expense of the complexity of the circuit. Fig. 5-5 shows an

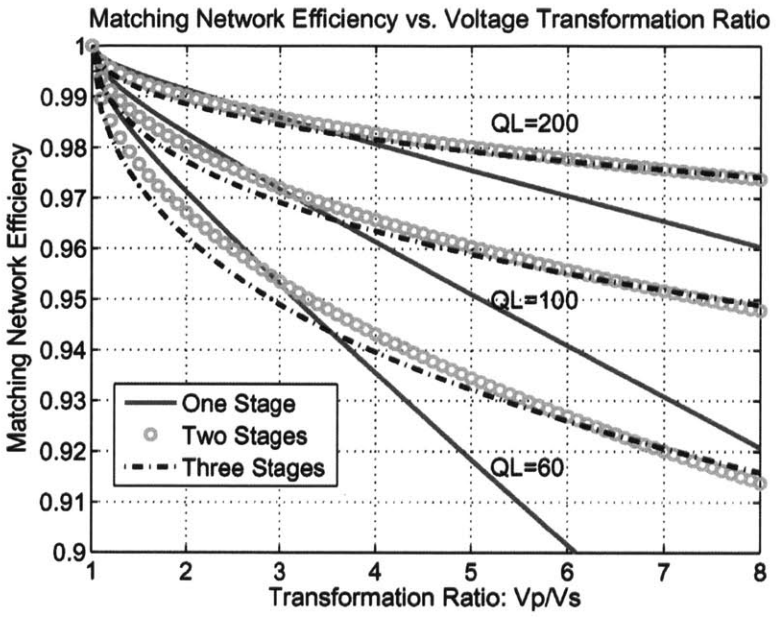


Figure 5-5: High efficiency matching network transformation stage [1].

overview of the matching network efficiency. With an inductor Q of 100, a single stage matching network with 5:1 of voltage transformation ratio can achieve over 95 % of efficiency. As a result, the matching network is very suitable to provide additional voltage transformation for our high-density high voltage-conversion-ratio converter.

5.1.2 Power Density Optimization

With a fixed voltage conversion ratio and given technologies for passive components, the output power level can be chosen to optimize the power density of the matching network. Fig. 5-6 shows an example of the area trade off in the matching network for an exemplary system having a 6:1 ac to dc voltage conversion ratio. In this example, a TSMC 1 nF/mm^2 MiM capacitor process (with 19 V blocking voltage) is used for calculation and thin-film v-groove magnetics (L=1.7 nH/mm, width=212 μm and Q of 66 @ 100MHz) [10] are used for matching network inductors. The ac input voltage of the matching network is 6 V from line to neutral (12 V_{pk} line-to-line

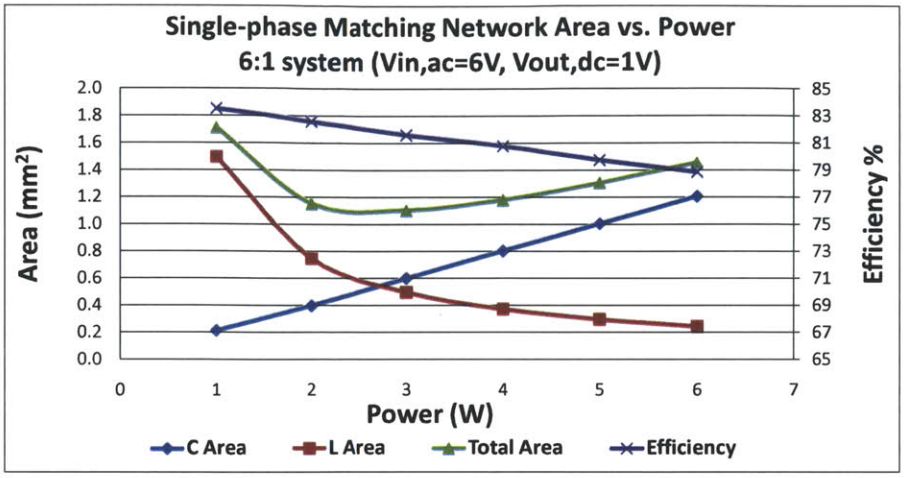


Figure 5-6: This plot shows the area trade-off in the matching network for an exemplary ac power delivery system. With a given technology for passive components and voltage transformation ratio, the optimal power density of the matching network is output power dependent.

voltage) and the dc output voltage of the rectifier is 1 V. The voltage transformation ratio of the matching network is thus (3π):1 and the full bridge rectifier provides a fundamental amplitude ac-to-dc conversion of $(2/\pi)$:1. The plot shows that the inductor area dominates the total system area when the output power is less that 2 W. The optimal density is obtained at about 2.3 W when the areas of L and C are balanced. When the output power is larger than the optimal power, capacitor area becomes the major portion of the total system area. In addition, efficiency of the system degrades due to smaller Q in the larger capacitors as the output power increases. The achievable power density of the matching network transformer exceeds 2 W/mm^2 with these typical passive technologies. (The Matlab matching network components calculation code is shown in Appendix. B.2). Of course, one can also resort to tapped inductors or transformers to provide voltage transformation, and can also apply a combination of these methods (e.g., using the transformer leakage as part of a matching network).

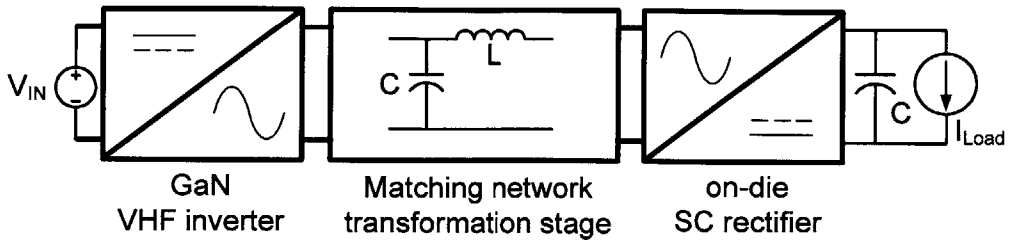


Figure 5-7: Proposed high power density high step-down ratio dc-dc converter architecture.

5.2 50 MHz Dc-dc Converter Prototype

The matching network transformation stage, the GaN frequency multiplier and the low-voltage integrated CMOS switched-capacitor rectifier can be combined to create a whole dc-dc converter. The proposed converter structure is shown in Fig. 5-7. The GaN frequency multiplier converts the high input dc voltage into VHF ac output with a step-down conversion ratio, and then the matching network isolates the high-voltage input from the low-voltage load and provides additional step-down voltage conversion. Lastly, the switched-capacitor rectifier converts the rf ac power back to dc output for the load, while providing further voltage step down. With the possible GaN-on-Si technology, this architecture can also provide a fully integrated dc-dc converter solution for low-voltage applications. Both the non-isolated and isolated converter prototypes were built to demonstrate the feasibility of the hybird GaN-Si dc-dc converter architecture. (The detailed PCB schematics and layouts are shown in Appendix. A.3)

5.2.1 Non-isolated Prototype

The schematic of the non-isolated dc-dc converter prototype is shown in Fig. 5-8. The prototype dc-dc converter operates at 50 MHz, over ten times the frequency of state of the art designs in this range. The input voltage is 20 V and the output voltage is 2.5 V. The output power of the converter is 4 W. The output power and output voltage are chosen based on the switched-capacitor IC design. The detailed

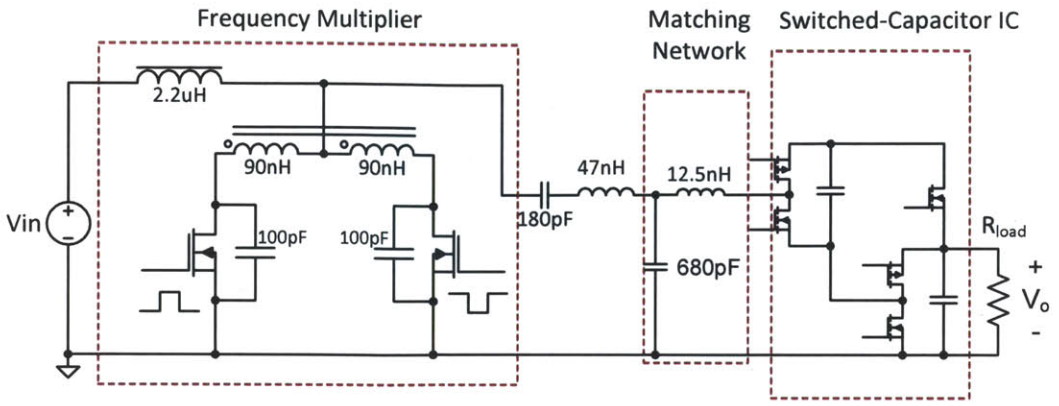


Figure 5-8: The schematic of the non-isolated dc-dc converter prototype. Information about the individual components and operating frequency are summarized in Table A.3.

design of the GaN frequency multiplier and integrated switched-capacitor rectifier in the 0.25 μm TSMC process were explained in Chapters 3 and 4, and detailed component design and selections are summarized here in Table A.1 and A.2. The GaN frequency multiplier is switched at 25 MHz and outputs 50 MHz ac power. 180 pF ATC capacitor and 47 nH Coilcraft Midi Spring air core inductor were used for the series resonant tank in the output of the inverter to extract the second harmonic for the output. The inverter provides an approximately 3:2 step-down conversion ratio between the 20 V dc input voltage and the 13 V peak ac fundamental output voltage. 680 pF ATC capacitor and 12.5 nH Coilcraft Mini Spring air core inductor were used for the L-section matching network to provide additional 4π:3 step-down voltage conversion ratio for the converter. Lastly, the half-bridge switched-capacitor rectifier provides a fundamental ac-to-dc conversion of $4/\pi$:1. Thus the converter has an overall 8:1 dc-to-dc step-down ratio.

Fig.5-9 shows the picture of the 50 MHz non-isolated GaN-Si dc-dc converter prototype board and Fig.5-10 shows the measured waveforms of the converter. As illustrated, the GaN inverter switches at 25 MHz with 4 V gate drive signals. The peak drain voltage for the GaN power device is about 65 V with a 20 V dc input voltage. The inverter outputs a 50 MHz ac voltage with amplitude of 13 V. There is a 2.5 V dc offset in the ac voltage due to the dc offset from the input of the rectifier. In

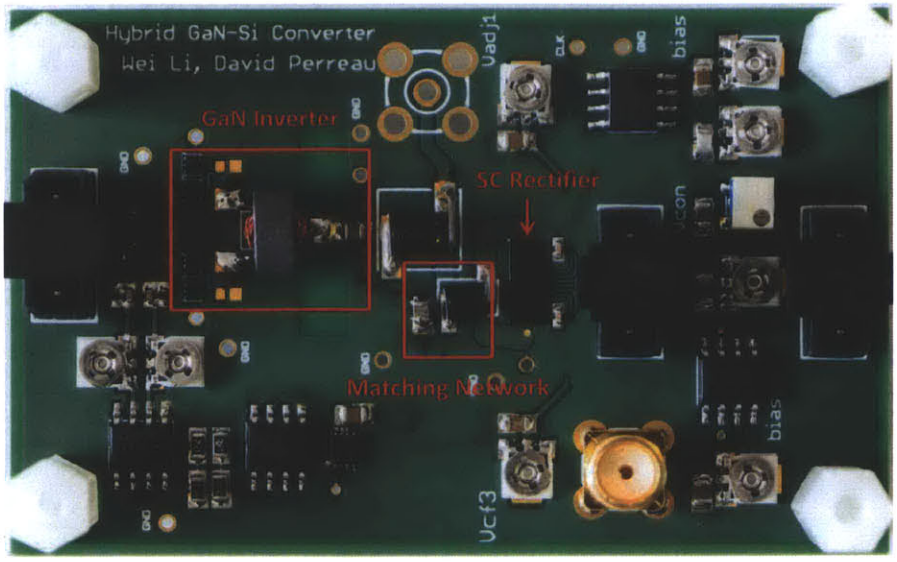


Figure 5-9: Picture of the 50 MHz non-isolated GaN-Si dc-dc converter.

addition, the measurement shows ground to $2V_o$ (5 V) voltage swing in the input of the half-bridge switched-capacitor rectifier. The overall converter efficiency is about 58 % with an output power of 4W, which matches with the estimate. (GaN frequency multiplier inverter efficiency is 92 %, matching network efficiency is 80 % and the SC rectifier efficiency is 81 %). The major loss breakdown is due to the poor Q from the commercial air core inductors (for the 12.5 nH Coilcraft Mini Spring air core inductor, Q's of 40 were measured) and the SC rectifier , which is realized with older-generation CMOS technology. It is noted that the converter here is to demonstrate the feasibility of the new VHF GaN-Si dc-dc converter architecture. Impelementation of the converter with state-of-the-art integrated thin film magnetics and modern CMOS technology can achieve much better performance.

5.2.2 Isolated Prototype

An isolated version of the hybrid GaN-Si dc-dc converter prototype was also built and tested to valid the concept for applications where isolation is required. The schematic of the isolated version of the dc-dc converter prototype is shown in Fig. 5-11, with

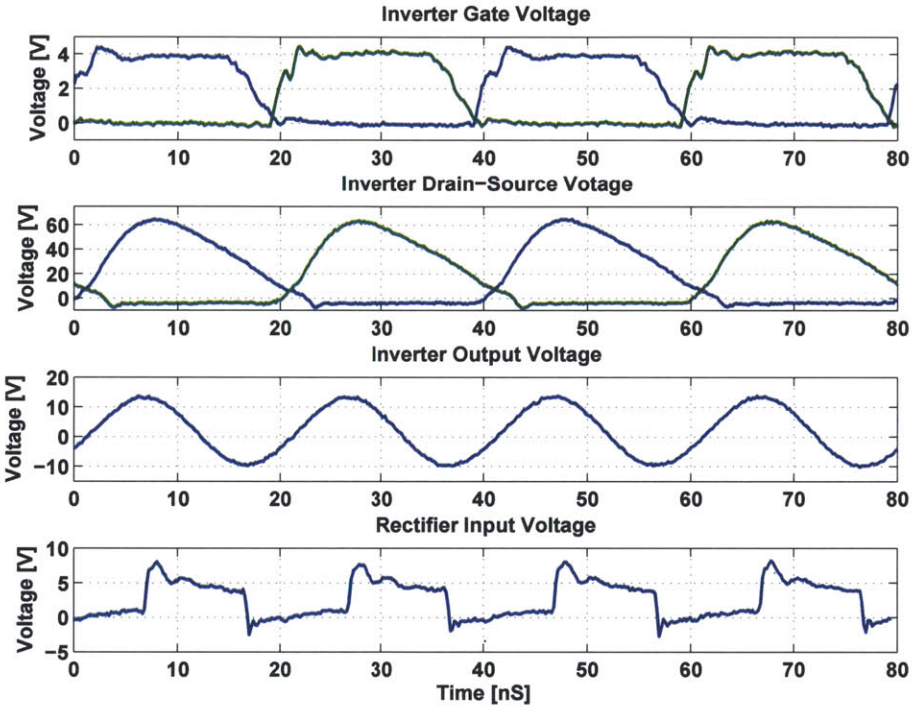


Figure 5-10: Experiment result for the 50 MHz non-isolated GaN-Si dc-dc converter. The input voltage is 20 V and the output voltage is 2.5 V. Output power is 4 W and the operation frequency is 50 MHz. The inverter output voltage is about 13 V and the input of the SC rectifier switches between 0 V and $2V_0$, which is 5 V.

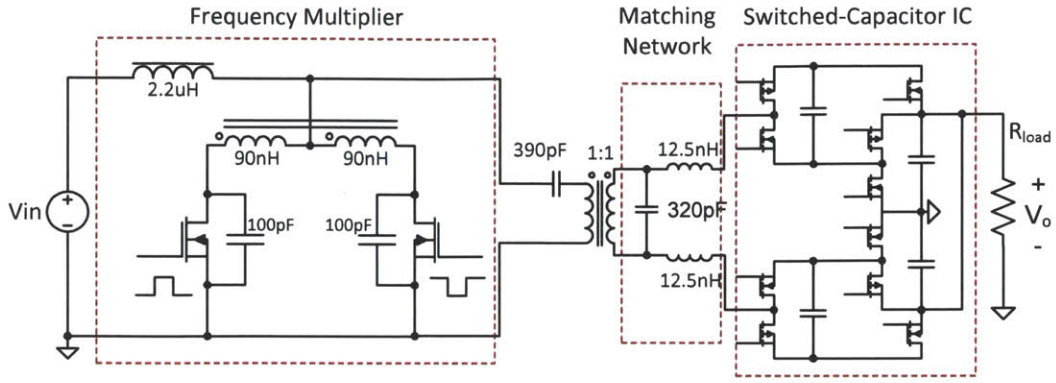


Figure 5-11: The schematic of the isolated dc-dc converter prototype. Information about the individual components and operating frequency are summarized in Table A.4.

detailed component designs and values indicated in Appendix. A.3. The isolated converter has the same specification as the non-isolated converter. The operation frequency is 50 MHz; input voltage is 20 V; output voltage is 2.5 V and output power is 4 W. The isolation is provided by a 1:1 hand-wound transformer with a BLN1728-8A/94 core. There are 8 turns of each winding (30 AWG wire, bifilar wound) on the transformer providing a magnetizing inductance L_m of 1.8 uH and leakage inductance L_l of 30 nH. The leakage inductance is absorbed as the resonant inductor for the output filter of the GaN frequency multiplier inverter and 390 pF ATC capacitor is used for this series resonant tank. Since isolation is provided, a full-bridge SC rectifier is used for the rectification stage to double the voltage swing in the input of the rectifier and further reduce the burden on the matching network. Again, the inverter provides an approximately 3:2 step-down conversion ratio between the 20 V dc input voltage and the 13 V peak ac fundamental output voltage. 320 pF ATC capacitor and two 12.5 nH Coilcraft Mini Spring air core inductors were used for the full-bridge matching network to provide additional 2π:3 step-down voltage conversion ratio for the converter. In the end, the full-bridge switched-capacitor rectifier provides a fundamental ac-to-dc conversion of $8/\pi$:1. Thus the converter has an overall 8:1 dc-to-dc step-down ratio.

Fig. 5-12 shows the picture of the 50 MHz isolated GaN-Si dc-dc converter pro-

totype board and Fig.5-13 shows the measured waveforms of the converter. Again, the GaN inverter switches at 25 MHz with 4 V gate drive signals. The peak drain voltage for the GaN power device is about 65 V with a 20 V dc input voltage. The inverter outputs a 50 MHz ac voltage with amplitude of 13 V. As a contrast to the half-bridge SC rectifier, the measurement shows -$2V_0$ and +$2V_0$ voltage swing ($\pm$5 V) in the input of the full-bridge switched-capacitor rectifier. The overall converter efficiency is about 61 % with output power of 4W. (The modeled GaN frequency multiplier inverter efficiency is 92 %, estimated transformer efficiency is 90 %, matching network efficiency is 93 % and the SC rectifier efficiency is 81 %). The isolated version of the hybrid GaN-Si dc-dc converter actually has better performance compared to the non-isolated version. Due to the low Q inductors, the system has better performance when the transformation ratio in the matching network is reduced by half, even with compromising the extra loss from the isolation transformer. This further demonstrated that the importance of providing step-down conversion ratio in each stage to reduce the burden in the transformation stage in high density power conversion when the performance of the passive components is limited.

Since the converter system requires impedance matching and resonance, regular PWM control will not work for this converter. Instead, on-off control can be implemented easily for power regulation. Such on-off control has been demonstrated to work well with resonant converters [45, 47].

5.3 Summary

This chapter presented the hybrid GaN-Si dc-dc converter architecture incorporating a matching network transformation stage. The frequency multiplier inverter and the switched-capacitor rectifier both provide voltage step-down conversion ratio to reduce the burden in the matching network transformation stage. The matching network transformation stage provides high power-density voltage conversion and separates

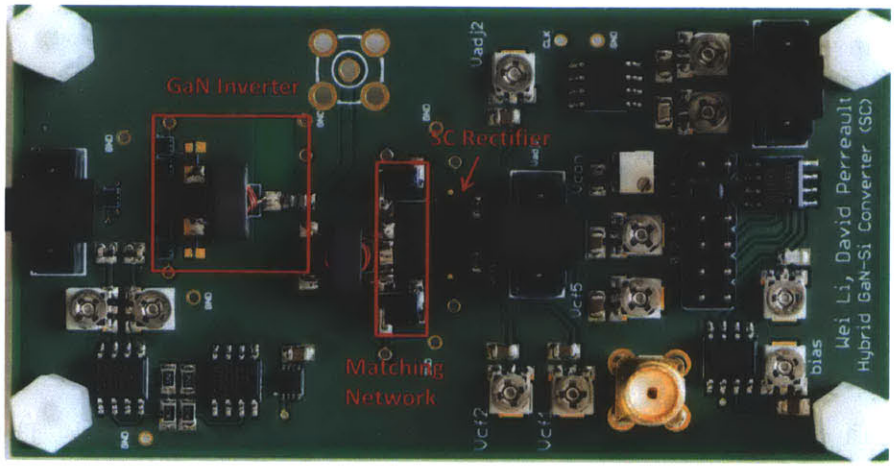


Figure 5-12: Picture of the 50 MHz isolated GaN-Si dc-dc converter.

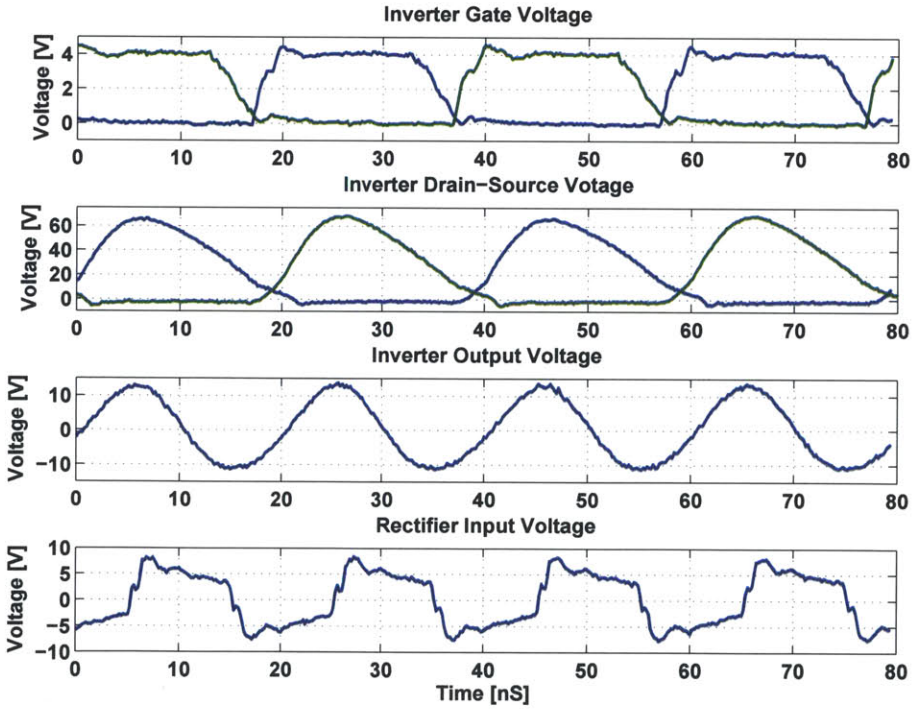


Figure 5-13: Experiment result for the 50 MHz isolated GaN-Si dc-dc converter. The input voltage is 20 V and the output voltage is 2.5 V. Output power is 4 W and the operation frequency is 50 MHz. The inverter output voltage is about 13 V and the input of the SC rectifier switches between $-2V_0$ and $+2V_0$, which is ± 5 V.

the rectifier stage from the high input voltage. In this case, high-speed high-voltage GaN device can be used in the high voltage inverter stage and high-speed low-voltage CMOS devices can be used in the rectifier stage. Both non-isolated and isolated version of the 50 MHz converter prototype were designed and built to demonstrate and verify the concept. The proposed dc-dc converter architecture is suitable for low-voltage portable electronics and applications where high power density and high voltage conversion ratio are desired. In the next chapter, we also show a different way to leverage this converter architecture to provide ac power delivery for microprocessors to reduce pin count and interconnect loss.

Chapter 6

Ac Power Delivery

Future computation systems pose a major challenge in energy delivery that is difficult to meet with existing devices and design strategies. To reduce interconnect bottlenecks and enable more flexible computation and energy utilization, it is desired to deliver power across the interconnect to the chip at high voltage and low current with on- or over-die transformation to low voltage and high current. Based on the converter introduced in the last chapter, this chapter presents an integrated converter architecture with high-voltage, high-frequency power delivery across the interconnect, with on-die transformation and rectification to power low-voltage digital loads.

6.1 Architecture

During the "War of Currents" era in the late 1880s, George Westinghouse and Thomas Edison became adversaries due to Edison's promotion of low-voltage direct current (dc) for the electric power distribution over alternating current (ac) supported by Westinghouse [69]. However, Edison's dc system suffered two major disadvantages: 1. The distribution range was limited and the cost penalty of the large required amount of conductor was high; 2. Higher distribution voltages could not easily be used with the dc system because there was no efficient, low-cost technology that would

allow reduction of a high transmission voltage to a low utilization voltage. On the other hand, in the alternating current system, a transformer could be used to locally step down a high distribution voltage to low voltages for customer loads. With the ease of changing voltages using a transformer, a high-voltage, low-current ac system can greatly reduce the conduction loss and conductor cost in transmission, which is what led the ac power delivery to become the dominant electric-power transmission system.

Today, delivery of power to microprocessors represents a similar challenge. Delivery of power to the die at the final very low voltage requires a dominant portion of the chip pin count, that could be better employed for computation and communication. Moreover, the present system leads to challenges of voltage control (drop) and conductor loss both on die and in the interconnect to the die. The difficulties of making efficient high-conversion-ratio dc-dc converters on die provides a similar barrier to high-voltage distribution and local conversion as in the war of the currents, but on a different scale.

As in the war of the currents, another possibility is high-voltage ac distribution across the interconnect, with local (on-die) transformation and rectification. Indeed, a version of this general idea has been proposed previously [18], but without any enabling means of realizing the high-frequency on-die magnetic transformers that would be required. This limitation aside, ac distribution in this application has important merits: It allows high-voltage and low current distribution, allows the use of low-voltage CMOS rectifiers on die, and enables the inverter to be placed off die where size and loss are less important and where it can be effectively realized in a non-CMOS device process.

However, with a remote inverter stage, our proposed GaN-Si converter architecture with matching network transformation stage meets all the ac power distribution requirements above. A complete ac power delivery architecture (Fig. 6-1) is proposed here for a low-voltage integrated power delivery system. High-voltage discrete power

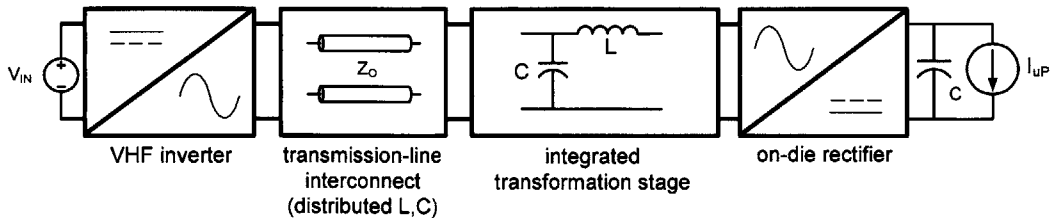


Figure 6-1: Architecture of an ac power delivery system.

devices (e.g., GaN transistors) can be used for the VHF inverter stage off die, generating high-voltage, low-current power at VHF frequencies (e.g., 50-100 MHz) which is delivered across the interconnect. Integrated passives form a matching network for the transformation stage, converting the VHF power to low voltage and high current. Integrated rectifiers using native low-voltage CMOS devices transform the waveforms back to dc, completing the power conversion system. To the authors' knowledge, aside from the author's recent paper [58], no in-depth analysis of the proposed ac power delivery architecture has been published, nor has the feasibility of the approach been validated. Here we present a detailed investigation of the achievable performance of such a system within currently available technology, along with a trade-off comparison among different implementation options. This chapter also presents an experimental validation of the feasibility of VHF ac power delivery using a discrete-component prototype system and an integrated circuit prototype.

6.2 Interconnect Loss Analysis

Fig. 6-2 shows a framework for comparing loss among dc and ac delivery systems. Let both systems have the same output voltage V_o and same output power P. In order to compare the interconnect loss fairly, also let both systems have the same amount of area for interconnect conductor, with unit sheet resistance R. We first make a comparison without a transformation stage between the input and load. For the dc system, there are only two conductors for power delivery and (6.1) shows the current and power loss for the interconnect. For the ac system, consider use of a

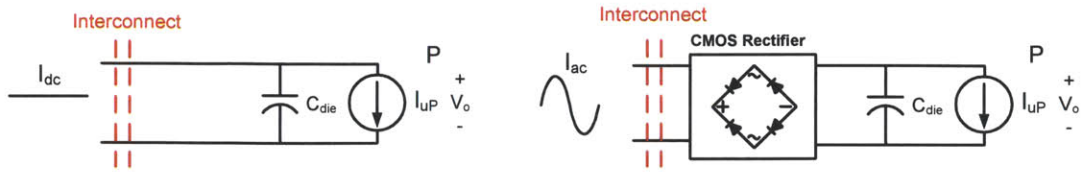


Figure 6-2: System for comparison of ac and dc interconnect loss. It is assumed that each system has the same interconnect area, the same output voltage V_o and same output power P.

full bridge rectifier, with sinusoidal current in the interconnect. Equation (6.2) shows the amplitude of the ac current in the conductor and power loss in the interconnect. Without any transformation, single-phase ac power delivery has 23% more conduction loss than the dc power system. However, with a high-performance integrated ac transformation stage, interconnect loss will be reduced by the square of the voltage transformation ratio.

$$I_{dc} = \frac{P}{V_o}$$
$$P_{Loss} = 2 \times I_{dc}^2 \times 2R = 4\frac{P^2 R}{V_o^2} \tag{6.1}$$

$$I_{ac} = \frac{\pi P}{(2V_o)}$$
$$P_{Loss} = 2 \times \frac{1}{2} I_{ac}^2 \times 2R = \frac{\pi^2}{2}\frac{P^2 R}{V_o^2} \tag{6.2}$$

Fig. 6-3 shows a simple schematic of a single phase ac power delivery system with a full bridge (CMOS) rectifier. Full bridge rectification doubles the voltage swing at the rectifier input, reduces the current through the devices and increases the input impedance of the rectifier. This can give us more favorable passive values for the matching network in high output power applications. In addition, the voltage transformation ratio required for the matching network is reduced by a factor of 2 when

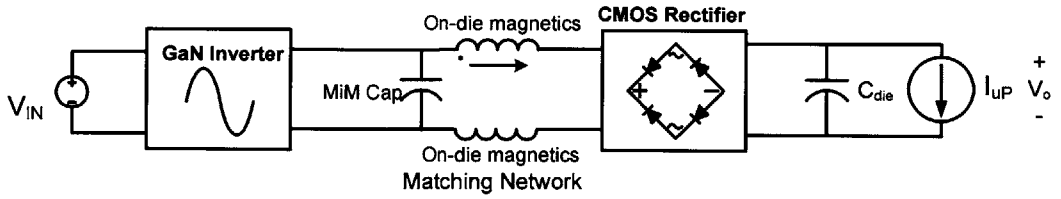


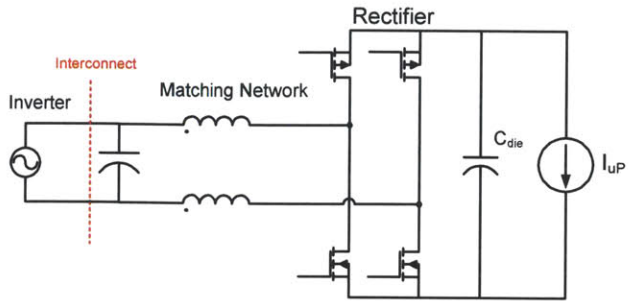
Figure 6-3: Sample schematic of an ac power delivery system. Diodes are shown for illustration purposes only; a synchronous CMOS rectifier would be used for an integrated circuit implementation.

the overall conversion ratio is held constant, which will give better performance in the matching network. While the above work illustrates the promise of ac power delivery, this thesis also explores methods to greatly improve achievable performance including the use polyphase VHF power delivery and matching network voltage transformation.

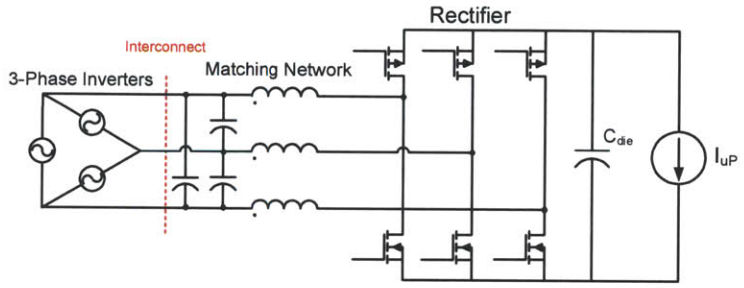
6.3 Polyphase System

In conventional ac power distribution systems, polyphase power transmission is normally used to reduce conduction loss and harmonics in the ac system and energy buffering/filtering requirements at the load. These advantages can also be leveraged in our integrated ac power delivery system. We also consider size and performance trade-offs for such polyphase VHF systems. In this comparison, a 1 V output voltage is chosen. An operation frequency of 100 MHz and an output power of 2 watts is used to optimize the values of passive components for integration purposes. (This power level can represent that of a small zone in a microprocessor, or that of an entire low-power digital IC). Four different kinds of polyphase systems are used in this comparison: single-phase full bridge (two-phase 180° system), 3-phase, 4-phase and 6-phase. The schematic of each system is shown in Fig. 6-4.

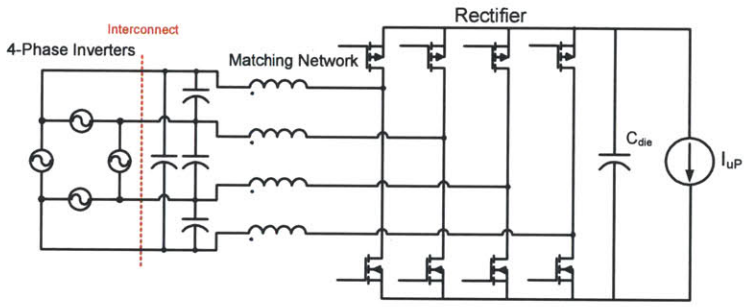
Matching networks are not traditionally employed in polyphase systems. However, we consider their designs here. For a polyphase "L-section" matching network, each phase branch has one series element and one shunt element. However, the shunt elements may be "delta" or "star" connected. Fig. 6-5 shows two configurations of



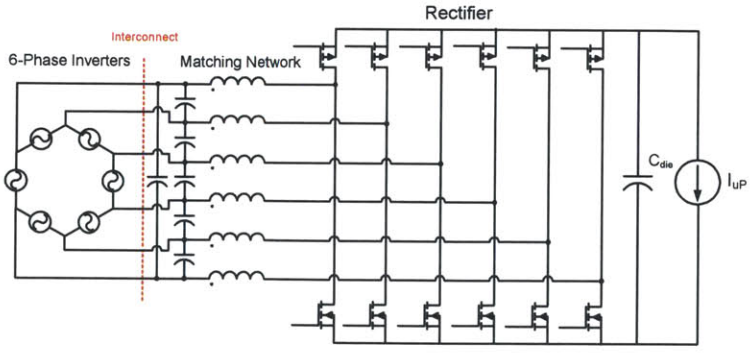
(a) Single phase full bridge



(b) Three phase delta source



(c) Four phase delta source



(d) Six phase delta source

Figure 6-4: Polyphase power delivery systems.

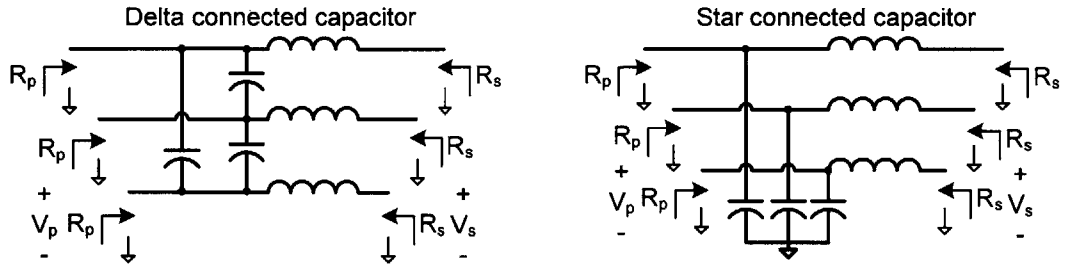


Figure 6-5: This plot shows two configurations of a polyphase matching network connection. The left matching network is with delta-connected shunt elements (capacitors) and the right one is with star ("wye"/"y") connected shunt elements (capacitors). (The Y-point may be left floating or connected to a fixed potential.)

a 3-phase matching network. For the matching network with star connected capacitors, the fundamental ac voltage at the "y" point is zero in balanced polyphase, but harmonics may exist. Depending on design choices and constraints, this center point can float or be connected to a fixed potential. Consequently, substrate-referenced capacitors can be used in the star system, but not the delta system. The values of the matching network elements with star-connected capacitors can be calculated from equations (6.3) and (6.4):

$$Q_T = \sqrt{(R_p/R_s - 1)} = \sqrt{(V_p^2/V_s^2 - 1)} \tag{6.3}$$

$$L = \frac{Q_T R_s}{(2\pi f)}; \quad C = \frac{Q_T}{R_p(2\pi f)} \tag{6.4}$$

where V_P and R_P are the voltage and input impedance seen from the input ("high-voltage") side and V_S and R_S are the voltage and impedance seen at the output ("low-voltage") side.

The values of the matching network elements with delta connected capacitors can be calculated from equations (6.5) and (6.6):

$$Q_T = \sqrt{(R_p/R_s - 1)} = \sqrt{(V_p^2/V_s^2 - 1)} \tag{6.5}$$

$$L = \frac{Q_T R_s}{(2\pi f)}; \quad C = \frac{Q_T}{R_p(2\pi f)[2sin(\frac{\pi}{m})]^2} \tag{6.6}$$

where m is the number of conductors (and half bridge rectifiers).

From equations (6.4) and (6.6), we can see that both the star connection and delta connection require the same inductor value for a given voltage conversion ratio. However, the values of capacitors in the delta shunt matching network are a factor of $1/[2sin(\frac{\pi}{m})]^2$ times those appearing in the star-connected shunt network, so are smaller-valued for less than m=6 phases (or half bridge rectifiers) and have the same value for m=6. On the other hand, the capacitors in the delta network have voltage ratings that are $2sin(\frac{\pi}{m})$ times those in the star network, requiring higher blocking voltage for less than m=6 phases (The required shunt-element energy storage is identical for the two networks). Some example data is shown in Table 6.1. The capacitor density usually decreases as the blocking voltage rating increases due to the thicker required insulation layer. Even though the delta-connected capacitor matching network requires smaller capacitance, the overall power density may not be higher due to the higher blocking voltage requirement. So the preferred polyphase matching network configuration depends on available capacitor characteristics.

In this polyphase system comparison, the total area for interconnect conductor is fixed for all systems, with unit sheet resistance R. According to equation (6.7), for the same power output and with ac sources connected off die, without considering any matching network voltage transformation, all polyphase systems have the same interconnect loss as long as they have the same line-to-neutral voltages. However, the capacitor blocking voltage will be different in different matching network configurations even with the same line-to-neutral voltages.

Table 6.1: Capacitor breakdown voltage requirement for a polyphase matching network system with 1V dc output

Ratio	Phases	Line to line	Line to ground
2.5:1	Full Bridge	5	2.5
	3-phase	4.3	2.5
	4-phase	3.5	2.5
	6-phase	2.5	2.5
4:1	Full Bridge	8	4
	3-phase	6.9	4
	4-phase	5.7	4
	6-phase	4	4
6:1	Full Bridge	12	6
	3-phase	10.4	6
	4-phase	8.5	6
	6-phase	6	6

"line to ground" is the amplitude of the ac component of the line-to-ground voltage on each phase, "line to line" is the amplitude of the line-to-line voltage difference between adjacent phases, which is $2sin(\frac{\pi}{m})$ *times the line-to-ground voltage.*

$$I_{ac} = \frac{\pi P}{(mV_o)}$$
$$P_{Loss} = m \times \frac{1}{2} I_{ac}^2 \times mR = \frac{\pi^2}{2} P^2 \frac{R}{V_o^2} \tag{6.7}$$

For integrated metal-insulator-metal (MiM) capacitors, SiO_2 is usually used for the dielectric, and the maximum blocking voltage depends on the thickness of the SiO_2. With a higher breakdown voltage rating, the required thickness (d) of the SiO_2 is larger since the maximum breakdown field of the SiO_2 is around 5.6MV/cm [70], and the capacitor density will be lower due to $C = \epsilon A/d$ (ϵ is the permittivity of the dielectric, A is the area of the capacitor and d is the insulation thickness). Moreover, the selection of the integrated capacitors is normally limited by the process. A typical TSMC MiM capacitor has a capacitance density of 1 nF/mm^2, and - based on density

characteristics, and material parameters - has a capacitor breakdown rating estimated to be as high as 19 V. According to Table 6.1 above, for a 6:1 voltage conversion ratio in the matching network, the maximum blocking voltage required for the capacitor among all polyphase systems is 12 V, well below the estimated 19 V breakdown voltage rating in the TSMC 1 nF/mm^2 MiM capacitor. As a result, a matching network with delta-connected capacitors is used to optimize the power density in this typical case.

The total system area computed in our comparison includes the area of the matching network, rectifier and output decoupling capacitor. Inductor information is all based on Di's result in [10]. 1 nF/mm^2 MiM capacitors are assumed for the matching network capacitors. (Metal resistance of the MiM capacitor is estimated for the matching network performance calculation). A MOS capacitor is used for the output decoupling capacitor (estimate capacitance density of 5 nF/mm^2 with breakdown voltage of 1 V). Semiconductor size and performance are calculated based on an IBM 65nm process. Since the output power is the sameamong the design options, the total rectifier device area is the same for all systems. In addition, rectifier device losses are also the same, but output ripple and filtering requirements are different. While this results in reasonable design trade-offs, better performance could be achieved with more advanced technologies. (The Matlab polyphase matching network system calculation code is shown in Appendix. B.3)

The comparison result in Fig. 6-6 shows that a 3-phase system has the best overall performance and density over different conversion ratios with the TSMC MiM capacitor technology. This topology appears best because it yields more favorable values of the passive components in the matching network and also minimizes the output capacitance due to the constant power delivery of the 3-phase system. The 3-phase matching network promises nearly 84% efficiency with a 6-to-1 conversion ratio and achieves close to 1 W/mm^2 power density including the transformation and rectification stage and output decoupling capacitor. In addition, a 3-phase system cancels the

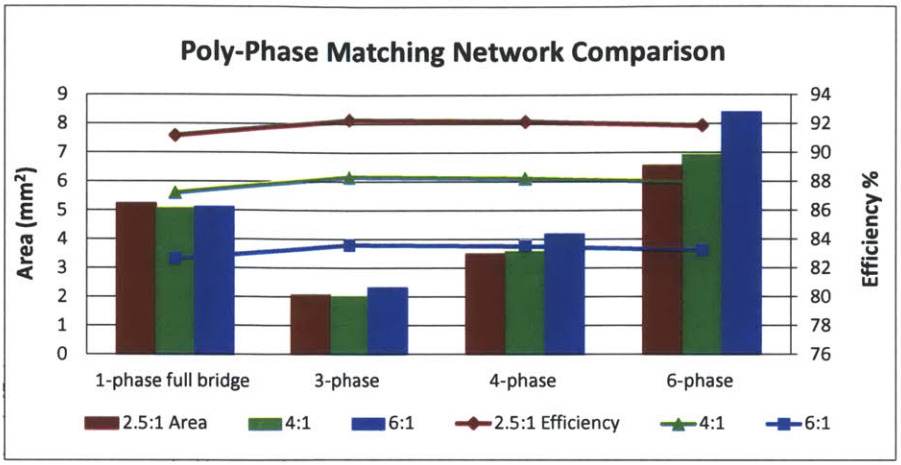


Figure 6-6: Comparison of 2-W polyphase systems. The conversion ratio is the line-to-neutral voltage of the ac input to the dc output voltage. The efficiency shown is for the matching network only. The optimized rectifier performance based on IBM 65nm is about 94% in all cases. The rectifier area is about 0.1 mm^2, which is negligible compared to the rest of the system.

third harmonic in the line-to-line voltages, which is better for the output filter design in the inverter. These results illustrate the value of polyphase transmission for VHF ac power delivery, and the potential for very high power density voltage conversion on die.

6.4 Discrete-Component Prototypes

In order to validate the feasibility of delivering polyphase ac power at VHF frequencies and rectifying it to provide a low-voltage dc output, a discrete experimental prototype was developed. It should be noted that proposed converter architecture is targeted for low-voltage integrated processes. The initial prototype introduced here is implemented with discrete components purely to validate the concept and provide insights for future designs based on integrated processes. It does not pursue the performance and power density expected in an integrated system. In addition, air core inductors are used instead of high-power-density integrated inductors (such as proposed in [10]) for this initial validation. The picture of the polyphase ac power delivery prototype board is shown in Fig. 6-7. For comparison purposes, two kinds

of systems are implemented: a 3-phase system with separate single-phase matching networks and individual full bridge rectifiers, and a 3-phase system with Δ connected capacitor matching network and 3-phase bridge rectifier.

For the initial testing, the VHF ac power is supplied by a power amplifier instead of custom-built VHF inverters. 3-phase power is generated from this single-phase source by power-dividing its output equally into 3 coaxial cables, each different in length from an adjacent cable by 120 electrical degrees (a third of a wavelength); floating outputs are then generated with a set of RF transformers. 1:8 Coilcraft WBC8-1L RF transformers are used for power amplifier impedance matching and forming the 3-phase delta/full-bridge ac source. The system operates at 50 MHz with the input line-to-neutral ac voltage of 6 V and the DC output voltage of 2 V. Output power is about 0.5 W, which is limited by the discrete RF transformers. Infineon BAT60A diodes are used for the rectifiers, as CMOS rectifiers having appropriate characteristics were not available.

Forming a symmetric PCB layout is very important for the the 3-phase Δ system since 3-phase matching network can interact with each phase. The first PCB prototype failed due to the mismatch overlap capacitances on each trace; this is hard to correct by changing the capacitance on the matching network if the parasitic asymmetry is significant. (The detailed PCB schematics and layouts are shown in Appendix. A.4)

Fig. 6-8 shows the schematic of a 3-phase system with separate single-phase matching networks and individual full bridge rectifiers. 39 pF ATC capacitors and 135 nH Coilcraft Maxi Spring air core inductors were used to form each of the separate single-phase $3\pi/2$:1 matching networks. The rectifier provides a fundamental ac-to-dc conversion of $2/\pi$:1, and hence the overall voltage conversion ratio in the ac system is 3:1. Since this is a full bridge system, the line-to-line voltage is 12 V, which is twice the line-to-neutral voltage.

Fig. 6-9 shows the schematic of the 3-phase delta-source system. 68 pF ATC

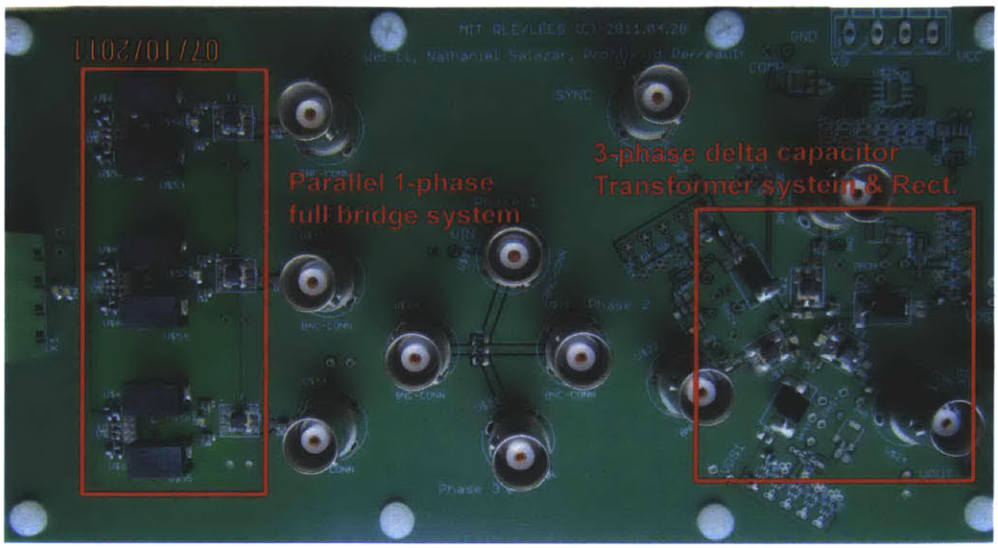


Figure 6-7: Picture of the polyphase ac power delivery PCB prototype test board.

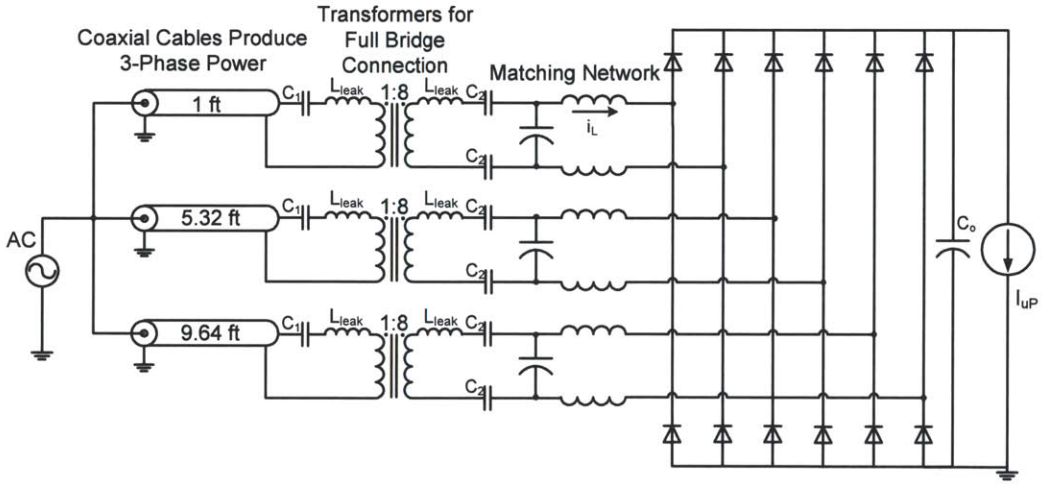


Figure 6-8: Schematic of the prototype 3-phase system with separate single-phase matching networks and individual full bridge rectifiers. C_1 and C_2 are 680 pF and 68 pF respectively. They are used for transformer leakage inductance cancellation. 39 pF ATC capacitors and 135 nH Coilcraft Maxi Spring air core inductors were used to form the matching networks. 1:8 Coilcraft WBC8-1L RF transformers are used for isolation. RG-58/U 50 Ω coaxial cables are used to split the VHF ac power into 3 phases. Information about the individual components is summarized in Table A.5.

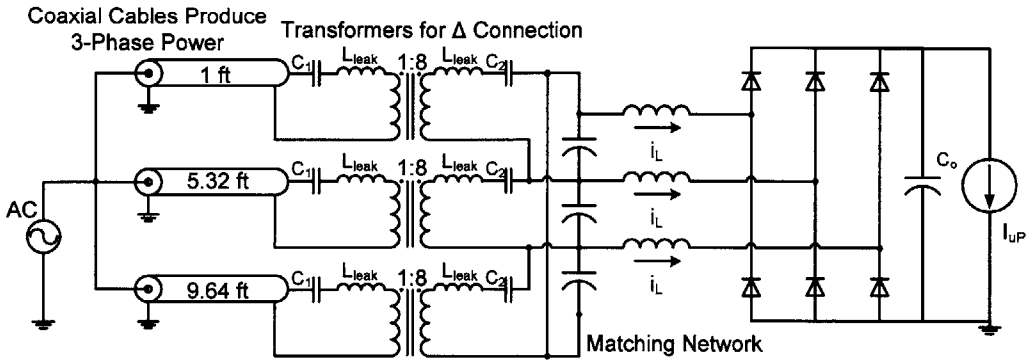


Figure 6-9: Schematic of the prototype 3-phase delta-source ac power delivery system. C_1 and C_2 are 680 pF and 68 pF respectively. They are used for transformer leakage inductance cancellation. 68 pF ATC capacitors and 47 nH Coilcraft Midi Spring air core inductors were used to form the 3-phase delta-connected capacitor matching network. 1:8 Coilcraft WBC8-1L RF transformers are used for isolation. RG-58/U 50 Ω coaxial cables are used to split the VHF ac power into 3 phases. Information about the individual components is summarized in Table A.5.

capacitors and 47 nH Coilcraft Midi Spring air core inductors were used to form the 3-phase delta connected capacitor matching network with a $3\pi/2$:1 voltage conversion ratio. Again the rectifier provides a fundamental ac-to-dc conversion of $2/\pi$:1. Thus the ac line-to-neutral to dc output voltage conversion ratio in the system is 3:1. Since the Δ to Y connection provides voltage conversion of $\sqrt{3}$:1, the line-to-line voltage in this system is $6\times\sqrt{3} \approx 10.4$ V.

The measured line-to-neutral voltages of the two systems are shown in Fig. 6-10. Both systems show 3-phase 6 V line-to-neutral voltages and 2 V dc output voltage. In addition, Fig. 6-11 shows the line-to-line voltages of both systems. The parallel single-phase system shows 12 V line-to-line input voltages, and the system with the 3-phase matching network having delta-connected capacitors shows around 10.5 V line-to-line ac voltages in the input. The full bridge rectifiers in the parallel single-phase system show the +/- V_o swing in the input of the rectifier, and the Y-connected 3-phase rectifiers in the 3-phase matching network system show only ground to V_o swing.

The measured overall system efficiency is about 70% for the 3-phase system with separate single-phase matching networks and 65% for the 3-phase delta sys-

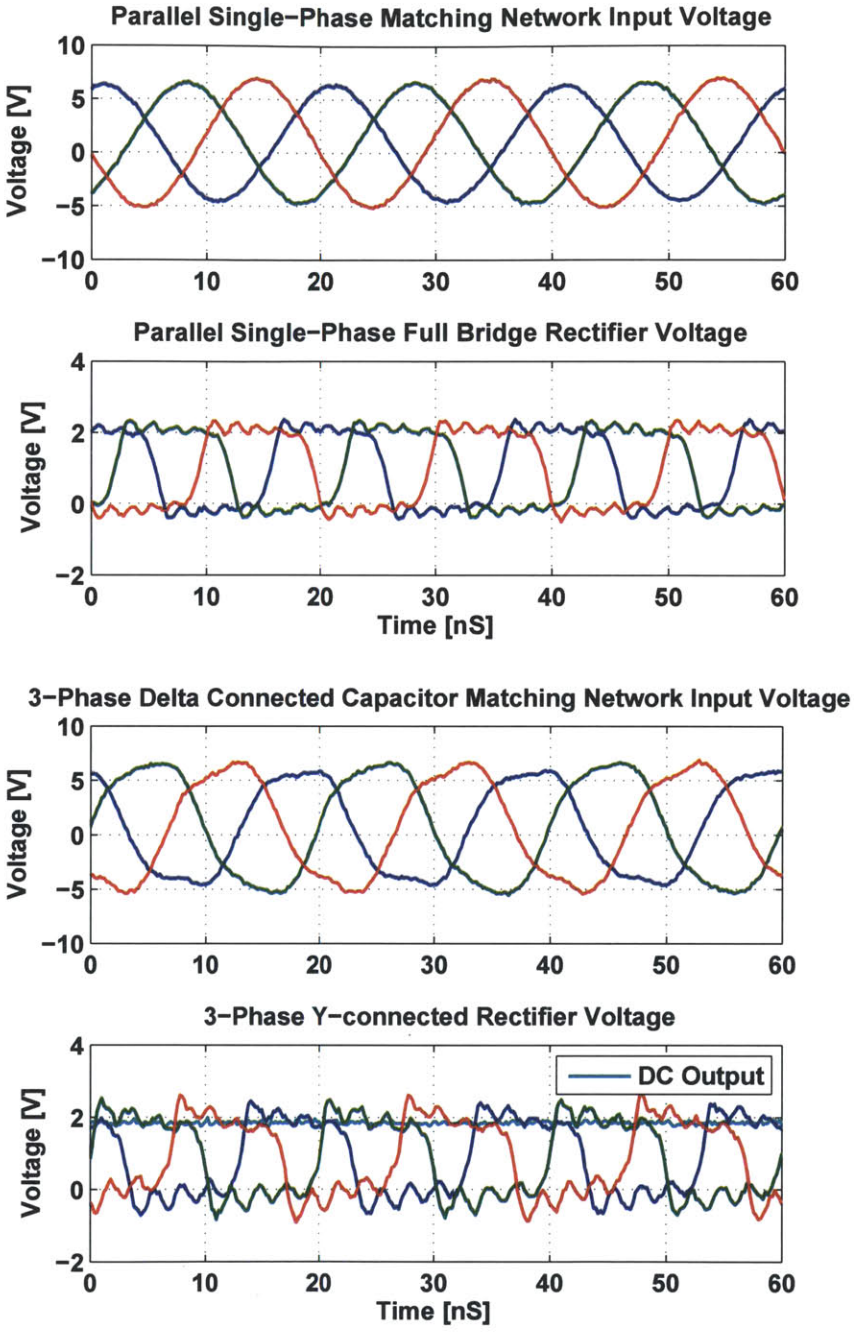


Figure 6-10: Experimental results for the 3-phase 50 MHz power delivery systems. Both the system with parallel single-phase matching networks and the system with a 3-phase matching network having delta-connected capacitors shows 6 V line-to-neutral input ac voltages and 2 V dc output voltage.

tem, which matches the calculated performance. (Estimated transformer efficiency is 98%, matching network efficiency is 92% for the single phase and 91% for the delta network, and the rectifier efficiency is approximately 80% for the full bridge and 75% for the 3-phase bridge). The largest loss in the discrete prototype is due to the rectifier diode drops, which is not surprising given the low system output voltage. In the targeted applications, with fast low-voltage integrated CMOS transistors, synchronous rectification can provide much better performance for this converter architecture.

6.5 50 MHz Prototype With Custom CMOS Rectifier

Based on the discrete-component prototype, which successfully validated the ac power delivery concept, another prototype with a customized IC was built to demonstrate the VHF CMOS synchronous rectification and improve the output power level and voltage conversion ratio. The integrated rectifier was designed and built in a TSMC 0.25 μm CMOS process. The rectifier IC can be configured as a 3-phase rectifier or into three separate full-bridge rectifiers. Each rectifier phase is optimized to output 2 W of power, so the whole system has total 6 W of output power. The output voltage is 2.5 V and the switching frequency is 50 MHz. The rectifiers are controlled in a class DE fashion to minimize the switching loss at VHF and achieve better efficiency. The detail of the rectifier IC design was shown in chapter 4. As with the discrete-component prototype, two kinds of systems were built: a 3-phase system with separate single-phase matching networks and individual full bridge rectifiers, and a 3-phase system with Δ connected capacitor matching network and 3-phase bridge rectifier. Both systems have the same $4\sqrt{2}$:1 voltage conversion ratio, 14 V line-to-neutral ac input voltage (the input voltage is chosen to match the 50 Ω impedance of the coaxial cable with 2 W of output power.) and 2.5 V dc voltage. The ac power is supplied by the RF power amplifier (10W1000, Amplifier Research), with the input

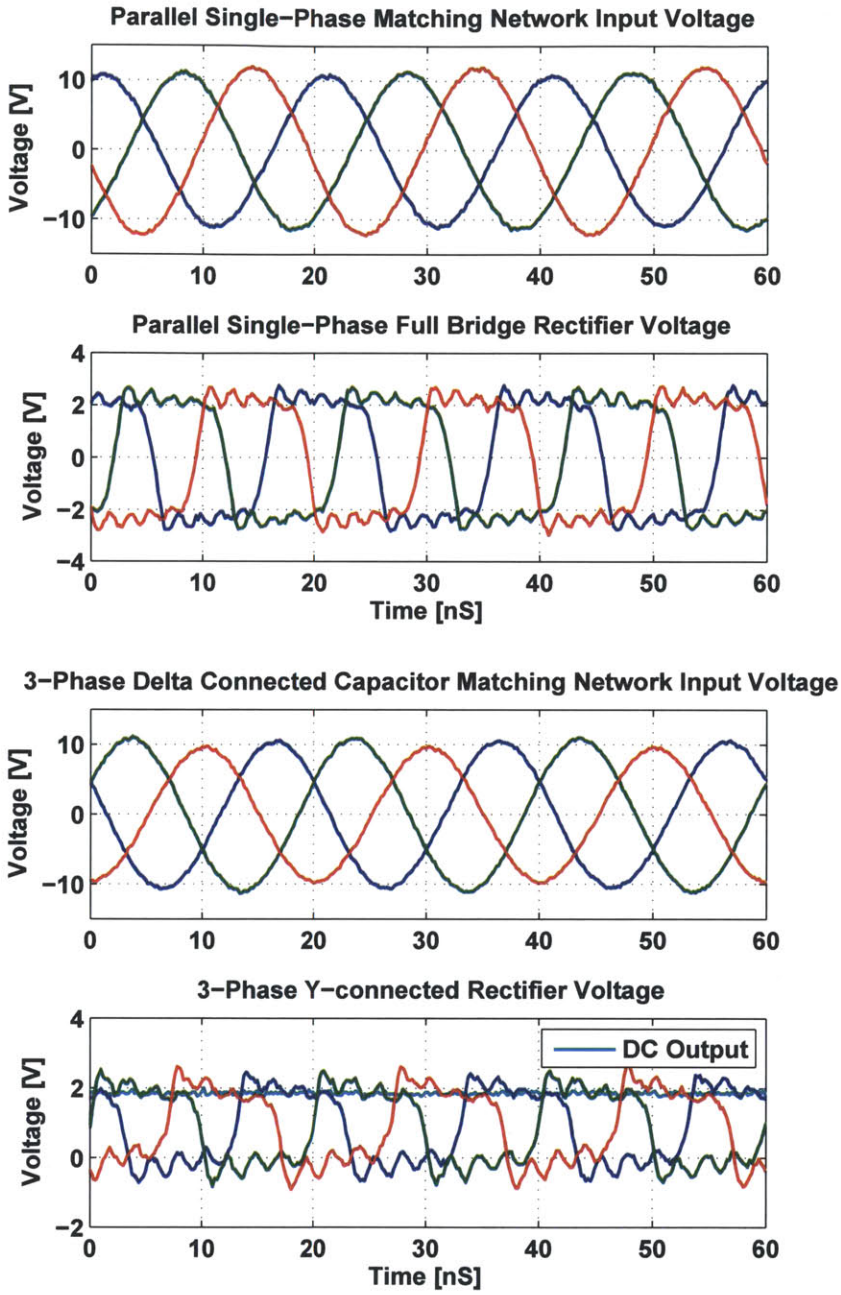


Figure 6-11: Additional experimental results for the 3-phase 50 MHz power delivery systems. Top is the measured waveforms of the 3-phase system with separate single-phase matching networks and separate single-phase full bridge rectifiers. It has line-to-line ac voltages of 12 V. The next plot shows the +/- 2 V rectifier switching waveforms, with peak amplitude equal to the output voltage. The bottom plot of the half-bridge rectifier input waveforms is the result for the system with the 3-phase matching network with having delta-connected capacitors. It has a line-to-line voltage of 10.5 V and shows the rectifier inputs switching between 0 V and the output voltage.

ac power is measured by a directional RF power meter (5010B, Bird Electronics Corp.). 3-phase power is generated from this single-phase source by power-dividing this source equally into 3 coaxial cables, each different in length from an adjacent cable by a third of a wavelength. (The detail PCB schematics and layouts are shown in Appendix A.5)

The schematic of the 3-phase system with separate single-phase matching networks and individual full bridge rectifiers is shown in Fig. 6-12. 100 PF and 68 nH Coilcraft Midi Spring air core inductors were used to form a matching network to match the 50 Ω output impedance of the power amplifier to the 3-phase coaxial cables. Isolation and single-to-double-ended operation is provided by a 1:1 hand-wound transformer with a BLN1728-8A/94 core. There are 7 turns of each winding (30 AWG wire, bifilar wound) on the transformer providing a magnetizing inductance L_m of 1.2 uH and leakage inductance L_l of 30 nH. A 330 pF capacitor is connected in series of the primary side of the transformer for leakage inductance cancellation. 240 pF ATC capacitors and two 18.5 nH Coilcraft Mini Spring air core inductors were used to form a matching network with a $\sqrt{2}\pi$:1 voltage conversion ratio to match the input impedance of the full-bridge rectifier to the 50 Ω coaxial cable. The full-bridge rectifier provides a fundamental ac-to-dc conversion of $4/\pi$:1. Thus the whole system provides a $4\sqrt{2}$:1 voltage conversion ratio from the ac input voltage to the dc output voltage.

Fig. 6-12 shows the picture of the prototype board and Fig. 6-14 shows the experimental result. The measurement shows 50 MHz 3-phase ac input voltages with 14.1 V amplitudes. In the input of the full-bridge rectifier, $-V_o$ to $+V_o$ ($\pm$2.5 V) voltage swing is observed. The overall efficiency of the 3 individual full-bridge rectifier system is 76 % with matching network efficiency of 88 % (inductor Q is 88) and rectifier efficiency of 87 %.

The schematic of the 3-phase matching networks with delta connected capacitor system is shown in Fig.6-15. 100 PF and 68 nH Coilcraft Midi Spring air core inductor were used to form a matching network to match the 50 Ω output impedance of the

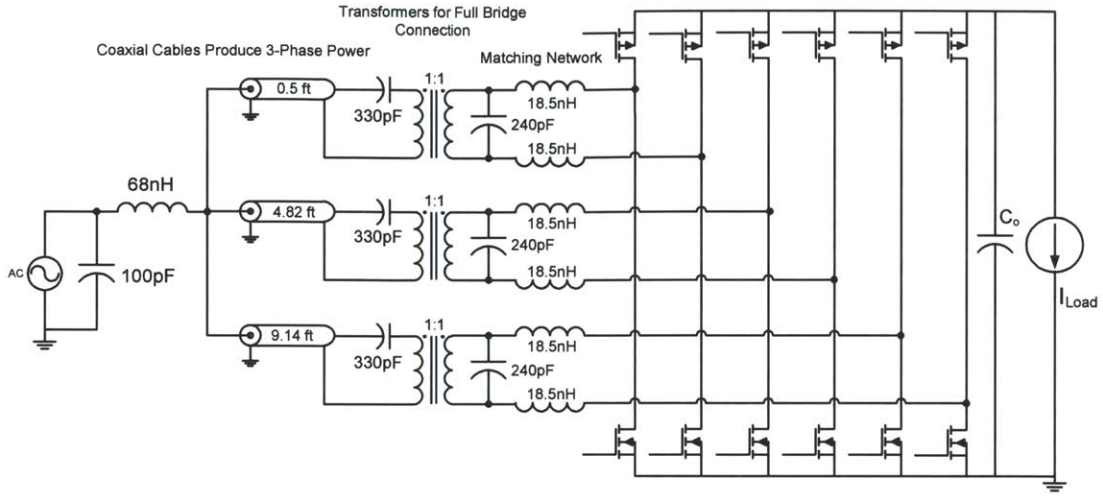


Figure 6-12: Schematic of the 3-phase system with separate single-phase matching networks and individual full bridge rectifiers IC prototype. Information about the individual components and the system are summarized in Table A.6.

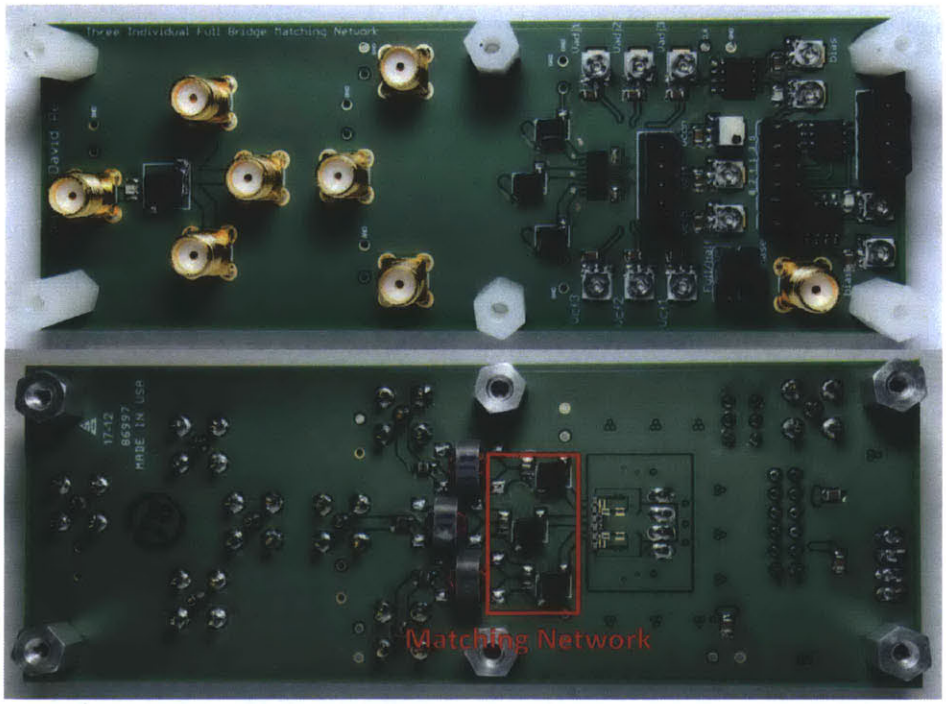


Figure 6-13: Pictures of the 3-phase system with separate single-phase matching networks and individual full bridge rectifiers IC prototype board. Transformers and part of the matching networks are shown in the bottom of the board.

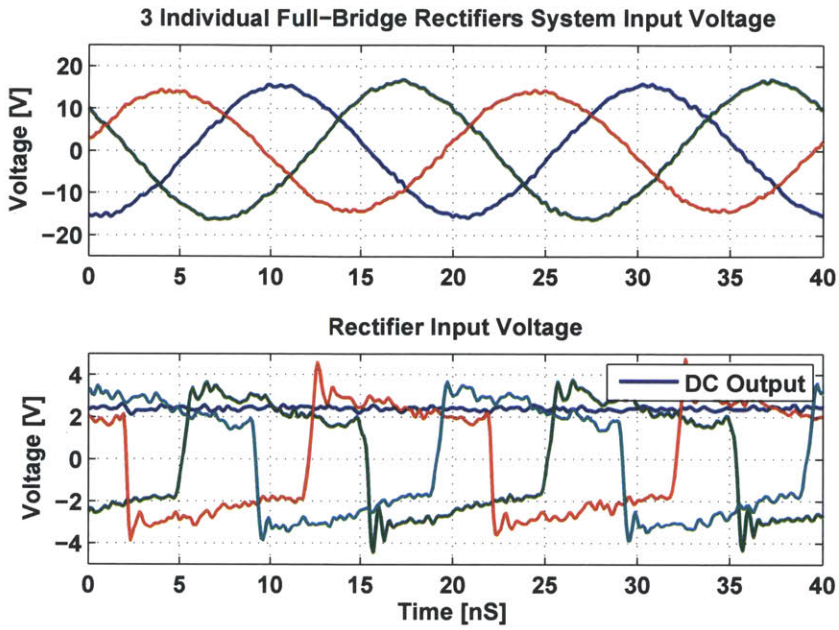


Figure 6-14: Measured waveforms of the 3-phase system with separate single-phase matching networks and individual full bridge rectifiers IC prototype. -V_o to +V_o ($\pm$2.5 V) voltage swing is shown in the input of the full-bridge rectifier.

power amplifier to the 3-phase coaxial cables. 150 pF ATC capacitors and 18.5 nH Coilcraft Mini Spring air core inductors were used to form the 3-phase delta matching network with a $2\sqrt{2}\pi$:1 voltage conversion ratio to match the input impedance of the 3-phase bridge rectifier to the 50 Ω coaxial cable. The 3-phase bridge rectifier provides a fundamental ac-to-dc conversion of $2/\pi$:1. Thus the whole system provides a $4\sqrt{2}$:1 voltage conversion ratio from the ac input voltage to the dc output voltage. Since the Δ to Y connection provides voltage conversion of $\sqrt{3}$:1, the line-to-line voltage in this system is $\sqrt{3}$ times of the 14 V line-to-neutral voltage, which is about 24 V.

Fig. 6-15 shows the picture of the prototype board and Fig. 6-17 shows the experimental result. Same as the 3-phase system with separate single-phase matching networks and individual full bridge rectifiers, the measurement shows 50 MHz 3-phase ac input voltages with 14.1 V amplitudes. However, in the input of the 3-phase bridge rectifier, only 0 to +V_o (2.5 V) voltage swing is observed. In order to maintain the same system voltage conversion ratio, the matching network voltage transformation

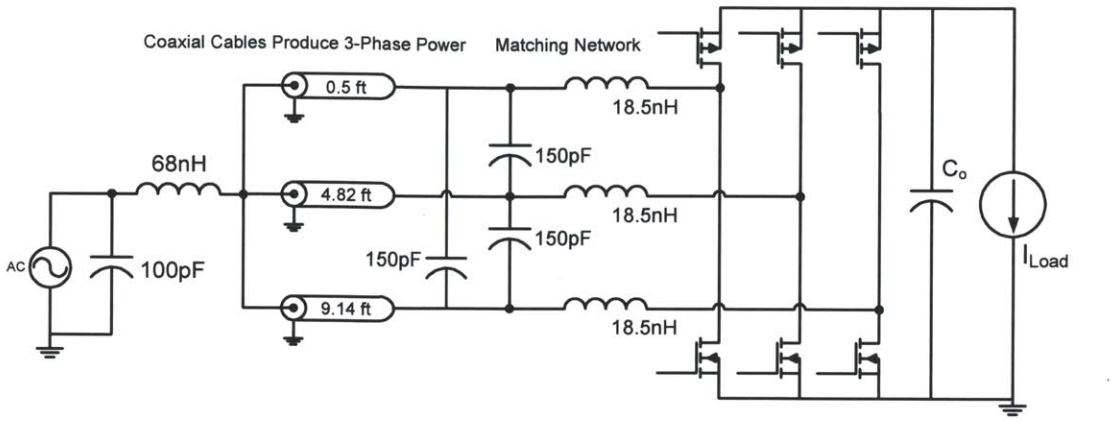


Figure 6-15: Schematic of the 3-phase matching networks with delta connected capacitor system IC prototype. Information about the individual components and the system are summarized in Table A.7.

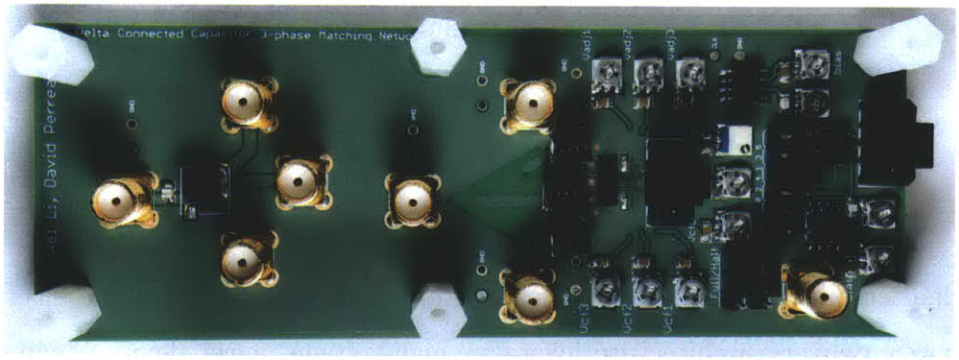


Figure 6-16: Pictures of the 3-phase matching networks with delta connected capacitor system IC prototype board.

ratio in the delta system is two times higher compared to the matching network voltage transformation ratio in the 3 individual full-bridge system. As a result, the matching network efficiency in the delta system is relatively lower, which is 80 % with inductor Q of 70. The overall efficiency of the delta system is 70 % rectifier efficiency of 87 %. The circulating power in the delta matching network also contribute higher conduction loss in the system. However, the delta matching network requires smaller capacitance in the matching network but with higher voltage rating requirement on the capacitors. These are the design trade-offs needed to be considered.

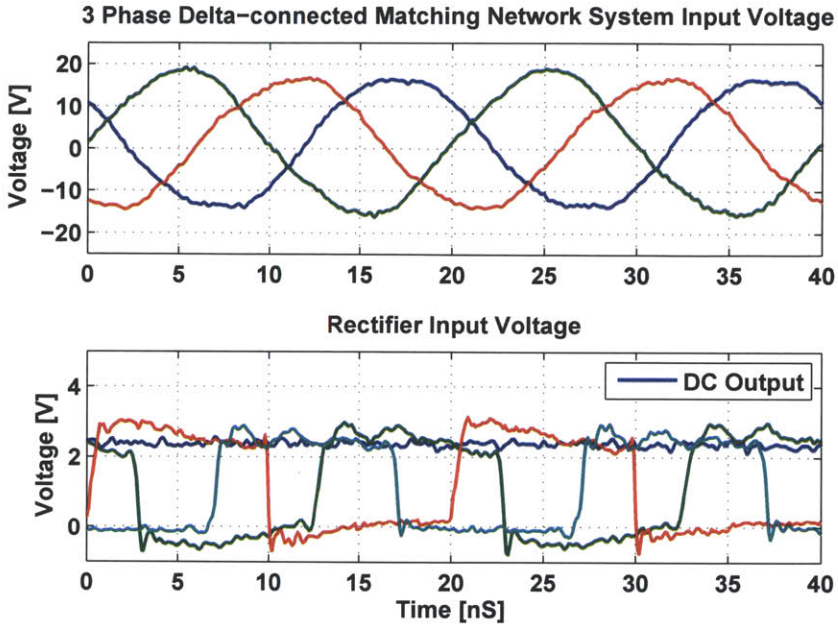


Figure 6-17: Measured waveforms of 3-phase matching networks with delta connected capacitor system IC prototype.

6.6 Conclusion

This chapter presents an ac power delivery architecture for low-voltage electronics. This power delivery architecture leverages high-voltage power devices (which may be off die) and low-voltage integrated Si CMOS devices. It takes advantage of a transformation stage using integrated inductors to provide integrated power delivery. Analysis reveals that such a system is feasible, and that polyphase RF power delivery is advantageous. A discrete prototype operating at 50 MHz has been designed and built to demonstrate and verify the concept. With the ac power transformation stage and rectifier stage on die, this architecture promises to help reduce pin count and interconnect loss for microprocessors.

Chapter 7

Conclusion and Future Work

7.1 Thesis Contributions

This thesis explores architectures, topologies and design techniques for high-density high-conversion-ratio low-voltage-output power converters. There are four major contributions of this thesis. The first is design, analysis and implementation of a new frequency multiplier inverter suitable for efficient operation at very high frequencies (VHF) for step-down conversion. This new inverter has an output frequency of twice the individual device switching frequency and provides a 3:2 step-down voltage conversion ratio. The lower switching frequency in the inverter provides lower switching loss and extends the lower output power limit due to the device output capacitance. The step-down conversion ratio in the inverter can reduce the burden for the transformation stage in the converter and improve the performance for high step-down ratio converters. Both the experimental and simulation result from the 50 MHz prototype implemented with GaN-on-Si transistors demonstrates the high performance and wider output power range of this frequency multiplier compared to conventional resonant inverter topologies.

The second main contribution of this thesis is the design and implementation of the new CMOS switched-capacitor rectifier. The SC rectifier only requires low-

voltage devices and the flying devices can be self-driven, greatly simplifying gate drive considerations for VHF operation. The multi-step structure of this SC rectifier is well-suited to implementation in low-voltage CMOS, and can provide multiple times higher voltage step-down ratios compared to conventional bridge rectifiers. High step-down ratio power converters can benefit from the high step-down voltage conversion ratio of the SC rectifier and achieve better performance. A 50 MHz full-bridge SC rectifier IC implemented in a TSMC 0.25 μm process is presented that validates the concept and demonstrates the feasibility of VHF CMOS synchronous rectification.

The third contrition of this thesis is the development of a hybrid GaN-Si step-down dc-dc converter architecture capable of operating at VHF frequencies. The hybrid GaN-Si dc-dc converter consists of a VHF GaN frequency multiplier inverter stage, a transformation stage and a switched-capacitor rectifier stage. With transformation stage - implemented with a matching network, the low-voltage rectifier stage can be separated from the high input voltage such that the high-voltage inverter stage does not need to carry the high output current and the low-voltage rectifier stage does not need to see the high inverter voltage. In addition, the matching network also provide a high power density, high performance and integratable solution for voltage transformation in the converter. The proposed dc-dc converter architecture is suitable for low-voltage portable electronics and applications where high power density and high voltage conversion ratio are desired. The 50 MHz 4 W output power converter prototype with 8:1 voltage conversion ratio validates the converter concept.

The last contribution of the thesis is an investigation of a very high frequency ac power delivery architecture for microprocessors and other low-voltage digital ICs. With remote inverters, high-voltage low-current ac power can be delivered across the interconnect into the silicon die. And integrated matching network and CMOS low-voltage rectifier converts the high-voltage ac into low-voltage dc for application use. With the proposed ac power delivery architecture, one can reduce the interconnect loss and pin-count burden that limits many modern digital devices. In addition,

multi-phase VHF ac systems are also explored and developed to provide higher power density and better performance for the system. A 50 MHz 3-phase ac power delivery prototype is implemented that demonstrates the feasibility of VHF ac voltage transformation and synchronous rectification.

7.2 Thesis Summary

The thesis is divided into 7 chapters, including this concluding chapter. Chapter 1 presents background and motivations of this research, and provides a brief description of the advantages of the proposed power converter architecture approaches. Chapter 2 overviews some possible architectures for very-high-frequency (VHF) high voltage conversion ratio power converters, including their design trade-offs and limitations.

Chapter 3 overviews some inverter architectures and proposes the frequency multiplier inverter for step-down power converters. The design limitations of the classic resonant inverters are discussed. The detailed design analysis and advantages of the frequency multiplier are also described. This chapter also presents a 50 MHz frequency multiplier prototype with EPC discrete GaN devices. The power devices are switched at 25 MHz and the inverter output frequency is 50 MHz. The measurement shows 92.5 % efficiency for the 5 W frequency multiplier.

Chapter 4 discuss the limitations of the conventional bridge rectifier for step-down power conversion and presents a new switched-capacitor (SC) rectifier architecture. This chapter first shows the detailed analysis of the operation of a two-step switched-capacitor rectifier and then expand this analysis for the general multi-step switched-capacitor rectifier architecture, including the driving scheme for the switched-capacitor rectifier. Furthermore, the design of a two-stage SC rectifier integrated circuit prototype built in a TSMC 0.25 μm CMOS process is shown. This chapter concludes with the experimental results of the IC prototype operating at 50 MHz.

Chapter 5 demonstrates a complete hybrid GaN-Si dc-dc converter. Three different types of prototype designs are presented: a GaN-Si dc-dc converter with half-bridge switched-capacitor rectifier, a GaN-Si dc-dc converter with isolated full-bridge switched-capacitor rectifier and a GaN-Si dc-dc converter with isolated conventional full-bridge rectifier. All systems are operated at 50 MHz with 5 W of output power. Detailed analyses and design trade-off among different systems are discussed, and measurement results are shown to verify the concept.

Chapter 6 introduces the ac power delivery architecture. With ac power delivery from remote inverters, high voltage and low current can be delivered across the interconnect into microprocessors (or other digital ICs) to save pin count and interconnect loss. This chapter also explores the multi-phase ac power systems operating at VHF. The design trade-offs for multi-phase matching networks for voltage transformation are also investigated and developed. Based on this investigation, we first show a 50 MHz discrete prototype to validate the high-frequency matching network and rectification. Next, we describe the design of a polyphase ac power delivery system incorporating an integrated circuit (IC) synchronous rectifier implemented in a TSMC 0.25 μm CMOS process. The chapter concludes with IC measurement results and the demonstration of the VHF ac power delivery architecture.

7.3 Future Work

Although the prototypes have shown solid results, there are still several ways to improve the proposed converter architecture. The CMOS synchronous rectification implemented in this thesis is controlled by voltage controlled delay lines. These delay lines are fine tuned externally to achieve the optimal delay for the rectifiers. Real-time automatic delay control is very valuable to the converter. There are many lossless current sensing techniques available [71, 72]. In order to synchronize with the inductor current, one possibility is to track the voltage across the inductor. The phase of the

inductor current lags that of the voltage by $\pi/2$ with high Q inductors. And voltage measurement can be much more efficient compared to current sensing.

The second is to develop a control technique for the proposed converter. In our prototypes, regulation of the converter was not implemented, and this is necessary for commercial applications. As mentioned in chapter 5, on-off control can be used to regulate the converter. However, it sacrifices the high bandwidth in the converter and larger output decoupling capacitance is required. If a better current sensing technique can be developed for the converter, it adds more freedom to the control scheme. PWM control may become possible to regulate the rectifier stage. And there are many available techniques to modulate the inverter output power at VHF (such as the outphasing technique [73, 74, 75, 76, 77]).

Another possibility to improve the converter performance is to develop a better transformation stage. The matching network transformation stage has been developed and proven to have high power density and high efficiency with high Q inductors. However, the performance of the matching network is directly proportion to the transformation ratio of the network and the performance of the inductor, Q. If the inductor Q is limited and high transformation ratio is required, the performance of the matching network is less attractive. Alternative techniques include conventional transformers, transmission-line transformers and the distributed transformer. The distributed active transformer appears to have the potential as an alternative high-performance integrated transformation stage [78, 79]. Further development of transformation techniques is worthwhile for the converter design.

Appendix A

Board Layouts and Schematics

A.1 GaN Frequency Doubler PCB

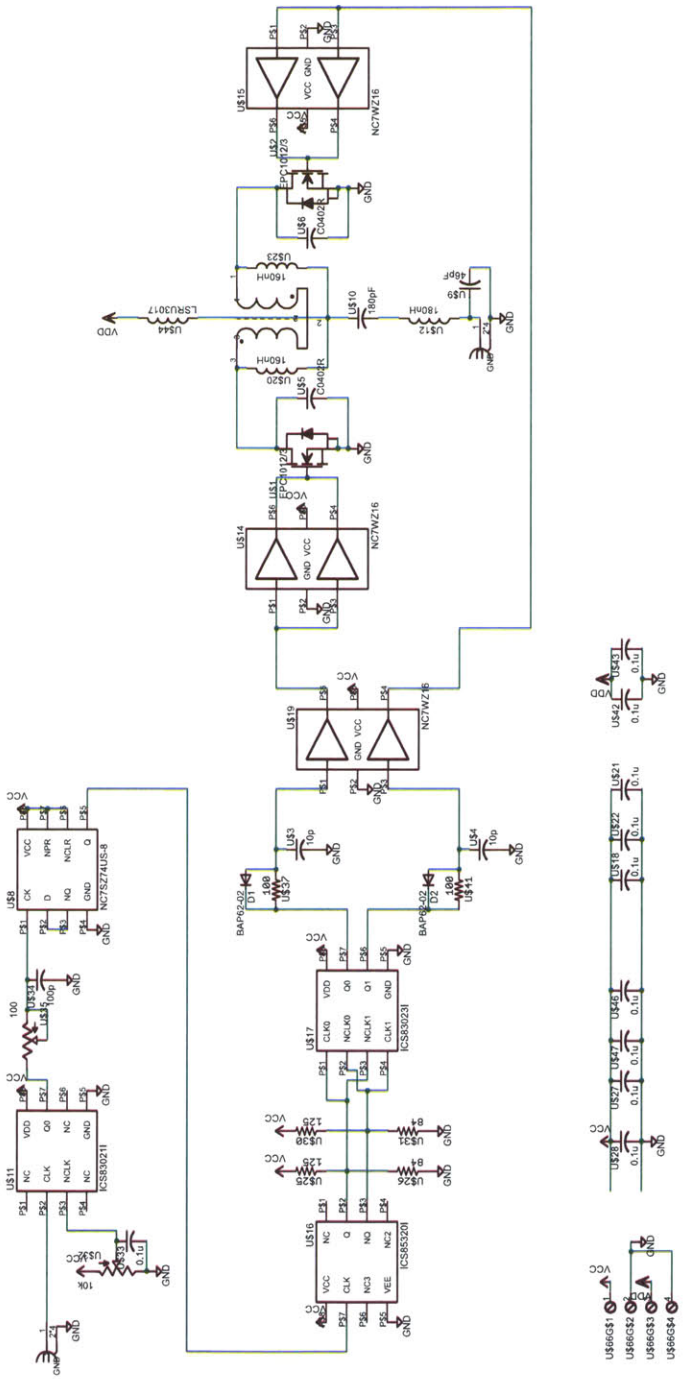


Figure A-1: The Schematic of the Frequency Multiplier PCB Prototype.

Table A.1: GaN Frequency Doubler Bill of Materials

Parts/Spec	**Value**	**Description**
Input Voltage	20 V	-
Power	5 W	-
Output Frequency	50 MHz	-
Switching Frequency	25 MHz	-
Output Voltage	13 V	-
U11	ICS83021I	Clock buffer
U8	NC7SZ74US-8	Flipflop, converts 50 MHz to 25 MHz
U16	ICS85320I	Single-ended-to-differential clock translator
U17	ICS83023I	Differential-to-single-ended clock fanout buffer
U19	NC7WZ16	Buffer for clock
U14, U15	NC7WZ16	GaN gate driver
U5, U6	EPC2012	EPC 200 V GaN power device
U44	SRU3017 2.2 uH	Choke inductor
U20	BLN1728-8A/94	3 turns AWG 28 wire, bifilar wound, L_m=92 nH and L_{leak}=25 nH
U10	180 pF	ATC 100A rf capacitor for series resonant tank
U12	130 nH	Coilcraft MAXI air core inductor, 75 nH matching network inductance and 55 nH filtering inductance
U9	90 pF	ATC 100A rf capacitor for matching network

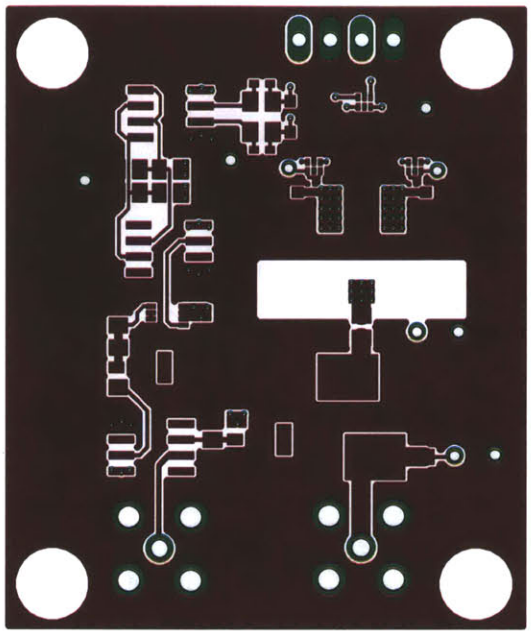


Figure A-2: The Layer 1 PCB Layout of the Frequency Multiplier Prototype.

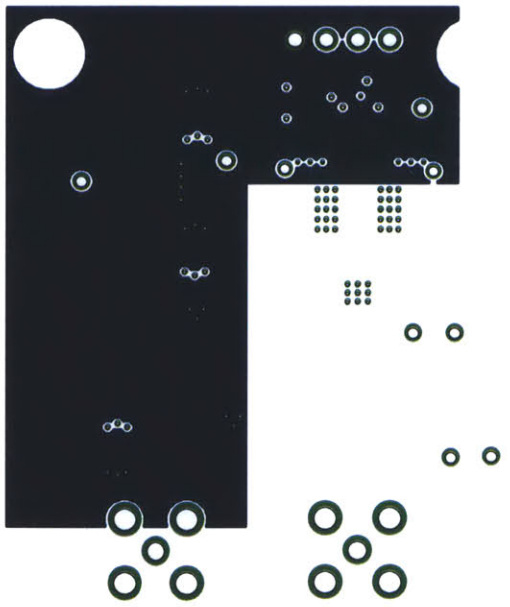


Figure A-3: The Layer 2 PCB Layout of the Frequency Multiplier Prototype.

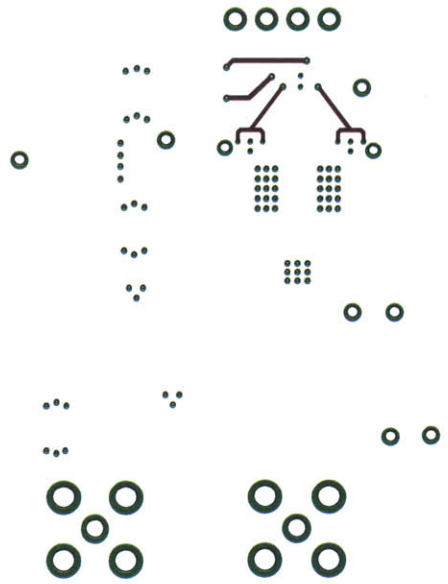


Figure A-4: The Layer 3 PCB Layout of the Frequency Multiplier Prototype.

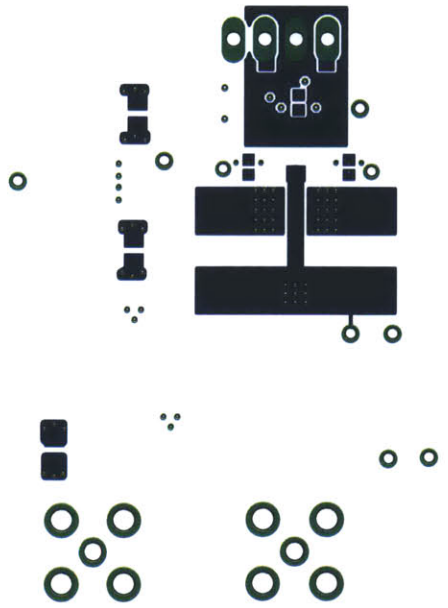


Figure A-5: The Layer 4 PCB Layout of the Frequency Multiplier Prototype.

A.2 SC Rectifier PCB

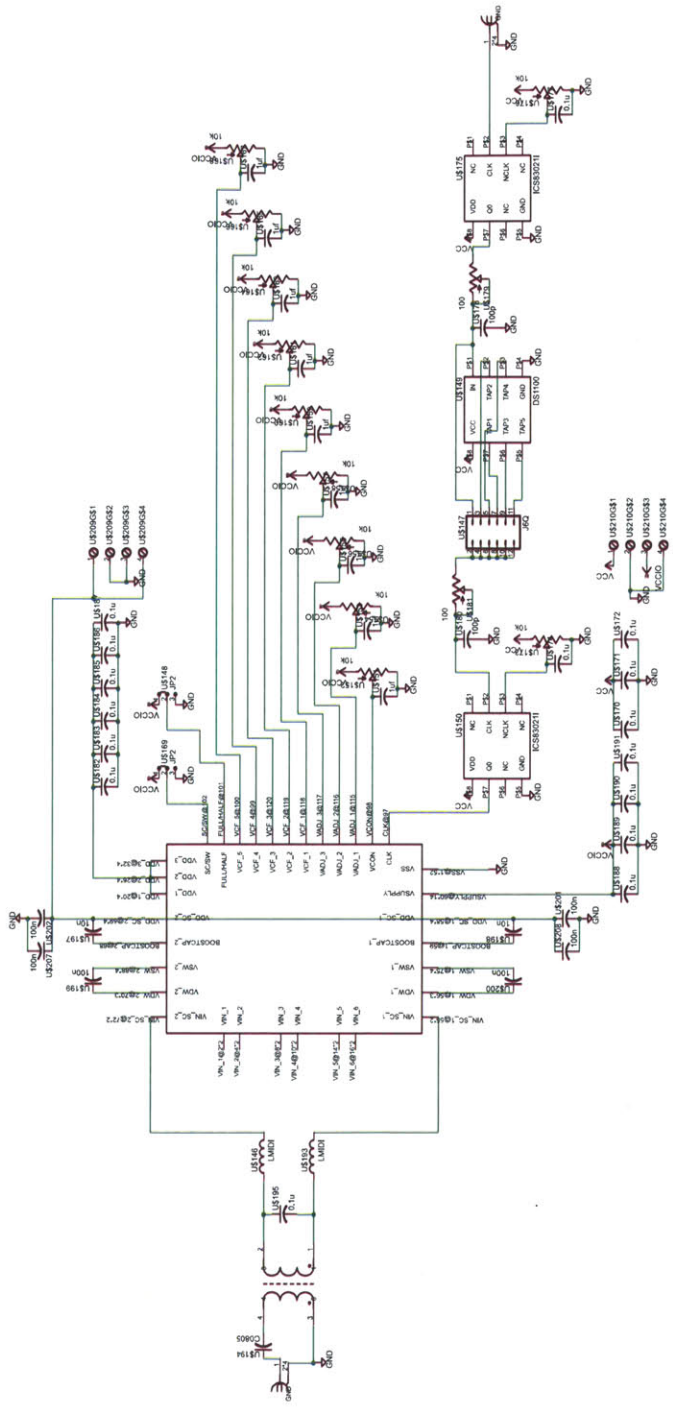


Figure A-6: The Schematic of the Frequency Multiplier PCB Prototype.

Table A.2: SC Rectifier Bill of Materials

Parts/Spec	**Value**	**Description**
Input Voltage	20 V	Ac voltage amplitude
Power	4 W	-
Operation Frequency	50 MHz	-
Output Voltage	2.5 V	-
U175, U150	ICS83021I	Clock buffer
U149	DS1100LZ-20+	5 tap 20 ns 5tap delay line, each tap is 5 ns.
U179, U181	P1E101CT	100 Ω trimmer for clk delay
U178, U180	100 pF 0805	Capacitor for clk delay
U202, U208	10 nF 01005	Capacitor for gate driver in the SC rectifier referenced to Vdd
U199, U200	0.22 μF 0204	Flying capacitor for SC rectifier
U201, U202, U207, U208	0.22 μF 0204	Output decoupling capacitor for SC rectifier
U188, U189	0.1 μF 0201	Decoupling capacitor for control circuits on chip
U190, U191	0.1 μF 0402	Decoupling capacitor for control circuits on chip
Transformer	BLN1728-8A/94	1:1 turns ratio, 7 turns AWG 30 wire, bifilar wound, L_m=1.2 μH and L_{leak}=30 nH
U194	360 pF	ATC 100A rf capacitor for leakage inductance cancellation
U146, U193	22 nH	Coilcraft MIDI air core inductor for matching network
U195	180 pF	ATC 100A rf capacitor for matching network

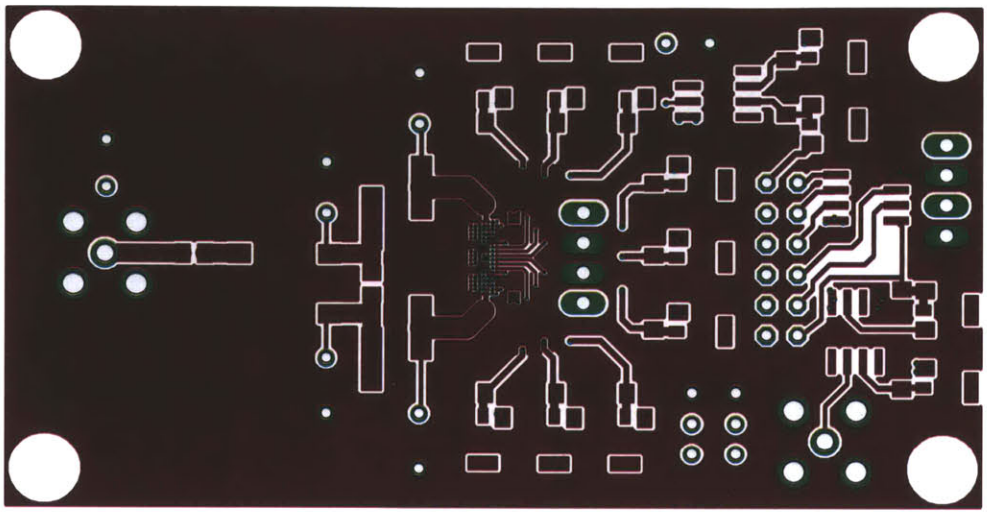


Figure A-7: The Layer 1 PCB Layout of the Switched-Capacitor Rectifier IC Prototype.

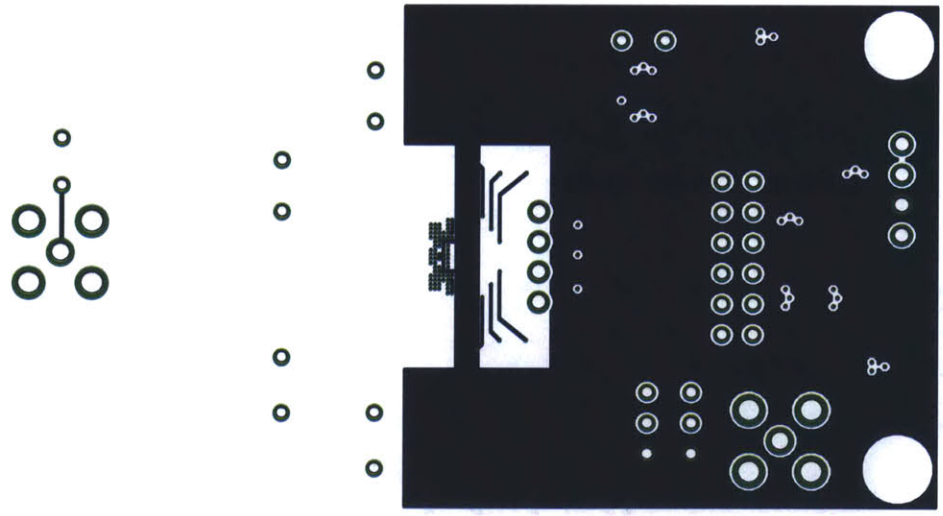


Figure A-8: The Layer 2 PCB Layout of the Switched-Capacitor Rectifier IC Prototype.

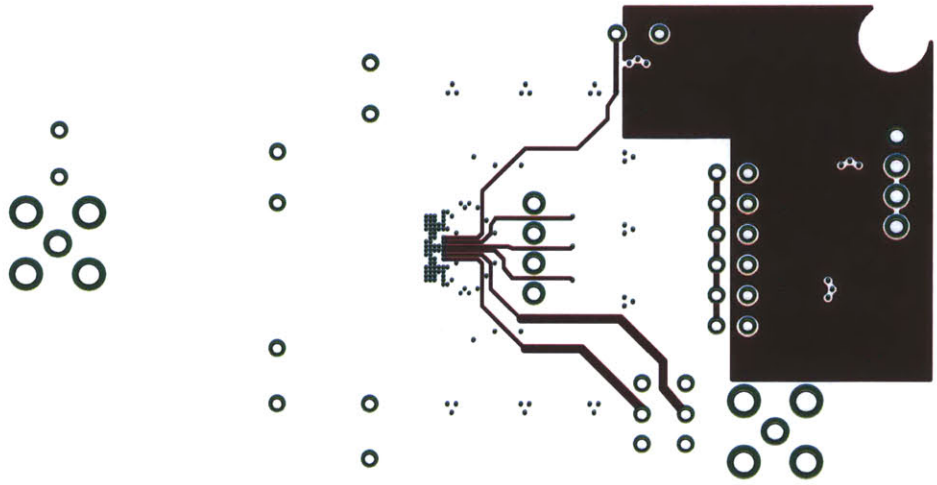


Figure A-9: The Layer 3 PCB Layout of the Switched-Capacitor Rectifier IC Prototype.

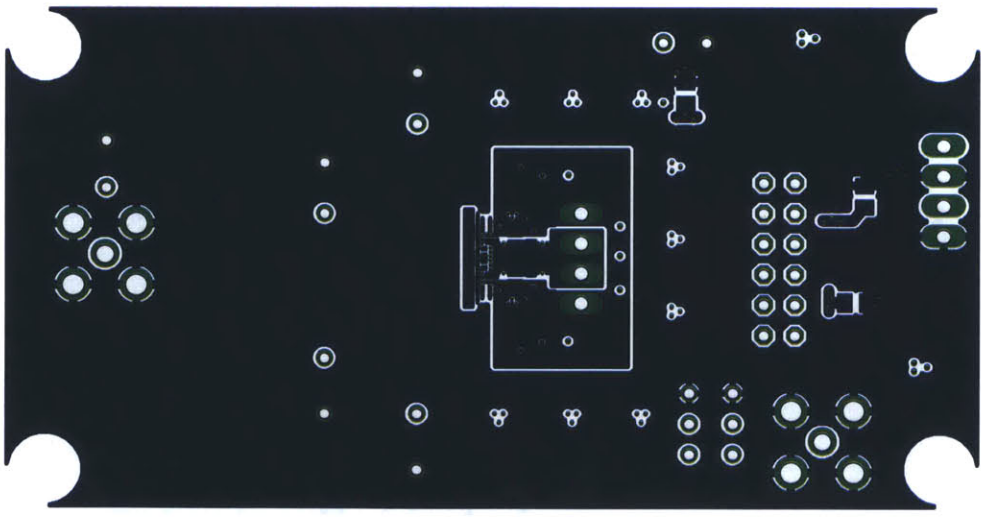


Figure A-10: The Layer 4 PCB Layout of the Switched-Capacitor Rectifier IC Prototype.

A.3 GaN-Si Dc-dc Converter PCB

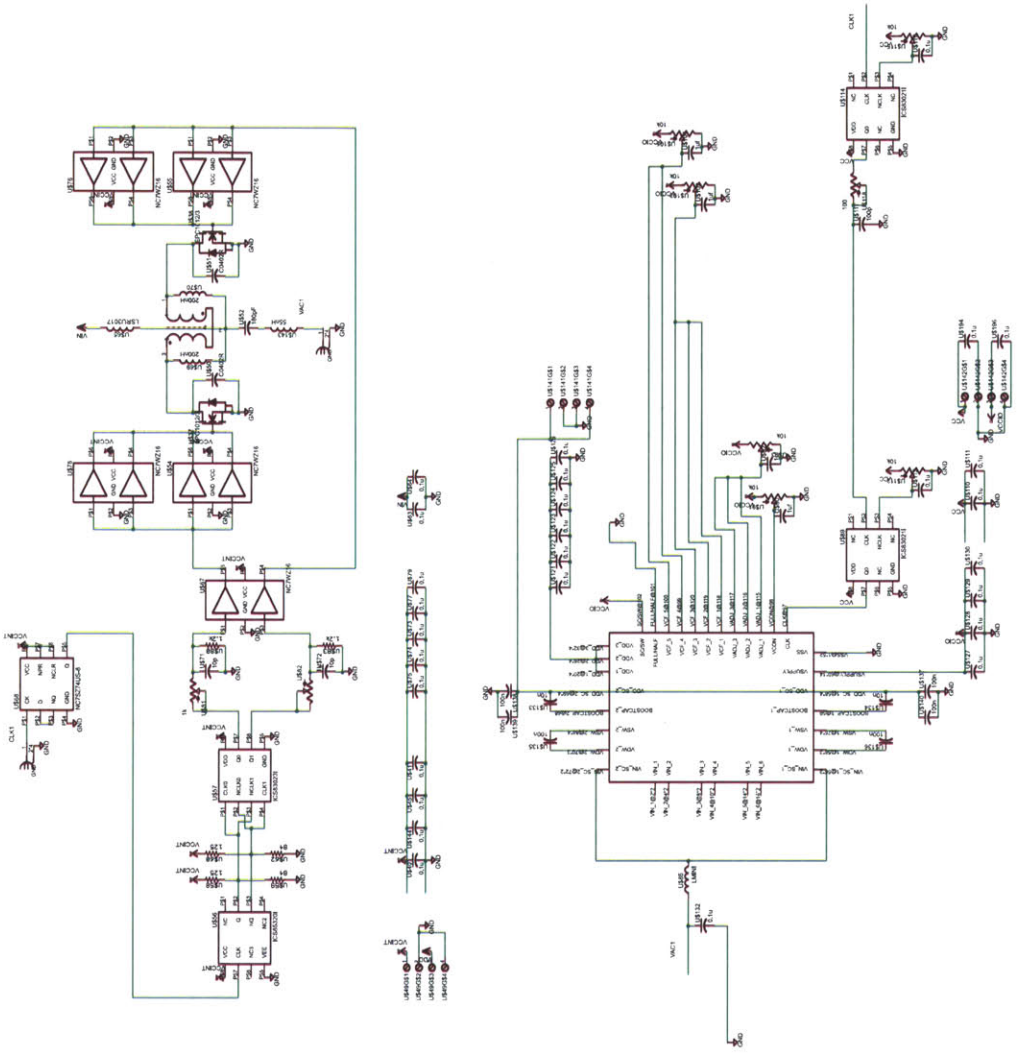


Figure A-11: The Schematic of the Non-isolated GaN-Si Dc-dc Converter PCB Prototype.

Table A.3: GaN-Si Dc-dc Converter Bill of Materials

Parts/Spec	**Value**	**Description**
Input Voltage	20 V	Dc
Power	4 W	-
Operation Frequency	50 MHz	-
Output Voltage	2.5 V	Dc
U89, U114	ICS83021I	Clock buffer
U68	NC7SZ74US-8	Flipflop, converts 50 MHz to 25 MHz
U56	ICS85320I	Single-ended-to-differential clock translator
U57	ICS83023I	Differential-to-single-ended clock fanout buffer
U54, U55, U76, U78	NC7WZ16	GaN fet driver
U37, U38	EPC2012	EPC 200 V GaN power device
U65	SRU3017 2.2 uH	Choke inductor
U69	BLN1728-8A/94	1:1 coupled indcutor, 3 turns AWG 28 wire, bifilar wound, L_m=92 nH and L_{leak}=25 nH
U52	180 pF	ATC 100A rf capacitor for series resonant tank
U143	55 nH	Coilcraft MIDI air core inductor, filtering inductance
U112, U118	P1E101CT	100 Ω trimmer for clk delay
U113, U117	100 pF 0805	Capacitor for clk delay
U133, U134	10 nF 01005	Capacitor for gate driver in the SC rectifier referenced to Vdd
U135, U136	0.22 μF 0204	Flying capacitor for SC rectifier
U137, U138, U139, U140	0.22 μF 0204	Output decoupling capacitor for SC rectifier
U127, U128	0.1 μF 0201	Decoupling capacitor for control circuits on chip
U129, U130	0.1 μF 0402	Decoupling capacitor for control circuits on chip
U85	12.5 nH	Coilcraft MINI air core inductor for matching network
U132	680 pF	ATC 100A rf capacitor for matching network

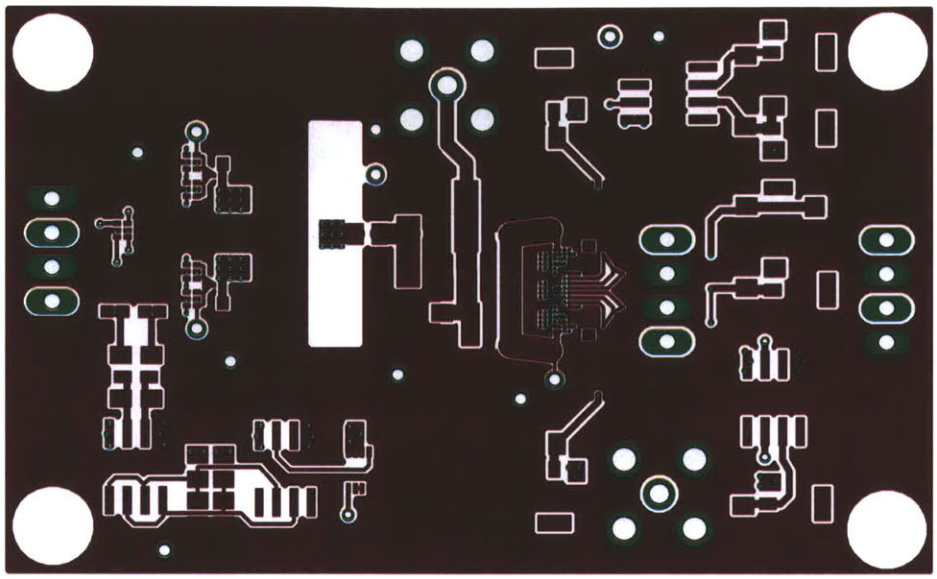


Figure A-12: The Layer 1 PCB Layout of the Non-isolated GaN-Si Dc-dc Converter Prototype.

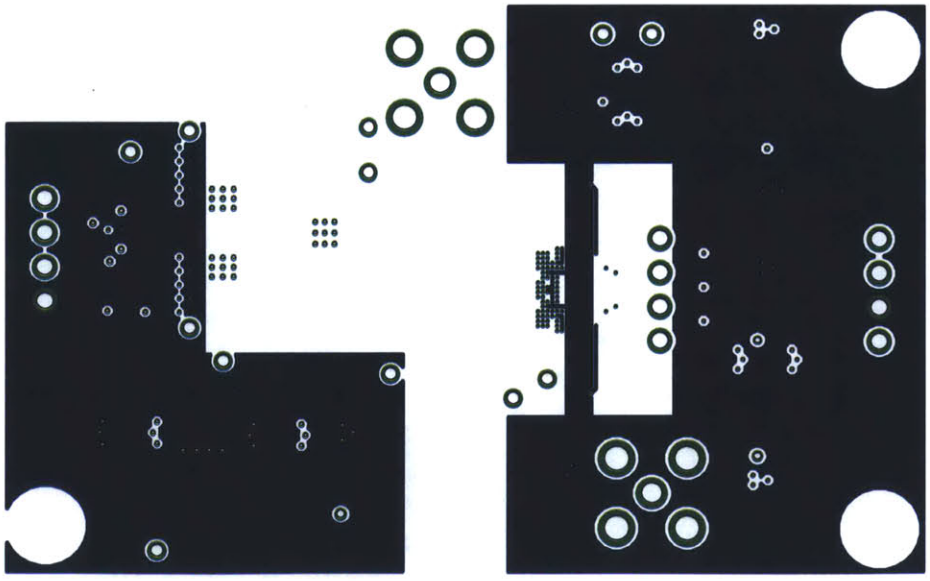


Figure A-13: The Layer 2 PCB Layout of the Non-isolated GaN-Si Dc-dc Converter Prototype.

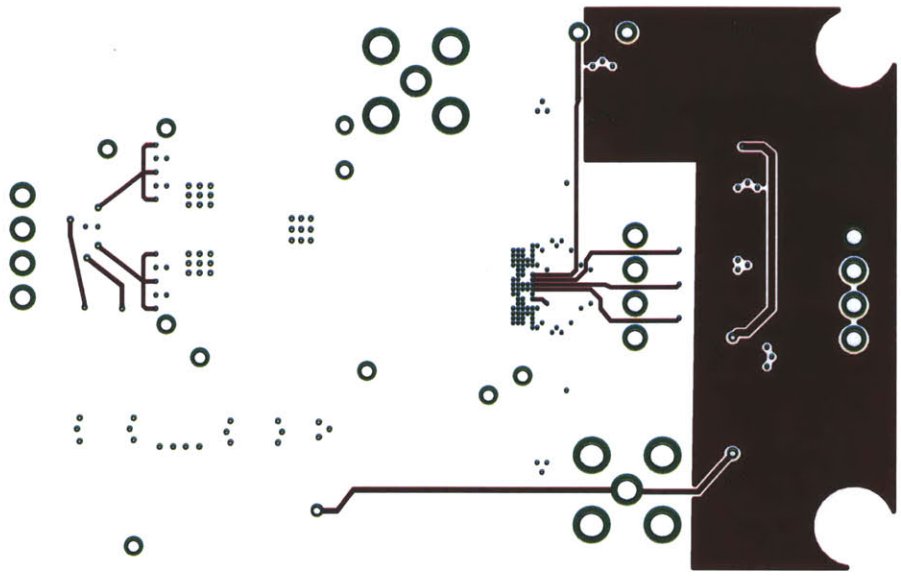


Figure A-14: The Layer 3 PCB Layout of the Non-isolated GaN-Si Dc-dc Converter Prototype.

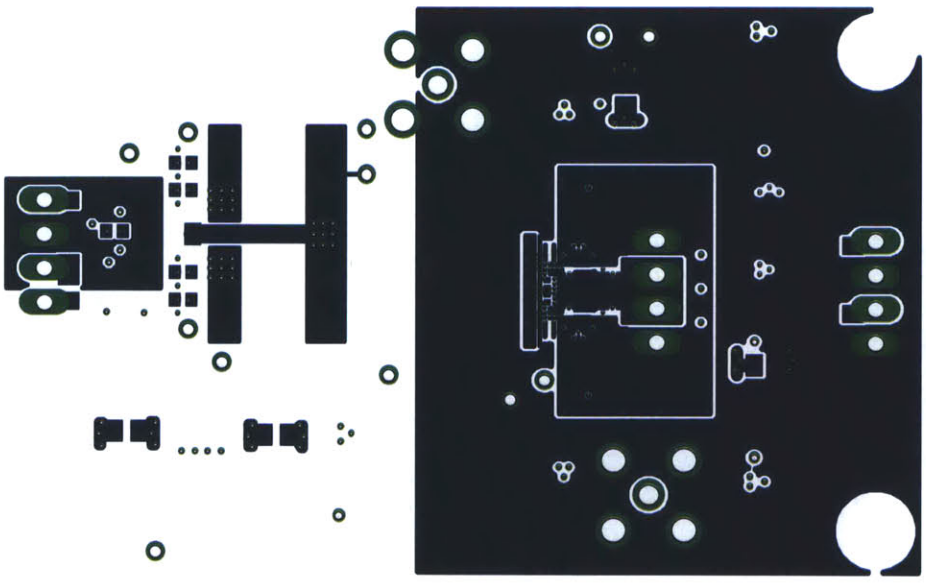


Figure A-15: The Layer 4 PCB Layout of the Non-isolated GaN-Si Dc-dc Converter Prototype.

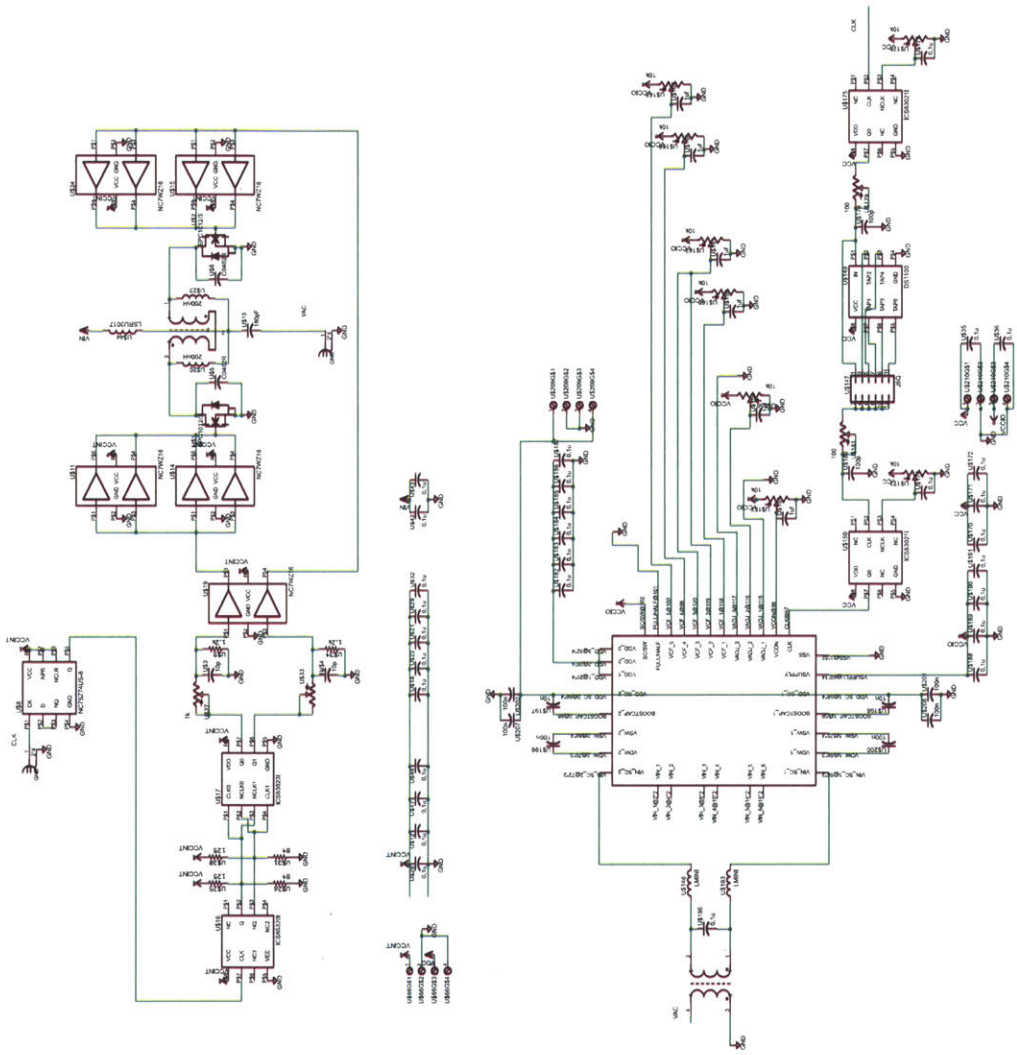


Figure A-16: The Schematic of the Isolated GaN-Si Dc-dc Converter PCB Prototype.

Table A.4: GaN-Si Dc-dc Isolated Converter Bill of Materials

Parts/Spec	Value	Description
Input Voltage	20 V	Dc
Power	4 W	-
Operation Frequency	50 MHz	-
Output Voltage	2.5 V	Dc
U150, U175	ICS83021I	Clock buffer
U8	NC7SZ74US-8	Flipflop, converts 50 MHz to 25 MHz
U149	DS1100LZ-20+	20 ns 5tap delay line, each tap is 5 ns.
U16	ICS85320I	Single-ended-to-differential clock translator
U17	ICS83023I	Differential-to-single-ended clock fanout buffer
U11, U14, U15, U24	NC7WZ16	GaN fet driver
U1, U2	EPC2012	EPC 200 V GaN power device
U44	SRU3017 2.2 uH	Choke inductor
U20	BLN1728-8A/94	1:1 coupled indcutor, 3 turns AWG 28 wire, bifilar wound, L_m=92 nH and L_{leak}=25 nH
U10	390 pF	ATC 100A rf capacitor for series resonant tank
Transformer	BLN1728-8A/94	1:1 turns ratio, 8 turns AWG 30 wire, bifilar wound, L_m=1.8 μH and L_{leak}=30 nH, leakage inductance is used for inverter output filter inductance.
U181, U179	P1E101CT	100 Ω trimmer for clk delay
U180, U178	100 pF 0805	Capacitor for clk delay
U197, U198	10 nF 01005	Capacitor for gate driver in the SC rectifier referenced to Vdd
U199, U200	0.22 μF 0204	Flying capacitor for SC rectifier
U201, U202, U207, U208	0.22 μF 0204	Output decoupling capacitor for SC rectifier
U188, U189	0.1 μF 0201	Decoupling capacitor for control circuits on chip
U190, U191	0.1 μF 0402	Decoupling capacitor for control circuits on chip
U146, U193	12.5 nH	Coilcraft MINI air core inductor for matching network
U132	320 pF	ATC 100A rf capacitor for matching network

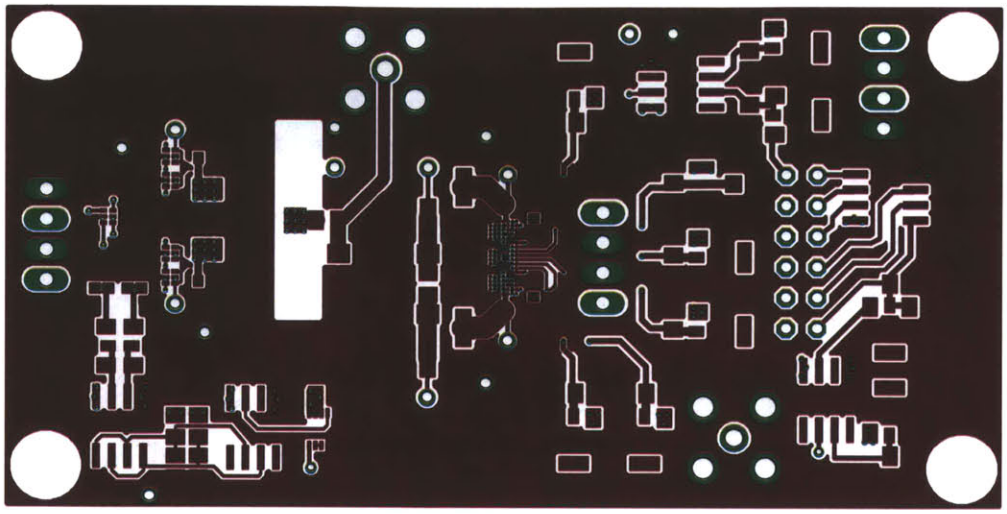


Figure A-17: The Layer 1 PCB Layout of the Isolated GaN-Si Dc-dc Converter Prototype.

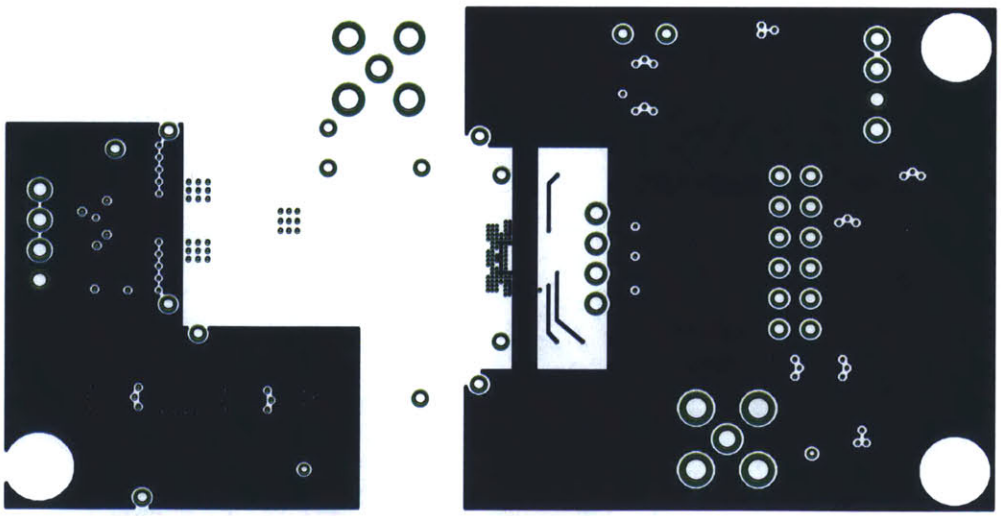


Figure A-18: The Layer 2 PCB Layout of the Isolated GaN-Si Dc-dc Converter Prototype.

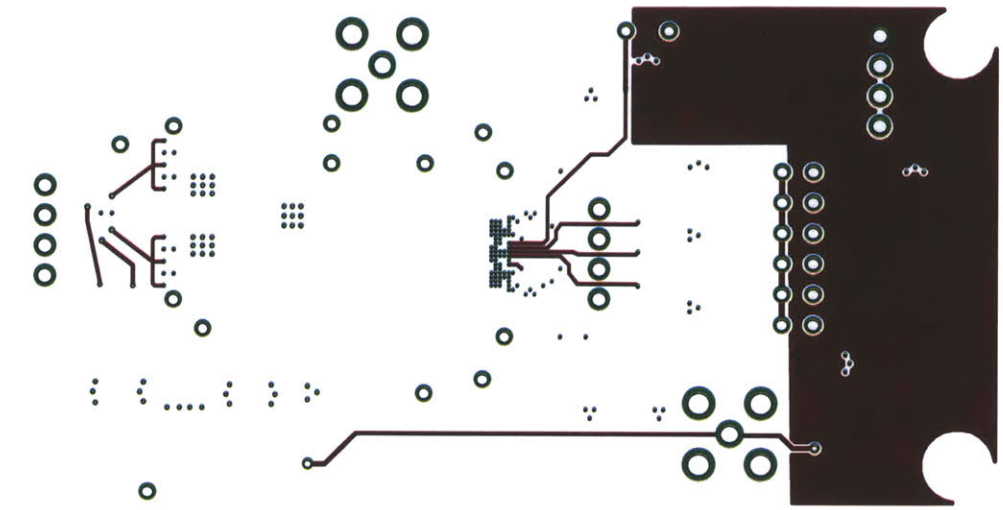


Figure A-19: The Layer 3 PCB Layout of the Isolated GaN-Si Dc-dc Converter Prototype.

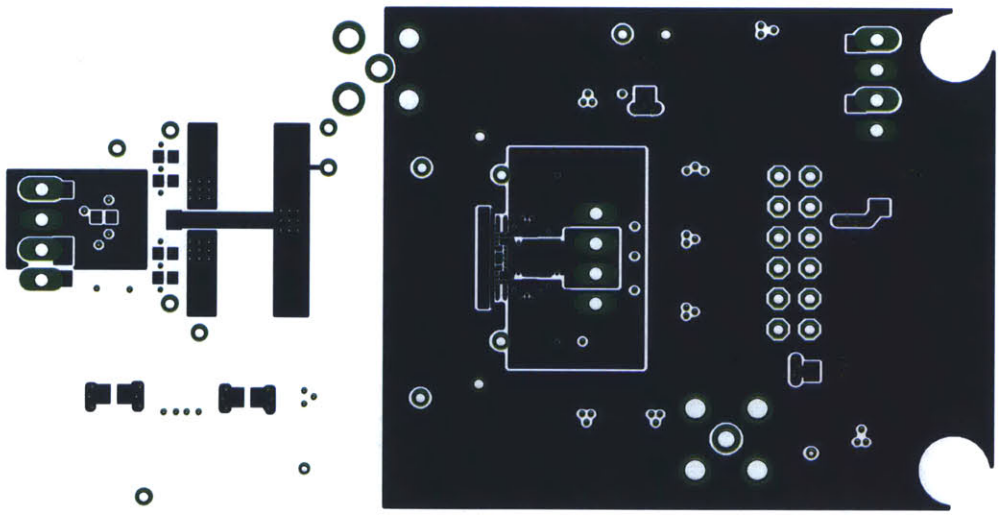


Figure A-20: The Layer 4 PCB Layout of the Isolated GaN-Si Dc-dc Converter Prototype.

A.4 Ac Power Delivery Discrete PCB

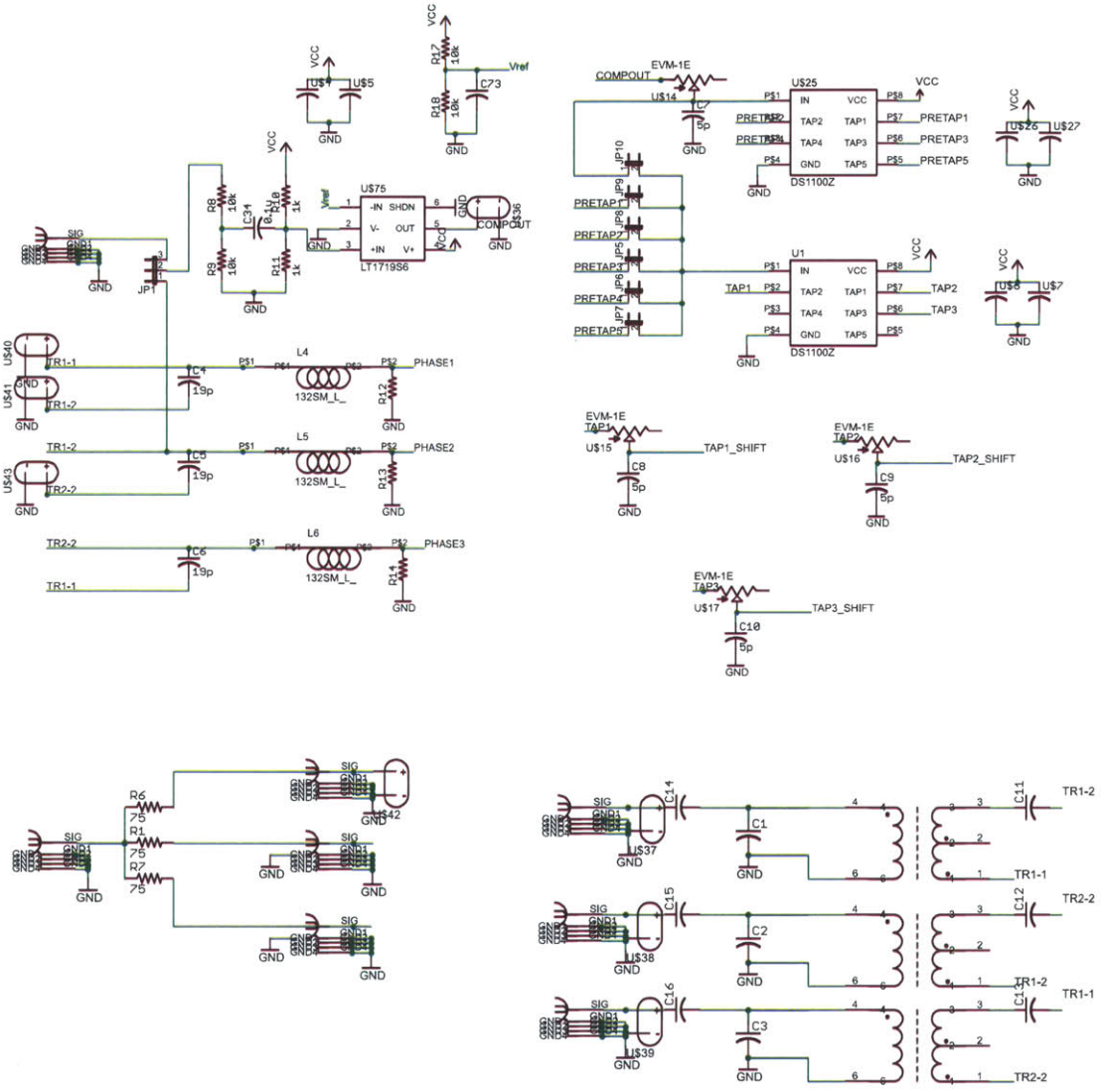


Figure A-21: The Schematic of the Ac Power Delivery Discrete PCB Prototype.

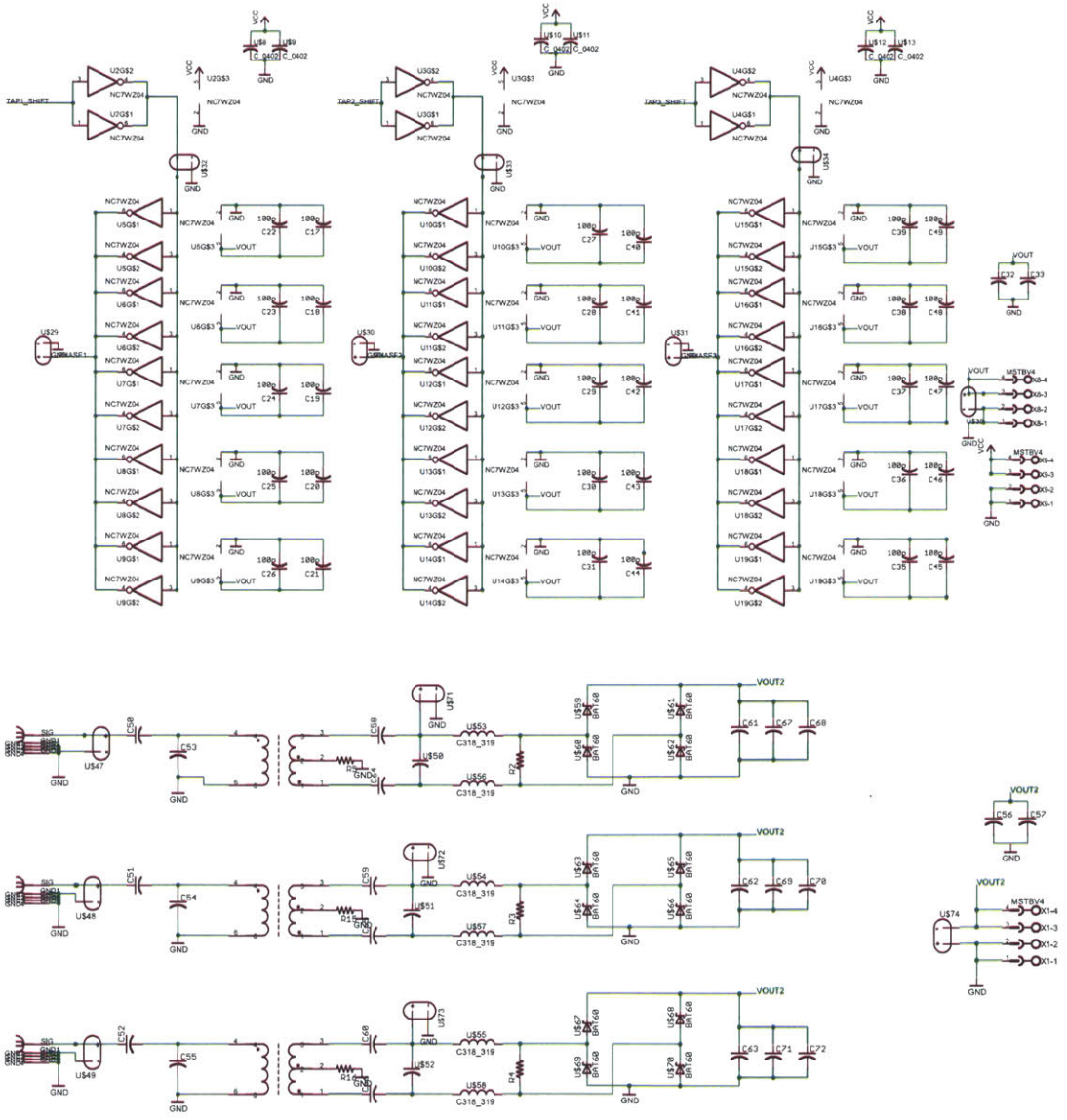


Figure A-22: The Schematic of the Ac Power Delivery Discrete PCB Prototype (cont'd).

Table A.5: Ac Power Delivery Discrete PCB Bill of Materials

Parts/Spec	**Value**	**Description**
Input Voltage	6 V	Ac amplitude
Power	0.7 W	-
Operation Frequency	50 MHz	-
Output Voltage	2 V	Dc
Coaxial cables	RG-58	1 ft, 5.32 ft and 9.64 ft coaxial cables for 3-phase power splitter
R1, R6, R7	75 Ω 0805	Resisters network to match the 50 Ω power amplifier output impedance with the 3-phase coaxial cable power splitter
Transformers	WBC8-1L	Coilcraft 8:1 rf transformer
C14, C15, C16, C50, C51, C52	680 pF	ATC 100A rf capacitor for 14.5 nH primary leakage inductance cancellation
C58, C59, C60, C64, C65, C66	32 pF	ATC 100A rf capacitor for 156 nH secondary leakage inductance cancellation
C11, C12, C13	68 pF	ATC 100A rf capacitor for 156 nH secondary leakage inductance cancellation
U53, U54, U55, U56, U57, U58	135 nH	Coilcraft MAXI air core inductor for three individual phase matching network
U50, U51, U52	39 pF	ATC 100A rf capacitor for three individual phase matching network
L4, L5, L6	47 nH	Coilcraft MIDI air core inductor for 3-phase delta connected matching network
C4, C5, C6	68 pF	ATC 100A rf capacitor for 3-phase delta connected matching network
U59 - U70	BAT60	Infineon schottky diode for rectifiers

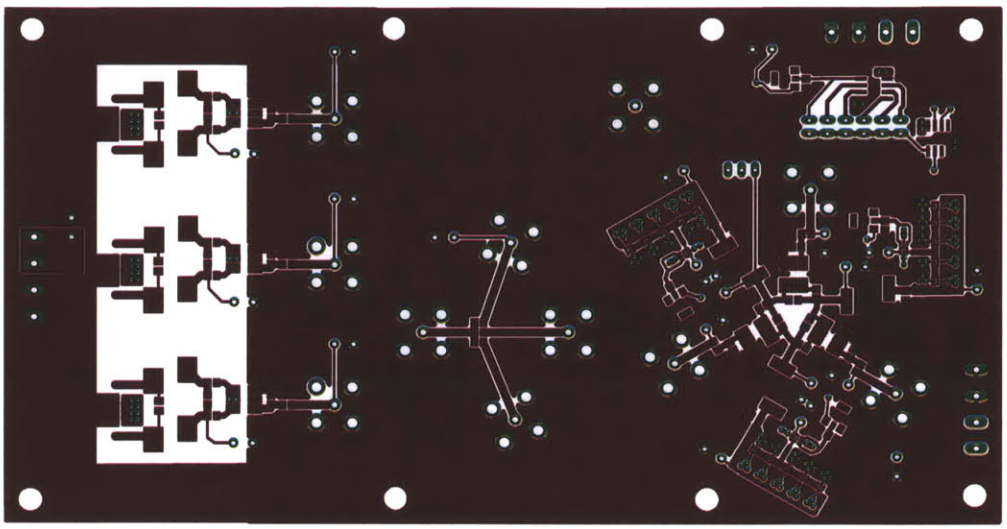


Figure A-23: The Layer 1 PCB Layout of the Ac Power Delivery Discrete PCB Prototype.

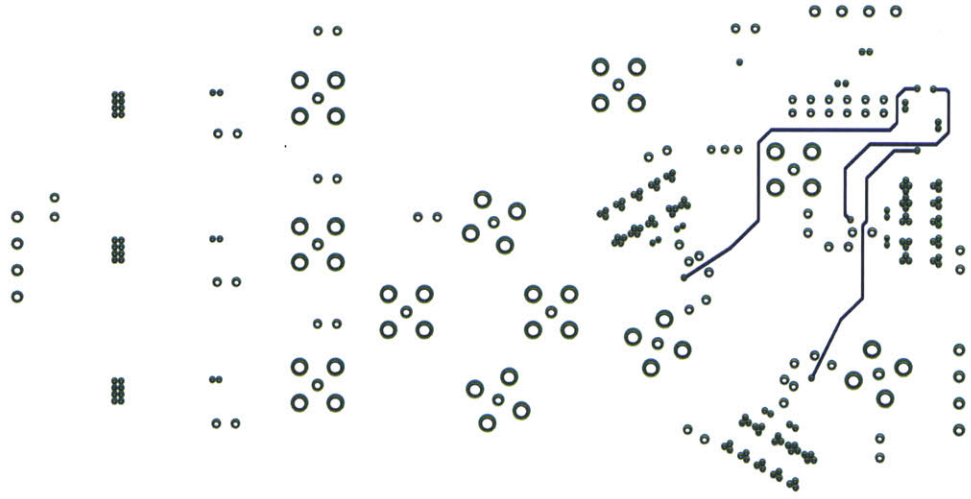


Figure A-24: The Layer 2 PCB Layout of the Ac Power Delivery Discrete PCB Prototype.

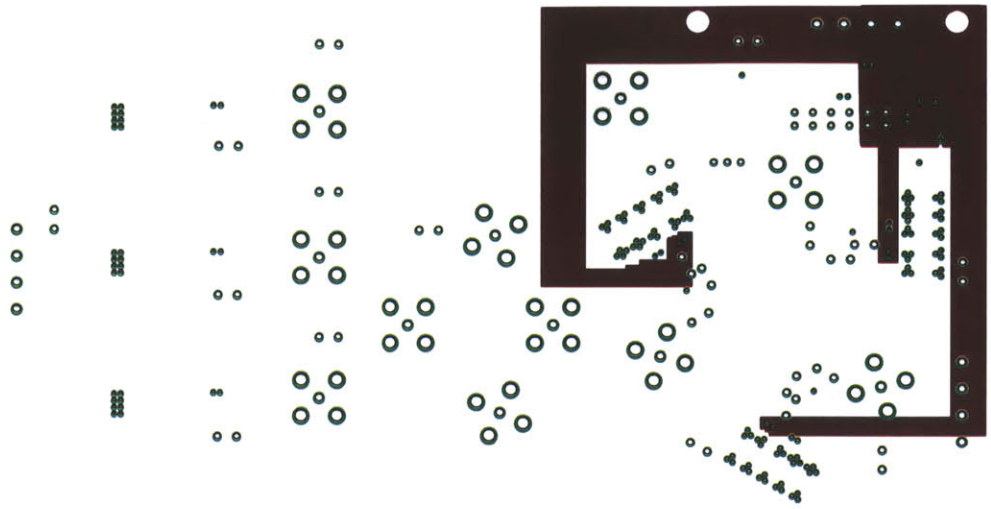


Figure A-25: The Layer 3 PCB Layout of the Ac Power Delivery Discrete PCB Prototype.

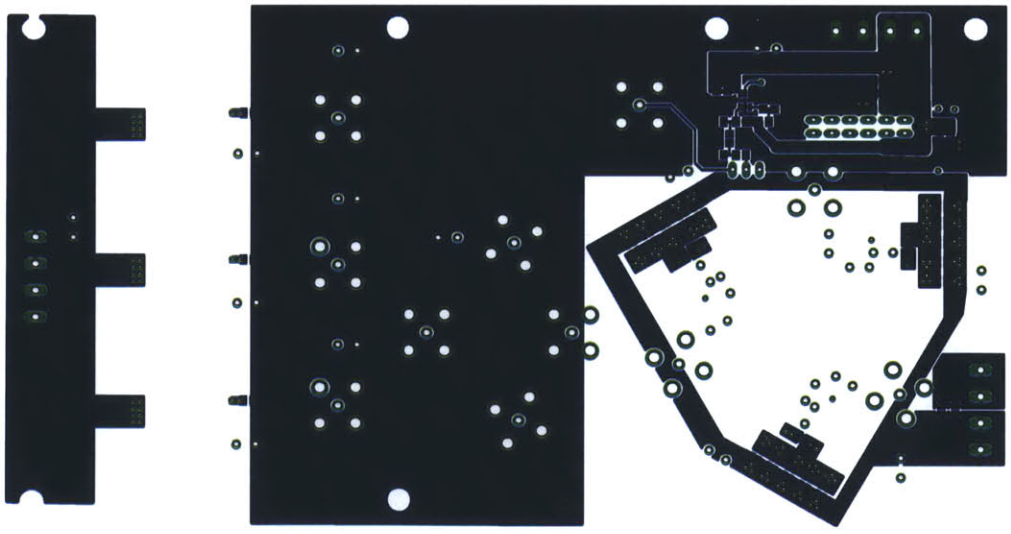


Figure A-26: The Layer 4 PCB Layout of the Ac Power Delivery Discrete PCB Prototype.

A.5 Ac Power Delivery IC PCB

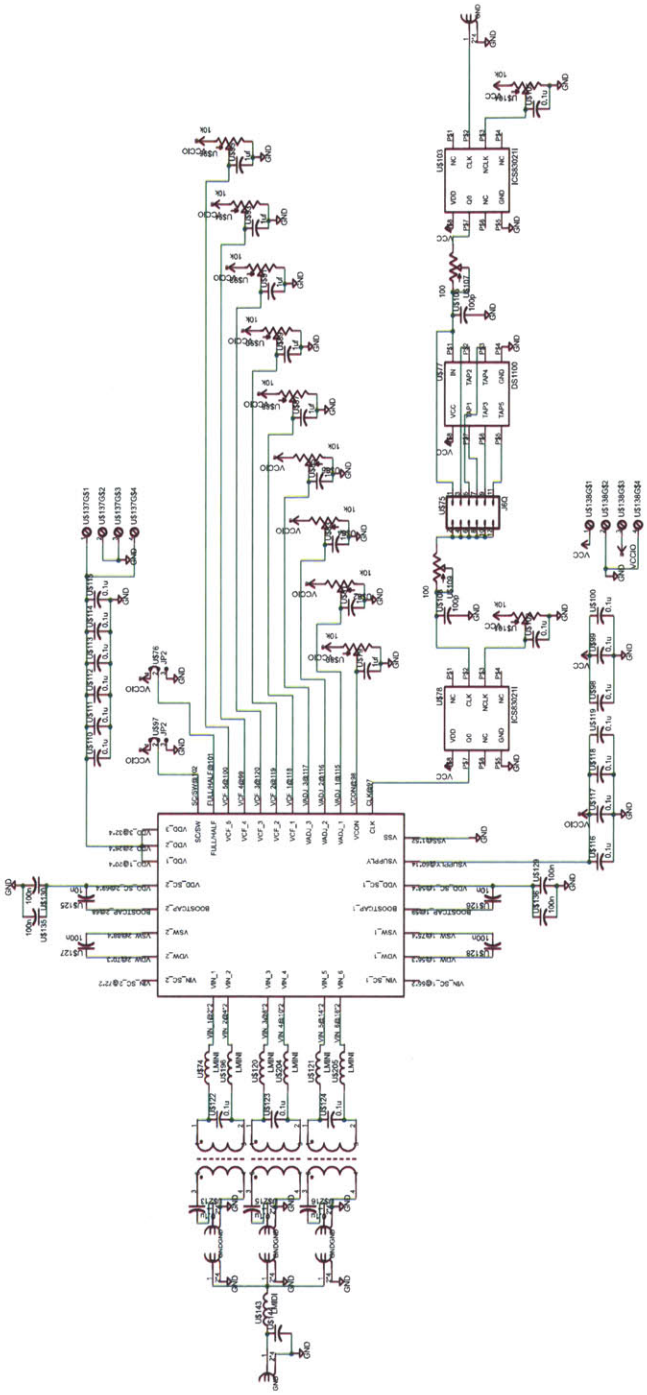


Figure A-27: The Schematic of the Ac Power Delivery 3 Individual Full-bridge IC PCB Prototype.

Table A.6: Ac Power Delivery 3 Individual Full-bridge IC Prototype Bill of Materials

Parts/Spec	**Value**	**Description**
Input Voltage	14.1 V	Ac amplitude
Power	6 W	-
Operation Frequency	50 MHz	-
Output Voltage	2.5 V	Dc
Coaxial cables	RG-58	1 ft, 5.32 ft and 9.64 ft coaxial cables for 3-phase power splitter
U143	68 nH	Coilcraft MIDI air core inductor for matching network to match the 50 Ω power amplifier output impedance to the 3-phase coaxial cables
U144	100 pF	ATC 100A rf capacitor for the matching network described above
U78, U103	ICS83021I	Clock buffer
U77	DS1100LZ-20+	20 ns 5tap delay line, each tap is 5 ns.
U107, U109	P1E101CT	100 Ω trimmer for clk delay
U106, U108	100 pF 0805	Capacitor for clk delay
U110 - U115	0.1 μF 0204	Output decoupling capacitor for SC rectifier
U116, U117	0.1 μF 0201	Decoupling capacitor for control circuits on chip
U118, U119	0.1 μF 0402	Decoupling capacitor for control circuits on chip
Transformers	BLN1728-8A/94	1:1 turns ratio, 7 turns AWG 30 wire, bifilar wound, L_m=1.2 μH and L_{leak}=30 nH
U213, U215, U216	330 pF	ATC 100A rf capacitor for leakage inductance cancellation
U74, U120, U121, U196, U204, U205	18.5 nH	Coilcraft MINI air core inductor for matching network
U122, U123, U124	240 pF	ATC 100A rf capacitor for matching network

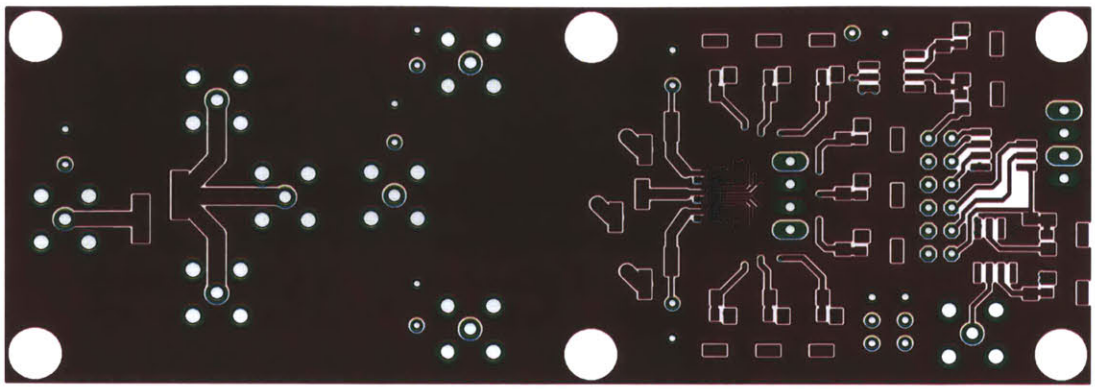


Figure A-28: The Layer 1 PCB Layout of the Ac Power Delivery 3 Individual Full-bridge IC PCB Prototype.

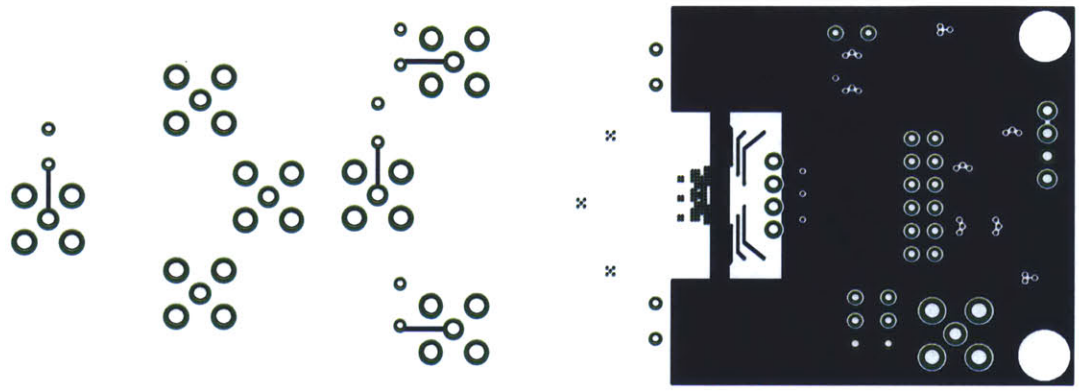


Figure A-29: The Layer 2 PCB Layout of the Ac Power Delivery 3 Individual Full-bridge IC PCB Prototype.

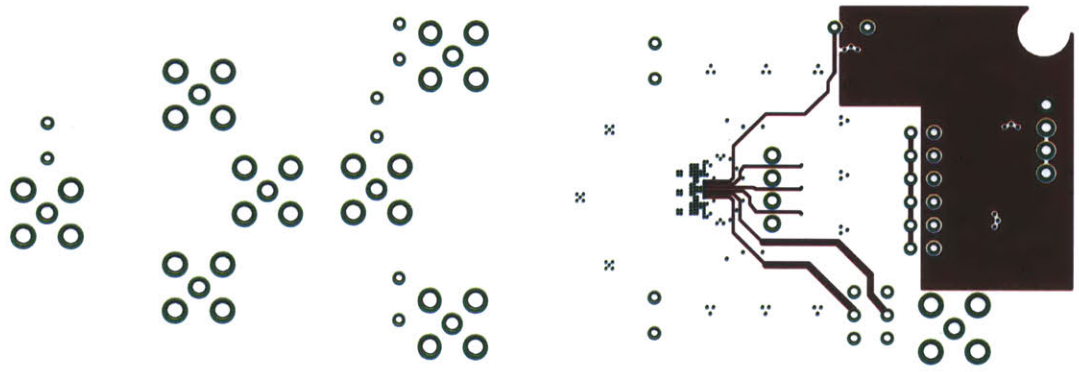


Figure A-30: The Layer 3 PCB Layout of the Ac Power Delivery 3 Individual Full-bridge IC PCB Prototype.

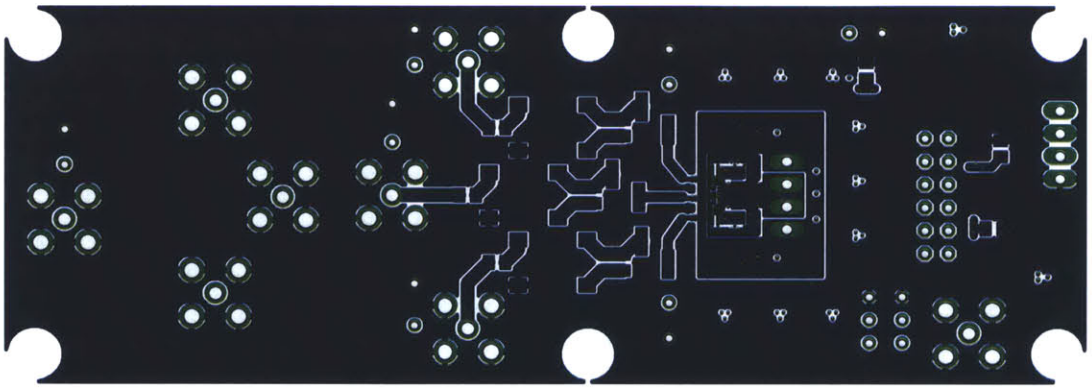


Figure A-31: The Layer 4 PCB Layout of the Ac Power Delivery 3 Individual Full-bridge IC PCB Prototype.

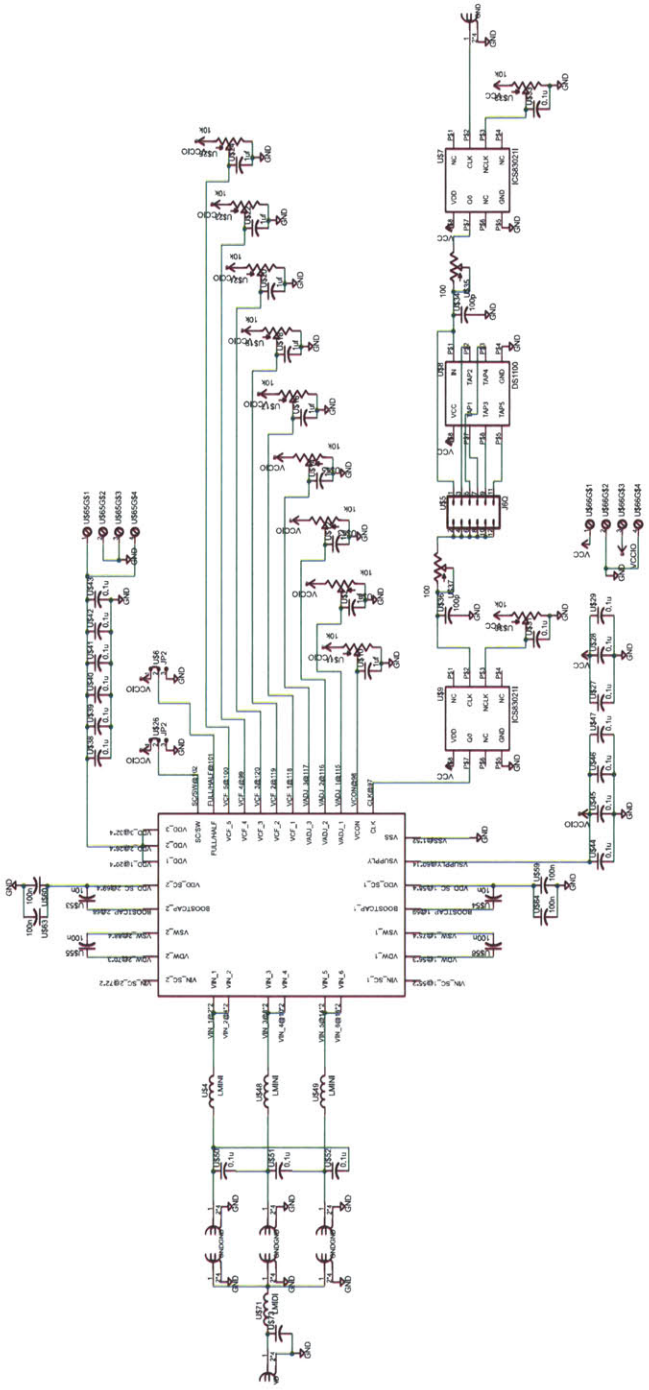


Figure A-32: The Schematic of the Ac Power Delivery Delta System IC PCB Prototype.

Table A.7: Ac Power Delivery Delta System IC Prototype Bill of Materials

Parts/Spec	**Value**	**Description**
Input Voltage	14.1 V	Ac amplitude
Power	6 W	-
Operation Frequency	50 MHz	-
Output Voltage	2.5 V	Dc
Coaxial cables	RG-58	1 ft, 5.32 ft and 9.64 ft coaxial cables for 3-phase power splitter
U71	68 nH	Coilcraft MIDI air core inductor for matching network to match the 50 Ω power amplifier output impedance to the 3-phase coaxial cables
U73	100 pF	ATC 100A rf capacitor for the matching network described above
U7, U9	ICS83021I	Clock buffer
U8	DS1100LZ-20+	20 ns 5tap delay line, each tap is 5 ns.
U35, U37	P1E101CT	100 Ω trimmer for clk delay
U34, U36	100 pF 0805	Capacitor for clk delay
U38 - U43	0.1 μF 0204	Output decoupling capacitor for SC rectifier
U44, U45	0.1 μF 0201	Decoupling capacitor for control circuits on chip
U46, U47	0.1 μF 0402	Decoupling capacitor for control circuits on chip
U4, U48, U49	18.5 nH	Coilcraft MINI air core inductor for matching network
U50, U51, U52	150 pF	ATC 100A rf capacitor for matching network

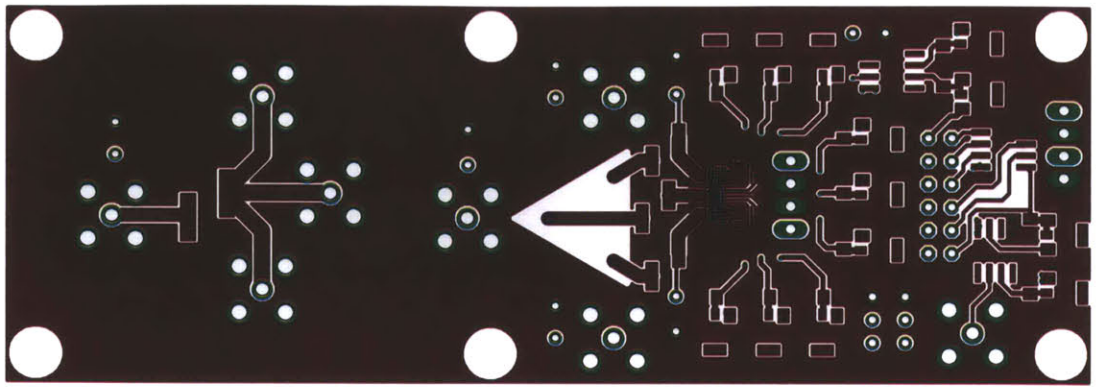


Figure A-33: The Layer 1 PCB Layout of the Ac Power Delivery Delta System IC PCB Prototype.

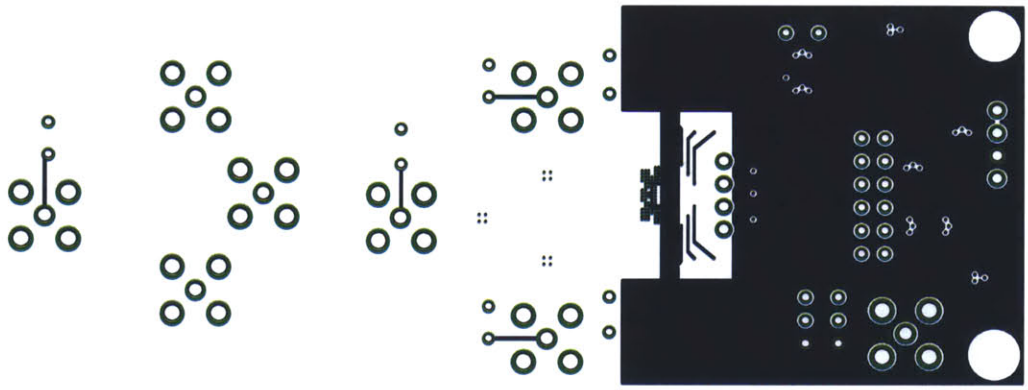


Figure A-34: The Layer 2 PCB Layout of the Ac Power Delivery Delta System IC PCB Prototype.

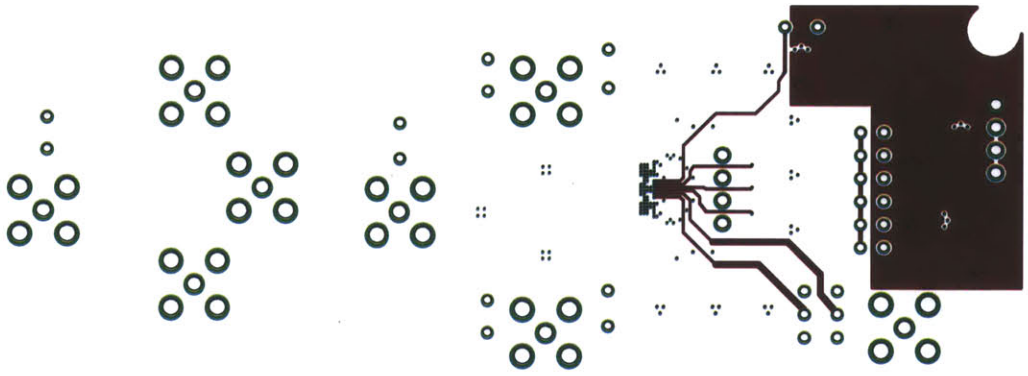


Figure A-35: The Layer 3 PCB Layout of the Ac Power Delivery Delta System IC PCB Prototype.

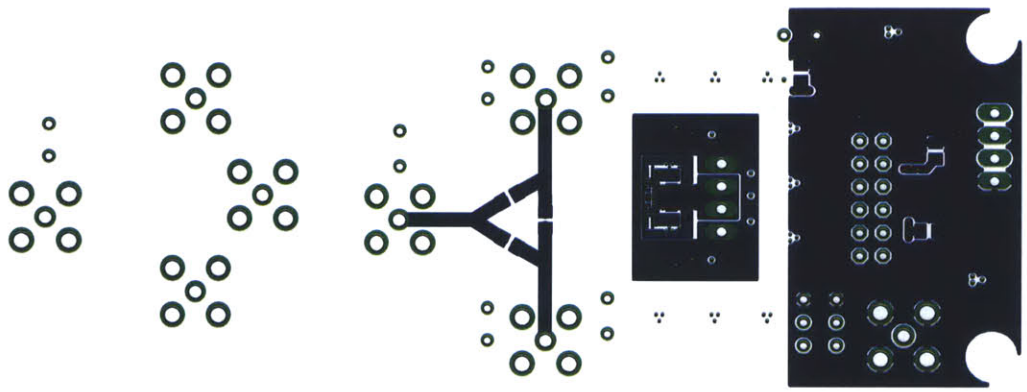


Figure A-36: The Layer 4 PCB Layout of the Ac Power Delivery Delta System IC PCB Prototype.

Appendix B

MATLAB Codes

B.1 Rectifier Optimization Codes

```
clear;
clc;
t99=tic;
%% calculate and optimize rectifier loss and parameters

%MOSFETs parameters
display(' ');
display('Si Device Parameters:');
display('***************');

Si = Si_Params('CM025_2.5');     % CM025_2.5 CM018_1.8
%IBM: BICMOS5HPE_3.3 CMRF6SF_2.5 BICMOS7WL_1.8 CMRF8SF_1.5 ...
    CMOS9SF_1.2 CMOS10SF_1.0

%rectifier operation parameters
Fs = 50e6;
```

```
D = 0.5;
Vin = Si.Voltage;       %input voltage V
Vo = Si.Voltage;      %output voltage V
Vg = Vo;         %gate voltage V
%P=Po/phase;
P=2;
Io = P/Vo;

%% for converntional bridge rectifiers
Iin = Io*pi/(sin(D*pi))^2;       %input current (A)
T = 1/Fs;
Iin_ripple = 2;      %peak to peak input current ripple ratio
Vo_ripple = 0.05;     %peak to peak output voltage ripple ratio

[Loss,Co,Wp_opt,Wn_opt,TF]= ...
    Rectifier(Si,Vin,Vo,Vg,Iin,D,P,Vo_ripple,Fs);


%% for switched-capacitor rectifiers
Iin = Io*pi/(sin(D*pi))^2/2;       %input current (A)

[Loss,Co,Wp_opt1,Wn_opt1,TF]= ...
    SC_Rectifier(Si,Vin,Vo,Vg,Iin,D,P,Vo_ripple,Fs);

display(' ');
toc(t99)



% this function calculates the loss of the rectifier and optimizes ...
   the size
% of the MOSFETs.
function [Loss,Co,Wp_opt,Wn_opt,TF]= ...
Rectifier(Si,Vin,Vo,Vg,Iin,D,P,Vo_ripple,Fs)
```

```
%% Rectifier parameters

Co = P/Vo/Fs/2/(Vo*Vo_ripple);
%calculate the output filter capacitance based on output voltage ratio


% converter loss mechanisms

%Conduction loss
P_con_n = @(Wn)1/4*Iin.^2*Si.Rcn0./Wn;
P_con_p = @(Wp)1/4*Iin^2*Si.Rcp0./Wp;

%Capacitive loss
P_cap_n = @(Wn)Fs*Vg^2*(Si.Cgn0*Wn) + Fs*Vo^2*(Si.Con0*Wn);
P_cap_p = @(Wp)Fs*Vg^2*(Si.Cgp0*Wp) + Fs*Vo^2*(Si.Cop0*Wp);

%Gate driver loss
%If each stage has the same propagation delay, short circuit loss is
%negligible, so we only account for the switching capacitive loss
%(Anthony J. S)

%from the propagation delay optimization
%the taper factor is

%inverter Wp/Wn ratio
%assuming Wp/Wn = 3/1 to have the same L->H and H->L transition
%2.5 for IBM 65nm
alpha=3;

%TF = 0:10/10000:10;
%y = TF.*(log(TF)-1)-(Con0+alpha*Cop0)/(Cgn0+alpha*Cgp0);
%plot(TF,y)
```

```
Cx = (Si.Con0+alpha*Si.Cop0);
Cy = (Si.Cgn0+alpha*Si.Cgp0);
x=fsolve(@(x)(x.*(log(x)-1)-Cx/Cy),[1.1, 10]);
TF=1/x(1,1);  %optimal tapper factor for propagation delay (Brian S. C)

%by sweeping the tapper factor, we can get different sets of optimal ...
   sizes
%for transistors. Then we manually verify and decide the final ...
   optimal TF
%for the converter.
TF=1/6;     %accoding to simulation, TF=1/11 for soft-switching and ...
   TF=1/9 for hard-switching

%since the last stage of the driver is one single power MOSFET ...
   instead of
%an inverter as previous stages. As a result, we converter the ...
   equivalent
%width of an inverter to give the same input capacitance as the power
%MOSFET.
Wn_eff = @(Wn) Wn*Si.Cgn0/Cy;
Wp_eff = @(Wp) Wp*Si.Cgp0/Cy;

%for n stages, the power consumption of the gate driver is
%P_drv = Fs*Vg^2*(Wn_eff+Wp_eff)*(Cx+Cy)*TF*(1-TF^n)/(1-TF);

%since the power dissipation in the input stages is insignificant, ...
   so we
%can let the number of stages n -> inf, then we can eliminate the ...
   variable
%n.
P_drv_n= @(Wn)Fs*Vg^2*Wn_eff(Wn)*(Cx+Cy)*TF/(1-TF);
P_drv_p= @(Wp)Fs*Vg^2*Wp_eff(Wp)*(Cx+Cy)*TF/(1-TF);
```

```
%% Optimization process
display(' ');
display('Optimizing Power MOSFET Size');
display(' ');
%as a result, the total loss in the system is
%P_tot = P_con_n(Wn) + P_con_p(Wp) + P_cap_n(Wn) +  P_cap_p(Wp) + ...
    P_drv_n(Wn) + P_drv_p(Wp)
%         + P_bw_in + P_bw_out + P_L;

%optimize the width for NMOS by letting the deritive of the total loss
%respect to Wn to be zero
P_tot_dWn = @(Wn)-1/4*Iin.^2*Si.Rcn0./Wn.^2 + Fs*Vg^2*Si.Cgn0 + ...
    Fs*Vo^2*Si.Con0*Wn +Fs*Vg^2*Si.Cgn0/Cy*(Cx+Cy)*TF/(1-TF);
Wn = fsolve(P_tot_dWn, [100e-6, 0.1]);
Wn_opt = Wn(1,1);

%optimize the width for PMOS by letting the deritive of the total loss
%respect to Wp to be zero
P_tot_dWp = @(Wp)-1/4*Iin.^2*Si.Rcp0./Wp.^2 + Fs*Vg^2*Si.Cgp0 + ...
    Fs*Vo^2*Si.Cop0*Wp +Fs*Vg^2*Si.Cgp0/Cy*(Cx+Cy)*TF/(1-TF);
Wp = fsolve(P_tot_dWp, [100e-6, 0.1]);
Wp_opt = Wp(1,1);

%display summary
Loss.P_con_n = P_con_n(Wn_opt);
Loss.P_con_p = P_con_p(Wp_opt);
Loss.P_cap_n = P_cap_n(Wn_opt);
Loss.P_cap_p = P_cap_p(Wp_opt);
Loss.P_drv_n = P_drv_n(Wn_opt);
Loss.P_drv_p = P_drv_p(Wp_opt);

display(['Input Voltage = ', num2str(Vin), 'V']);
display(['Input Current = ', num2str(Iin), 'A']);
display(['Output Voltage = ', num2str(Vo), 'V']);
```

```
%Switching_Freqency = Fs;
display(['Switching Frequency: ', num2str(Fs/1e6), 'MHz']);
display(['Output voltage ripple: ', num2str(Vo_ripple*100), '%']);
display(['Output filter capacitance: ', num2str(Co/1e-6), 'uF']);
%Taper_Factor = TF;
display(['Taper_Factor is ', num2str(TF)]);
Loss.Total = Loss.P_con_n + Loss.P_con_p + Loss.P_cap_n +  ...
    Loss.P_cap_p + Loss.P_drv_n + Loss.P_drv_p;

display(['Optimal Width of NMOS: ', num2str(Wn_opt*1e6), 'um']);
display(['Optimal Width of PMOS: ', num2str(Wp_opt*1e6), 'um']);
display(['Total Loss = ', num2str(Loss.Total)]);
Efficiency = (1 - Loss.Total/P)*100;
display(['Efficiency of the Converter: ', num2str(Efficiency), '%']);

%plot the loss distribution
result = [Loss.P_con_n  Loss.P_con_p  Loss.P_cap_n   Loss.P_cap_p   ...
    Loss.P_drv_n  Loss.P_drv_p]*1e3;

figure('Name','Power Losses Distribution','NumberTitle','off')
pie(result, ...
    {['Pcon_n ',num2str(Loss.P_con_n/Loss.Total*100, '%2.1f'),'%'], ...
    ['Pcon_p ',num2str(Loss.P_con_p/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pcap_n ',num2str(Loss.P_cap_n/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pcap_p ',num2str(Loss.P_cap_p/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pdrv_n ',num2str(Loss.P_drv_n/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pdrv_p ',num2str(Loss.P_drv_p/Loss.Total*100, '%2.1f'),'%'],  ...
    })

display(' ');
end
```

```
% this function calculates the loss of the rectifier and optimizes ...
    the size
% of the MOSFETs.
function [Loss,Co,Wp_opt1,Wn_opt1,TF]= ...
SC_Rectifier(Si,Vin,Vo,Vg,Iin,D,P,Vo_ripple,Fs)


%% Rectifier parameters

Co = P/Vo/Fs/2/(Vo*Vo_ripple);
%calculate the output filter capacitance based on output voltage ratio


% converter loss mechanisms

%Conduction loss
P_con_n = @(Wn)1/4*Iin.^2*Si.Rcn0./Wn;
P_con_p = @(Wp)1/4*Iin^2*Si.Rcp0./Wp;

%Capacitive loss
P_cap_n = @(Wn)Fs*Vg^2*(Si.Cgn0*Wn) + Fs*Vo^2*(Si.Con0*Wn);
P_cap_p = @(Wp)Fs*Vg^2*(Si.Cgp0*Wp) + Fs*Vo^2*(Si.Cop0*Wp);

%Gate driver loss
%If each stage has the same propagation delay, short circuit loss is
%negligible, so we only account for the switching capacitive loss
%(Anthony J. S)

%from the propagation delay optimization
%the taper factor is

%inverter Wp/Wn ratio
%assuming Wp/Wn = 3/1 to have the same L->H and H->L transition
%2.5 for IBM 65nm
```

```
alpha=3;

%TF = 0:10/10000:10;
%y = TF.*(log(TF)-1)-(Con0+alpha*Cop0)/(Cgn0+alpha*Cgp0);
%plot(TF,y)
Cx = (Si.Con0+alpha*Si.Cop0);
Cy = (Si.Cgn0+alpha*Si.Cgp0);
x=fsolve(@(x)(x.*(log(x)-1)-Cx/Cy),[1.1, 10]);
TF=1/x(1,1);  %optimal tapper factor for propagation delay (Brian S. C)

%by sweeping the tapper factor, we can get different sets of optimal ...
   sizes
%for transistors. Then we manually verify and decide the final ...
   optimal TF
%for the converter.
TF=1/6;    %accoding to simulation, TF=1/11 for soft-switching and ...
   TF=1/9 for hard-switching

%since the last stage of the driver is one single power MOSFET ...
   instead of
%an inverter as previous stages. As a result, we converter the ...
   equivalent
%width of an inverter to give the same input capacitance as the power
%MOSFET.
Wn_eff = @(Wn) Wn*Si.Cgn0/Cy;
Wp_eff = @(Wp) Wp*Si.Cgp0/Cy;

%for n stages, the power consumption of the gate driver is
%P_drv = Fs*Vg^2*(Wn_eff+Wp_eff)*(Cx+Cy)*TF*(1-TF^n)/(1-TF);

%since the power dissipation in the input stages is insignificant, ...
   so we
%can let the number of stages n -> inf, then we can eliminate the ...
   variable
```

```
%n.
P_drv_n= @(Wn)Fs*Vg^2*Wn_eff(Wn)*(Cx+Cy)*TF/(1-TF);
P_drv_p= @(Wp)Fs*Vg^2*Wp_eff(Wp)*(Cx+Cy)*TF/(1-TF);


%% Optimization process
display(' ');
display('Optimizing Power MOSFET Size');
display(' ');
%as a result, the total loss in the system is
%P_tot = P_con_n(Wn) + P_con_p(Wp) + P_cap_n(Wn) +  P_cap_p(Wp) + ...
    P_drv_n(Wn) + P_drv_p(Wp)
%         + P_bw_in + P_bw_out + P_L;

%optimize the width for NMOS of the floating bridge by letting the ...
    deritive of the total loss
%respect to Wn to be zero
P_tot_dWn = @(Wn)-1/4*Iin.^2*Si.Rcn0./Wn.^2 + Fs*Vg^2*Si.Cgn0 + ...
     Fs*Vo^2*Si.Con0*Wn;
Wn = fsolve(P_tot_dWn, [100e-6, 0.1]);
Wn_opt1 = Wn(1,1);


%optimize the width for the NMOS sitting on the Vout
P_tot_dWn = @(Wn)-1/4*Iin.^2*0.9199^2*Si.Rcn0./Wn.^2 + ...
     Fs*Vg^2*Si.Cgn0 + Fs*Vo^2*Si.Con0*Wn + ...
     Fs*Vg^2*Si.Cgn0/Cy*(Cx+Cy)*TF/(1-TF);
Wn = fsolve(P_tot_dWn, [100e-6, 0.1]);
Wn_opt2 = Wn(1,1);


%optimize the width for the NMOS in the low-side bridge
P_tot_dWn = @(Wn)-1/4*Iin.^2*1.8535^2*Si.Rcn0./Wn.^2 + ...
     Fs*Vg^2*Si.Cgn0 + Fs*Vo^2*Si.Con0*Wn + ...
```

```
    Fs*Vg^2*Si.Cgn0/Cy*(Cx+Cy)*TF/(1-TF);
Wn = fsolve(P_tot_dWn, [100e-6, 0.1]);
Wn_opt3 = Wn(1,1);


%optimize the width for PMOS of the floating bridge by letting the ...
   deritive of the total loss
%respect to Wp to be zero
P_tot_dWp = @(Wp)-1/4*Iin.^2*Si.Rcp0./Wp.^2 + Fs*Vg^2*Si.Cgp0 + ...
    Fs*Vo^2*Si.Cop0*Wp;
Wp = fsolve(P_tot_dWp, [100e-6, 0.1]);
Wp_opt1 = Wp(1,1);


%optimize the width for PMOS in the low-side bridge
P_tot_dWp = @(Wp)-1/4*Iin.^2*Si.Rcp0./Wp.^2 + Fs*Vg^2*Si.Cgp0 + ...
    Fs*Vo^2*Si.Cop0*Wp +Fs*Vg^2*Si.Cgp0/Cy*(Cx+Cy)*TF/(1-TF);
Wp = fsolve(P_tot_dWp, [100e-6, 0.1]);
Wp_opt2 = Wp(1,1);


%display summary
Loss.P_con_n = P_con_n(Wn_opt1) + P_con_n(Wn_opt2)*0.9199^2 + ...
    P_con_n(Wn_opt3)*1.8535^2;
Loss.P_con_p = P_con_p(Wp_opt1) + P_con_p(Wp_opt2);
Loss.P_cap_n = P_cap_n(Wn_opt1) + P_cap_n(Wn_opt2) + P_cap_n(Wn_opt3);
Loss.P_cap_p = P_cap_p(Wp_opt1) + P_cap_p(Wp_opt2);
Loss.P_drv_n = P_drv_n(Wn_opt2) + P_drv_n(Wn_opt3);
Loss.P_drv_p = P_drv_p(Wp_opt2);
Loss.P_bypass = 0.1*1/4*Iin.^2;


display(['Input Voltage = ', num2str(Vin), 'V']);
display(['Input Current = ', num2str(Iin), 'A']);
```

```
display(['Output Voltage = ', num2str(Vo), 'V']);
%Switching_Freqency = Fs;
display(['Switching Frequency: ', num2str(Fs/1e6), 'MHz']);
display(['Output voltage ripple: ', num2str(Vo_ripple*100), '%']);
display(['Output filter capacitance: ', num2str(Co/1e-6), 'uF']);
%Taper_Factor = TF;
display(['Taper_Factor is ', num2str(TF)]);
Loss.Total = Loss.P_con_n + Loss.P_con_p + Loss.P_cap_n +  ...
    Loss.P_cap_p + Loss.P_drv_n + Loss.P_drv_p + Loss.P_bypass;

display(['Optimal Width of NMOS: ', num2str(Wn_opt1*1e6), 'um']);
display(['Optimal Width of PMOS: ', num2str(Wp_opt1*1e6), 'um']);
display(['Total Loss = ', num2str(Loss.Total)]);
Efficiency = (1 - Loss.Total/P)*100;
display(['Efficiency of the Converter: ', num2str(Efficiency), '%']);

%plot the loss distribution
result = [Loss.P_con_n  Loss.P_con_p  Loss.P_cap_n   Loss.P_cap_p  ...
    Loss.P_drv_n  Loss.P_drv_p  Loss.P_bypass]*1e3;

figure('Name','Power Losses Distribution','NumberTitle','off')
pie(result, {['Pcon_n ',num2str(Loss.P_con_n/Loss.Total*100, ...
   '%2.1f'),'%'], ...
    ['Pcon_p ',num2str(Loss.P_con_p/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pcap_n ',num2str(Loss.P_cap_n/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pcap_p ',num2str(Loss.P_cap_p/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pdrv_n ',num2str(Loss.P_drv_n/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pdrv_p ',num2str(Loss.P_drv_p/Loss.Total*100, '%2.1f'),'%'],  ...
    ['Pbypass ',num2str(Loss.P_bypass/Loss.Total*100, '%2.1f'),'%'], ...
        ...
    })

display(' ');
end
```

B.2 Matching Network Calculation Codes

```
%*****************************************************************
%Matching Network Calculation
%
%The inductors we used in here are provided from Prof.Sullican in ...
    Dartmouth
%since the inductor structure is a one-terun inductor,  the ...
    inductance is
%proportional to the length, so we assume that the Q for the inductor
%is constant.
% -------|----|Xs|---
% Vp    |Xp|         Vs
% -------|-----------
%*****************************************************************
function [L, C, Eta, ...
    Area]=Matching_network(Vp,Vs,Rs,config_cap,config,stage,Fs)

%% calculate the Q of inductor
%inductor depth = 95.1um
L_unit = 1.7e-9;     %H/mm
L_w = 212e-6;          %inductor width (m)
%Rdc = 6.808m ohm
Rac = 18.68e-3; %ohm @100MHz
%Rac = 25e-3/2; %ohm @50MHz

%since the matching network only carries AC
Q_L = 2*pi*Fs*L_unit/Rac;

%% calculate matching network component values and efficiency

display('************************ ');
```

```
display('Matching Network Parameters: ');
display(' ');

Rp=Rs*Vp^2/Vs^2;
i=1;
Ratio = (Vp/Vs)^(2/stage);
Q = sqrt((Vp/Vs)^(2/stage)-1);      % Quality factor of each stage
Eta = 1;
C_Area = 0;
L_Area = 0;

for i=1:stage

    Rs(i+1) = Rs(i);
    Rs(i) = Rp(i)/Ratio;
    Rp(i+1) = Rs(i);
    switch config

        case(1)

            L(i) = Q*Rs(i)/(2*pi*Fs);
            C(i) = Q/Rp(i)/(2*pi*Fs);
            [Resr, Q_C, area]=MOSCAP_Q(config_cap,C(i),Fs);        ...
               %calculate the Q of the MOScap
            Q_C=100;
            Q_L=70;
            Eta = Eta*(1-Q/Q_C)/(1+Q/Q_L);
            display(['L', num2str(i), ' = ', num2str(L(i)/1e-9), 'nH']);
            display(['C', num2str(i), ' = ', num2str(C(i)/1e-12), ...
               'pF']);
            display('************************ ');
            L_Area = L_Area + L(i)/L_unit*1e-3*L_w
            C_Area = C_Area + area
            display('************************ ');
```

```
            display(' ');
            i=i+1;


        case(2)

            L(i) = Rp(i)/Q/(2*pi*Fs);
            C(i) = 1/Q/Rs(i)/(2*pi*Fs);
            [Resr, Q_C, area]=MOSCAP_Q(config_cap,C(i),Fs);        ...
               %calculate the Q of the MOScap
            Eta = Eta*(1-Q/Q_L)/(1+Q/Q_C);
            display(['L', num2str(i), ' = ', num2str(L(i)/1e-9), 'nH']);
            display(['C', num2str(i), ' = ', num2str(C(i)/1e-12), ...
               'pF']);
            display('************************ ');
            L_Area = L_Area + L(i)/L_unit*1e-3*L_w
            C_Area = C_Area + area
            display('************************ ');
            display(' ');
            i=i+1;

    end
end

Area = C_Area + L_Area;

display(['Efficiency: ', num2str(Eta*100), '%']);
display(['Total Area: ', num2str(Area*1e6), 'mm^2']);



display(' ');
```

B.3 Polyphase Matching Network Codes

```
%*****************************************************************
%Matching Network Calculation
%
%The inductors we used in here are provided from Prof.Sullican in ...
   Dartmouth
%since the inductor structure is a one-terun inductor,  the ...
   inductance is
%proportional to the length, so we assume that the Q for the inductor
%is constant.
% -------|-----|Xs|---
% Vp    |Xp|         Vs
% -------|------------
%*****************************************************************
clear;
clc;
t99=tic;

%% parameters of the network
%Vp =sqrt(2*50*6/3)*2*sqrt(3);     %input voltage (V) peak to peak
%Vp =sqrt(2*50*5)*2;
%Vp =sqrt(2*65*6/3)*2;
Vp = 28;

Vo = 2.5;
%Vo = Vo*4/pi;     %get the fundamental of square waveform
Vs = 10;      %output voltage (V)
%Vs = Vs*4/pi;    %get the fundamental of square waveform


D=0.5;       %duty ratio for rectifier
```

```
Po=5;       % power transfer
P=Po;
%35m ohm is the on-resistance from the MOSFET switches
%Rs=Vs^2/P*2/pi^2*(sin(pi*D))^2;

%Rp=Rs*Vp^2/Vs^2;
%Rp=Rs*Vp^2/Vs^2/2;

Fs = 50e6;    %switching frequency 100MHz

config_cap = 1; %1. integrated; 2. with bumps and route the ...
    interconnect externally
stage = 1;
%stage = num2str(n);
%for the optimal efficiency, the Q should be the same in every stage
%from n1+n2+n3+... =< n*(n1*n2*n3*...)^(1/n)


%% calculate matching network component values and efficiency

display(' ');
config = 1;      %1. low pass; 2. high pass

%Rs=Vo^2/P/2;
Rs=Vs^2/P*2/pi^2*(sin(pi*D))^2; %full bridge
%Rs=2/0.8*(Vs/Vp)^2;
%Rs=2*Vs^2/P/pi^2*(sin(pi*D))^2; %half bridge
Vs = Vs*4/pi;    %get the fundamental of square waveform
[L, C, Eta, Area]=Matching_network(Vp,Vs,Rs,config_cap,config,stage,Fs);

%Q=4;    %Q of the total network
%[L1, L2, C, Eta, ...
    Area]=Matching_network_pi(Vp,Vs,Rs,config_cap,config,stage,Fs,Q);
```

```
%% calculate Multi-phase matching network component values and ...
   efficiency

display(' ');
config = 1;      %1. low pass; 2. high pass
phase=3; % only work for 3 and 4 phases!!!!!

Phase_type = '3';

    switch Phase_type
        case{'1'}
            Vs=Vo;
            P=Po;
            Rs=2*Vs^2/P/pi^2*(sin(pi*D))^2; %half bridge
            Vs = Vs*4/pi;    %get the fundamental of square waveform
            [L, C, Eta, Area]= ...
            Matching_network(Vp,Vs,Rs,config_cap,config,stage,Fs);

        case{'2'}
            Vs=2*Vo;
            P=Po;
            Rs=Vs^2/P*2/pi^2*(sin(pi*D))^2; %full bridge
            Vs = Vs*4/pi;    %get the fundamental of square waveform
            [L, C, Eta, Area]= ...
            Matching_network(Vp,Vs,Rs,config_cap,config,stage,Fs);

        otherwise
            Vs=Vo;
            P=Po/phase;
            %Vp = Vp*(2*sin(pi/phase));
            Rs=Vs^2/P*2/pi^2*(sin(pi*D))^2; %n phase rectifier
            %[L, C, Eta, Area]=Three_phase_matching_network
            %(Vp,Vs,Rs,config_cap,config,stage,Fs);
```

```
            Vs = Vs*4/pi;    %get the fundamental of square waveform
            [L, C, Eta, Area]=Multi_phase_matching_network ...
            (Vp,Vs,Rs,config_cap,config,phase,stage,Fs);

    end


    phase=4;


            Vs=Vo;
            P=Po/phase;
            %Vp = Vp*(2*sin(pi/phase));
            Rs=Vs^2/P*2/pi^2*(sin(pi*D))^2; %n phase rectifier
            %[L, C, Eta, Area]=Three_phase_matching_network
            %(Vp,Vs,Rs,config_cap,config,stage,Fs);
            Vs = Vs*4/pi;    %get the fundamental of square waveform
            [L, C, Eta, Area]=Multi_phase_matching_network ...
            (Vp,Vs,Rs,config_cap,config,phase,stage,Fs);

    phase=6;


            Vs=Vo;
            P=Po/phase;
            %Vp = Vp*(2*sin(pi/phase));
            Rs=Vs^2/P*2/pi^2*(sin(pi*D))^2; %n phase rectifier
            %[L, C, Eta, Area]=Three_phase_matching_network
            %(Vp,Vs,Rs,config_cap,config,stage,Fs);
            Vs = Vs*4/pi;    %get the fundamental of square waveform
            [L, C, Eta, Area]=Multi_phase_matching_network ...
            (Vp,Vs,Rs,config_cap,config,phase,stage,Fs);

%% calculate and optimize rectifier loss and parameters
```

```
%MOSFETs parameters
display(' ');
display('Si Device Parameters:');
display('***************');

Si = Si_Params('CM025_2.5');     %CMOS9SF_1.2 CM025_2.5 CM018_1.8 ...
    CMOS10SF_1.0

%rectifier operation parameters
Vin = 2.5;       %input voltage V
Vo = 2.5;      %output voltage V
Vg = Vo;         %gate voltage V
%P=Po/phase;
P=Po;
Io = P/Vo;
Iin = Io*pi/(sin(D*pi))^2;       %input current (A)
T = 1/Fs;
Iin_ripple = 2;      %peak to peak input current ripple ratio
Vo_ripple = 0.05;     %peak to peak output voltage ripple ratio

[Loss,Co,Wp_opt,Wn_opt,TF]=Rectifier(Si,Vin,Vo,Vg,Iin,D,P,Vo_ripple,Fs);


display(' ');
toc(t99)




%*************************************************************
%Multi Phase Matching Network Calculation
```

```
%
%The inductors we used in here are provided from Prof.Sullican in ...
    Dartmouth
%since the inductor structure is a one-terun inductor,  the ...
    inductance is
%proportional to the length, so we assume that the Q for the inductor
%is constant.
% ------|----|Xs|---
% Vp    |Xp|        Vs
% ------|----------
%*****************************************************************
function [L, C, Eta, Area]= ...
Multi_phase_matching_network(Vp,Vs,Rs,config_cap,config,phase,stage,Fs)

%% calculate the Q of inductor
%inductor depth = 95.1um
L_unit = 1.7e-9;     %H/mm
L_w = 212e-6;          %inductor width (m)
%Rdc = 6.808m ohm
Rac = 18.68e-3; %ohm @100MHz
%Rac = 25e-3/2; %ohm @50MHz

%since the matching network only carries AC
Q_L = 2*pi*Fs*L_unit/Rac;

%% calculate matching network component values and efficiency

display('************************ ');
display([num2str(phase),'-Phase Matching Network Parameters: ']);
display(' ');

Vp=Vp/(2*sin(pi/phase));
Rp=Rs*Vp^2/Vs^2;
%for balanced load, Rp get gain of 3 from the Y to Δ transformation
```

```
i=1;
Ratio = (Vp/Vs)^(2/stage);
Q = sqrt((Vp/Vs)^(2/stage)-1);      % Quality factor of each stage
Eta = 1;
C_Area = 0;
L_Area = 0;

for i=1:stage

    Rs(i+1) = Rs(i);
    Rs(i) = Rp(i)/Ratio;
    Rp(i+1) = Rs(i);
    switch config

        case(1)

            L(i) = Q*Rs(i)/(2*pi*Fs);
            C(i) = Q/Rp(i)/(2*pi*Fs)/(2*sin(pi/phase))^2;
            %convert the Y capacitance back to Δ
            [Resr, Q_C, area]=MOSCAP_Q(config_cap,C(i),Fs);
            %calculate the Q of the MOScap
            Q_C=100;
            Q_L=50;
            Eta = Eta*(1-Q/Q_C)/(1+Q/Q_L);
            %in 3 phase, the efficiency calculation is the same
                                        %as single phase. the ...
                                           parallel
                                        %resistance increased by ...
                                           a factor
                                        %of 3 but the impedance ...
                                           is also
                                        %increased by a factor of ...
                                           3. so
                                        %the parallel Q did not ...
```

```
                                                change.
            display(['L', num2str(i), ' = ', num2str(L(i)/1e-9), 'nH']);
            display(['C', num2str(i), ' = ', num2str(C(i)/1e-12), ...
                'pF']);
            display('************************ ');
            L_Area = L_Area + L(i)/L_unit*1e-3*L_w
            C_Area = C_Area + area
            display('************************ ');
            display(' ');
            i=i+1;


        case(2)

            L(i) = Rp(i)/Q/(2*pi*Fs)/phase;
            C(i) = 1/Q/Rs(i)/(2*pi*Fs);
            [Resr, Q_C, area]=MOSCAP_Q(config_cap,C(i),Fs);
            %calculate the Q of the MOScap
            Eta = Eta*(1-Q/Q_L)/(1+Q/Q_C);
            display(['L', num2str(i), ' = ', num2str(L(i)/1e-9), 'nH']);
            display(['C', num2str(i), ' = ', num2str(C(i)/1e-12), ...
                'pF']);
            display('************************ ');
            L_Area = L_Area + L(i)/L_unit*1e-3*L_w
            C_Area = C_Area + area
            display('************************ ');
            display(' ');
            i=i+1;

    end
end

Area = C_Area + L_Area;
```

```
display(['Efficiency: ', num2str(Eta*100), '%']);
display(['Total Area: ', num2str(Area*1e6), 'mm^2']);



display(' ');
end
```

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