Fabrication and characterization of germanium-on-silicon photodiodes

by

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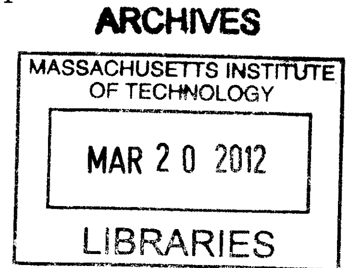

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Abstract

Germanium is becoming an increasingly popular material to use in photonic systems. Due to its strong absorption in the near infrared and its relative ease of integration on silicon, it is a promising candidate for the fabrication of CMOS-compatible photodetectors.

The goal of this thesis is to understand the physics of Ge-on-Si photodiodes, especially the dark current. Low-pressure chemical vapor deposition was used to deposit thick (1 - 2 μm) films on silicon substrates either selectively in oxide windows or in blanket films. Photodetectors were fabricated in both types of films and their optical and electronic properties are discussed.

It was found that the main source of leakage current in these detectors is the generation of carriers at the Ge/passivation interface. This especially affects small devices, as the perimeter/area ratio is much larger than for large devices. A post-metallization anneal in nitrogen at 400°C was found to reduce the dark current of small devices (10 x 10 μm) by $\sim$1000X at -1 V. The same anneal reduces the dark current of larger devices (100 x 100 μm) by $\sim$140X. Through metal-oxide-semiconductor capacitor and doping studies, it was found that the anneal draws holes to the surface of the germanium, leading to better isolation of the devices and reduced leakage current.

It was also found that threading defects play a role in leakage current. Threading defects arise because of the 4% lattice mismatch between germanium and the underlying silicon. For 1 μm-thick germanium films, as-grown samples are expected to have $\sim$5 x 10^8 cm^{-2} threading defects. At this level, these defects are the dominant leakage current mechanism. Annealing the films at high temperatures can reduce the defect density.

Large-area (300 x 300 μm) devices fabricated with a post-metallization anneal and with a threading defect density of $\sim$2 x 10^7 cm^{-2} were found to have a dark current density of $\sim$1 mA/cm^2 and a responsivity of 0.32 A/W at -1 V and 1550 nm.

Thesis Supervisor: Judy L. Hoyt
Title: Professor

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Chapter 1

Introduction

As electronic systems reach their physical limits, new system architectures will be needed to continue technological progress. Integrated electronic-photonic systems are emerging as a potential solution to overcome the scaling limits of electronics. By moving certain functions from the electrical realm to the photonic realm, systems can save energy, operate faster, and exploit parallelism to a larger degree.

Due to the relative expense of materials traditionally used in optics compared to those in complementary metal-oxide-semiconductor (CMOS) systems, a large research effort is underway to integrate photonic components on a silicon chip [1] [2]. Germanium has an indirect bandgap at 0.66 eV, but it has a direct bandgap that is only slightly larger. Due to this small direct bandgap of 0.80 eV, germanium is an attractive candidate for use in optically absorbing devices and optically emitting devices. Researchers have recently found a way to fabricate a germanium laser [3] and germanium has also been used as an electro-optic modulator [4] [5]. Furthermore, SiGe alloys are already being used in CMOS systems [6], making integration of pure germanium an attractive possibility.

Photodiodes, or diodes that generate current when illuminated, are often used in integrated electronic-photonic systems either as an interconnect between the electron-

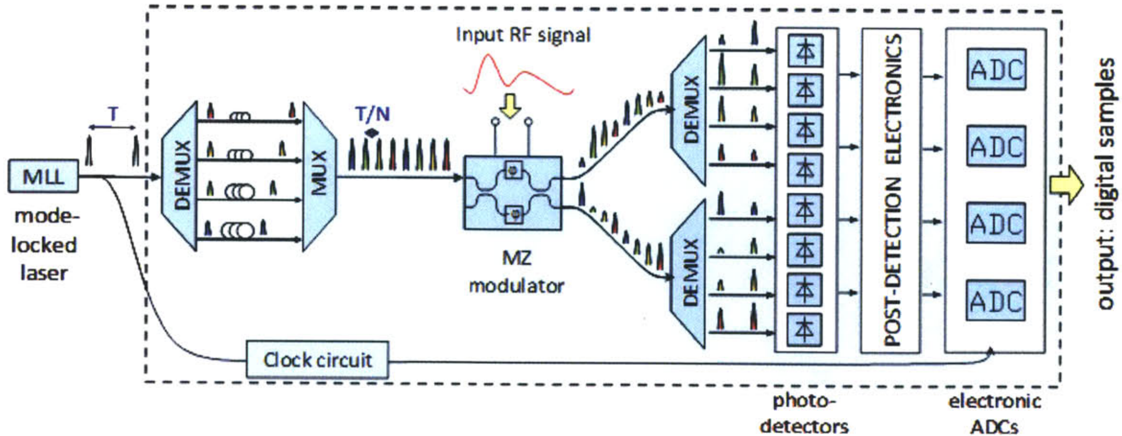

Figure 1-1: A schematic diagram of the electronic-photonic analog to digital converter in this study. Everything inside the dotted box can be integrated on a single silicon substrate. From [7].

ics and the photonics or as an infrared sensor. This thesis focuses on the fabrication, characterization, and modeling of Ge-on-Si photodiodes made for two applications. In the first application, the germanium photodiode will be used as a photodetector in an integrated electronic-photonic analog-to-digital converter (ADC). In this application, the sampling source of the ADC is switched from an electronic source to an optical source [7]. This change has the potential to reduce the timing jitter in the system by 100X. If, however, this substitution is made, a new family of silicon-compatible photonic devices is needed to complete the ADC. Silicon electro-optic modulators are needed to sample the outside signal, silicon-compatible waveguides are needed to transmit the signal across the chip, ring filters with microheaters are needed to select the signal, and, finally, photodetectors are needed to convert the signal back into an electronic signal at the end. A schematic diagram of such a system is illustrated in Figure 1-1 and an optical micrograph of a partial system is in Figure 1-2.

The second application for germanium photodiodes in this thesis is as infrared sensors for imaging applications. In this case, the goal is to integrate the sensor and the read-out circuitry on a Si substrate [8]. Currently, to absorb wavelengths in the

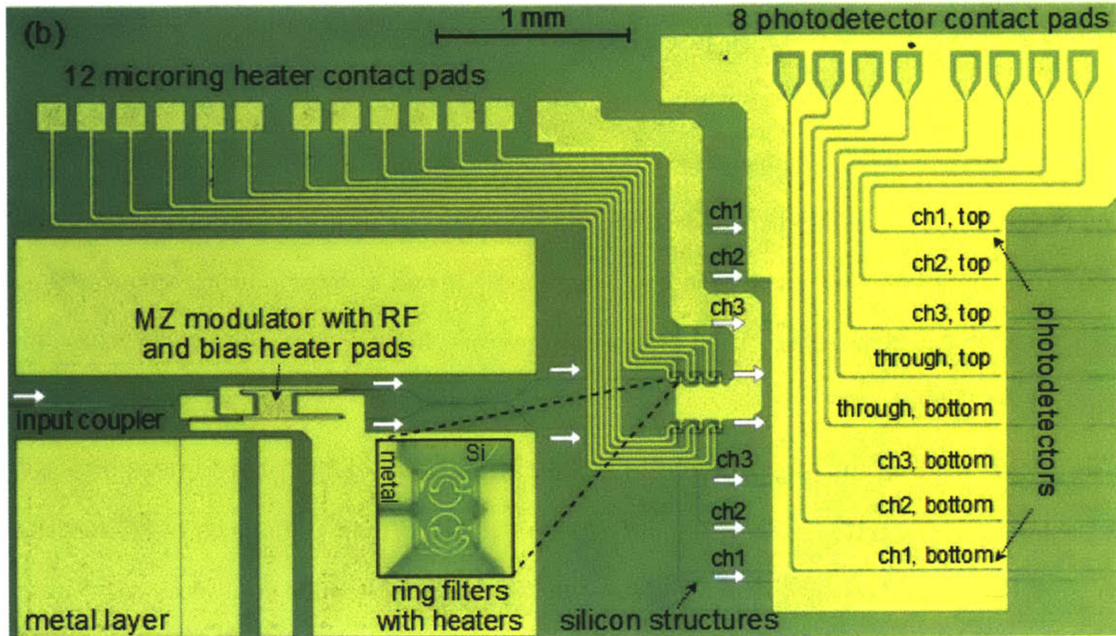

Figure 1-2: An optical micrograph of part of the integrated electronic-photonic ADC. The image shows Mach-Zender Si modulators, ring filters with micro-heaters, and photodetectors. From [7].

visible to near infrared, these systems are made using InGaAs for the detector and InP for the substrate [9]. While the detectors display excellent noise characteristics, the materials set is expensive. Switching to a silicon substrate has the potential to reduce the cost of the system. However, if silicon is used as the substrate, a new material would be needed for the detector, as InGaAs is very difficult to integrate on silicon. Germanium is a promising candidate for these new detectors because of its similar absorption spectrum to InGaAs and its relative ease of integration on silicon.

1.1 Importance of the diode dark current

The leakage current of photodiodes in the dark is known as the "dark current" of the device. In both applications discussed above, achieving a low dark current is of paramount importance. In the analog-to-digital converter, the system can tolerate a certain level of dark current (usually quoted as $\sim$1 μA), because the subsequent

amplifier also introduces noise into the system. A dark current higher than $\sim$1 μA will reduce the signal-to-noise ratio of the ADC and potentially introduce errors in the system. Furthermore, because the photodiodes are normally operated in reverse bias, any leakage current will contribute to standby power consumption. Reducing the dark current of the photodiodes can lead to a higher SNR and a lower power consumption. Furthermore, one can relax other design parameters, like the germanium thickness or size of the device.

For the infrared imaging application, the dark current of the photodiodes directly impacts the sensitivity of the system. State-of-the-art InGaAs devices have demonstrated 18 nA/cm^2 dark current at -1 V at 273 K [9]. To fully compete with these diodes and not lose resolution of the signal, the dark current of germanium devices must be comparable.

This thesis will mainly focus on the mechanisms of dark current in Ge-on-Si photodiodes and methods to reduce it. It is found that the material quality and surface conditions of the germanium contribute greatly to the dark current. Optimizing these characteristics is key to fabricating germanium photodiodes on silicon substrates with low leakage current.

1.2 Basic structure of Ge-on-Si photodiodes

There are many variations of Ge-on-Si photodiodes, but they all share some basic characteristics. Germanium is grown on a silicon substrate, usually without the benefit of any interfacial buffer layer. The junction may be laterally oriented or vertically oriented, but it is always a *pin* junction. The dopants may be either grown *in-situ* or ion implanted after germanium growth. The dark current of the device is the leakage current of this *pin* diode in the dark.

To measure an optical response, the device can either be vertically illuminated or

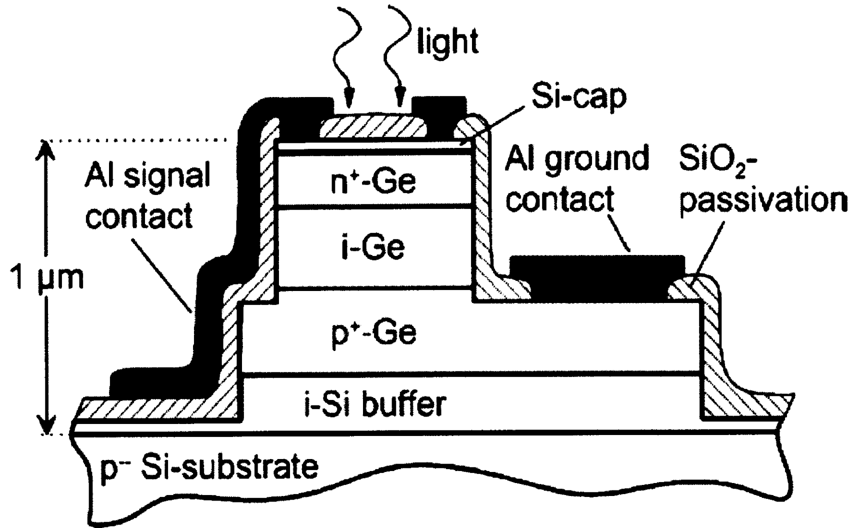

Figure 1-3: A cross-sectional schematic diagram of a typical Ge-on-Si diode. This diode is fabricated from Ge grown on a thin *i*-Si buffer and is a vertical *pin* junction. From [10].

edge coupled. Optical absorbtion occurs mainly in the intrinsic region of the device, where a high electric field exists. The high electric field moves the carriers out of the intrinsic region and to the contacts where they are collected. An example of a typical Ge-on-Si diode can be found in Figure 1-3.

1.3 Roadmap of this thesis

This thesis primarily discusses the effect of material quality and surface passivation on the dark current of Ge-on-Si photodiodes. Chapter 2 gives a brief overview of photodiode operation and previous work done in this field. Chapter 3 discusses the results from diodes fabricated from selectively-grown Ge-on-Si. It primarily looks at the effect of material quality on dark current density and photoresponse. Chapter 4 discusses results from diodes fabricated from blanket Ge-on-Si films. This chapter is primarily concerned with the effects of surface passivation on the dark current. Chapter 5 discusses the physics and modeling of the blanket Ge-on-Si photodiodes.

A model for these devices is developed and experiments were conducted to prove the model. Chapter 6 summarizes the thesis and suggests future work.

Chapter 2

Thesis Background

This chapter discusses the operation of germanium diodes and gives an overview of previous research done on these devices. It will first discuss the operation and basic physics of photodiodes and then it will discuss the advantages and disadvantages of using germanium for photodiode applications. The chapter will then discuss previous work in the field to improve the germanium material quality. Finally, the chapter concludes with a discussion of state-of-the-art Ge-on-Si devices.

2.1 Physics of photodiodes

Semiconductor photodiodes are generally fabricated from standard pn-junctions or pin-junctions, schematics of which can be seen in Figure 2-1. Upon illumination with an energy greater than or equal to the bandgap of the material, electron-hole pairs are generated resulting in current flow.

In an ideal diode, only those minority carriers generated within a diffusion length of the depletion region contribute to the current. These carriers reach the depletion region, are swept across by the high electric field, and reach the other side. Minority carriers generated beyond a diffusion length from the depletion region recombine

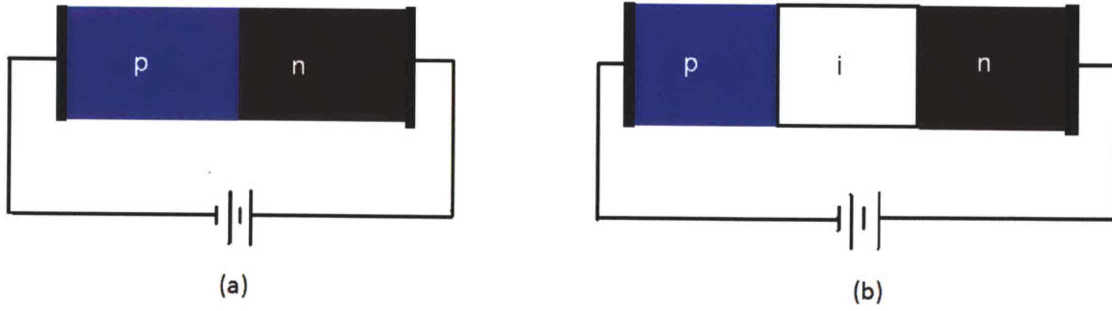

Figure 2-1: Schematic illustrations of (a) a *pn* junction diode and (b) a *pin* junction diode. Carriers generated in the depletion regions will be collected as photo current.

before they reach the high field region. In the *pn*-junction diode case, the total current in the device can be expressed as [11]:

$$I = I_0(exp(\frac{qV}{kT}) - 1) - qAG_0(L_p + L_n) \tag{2.1}$$

where the first term is the diode dark current and the second term is the current due to the light. In the above equation, q is the charge of an electron, I_0 is the reverse saturation current, k is Boltzmann's constant, T is the temperature, A is the cross-sectional area, G_0 is the optical carrier generation rate in steady state (assumed to be constant), L_p is the diffusion length for holes, and L_n is the diffusion length for electrons.

The responsivity of a photodiode is defined as

$$R = \frac{I_{photo}}{P_{optical}} \tag{2.2}$$

where I_{photo} is the photogenerated current and $P_{optical}$ is the input optical power. As indicated by the above expressions, the responsivity of a *pn*-junction diode is limited by the diffusion lengths of the carriers. Inserting an intrinsic layer to create a *pin*-junction diode is a common method used to increase responsivity. In a properly designed *pin* diode, the entire intrinsic region is depleted. Any carriers generated in the intrinsic (depleted) region or within a diffusion length on either side will be

swept across the junction and collected on the opposite side, assuming negligible recombination of photogenerated carriers in the depletion region itself. Germanium's absorption depth at 1550 nm is on the order of 1 μm [12], so the intrinsic layer in *pin*-photodiodes is usually ~1 μm wide in order to provide ample space in which to generate carriers. It should be noted that in the case of relatively high minority carrier lifetimes (10^{-6} - 10^{-3} s) and moderately high doping concentrations (10^{18} cm^{-3}), the diffusion length of minority carriers will be on the order of 1 μm, indicating that significant photocurrent will originate in the quasineutral regions. As discussed in later sections, the germanium in this work is defected due to threading dislocations that originate during growth. These dislocations may have a deleterious effect on lifetime, reducing the diffusion length of minority carriers in this thesis.

2.2 Optical properties of germanium

Germanium is an excellent candidate for use in *pin* photodiodes that absorb over the visible to near infrared part of the electromagnetic spectrum. While technically germanium is an indirect bandgap material (E_g = 0.66 eV), it also has a direct bandgap that is only slightly larger (0.80 eV). The bandstructure of Ge can be seen in Figure 2-2

Due to this direct bandgap, Ge absorbs strongly out to ~1.55 μm (~0.80 eV). An absorption curve of Ge compared to other materials can be seen in Figure 2-3. In the near infrared, germanium's main competitors are InGaAs and other III-V materials that are generally more expensive and harder to integrate onto Si.

It should be noted that some III-V materials, like InGaAs, have a smaller bandgap than Ge, allowing them to absorb light at longer wavelengths. This is an important difference especially in infrared sensor applications and methods to increase the spectrum over which germanium absorbs will be discussed later in section 2.4.2.

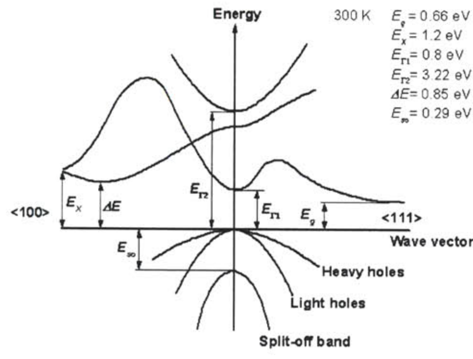

Figure 2-2: The band structure of Ge at 300K. The indirect bandgap of 0.66 eV is at the L point while the direct bandgap of 0.8 eV is at the Γ point. From [13].

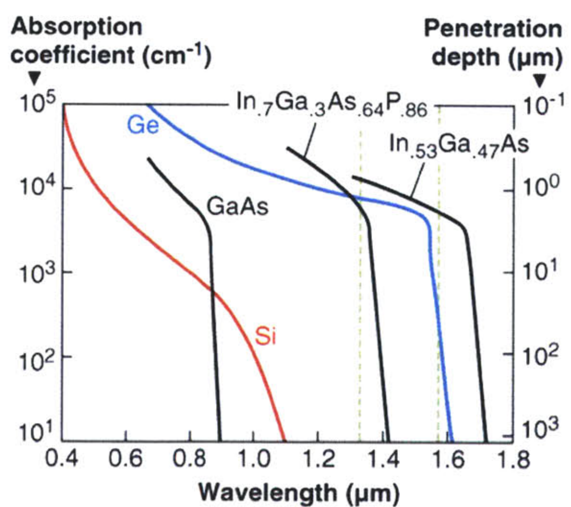

Figure 2-3: Absorption coefficient versus wavelength for a number of different semiconductors. Ge absorbs strongly out to ~1550 nm, making it a strong candidate to compete with materials like InGaAs and InGaAsP. From [12].

2.3 Integration of germanium on silicon

Germanium and SiGe integration on Si has long been studied for metal-oxide-semiconductor field effect transistors (MOSFETs) [14] [15] [16] and heterojunction bipolar transistors (HBT) [17] [18]. SiGe alloys are currently used in state-of-the-art pMOSFETs in the source/drain regions. Since SiGe has a larger lattice constant than Si, when SiGe is grown in these regions, it exerts strain on the channel. The strain in the channel can improve device performance [6]. Furthermore, with its improved mobility over Si, Ge is an attractive candidate for use as a channel material in MOSFETs. Ge MOSFETs, or even strained Ge MOSFETs, are an active area of research which has been producing promising results [19].

Regardless of application, germanium is too expensive to be used as a substrate. A four inch germanium wafer can cost up to a few thousand dollars while a six inch silicon wafer is only ~$10. For the final product to be cost effective, the germanium must be integrated on a silicon substrate. Integration of Ge on Si substrates is not without its challenges. Due to the 4% lattice mismatch between Ge and Si, when Ge is grown directly on a silicon substrate, it starts to form misfit/threading defects quickly. The critical thickess, or the thickness of film that can be deposited before defects start to form, of Ge on Si is ~2 nm [20], although researchers are looking at ways to increase it [21]. For a MOSFET application, a few nanometers of germanium may be all that is needed. For a photodiode, however, much thicker Ge is needed to absorb light. Depositing 1 - 2 μm of germanium directly on silicon results in films with 10^8 - 10^9 defects per square centimeter.

Researchers have been studying ways in which to reduce the threading defects in thick (1 - 2 μm) Ge films grown on silicon substrates. One possibility is to grow the Ge on a relaxed graded buffer layer. In this method, prior to growing pure Ge, a SiGe alloy is grown, which gradually increases the concentration of germanium. The goal is to confine all of the threading defects to this buffer layer, leaving the top layer of

Ge with virtually no defects. Fitzgerald, *et al.* have done this and achieved a defect density of 2 x 10^6 cm^{-2} [22].

The difficulty with growing a SiGe buffer layer is that it takes both time and resources. The buffer layer is usually 5 - 7 μm, while the top Ge layer is often only 1 - 2 μm. This thick buffer layer is needed to fully relax the Si_xGe_{1-x} alloy and effectively "trap" the threading dislocations in the buffer layer. Thus, much of the growth time is actually spent growing the buffer layer and not the Ge. Furthermore, some applications are not compatible with photodiodes grown on a thick buffer layer. An alternative is to grow the Ge on a one-step buffer, *i.e.* grow a thin layer of $Si_{0.8}Ge_{0.2}$ [23].

Another possibility for reducing the threading defect density is to anneal the wafer after growth. This is usually done in a cyclic fashion by alternating between a high temperature (~800°C) and a low temperature (~400°C) multiple times. By annealing the film, the defects move, annihilating one another or making their way to the edge of the wafer. Cyclic annealing has been studied in great detail and it was found that it is possible to reduce the defect density by ~10X [24] [25].

Finally, the defect density can be reduced by growing the germanium selectively in small areas. In this case, oxide is first deposited on a silicon wafer and patterned into holes. Growing Ge selectively in the holes benefits the quality of the Ge film in two ways. First, defects generated on one area of the wafer cannot propagate to another area of the wafer because the oxide is in the way. This is called the small area effect and is illustrated schematically in Figure 2-4.

Furthermore, when defects do form at the Ge/Si interface, they generally propagate towards the Ge surface at an angle (rather than straight up). If the height of the oxide is tall enough, the defect will be annihilated when it reaches the oxide sidewall and it will never reach the top of the film. This is called aspect ratio trapping [27] and is illustrated in Figure 2.3. By combining both selective growth and annealing,

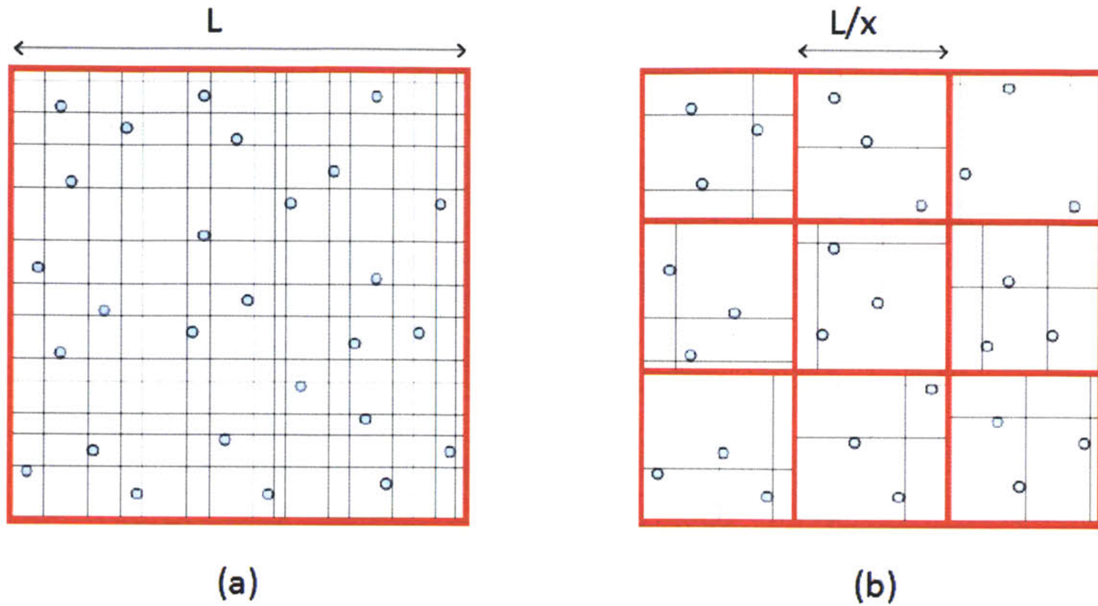

Figure 2-4: A schematic illustration of how dislocations propagate in (a) a large area and (b) a small area. In a large area, the defects can propagate a long way, potentially impacting a large portion of the film. In a small area, defects from one square cannot propagate into a neighboring square, thus reducing the defect density. From [26].

researchers have achieved very high quality germanium grown directly on silicon [25]. Figure 2-6 shows Nomarski micrographs of 10 x 10 μm Ge islands after a 10 minute anneal and after a cyclic anneal. After a 10 cycle anneal, the film had 2.3 x 10^6 cm^2 defects. While still somewhat high, this value is $\sim$10X lower than similarly annealed blanket films. Furthermore, some Ge islands were defect free after the anneal.

2.3.1 Germanium growth

Germanium can be grown on silicon substrates in a number of different ways. Researchers have used molecular beam epitaxy (MBE) [29] [10], ultrahigh vacuum chemical vapor deposition (UHVCVD) [30] [31], reduced pressure chemical vapor depostion (RPCVD) [32] [33], and low energy plasma enhance chemical vapor deposition (LEPECVD) [34].

Regardless of the growth system, most germanium is grown using a two-step

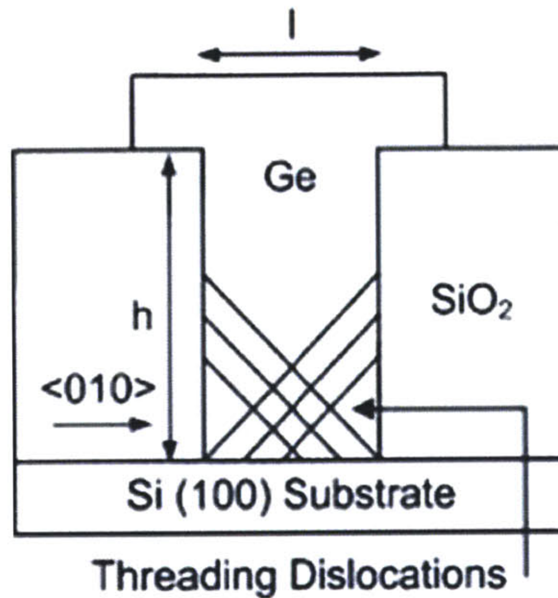

Figure 2-5: A schematic illustration of aspect ratio trapping. The defects terminate at the oxide sidewalls leaving the top of the film virtually defect free. For materials with crystal orientations like the one in the figure, the angle that the defects form with the substrate is 45°. This is because the threading dislocations will propagate in the ⟨110⟩ direction on the (111) plane. From [28].

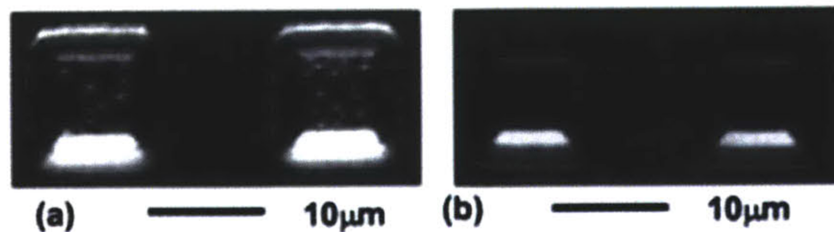

Figure 2-6: Nomarski micrographs of 10 x 10 *mu*m Ge islands grown selectively. The dimples in the Ge film were caused by an iodine etch as a way to highlight the defects. (a) With a 900°C anneal for 10 minutes, the defect density was 4.3 x 10^7 cm^2. (b) After a 10X anneal between 900°C and 100°C, the defect density was 2.3 x 10^6 cm^2. From [25].

growth process. The first step is generally done at low temperature (300°C - 400°C). The low temperature is necessary to create a smooth germanium film and to suppress islanding. After this seed layer is deposited, the temperature is increased to the range of 600°C to 750°C. This high temperature promotes faster germanium deposition while maintaining a smooth film. Finally, there is sometimes a post-growth anneal in a hydrogen ambient to reduce the threading defects.

2.4 Ge-on-Si diodes

2.4.1 Figures of merit for photodiodes

There are three typical figures of merit for photodiodes. Their relative importance differs in different applications. The first is dark current. Dark current is simply the leakage current when the diodes are in the dark. A low dark current is important to keep the signal-to-noise (SNR) ratio high. A low dark current is of the utmost importance for infrared imaging applications because it is the dominant noise in the system. For high-speed applications, low dark current is not the most important characteristic, but by reducing the dark current, standby power consumption and other design paramters can be relaxed. The dark current, and factors that affect it, will be discussed in detail in Chapter 5. Comparing the dark current of different devices is not always straightforward. Some groups only quote the dark current density of the devices. However, this can be misleading because the dark current does not always scale with the area of the device. This thesis attempts to quote both the absolute dark current and the size of devices fabricated by other groups. However, sometimes this data is not available and the dark current density is quoted instead.

The second figure of merit is the photoresponse, or responsivity, of the devices. This is a measure of how well the diode absorbs light, converts it to electron-hole pairs, and extracts the generated carriers from the device. Having a high responsivity is

also important for a high SNR.

The final figure of merit is the frequency response of the devices. It is important for these devices to switch on and off rapidly, especially for high-speed applications like the analog-to-digital converter mentioned in Chapter 1. For imaging applications, the frequency response of the device is not very important and is often ignored. The frequency response is often limited by one of two things. It can be limited by the RC time constant of the overall device or it can be limited by the transit time of the carriers across the device. If the frequency response is dominated by the transit time, it is important to keep the intrinsic region narrow so that the carriers have a short distance to travel. However, making this region narrow can mean that there is not as much material for absorbing light, resulting in lower SNR ratios. For this reason, it is important for high speed devices to still have a low dark current.

2.4.2 Previous work on blanket diodes

As mentioned earlier, the simplest way to fabricate a Ge-on-Si photodiode is to grow Ge directly on Si without a graded buffer layer. When the germanium is grown across the entire wafer, it is referred to as a "blanket film." Depending on the application, germanium is grown using different growth tools. Using MBE allows tight control over doping profiles, resulting in high internal electric fields. Oehme, *et al.* have used MBE to fabricate a Ge-on-Si diode with a 39 GHz bandwidth at -2 V. At -1 V, the dark current of a 5 μm radius circular device was 75 nA (95 mA/cm^2) [35].

Germanium is also often grown using ultra-high vacuum chemical vapor deposition (UHV-CVD). Colace, *et al.* achieved dark current densities of $\sim$250 mA/cm^2 (16 muA for an 80 x 80 μm device) and a bandwidth of 10 Gbit/s. Furthermore, the responsivity of their devices at 1550 nm was 0.2 A/W [31]. Liu *et al.* achieved dark current densities of 10 mA/cm^2 while increasing the responsivity to 0.52 A/W [36].

More recently, reduced-pressure chemical vapor deposition (RPCVD) has been

used as a cost-effective substitute for MBE or UHVCVD to grow germaium films. Osmond *et al.* have reported a 10 μm device in diameter with a dark current of 225 nA ($\sim$300 mA/cm^2) at -1 V. Furthermore, these devices had a responsivity of 0.21 A/W at 1500 nm and a frequency response of 49 GHz when biased at -5 V [37].

Kim, *et al.* have used RPCVD to fabricate devices that operate at 36 GHz at -1 V [33]. These devices used germanium that was 1.2 μm thick. Devices with 1.7 μm of Ge that had a diameter of 17 μm displayed dark current of 42 nA, or 19 mA/cm^2. Thicker devices had a frequency response of 13 GHz at -1 V and a responsivity of 0.74 A/W at 1550 nm.

Finally, a new growth method called low-energy plasma-enhanced chemical vapor deposition (LEPECVD) had been used to deposit germanium films. Comparable levels of threading defects to UHVCVD and MBE growth were reported with anneals ($\sim$2 x 10^7 cm^{-2}). When fabricating large area devices (radius $\sim$1 mm), they report dark current densities as low as 1 μA/cm^2 [34].

When comparing leakage current densities of diodes fabricated Ge-on-Si films, it is often useful to compare them to leakage current densities on bulk Ge wafers. Ge-on-Si films will have some number of threading defects (10^6 cm^2 or more), but a bulk Ge wafer should be virtually defect free. Diodes fabricated on bulk Ge wafers are most often *pn* structures rather than *pin* because they are used to study source/drain regions of Ge MOSFETs. This different structure makes a direct comparison difficult; however, work has been done to minimize damage due to ion implantation and reduce surface effects.

Takagi, *et al.* used a process known as gas phase doping to eliminate ion implantation entirely. After annealing at 500°C - 600°C, they achieved an *n*-type activation of $\sim$10^{19} cm^{-3}. Diodes fabricated from these junctions displayed leakage current densities of $\sim$1 mA/cm^2 at -1 V [38]. Furthermore, Woo, *et al.* did a study on implantation energy, dose, and annealing conditions to minimize the leakage current. They found

that the most important aspect of junction design was keeping the junction as far from the surface as possible. In their study, a high implant energy (100 KeV) produced devices with the lowest leakage current density, despite the larger amount of damage caused by the implant. At -1 V, these devices had a leakage current density of $\sim$0.1 mA/cm^2. They also found that it was possible to modify the activation anneal conditions to repair the crystal damage done by the implantation [39].

In addition to focusing on the dark current, responsivity, and frequency response of devices, some groups have been investigating ways to extend the wavelength range over which germanium absorbs. To do this, they add strain to the device which shrinks the bandgap and allows germanium to absorb at longer wavelengths.

After growth at high temperature, there is residual strain in the Ge films. This strain is not due to the lattice mismatch as in thinner films, but rather due to the difference in thermal expansion coefficients. As the germanium and silicon layers cool to room temperature, they contract at different rates. This leaves a residual tensile strain in the film. This was first documented by Kimerling, *et al.* [40]. A plot of germanium's absorption coefficient versus energy can be seen in Figure 2-7. For germanium grown on silicon, the direct bandgap shrinks from 0.80 eV to 0.77 eV.

Other groups have tried to add additional strain to the germanium. Liu *et al.* added a backside silicide to the wafer after processing. The silicide induced a slight bowing in the wafer, increasing the tensile strain in the Ge from 0.20% to 0.25% [36].

Saraswat, *et al.* characterized germanium photodetectors when applying external strain using a four point bending setup. They found that the photoresponse at 1550 nm increased from 0.67 A/W to 0.75 A/W with 113 MPa of tensile stress and decreased from 0.67 A/W to 0.48 A/W with 177 MPa of compressive stress [41]. This is consistent with the theoretical calculations on the deformanation potentials reported in [42].

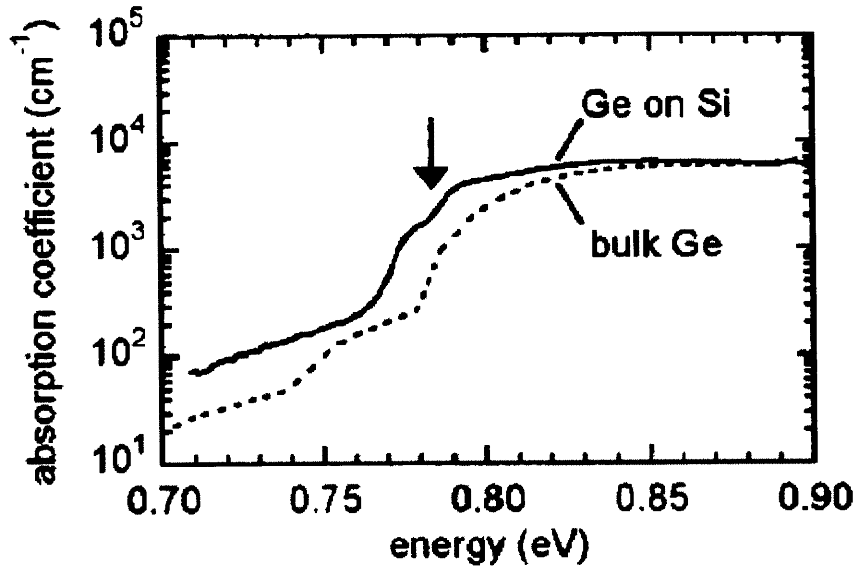

Figure 2-7: Plot of absorption coefficient versus energy for bulk Ge and Ge-on-Si. The difference in thermal expansion coefficients between Ge and Si leaves a residual tensile strain in the Ge after high temperature growth. The result is that Ge-on-Si will absorb light of lower energy than bulk Ge. From [40].

2.4.3 Previous work on selective diodes

As mentioned earlier, one way to reduce the threading defects in germanium films grown on silicon substrates is to grow them selectively. As shown by Kimerling *et al.*, the threading defect density has a direct impact on the dark current of $Si_{0.75}Ge_{0.25}$ diodes grown on buffers of different grades [43]. By growing germanium selectively, it is possible to reduce the defect density and improve the dark current density. Yu, *et al.* reported on selectively-grown films with a defect density of 1 x 10^7 cm^2. Large diodes (150 μm radius) fabricated from this germanium displayed a dark current of ~6 μA (dark current density of ~8 mA/cm^2) at -1 V. The responsivity of these devices was 0.64 A/W at -1 V and 1550 nm [44].

Aberg, *et al.* have devised a new way to grow germanium selectively. Rather than patterning somewhat large (~10 μm) oxide holes, they pattern a very small (~100 nm) window with a high aspect ratio. Germanium is grown in this seed region to a height of ~1 μm. Over that space, nearly all of the dislocations terminate at the

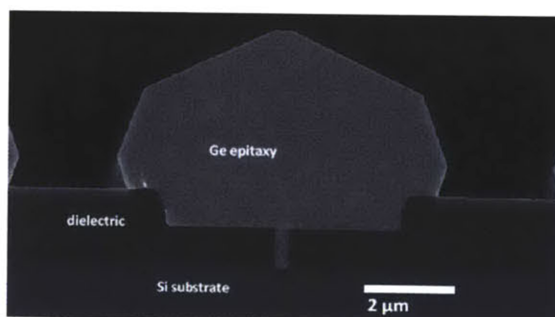

Figure 2-8: A cross-sectional SEM of selectively-grown Ge on Si utilizing a high aspect ratio seed region. Nearly all of the defects terminate before they reach the higher region where the device is located. From [45].

oxide sidewalls. Then the window widens to ~5 μm, which is a large enough area to fabricate an infrared imager [45]. A cross-sectional scanning electron micrograph (SEM) can be seen in Figure 2-8.

At room temperature, devices fabricated from these germanium films demonstrated ~30 pA of dark current at -1 V. For a device size of 10 x 10 μm, this corresponds to a dark current density of ~30 $\mu A/cm^2$.

Loh, *et al.* have been fabricating germanium photodiodes from selectively grown UHVCVD. In an experiment where they included a thin $Si_{0.8}Ge_{0.2}$ buffer layer, they achieved dark current densities on the order of ~20 mA/cm^2 (~170 nA for a 25 x 25 μm square). Furthermore, leakage current analysis indicated that the bulk dark current density is ~2 mA/cm^2. These devices also displayed a 3 dB frequency of 15 GHz at -1 V [46]. The same group has also investigated adding strain to these selective devices by growing the germanium on different buffer layers. They report an increase in photoresponse from 0.1 to 0.2 A/W at 1520 nm and -1 V [23].

A summary table of the dark current and dark current densities for devices fabricated from blanket and selective Ge-on-Si can be found in Table 2.1. The values of the dark current density varies widely from 1 $\mu A/cm^2$ to 300 mA/cm^2 and could be due to a number of parameters. Some groups were more interested in fabricating a

device that operated at high speed and, thus, did not investigate the sources of leakage current very much. The dark current is somewhat dependent on the threading defects in the germanium film. The concentration of threading defects is due to a number of processing conditions such as the anneal conditions, the thickness of the germanium, and whether or not the germanium was grown on a buffer layer. Unfortunately, very few of the references quantify the dislocation density in their germanium films. Finally, as will be discussed in Chapter 5, the dark current is also dependent on the doping profiles in the device. There will be variations in the doping profile due to the implant conditions, the activation anneal thermal budget, and the growth method used. This background is meant to be an overview of the field. Mechanisms responsible for the dark current will be discussed in Chapter 5.

Table 2.1: Summary of previous work on dark current

Author and reference	Size of device	Dark current at -1 V (nA)	Dark current density at -1 V (mA/cm^2)
Oehme [35]	5 μm radius	75	95
Colace [31]	80 x 80 μm	16000	250
Liu [36]			10
Osmond [37]	5 μm radius	225	300
Kim [33]	8.5 μm radius	42	19
Osmond [34]			0.001
Yu [44]	150 mum radius	6000	8
Aberg [45]	10 x 10 μm	0.03	0.03
Loh [46]	25 x 25 μm	170	20

2.4.4 Waveguide integrated Ge diodes

To move towards full integration of a germanium detector in an integrated photonic system, many groups have fabricated Ge diodes and Si waveguides on a single chip. In these systems, germanium detectors can either be butt-coupled or evanescently coupled to the silicon waveguide. The layouts of each are illustrated in Figure 2-9. In addition to variation of coupling schemes, the devices may either be oriented with

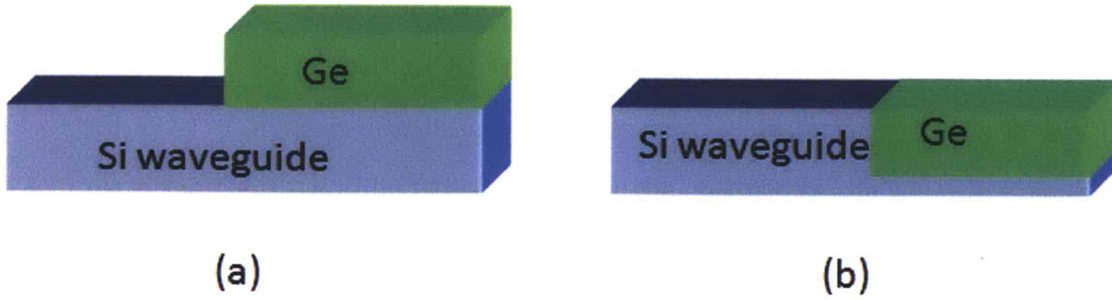

Figure 2-9: Schematic diagrams of two types of waveguide integrated detectors. (a) An evanescently coupled Ge detector grown on top of a Si waveguide. (b) A butt coupled detector grown where Si has been etched away.

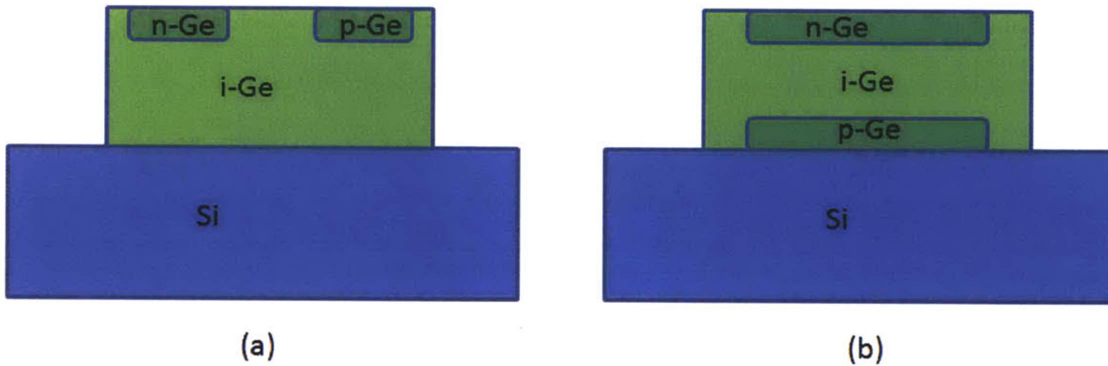

Figure 2-10: A schematic illustration of (a) a lateral *pin* structure and (b) a vertical *pin* structure. Each offers its own benefits and integration challenges.

a vertical *pin* structure or a lateral one. This difference is illustrated in Figure 2-10 and the implications will be discussed later in the section.

Feng, *et al.* and Vivien, *et al.* have both fabricated butt-coupled Ge detectors with silicon waveguides [47] [48]. They achieved 3 dB frequencies of 32 GHz and 42 GHz, respectively, and report responsivities of ≥ 1 A/W. The devices in Feng had a much higher dark current density of $\sim$16 A/cm^2 while Vivien achieved 60 mA/cm^2. The dark current density in [48] was given explicitly in the paper and the dark current density of [47] was calculated from the absolute dark current and active area of the device, both of which were given explicitly in the paper.

Yin, *et al.* [49] and Feng, *et al.* [50] have both fabricated vertical *pin* junctions

that are evanescently coupled to a Si waveguide. The dark current densities were comparable (60 mA/cm^2 and 30 mA/cm^2 respectively), but the devices in [50] displayed a 3 dB frequency of 12 GHz while [49] operated at 29.4 GHz. Neither group is forthcoming with their growth system or details, so it is difficult to say whether these differences are due to the quality of the Ge or the device architecture itself.

Wang, *et al.* have fabricated a similar device, except the junction was a lateral *pin* structure evanescently coupled to a Si waveguide. They report a 3 dB frequency of 18 GHz and an absolute dark current as low as 15 nA at -1 V [51]. Wang also compared both laterial *pin* and vertical *pin* structures which were evanescently coupled on a silicon waveguide. They found that the vertical diode had a higher bandwidth (5.5 GHz compared to 3.4 GHz) but a lower responsivity (0.29 A/W compared to 1.16 A/W). They attributed the lower responsivity of the vertical device to a smaller optical mode overlap due to the highly doped Ge region at the diode/waveguide interface [52].

From a statistical perspective, Kopp, *et al.* achieved a yield of 99% for germanium detectors integrated in a CMOS-compatible process flow on a 200 mm wafer, thus demonstrating the overall feasibility of germanium diodes integrated in a CMOS process. They achieved a dark current density of 7 mA/cm^2 and a median bandwidth of 9 GHz over 1100 photodiodes [53].

2.4.5 Other types of Ge-on-Si diodes

There are also other forms of Ge-on-Si diodes that have been fabricated. Metal-semiconductor-metal structures have high dark current but can operate at high speeds (25 GHz) [54]. Diodes have also been fabricated from superlattice structures [55] and from avalanche structures [56]. Futhermore, the germanium film is not always grown using some sort of chemical vapor deposition or epitaxy. Waveguide integrated Ge detectors have been fabricated by rapid melt growth of the Ge [57], by bonding of a Ge

wafer to a Si wafer [58], and by depositing poly-crystalline Ge by thermal evaporation [59].

2.5 Scope of this thesis and chapter summary

Previous work has focused primarily on germanium integration on silicon substrates and on fabricating devices with a high 3 dB frequency. This thesis focuses on reducing the leakage current in small devices. When device dimensions are on the order of $\sim$100 μm, perimeter or surface effects on the dark current are dwarfed by the leakage current of the active area. However, when devices are scaled down, the dark current does not usually scale proportional to the area. By understanding the physics of the dark current, it may be possible to make devices that are small ($\sim$10 μm) with low leakage current.

This chapter outlined the operation of germanium photodiodes and discussed methods which have been used to integrate Ge photodiodes on silicon substrates. It discussed three ways of reducing the threading defects that arise from the lattice mismatch: growing germanium on a SiGe buffer, using a high temperature anneal after growth, or growing germanium in small areas. It then discussed previous work on germanium photodiodes fabricated from blanket films and from selective films and it also discussed how tensile strain affects the photoresponse of devices. The dark current and dark current density of previous devices varies widely and its origin is not well understood. This thesis attempts to study and explain the dark current mechanisms in small Ge-on-Si photodiodes. Finally, this chapter discussed waveguide-integrated device architectures and results. Full integration of these diodes in an electronic-photonic system is a major goal of the field and this thesis will discuss attempts at MIT to integrate a germanium photodiode with a silicon waveguide.

Chapter 3

Photodiodes fabricated using selectively grown germanium

This chapter discusses the fabrication and characterization of photodiodes made from selectively-grown germanium. There are numerous benefits from using selectively-grown germanium. It enables integration with larger and more complex electronic-photonic systems and increases the germanium growth rate. Furthermore, there is also the possibility to grow germanium films with fewer defects as compared to a blanket film. In this thesis, we pursue the integration of a germanium photodiode into an electronic-photonic analog-to-digital converter.

This chapter first describes the growth of germanium on silicon wafers in oxide holes. Next, it outlines the fabrication of diodes made from these films. It then describes the electrical and optical characteristics of stand-alone test devices. Finally, it describes the fabrication and characterization of diodes integrated on top of a silicon waveguide.

3.1 Selective germanium growth

Growing germanium selectively in oxide windows presents a series of challenges that are different from blanket Ge growth. Optimum growth parameters must be found so that the germanium fills the oxide windows completely and uniformly. Furthermore, different planes of atoms grow at different rates, which leads to faceting. Care must be taken to reduce faceting on the germanium surface. Finally, and most importantly, the surface of the Si wafer must be extremely clean. A contaminated surface will cause the germanium film to have many threading dislocations or even be polycrystalline instead of single crystalline, resulting in fabrication difficulties and poor device performance.

3.1.1 Surface preparation

For blanket germanium growth a virgin wafer is typically cleaned and then placed into an epitaxial reactor for the growth itself. The wafer sees very minimal processing prior to growth (typically only a wet chemical clean) and a high temperature (~1080°C) pre-bake is used to drive off any contaminants from the surface. This results in a very clean Si surface and a high quality Ge film. For selective growth, however, the wafer must go through more processing prior to growth, potentially leaving the surface contaminated.

For this work, the wafers were first cleaned using a standard RCA clean [60]. Then 1 - 2 μm of a PE-CVD oxide was deposited. The oxide was patterned with photolithography and then etched using a C_4F_8:CH_2F_2 1:1 plasma. This dry etch was intended to produce vertical sidewalls. The photoresist was then stripped using an oxygen plasma and the wafers received a double piranha clean. Finally, the wafers received an RCA clean with two short HF dips to remove any oxide in the windows while minimizing oxide loss in the field. Immediately before growth, the wafers received a 5 minute pre-bake in the growth chamber at 900°C to drive off any remaining

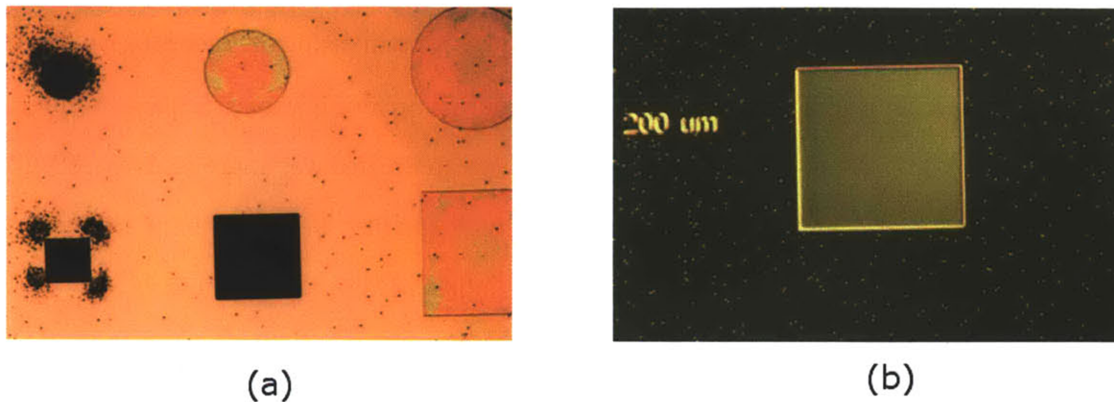

Figure 3-1: Nomarski micrographs polycrystalline Ge and single crystalline Ge. (a) A contaminated Si surface caused the germanium to grow in a poly-crystalline film rather than single crystalline. The poly-crystalline Ge can be seen in the dark, sandy parts of the image. In the clear parts of the image, the Ge growth was inconsistent. (b) A sacrificial oxidation step cleaned the Si surface and resulted in crystalline Ge growth. The square in the image shows a smooth Ge film.

surface contaminants.

This process resulted in a silicon surface that was still not clean enough for high-quality Ge growth. The germanium grown on this surface was virtually always poly-crystalline, as seen in Figure 3-1(a). It was hypothesized that the etch chemistry of the oxide etch left fluorocarbons on the surface of the silicon, which could not be removed with basic wet cleans [61].

To ensure a clean Si surface, a sacrificial oxidation step was used [62]. After the piranha cleans above, a thermal oxidation was done on the wafers at 800°C. 5 - 10 nm of oxide was grown and then subsequently stripped off in a 10:1 BOE bath. The wafers then received an RCA clean and a 900°C pre-bake. This reliably left the surface of the wafer clean and resulted in single crystalline germanium growth, as seen in Figure 3-1(b). Figure 3-1 shows images of germanium grown using identical growth parameters but the two different cleaning processes. Table 3.1 outlines the differences in surface preparation steps. Process B was used on all of the subsequent wafers.

After the surface preparation, germanium was grown using a general two-step method. The first step was done at low temperature (365°C) and 60 T chamber pressure to ensure a smooth Ge film. Next, the temperature was increased to 750°C to increase the growth rate while maintaining high quality Ge. Details of the temperature and pressure for this final step can be found in the next section.

Table 3.1: Surface preparation procedures

Process A	Process B
Pattern field oxide	Pattern field oxide
Dry etch in C_4F_8/CH_2F_2 plasma	Dry etch in C_4F_8/CH_2F_2 plasma
Wet etch in BOE	Wet etch in BOE
Double piranha with HF dip	Double piranha with HF dip
RCA clean with short HF dip	RCA clean with short HF dip
	Thermal oxidation
	Oxide removal in BOE
	RCA clean with short HF dip
Pre-bake at 900°C	Pre-bake at 900°C
Ge growth	Ge growth

3.1.2 Hole filling and faceting

Growth techniques for the high temperature step were studied by Kim to optimize hole filling and germanium faceting [26] [63]. Details can be found elsewhere [63] and a summary is provided here. Kim demonstrated that increasing the Ge growth temperature greatly reduced the {311} faceting, leading to better hole filling behavior. Increasing the germane partial pressure also reduces the faceting. Furthermore, low pressure is needed to ensure good selectivity of germanium on silicon (rather than deposition on the SiO_2). It was found that growing Ge at 750°C with a germane partial pressure of 133 Pa and a chamber pressure of 10 T yielded germanium which filled the oxide holes the best while maintaining good selectivity to silicon over oxide.

3.1.3 Growth parameters and threading dislocations

The final growth parameters of 750°C, 10 T, and 133 Pa of germane partial pressure resulted in germanium that filled the oxide holes well and minimized faceting [63]. The threading dislocation density of these films was found to vary with window size [63]. It was found that a cyclic anneal can reduce the defect density of a large area, 0.8 μm-thick film from 10 x 10^8 cm^{-2} for an as-grown sample to 1.2 x 10^8 cm^{-2} for a film annealed four times. Furthermore, the defects in an an unannealed, 1 μm-thick film decrease with the size of the window opening. A 5 μm-wide opening had a defect density of 5.5 x 10^8 cm^{-2}. This decreased to 1.7 x 10^8 cm^{-2} for a 0.65 μm-wide opening. A 0.65 μm-wide opening with 1 μm of Ge that was cyclically annealed four times showed very few defects. This number was not quantified because the sparseness of the defects led to low confidence in the measurement.

3.2 Fabrication of photodiodes

Photodiodes were fabricated from the selectively-grown Ge films. The fabrication was a joint effort between MIT Lincoln Laboratory (MITLL) and MIT's Microsystems Technology Laboratory (MTL). The surface preparation of *p+* Si wafers, including sacrifical oxidation, was all done at MITLL. The germanium growth was done at MTL as part of this thesis using the two step method described previously. During the growth of the low-temperature seed, the germanium was optionally doped *p*-type with B_2H_6. This doping helps to reduce the impact of the dislocations that are present in the first 200 nm of the Ge film by incorporating them into the *p*-type contact. It also helps to reduce the series resistance of the device by reducing the impact of the valence band offset between the Ge and the Si on the current conduction [64]. After growth, the samples went back to MITLL for the final processing into photodiodes.

After growth, a chemical-mechanical polishing (CMP) step was used to planaraize

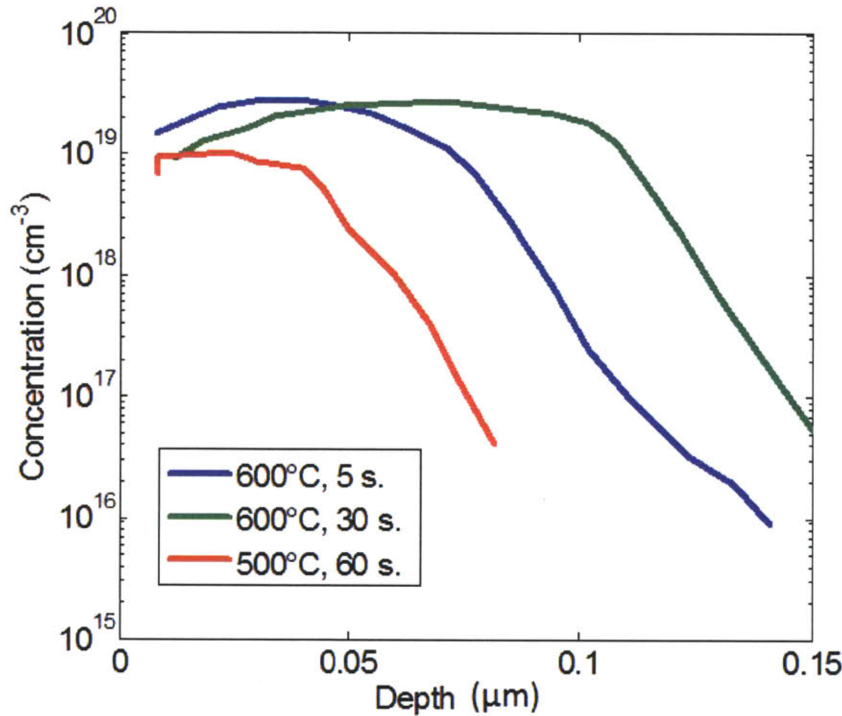

Figure 3-2: Spreading resistance profiling of three different activation anneal conditions. The 600°C anneal for 5 seconds was chosen both to maximize the active phosphorus concentration while minimizing the diffusion into the Ge. The implant was done at 25 keV with a dose of 1 x 10^{15} cm^{-2}. Courtesy of Solecon Laboratories.

the Ge surface. Due to the sensitivity of germanium to typical CMP slurries [65, 66], this step was carried out using only water. After CMP, the wafers were implanted with phosphorus at an energy of 25 keV and a dose of 1 x 10^{15} cm^{-2} through a ~10 nm screen oxide. The dopants were then activated using a rapid thermal anneal at 600°C for 5 seconds to form a vertical *pin* junction. Spreading resistance profiling was performed by Solecon Laboratories on three different annealing conditions, as seen in Figure 5-9. The 600°C anneal for 5 seconds was found to have the highest overall activation of phosphorus of 3 x 10^{19} cm^{-3}. It also resulted in the steepest profile, which yielded the highest internal electric field in the device.

After activation, 90 nm of PE-CVD oxide was deposited. Contact vias were etched using a combination of dry and wet etches. Finally, metal was deposited and patterned

into contacts.

3.3 Electrical characterization

As mentioned earlier, low dark current is an important figure of merit for these devices. The crystal orientation of the device, the inclusion of a post-growth cyclic anneal, and whether or not the junction intersected the sidewall all impacted the dark current.

3.3.1 Effect of cyclic annealing on dark current

After the high temperature growth step, some of the devices received a 4X cyclic anneal between 800°C and 450°C for times of 150 seconds and 90 seconds respectively. The anneal served to reduce the dislocation density as mentioned previously. Figure 3-3 compares a device that received the anneal and one that did not. In both cases, the germanium islands were 5 x 10 μm with $n+$ regions that measured 1 x 4 μm. The cyclic anneal reduced the dark current at -1 V by ~5X. This is consistent with the reduction in dislocation density in the Ge film. Furthermore, the anneal increases the forward current by reducing the series resistance. This will reduce the RC time constant of the device which is important for high-speed applications. The frequency response of these diodes is discussed in appendix D.

The reduction in series resistance could be due to two factors. First, the reduction in dislocation density could improve the series resistance by reducing the recombination of carriers in the $n+$ contact region, allowing those carriers to be extracted from the device more efficiently. Secondly, the anneal may also cause outdiffusion of the boron from the Si wafer into the Ge film. This autodoping of the Ge film serves to reduce the impact of the valence band offset between the Si and the Ge and reduce the series resistance [64].

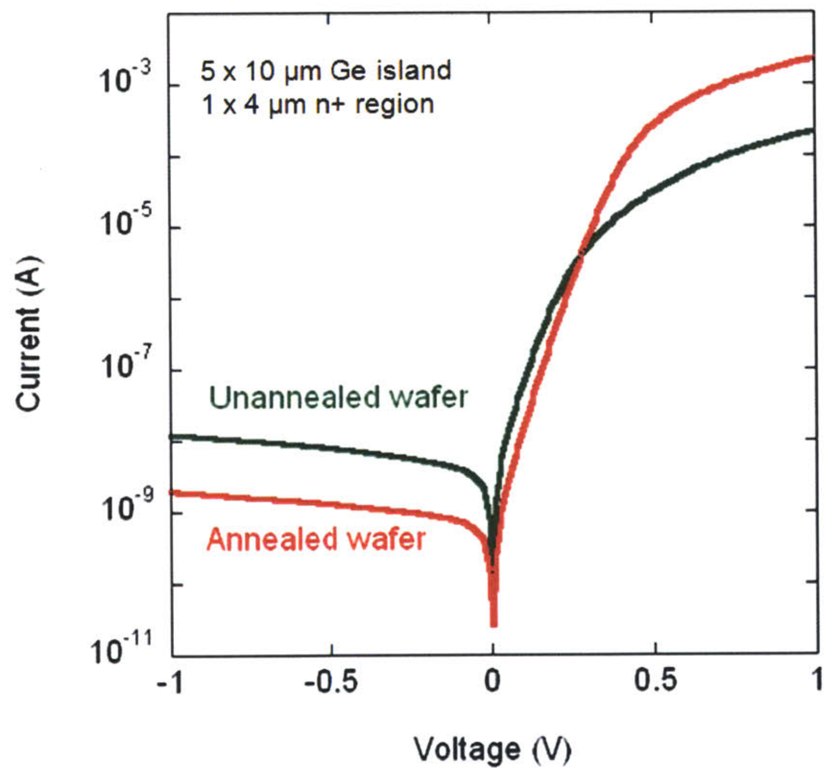

Figure 3-3: Current versus voltage characteristic illustrating the effect of a cyclic anneal on the dark current of 5 x 10 μm photodiodes. The cyclic anneal reduces the threading dislocation density, resulting in lower dark current and high forward current. The annealed wafer was #5223 and the unannealed wafer was #5222.

3.3.2 Effect of orientation on dark current

The germanium films were grown in windows that were etched both parallel to the wafer flat, the $\langle 110 \rangle$ direction, and at a 45° angle to the flat, the $\langle 100 \rangle$ direction. Previous studies have shown that the orientation of the window has an effect on the dark current, with windows with $\langle 100 \rangle$-oriented sidewalls having lower leakage currents [67].

In this study, it was also found that the orientation of the window has an effect on the yield of the devices. This is illustrated in Figure 3-4. Eight devices were measured for each orientation. For the $\langle 110 \rangle$ direction, half of the devices were very leaky, while one had a steep slope in reverse bias, and three rectified well. For the $\langle 100 \rangle$ direction, one device was very leaky, while the remaining seven rectified well. It is possible that this effect is a result of processing conditions which impacted device yield. No attempt was made to reproduce the results to check this conjecture.

3.3.3 Layout of the $n+$ region

The intersection of the $n+$ region with the oxide sidewall also had a significant impact on diode performance. Figure 3-5 shows IV characteristics for two 100 x 100 μm square devices. In one device, the dopants were implanted to completely cover the top of the film. In the other device, the dopants were implanted 5 μm away from the sidewall. As the figure shows, when the dopants intersect the sidewall of the device, the diode no longer rectifies. This suggests that the oxide sidewall significantly degrades the junction. Note that in the devices discussed in Section 3.3.2, the $n+$ region was kept away from the window edge.

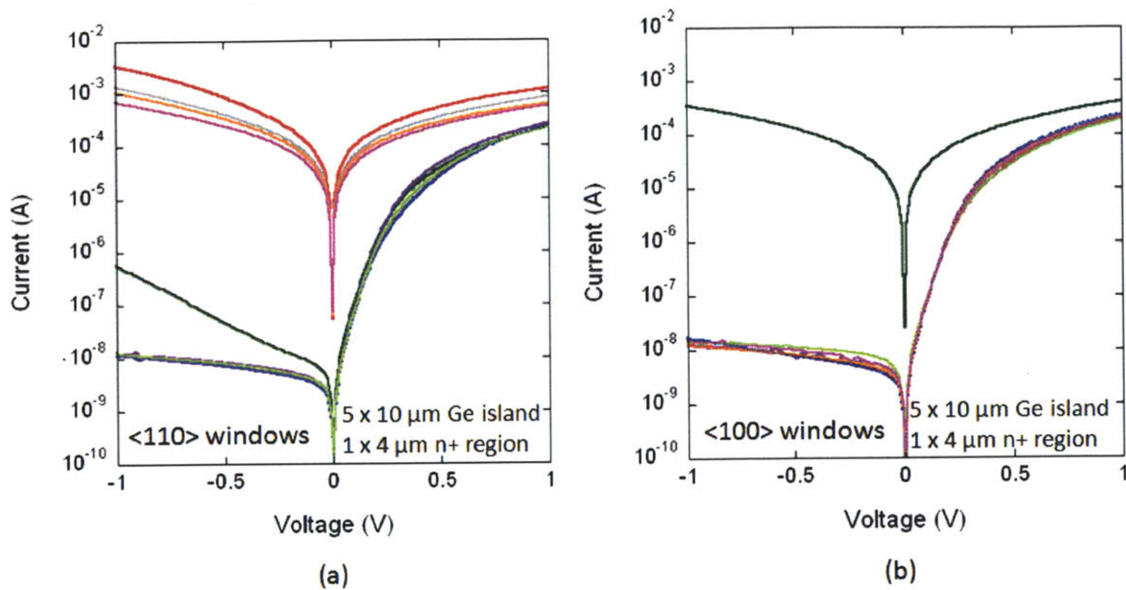

Figure 3-4: IV curves illustrating the effect of the orientation of the Ge film on the dark current of devices. Devices made in the windows in the ⟨110⟩ direction (a) had a much lower yield than devices made in windows in the ⟨100⟩ direction (b). The devices in this figure are all 5 x 10 μm Ge islands with 1 x 4 μm $n+$ regions. They are all unannealed. Curves represent eight different devices of the same size all from wafer #5222.

3.3.4 Lowest dark current

The lowest dark current measured on these samples was from one of the smallest devices fabricated. Unfortunately, due to its size, the yield was low for this type of device. The device is 0.35 x 10 μm large with an $n+$ region of 0.25 x 5 μm. The device was fabricated in the ⟨100⟩ direction on an unannealed wafer (fewer of the annealed devices survived processing) and the IV curve is shown in Figure 3-6. The dark current of this device was 0.5 nA at -1 V and the dark current density was 40 mA/cm^2.

3.3.5 Size dependence of dark current densities

As mentioned earlier, as the size of the device shrinks, the quality of the germnaium film should improve. Dark current density can be used as a measure of film quality.

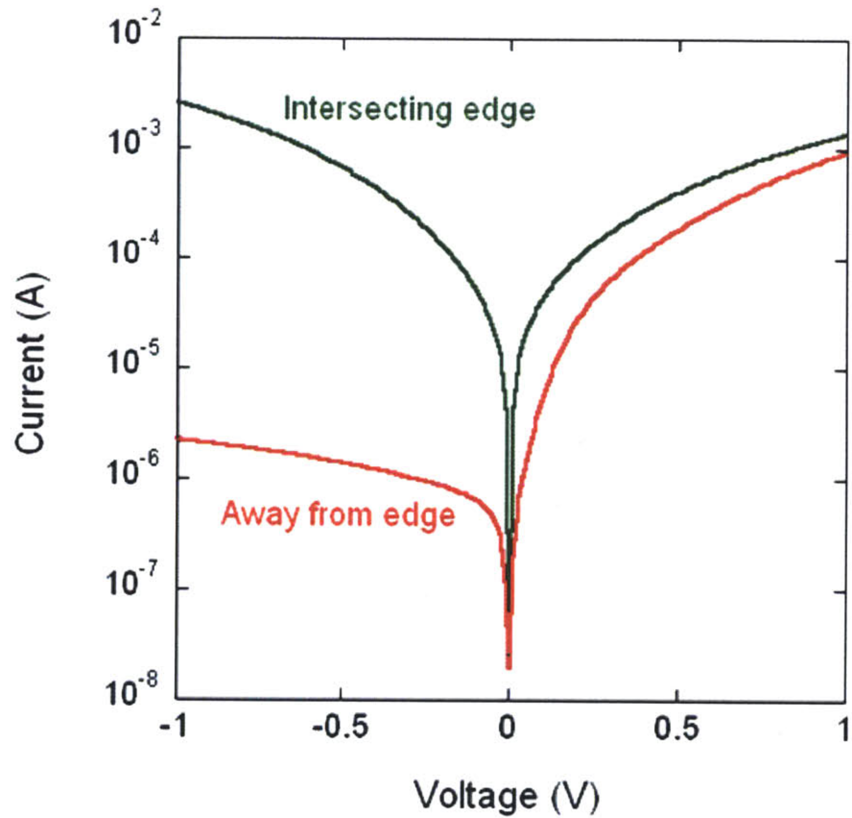

Figure 3-5: IV curves from diode with different n-type layouts. When the junction intersects the sidewall of the device, the leakage current is very high. These devices were all from wafer #5222.

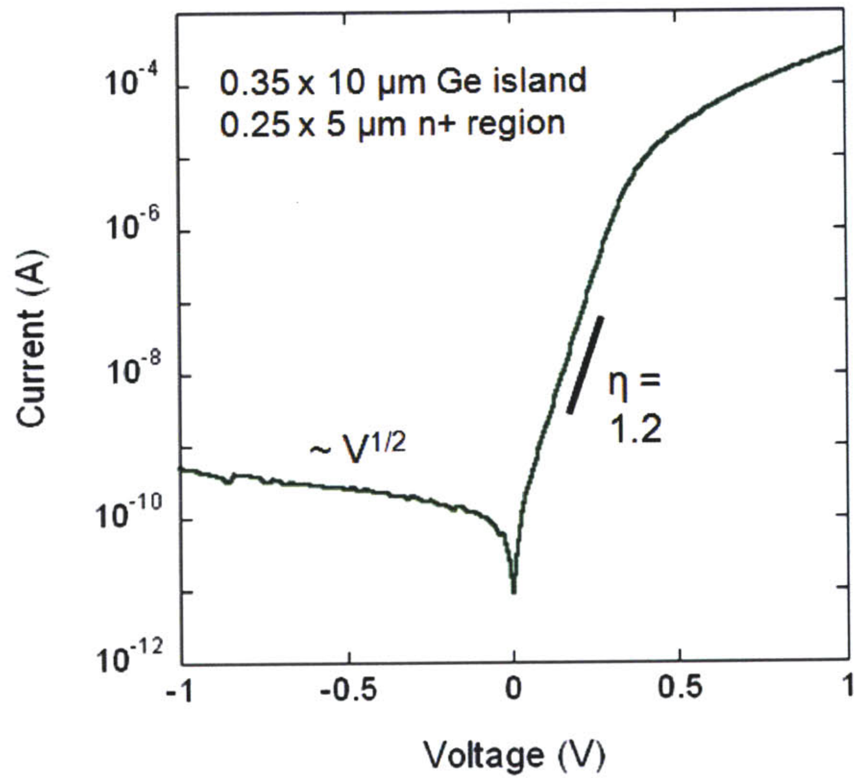

Figure 3-6: IV curve from the diode with the lowest dark current. The Ge island is 0.35 x 10 μm with an $n+$ region of 0.25 x 5 μm. The dark current at -1 V is 0.5 nA. This device was fabricated in germanium that was grown in windows aligned along the $\langle 100 \rangle$ direction. The wafer (#5222) did not receive an anneal.

The lowest dark current densities reported to date have been ~0.1 mA/cm^2 [22] [45]. In both cases, the defect density is expected to be low. In [22], the graded buffer layer increases the germanium concentration gradually so that threading dislocation density is minimized. In [45], the germanium is grown selectively, first in a very high aspect ratio hole and then in a larger region. Most of the defects terminate in the high aspect ratio region, resulting in a very high quality film at the top of the germanium.

Table 3.2: Size dependence of dark current density

Oxide window size	*n+* region size	Dark current at -1 V	Dark current density at -1 V
0.35 x 10 μm	0.25 x 10 μm	0.5 nA	40 mA/cm^{-2}
5 x 10 μm	1 x 4 μm	2 nA	50 mA/cm^{-2}
100 x 100 μm	4(9 x 89 μm)	2 μA	62 mA/cm^{-2}

The dark current densities of some different size devices in this study can be found in Table 3.2. The dark current density was calculated by dividing the absolute current by the area of the *n+* region, not the area of the oxide window size, because the *n+* region defines the active area of the device. As the device size shrinks, the dark current density improves. This is most likely due to the reduction in threading dislocations in the germanium film for smaller devices. However, as described earlier, the decrease in window size of over 2 orders of magnitude should result in a large improvement in threading dislocation density. The dark current density, while improved, does not reflect this expected improvement in material quality, showing an improvement of ~1.5X. This indicates that something else is dominating the dark current. The sources of dark current are analyzed further in Chapter 5 and it is likely that the dark current is limited by generation in the depletion region due to another trap source.

3.4 Optical characterization

Photoresponse measurements were done on larger devices. A broadband laser (1260 nm - 1630 nm) was used as the light source and was coupled in through a fiber. The details of the measurement can be found in Appendix B. The current was measured for three different input power levels and responsivity was calculated as an average of the three points. This section will discuss the effect of the germanium film thickness and the effect of the size of the device on the photoresponse

3.4.1 Thickness of Ge film

Figure 3-7 shows the responsivity versus wavelength curves for devices with 1 μm thick Ge and 2 μm thick Ge. It is expected that a thicker Ge film will absorb more light; however, since the germanium absorption coefficient is an exponential curve with respect to wavelength, it is not expected that a doubling in film thickness should double the photoresponse. A doubling of the film thickness should result in a photoresponse that increases by less than 2X. Figure 3-7 shows the photoresponse increase by $\sim$2X, suggesting that the film quality is improving with thickness. This improvement was found in [63] and is likely leading to the improvement in photoresponse.

3.4.2 Different size Ge islands

It was found that the photoresponse also varies based on the size of the Ge island. Figure 3-8 shows normalized photoresponse curves for three different size Ge islands. These devices had different absolute responsivities. To normalize them, the first 5 values (at 1300, 1305, 1310, 1315, and 1320 nm) of the responsivity were averaged. Then each point was divided by that average and the result was plotted.

The figure shows that the absorption edge of the germanium shifts to longer wavelengths as the device size grows. The total bandgap shift is $\sim$25 meV. This

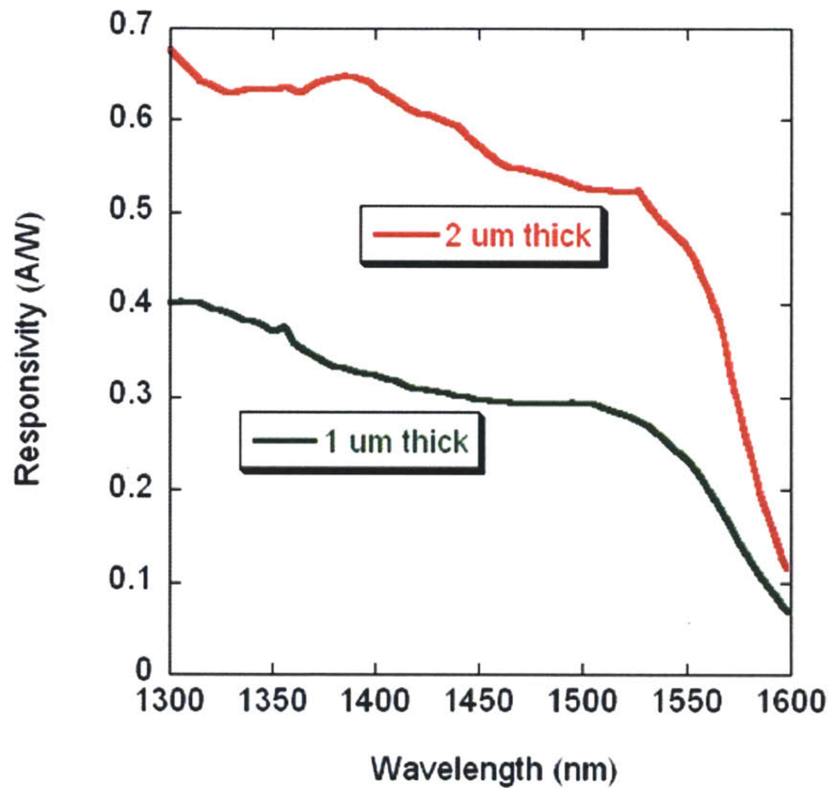

Figure 3-7: Responsivity curve for two different Ge thicknesses. The responsivity is nearly double for a film that is nearly double the thickness. Since most of the absorption of light happens in the top of the film, this suggests that the film quality is improving with thickness. This data of the 2 μm film was taken from wafer #5365 and the data from the 1 μm film was taken from wafer #5363.

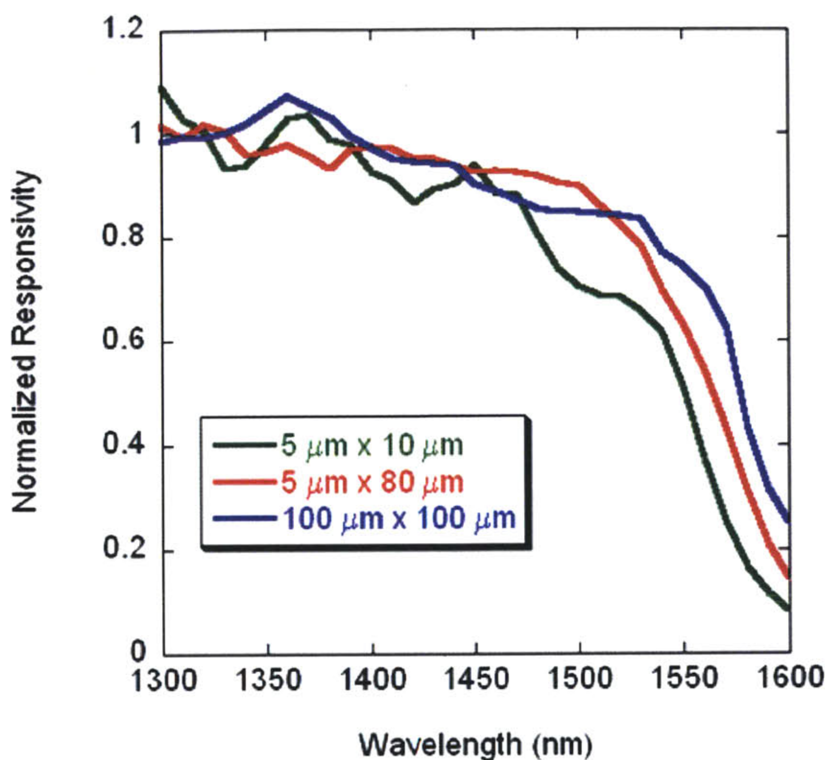

Figure 3-8: Normalized responsivity curves for three different Ge island sizes. The absorption edge is shifted out to longer wavelengths for the larger devices, suggesting a difference in the strain. This data was measured on wafer #5223.

suggests that there is more strain in the larger devices.

Raman spectroscopy was performed at Freescale Semiconductor to confirm the differences in strain. The Raman analysis was done with a laser of 514.5 nm and the Ge peaks were compared to Ge peaks for a bulk Ge wafer. The strain is summarized in Figure 3-9.

The figure shows that, as the device size grows, the tensile strain increases. This tensile strain shrinks the bandgap and allows the Ge to absorb at longer wavelengths. It is important to note that the strain in these devices is not due to the lattice mismatch between the Si and the Ge (as is the case for thin Ge films). This strain is caused by the difference in thermal expansion coefficients between the Si and Ge. Immediately after Ge growth, the wafers are annealed at a high temperature. When

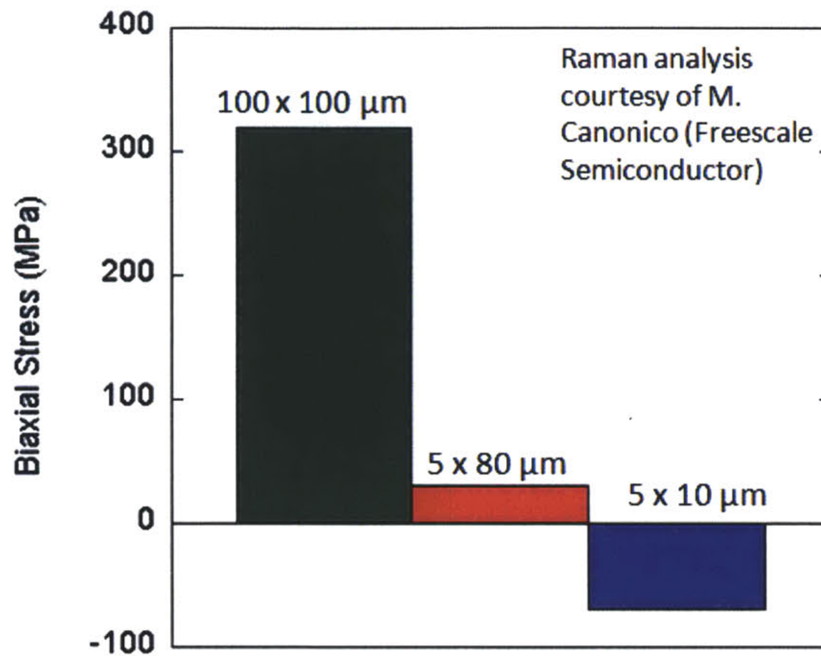

Figure 3-9: Residual tensile strain in three different Ge island sizes. The tensile strain is largest for the largest device, pushing the responsivity curve out to longer wavelengths. The analysis was done on wafer #5223.

they cool to room temperature, the Ge and Si contract by different amounts, leaving some residual strain. It should be noted that, according to the Raman data, the smallest device is under slight compressive strain. This compressive strain is expected to widen the bandgap [40] and is consistent with the responsivity data.

The strain in the 100 μm device is comparable to the strain found in blanket Ge epitaxial films [40]. As the device size shrinks, the strain decreases. This size dependence of strain has been observed previously [68] and can be explained by the faceting in the Ge film. When the Ge grows in oxide windows, the films grow with facets around the sides. These facets are normally 1 - 2 μm wide and serve to relax the strain in the film. For a large (100 μm) device, the facets are a small portion of the overall surface area, so much of the strain is retained. For smaller devices, however, the facets are actually a large fraction of the surface area and much of the strain is relaxed. A cross-sectional SEM of a Ge film grown in this work with facets

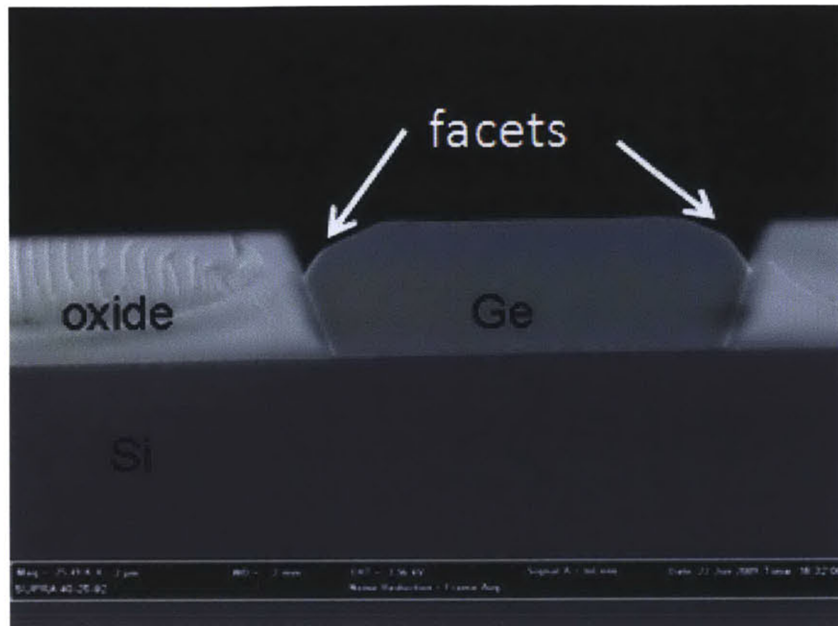

Figure 3-10: A cross-sectional scanning electron micrograph of the facets in the Ge film. The facets serve to relax some of the strain during growth, leading to less strain in smaller devices and more strain in larger devices.

can be seen in Figure 3-10.

3.5 Waveguide integrated devices

After stand-alone Ge photodiodes were characterized, a process was developed to integrate a Ge diode in a Si electro-optic modulator process flow. This flow integrated Si modulators, Si waveguides, and Ge diodes using only CMOS-compatible processing steps. The process development was a joint effort between MIT Lincoln Laboratory and the Microsystem Technology Lab at MIT. Most of the fabrication was carried out at MITLL, with the exception of the Ge growth which was done at MTL. This section will discuss the process flow, electrical characteristics, and optical characteristics of Ge detectors integrated in this flow.

3.5.1 Ge diode fabrication

A process flow to fabricate Si waveguides and Si modulators was already well-developed by MIT LL. The goal of this study was to integrate the fabrication of a Ge diode. Due to thermal budget constraints, it was decided to integrate the germanium towards the end of the fabrication.

A cross-sectional schematic diagram of the wafer with Si modulators can be seen in Figure 3-11. For the purposes of this chapter, this is the starting substrate. The Si modulators are fabricated on silicon-on-insulator wafers so that the waveguides can be optically isolated from the bulk of the wafer. After modulator fabrication, the Si was etched. There were two flavors of Ge diodes grown. In the first, 50 nm of Si was left on which to grow Ge. In the second, all of the Si was etched away and the Ge was grown laterally from the sides of the Si modulator. This was done to ensure that the operation of the Ge diode would not be influenced by the underlying Si. Previous studies on Si diodes have shown that, under certain circumstances, they can absorb light in the near infrared [69]. By etching away all of the Si, that possibility was removed. The two different versions of the diode are shown schematically in Figure 3-12.

To minimize dopant diffusion in the Si, the Ge did not receive a post-growth cyclic anneal, regardless of the flavor of the diode. The structure was covered with either a PE-CVD oxide or a PE-CVD oxynitride. Contact vias were etched and filled with tungsten plugs. Finally, metal contacts were deposited and patterned. A cross-sectional schematic diagram of the final structure, lateral *pin* structures, can be seen in Figure 3-12.

Figure 3-13(a) shows the intended diode structure with 50 nm of silicon present. The actual diode structure had significant Ge overgrowth and looked more like the schematic in 3-13(b). The implications of this overgrowth will be discussed in Section

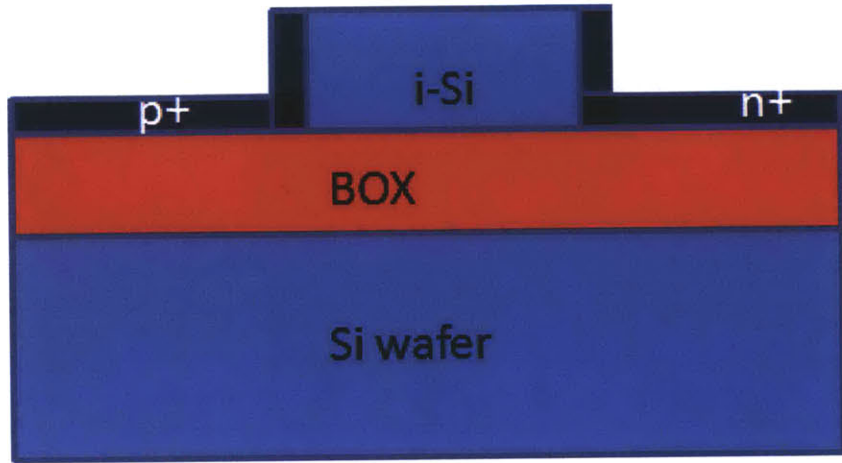

Figure 3-11: Schematic diagram of a silicon modulator fabricated by MIT LL. This was the starting substrate for the fabrication of waveguide-integrated Ge diodes.

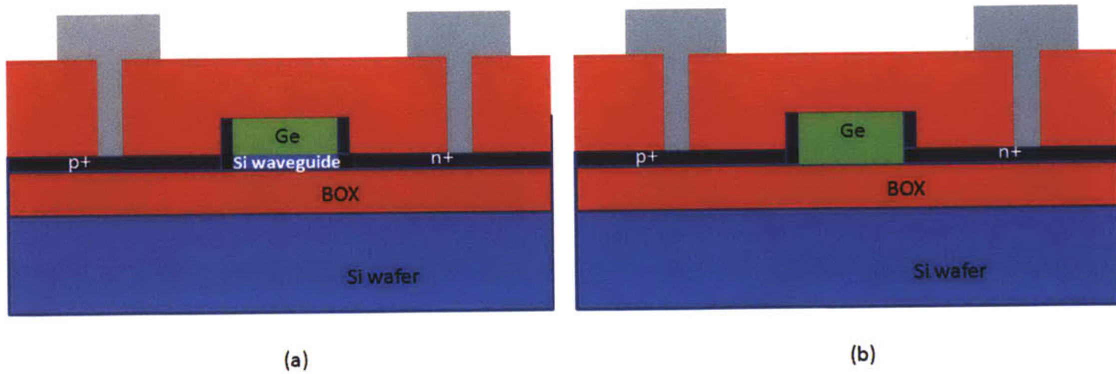

Figure 3-12: Schematic diagrams of the two different types of waveguide-integrated germanium diodes. (a) A germanium detector fabricated on ~50 nm of Si. (b) A germanium detector fabricated by growing the germanium laterally from the Si sidewalls. In (b) all of the underlying Si is removed prior to germanium growth. Both diagrams are oriented such that the light propagates into the page and absorption in the germanium also takes place into the page.

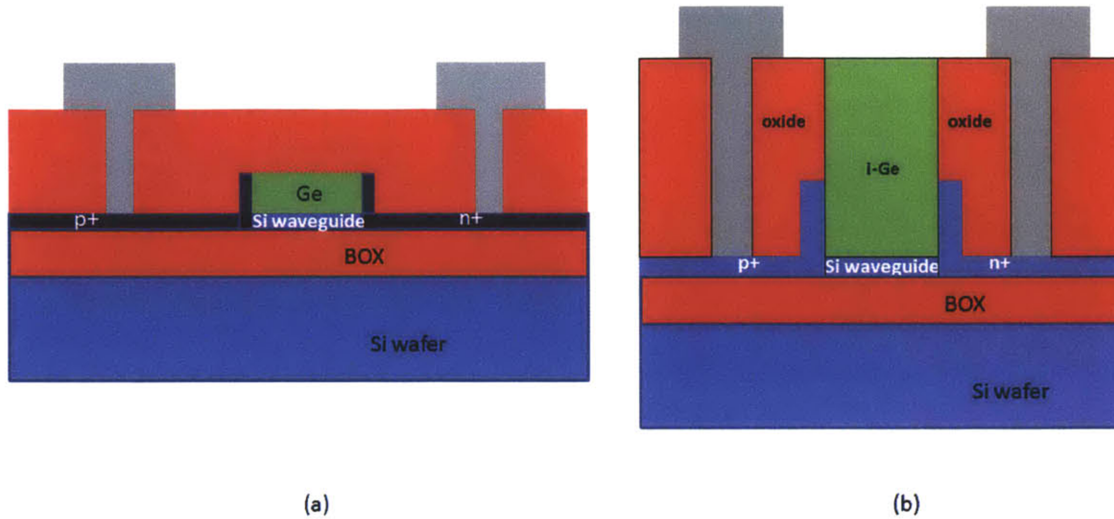

Figure 3-13: Schematic diagrams of (a) intended and (b) actual waveguide-integrated Ge diode. The germanium overgrowth was unplanned but not detrimental to operation of the device.

3.5.2.

Due to processing difficulties, only a few sizes of devices survived each fabrication run. In the first run, where 50 nm of Si was left on which to grow Ge, only the 100 x 0.25 μm devices survived. In the second run, where all of the Si was etched, only the 500 x 0.35 μm and 5 mm x 0.35 μm devices survived. For brevity, the devices will only be referred to by their length in the subsequent sections.

3.5.2 Diodes grown on 50 nm of Si

Figure 3-14 shows a typical current versus voltage characteristic for a device grown on 50 nm of Si. The dark current is ~0.27 nA at -1 V (~1.1 mA/cm^{-2}) and the I_{on}/I_{off} ratio is 10^7 which is one of the highest reported in the literature.

Optical measurements were taken by using the same broadband laser mentioned earlier and a lensed fiber with a 3 μm diameter spot size. Light was coupled from the edge of the device into the Si waveguide. A typical responsivity versus wavelength curve can be seen in Figure 3-15.

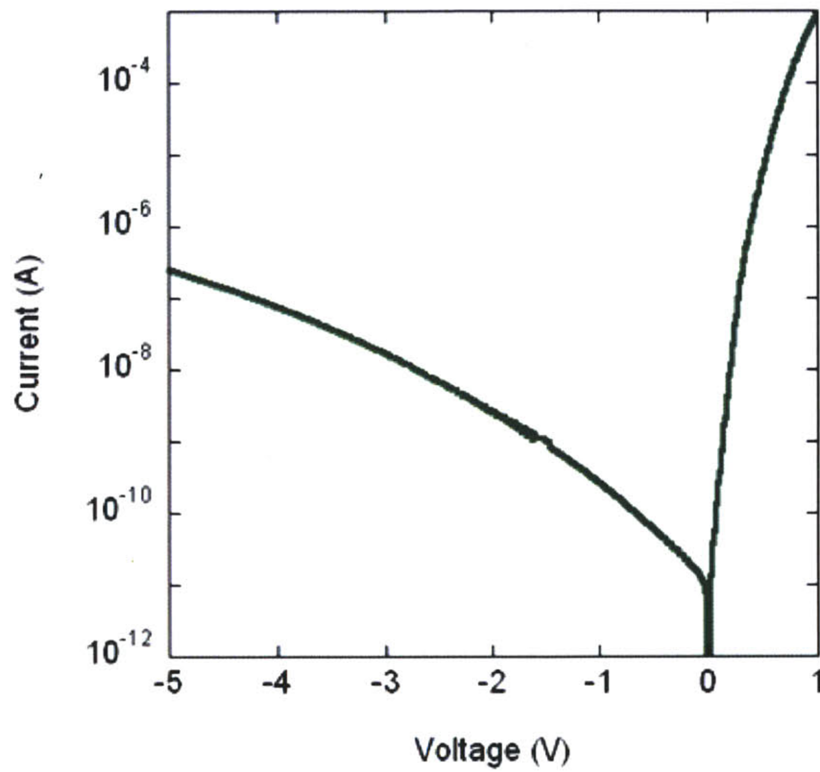

Figure 3-14: Current versus voltage characteristic for a 100 x 0.25 μm waveguide-integrated device. At -1 V, the dark current is ~0.27 nA. This measurement was taken on a device fabricated on wafer #5800.

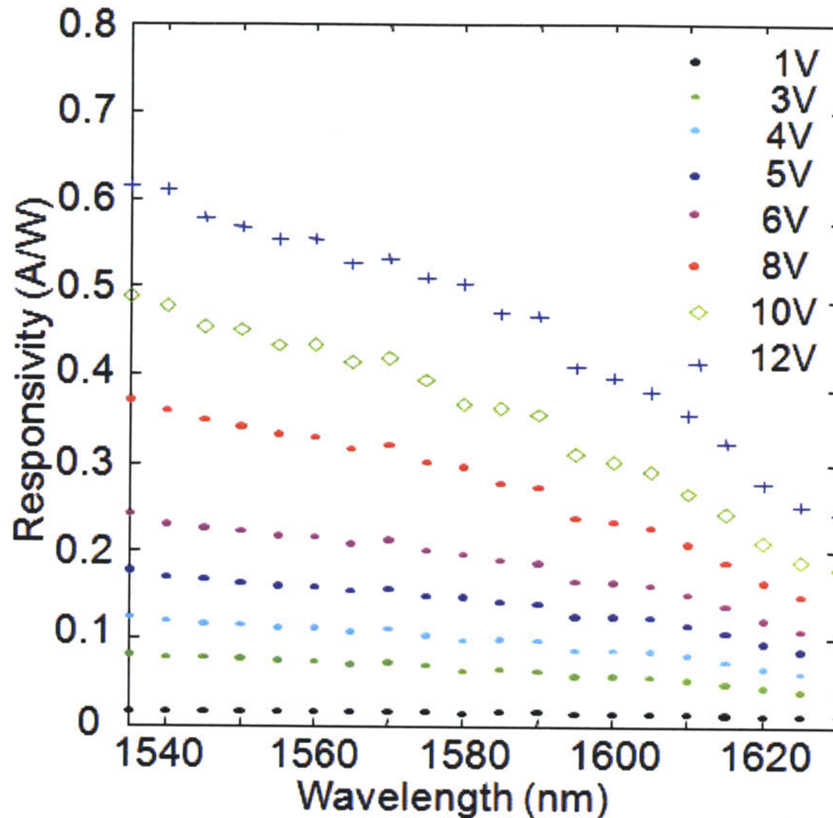

Figure 3-15: Responsivity versus wavelength curve for a 100 x 0.25 μm waveguide-integrated device. The responsivity is low at low voltages, but increases with increasing voltage. This device was fabricated on wafer #5800.

As seen in the figure, the responsivity at low voltages is low. At -1 V and 1550 nm, the responsivity is 0.02 A/W. However, this rises to 0.58 A/W at -12 V and 1550 nm. A remarkable feature of this responsivity curve is that the roll-off at 1550 nm is not as sharp as it is in the vertically illuminated devices. From 1550 nm to 1630 nm, the responsivity only falls by approximately 2X. For a vertically illuminated device, it falls by roughly 5X over the same range. This is likely due to the geometry of the device. Since the light is coupled from the edge and the device is so long, there is 100 μm over which the light can be absorbed (compared to 2 μm of Ge for the vertically illuminated devices). Germanium does not absorb long wavelengths very strongly, but, given enough material, it can. Figure 3-15 demonstrates the effect of the long Ge absorption tail.

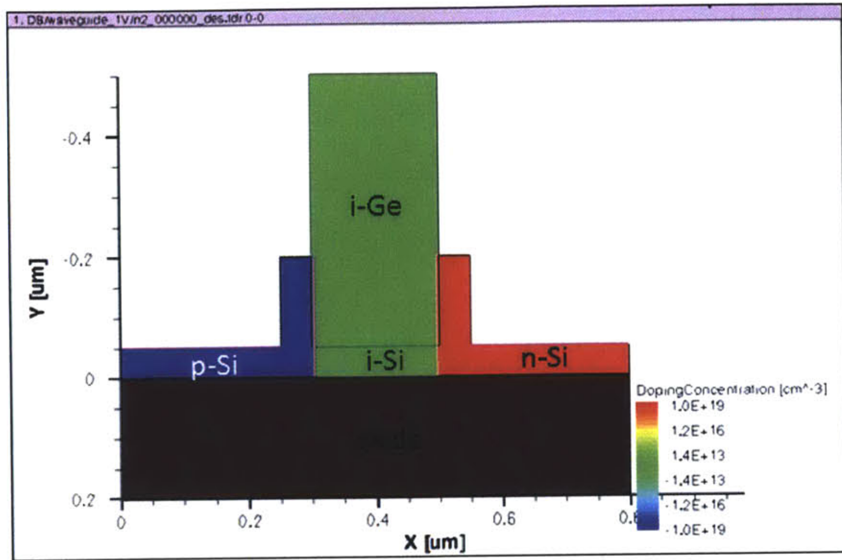

Figure 3-16: Cross-sectional schematic of simulated device in Sentaurus. The silicon wings are doped, but the germanium is intrinsic. The entire structure sits on the burried oxide.

The strong voltage dependence of the device was investigated as well. Since the device is so narrow, it was anticipated that it would be fully depleted at or close to 0 V. Simulations were done in Sentaurus Device to further explore the electrostatics of the device.

Figure 3-16 shows the cross-section of the device in Sentaurus. The *p*- and *n*- type Si wings were each doped to 10^{19} cm^{-3} and the germanium was left intrinsic. Figure 3-17 shows the cross-section of the device with two different voltages applied. Figure 3-17(a) shows the device with an applied bias of -1 V. In this case, the maximum electric field is actually in the underlying Si and not in the Ge. The field is low in the Ge itself. At -5 V (Figure 3-17(b)), the maximum electric field is in the Ge and the underlying Si.

Figure 3-18 shows the electric field along a vertical cut down the center of the germanium. The different curves represent different applied voltages. The black dashed lines indicate the germanium region. The figure indicates that it is difficult to

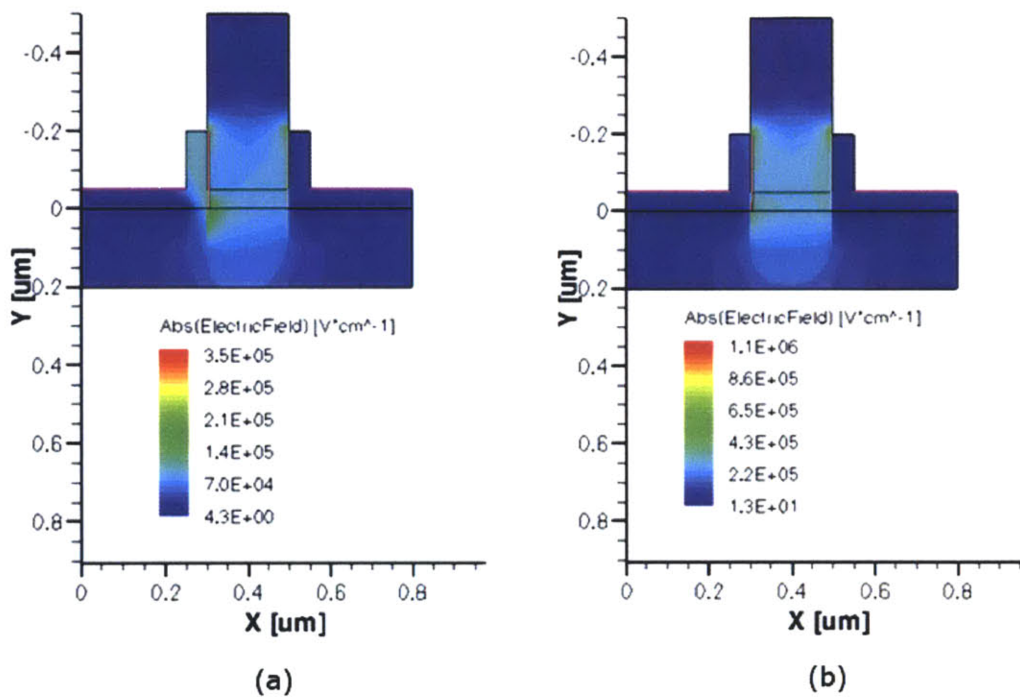

Figure 3-17: Electric field at (a) -1 V and (b) -5 V. At low voltages, the electric field is in the underlying Si and not in the Ge.

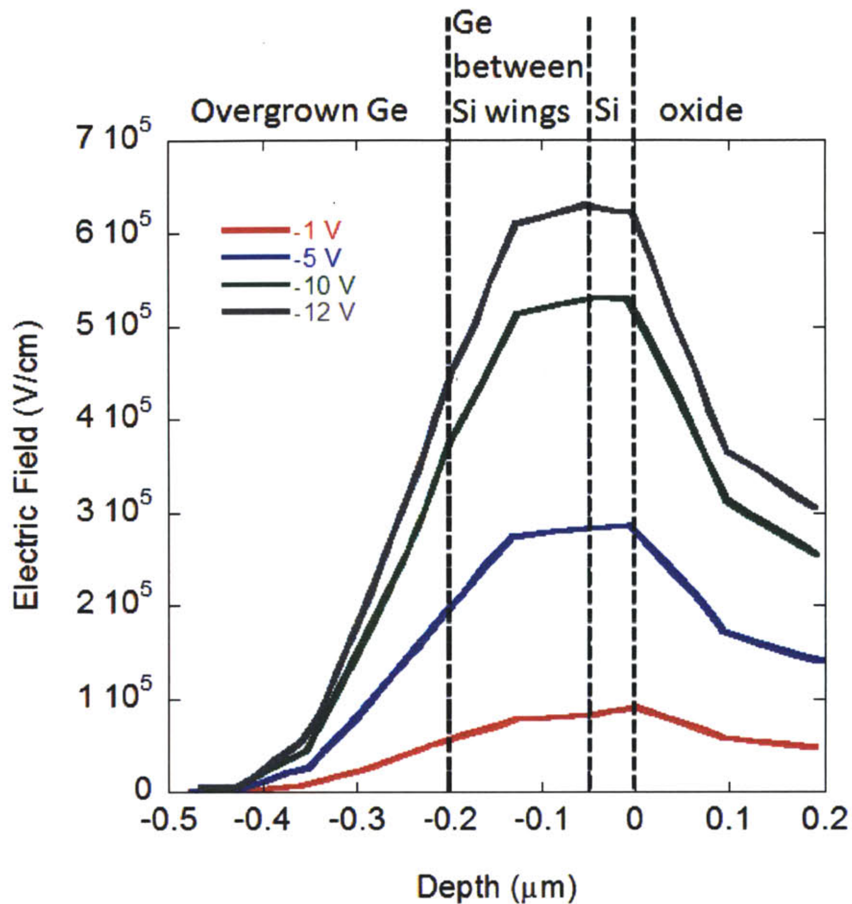

Figure 3-18: Electric field down a vertical cut in the germanium. It is difficult to get a high electric field in the germanium.

get a high electric field in the germanium and that the electric field is preferentially in the underlying silicon. This is most likely due to the fact that the Ge is not doped separately. The p- and n-type contacts are in the Si.

3.5.3 Diodes grown laterally

While the responsivity that was measured in Figure 3-15 can be explained by the long tail of the absorption curve, there was some concern that the underlying Si could also be responsible for the absorption. To clarify which material was absorbing light, the Si was etched entirely down to the buried oxide and Ge was grown laterally from the

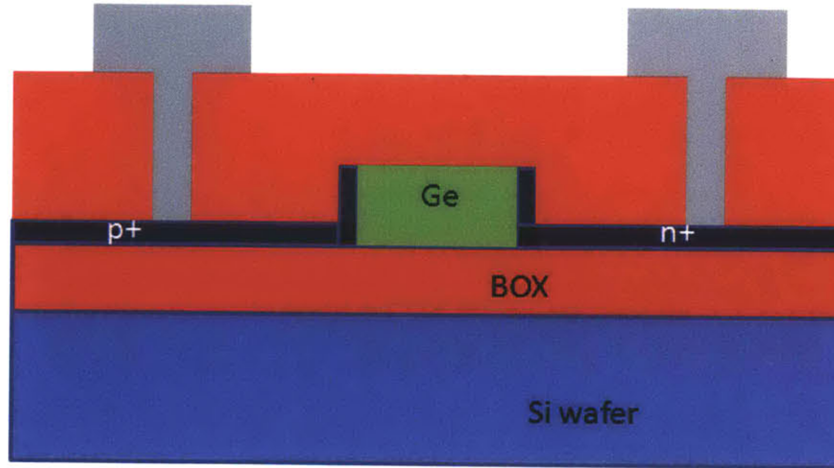

Figure 3-19: A schematic cross-sectional diagram of a Ge diode grown laterally from Si sidewalls. By removing all of the silicon, any measured photoresponse must be due to light absorbed in the the germanium.

sides. A schematic diagram of the device can be seen in Figure 3-19.

Typical current versus voltage curves for both a 5 mm long device and a 500 μm device can be seen in Figure 3-20. The 500 μm long device has a very flat curve in reverse bias, while the 5 mm long device has a much steeper slope. It is unclear what is the cause of these different shapes, though they are very consistent across devices and die. At -1 V, the 500 μm devices have a dark current of 0.1 nA and the 5 mm devices have a dark current of 1 nA.

Figure 3-21 shows the responsivity versus wavelength curves for a typical 5 mm device at different reverse biases. Unfortunately, there were no working test structures on the chip to test for fiber-to-chip loss, so these measurements do not take that into account. Assuming a moderate value for the loss (2 dB), the actual responsivity of these devices could be significantly higher.

The responsivity for this device at -8 V and 1550 nm is 0.22 A/W. This is slightly lower than the photoresponse for the devices grown on 50 nm of Si, but still on the same order. This difference could easily be attributed to fiber-to-chip loss. This

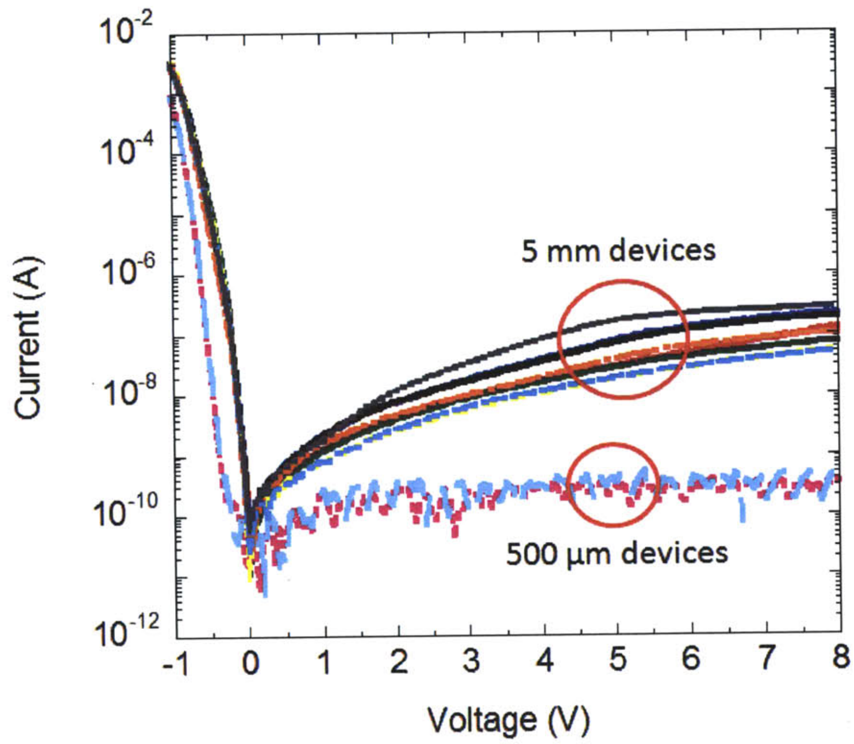

Figure 3-20: Current versus voltage characteristics for two different lengths of laterally-grown diodes. The slopes of the dark current are very different for the different devices. The data was taken on devices from wafer #6665.

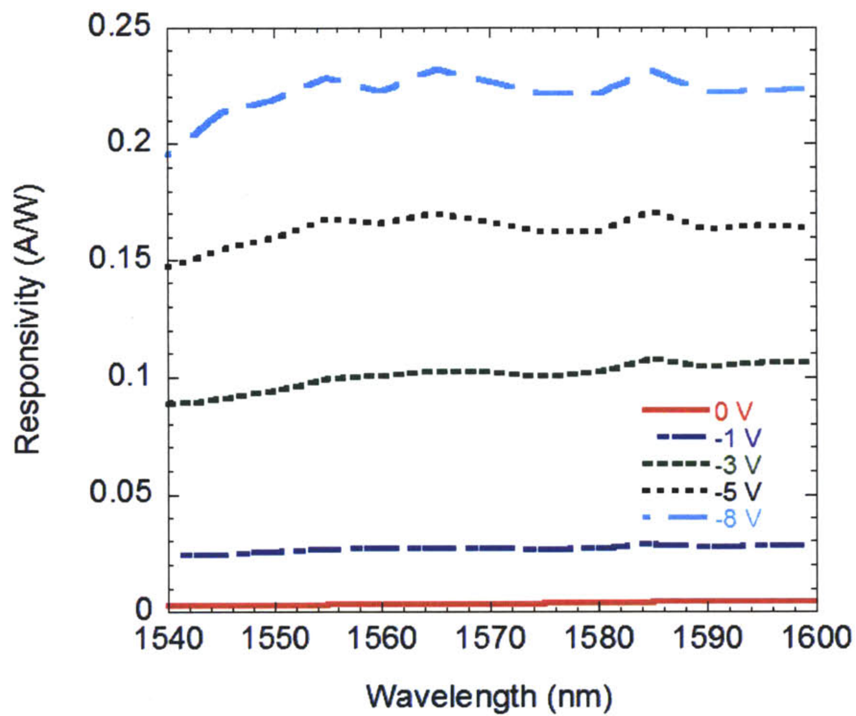

Figure 3-21: Responsivity versus wavelength characteristics for 5 mm long diodes. Responsivity is low at low biases, but improves to 0.22 A/W at -8 V and 1550 nm. The data was taken on devices from wafer #6665.

indicates that the germanium was indeed responsible for the photoresponse in the previous devices.

3.6 Chapter summary

This chapter discussed the fabrication and characterization of Ge diodes made from selectively-grown Ge films. It detailed the effect of junction position, annealing, and window size on the dark current of these devices. It also described the optical characterization of these devices and found that there is residual strain in the large devices. This strain, however, decreases with island size, making the bandgap slightly larger for small devices. This results in a shift of the photoresponse to shorter wavelengths.

This chapter also discussed the electrical and optical characterization of waveguide-integrated Ge diodes. These were some of the lowest dark current density devices that have been reported and they absorbed light out to longer wavelengths, due to their geometry.

Chapter 4

Photodiodes fabricated in blanket Ge-on-Si

Reproducibility was a large problem in the fabrication of diodes from selectively-grown germanium films. Even with the sacrificial oxidation step, it was hard to judge how many threading dislocations were present in the germanium film from lot to lot. Without a firm grasp on the defects, it was hard to fully characterize the diodes. To allow us to study the physics of the devices more closely, diodes were also fabricated from blanket Ge films. This allowed more iterations of the process and let us hone in on the best device architecture.

This chapter discusses the electrical and optical characterization of diodes fabricated from a blanket Ge film. It first briefly discusses the germanium growth and then outlines the device fabrication procedure. Next, it discusses the effects of seed doping, passivation material, and a post-metallization anneal (PMA) on the dark current. To futher investigate the effects of the PMA, metal-oxide-semiconductor capacitors (MOSCAPs) were also fabricated and their electrical characteristics are discussed. Finally, the optical characteristics of these diodes are discussed.

4.1 Ge growth and fabrication

The growth of blanket Ge-on-Si films has been studied extensively in [26] and [70]. The effects of many factors on the growth and quality of the films are well documented there, but this section will summarize the important findings from that work. Unless otherwise specified, the optimal growth parameters described here were used to grow the germanium films used in this study.

Blanket germanium films were grown in a low-pressure chemical vapor deposition (LPCVD) epitaxial growth system. The starting substrates were six inch p-type CZ Si wafers with resistivities in the range of 0.005 - 0.02 Ω-cm. The effects of chamber temperature, pressure, and hydrogen flow on the quality of the films were studied. It was found that a two-step growth procedure yielded the best results. The first step involved growing a low temperature $p+$ Ge seed layer. The optimum growth parameters for this layer were found to be 335°C at a pressure of 30 Torr with a hydrogen flow of 30 slpm. The seed layer must be at least 45 nm thick to yield a smooth surface morphology.

After seed layer growth, a thick ($\sim$2 μm) Ge cap layer was grown at a higher temperature. The optimal temperature window for this step was determined to be 600°C - 700°C. At 650°C, chamber pressures between 30 Torr and 90 Torr yield smooth films. The hydrogen flow was kept at 30 slpm.

The films were cyclically annealed between 450°C and 830°C for 90 seconds and 150 seconds respectively. The samples went through 4 cycles of this anneal, all at a pressure of 30 T. It was found that a 4X anneal was a good trade-off between the amount of time needed for the anneal and the resulting film quality. Films grown with a 4X anneal previously were found to have a threading defect density of 2 x 10^7 cm^{-2} [24].

Two different fabrication flows were used in this study. The first used a mesa etch to isolate the diodes while the second relied on $n+$ implantation for isolation. Both

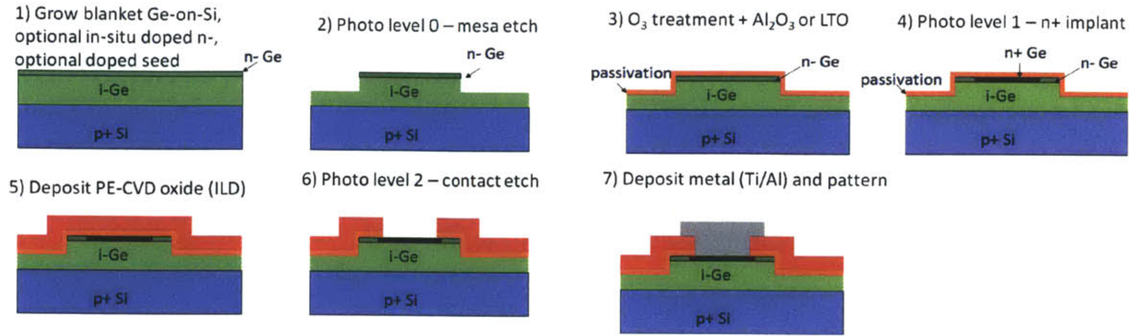

Figure 4-1: Schematic process flow of the mesa-isolated diode fabrication process. There is optional doping in the Ge seed layer and at the top ~200 nm of Ge. The passivation is either LTO or alumina.

flows will be described here.

4.1.1 Process flow with mesa isolation

In this process flow, first 10 - 20 nm of LP-CVD oxide was deposited on the germanium film. This was to promote photoresist adhesion (it was found that standard OCG photoresist would not adhere to pure Ge). This stack was then patterned and mesa etched in a solution of H_2O:H_2O_2:HCl 4:3:1 for 30 - 60 seconds to remove 0.25 - 0.5 μm of Ge. Following the etch, the oxide was stripped in buffered oxide etch (BOE). The wafers were then cleaned and the passivation material was deposited. The passivation material was either an LP-CVD oxide or Al_2O_3 deposited by atomic layer deposition. Next, the wafers were patterned and implanted with phosphorus at an energy of 35 keV and a dose of 5 x 10^{14} cm^{-2}. The projected range of the implant was ~25 nm below the Ge/oxide interface.

After implant, the junction was activated either at 550°C or 600°C for 10 seconds in a nitrogen ambient. Next, a thick (~100 nm) layer of PE-CVD oxide was deposited and contact vias were etched using standard dry and wet processes. A Ti/Al stack was deposited and etched to make metal contacts. A schematic diagram of this process flow can be found in Figure 4-1.

In addition to varying the passivation material, doping variations were studied. The seed layer was optionally doped p-type using B_2H_6 at 2 x 10^{18} cm^{-3}. This doping served two purposes. It included the highly defected region at the Si/Ge interface into the p-type contact, thereby removing it from the depletion region of the device. It also introduced some autodoping into the Ge cap layer, changing the doping profile of the entire device. On some wafers, the top 0.2 μm of the Ge cap layer was doped n-type using PH_3 to 5 x 10^{17} cm^{-3}. The purpose of this doping was to reduce the electric field at the surface of the germanium and reduce the recombination current. The effects of these doping variations will be discussed later in the chapter.

4.1.2 Process flow without mesa etch

The wet mesa etch of the germanium layer was difficult to control. The etch rate varied widely and it etched more quickly in the lateral direction than in the vertical direction, making alignment difficult in later steps. To fix this, the mesa etch was skipped and the top of the germanium film was never in-situ doped n-type. These devices relied on only the $n+$ implant and the field oxide to isolate them from neighboring devices.

In this process flow, PE-CVD oxide was first deposited and etched in BOE to make alignment marks. The oxide in the field was then stripped, leaving the alignment marks behind. (For the exact details on this part of the fabrication, please see appendix A.) Next, a screen oxide was deposited in an LP-CVD tube and the wafers were implanted. The energy of the implant ranged from 30 to 55 keV and the dose ranged from 5 x 10^{14} to 7 x 10^{14} cm^{-2}. The conditions varied to compensate for the variations in oxide thickness. The goal was to have the projected range be 50 - 60 nm below the Ge/oxide interface. A typical simulation done using the Stopping Range of Ions in Matter (SRIM) of the ion implantation profile can be seen in Figure 4-2. The intended projected range was deeper on these wafers (as compared to the

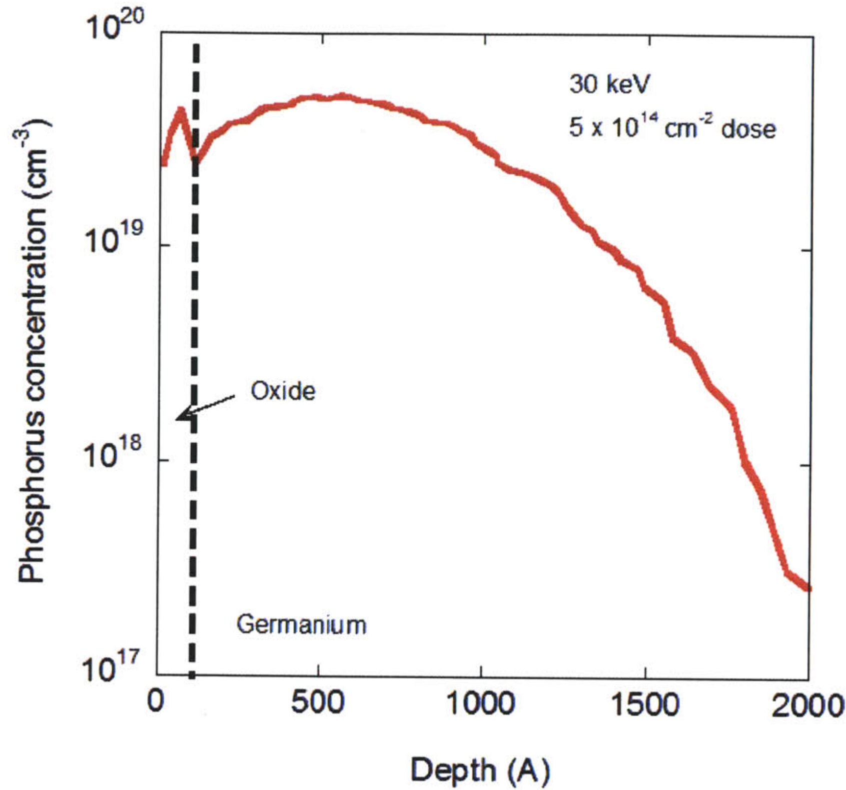

Figure 4-2: Simulated ion implantation profile of phosphorus in germanium. For this simulation, the oxide thickness was 8 nm and the implant energy was 30 keV. This put the projected range ~58 nm beneath the germanim/oxide interface. The dose was 5 x 10^{14} cm^{-2}.

mesa-isolated wafers) to ensure that the junction was not etched when the screen oxide was removed.

After implant, the dopants were activated at 550°C for 30 seconds. The longer anneal time was chosen to diffuse the phosphorus deeper into the germanium and to make sure that the junction was not etched when the screen oxide was removed. After removal of the screen oxide in BOE, the passivation layer, either ~10 nm of LP-CVD oxide or ~10 nm of Al_2O_3 deposited by atomic layer deposition (ALD), was used. A thicker (~100 nm) layer of PE-CVD oxide was then deposited and contact vias were etched using standard dry and wet processes. Finally a Ti/Al stack was deposited and patterned into contact pads. A schematic diagram of this process flow

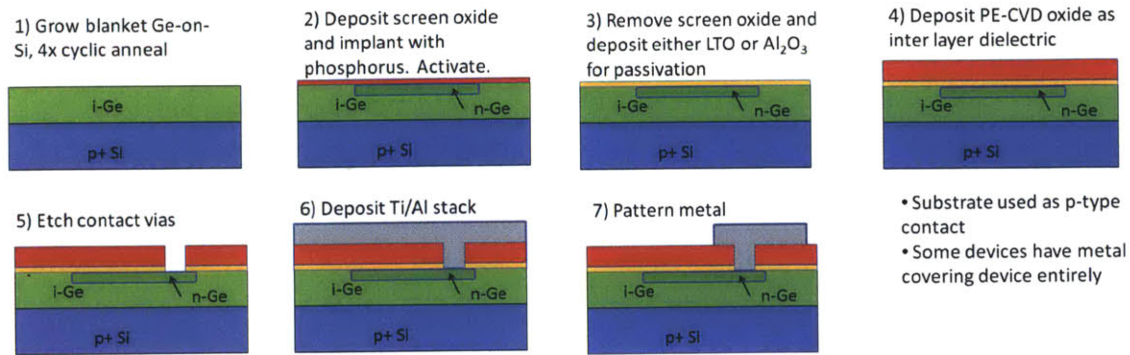

Figure 4-3: Schematic process flow of the non-mesa isolated diodes. The steps to fabricate first-level alignment marks are omitted for brevity. The $p+$ Si substrate is used as the p-type contact.

can be seen in Figure 4-3.

In addition to the different passivation materials, this process allowed for the study of the effect of a post-metallization anneal. After metallization, some pieces of the wafers were annealed in nitrogen at temperatures ranging from 300°C to 450°C for 45 minutes.

4.2 Electrical characterization of blanket Ge-on-Si diodes

In this section, the electrical characterization of diodes fabricated with a mesa etch and without a mesa etch will be described. The impact of seed doping, passivation material, dopant activation anneal, and doping structure of the Ge cap layer are all studied for the mesa isolated devices. The impact of passivation material and post-metallization anneal are studied for the devices fabricated without a mesa etch.

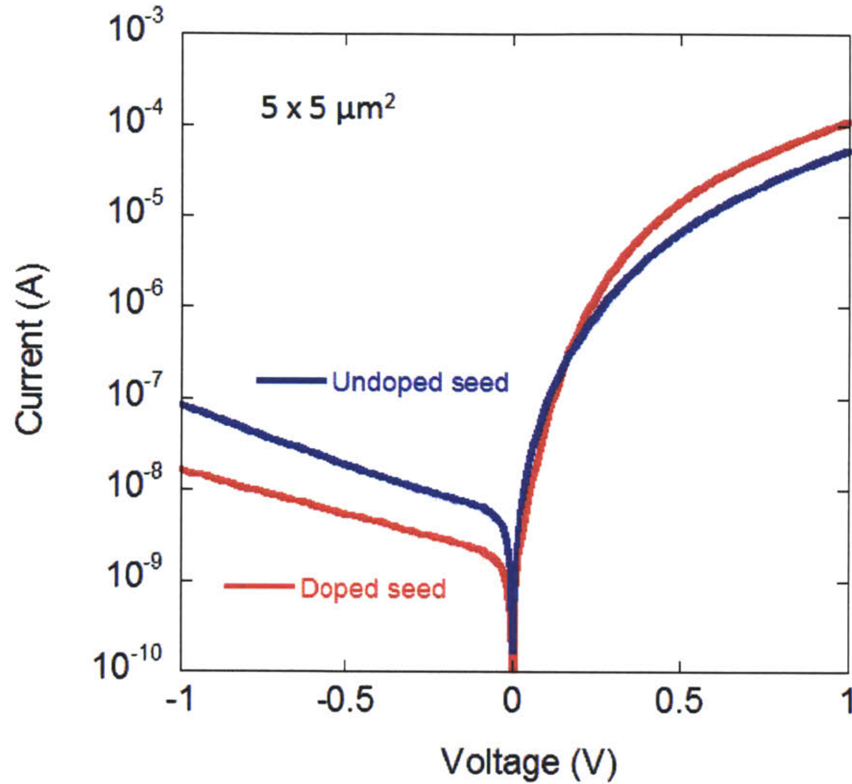

Figure 4-4: Current versus voltage characteristics for 5 x 5 μm devices with a doped and an undoped seed. The inclusion of doping in the seed reduces the dark current by ~5X at -1 V. These devices were passivated with Al_2O_3 and the dopants were activated at 600°C for 10 seconds. The device with the undoped seed is wafer #6444 and the device with the doped seed is wafer #6446.

4.2.1 Electrical characterization of mesa-isolated devices

In the first study, the low temperature germanium seed was grown both with and without *p*-type doping. The effect of this doping can be seen in Figure 4-4. The seed doping serves to reduce the leakage current for a 5 x 5 μm device passived with LTO by ~5X at -1 V. Due to processing difficulties, the yield was very small on larger devices. This is likely because the highly defected region at the Si/Ge interface is incorporated into the *p+* contact region and is not in the body of the device. When left undoped, the defects are in the depletion region of the device and can act as generation centers to contribute to the dark current.

It should be noted that the series resistance of these devices is high (~1 kΩ). This is likely due to the small size of the contact opening. Due to photolithography limitations, the contact via opening is only 1 x 1 μm square, likely leading to a high contact resistance.

In the next study, devices were fabricated with the doped seed and the passivation material was varied. Figure 4-5 shows the current versus voltage characteristics for 10 x 10 μm devices passived with LTO and Al_2O_3. At -1 V, the Al_2O_3 reduces the dark current by ~6X. Larger devices (20 x 20 μm and larger) show a smaller effect of the passivation: at -1 V, the Al_2O_3 reduces the dark current by 2 - 3X. This indicates that the effect of the passivation is mainly around the perimeter of the device. The series resistance for these devices is much better because the contact via is larger than for the 5 x 5 μm device. The contact opening is 6 x 6 μm as compared to 1 x 1 μm.

Figure 4-6 shows the current versus voltage characteristics for 10 x 10 μm devices passivated with Al_2O_3 with different dopant activation anneals. The 550°C activation anneal reduces the dark current by ~3X over the 600°C anneal. This effect ranges from 2 - 5X over all device sizes. It is hypothesized that a higher activation annealling temperature degrades the leakage current because the Al_2O_3 film does not withstand high temperatures very well [71] [72].

Finally, the effect of *n*-type surface doping ($N_d = 3.5 \times 10^{17}$ cm^{-3}) at the top 0.2 μm of the Ge film was studied. Figure 4-7 shows the current versus voltage characteristics for a 10 x 10 μm device passivated with alumina, with dopant activation at 550°C, with and without an *n*- layer at the top of the Ge. The *n*-type layer reduces the dark current by 25% across all device sizes. The *n*- layer reduces the electric field at the surface, resulting in a lower surface generation current.

In summary, the lowest leakage diodes from the mesa isolated process flow can be made by including *p*-type doping of ~2 x 10^{18} cm^{-3} in the Ge seed, passivating the

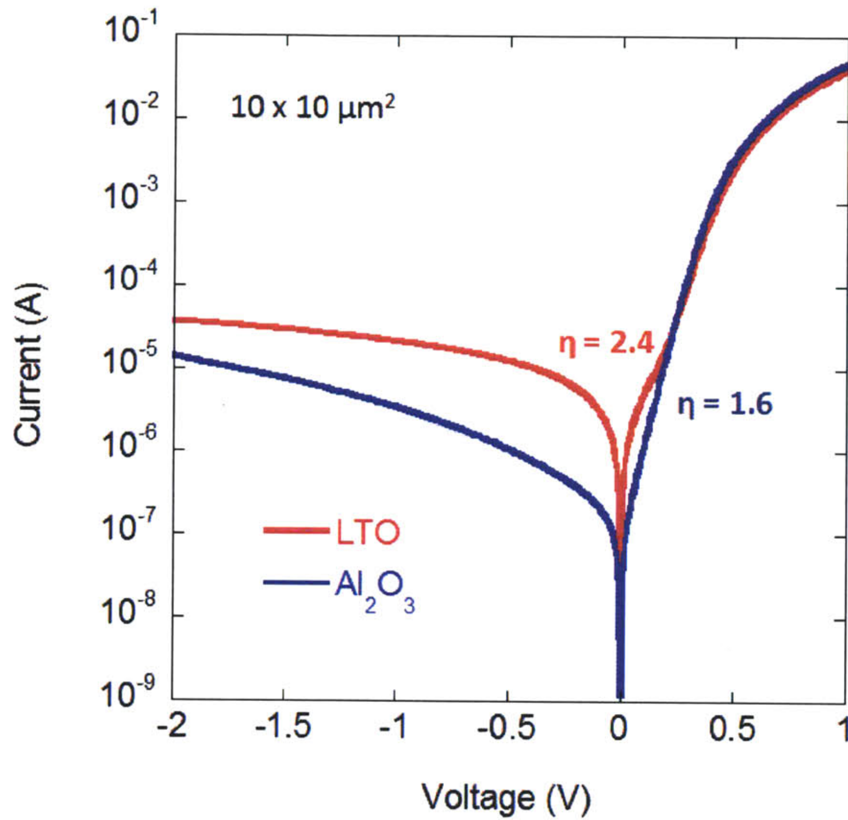

Figure 4-5: Current versus voltage characteristics for 10 x 10 μm mesa-isolated devices with different passivation materials. Using alumina to passivate the diodes reduces the dark current and improves the ideality factor. The dopants were activated at 550°C for 10 seconds. The device passivated with alumina was from wafer #6508 and the device passivated with LTO was from wafer #6505.

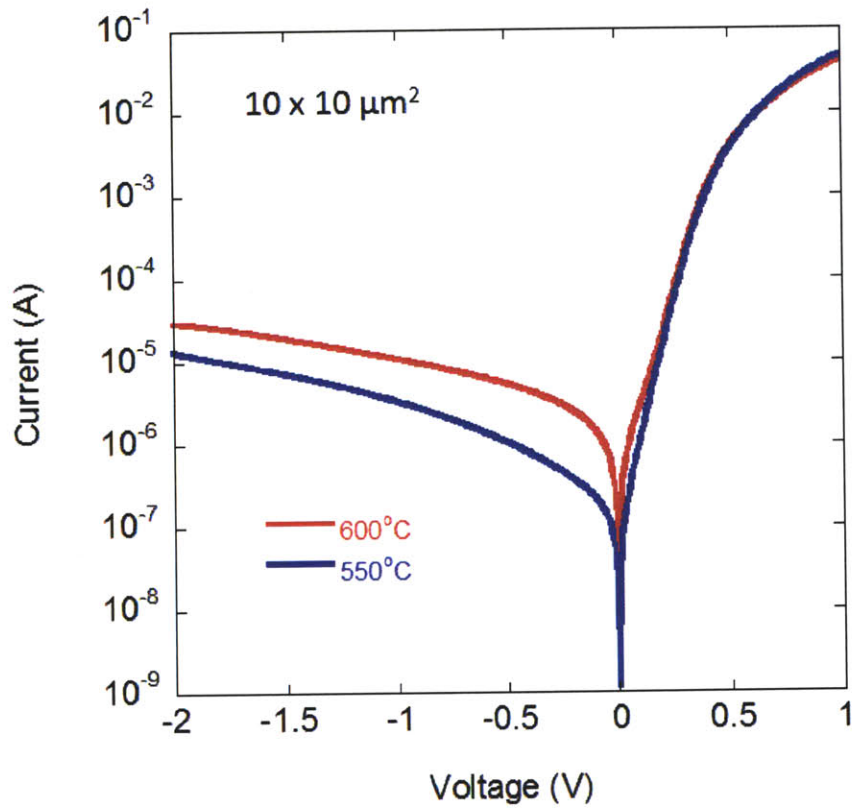

Figure 4-6: Current versus voltage characteristics for mesa-isolated devices passivated with Al_2O_3 with dopants activated at different temperatures. The 550°C anneal results in a lower dark current than the 600°C anneal. The device activated at 550°C was from wafer #6508 and the device activated at 600°C was from wafer #6506.

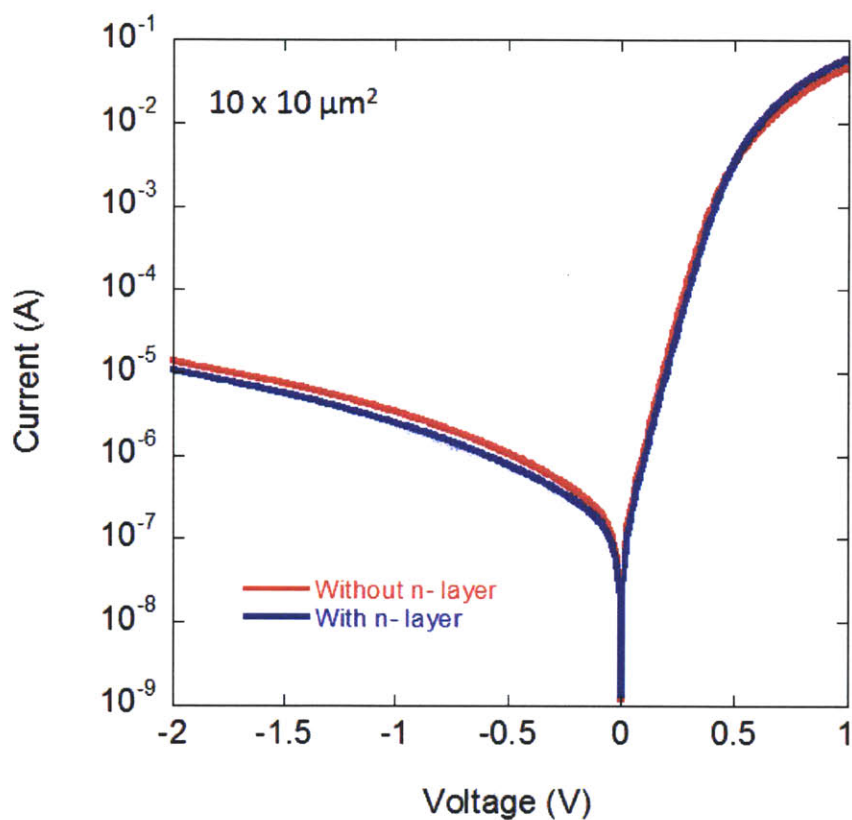

Figure 4-7: Current versus voltage characteristics for mesa-isolated devices with and without an n- layer at the Ge surface. The n- layer reduces the dark current by 25% across all device sizes. The devices were passivated with alumina and activated at 550°. The device with the n- doping was from wafer #6510 and the device without the n- doping was from wafer #6508.

structure with alumina, activating the dopants at 550°C, and including an n- layer at the top of the film to reduce the electric field. A 10 x 10 μm device made with these conditions demonstrated a dark current of 2.5 μA at -1 V.

4.2.2 Electrical characterization of non-mesa isolated diodes

As mentioned earlier, the mesa etch of the germanium film was hard to control. Removing 0.5 μm of germanium in the vertical direction often removed 1 μm of germanium in the lateral direction, making alignment difficult in subsequent steps. Eliminating the mesa etch and relying on n+ doping to isolate the devices fixed this problem.

These wafers were also designed to study the effect of passivation on the leakage current. Figure 4-8 shows the current versus voltage characteristics for 100 x 100 μm devices passivated with both LTO and Al_2O_3. The Al_2O_3 reduces the dark current by ~6X at -1 V. This reduction is consistent for the larger (100 x 100 μm and larger) device sizes. Small devices (20 x 20 μm), however, had problems with large contact resistance, so a comparison is invalid.

To improve the series resistance of the 100 μm square Al_2O_3 device, the wafers were annealed in nitrogen at temperatures ranging from 300°C to 450°C. The LTO devices were included as a control group. The Al_2O_3 devices did not survive these temperatures, as the dark currents often degraded. This is perhaps due to the alumina film's inability to withstand high temperatures. The LTO devices, however, showed significant improvement in dark current.

Effect of a post-metallization anneal on devices passivated with LTO

Figure 4-9(a) shows the current versus voltage characteristics for 10 x 10 μm square devices after a post-metallization anneal (PMA) at various temperatures. Without an anneal, the dark current is roughly 10 μA at -1 V. After an anneal at 400°C, the

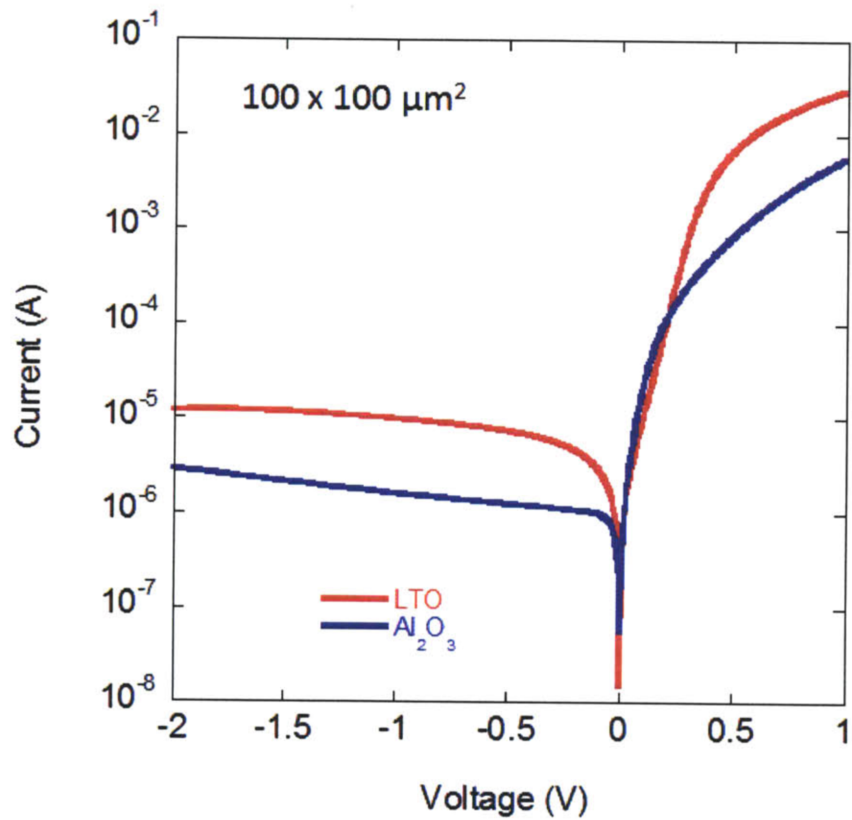

Figure 4-8: Current versus voltage characteristics for devices fabricated without a mesa etch. Both curves are of 100 x 100 μm devices passivated with LTO or Al_2O_3. Passivating the device with Al_2O_3 reduces the dark current by ~6X at -1 V. The device passivated with alumina was from wafer #6595 and the device passivated with LTO was from wafer #6596.

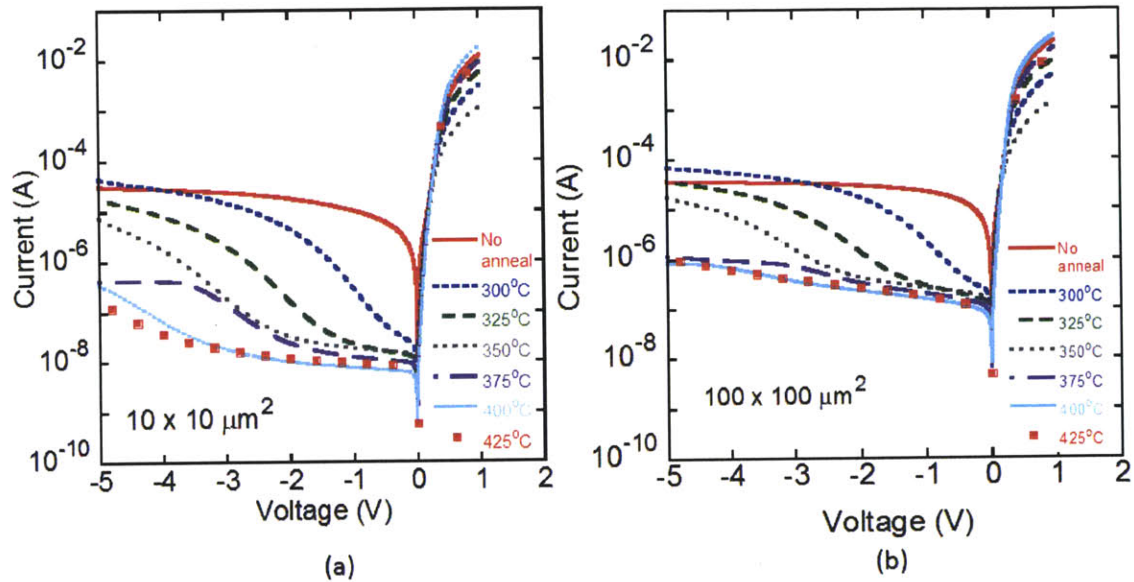

Figure 4-9: Current versus voltage characteristics (a) 10 x 10 μm devices and (b) 100 x 100 μm devices after post-metallization anneals at various temperatures. The anneal reduces the dark current by ~1000X for the 10 x 10 μm device and by ~140X for a 100 x 100 μm device. These devices were passivated with LTO. These devices were all from wafer #6596 with different pieces annealed at different temperatures.

dark current has dropped to 8 nA, roughly a factor of 1000X lower than for diodes without a PMA. Furthermore, the anneal dramatically changes the voltage dependence in reverse bias. The dark current for an unannealed device rises rapidly with increasing applied bias. As the anneal temperature increases, the current increases more gradually with reverse bias. As indicated in Figure 4-9(a), annealing at temperatures higher than 400°C does not yield a significant improvement in the dark current. Annealing at temperatures higher than 425°C caused the contacts to spike and resulted in shorted diodes. A similar investigation of larger devices shows a dark current reduction of ~140X for 100 μm square devices (as shown in Figure 4-9(b)) and ~35X for 300 μm square devices. The difference in dark current reduction factors indicates that the anneal is affecting the perimeter of the devices. Smaller devices have a larger perimeter-to-area ratio and are thus affected more by changing the passivation at the perimeter of the device.

To further study the perimeter and area dependencies of the dark current, the total current was broken down into its perimeter and area components. The total dark current can be expressed as

$$I_{Total} = J_P \times Perimeter + J_A \times Area \tag{4.1}$$

where J_P is the current due to the perimeter of the device and J_A is the perimeter due to the area of the device. Dividing the entire equation by the area of the device yields the following equation.

$$J_{Total} = J_P \times \frac{Perimeter}{Area} + J_A \tag{4.2}$$

When the total current density is plotted against the perimeter/area ratio for a range of different size devices, the slope of the line corresponds to the perimeter component of the leakage current and the y-intercept corresponds to the area component. Figure 4-10 shows the plots of J_{Total} v. $\frac{Perimeter}{Area}$ for both the unannealed and the annealed devices at -1 V. The anneal causes the J_P values to decrease by ~1000X from 2500 μA to 2 μA, further supporting the conclusion that the anneal primarily affects the perimeter of the devices. The fact that J_A is negative for the unannealed devices indicates that the dark current of the unannealed devices does not fit this model very well and another mechanism dominates the dark current.

To investigate the effects of the anneal metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated. The same Ge growth process was used and the wafers underwent the same LTO deposition process and Ti/Al stack processing as the diode wafers. A cross-sectional schematic diagram of the MOSCAPs is shown in Figure 4-11. These capacitors were subjected to PMA in N_2 for 45 minutes at varying temperatures. High-frequency capacitance-voltage (C-V) curves are shown in Figure 4-11. The PMA shifts the flatband voltage to higher voltages, suggesting that the anneal induces a

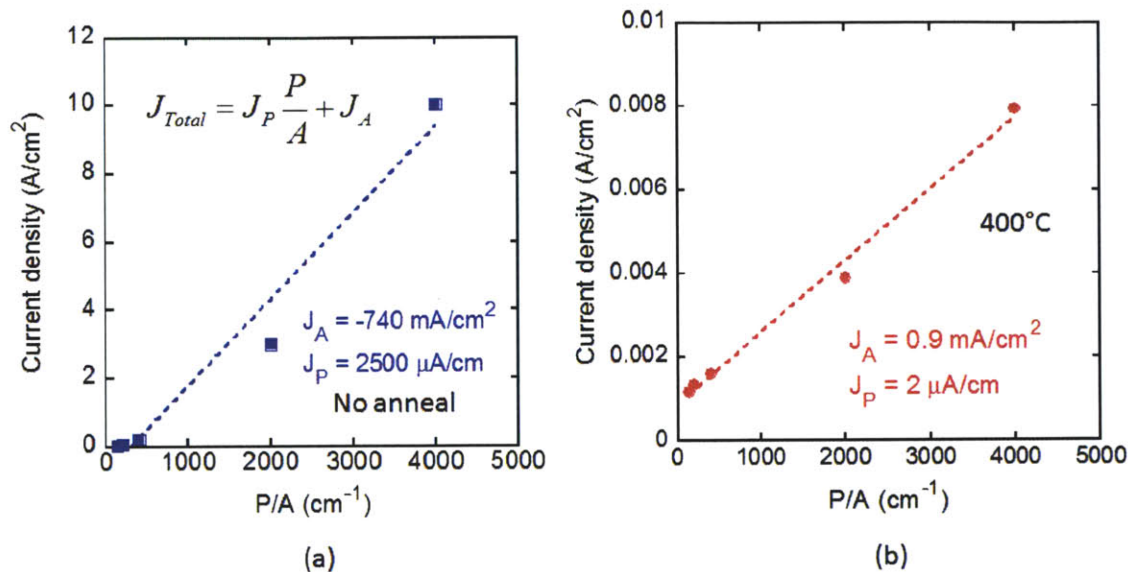

Figure 4-10: Perimeter/area analysis at -1 V for devices (a) without and (b) with a PMA. The anneal decreases the J_P values by ~1000X, indicating that the anneal primarily affects the perimeter of the devices. The J_P and J_A values of both annealed and unannealed devices can be seen in the figure.

negative fixed charge at the LTO/Ge interface. Other ambients were tested as well, as shown in figure 4-12. The shift is consistent in different ambients, indicating that the change in flatband voltage is due to a temperature effect and not an ambient effect.

Without an anneal, the Ge surface is depleted at 0 V. This large depletion region creates a high electric field at the surface and increases the surface recombination velocity, consistent with the large leakage current observed for diodes without the PMA. After an anneal at 400°C, the C-V characteristics indicate that the Ge surface is accumulated with holes at 0 V. This hole charge better isolates the device and reduces the region of high electric field, thereby reducing the dark current. Schematic illustrations of this are in Figure 4-13. It is important to note that the annealed devices will still have a small depletion region around the perimeter of the device due to the accumulated holes and $n+$ implant. This depletion region, however, is much

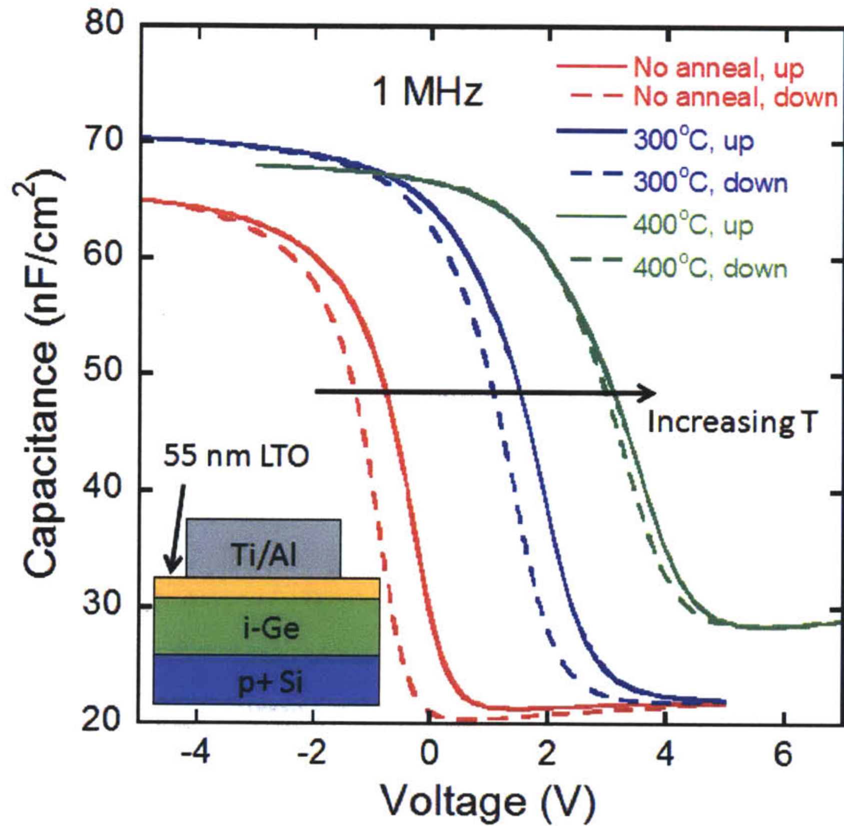

Figure 4-11: Capacitance versus voltage characteristics for 300 x 300 μm devices annealed at different temperatures in N_2. The flatband voltage shifts to the right with increasing temperature and the hysteresis improves slightly. These devices were fabricated on wafer #6725.

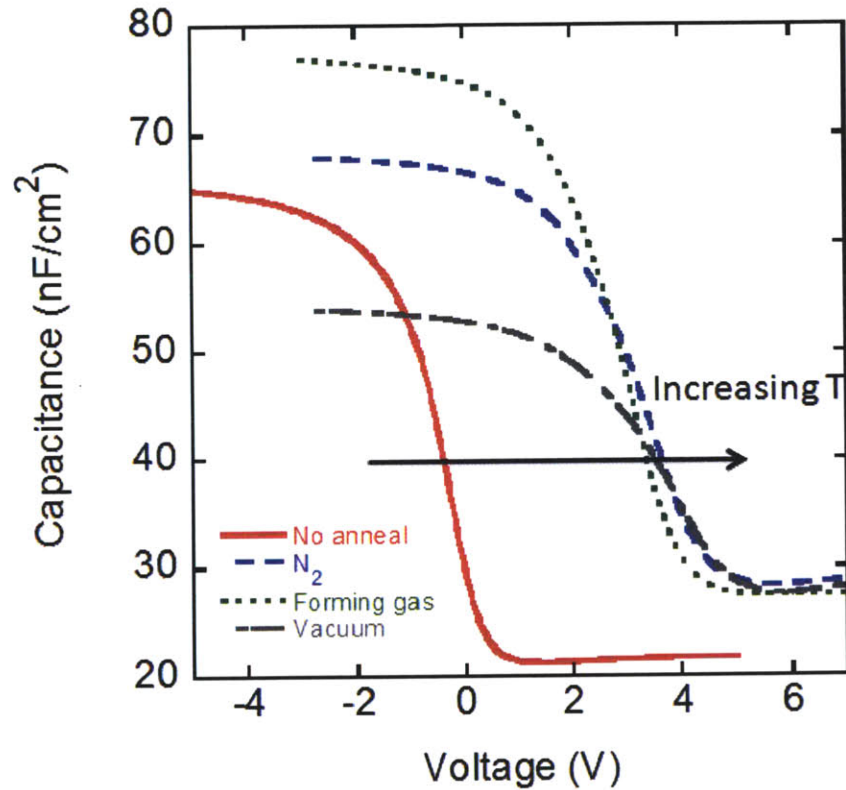

Figure 4-12: Capacitance versus voltage characteristics for 300 x 300 μm devices annealed in different ambients at 400°C. The flatband voltage shift is consistent across all ambients, indicating that the shift is due to temperature and not to ambient. The variation in C_{ox} can be attributed to oxide thickness variation across the wafer. These devices were fabricated on wafer #6725.

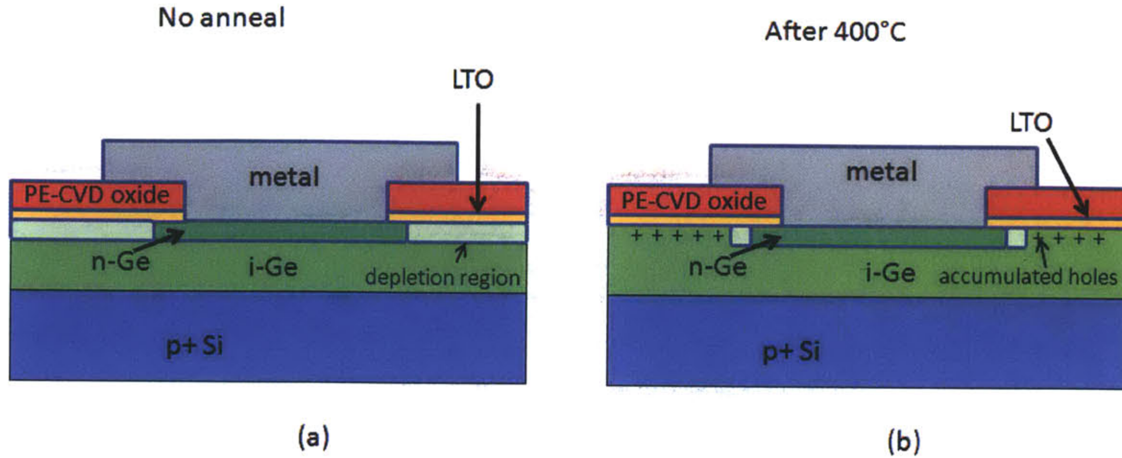

Figure 4-13: Schematic cross-sectional diagrams of the diodes (a) without and (b) with an anneal. Without an anneal, the Ge surface is depleted, causing a high electric field at the surface and a large recombination velocity. The anneal introduces a negative fixed charge at the Ge/LTO interface which attracts holes to the surface of the germanium. These holes better isolate the devices and reduce the depletion region width.

smaller than that in an unannealed device.

The flatband voltage shift from a device without an anneal to a device annealed at 400°C is 3.55 V. Assuming that this shift is entirely due to a change in the fixed charge, ΔQ_f, this corresponds to a $\Delta Q_f = C_{ox} * \Delta V_{FB} = 1.5 \times 10^{12}$ cm^{-2}.

Positive shifts in the flatband voltage with nitrogen, forming gas, or oxygen annealing have been reported for Ge MOS capacitors passivated with GeON [73], Al_2O_3 [74], HfO_2 [75], and a SiO_2/GeO_2 bilayer [76]. These results are consistent with theoretical calculations that dangling bonds in Ge are always negatively charged [77] at the Ge/dielectric interface and that an anneal increases the number of dangling bonds. Using the Berglund method [78], the interface state density (D_{it}) of the devices in this work was found to be in the 2 - 4 x 10^{12} cm^{-2} eV^{-1} range at the flatband voltage. There is a slight increase in D_{it} upon annealing. This increase in D_{it} does not have a deleterious effect on the diodes, though, because the effect is small compared to the effect of the increased fixed charge.

To confirm that the anneal draws holes to the surface, diodes were fabricated from germanium which was *in-situ* doped *p*-type with B_2H_6 at the end of the growth. This caused the top 0.2 μm to be doped to ~5 x 10^{17} cm^{-3}. The goal of this was to intentionally introduce holes at the interface to compensate for the depletion region. A cross-sectional schematic diagram of this device can be seen in Figure 4-14(b).

Figure 4-14(a) shows the current versus voltage characteristics for an unannealed device without any *p*-type doping at the top of the germanium, an unannealed device with *p*-type doping at the top of the germanium, and an annealed device with *p*-type doping at the top of the germanium. The devices were all 5 x 5 μm. The *p*-type doping reduces the dark current at low biases by ~400X. Furthermore, the PMA does not reduce the dark current by a significant amount, indicating that the PMA introduces fewer holes than 5 x 10^{17} cm^{-3}. This is further supported by the fact that the dark current takes on a steep slope around -1 V. For devices that just received a PMA (like those in Figure 4-9(a)), the steep slope does not start until around -3 V. This steep slope is likely the result of a tunneling effect due to a high electric field. Since the doping introduces more holes, there will be a higher built-in electric field and it will require a lower bias to induce tunneling. This tunneling current will be discussed in greater detail in Chapter 5.

Reproducibility

The consistency of results from run to run was excellent. The diode wafers and MOSCAP wafers above were fabricated months apart, indicating that these results are robust and reproducible. To ensure the reproducibility of the diode results, the same process was done approximately one year after the original results were found. Figure 4-15 shows the current versus voltage characteristics for 10 x 10 μm and 100 x 100 μm devices fabricated in these two different runs. "Run A" is the early run and "Run B" is the later run. The dark current curves are nearly identical with the

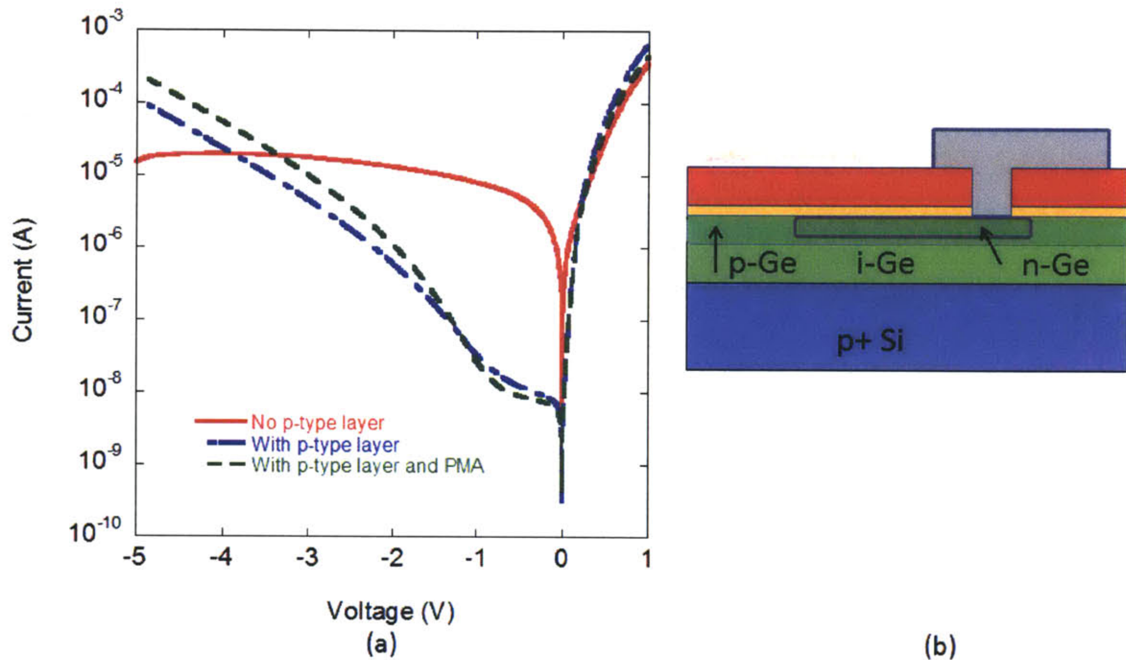

Figure 4-14: (a) Current versus voltage charcteristics for 5 x 5 μm devices with different PMA and *p*-type doping characteristics. (b) A cross-sectional schematic diagram of a device doped *in-situ* *p*-type at the surface. The *p*-type doping reduces the dark current by ~400X as compared to an unannealed device without any *p*-type doping. When the doping is present at the top of the germanium, a PMA does not have a large effect. The device grown without a *p*-type layer was from wafer #6881 and the devices grown with a *p*-type layer were from wafer #6610.

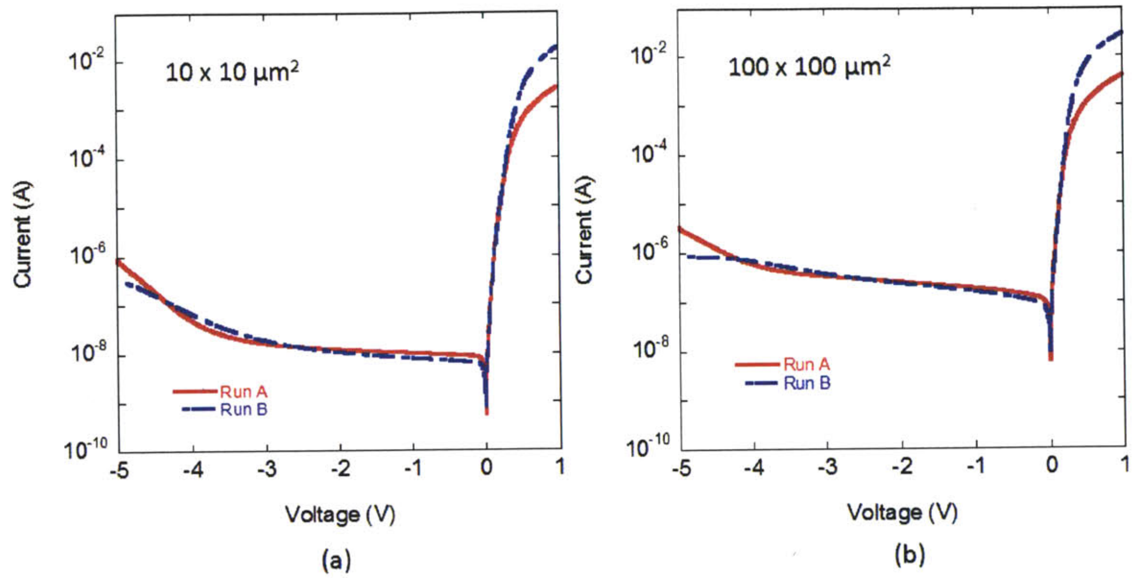

Figure 4-15: Current versus voltage characteristics for (a) 10 x 10 μm devices and (b) 100 x 100 μm devices fabricated in different runs. These devices were passivated with LTO and received a PMA at 400°. The dark current characteristics are nearly identical for these runs, indicating that the results are reproducible and consistent. The device fabricated in Run A was from wafer #6596 and the device fabricated in Run B was from wafer #6881.

only appreciable difference being the series resistance. It seems that the later run has a better series resistance which is most likely due to better simulation of the ion implant because the screen oxide thickness was more consistent among wafers. These results show that the effect of the fixed charge is consistent for the materials available and has a large effect on the dark current.

4.3 Photoresponse of diodes fabricated from blanket Ge-on-Si

The photoresponse of both the mesa-isolated and non-mesa isolated devices was tested. Details of the photoresponse measurement and calibration procedure can be found in Appendix B. The photoresponse of both types of devices are similar,

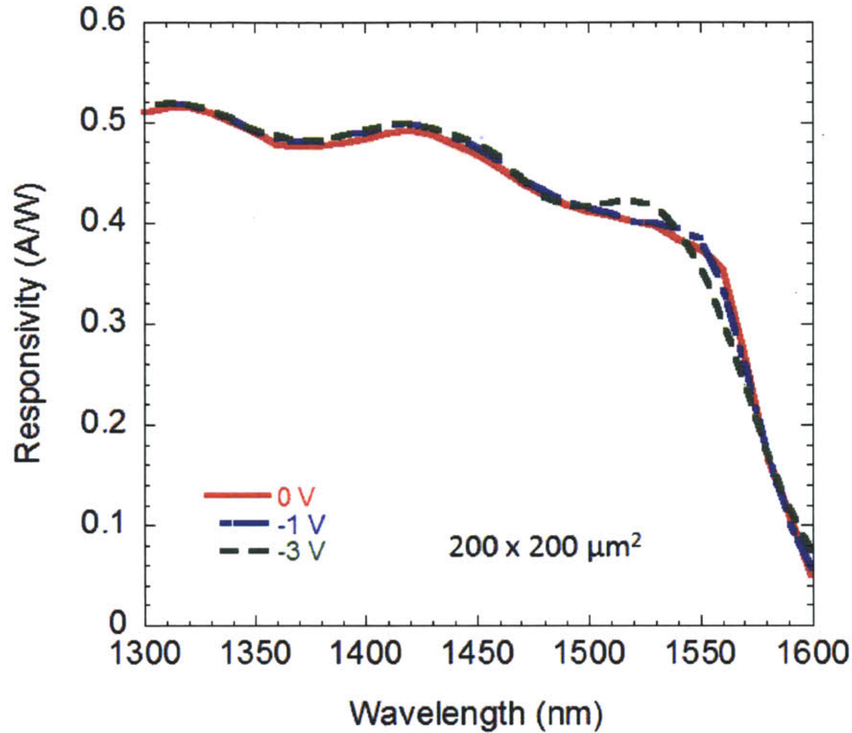

Figure 4-16: Photoresponse versus wavelength characteristic for a 200 x 200 μm device passivated with Al_2O_3 and fabricated with a mesa etch. The lack of a voltage dependence indicates a high internal electric field. At 1300 nm, the responsivity is 0.51 A/W. At 1550 nm, it has fallen to 0.36 A/W. This device did not receive a PMA. This device was from wafer #6508.

indicating that the PMA does not have much effect on the photoresponse.

Figure 4-16 shows the photoresponse versus wavelength characteristic for a 200 x 200 μm mesa-isolated device. The device was passivated with Al_2O_3. At 1300 nm, the photoresponse is 0.51 A/W. At 1550 nm, the photoresponse falls to 0.36 A/W. The photoresponse does not depend much on voltage, indicating a large internal electric field at 0 V. The photoresponse was similar for mesa-isolated devices passivated with LTO.

Figure 4-17 shows the photoresponse versus wavelength characteristic for a 20 x 20 μm non-mesa isolated device. This device was passivatd with LTO and saw a PMA at 400° in N_2 for 45 minutes. At 1300 nm, the photoresponse is 0.44 A/W and it falls

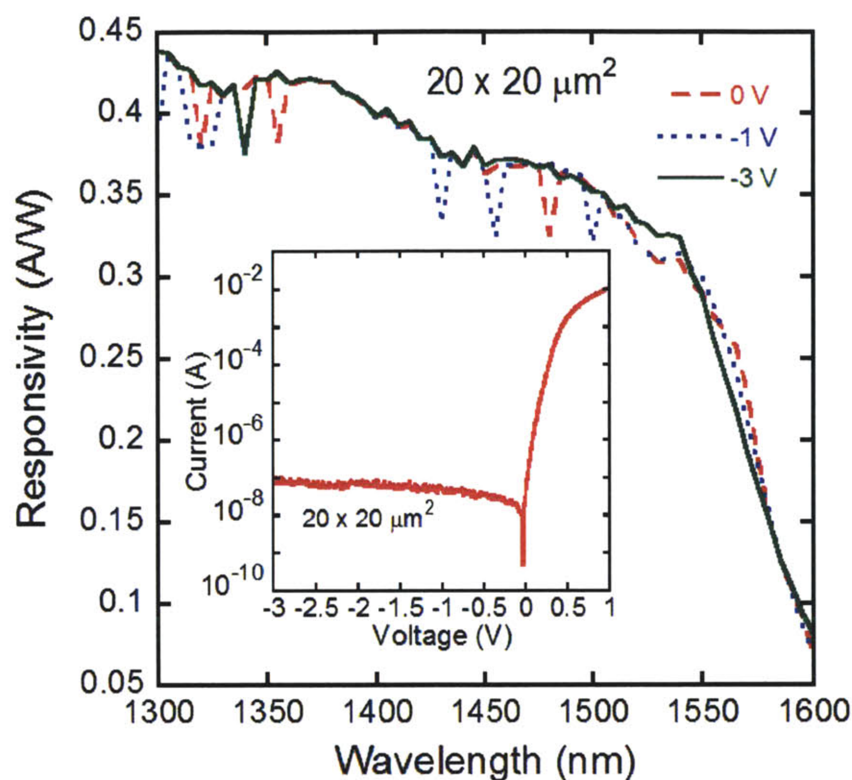

Figure 4-17: Responsivity versus wavelength curve for a device fabricated without mesa isolation. This is a 20 x 20 μm device passivated with LTO and subjected to a PMA at 400°C for 45 minutes. The curve shows comparable photoresponse to the mesa-isolated device. Inset: dark current of the device. This device was fabricated from wafer #6596.

to 0.30 A/W at 1550 nm. Again, there is not much voltage dependence, indicating a large internal electric field. The inset to figure 4-17 shows the current versus voltage characteristic for this device. The dark current at -1 V is ~30 nA.

A 200 x 200 μm device passivated with LTO and with a PMA was also measured. The responsivity of this device was comparable to the 200 μm device shown in Figure 4-16, indicating that the mesa-etch does not effect the photoresponse. At 1300 nm, the responsivity was 0.52 A/W and at 1550 nm, it was 0.40 A/W. A comparison of the photoresponse of the device in Figure 4-16 and a 200 x 200 μm device fabricated in blanket Ge-on-Si that received a PMA can be seen in Figure 4-18. The curves are nearly identical, indicating that the PMA does not substantially effect the residual

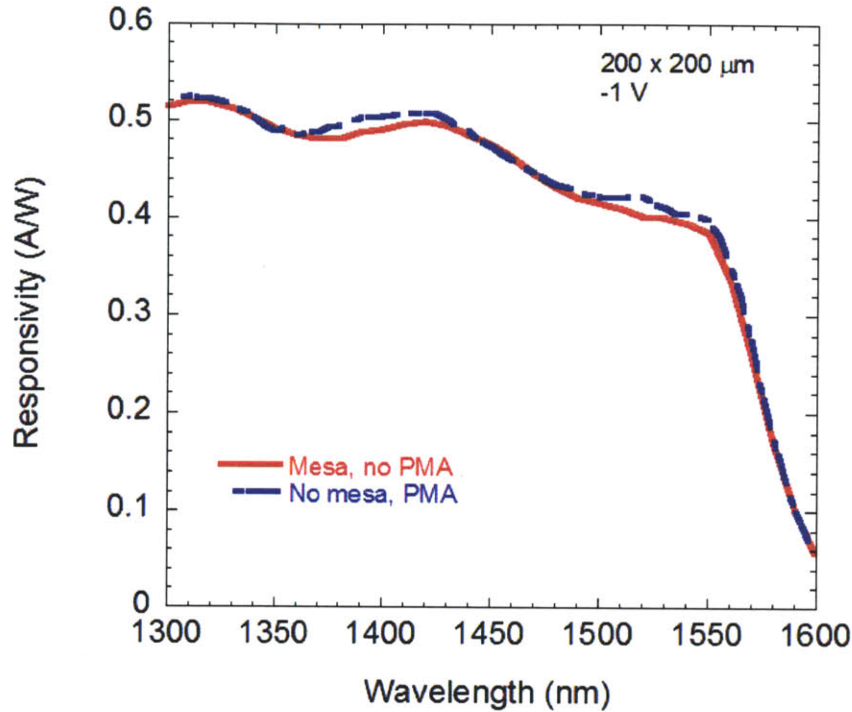

Figure 4-18: Responsivity versus wavelength curves for 200 x 200 μm devices measured at -1 V. The solid red curve was measured on a device that was mesa isolated and did not receive a PMA. The dashed blue curve was measured on a device that did not receive a mesa etch but that did receive a PMA. The nearly identical curves indicate that the PMA does not change the residual tensile strain in the films after growth. The device fabricated with a mesa etch was from wafer #6508 and the device fabricated without a mesa etch was from wafer #6881.

tensile strain present in the films after growth. The dark currents of these devices at -1 V are 0.70 μA for the device with the PMA and 18 μA for the device without the PMA.

4.4 Chapter summary

This chapter discussed the fabrication, electrical characterization, and optical characterization of germanium photodiodes fabricated from a blanket Ge-on-Si growth process. It was found that mesa-isolated devices were problematic due to the uncontrolled nature of the wet etch. This caused processing problems which probably

also increased the dark current of the devices. To solve this problem, the process was modified to eliminate the mesa etch. Devices fabricated without the mesa etch demonastrated a reduction in dark current. However, a much larger improvement occurred when these devices were annealed after metallization. MOSCAP measurements show that the anneal changes the fixed charge at the Ge/oxide interface, which better isolates the device and reduces the dark current.

Finally, optical measurements of both types of devices show that the photoresponse is roughly the same, indicating that the anneal does not have much effect on the optical properties of the film.

Chapter 5

Dark current leakage mechanisms

In this chapter the mechanisms that are responsible for the leakage current in the diodes fabricated from blanket Ge-on-Si are explored. Both annealed and unannealed devices are analyzed. For the purposes of this chapter an "annealed" device is one annealed at 400°C for 45 minutes and an "unannealed" device is one that did not receive a post-metallization anneal (PMA). The scaling behavior and temperature dependence of the dark current of these devices and simulations performed in Sentaurus Device are presented.

5.1 Overview of dark current mechanisms

There are four main sources of reverse bias leakage current in diodes. These have been studied by others and details can be found in [79, 80]. A short overview will be given here.

The first source of leakage current is due to the diffusion of minority carriers in the quasi-neutral regions of the device. This component is given by

$$J_{diffusion} = qD_n \frac{n_i^2}{N_A L_n}[exp(\frac{qV}{kT}) - 1] \tag{5.1}$$

where q is the charge of an electron, D_n is the diffusion constant of electrons, n_i is the intrinsic carrier density, N_A is the concentration of acceptors, and L_n is the diffusion length of electrons given by $\sqrt{D_n \tau}$ where τ is the minority carrier lifetime. In reverse bias, this equation simplifies to

$$J_{diffusion} = qD_n \frac{n_i^2}{N_A L_n} \tag{5.2}$$

That is, the leakage current is constant with constant doping and temperature. As a function of temperature, the dominant temperature dependence of the diffusion current is proportional to $e^{(-E_g/kT)}$, where E_g is the bandgap of the material. This temperature dependence is due to the n_i^2 term. The intrinsic carrier concentration can be writted as

$$n_i = N_s exp(\frac{-E_g}{2kT}) \tag{5.3}$$

where N_s is the density of states and the other variables are defined as before. Diodes that are dominated by this form of leakage current are very high quality with good passivation.

The second form of leakage current is due to generation of carriers in the depletion region defined by the metallurgical junction. This mechanism can be described by

$$J_{bulk} = qW \frac{n_i}{\tau_g} [exp(\frac{qV}{2kT}) - 1] \tag{5.4}$$

where all constants are defined as before and W is the width of the depletion region and τ_g is the minority carrier generation lifetime. When a reverse bias is applied to the device, the depletion region will grow and the leakage current will increase. The extent to which the current increases is defined by how the depletion region grows, which in turn is dependent on the doping profile. For a diode with constant doping, the depletion region grows as a function of V^α where $\alpha = \frac{1}{2}$. For a

linearly graded doping profile, the depletion region grows as a function of V^{α} where $\alpha = \frac{1}{3}$. For devices with a doping profile in between, the voltage dependence will be in between $\frac{1}{3}$ and $\frac{1}{2}$.

For diodes with leakage current dominated by the generation of carriers in the bulk, there is also a temperature dependence of the dark current. For these devices, an exponential dependence on $\sim \frac{E_g}{2}$ is expected due to the n_i term.

The third form of leakage current is generation of carriers at the surface of the semiconductor. It should be noted that this is different from the generation of carriers in a depletion region at the surface. This current is due to electrically active states at the semiconductor/insulator interface. The equation for this current can be written as

$$J_{surface} = qS_0 n_i [exp(\frac{qV}{2kT}) - 1] \tag{5.5}$$

where S_0 is the surface recombination velocity and is proportional to the interface trap concentration and the other variables are the same as before. In reverse bias, this current has no dependence on voltage (*i.e.* $\alpha = 0$). As a function of temperature, however, devices dominated by this mechanism will show a dominant exponential dependence on $\sim \frac{E_g}{2}$.

The fourth source of leakage current in diodes is tunneling and field assisted emission. Current due to these effects can vary widely depending on the exact mechanism at work. The general electric field dependence of these types of leakage currents can be written as

$$J_{tunnel} \propto exp(E^x) \tag{5.6}$$

where E is the electric field and x is a fitting parameter.

Figure 5-1 is a schematic representation of where these types of leakage currents

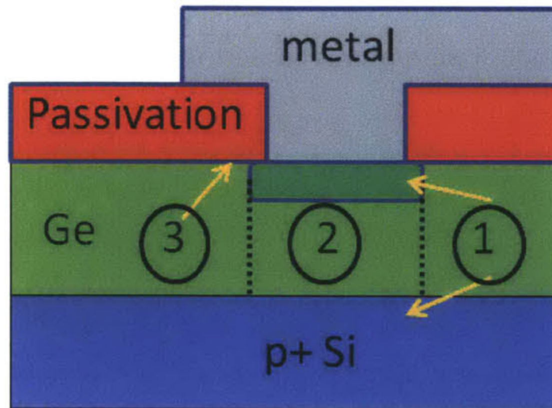

Figure 5-1: A schematic diagram of where the different sources of leakage current originate. (1) refers to the quasi-neutral regions where diffusion current originates. (2) refers to the depletion region of the device where generation of minority carriers occurs. (3) refers to the semiconductor/insulator interface, also the source of generation of minority carriers.

originate for the devices in this thesis. The regions labeled with a "1" indicate the quasi-neutral regions where diffusion current occurs. The region labeled with "2" indicate the depletion region in the bulk of the device where carrier generation occurs. The region labeled with "3" indicates the surface where surface generation occurs. Tunneling and field assisted emission can occur both in the bulk and at the surface and have been omitted from the figure for clarity.

5.2 Experimental scaling and temperature dependencies

To investigate the mechanisms behind the leakage current in the diodes fabricated from blanket Ge-on-Si films, the scaling, voltage, and temperature dependencies were all investigated for annealed and unannealed devices.

5.2.1 Scaling and voltage dependence of devices

Investigating how the dark current scales with different sizes was the first step to exploring the mechanisms. Only square diodes were available on the mask set utilized. Figure 5-2 shows the dark current for unannealed devices scaled by both the perimeter and the area of the devices. It is clear from the figure that the dark current of these devices does not scale with the area. Furthermore, the larger devices may be scaling with perimeter, although it is not a strong dependence. The smaller devices do not scale with anything. This indicates that unannealed devices are not dominated by diffusion or by generation current in the depletion region since both of these would scale with area.

Figure 5-3 shows the dark current scaled by perimeter and area for the annealed devices. From this figure, it is clear that the small devices scale with the perimeter and the large devices scale with the area of the device. This indicates that the large devices may be dominated by diffusion current or generation in the bulk while the small devices are dominated by a different effect. This is likely due to the sizes of the devices. The larger devices have small perimeter/area ratios and will be dominated by an area effect. The smaller devices have large perimeter/area ratios and will be dominated by a perimeter effect. All sized devices will have both effects, but they will be more or less pronounced based on the size of the device.

Temperature-dependent current versus voltage measurements were also taken. The devices were cooled using a liquid nitrogen source and current versus voltage curves were taken at seven different temperatures for two different device sizes. For some devices at lower temperatures, the current values were below the noise level of the parameter analyzer ($\sim 10^{-13}$ A). In that case, the data has not been shown.

Figure 5-4 and Figure 5-5 show the temperature-dependent current versus voltage

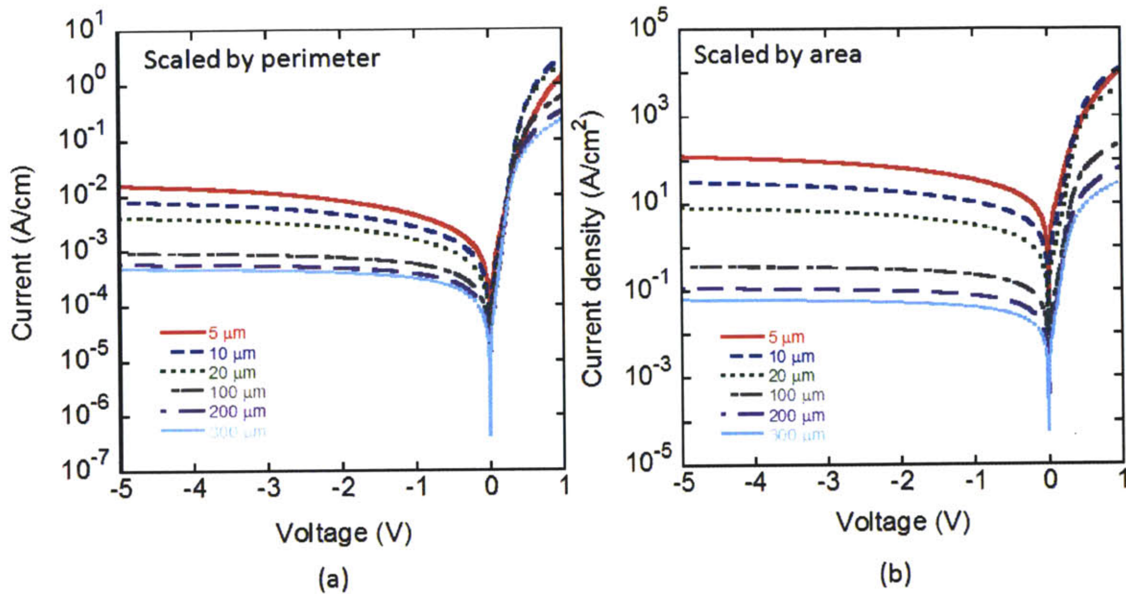

Figure 5-2: Current versus voltage characteristics scaled by (a) perimeter and (b) area for unannealed diodes. The larger devices scale with perimeter while the smaller devices do not scale at all. These measurements were all taken on devices fabricated on wafer #6596.

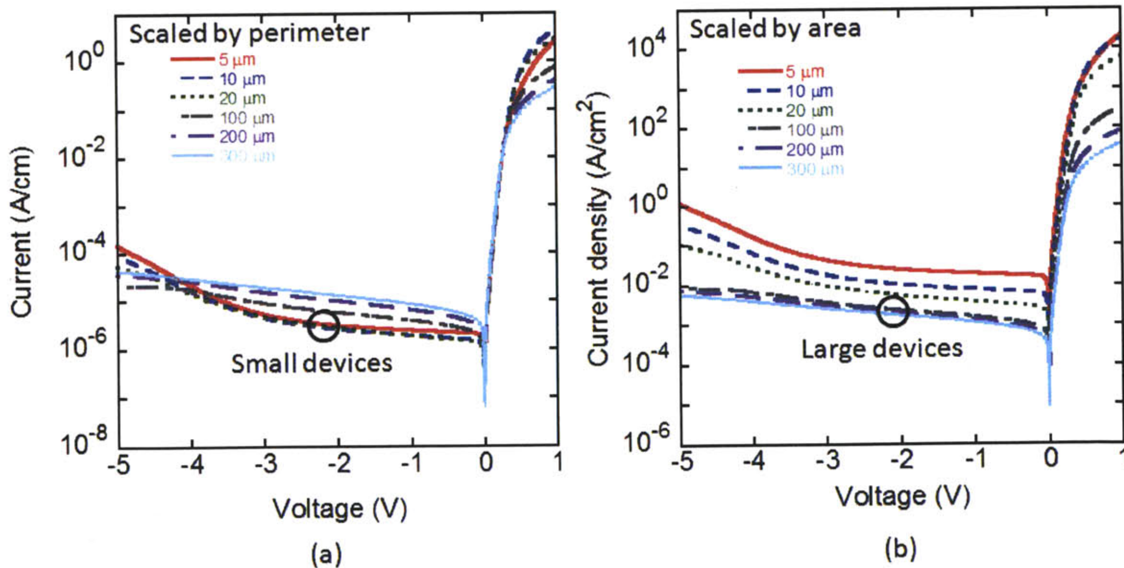

Figure 5-3: Current versus voltage characteristics scaled by (a) perimeter and (b) area for annealed diodes. The larger devices scale with area while the smaller devices scale with perimeter. This apparent difference is likely due to the difference in perimeter/area ratios of the different devices. These measurements were all taken on devices fabricated on wafer #6596.

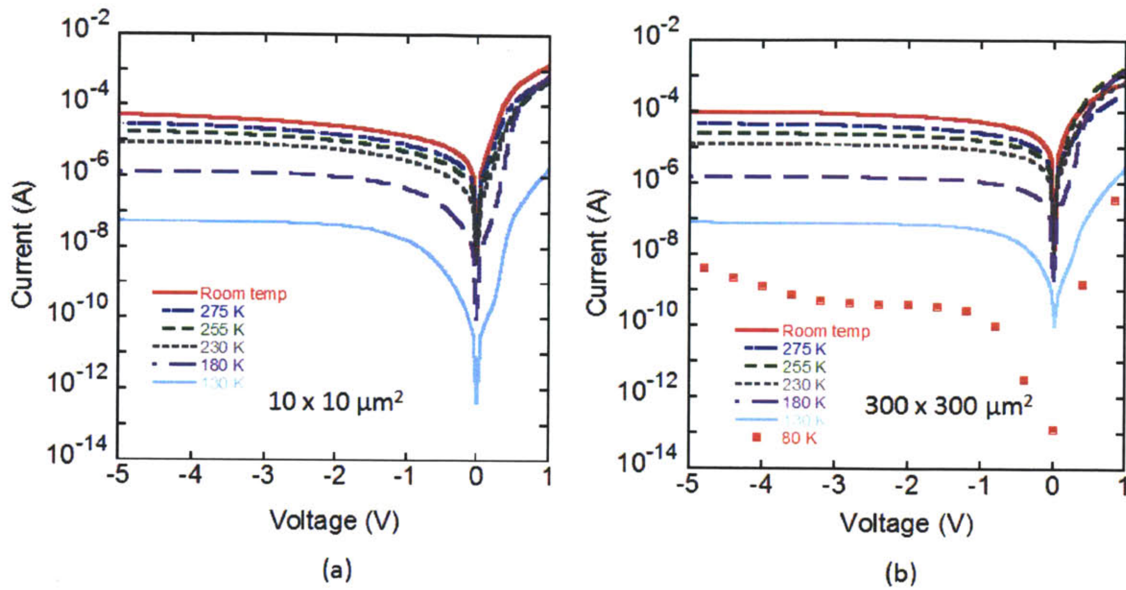

Figure 5-4: Current versus voltage characteristics at different temperatures for (a) a 10 x 10 μm device and (b) a 300 x 300 μm device on an unannealed wafer. Both sizes demonstrate an activation energy of the dark current at -1 V of 0.12 eV. These measurements were all taken on devices fabricated on wafer #6596.

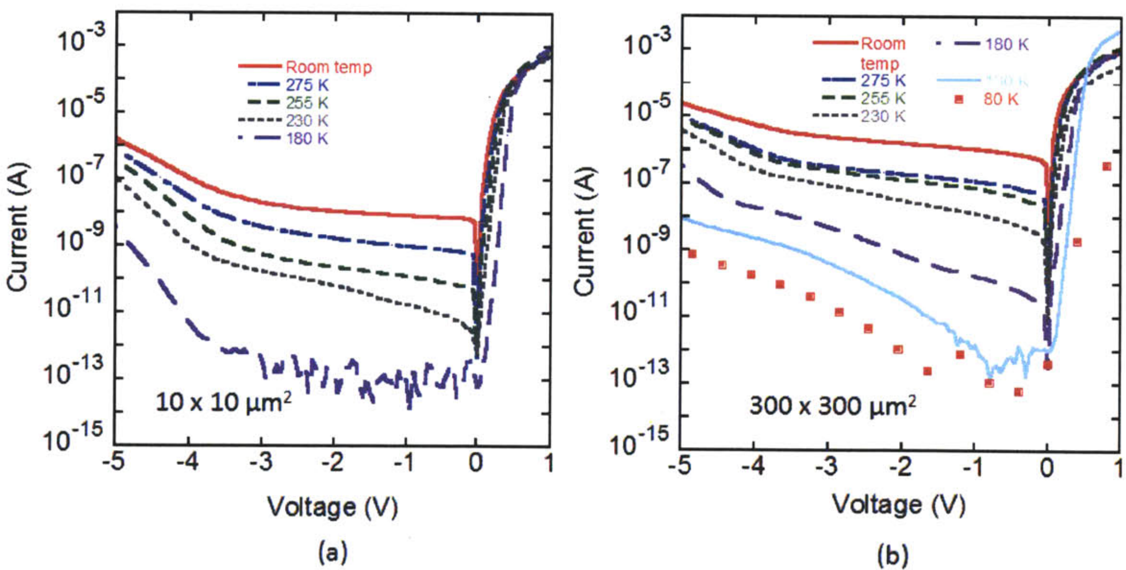

Figure 5-5: Current versus voltage characteristics at different temperatures for (a) a 10 x 10 μm device and (b) a 300 x 300 μm device on an annealed wafer. The 10 x 10 μm device has an activation energy of 0.54 eV at -1 V while the 300 x 300 μm device has an activation energy of 0.33 eV. These measurements were all taken on devices fabricated on wafer #6596.

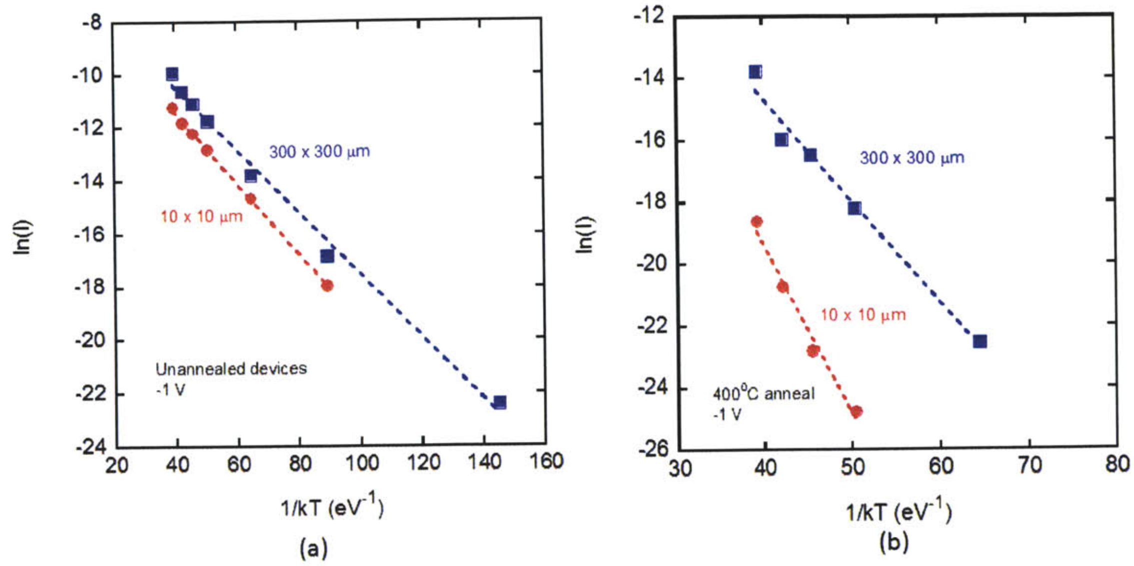

Figure 5-6: Activation energy extraction for (a) unannealed devices and (b) annealed devices. The activation energies for the unannealed devices was 0.12 eV. The activation energy for large annealed devices was 0.33 eV and for small annealed devices was 0.54 eV. These measurements were all taken on devices fabricated on wafer #6596.

curves for both unannealed devices and annealed devices of two different sizes. From Figure 5-4, it is shown that the current is weakly temperature at higher temperatures and does not decrease significantly until below 230 K. Furthermore, extracting the activation energy at -1 V yields a value of 0.12 eV for both devices. This activation energy is consistent with tunneling or field-assisted emission as the source of dark current. The plot used to extract the activation energy can be seen in Figure 5-6(a).

Figure 5-5 shows different behavior. The IV curves are well-spaced as a function of temperature. Extracting the activation energy of these devices yields two different values: 0.54 eV for the 10 x 10 μm device and 0.33 eV for the 300 x 300 μm device. The activation energy of the larger device matches the value of half of the bandgap for germanium, possibly indicating the presence of minority carrier generation in the bulk. The plots used to extract the activation energies can be seen in Figure 5-6(b).

The final piece of analysis that was done on these devices was to extract the voltage dependence of the IV curve in reverse bias. By taking the natural log of both

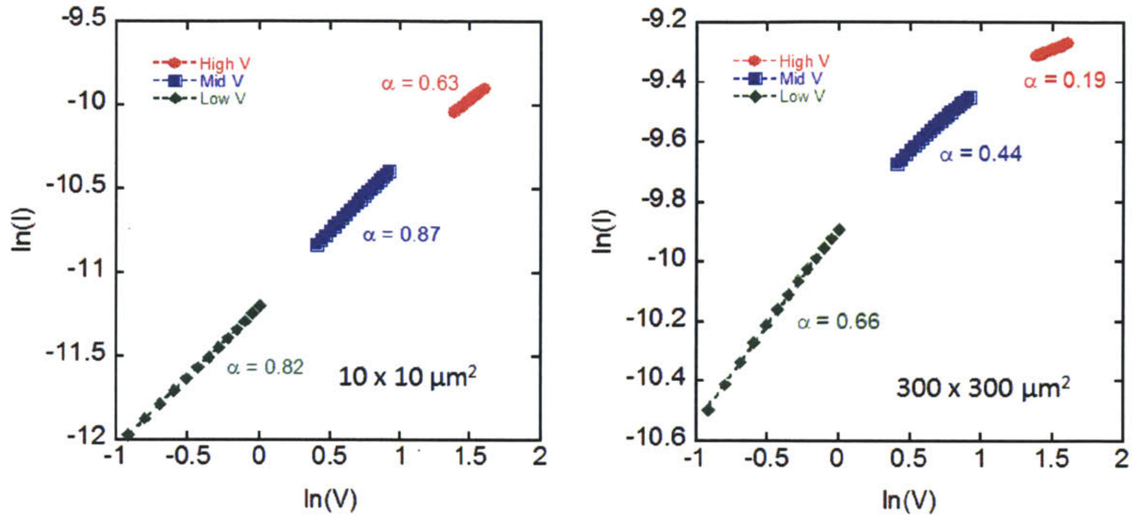

Figure 5-7: The natural log of the current v. the natural log of the voltage for a (a) 10 x 10 μm device and a (b) 300 x 300 μm device from an unannealed wafer. At low biases, the value of α is 0.82 for the small device and 0.66 for the large device. This analysis was done on devices fabricated on wafer #6596.

the current and the voltage and fitting the points to a line, the power dependence of the voltage, or α can be extracted. For these devices α should be in between $\frac{1}{3}$ (the value for a linearly graded doping profile) and $\frac{1}{2}$ (the value for a constant doping profile).

Figure 5-7 shows the α extraction for the unannealed devices. The "low V" range is defined as -0.4 to -1 V, the "mid V" range is defined as -1.5 to -2.5 V, and the "high V" range is defined as -4 to -5 V. The figure shows that, at low voltages, the value of α is slightly different for the two different sizes: 0.82 for a 10 x 10 μm device and 0.66 for a 300 x 300 μm device. Both values are higher than 0.5, indicating that the dominant leakage mechanism is not bulk generation of carriers in the depletion region.

Figure 5-8 shows the α extraction for the annealed devices. The voltage ranges are defined as before. These devices show very different behavior. The 10 x 10 μm device has α = 0.15 while the 300 x 300 μm device has α = 0.39. These values are much lower than the values for the unannealed devices, indicating an entirely different

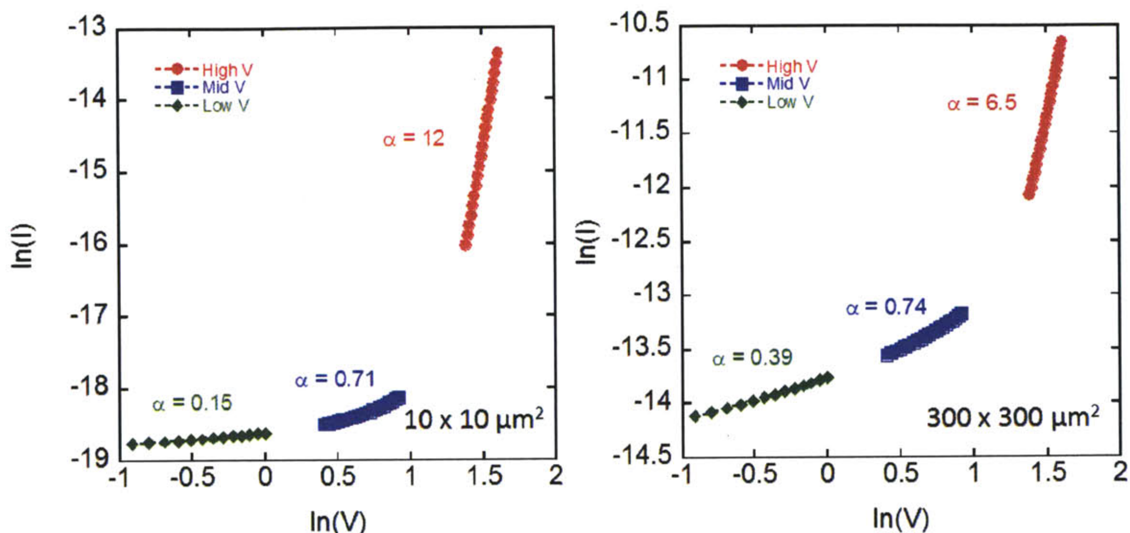

Figure 5-8: The natural log of the current versus the natural log of the voltage for a (a) 10 x 10 μm device and a (b) 300 x 300 μm device from an annealed wafer. At low biases, the value of α is 0.15 for the small device and 0.39 for the large device. This analysis was done on devices fabricated on wafer #6596.

mechanism for the source of the dark current.

5.2.2 Summary of scaling and voltage dependencies

Table summarizes the scaling dependencies, activation energies, and voltage dependencies of large and small devices on both unannealed and annealed wafers in reverse bias.

Table 5.1: Summary of device dependencies. A "small" device measures 10 x 10 μm and a "large" device measures 300 x 300 μm.

Device description	Current scaling	Activation energy at -1 V (eV)	Voltage dependence (α) at low bias
Small, unannealed	None	0.12	0.82
Large, unannealed	Perimeter	0.12	0.66
Small, annealed	Perimeter	0.54	0.15
Large, annealed	Area	0.33	0.39

The large annealed devices show characteristics that match perfectly with the

characteristics of leakage current that is dominated by bulk generation in the depletion region. The small annealed devices will also have generation of carriers in the depletion region, but their α dependence and scaling dependence indicate that there is another mechanism at work. The α of 0.15 indicates that the other mechanism is most likely surface generation current. This is supported by the fact that the dark current scales with the perimeter of the devices.

The unannealed devices have activation energies that do not match either the bandgap nor half of the bandgap. Furthermore, the values of α are larger than what one would expect for current dominated by generation in the bulk. Thus, the dark current of these devices may be dominated by tunneling (*e.g.* band-to-band tunneling or trap assisted tunneling) or some field assisted emission. This is most likely due to the large depletion region at the surface of the Ge, as indicated by the MOSCAP measurements in Chapter 4.

5.3 Modeling of annealed devices

To confirm the dominant dark current mechanisms, the devices were modeled in Sentaurus Device. The most straightforward device to model was the large annealed device. The hypothesis is that the dark current is dominated by generation of minority carriers in the depletion region. This is responsible for the $\alpha = 0.39$ dependence and the activation energy of 0.33 eV. To model the device, it is necessary to get an accurate doping profile of the p-type autodoping. Spreading resistance profiling was done on the samples, seen in Figure 5-9, and the profile was imported into Sentaurus Device. Shockley-Read-Hall recombination/generation models were activated and a lifetime of 0.2 μs was used. A cross-section of the device used in the simulation can be seen in Figure 5-10.

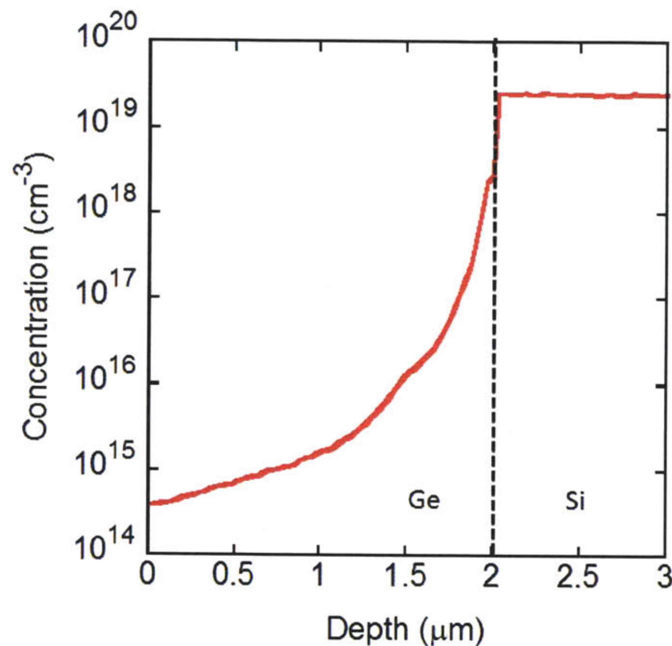

Figure 5-9: Spreading resistance profiling of boron in the germanium film. The autodoping from the seed layer causes the top of the germanium film to be doped ~5 x 10^{14} cm^{-3}. This analysis was done on devices fabricated on wafer #6596. Analysis courtesy of Solecon Laboratories.

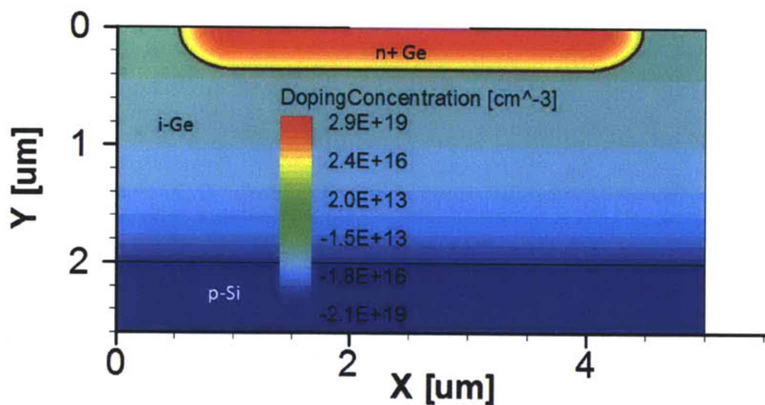

Figure 5-10: Cross-sectional diagram of device modeled in Sentaurus Device. The p-type doping profile was imported from the spreading resistance profiling and the n-type doping was estimated using a gaussian distribution.

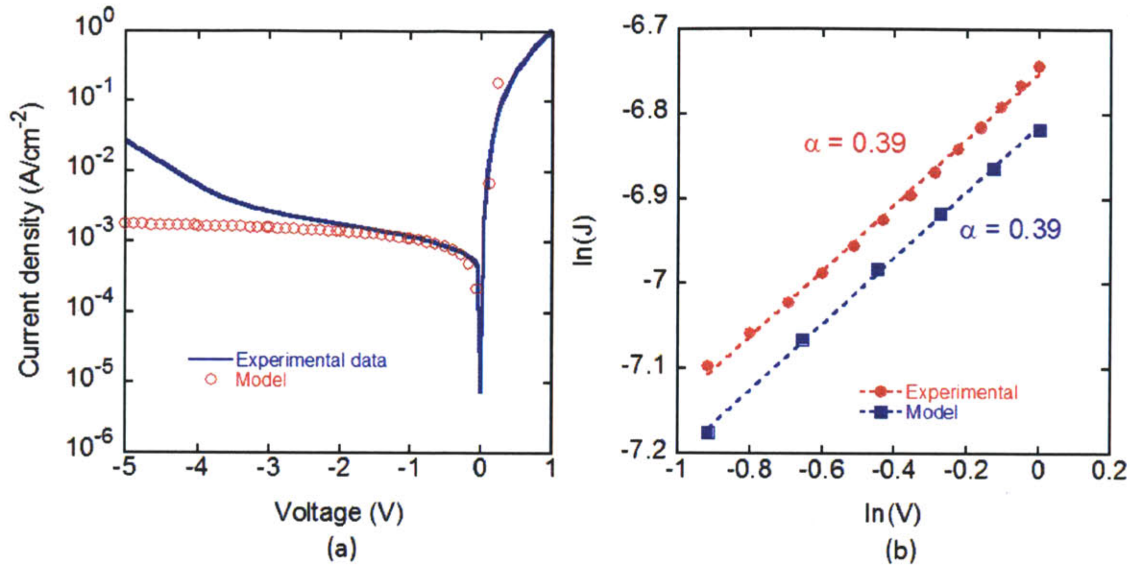

Figure 5-11: (a) Current versus voltage curves for a 300 x 300 μm device and simulated device with a minority carrier lifetime of 0.2 μs. (b) ln(J) versus ln(V) of experimental and simulated devices. Both the current density and the α dependence match very well at biases below -2 V. The experimental data was taken from a device on wafer #6596.

Figure 5-11 shows the current density versus voltage characteristics of the simulated structure as compared to an actual device that was 300 x 300 μm large. 5-11(a) shows the full current versus voltage characteristic. It shows that there is excellent agreement between simulation and experiment out to ~-2 V. Figure 5-11(b) shows the natural log of the current density versus the natural log of the voltage for the simulated structure and the experimental device. The α values match very well in the -0.4 to -1 V range. The excellent agreement in both absolute current density and α indicate that the dominant leakage current mechanism for the large and annealed devices is Shockley-Read-Hall generation with a carrier lifetime of 0.2 μs.

Figure 5-12 shows the sensitivity of the dark current density on the minority carrier lifetime parameter, τ. For a 10X increase in the lifetime, the dark current drops by 10X and the α dependence remains the same. The figure shows current density versus voltage for four different values of the lifetime, including $\tau = 0.2$ μs.

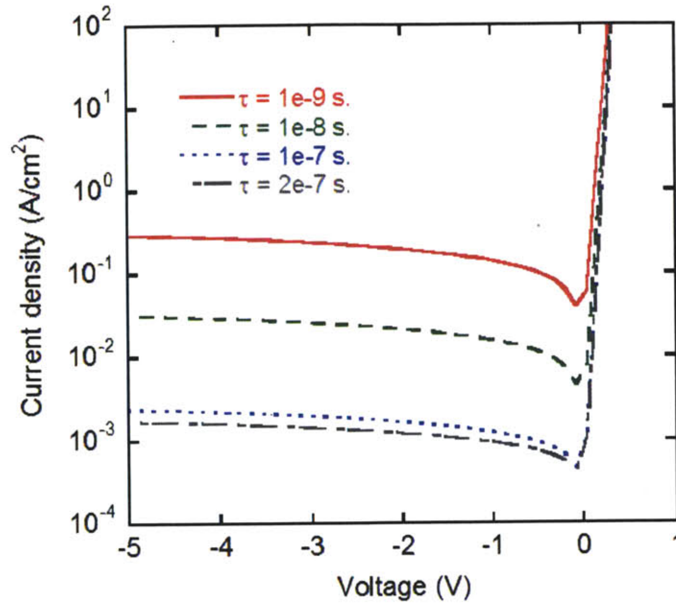

Figure 5-12: Simulated current density versus voltage for different values of minority carrier lifetime. As the lifetime increases, the dark current decreases by an equal magnitude. A value of $\tau = 0.2$ μs was found to best fit the large and annealed devices in this study.

5.4 Modeling of small devices

To accurately model the current versus voltage characteristics for small devices which were both annealed and unannealed the simulations had to be changed to 3D simulations to more accurately represent the perimeter/area ratio. A slice of the simulation can be seen in figure 5-13. It should be noted that the actual devices are square, but the most efficient way to do three dimensional simulations in Sentaurus Device is to exploit the use of cylindrical coordinates. Thus, the modeled devices will be circles rather than squares. A drawback to this choice is that the perimeter/area ratios will not be perfect for the simulations, making it difficult to match both the absolute current and the voltage dependence of the current simultaneously. For the sake of these simulations, it was more important to match the trend in α than it was to perfectly match the current. Thus, the surface recombination velocity was extracted to match the α values for the three smaller devices.

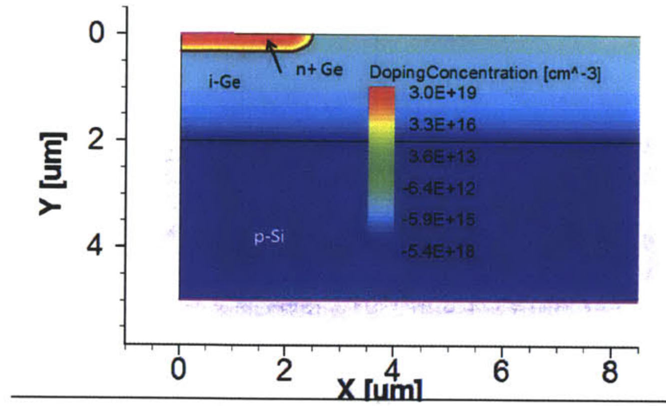

Figure 5-13: A cross-sectional schematic diagram of the structure used to calculate the surface recombination velocity. This is a slice of the device which is rotated radially to create a cylindrical device. The colors indicate the doping level.

For reference, the α values of experimental devices at low bias voltages are given in Figure 5-14(b). This figure shows that, as the device size grows, so does α, until it reaches a value of 0.39 for a 300 x 300 μm device (not shown). The steepness of the slope reflects the balance of current due to generation in the depletion region of the bulk of the device and generation of current at the surface. The more surface generation current that is present, the flatter the curve will be (*i.e.* α approaches 0). The more bulk generation is present, the more α will trend towards 0.39.

Before S_0 was extracted, an estimate of the fixed charge both before and after anneal had to be calculated. MOSCAP modeling in Sentaurus Device using the same doping profile in the germanium indicated that the fixed charge of the device without a PMA was ~0.5 x 10^{12} cm^{-2} and devices with an anneal had a fixed charge of ~1 x 10^{12} cm^{-2}.

Experimental data was used to extract an estimate of the surface recombination velocity. For the small sizes (*i.e.* 5 μm, 10 μm, 20 μm), the total device current can be written as

$$I_{total} = J_A A + I_{surface} \tag{5.7}$$

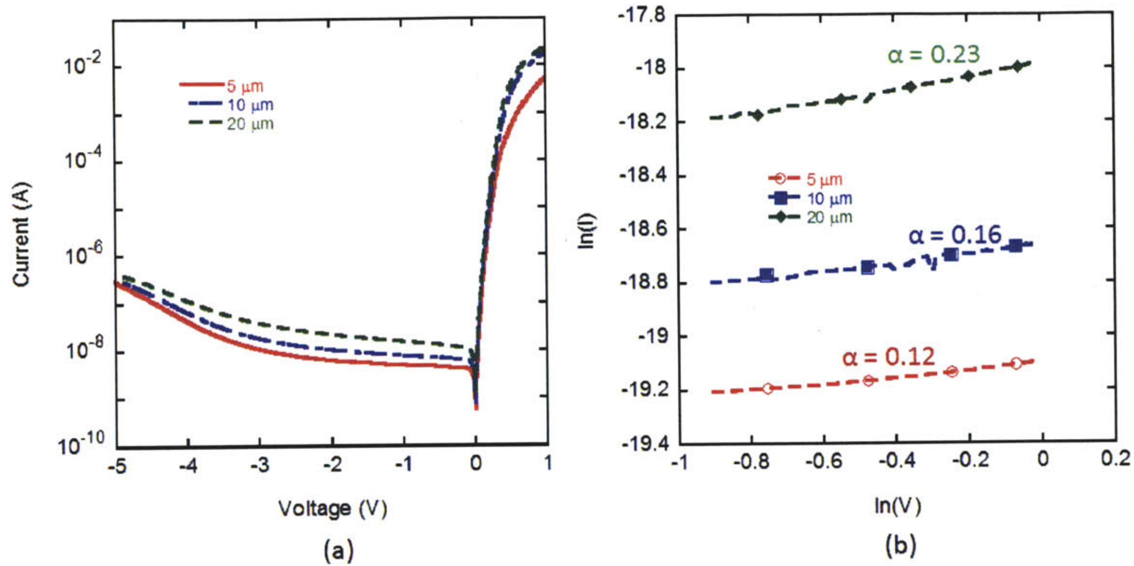

Figure 5-14: (a)Current versus voltage characteristics and (b)α extraction for devices of different sizes after an anneal. As the device size grows, the current is dominated by generation of carriers in the depletion region and α approaches 0.39. As the device size shrinks, the current is dominated by surface generation of carriers and α approaches 0. This analysis was done on devices fabricated on wafer #6596.

where J_A is the areal component of the current, A is the area of the $n+$ region of the device, and $I_{surface}$ is the current due to surface generation. In reverse bias, the surface generation current can be written as

$$I_{surface} = qA_{eff}S_0 n_i \tag{5.8}$$

where q is the charge on an electron, A_{eff} is the area over which surface generation takes place (not the area of the $n+$ region), S_0 is the surface recombination velocity, and n_i is the intrinsic carrier concentration. By knowing the total measured current and the value of J_A ($\sim$1 mA/cm^2) from the large area devices, the total surface current can be calculated. The charge of an electron and the intrinsic carrier concentration are constant, which leaves only the surface recombination velocity and the area. Thus, both S_0 and A_{eff} are unknowns.

To get an estimate of the area, simulations were run with a small active device

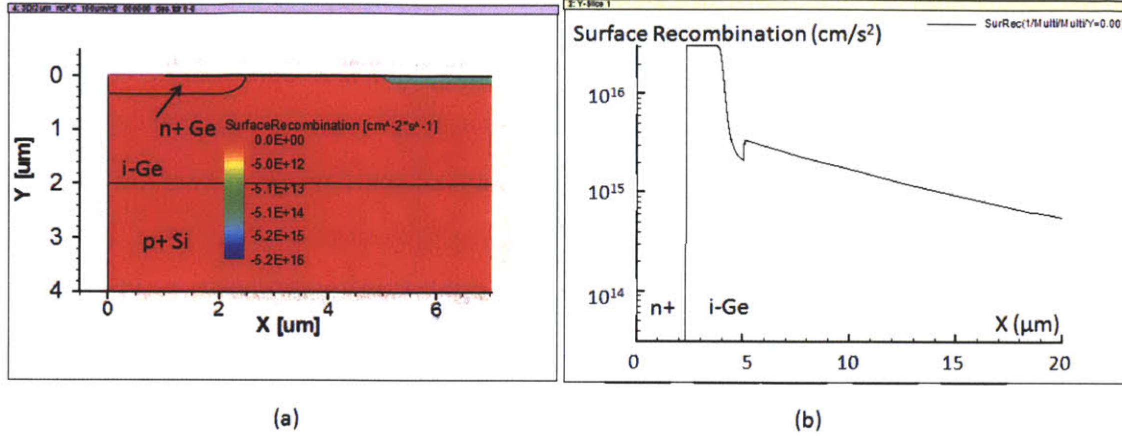

Figure 5-15: (a) A two dimensional plot of the surface generation current and (b) a one dimensional plot of the surface generation current in the y direction just below the surface of the Ge. The maximum surface generation takes place within a ~2 μm region from the edge of the $n+$ region.

area and a large Ge/oxide interface area. This helped to generate an estimate of how far the surface generation current extended from the edge of the $n+$ region. Figure 5-15 shows both a two dimensional plot of the surface generation current and a cut in the y direction of the surface generation. The majority of the surface generation takes place over the first ~2 μm of the Ge/oxide interface. Using both 2 μm and 4 μm as the estimates of the distance over which surface generation occurs, the values of S_0 are summarized in table 5.2.

Table 5.2: Summary of surface recombination velocity extraction

Device size	Surface current (at -1 V)	S_0 (cm/s) assuming 2 μm width	S_0 (cm/s) assuming 4 μm width
5 x 5 μm	4.9 nA	3460	1350
10 x 10 μm	7.2 nA	2660	1156
20 x 20 μm	11.2 nA	2270	1057

The table demonstrates that there is reasonable agreement among S_0 values for various device sizes. Furthermore, the value of S_0 is expected to be in the 10^3 cm/s range.

The goal of the simulations was to match the α values for the three smallest device

sizes. Again, since the perimeter/area ratios will be different for square and circular devices, the absolute current is not expected to match. Since the dark current of the three smallest device sizes scales with the perimeter of the devices, it was decided to simulate devices with the same perimeter. Thus, radii of the simulated devices were chosen to be 2.5 μm, 5.75 μm, and 12 μm to match square devices with sides of the $n+$ regions measuring 4 μm, 9 μm, and 19 μm.

An S_0 value of 5000 cm/s was found to give the best fit for the α values. Figure 5-16 shows the simulated absolute dark current and the α values for the three different device sizes with $S_0 = 5000$ cm/s. The absolute dark current is of the right order of magnitude as compared to the experimental devices shown in Figure 5-14(a). The α values match experiment very well. From run to run, it was found that the α value of a 4 x 4 μm device varied between 0.9 and 0.12 for an actual device. Similar variations were found for the other sizes, though the trend is always the same. Thus, it was concluded that using a value of $S_0 = 5000$ cm/s is a reasonable estimate of the surface recombination velocity.

After extracting the value of S_0 for the devices, it was necessary to show the reduction in dark current for different surface conditions of the germanium. It was hypothesized previously that the anneal introduces a negative fixed charge which reduces the depletion region around the device. Thus, by switching the fixed charge from -1 x 10^{12} cm^{-2} to 0.5 x 10^{12} cm^{-2}, the simulations should show a drastic reduction in dark current. Figure 5-17 shows the current versus voltage characteristics for identical devices with different fixed charges. The reduction in dark current at -1 V is $\sim$1000X.

Furthermore, the change in fixed charge accurately models the experimentally observed trend in ideality factor. The ideality factor of a diode is a measure of how closely the IV curve follows the ideal diode curve in forward bias. For an ideal diode, the ideality factor (η) is equal to 1. η usually ranges from 1 to 2 based on the quality

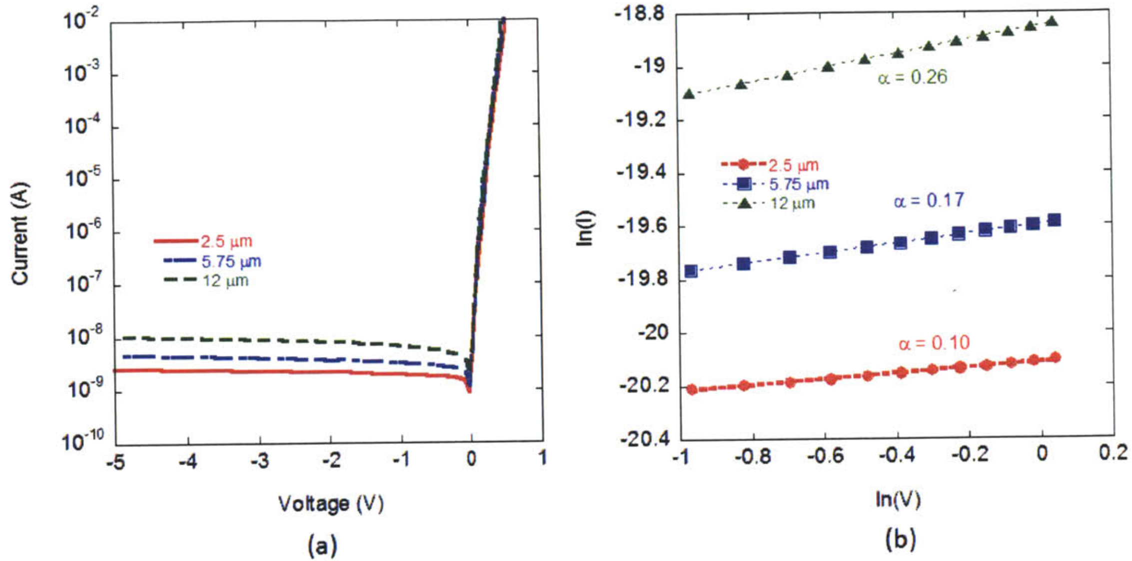

Figure 5-16: (a) Current versus voltage characteristics for devices of three different sizes and (b) their extracted α dependence. As the device size grows, α increases, keeping with the same trend as experimental devices. These simulations were done with a surface recombination velocity $S_0 = 5000$ cm/s.

of the diode. For experimental devices, η is 1.1 while unannealed devices have $\eta =$ 1.6. For the modeled devices, the ideaity factor is 1.1 for the devices with a negative fixed charge while $\eta = 1.4$ for a positive fixed charge.

The final simulation to check was to investigate the effect of p-type doping in the top of the film. Figure 5-18 shows the current versus voltage characteristics of "unannealed" devices (*i.e.* those with a positive fixed charge at the Ge/oxide interface) with and without p-type doping at the top 200 nm of the Ge film. The addition of a p-type layer has the same effect as the anneal. The p-type layer reduces the dark current by ~1000X, even with a positive fixed charge at the interface.

Furthermore, Figure 5-19 shows simulated current versus voltage characteristics for devices with a p-type layer at the top of the Ge with a positive fixed charge and with a negative fixed charge. There is virtually no difference in the dark current for different fixed charge scenarios as expected. Moreover, when comparing the ex-

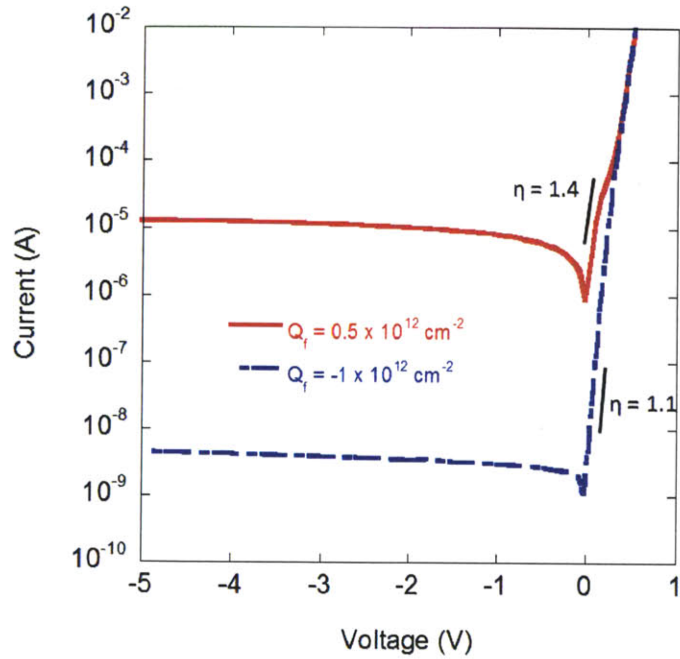

Figure 5-17: Current versus voltage characteristics for simulated devices with Q_f = -1 x 10^{12} cm^{-2} and Q_f = 0.5 x 10^{12} cm^{-2}. The radius of the device was 5.75 μm and S_0 = 5000 cm/s. The change in fixed charge reduces the dark current by ~1000X.

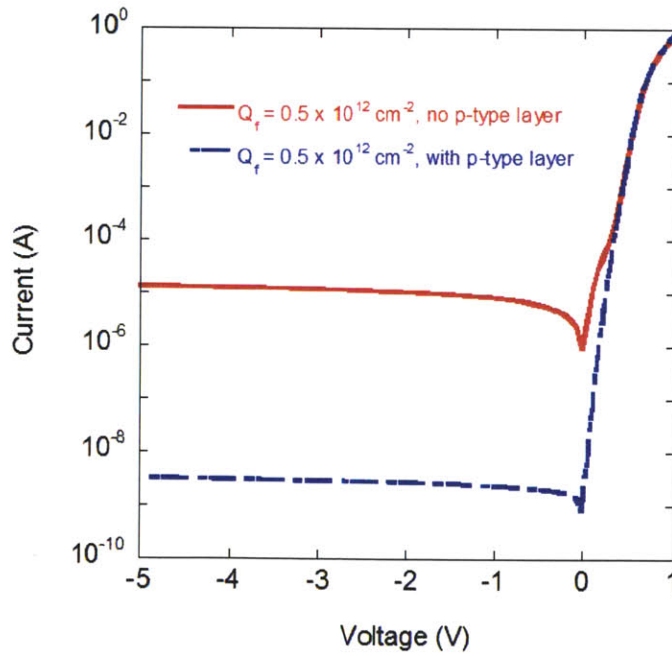

Figure 5-18: Current versus voltage characteristics for simulated devices with Q_f = 0.5 x 10^{12} cm^{-2} with and without a p-type layer. The addition of a p-type layer reduces the dark current in a similar fashion to the change in fixed charge.

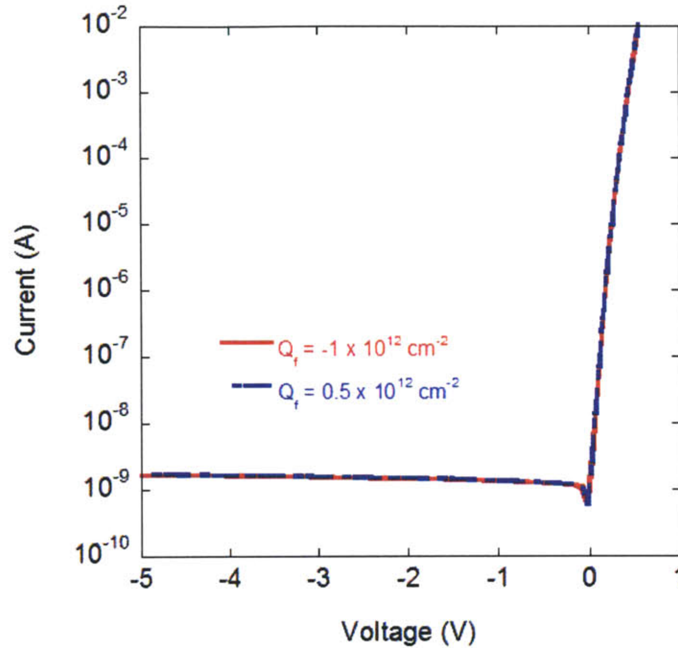

Figure 5-19: Current versus voltage characteristics for simulated devices with p-type layers with Q_f = -1 x 10^{12} cm^{-2} and Q_f = 0.5 x 10^{12} cm^{-2}. The change in fixed charge has virtually no effect on the dark current when there is a p-type layer at the top of the Ge.

perimental current versus voltage curves for devices with a p-type layer and devices without a p-type layer but with a PMA, there is a "kink" in the curve where the leakage current begins to increase rapidly. Due to the steep slope and the pinning of the current at high temperatures, this is most likely a tunneling effect, caused by the onset of a high electric field. When comparing these kinks, it is clear that the devices with the p-type doping have tunneling occur at lower bias ($\sim$-1 V as compared to $\sim$-2.5 V). This is most likely because there is a high electric field surrounding the entire $n+$ region for a device with the p-type doping. For devices with only the PMA, the high electric field is only in a small region around the perimeter of the device. The high electric field regions for both types of devices are illustrated schematically in Figure 5-21.

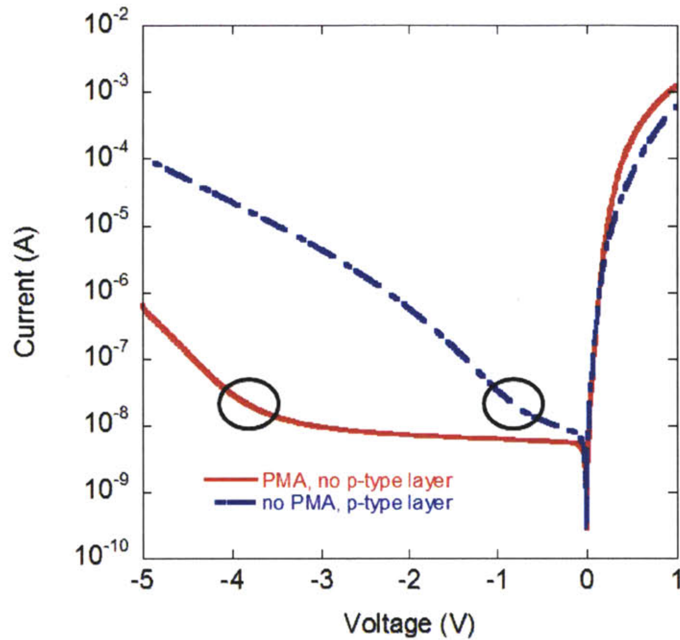

Figure 5-20: Current versus voltage characteristics for 5 x 5 μm experimental devices. One device received a PMA while the other had a p-type layer grown in the top of the germanium. The circles indicate the "kink" in the curve where the dark current increases rapidly. The reduction in dark current is similar for both devices, but the kink for a device with a p-type layer happens at a lower reverse bias. The device with the p-type layer was from wafer #6610 and the device without the p-type layer but with a PMA was from wafer #6596.

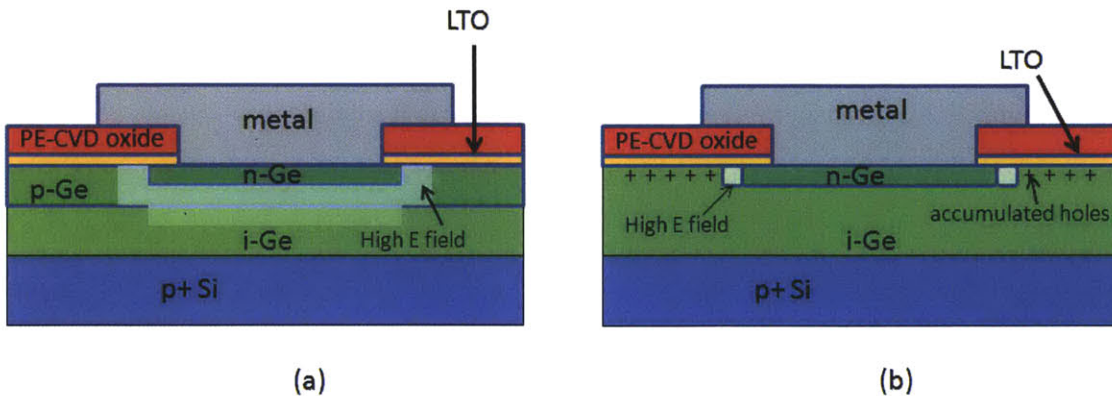

Figure 5-21: Schematic diagrams of the location of the high electric field for (a) a device doped p-type in the top of the germanium and (b) a device which received a PMA. When devices were doped p-type, a high electric field forms around the $n+$ region and results in tunneling beginning at a lower applied bias. When the devices received a PMA, there was only a small region of the device where there was a high electric field. Thus, tunneling began at a higher applied bias.

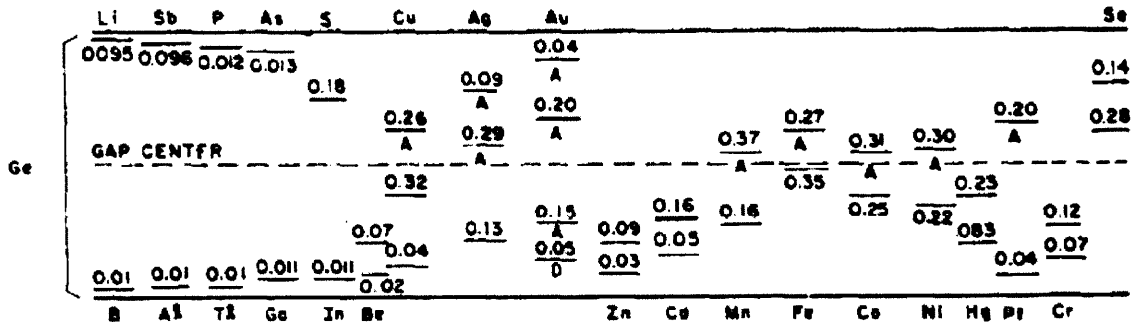

Figure 5-22: Defect levels in germanium due to material contaminants. Candidates for mid-gap defect levels are Fe and Cu. Shallower defects may be caused by Ag, Au, or Cr. From [88].

5.5 Origin of dark current

Experimental and modeling results indicate that the dark current of large germanium photodiodes is dominated by generation in the depletion region as defined by the $n+$ implant of the device. Furthermore, the dark curent of small germanium photodiodes is dominated by generation of carriers at the surface in the region outside the $n+$ implant. These results, however, do not indicate what is responsible for generation of carriers. The activation energies of the dark current can give us some hints.

At -1 V, the activation energy of small and large devices was 0.54 eV and 0.33 eV respectively. These activation energies indicate that there is a trap mechanism at work, somewhere in the bandgap. For the large devices, the trap is in the middle. For the small devices, the trap is either 0.54 eV away from the valence band or 0.54 eV away from the conduction band (*i.e.* 0.12 eV from one of the band edges). These trap levels are caused by some sort of defect, either crystal defects or material contaminants. Traps in germanium devices fabricated from a bulk wafer have been studied in detail previously [81, 82, 83, 84, 85, 86, 87]. A summary of the activation energies of a range of defects in germanium can be found in figure 5-22.

Mid-gap states in germanium may be caused by either iron or copper while shallower states (at 0.54 eV) may be caused by silver, gold, or chromium. To further

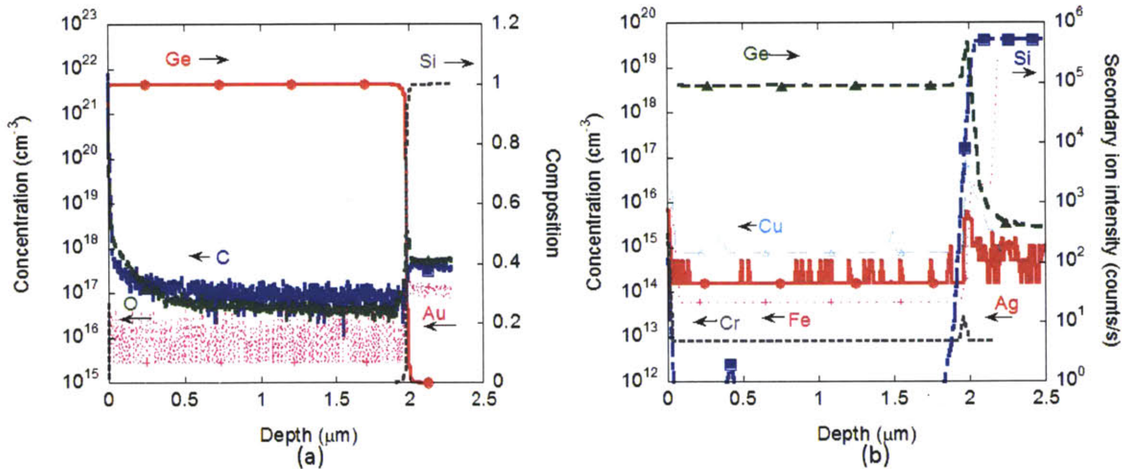

Figure 5-23: SIMS profiles for (a) Ge, Si, O, C, and Au and (b) Ge, Si, Cu, Ag, Fe, and Cr. The concentrations of Cu, Ag, Fe, and Cr were all below the detection level of SIMS. The concentration of oxygen, however, is in the 10^{17} cm^{-3} range in the top 0.4 μm of the film. This analysis was done on wafer #6596.

investigate the source of the contaminants, samples were sent for secondary ion mass spectroscopy (SIMS). SIMS profiles of gold, copper, silver, iron, and chromium can be seen in Figure 5-23. The figure shows that these metals are not present in any appreciable amount in our samples. However, we cannot rule out material contaminants as the source of traps since trap densities expected from the deep level transient spectroscopy (DLTS) data (discussed next) are below the SIMS detection limit.

Deep level transient spectroscopy is another way to analyze the activation energy of defects in semiconductors [89]. In this process, the sample is cooled to cryogenic temperatures and a voltage is pulsed across the device. Based on how the current recovers at different temperatures, trap levels can be extracted. Furthermore, the shape of the recovery can indicate mechanisms of leakage current. A previous study on plastically deformed germanium has shown that an anneal in the range of 580°C reduces the amplitude of the DLTS signal by 10X while not affecting the threading defect density [90]. This suggests that the anneal temperatures in this study may change the magnitude of the number of traps without changing the number of defects.

Previous DLTS studies on germanium have indicated a wide range of traps due to many different mechanisms. They are summarized in tables 5.3 and 5.4.

Table 5.3: Hole traps in Ge

Trap level, E (E_V + E)	Author and citation	Due to
0.1 eV	Simoen [91]	dislocations
0.15 eV	Auret [92]	
0.16 eV	Poulin [93]	divacancy
0.18 eV	Auret [92]	divacancy
0.25 eV	Mooney [94]	vacancy-oxygen
0.27 eV	Markevich, Auret [95] [96]	vacancy-oxygen
0.30 eV	Coutinho, Auret, Poulin [97] [96] [93]	divacancy, impurity + defect
0.31 eV	Lindberg [98]	vacancy-Sb
0.52 eV	Poulin [93]	impurity + defect

Table 5.4: Electron traps in Ge

Trap level, E (E_C - E)	Author and citation	Due to
0.12 eV	Mooney [94]	interstitial complex
0.13 eV	Auret [96]	
0.15 eV	Auret [92]	implant defects
0.20 eV	Auret [96]	interstitial + Sb
0.21 eV	Markevich, Auret [95] [96]	Sb, vacancy + oxygen
0.24 eV	Auret [96]	interstitial + Sb
0.26 eV	Mooney [94]	
0.27 eV	Poulin [99]	impurity + defect
0.29 eV	Kolkovsky [100]	
0.30 eV	Simoen, Auret [101] [92]	Ni, implant defects
0.31 eV	Auret [96]	vacancy
0.32 eV	Poulin [99]	divacancy
0.53 eV	Mooney [94]	

Samples from this work were studied using DLTS. Due to capacitance constraints, only the largest diodes were suitable for DLTS studies. Analysis on the 300 x 300 μm squares was performed by Daniel Johnstone from Semetrol on both annealed and unannealed wafers, looking for defects at 0.33 eV and 0.12 eV. DLTS measurements

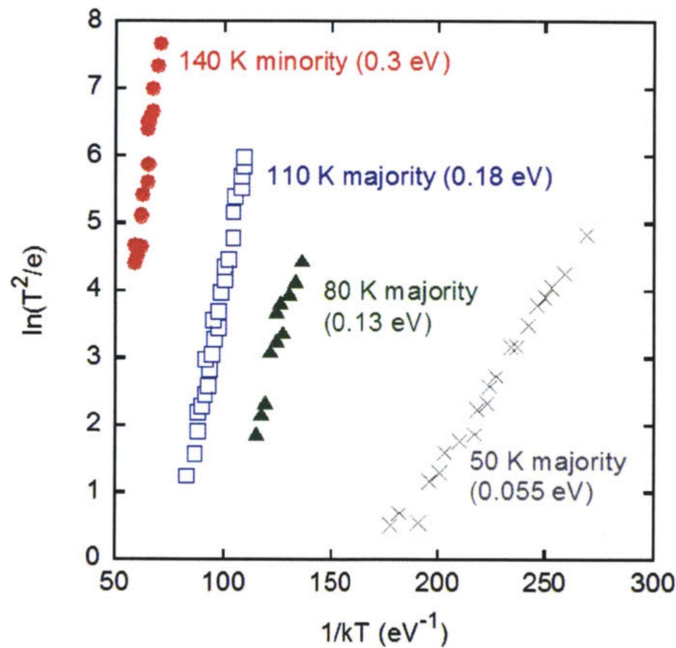

Figure 5-24: Arrhenius plot of different trap levels found in a 300 x 300 μm device that received a PMA. The analysis indicates that there is one minority trap and three majority traps present. Analysis courtesy of Daniel Johnstone, Semetrol. This analysis was done on wafer #6596.

on the annealed sample showed the presence of four trap levels at $E = E_v + 0.055$, $E = E_v + 0.13$, $E = E_v + 0.18$, and $E = E_c - 0.3$, as indicated in Figure 5-24. Unfortunately, the leakage current of the unannealed sample was too high to give an accurate measurement of trap concentration. Capacitance transients as a function of filling pulse duration were taken at 100 K on the annealed sample and the DLTS signal versus filling pulse duration can be seen in Figure 5-25. At 100 K, there were two trap levels very close to one another. The solid line represents a trap higher in energy while the dashed line represents a trap lower in energy. The sum of these is given in the dotted curve. The logarithmic shape of the sum is consistent with this trap level being associated with dislocations [91, 102].

To test this hypothesis, photodiodes were fabricated from blanket Ge-on-Si where the post-growth anneal (a cyclic anneal between 800°C and 450°C) was either elimi-

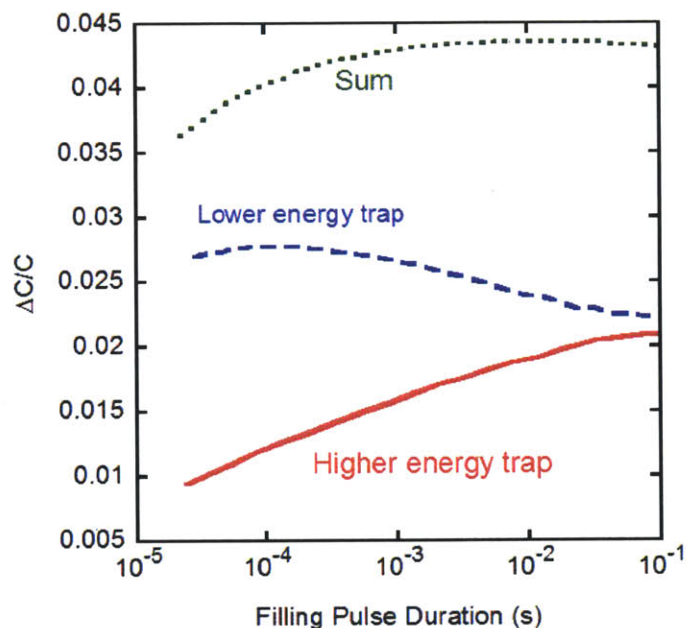

Figure 5-25: DLTS signal at 100K as a function of filling pulse duration for a 300 x 300 μm device that received a PMA. There were two trap states close in energy at 100K. The solid line is the DLTS signal for a trap slightly higher in energy and the dashed line is the signal for the trap slightly lower in energy. The dotted line is the sum. The logarithmic shape of the dotted curve is consistent with this trap level being associated with dislocations [91, 102]. Analysis courtesy of Daniel Johnstone, Semetrol. This analysis was done on wafer #6596.

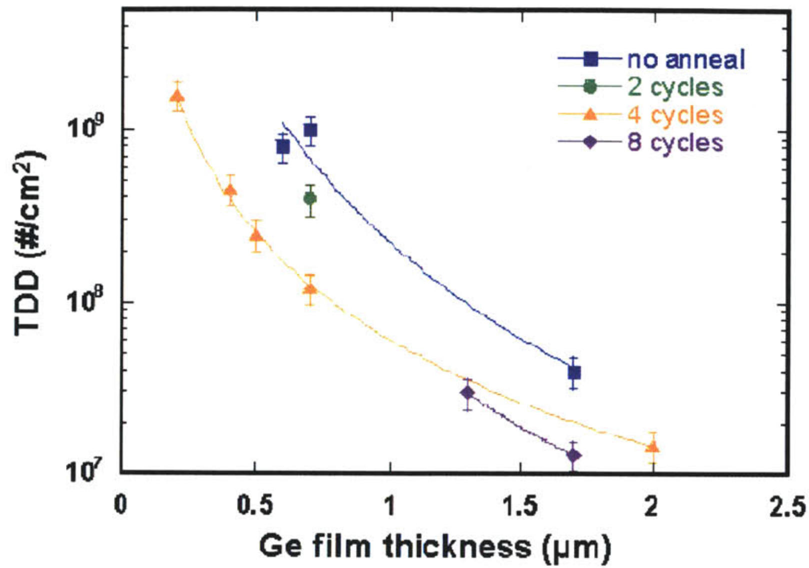

Figure 5-26: Threading dislocation density as measured by plan-view transmission electron microscopy versus thickness for different annealing cycles. At 1 μm, the threading dislocations in germanium from an unannealed sample to one annealed for four cycles are reduced by ~4X. From [26].

nated or reduced to change the dislocation density. The thickness of the germanium was reduced to 1 μm in an attempt to obtain a large spread in the threading dislocation density. Previous studies on similarly grown layers have shown that the dislocation density for 1 μm films without an anneal should be on the order of 2 x 10^8 cm^{-2} while the defects for a 4X anneal should be 5 x 10^7 cm^{-2} [26]. Threading defect density as a function of film thickness for different annealing cycles can be seen in Figure 5-26.

Comparison of the dark current for 300 x 300 μm devices with different anneals can be seen in Figure 5-27. The inclusion of a two cycle high temperature post-growth anneal reduces the dark current by 45X. The reduction decreases to 14X for 10 x 10 μm devices that received two anneal cycles, indicating that the effect of the anneal is mostly an areal effect. There is little benefit observed for annealing beyond two cycles. This suggests that the threading defects are associated with the dark current

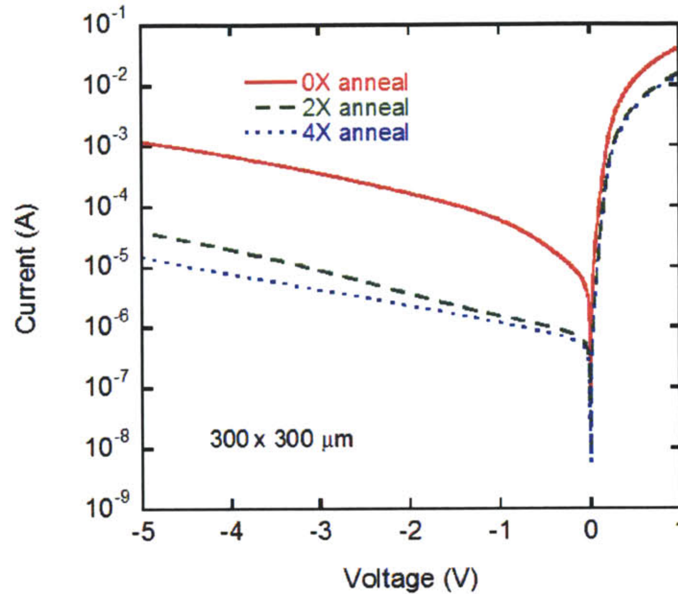

Figure 5-27: Current versus voltage for 300 x 300 μm devices annealed for a different number of cycles. These devices were passivated with LTO and received a post-metallization anneal. The reduction in dark current at -1 V is ~45X and decreases to 14X for 10 x 10 μm devices. Devices without a post-growth anneal were from wafer #6879 while devices with a 2X anneal were from wafer #6884 and devices with a 4X anneal were from wafer #6882.

when the defect level is high, but when the density is reduced to less than $\sim 10^8$ cm^{-2}, another mechanism is dominant. Furthermore, the dark current for the devices fabricated without a post-growth anneal scales with the area of the devices as seen in Figure 5-28. This further supports the hypothesis that the threading defects are the dominant mechanism responsible for the dark current when the defect level is in the 10^8 cm^{-2} range.

It should be mentioned that it is possible the threading dislocations are not acting alone. It is possible that the dislocations are serving as gettering sites for heavy metal impurities. While SIMS did not detect heavy metals in a large concentration, there is a chance that they are still present in the films.

The defects contributing to the dark current could also be due to residual damage from phosphorus implantation. Previous studies have shown that germanium can

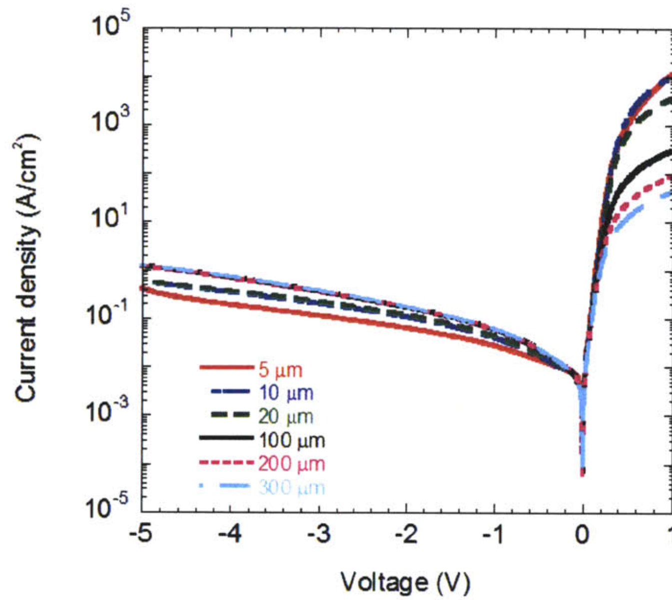

Figure 5-28: Dark current density versus voltage for different device sizes fabricated on a wafer which did not see a post-growth anneal. The dark current scales with the area of the device, indicating that, when the defect density is on the order of 10^8 cm^{-2} the defects are the main source of leakage current. These devices were all on wafer #6879.

recrystallize by solid phase epitaxy after phosphorus implantation with an anneal at 400°C for 60 seconds [103]. Since the activation anneal after implantation was done at 550°C for 30 seconds, it was expected that most of the damage caused by the implant would be gone and there would not be an effect on the dark current. However, end-of-range damage would still be present [104] [105] and this might affect the dark current. To test this, devices were fabricated with identical processing steps except for the dose of the implant. One wafer was implanted with a dose of 5 x 10^{14} cm^{-2} and another was implanted with a dose of 1 x 10^{14} cm^{-2}. Both of these doses were expected to amorphize the germanium; however, the higher dose was expected to leave more end-of-range damage. Thus, the wafer with the lower dose implant had less damage and might be expected to have a lower dark current.

Figure 5-29 shows the current versus voltage characteristics for 300 x 300 μm devices with and without a PMA for different implant doses. The largest device sizes

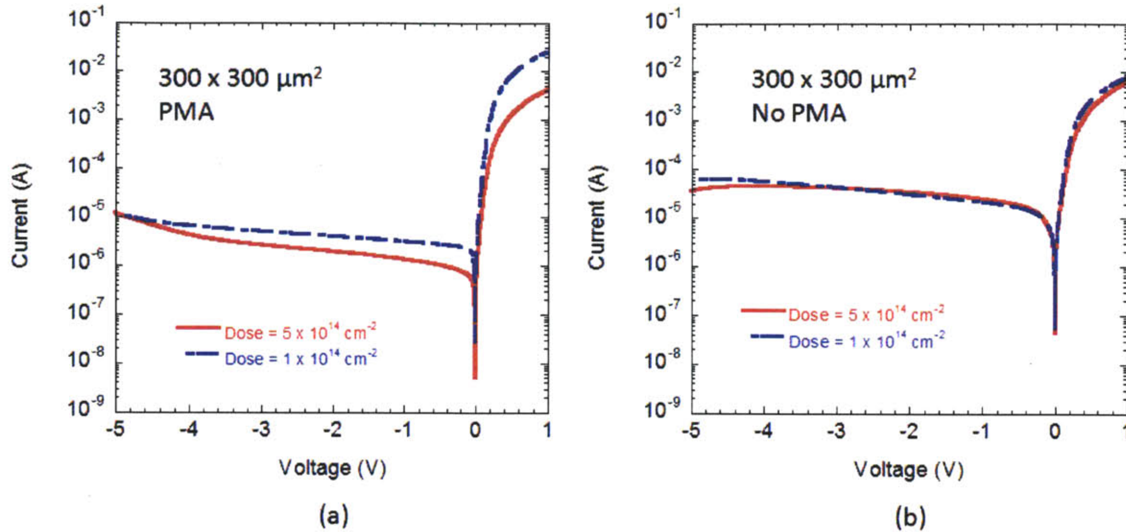

Figure 5-29: Current versus voltage for 300 x 300 μm devices with different implant doses (a) with a PMA and (b) without a PMA. Without a PMA, there is virtually no effect on the dark current. With a PMA, the higher dose implant has a slightly lower leakage current which is the opposite effect that is expected if implant damage were the source of the leakage current. The devices with an implant dose of 5 x 10^{14} cm^{-2} were fabricated on wafer #6881 and the devices with an implant dose of 1 x 10^{14} cm^{-2} were fabricated on wafer #6988.

were chosen because the end-of-range implant damage is expected to be an areal effect and these devices should have minimal perimeter effects. For devices without a PMA, the leakage current is virtually the same for the different doses. For devices with a PMA, the higher dose implant has a slightly lower leakage current which is the opposite of what was expected based upon simplified assumptions. The increase in dark current for the lower dose may be explained by the slightly larger depletion region at any given bias.

It should be noted that end-of-range damage from implantation in germanium has been shown to change in size and density with an anneal around 400°C [104] [106]. It is tempting to attribute the reduction in dark current to these changing defects. However, the MOSCAP samples discussed in chapter 4 did not receive an implant at all and the flatband voltage still shifted. Thus, it is unlikely that the end-of-range damage is the dominant factor for the leakage current.

It is also possible that impurities such as oxygen, carbon, or hydrogen contribute to the dark current. These may act alone or may form complexes with crystal defects. The 0.12 eV activation energy for the leakage current is associated with all sizes of unannealed devices, which are believed to have large perimeter depletion regions at the surface. This indicates that this defect is associated with the surface. Tables 5.3 and 5.4 indicate that a crystal defect may be responsible for this trap state, perhaps coupled with an impurity. Previous work has indicated that oxygen forms thermal donors in germanium when annealed in the range of 300°C - 500°C [107] [108]. Hall effect measurements have shown activation energies of these thermal donors at 0.017, 0.04, and 0.2 eV [109]. SIMS analysis on our films showed oxygen content in the top 300 nm of the film to be $\sim 10^{17}$ cm^{-3}, suggesting that oxygen complexes may be at play during the PMA.

It is further hypothesized that the equilibrium result of this reaction is to form GeO_4 complexes which act as thermal donors - *i.e.* nearly all are ionized. However, the GeO_4 complex must first form a GeO_3 complex which must first form a GeO_2 complex. Fuller has hypothesized that, for an incomplete reaction, the primary effect will be mostly GeO_2 complexes [109]. The GeO_3 complex would be neutral or partially ionized while the GeO_2 complex would result in an overall decrease in donors. Figure 5-30 shows the donor concentration as a function of temperature and time for various oxygen-doped germanium samples. The equilibrium value of donors differs based on the temperature of the reaction. At 350°C, equilibrium is not reached for $\sim$100 hours. This implies that, for the temperatures and times in this study, the reaction is not reaching the final stage, but rather being stopped in an intermediate part where GeO_2 can form. It is possible that these complexes are responsible for the increase in holes at the surface of the germanium.

Another hypothesis is that the 0.12 eV activation energy of the unannealed devices is caused by hydrogen. Since the germanium is grown epitaxially using GeH_4 as its

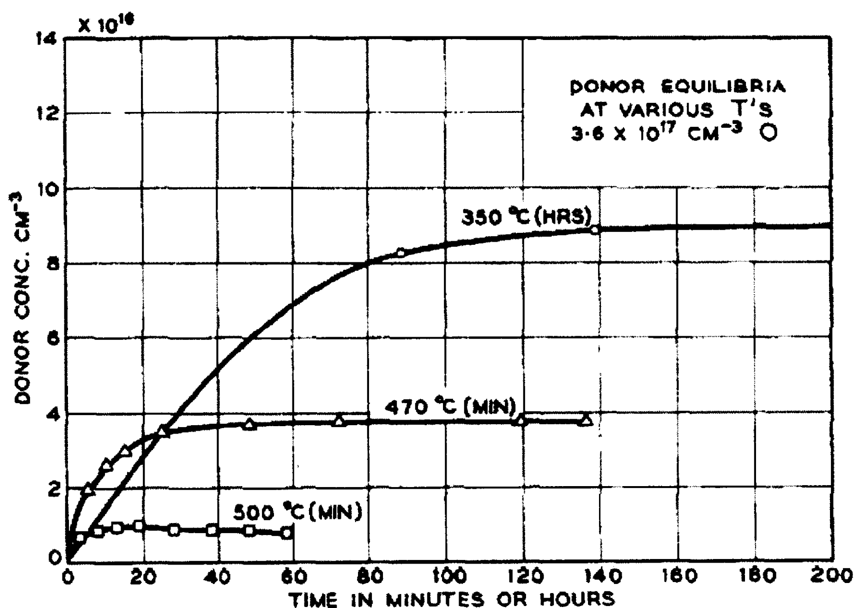

Figure 5-30: Thermal donor concentration as a function of time and temperature. For the times and temperatures in this work, the reaction as not reached equilibrium and an intermediate complex of GeO_2 is formed. From [110].

source, there is most likely an appreciable level of hydrogen in the germanium film. Dobaczewski, *et al.* have found a donor level with activation energy of 0.11 eV due to hydrogen [111]. Furthermore, hydrogen is known to form both thermal donors and thermal acceptors based on various annealing temperatures and other atomic elements present [112]. More experiments would be needed to fully elucidate the effects of both hydrogen and oxygen on the germanium.

Finally, it should be noted that Van de Walle, *et al.* have hypothesized that dangling bonds at any interface involving germanium will always be negatively charged [113]. This is unlike their behavior at silicon interfaces and implies that even materials such as HfO_2 or $LaYO_3$, which have shown promising results for Ge MOSFET applications [114] [115], will result in a similar problem for germanium diodes as observed in this study. The dangling bonds lead to a fixed charge which will cause a large depletion region at the surface, regardless of the passivation material. This suggests that care must be taken to design the surface of the germanium such that

this depletion region is eliminated, especially when fabricating small devices.

5.6 Chapter summary

This chapter examined the underlying physics and operation of the germanium diodes fabricated and characterized in chapter 4. It discussed the scaling, temperature dependence, and voltage dependence of the devices and formulated a theory for their operation. Modeling and sensitivity analysis in Sentaurus Device showed that the minority carrier lifetime was $\sim$0.2 μs and that a reasonable estimate of the surface recombination velocity was $\sim$5000 cm/s. The modeling further showed the large effect that the fixed charge at the Ge/oxide interface can have on the dark current of the diode.

Finally, the chapter showed that the threading dislocations play a significant role in the dark current for densities in the 10^8 cm^{-2} range. Below that, the dark current is most likely limited by another mechanism. It is hypothesized that either oxygen or hydrogen impurities are associated with the dark current, perhaps aided by the presence of dislocations in the film.

Chapter 6

Thesis summary and future work

This chapter will summarize the thesis and ennumerate the specific contributions to the field of Ge-on-Si photodiodes. It will end with suggestions for future work.

6.1 Thesis summary

The goal of this thesis was to understand the leakage current mechanisms present in Ge-on-Si photodiodes. Diodes were fabricated both from selectively-grown Ge-on-Si and from blanket Ge-on-Si deposited by low-pressure chemical vapor deposition. Both the dark current and the responsivity were studied in this thesis.

It was found that a responsivity of ~0.25 A/W for a 1 μm-thick film and ~0.50 A/W for a 2 μm-thick film were typical values at 1550 nm and -1 V. Furthermore, it was also confirmed that the presence of tensile strain in the film shifts the responsivity curve out to longer wavelengths, as observed in earlier studies. This tensile strain is due to differences in the thermal expansion coefficients between the Ge and the underlying Si. This strain shrinks the bandgap slightly and makes absorption at longer wavelengths possible.

Furthermore, it was found that the surface conditions of the germanium were very important to the leakage current of the device. As deposited, a low-pressure CVD

oxide has a positive fixed charge at the germanium/oxide interface. This causes a large depletion region to form around the device, which dwarfs the actual size of the device. This depletion region causes a high electric field to be near the surface, increasing the leakage current. After a post-metallization anneal (PMA), the fixed charge becomes negative. The negative fixed charge draws holes to the surface which better isolates the device and reduces the leakage current. Growing a germanium film with the top part doped p-type confirmed the interpretation of these results.

Beyond the surface conditions other leakage current mechanisms were investigated. It was found that, when the threading defect density is increased above $\sim 10^8$ cm^{-3}, the threading defects are the dominant source of leakage current. Deep level transient spectroscopy confirmed the importance of the defects in a dominant trap level. However, attempting to reduce the defect density much below that by annealing does not seem to have an effect on the dark current. Based on previous studies in the literature, it seems likely that either oxygen or hydrogen are causing the trap levels.

6.2 Contributions

- Photodiodes fabricated from selectively-grown germanium films were characterized and it was found that, below a certain defect density, the dark current density is not dependent on defects. The dark current is likely dependent on something else, such as generation in the depletion region due to another contaminant.

- The impact of strain on the photoresponse for selectively-grown diodes was characterized and confirmed with Raman analysis.

- The impact of germanium passivation was studied and it was found that similar devices patterned with Al_2O_3 have $\sim$6X less leakage current than devices patterned with a low temperature oxide.

- The impact of a post-metallization anneal was studied on photodiodes fabricated from blanket Ge-on-Si. Through MOSCAP measurements, it was found that the anneal was changing the fixed charge of the Ge/oxide interface, thereby drawing holes to the surface and better isolating the devices.

- The devices made from blanket Ge-on-Si were modeled using Sentaurus Device. A minority carrier lifetime of 0.2 μs and a surface recombination velocity of 5000 cm/s were extracted. These values were used to demonstrate that the fixed charge at the surface is responsible for the ~1000X reduction in dark current. Furthermore, the simulations show that including a p-type layer at the top of the Ge will reduce the dark current by ~1000X regardless of the fixed charge at the interface.

6.3 Future work

For infrared imaging applications, germanium photodiodes should absorb light out to longer wavelengths (1.6 - 1.7 μm). To do this, more strain is needed in the film. Introducing strain across the entire wafer proved unfruitful in this thesis, but introducing strain in a localized way may be promising. A high-stress material either above or around the device (much like the high-stress material currently used in nMOSFETs) is one possibility to introduce stress.

The reduction in dark current after the PMA indicates that the surface conditions of the germanium are vitally important to fabricating a photodiode with low leakage current. While the data is clear that a PMA changes the fixed charge at the interface, the physics behind this change are not well understood. To further explore the origin of fixed charge, different annealing conditions should be studied, both with MOSCAPs and photodiodes. Detailed DLTS analysis would be helpful for different annealing conditions.

For example, the oxygen complexes described in Chapter 5 have been shown to disappear upon annealing at higher temperatures [110]. When films were annealed above 470°C, the thermal donors disappear and the germanium returns to its original state. If oxygen thermal donors are the source of the fixed charge, then a higher temperature anneal should be able to confirm this. The anneal should be done prior to the deposition of metal. It was found that annealing germanium photodiodes at temperatures higher than 425°C results in the spiking of the contacts. For this reason, the films should be annealed at higher temperatures and then the metal should be deposited.

To check for hydrogen, SIMS or surface SIMS should be done to quantify the concentration of hydrogen. This should be done both before and after the PMA. It is possible that the hydrogen is diffusing out of the germanium during the PMA, thus removing the defect energy level.

Furthermore, to fully optimize the doping structure of the germanium, gated diodes should be made. The gate can be used to modulate the surface conditions of the germanium, thus allowing the optimal concentration of holes. It was seen in chapter 4 that the addition of too many holes at the surface of the germanium can allow tunneling current to begin at relatively low biases. Gated diodes would allow the optimal concentration of holes to be found so that future diodes could be made from films doped at the optimum values.

Finally, with the knowledge of the optimal doping profiles, integration of selectively grown Ge-on-Si should be studied again with the goal of lowering the dark current. Aberg, *et al.* have shown promising results with their work on selectively grown Ge diodes [45], but with the knowledge of fixed charge and doping profiles in this thesis, those devices could be better understood and perhaps improved upon.

Appendix A

Process flows used in this thesis

A.1 Mesa isolation flow

This process outlines the steps and tools used in MIT MTL to fabricate mesa isolated Ge-on-Si photodiodes. Note that standard photoresist in ICL would not adhere to germanium, so a sacrificial oxide layer was used. The following process flow does not include all of the film thickness checks on the UV1280 or any scanning electron microscopy. These tools were used often, whenever they would be useful. In particular, the UV1280 was used to calibrate every etch on a dummy wafer and to verify that films were gone when they should be.

Table A.1: Process flow for mesa isolation

Step	Tool	Notes
RCA clean + HF dip	ICL RCA station	Pre-epi clean
Ge growth	Epi reactor	2 μm
Ge RCA clean	ICL RCA station	pre-LTO deposition clean
LTO deposition	ICL tube 6C	~10 nm for hard mask
Coat frontside of wafer	ICL coater	standard recipe

To be continued on next page

Etch backside Ge	ICL Lam490B	Poly-Si timed etch, 8 - 10 min.
Ash photoresist	ICL asher	standard recipe
Coat wafers with photoresist	ICL coater	standard recipe
Expose wafers	ICL i-stepper	Expose mesa mask
Develop pattern	ICL coater	standard recipe
Etch LTO	ICL BOE station	10 - 30 s.
Ash photoresist	ICL asher	standard recipe
Etch mesas	TRL acidhood2	H_2O:H_2O_2:HCl 4:3:1 for 30 - 60 s.
Remove LTO	TRL acidhood2 or ICL BOE station	BOE for 10 - 30 s.
Ge RCA clean	TRL acidhood2 or ICL RCA station	pre-passivation clean
Passivation deposition	ICL ALD or ICL tube 6C	~10 nm of Al_2O_3 or LTO
Coat frontside of wafer	ICL coater	standard recipe
Expose wafers	ICL i-stepper	expose $n+$ mask
Develop wafers	ICL coater	standard recipe
Ion implant	Sent to Innovion	implant P, energy and dose vary
Ash photoresist	ICL asher	standard recipe
Ge RCA clean	TRL acidhood2	use acidhood2 instead of RCA station because of alumina
Deposit interlayer dielectric	ICL DCVD	~150 nm oxide
Ge RCA clean	TRL acidhood2	use acidhood2 instead of RCA station because of alumina
Activate dopants	ICL RTP	550° - 600°, 10 - 60 s.
Coat wafers with photoresist	ICL coater	standard recipe

To be continued on next page

Expose wafers	ICL i-stepper	Expose contact via mask
Develop pattern	ICL coater	standard recipe
Dry etch of contact vias	ICL AME5000	recipe: NICOLEOXIDE
Wet etch of contact vias	TRL acidhood2	BOE, 15 - 30 s.
Pre-metal clean	TRL acidhood2	50:1 HF, 30 - 60 s.
Metal deposition	ICL Endura	recipe: CAITTIAL, 100 nm Ti and 1 μm Al
Coat wafers with photoresist	ICL coater	standard recipe
Expose wafers	ICL i-stepper	Expose metal via mask
Develop pattern	ICL coater	standard recipe
Dry etch of metal contact	ICL Rainbow	recipe: Nicole_TiAl

A.2 Process flow without mesa isolation

This process flow was used to fabricate diodes without the mesa isolation etch. The mesa etch rate was highly variable and hard to control. Furthermore, the effect of the mesa sidewalls and corners was unknown. This flow was developed to use the same mask set but skip the mesa etch. To fully delineate which part of the flow was the part to preserve the alignment marks, that part is given in the next section.

Table A.2: Process flow without mesa isolation

Step	Tool	Notes
RCA clean + HF dip	ICL RCA station	Pre-epi clean
Ge growth	Epi reactor	2 μm
Coat frontside of wafer	ICL coater	standard recipe

To be continued on next page

Etch backside Ge	ICL Lam490B	Poly-Si timed etch, 8 - 10 min.
Ash photoresist	ICL asher	standard recipe
Alignment mark protection flow	Various	Various
Ge RCA clean	ICL RCA station	pre-LTO deposition clean
Screen oxide deposition	ICL tube 6C	~10 nm of LTO
Coat frontside of wafer	ICL coater	standard recipe
Expose wafers	ICL i-stepper	expose $n+$ mask
Develop wafers	ICL coater	standard recipe
Ion implant	Sent to Innovion	implant P, energy and dose vary
Ash photoresist	ICL asher	standard recipe
Ge RCA clean	ICL RCA station	pre-activation clean
Activate dopants	ICL RTP	550° - 600°, 10 - 60 s.
Remove screen oxide	ICL BOE station	BOE for 10 - 30 s.
Ge RCA clean	ICL RCA station	pre-passivation clean
Passivation deposition	ICL tube 6C or ICL ALD	~10 nm of LTO or Al_2O_3
Interlayer dielectric deposition	ICL DCVD	~150 nm of oxide
Coat frontside of wafer	ICL coater	standard recipe
Expose wafers	ICL i-stepper	expose contact via mask
Develop wafers	ICL coater	standard recipe
Dry etch of contact vias	ICL AME5000	recipe: NICOLEOXIDE
Wet etch of contact vias	TRL acidhood2	BOE, 15 - 30 s.
Pre-metal clean	TRL acidhood2	50:1 HF, 30 - 60 s.
Metal deposition	ICL Endura	recipe: CAITTIAL, 100 nm Ti and 1 μm Al

To be continued on next page

Coat wafers with photoresist	ICL coater	standard recipe
Expose wafers	ICL i-stepper	Expose metal via mask
Develop pattern	ICL coater	standard recipe
Dry etch of metal contact	ICL Rainbow	recipe: Nicole_TiAl
Post-metallization anneal	TRL tube A3 or XX	anneal in N_2, forming gas, or vaccum between 300°C - 425°C

A.3 Alignment mark protection flow

This process flow was developed so that the mask set used for the mesa-isolation process could also be used in a process without mesa isolation. This need stems from the fact that the mesa etch made the first level of alignment marks. The subsequent implant does not leave marks that are usable for alignment in later steps. In order to align to the implants, they had to be aligned to something. This process uses a PE-CVD oxide to create the alignment marks and then shutters the exposure in later steps to protect the marks but leave everything else open. The rest of the oxide structures are then removed with BOE.

Table A.3: Process flow for mesa isolation

Step	**Tool**	**Notes**
Ge RCA clean	ICL RCA station	Pre-deposition clean
PE-CVD deposition	ICL DCVD	100 - 150 nm
Coat wafers with photoresist	ICL coater	standard recipe
Expose n+ mask	ICL i-stepper	standard recipe
Develop pattern	ICL coater	standard recipe

To be continued on next page

Etch pattern	ICL BOE station	30 - 90 s.
Ash photoresist	ICL asher	standard recipe
Coat wafers with photoresist	ICL coater	standard recipe
Expose wafers	ICL i-stepper	No mask is used. Do not expose entire reticle
Develop pattern	ICL coater	Resist should only be around perimeter of die. Alignment marks should be covered.
Remove oxide over most of die	ICL BOE station	30 - 90 s.
Ash photoresist	ICL asher	standard recipe

Appendix B

Procedure for taking photoresponse measurements

This appendix details the procedure and experimental setup for measuring the photoresponse of Ge-on-Si photodiodes fabricated in this thesis. The procedure changed over the years, but this is the final procedure that was used and very similar to previous versions.

In short, a Santac broadband laser (1260 nm - 1630 nm) coupled to a fiber was used to shine light on the devices and the output current was measured. The input power of the laser was varied and the photoresponse was calculated either from averaging the different current/power values or by measuring the slope of the line formed by the values. The measurements were done in Prof. Rajeev Ram's Physical Optics and Electronics Group's facilities. A schematic diagram of the setup can be seen in Figure B-1 and a more complete description of the measurement is included there.

Measurement setup

As mentioned before, a broadband Santac laser was used which is actually the combination of three different laser sources. A fiber was connected to the laser and

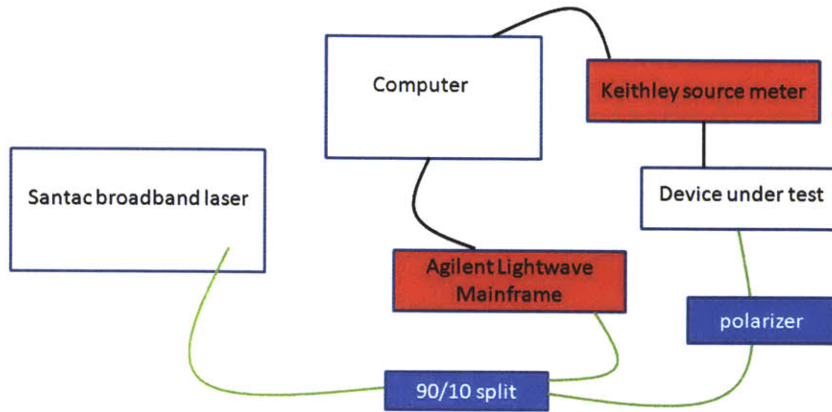

Figure B-1: A schematic diagram of the photoresponse measurement setup. The red boxes are the measurement instruments and the blue boxes are optical instruments. Furthermore, the green lines represent optical signals while the black ones represent electrical signals.

eventually split so that 90% of the light went to the device and 10% went to a lightwave mainframe that measured the output power of the laser. This split served as the power measurement of the laser. The rest of the light was then coupled to the device under test (DUT) either using a lensed fiber with a ~3 μm spot size or a cleaved fiber with a ~10 μm spot size. The fibers were chosen based on the size of the device. Large devices almost always used a cleaved fiber while small devices and waveguide-integrated devices always used a lensed fiber. The fibers went through three polarizers before reaching the DUT so that the polarization could be changed by the user.

The fiber was brought to the measurement setup stage and mounted on a custom-machined fiber mount. The fiber could then be positioned with the use of 3 micrometers. The DUT was place on a custom-machined stage and electrical contact was made using a standard probe. The current was measured using a Keithley source meter (though previous iterations used an Agilent parameter analyzer). A diagram of the system can be seen in Figure B-1.

Jason Orcutt wrote python and Matlab scripts which controlled the power from the laser and the voltage applied to the device using GPIB. These scripts also sensed

the output current of the device and saved them as Matlab data files. Python was used for responsivity measurements while Matlab was often used to measure the current versus voltage curve.

Each time a new set of measurements was going to be made, the setup had to be calibrated using a known device. To that end, a germanium photodiode from Thor Labs was purchased. Thor Labs measured the responsivity of the device from 800 nm to 1700 nm in increments of 10 nm. By measuring the Thor Labs device, a comparison could be made with the measured responsivity and the known responsivity and calibration coefficients could be determined at different wavelengths.

To measure new devices, a device was placed on the stage and contacted with a probe. A standard current versus voltage curve was taken in the dark and the data was saved. Next, the fiber had to be positioned carefully. The positioning of the fiber was a little different for vertically-coupled devices and edge-coupled devices and will be described separately.

Positioning of fiber for vertically-coupled devices

This fiber positioning system was used for all stand-alone vertical *pin* devices. The fiber was positioned over the DUT. Using a camera mounted on the table, the vertical distance from the laser to the DUT could be observed (but not measured with good accuracy). Using the micrometers, the fiber was lowered to an estimate of the focal length of the beam to ensure that as much light as possible was coupled into the device itself and not scattering to the field regions. To make sure the fiber was accurately placed, the laser was turned on and a bias (usually -1 V) was applied to the DUT. The fiber was moved in the x, y, and z directions using the micrometers while the output current was monitored on the Keithley. When the position which generated the maximum current was reached, the polarizers were moved to make sure the output current was at its maximum. For the vertically-coupled devices, the polarizers did

not change the signal by much. A few iterations of using the micrometers and the polarizers were done to ensure that the maximum signal was attained.

Positioning of the fiber for edge-coupled devices

This fiber positioning system was used for all waveguide-integrated devices. For these devices, the samples were cleaved carefully using a die saw and the sides were polished to give a clean waveguide surface on the edge of the test chip. The fiber was mounted horizontally rather than vertically and moved close to the edge of the chip. Using the optical microscope, the fiber was positioned close to the waveguide of interest. Making sure the fiber and the edge of the chip were both in focus at the same time, gives a reasonable starting position for alignment. The laser was then turned on. Using an infrared camera mounted to the microscope, it is possible to see the light being coupled into the waveguide. The z position was varied to get the light to travel as far down the waveguide as possible. After the z position was determined, a voltage was applied to the device and the current was monitored on the Keithley. The fiber was moved in the x and y directions to maximize the current. (At this point, the fiber may be moved in the z direction a bit, but a lot of adjustment should be unnecessary.) Finally, the polarizers were adjusted to maximize the output current of the DUT. It should be noted that the waveguides fabricated in this study were often highly polarized and, by using the polarizers, the responsivity could increase by as much as 10X.

Measurement and responsivity calculations

Once the fiber was positioned, contact was made to the device again using the probes and the python routine "responsivity.py" was run. This routine controls the wavelength and power of the laser and measures the ouptut current of the device. Typically, vertical devices were measured from 1300 nm to 1600 nm while waveguide-integrated

devices were measured from 1540 to 1600 nm. This was because the waveguides were highly polarized and outside of that wavelength range, the responsivity would be very small and recalibrating the polarization for different wavelength ranges is very time consuming. Two or three different power levels were used from the laser and the current was measured at each.

After the raw data was measured, the numbers had to be processed a bit to get an accurate measurement of the responsivity. First, the current/power ratios were either averaged (for two powers) This is where the calibration coefficients were used. By comparing the measured photoresponse on the Thor Labs diode to the calibrated response given by the company, scaling coefficients could be determined. These scaling coefficients were then used to calculate the accurate value of the responsivity of the test devices. MATLAB code that both calculated the calibration coefficients and the final responsivity values is included below.

It should be noted that the Python responsivity routine often used three output powers, but the lowest one usually did not work, so those data points were ignored. The responsivity was then calculated by averaging the other two measured values (and multiplying by the calibration coefficient for the corresponding wavelength). Furthermore, the Thor Labs diode had measured responsivities spaced at every 10 nm and sometimes the measurement was taken at every 5 nm. In this casse, the calibration coefficients were interpolated to generate data for the Thor Labs diode at the intermediate steps.

MATLAB code to calculate responsivities

%{

First read in correction factors. 'correctionfactor.txt' is a text file with the correction coefficients calculated from multiplying the measured responsivity on the Thor Labs diode with the actual responsivity as given on the data sheet.

```
%}

corr_factor = textread('correctionfactor.txt');
corr_factor(31)=1.284;

%Need to interpolate correction factors in between

for i=1:30
    corr_factor_interp(2*i-1) = corr_factor(i);
    corr_factor_interp(2*i) = (corr_factor(i)+corr_factor(i+1))/2;
end

corr_factor_interp(61) = corr_factor(31);

%Dark current values at different voltages

Idark_0V = 8.04e-10;
Idark_1V = 3.1e-7;
Idark_3V = 1.04e-6;

%Read in wavelengths

waves = responsivity_data(:,1);

%At 0 V

power_meas_0V = [responsivity_data(:,3), responsivity_data(:,5), responsivity_data(:,7)];
```

```
power_corr_0V = power_meas_0V*9; %to nominally correct for 90/10 split

I_photo_meas_0V = [responsivity_data(:,4), responsivity_data(:,6), responsivity_data(:,8)];
I_photo_corr_0V = I_photo_meas_0V - Idark_0V;

R_meas_0V = I_photo_corr_0V./power_corr_0V;
R_0V = (R_meas_0V(:,2) + R_meas_0V(:,3))/2;

R_corr_0V = R_0V.*corr_factor_interp.';

%At -1 V

power_meas_1V = [responsivity_data(:,10), responsivity_data(:,12), responsivity_data(:,14)];
power_corr_1V = power_meas_1V*9; %to nominally correct for 90/10 split

I_photo_meas_1V = [responsivity_data(:,11), responsivity_data(:,13), responsivity_data(:,15)];
I_photo_corr_1V = I_photo_meas_1V - Idark_1V;

R_meas_1V = I_photo_corr_1V./power_corr_1V;
R_1V = (R_meas_1V(:,2) + R_meas_1V(:,3))/2;

R_corr_1V = R_1V.*corr_factor_interp.';

plot(waves, R_corr_0V, waves, R_corr_1V);

%At -3 V
```

```
power_meas_3V = [responsivity_data(:,17), responsivity_data(:,19), responsivity_data(:,21)];
power_corr_3V = power_meas_3V*9; %to nominally correct for 90/10 split

I_photo_meas_3V = [responsivity_data(:,18), responsivity_data(:,20), responsivity_data(:,22)];
I_photo_corr_3V = I_photo_meas_3V - Idark_3V;

R_meas_3V = I_photo_corr_3V./power_corr_3V;
R_3V = (R_meas_3V(:,2) + R_meas_3V(:,3))/2;

R_corr_3V = R_3V.*corr_factor_interp.';

plot(waves, R_corr_0V, waves, R_corr_1V, waves, R_corr_3V);

%Generates matrix with wavelengths and responsivities at different biases

R_tot = [waves, R_corr_0V, R_corr_1V, R_corr_3V];
```

Appendix C

Inducing strain in blanket Ge-on-Si

This appendix describes attempts to induce strain in photodiodes frabricated from blanket Ge-on-Si. The diodes in this appendix were all fabricated using the mesa isolation flow described in chapter 4. The goal was to use backside metallization to induce bowing in the wafer and increase the tensile strain in the germanium film. Efforts were ultimately unsuccessful.

C.1 Wafer bending theory

So-and-so *et al.* reported an increase in strain due to backside silicidation [36]. It was found that 2 μm of silicide deposited on the back of the wafer increased the strain in the frontside Ge by 0.05%. The strain in a thin film deposited on a wafer can be given by

$$\sigma_f = \frac{E_s d_s^3}{6(1-\nu_s) R d_f^2 (1 + d_s/d_f)} \tag{C.1}$$

where σ_f is the strain in the film, R is the radius of curvature of the substrate, E_s and ν_s are Young's modulus and Poisson's ratio of the substrate, and d_s and d_f are the thicknesses of the substrate and the film respectively [116]. Furthemore, if the

radius of curvature is much larger than the radius of the wafer, L, then the stress in the film can be related to the bow in the wafer and the equation becomes

$$\sigma_f = \frac{E_s d_s^3 B}{3(1-\nu_s)L^2 d_f^2 (1+d_s/d_f)} \tag{C.2}$$

where all variables are defined as above, B is the wafer bow, and L is the wafer radius. It should be noted that, in the above equations, the "film" is the film that is deposited on the substrate. For the samples in this work, the germanium on the top of the wafer and the metal on the back of the wafer should each follow this equation. Since the germanium has some residual stress from the high temperature growth, there is already a bow in the wafer. The metal on the backside should act to increase the overall bow in the wafer. To increase the overall bow the most, a high stress metal should be used on the back. It was further hypothesized that the substrate should be thinned, although the implications of this will be described in later sections.

C.2 Fabrication

After devices were fabricated using the mesa flow, different metals were sputtered onto the backsides of the wafer using the AJA Sputterer in the exploratory materials lab (EML). Both aluminum and tungsten were used. Since tungsten is a very high stress material, it was found that $\sim$0.25 μm could be deposited before the film started to flake. Aluminum is a much lower stress material, so up to 1 μm was used. The KLA-Tencor FLX tool in TRL was used to measure the bow in the wafer.

Wafer thinning was also studied. Samples were thinned to $\sim$300 μm (normally the thickness was $\sim$675 μm) by MIT Lincoln Laboratory and tungsten was deposited on the back of these thinned samples.

It should be noted that the samples in this study were smaller than a full wafer. The full wafers were usually cleaved in quarter wafer samples to make studying dif-

ferent metallization methods easier.

C.3 Results

Figure C-1 shows the responsivity versus wavelength curves for 200 x 200 μm devices passivated with Al_2O_3 fabricated with a mesa etch. There is no appreciable difference in all the curves, indicating that the backside metallization did not substantially change the strain in the film. Aluminum is a low-stress metal, so the lack of increasing strain is somewhat expected. Furthermore, it is possible that when the sample was thinned, some of the original tensile strain in the germanium film was lost and the additional W could not replace it. It is unclear why the W sample did not show a marked difference in responsivity, but perhaps the limited thickness of the W film is at fault.

It is hypothesized that in order to increase the strain in the devices, the strain must be more localized and closer to the device itself. This would involve putting a high stress film either over the top of the device (similar to the high stress nitride layer in state-of-the-art nMOSFETs) or surround the device with a high stress film. Unfortunately, photolithography limitations in MTL prohibit that from happening.

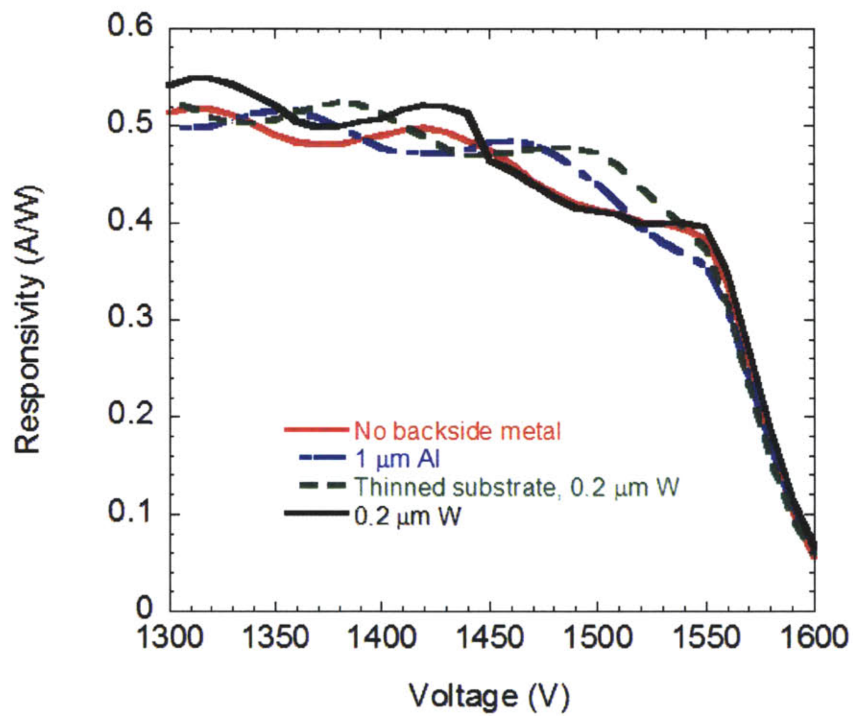

Figure C-1: Responsivity versus wavelength curves for 200 x 200 μm devices with various backside metallization schemes. These devices were fabricated using a mesa etch and passivated with Al_2O_3. Different backside metallization schemes had virtually no effect on the responsivity.

Appendix D

Frequency response of diodes fabricated in selectively-grown Ge-on-Si

Diodes fabricated in selectively-grown Ge-on-Si were made as part of a high speed analog-to-digital converter effort. The frequency response of these devices was measured by Jason Orcutt to measure the bandwidth of the devices. Due to the length of time required to run a measurement, only a few devices were measured. Results from both vertical *pin* devices and waveguide-integrated lateral *pin* devices are presented here.

D.1 Frequency response of vertical devices

Figure D-1 shows the frequency response of a 100 x 100 μm vertical *pin* structure. The germanium is 2 μm thick. The bandwidth is $\sim$3 GHz and changes slightly with applied bias. This frequency response of this device is likely limited by the RC time constant of the device due mainly to a large series resistance. The current versus voltage characteristic can be seen in Figure D-2.

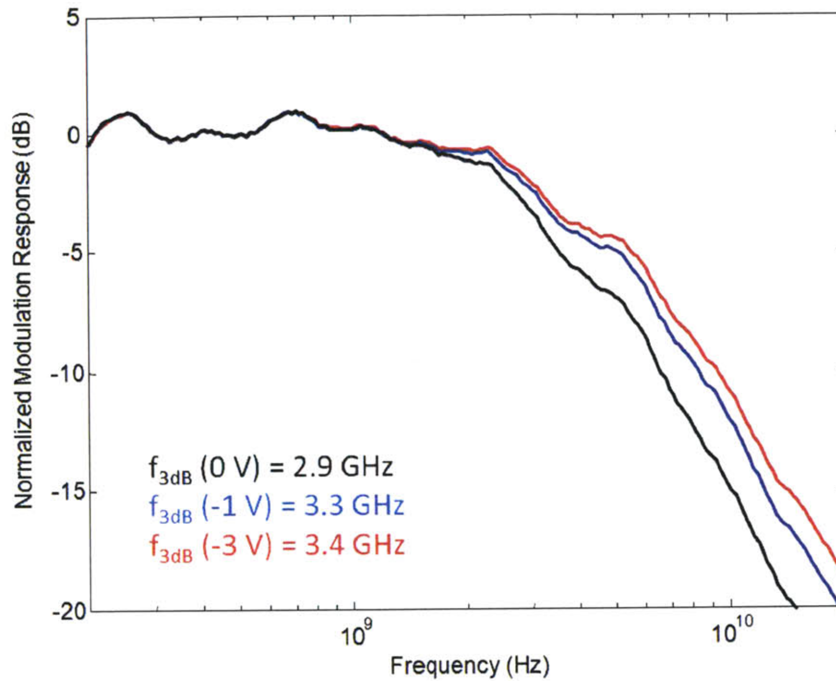

Figure D-1: Frequency response of a vertical *pin* device. The device is 100 x 100 μm square fabricated on wafer #5365. The bandwidth is ~3 GHz and changes only slightly with applied bias. Measurement courtsey of Jason Orcutt.

D.2 Frequency response of waveguide-integrated devices

The waveguide-integrated devices with measured frequency response are the ones described in section 3.5.1 grown on 50 nm of silicon. The frequency response for a 100 μm long device is shown in figure D-3 for different biases. The bandwidth of these devices is ~1 - 2 GHz. Based on some estimates of the series resistance and the capacitance of the device, the frequency response is likely not RC limited but rather limited by either germanium passivation problems or the material quality. Since the germanium is grown in a trench of silicon, the germanium will grow from three directions (rather than just one for stand alone devices). These additional Ge/Si interfaces likely increase the threading defects in the film. Furthermore, the films are not cyclically annealed after growth (to minimize dopant diffusion from the Si wings),

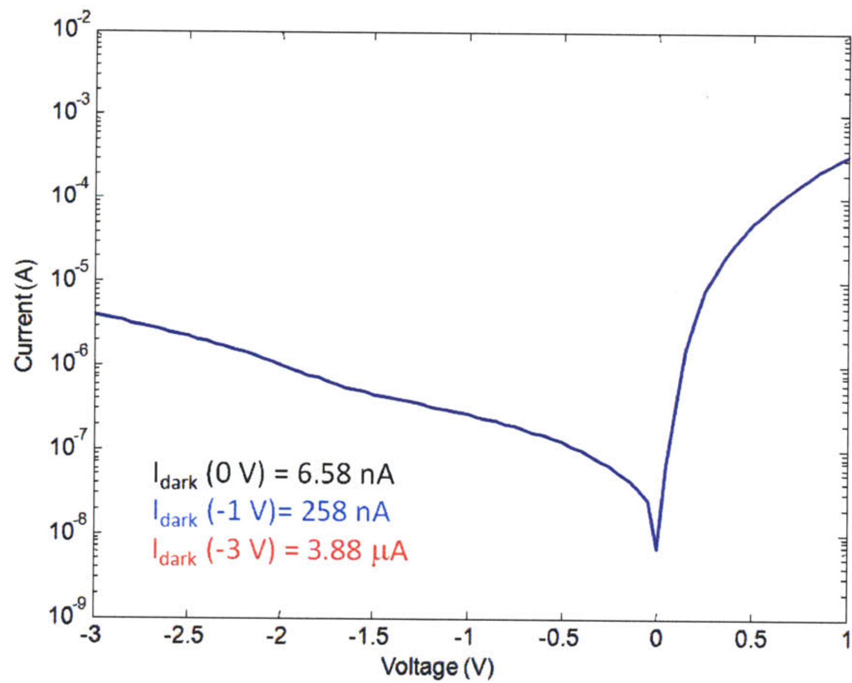

Figure D-2: Current versus voltage characteristic of a vertical *pin* device. The device is 100 x 100 μm square fabricated on wafer #5365. The series resistance on this device is $\sim$1000 Ω, limiting the bandwidth to $\sim$3 GHz. Measurement courtsey of Jason Orcutt.

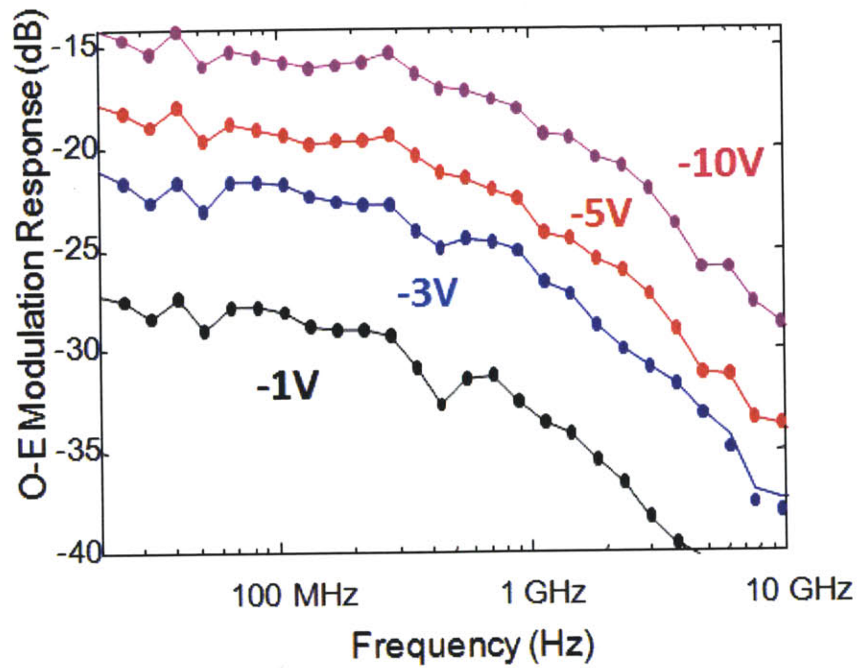

Figure D-3: Frequency response of a waveguide-integrated device. The device is 100 μm long and has a 3 dB bandwidth of 1 - 2 GHz. Measurement courtsey of Jason Orcutt. From wafer #5800.

leaving a high defect density.

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