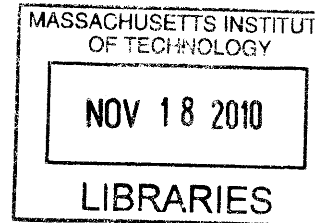
Fabrication and Electrical Characterization of Transistors made from Carbon Nanotubes and Graphene

by

Daniel Andrew Nezich

B.S., Michigan Technological University (2003)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Submitted to the Department of Physics
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2010

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Abstract

Carbon nanotubes and graphene are low-dimensional allotropes of carbon which exhibit novel mechanical and electrical properties. The methods for producing these materials and fabricating electronic devices from them are still under development. This thesis uses the fabrication and electronic analysis of field-effect transistors made from carbon nanotubes and graphene to gain insights into the growth process of these materials, to understand complications of the fabrication process, and to assess the quality of the materials through their electronic properties.

The numbers of semoconducting and metallic nanotubes produced by growth using two different catalysts are counted by the process of electrical cutting. Various high-current phenomena are observed and explained through use of multi-nanotube and charge leakage models. The high-current annealing method discovered for nanotubes is found to also be useful for improving the quality of graphene devices.

The graphene used for device fabrication is produced by thermal chemical vapor deposition on thin film nickel. The large area and weak adhesion of this material leads to the alteration of device designs and fabrication procedures, including substrate exposure and high-temperature annealing. A new nanofluidic device is introduced to study the enhanced lateral wet etching rate of materials in contact with graphene.

Two sets of graphene field-effect transistors are analyzed, a first for this type of material. Improved material quality results in improved electrical mobility. Two independent models are derived which relate the thickness of a graphene film to its gate-voltage dependent behaviour, and are justified by experiment. Temperature dependence, quantum capacitance, and multiterminal measurements are discussed.

Thesis Supervisor: Jing Kong
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Acknowledgments

I would first like to thank my advisor Jing Kong, for her guidance and support throughout my graduate career, and for her positive attitude, encouragement, and openness to discussion which saw this thesis work through to completion. I would also like to thank my co-advisor, Mildred Dresselhaus, who supervised my first year year and a half at MIT and has been an inspirational model of diligence and expertise, and her husband Gene Dresselhaus, who has been a source of timely advice, reminders, and levity. I am grateful to have worked with many excellent colleagues and friends both past and present in the the NMELAB and MGM groups, and would like to acknowledge especially those I have worked with for many years and through multiple research projects and chicken wings: Hootan Farhat, Alfonso Reina, Mario Hofmann, Kyeong-Jae Lee, Hyung-Bin Son, Shin Grace Chou, Georgii Samsonidze, Eduardo Barros, Federico Villalpando, Ying Feng, Ya-ping Hsieh, Xiaoting Jia, and Ming Tang. I have also had the pleasure to work with Liming Xie, Allen Hsu, Hyesung Park, Jessica Campos-Delgado, and many others who I have known for a shorter time, but who each have been a pleasure to collaborate with. I would also like to thank the timely efforts of our adiminstrative assistants, especially Laura Doughty who has helped me numerous times with organization, information, and advice.

I have been lucky to have collaborated with many people outside my own research group, in joint research projects and in sharing of facilities. For access to the NSL, fabrication training, and assistance with e-beam lithography I thank Professor Karl Berggren, Joel Yang, and Huigao Duan. For work with graphene mobility and frequency doubling devices I thank Professor Tomás Palacios, José Maria Tirado, and Han Wang. For useful discussions regarding electrical transport in graphene, and for equipment training and usage, I thank Professor Pablo Jarillo-Herrero, Michele Zaffalon, Britt Baugher, Thiti Taychatanapat, Javier Sanchez-Yamagishi, and Joel I-Jan Wang. For access to and training for e-beam lithography, and for scanning capacitance measurements with graphene, I thank Professor Ray Ashoori, Albert Wang, and Eric Lin. For fabrication equipment training and use I thank Professor Marc

Baldo, Professor Vladimir Bulović, Mihai Bora, Kaveh Milaninia, and Tim Heidel. For microfabrication training and advice in the EML and NSL I thank Kurt Broderick and Jim Daley. I also would like to acknowledge those with whom I have worked as a teaching assistant, for their guidance in my experience of this other aspect of academic life: Professors Richard Yamamoto (now deceased), Ulrich Becker, Pablo Jarillo-Herrero, and George Benedek, as well as Scott Sewell and Sean Robinson. To all these people and the many others I have worked with during my time at MIT who are too numerous to list but who have contributed to my rich graduate experience, my sincere gratitude.

I have been truly blessed in the love and emotional support, throughout my life and educational career, of my God, my parents Dennis and Laura Nezich, my siblings Valerie, Alexander, Catherine, Jonathan, Christina, and Marianne, my grandparents Stella and Edward "Boomie" Mikrut, and Dolores and Andrew Nezich (now deceased), and also Margart and Donald Cady and the rest of my extended family. I have also had the pleasure to make many good friends during my years at MIT, known collectively as Puffywumps (Puffysocials) and Mean People; thank you all for sharing with me a life outside of the laboratory. I especially thank Ryan Lang, my roommate of five years and my link to the social world and to reality television. And last but not least I thank Laura Cerritelli, my girlfriend and strongest support through the most difficult periods of my graduate work.

Contents

1 Introduction **19**

2 Background **23**

2.1 Graphene 23

2.2 Nanotubes 29

3 Nanotube and Graphene Device Fabrication **33**

3.1 Nanotube Production:
Thermal Chemical Vapor Deposition 34

3.1.1 Catalyst Preparation 34

3.1.2 Substrate Preparation 37

3.1.3 Catalyst Deposition 38

3.1.3.1 Dip-Coat 38

3.1.3.2 Drop-Coat 38

3.1.3.3 Drawing 39

3.1.4 Growth of Single Wall Carbon Nanotubes 39

3.1.4.1 Catalyst Recipe C02 39

3.1.4.2 Catalyst Recipe Mcat 40

3.2 Graphene Production 41

3.2.1 Mechanical Exfoliation 42

3.2.2 Thermal Chemical Vapor Deposition 43

3.2.2.1 Growth Method 44

3.2.2.2 Growth Observations 44

3.2.2.3 Transfer Method 48
3.3 Fabrication Equipment and Procedures 49
3.3.1 Thermal Chemical Vapor Deposition 50
3.3.2 E-Beam Lithography 52
3.3.2.1 PMMA E-Beam Resist 52
3.3.2.2 HSQ E-Beam Resist 55
3.3.2.3 JEOL 5910 SEM 55
3.3.3 Optical Lithography 56
3.3.3.1 S1813 Positive Resist 57
3.3.3.2 AZ5214-E Image Reversal Resist 58
3.3.3.3 Mask Fabrication 59
3.3.4 Metal Evaporation 60
3.3.5 Oxygen Plasma 61
3.3.6 Atomic Layer Deposition 62
3.4 Device Design and Fabrication 62
3.4.1 Nanotube Devices 63
3.4.1.1 Substrate Description 63
3.4.1.2 Fabrication 65
3.4.2 Exfoliated Graphene Devices 67
3.4.2.1 Fabrication 67
3.4.3 CVD Graphene Line Devices 69
3.4.3.1 Fabrication 71
3.4.3.2 Device Design 73
3.4.4 Edge Devices 74
3.5 Fabrication Challenges for Graphene 78
3.5.1 Graphene Enhancement of Wet Etch Rates 78
3.5.1.1 Hydrofluoric Acid Etching 78
3.5.1.2 Chromium Etching 82
3.5.2 Weak Adhesion of Graphene to the Substrate 93
3.5.2.1 Delamination under Thin Film Stress 94

3.5.2.2 Metal Delamination under Controlled Mechanical Force 95
3.5.2.3 Graphene Delamination under Controlled Mechanical Force 97
3.5.3 Lithography 99
3.5.3.1 Poor Photoresist Adhesion 99
3.5.3.2 Photoresist Crosslinking by Plasma 100
3.5.3.3 Photoresist Crosslinking by Overexposure 102
3.5.3.4 Lithography Residue Removal by Annealing 104

4 Nanotube Devices 109
4.1 Electrical Cutting 109
4.1.1 Method 110
4.1.2 Statistical Results 111
4.2 High-Bias Annealing 115
4.2.1 Lithography Residue 115
4.2.2 Crossing Nanotubes 117
4.3 Tier Effects 119
4.3.1 Double-Walled and Bundled Nanotubes 119
4.3.2 Impact Ionization 122
4.3.3 Optical Bump 123
4.3.4 P-N Junction Formation and Hysteresis 126
4.4 Conclusion 135

5 Two-Terminal Graphene Devices 137
5.1 Introduction 137
5.2 Device Fabrication 138
5.3 I-V Measurements 140
5.3.1 Measurement Procedure 140
5.4 Analysis Models 140
5.4.1 Single-Layer Graphene 141
5.4.2 Many-Layer Graphene 143

5.4.3 Single-Layer and Many-Layer Model Correspondence 144
5.4.4 Two Equivalent Analytic Forms 145
5.4.5 Model Choice 146
5.5 Analysis Procedure 148
5.5.1 Data Selection 148
5.5.2 Model Fitting Technique 150
5.6 Fitting Results 152
5.6.1 Model Correspondence 152
5.6.2 Fitting Parameter Distributions 154
5.6.3 Fitting Parameter Correlation 157
5.6.4 Model-Independent Parameter Correlation 160
5.6.5 Mixed Correlation 161
5.6.6 Thickness Calculation 163
5.7 Temperature Dependence 165
5.8 Conclusion 168

6 Lincoln Laboratory CVD Graphene Devices 171

6.1 Measurement Description 172
6.1.1 6-Terminal Devices 172
6.1.2 Van der Pauw Measurements 173
6.1.3 Capacitance Approximation 175
6.2 Two-Terminal Devices 177
6.2.1 Comparison to Graphene Line Devices 182
6.2.2 Top and Bottom Gating 184
6.2.2.1 Conductivity Map 185
6.2.2.2 Gate Voltage Series 186
6.2.2.3 Dirac Point Conductivity and Graphene Thickness Estimation 190
6.2.2.4 Converted Charge Coordinates 198
6.3 Hall Bar Devices 203

6.3.1 Cross Measurements 203
6.3.2 Linear Measurements 206

A SOP: E-Beam Lithography **211**

A.1 Overview 211
A.2 Pattern Design 212
A.3 NPGS Setup 214
A.4 SEM Setup 217
A.5 Writing the Pattern 220
A.6 Additional Notes 222
A.7 Alternate Runfile and Pattern Settings 227

B Gate Capacitance **231**

C Drift and Field-Effect Mobilities **235**

D Two Conductivity Fitting Models for Single-Layer Graphene **239**

E Abbreviations **245**

F Publications **247**

List of Figures

2-1 Graphene structure. 25

2-2 Graphene band structure. 27

2-3 Carbon nanotubes. 29

2-4 Carbon nanotube cutting lines. 31

3-1 Sample temperature during graphene growth. 45

3-2 CVD graphene on nickel, thickness boundaries. 46

3-3 CVD graphene on nickel, aperture used to image nickel grains. 47

3-4 CVD graphene transferred to SiO_2. 49

3-5 Thermal CVD system. 51

3-6 JEOL 5910 SEM. 56

3-7 Fonstad thermal evaporator. 60

3-8 Atomic Layer Deposition system. 63

3-9 Nanotube device optical images. 64

3-10 Nanotube device AFM image. 67

3-11 Exfoliated graphene device fabrication. 70

3-12 CVD graphene line device fabrication. 72

3-13 Chrome mask for CVD graphene line devices. 75

3-14 Hall bar device patterns. 76

3-15 Hall bar devices. 77

3-16 HF etch detached graphene. 80

3-17 HF etch collapsed metal pads. 81

3-18 Nanochannel fabrication process flow. 84

3-19 Etching of nanochannel with graphene. 85
3-20 Etching of nanochannel without graphene. 87
3-21 Etch rate of chromium nanochannel. 88
3-22 Bubble formation in nanochannel without graphene. 90
3-23 Optical interference in nanochannel without graphene. 92
3-24 Peeling metal leads. 94
3-25 Scratched metal pads. 96
3-26 Graphene cloverleaf device. 98
3-27 Cracked photoresist. 99
3-28 Plasma-baked photoresist. 101
3-29 Overexposed photoresist. 103
3-30 AFM of resist residue. 105
3-31 Temperature dependence of PMMA etch rate. 106
3-32 Graphene transfer by annealing. 108

4-1 Typical electrical cutting measurements. 112
4-2 AFM of electrically cut nanotubes. 113
4-3 Residue removal by solvent rinse. 115
4-4 Residue removal by high bias annealing. 116
4-5 High bias annealing of crossing nanotubes. 118
4-6 Diagram of Bundle vs. DWNT conduction. 120
4-7 Bias sweeps showing a threshold voltage. 121
4-8 Bias sweeps showing impact ionization. 122
4-9 Optical bumps in bias sweeps. 123
4-10 Optical bump sweep rate dependence. 125
4-11 Metallic tier. 127
4-12 Metallic tier time dependence. 128
4-13 Hysteresis in metallic nanotubes. 129
4-14 Hysteresis model. 131
4-15 Hysteresis fitting results. 134

5-1 Graphene and graphene line device. 139
5-2 Gate sweeps with good fit quality. 141
5-3 Band diagrams for graphene and graphite. 144
5-4 Histograms of device fitting parameters 1. 154
5-5 Histograms of device fitting parameters 2. 155
5-6 Histograms of transconductance mobility. 156
5-7 Histograms of model-independent fitting parameters. 160
5-8 Comparison of mobilities from fitting and slope. 163
5-9 Calculated thickness distributions. 164
5-10 Temperature dependence of CVD graphene devices. 166

6-1 Van der Pauw measurement connections. 173
6-2 Capacitance correction ratio. 177
6-3 Conductivity and mobility for top and bottom gating. 178
6-4 Mobility histogram for top and bottom gating. 181
6-5 Top vs. bottom gate mobility. 182
6-6 Conductivity dependence on top and bottom gate voltage. 185
6-7 Top and bottom gate sweeps. 187
6-8 Offset top and bottom gate sweeps. 188
6-9 Maximum mobilities for each gate voltage. 189
6-10 Dirac point conductivity analysis. 191
6-11 Transcendental thickness relation. 193
6-12 New potential coordinates related to gate voltages. 199
6-13 Conductivity dependence on charge densities Σ and Δ. 201
6-14 Conductivity variation with total charge Σ. 201
6-15 Conductivity variation with differential charge Δ. 202
6-16 Van der Pauw cross measurements. 204
6-17 Linear four-point measurements. 207

D-1 Resistor models of few-layer graphene conduction. 240

List of Tables

3.1 Catalyst recipes for nanotube growth. 35

3.2 Catalyst nomenclature. 35

3.3 Catalyst stock solutions. 36

3.4 Catalyst recipes from stock solutions. 36

3.5 Mcat recipe for nanotube catalyst. 37

4.1 Electrical cutting results. 113

5.1 Fitting uncertainties for model comparison. 153

5.2 Fitting parameters and uncertainties. 156

5.3 Fitting parameter correlation. 158

5.4 Data parameter correlation. 161

5.5 Mixed fitting and data parameter correlation. 162

5.6 Thickness fitting parameters. 165

6.1 Measurement descriptions. 172

6.2 Mobility of cross measurements. 205

6.3 Mobility of linear measurements. 208

A.1 E-beam lithography parameters. 218

B.1 Electrostatic capacitance values. 232

D.1 CVD graphene conduction model isomorphism. 244

Chapter 1

Introduction

This thesis work details the fabrication and electrical characterization of field-effect transistors made from carbon nanotubes and graphene which are grown by catalytic thermal chemical vapor deposition. The goal is to better understand the semiconducting and metallic nature of the materials produced by this growth method, in order to guide material growth and device design. Much of the work is exploratory in nature, providing a first observation and interpretation of various phenomena.

The primary approach to understanding these materials is though a statistical average of the electrical properties of many individual transistors, which was chosen due to the stochastic nature of the material growth. The electrical characterization consists primarily of conductivity measurements as a function of the gate-source voltage and drain-source voltage of the transistors. Most measurements are made at room temperature and in an ambient atmosphere, though additional measurements at low temperature and at low pressure for specific devices are discussed. These are supplemented by optical and atomic force microscope images.

Four main categories of results are presented. One chapter discusses device fabrication using both nanotubes and graphene. Another chapter discusses the measurement of nanotube devices. The final two chapters discuss the measurement of two sets of graphene devices. These discussions are preceded by an introduction to the physics of nanotubes and graphene, and a discussion of the measurements which were performed. The chapters containing measurements and their interpretation are

outlined briefly below.

The equipment and recipes used in this work for making nanotube and graphene field-effect transistors are described in Chapter 3. This includes both the growth of the nanotube and graphene materials by catalytic thermal chemical vapor deposition (CVD), and the design and procedures by which they are converted into field-effect transistors using conventional microfabrication equipment and techniques.

The large-area substrate coverage achieved by CVD graphene, compared to its conventional exfoliated form, provides unique fabrication challenges and opportunities. It is found in the course of this thesis work that graphene enhances the lateral wet etch rate of chromium films by a factor of 70, which is demonstrated by the construction of a novel nanofluidic channel device. The low interlayer bonding in graphite is also exploited through the use mechanical force as a means of defining and isolating graphene devices. Finally, this work resolves the issue of organic residue on devices through the development of a post-fabrication thermal annealing procedure. This procedure is demonstrated as an improved method of graphene transfer.

For this thesis, nanotubes are grown using a selection of similar catalysts, and fabricated into field-effect transistors which are studied in Chapter 4. Using a process called *electrical cutting*, where the nanotubes comprising the device channel are sequentially broken by application of a high drain-source voltage, the proportion of metallic to semiconducting nanotubes is determined. It is found that a catalyst containing molybdenum and iron shows no preference for producing semiconducting nanotubes over metallic nanotubes, while a catalyst containing only iron does, though with great variability. Additionally, an unexpected dependence is found where the number of bundled or multiwall nanotubes increases with the age of the catalyst.

The electrical cutting of nanotubes leads to a number of observations about measurements at high drain-source bias voltage. It is demonstrated that nanotubes can be cleaned of processing residue by the application of these high bias voltages, improving their current carrying ability. This technique proves useful for measurements of graphene devices. It is also found that metallic nanotubes exhibit an unusual double-peaked conduction as a function of gate voltage due to impurities, that evi-

dence of double-walled nanotubes is observed, and that impact ionization can be used to identify the imminent cutting of a nanotube and to ensure good cleaning of the nanotube. Two instances of time-dependent phenomena are observed, which are both explained by population of residue charge traps with a time constant of 6 seconds.

Graphene grown by the novel chemical vapor deposition method, pioneered in the Jing Kong group at MIT, is fabricated into two sets of field effect tansistors. The first set, discussed in Chapter 5, consists of simple back-gated transistors fabricated at MIT by the author out of a graphene film which has many multilayer regions. These transistors are the first ever fabricated from CVD graphene, and achieve an average field-effect mobility of 215 cm^2/Vs. Two models for the conduction in these devices, developed by the author, are presented, and their functional equivalence is shown to predict a relation between electrical measurements and independent measurements of device thickness. This relation is found to be experimentally satisfied, supporting treatment of the CVD graphene material as few-layer graphene. Temperature-dependent measurements are perfromed and support this interpretation.

The second set of graphene transistors was fabricated by collaborators at Lincoln Laboratory from a thinner, more uniform graphene film consisting of primarily 1-2 layers of graphene, and measurements perfomed on these devices by the author are discussed in Chapter 6. These transistors are top-gated as well as back-gated, with an average mobility of 400 cm^2/Vs, indicating an improved graphene material over the previous set of transistors. Top gating showed a decreased mobility, which is attributed to quantum capacitance and interface defects. The implication of electronic screening is discussed, resulting in an independent prediction relating electrical measurements and the graphene thickness which is experimentally verified. Hall bar geometry measurements show that the true mobility of these devices is above 1000 cm^2/Vs, indicating that contact effects are significant for simple two-terminal measurements.

The results presented in this thesis comprise a basis of practical knowledge for fabrication of CVD graphene transistors using simple processing techniques, and provide the first electronic characterization of this material.

Chapter 2

Background

This chapter introduces the materials of graphene and carbon nanotubes, and provides a brief overview of their physical structure and electronic properties. Much of this material is discussed in more detail in the literature [1].

Carbon nanotubes and graphene are closely related materials, and are allotropes of carbon which exhibit primarily sp^2 bonding. Graphene is a two-dimensional lattice of carbon atoms arranged in hexagons, and is a zero-bandgap semiconductor. Commonly, carbon nanotubes are described as graphene which has been cut, rolled, and rejoined into a seamless cylinder. A typical nanotube has a diameter of 1-3 nm, and experiences quantum confinement along this direction, making nanotubes a quasi-one-dimensional material. Carbon nanotubes may be semiconducting or metallic.

All three types of electronic behaviour are studied in this thesis. It is natural to discuss the structural and electronic properties of graphene first, and then extend these results to the case of carbon nanotubes. This procedure is followed below.

2.1 Graphene

Previously, it was thought that isolated graphene, a single atomic layer of graphite, was thermodynamically unstable, though this has since been shown to not be the case [2, 3, 4]. Early research in graphite led to near approaches to graphene, though, in the form of thin graphite films which had been isolated through intercalation (first

performed in 1841 and later studied from the 1930's onward, for a review see [5]), chemical exfoliation (1962, [6, 7]), or growth on top of metal films (1965, for a review see [8]). The widespread study of graphene began only after high-quality samples were isolated on an insulating substrate in 2004 [2].

Graphene is of great interest to the electronics community because it demonstrates colossal intrinsic field-effect mobility [9, 10, 11], high thermal conductivity [12], high current density [2, 13], and transparency [14]. Currently, the highest quality electronic devices are fabricated from graphene which is deposited on a substrate by mechanical exfoliation [2]. The typical dimensions of the graphene randomly deposited by this method are 10 μm to 100 μm [2, 15]. While these graphene sheets are sufficient for research studies, eventual application of graphene in large scale electronics will require graphene which can be deterministically placed on a substrate, which would ideally take the form of wafer-scale sheets of graphene. Two previously described methods which can achieve this scaling are the annealing of silicon carbide [16, 17, 18] and the reduction of graphene oxide [19, 20, 21]. This thesis works primarily with graphene obtained by another method, the thermal chemical vapor deposition (CVD) of graphene on thin nickel films [22].

Graphene is the name given to a single atomic layer of the three-dimensional crystal graphite (a common solid lubricant, well-known for its use in pencil "lead"). Graphene is a two-dimensional crystal with a two atom unit cell. The atoms are arranged in hexagons. This is illustrated in Figure 2-1(a). The following discussion draws heavily from [1].

In a cartesian coordinate system, the lattice is described by primitive vectors

$$\vec{a}_1 = \frac{3}{2}a\hat{x} + \frac{\sqrt{3}}{2}a\hat{y} = \sqrt{3}a\left(\frac{\sqrt{3}}{2}, \frac{1}{2}\right) \quad \vec{a}_2 = \frac{3}{2}a\hat{x} - \frac{\sqrt{3}}{2}a\hat{y} = \sqrt{3}a\left(\frac{\sqrt{3}}{2}, -\frac{1}{2}\right) \tag{2.1}$$

and basis vectors

$$\vec{\delta}_0 = (0,0) \qquad \vec{\delta}_1 = a\,(1,0) \tag{2.2}$$

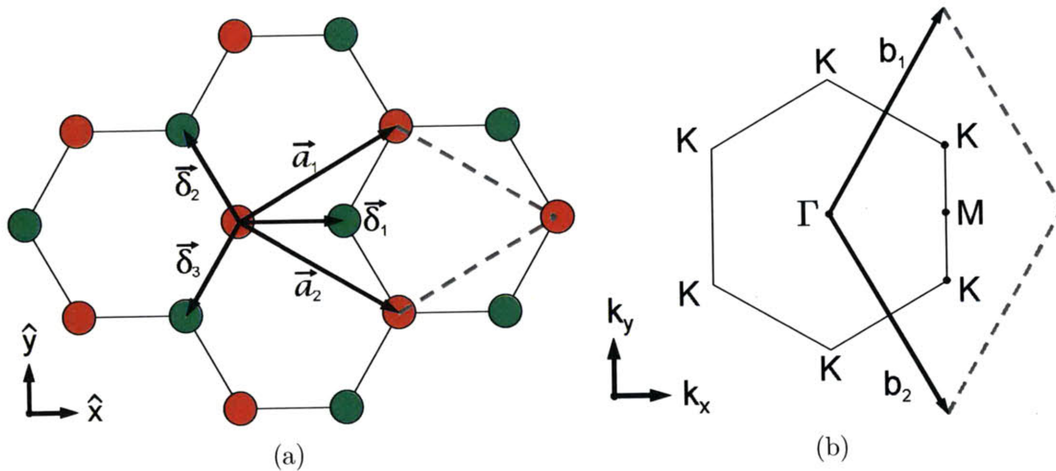


Figure 2-1: (a) Diagram of the arrangement of carbon atoms (circles) in graphene. Carbon atoms of each of the two sublattices are marked in red and green. The primitive vectors of the lattice are $\vec{a}_1$ and $\vec{a}_2$. The vectors $\vec{0}$ and $\vec{\delta}_1$ are the basis vectors corresponding to these primitive vectors. A unit cell may be taken to be one of the outlined hexagons, or the rhombus created by the primitive vectors and the dotted grey lines. Nearest neighbors to the central red atom are offset by the vectors $\vec{\delta}_i$. (b) Diagram of graphene in reciprocal space with primitive vectors $\vec{b}_1$ and $\vec{b}_2$. The first Brillouin zone is a hexagon rotated 30° with respect to the hexagons of the real space lattice, or alternatively a rhombus created by the primitive vectors and the dotted grey lines. High-symmetry points are given the conventional labels Γ, M, K, and K'. The K and K' points are not identical due to the two unit basis.

and reciprocal lattive vectors

$$\vec{b}_1 = \frac{2\pi}{3a/2}\left(\frac{1}{2}, \frac{\sqrt{3}}{2}\right) \qquad \vec{b}_2 = \frac{2\pi}{3a/2}\left(\frac{1}{2}, -\frac{\sqrt{3}}{2}\right) \tag{2.3}$$

where $a = 1.421$ Å is the carbon-carbon spacing, so that the length of the basis vectors $a_1 = a_2 = \sqrt{3}a = 2.461$ Å [23]. These distances are small compared to the graphite lattice spacing perpendicular to the graphene plane $a_{3,\perp} = 3.355$ Å. The corresponding densities of graphene and graphite are thus

$$\begin{aligned}
n_{2D} &= \frac{N_\delta}{A_{\text{cell}}} = \frac{N_\delta}{|\vec{a}_1 \times \vec{a}_2|} = \frac{(2 \text{ atoms/cell})\left(10^{16} \text{ Å}^2/\text{cm}^2\right)}{\left|\left(\frac{3}{2}, \frac{\sqrt{3}}{2}\right) \times \left(\frac{3}{2}, -\frac{\sqrt{3}}{2}\right)\right| \left(1.421^2 \text{ Å}^2/\text{cell}\right)} \\
&= 3.812 \times 10^{15} \text{ atoms/cm}^2 &(2.4)\\
\rho_{2D} &= \frac{M_W}{N_A} n_{2D} = \frac{12.0107 \text{ g/mol}}{6.022 \times 10^{23} \text{ atoms/mol}} \left(6.43 \times 10^{15} \text{ atoms/cm}^2\right) \\
&= 7.604 \times 10^{-8} \text{ g/cm}^2 &(2.5)\\
n_{3D} &= n_{2D}/a_3 = \frac{3.812 \times 10^{15} \text{ atoms/cm}^2}{(3.355 \text{ Å})(10^{-8} \text{ cm/Å})} \\
&= 1.136 \times 10^{23} \text{ atoms/cm}^3 &(2.6)\\
\rho_{3D} &= \rho_{2D}/a_3 = \frac{7.604 \times 10^{-8} \text{ g/cm}^2}{(3.355 \text{ Å})(10^{-8} \text{ cm/Å})} \\
&= 2.267 \text{ g/cm}^3 &(2.7)
\end{aligned}$$

The graphene band structure may be obtained from a first-nearest-neighbor simple tight-binding model using only the p_z (out of plane) orbitals as (Equations 2.27 and 2.28 in Reference [1]):

$$E_{g2D}(\vec{k}) = \frac{\epsilon_{2p} \pm tw(\vec{k})}{1 \pm sw(\vec{k})} \tag{2.8}$$

$$w(\vec{k}) = \sqrt{1 + 4\cos\left(\frac{3k_x a}{2}\right)\cos\left(\frac{\sqrt{3}k_y a}{2}\right) + 4\cos^2\left(\frac{\sqrt{3}k_y a}{2}\right)} \tag{2.9}$$

where the overlap integrals for nearest-neighbor electrostatic interaction energy t and

nearest-neighbor overlap integral s are empirically determined to be $t = -3.033$ eV and $s = 0.129$, and the self-energy of a p_z orbital can be defined to be $\epsilon_{2p} = 0$. The resulting band diagram is shown in Figure 2-2(a). An extension of this method to include the remaining $n = 2$ orbitals (2σ, p_x, and p_y), results in the band diagam shown in Figure 2-2(b).

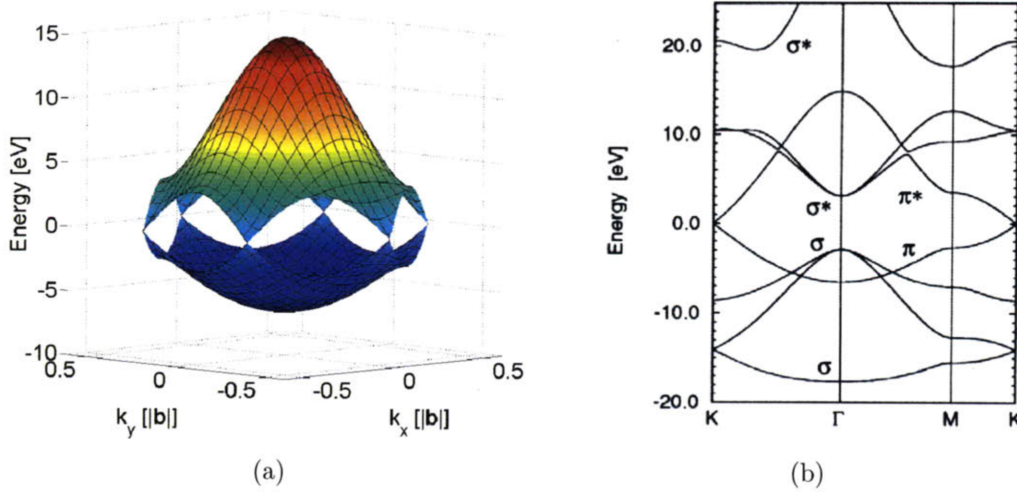


Figure 2-2: Graphene band structure. (a) Valence and conduction bands resulting from the p_z orbital. (b) Reproduction of Figure 2.8 in Reference [1]. Tight binding energy bands along the high-symmetry lines indicated in Figure 2-1(b), for all orbitals at the second quantum level. The bands of (a) are labeled π and π^*, and are the only bands that contribute to conduction at moderate energies.

Each carbon atom contributes four electrons to bonding at the $n = 2$ level. Since there are as many states in the Brillouin zone as there are atoms in the crystal, this means that the lowest four bands of Figure 2-2(b), labeled σ and π, are filled. The Fermi energy of graphene thus lies at the K (and K') points, where the fully-occupied π band touches the fully-unoccupied π^* band. This corresponds to the six corners of the hexagonal Brillouin zone, and is seen clearly in Figure 2-2(a) where the upper and lower bands touch. The point where the valence and conduction bands meet is called the Dirac point.

The conduction and valence bands in the vicinity of the Dirac points is conical (there is one Dirac point each at point K and at point K'). This can be seen by defining a new wavevector $\vec{k'} = \vec{k} - \vec{K}$, where $\vec{k}$ is the usual wavevector in reciprocal

space and $\vec{K}$ is the wavevector from the high symmetry point Γ to the symmetry point K (*i.e.*, ΓK). By substituting this definition into Equation 2.8 and restricting the analysis to regions near the K point ($|\vec{k'}| << 1/a$), it is found that the dispersion $E(\vec{k})$ is linear in the wavevector from the K point:

$$E^{\pm}(\vec{k'}) = \pm\frac{3a|t|}{2}|\vec{k'}| \tag{2.10}$$

where the ($\pm$) notation refers to the valence ($-$) or conduction ($+$) band. The error in this approximation is quadratic in $|\vec{k'}/\vec{K}|$. A similar analysis applies also to the Dirac point at the K' symmetry point. It is conventional to take the prime of k' as implicit, and this will be assumed in all further discussions.

The Fermi velocity v_F, defined as $(1/\hbar)(dE/dk)$, is readily obtained from Equation 2.10:

$$v_F = \frac{3at}{2\hbar} = \frac{3(1.421 \times 10^{-10}\ \mathrm{m})(3.033\ \mathrm{eV})}{2(6.582 \times 10^{-16}\ \mathrm{eVs})} \approx 9.8 \times 10^5 \frac{\mathrm{m}}{\mathrm{s}}. \tag{2.11}$$

This velocity is aproximately 1/300 of the speed of light. It is worth noting another similarity to light; namely that the electrons and holes in graphene are *massless* just as photons are. The effective mass of a carrier m^* is the second derivative of the dispersion $m^* = (1/\hbar^2)(d^2E/dk^2)$ which is clearly zero for the linear bands of Equation 2.10.

The density of states $n(E)$ of graphene can be found as

$$n(E) = \frac{g_s g_v}{2\pi(\hbar v_F)^2}|E| \tag{2.12}$$

where $g_s = 2$ is the spin degeneracy and $g_v = 2$ is the so-called valley degeneracy for the two Dirac points at the K and K' symmetry points. It is this electronic density of states which plays an important role in the electrical transport of graphene.

2.2 Nanotubes

Nanotubes appear as long cylinders of a hexagonal lattice of carbon atoms (a rolled-up graphene sheet) as shown in Figure 2-3(a). The tubes shown are called single wall nanotubes (SWNT) because they are formed by a single surface. When multiple of these cylinders are coaxial, the composite is referred to as a multiwall nanotube (MWNT). The first observation of carbon nanotubes in the literature is of 50 nm diameter multiwall nanotubes imaged by transmission electron microscope (TEM) by a Russian group in 1952 [24]. Further observations were made during and after 1976 following a group in France which observed nanotubes with 10 nm diameter and few walls [25]. However, widespread interest in nanotubes arose only after improved resolution TEM images taken by Sumio Iijima in 1991 revealed the individual walls of multiwall nanotubes [26]. Single wall nanotubes were conclusively observed shortly thereafter in 1993 [27, 28], and the field has grown greatly since.

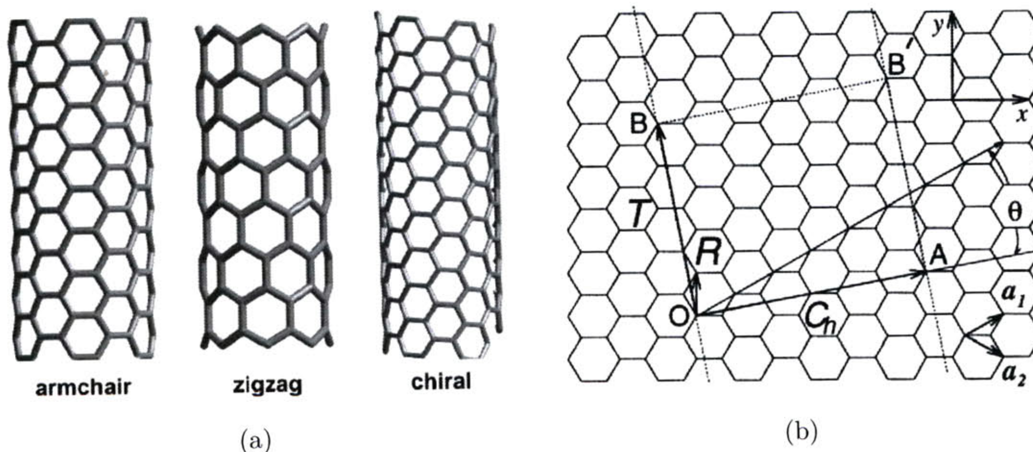


Figure 2-3: (a) Diagrams of carbon nanotubes, taken from Reference [29]. The nanotubes continue in the vertical direction, and the back of the nanotube is not shown for clarity. (b) Reproduction of Figure 3.2 of Reference [1], showing the relationship between a nanotube and a graphene sheet.

Because carbon nanotubes have the same hexagonal arrangement of carbon atoms as graphene, the band structure of a nanotube may be calculated from the band structure of graphene shown previously in Equation 2.8 and Figure 2-2(a), under the assumption that the curvature of the nanotube does not significantly affect the

electronic structure. The method by which this is accomplished is discussed in detail in Reference [30], and is outlined briefly below.

First it is noted that, for any nanotube, a circumference which passes through a carbon atom may be found. If the nanotube were cut perpendicular to this circumference through the middle of the atom and lain commensurate with a graphene sheet, the circumference would then appear as a vector, called the chiral vector C_h in Figure 2-3(b). The ends of the chiral vector must lie on atoms of the same graphene sublattice. This allows the chiral vector to be expressed in terms of the graphene primitive vectors (Equation 2.1) as

$$\vec{C_h} = n\vec{a}_1 + m\vec{a}_2 \tag{2.13}$$

where n is a positive integers and $|m| \leq n$.

The pair of integers (n, m), called the chiral index, completely specifies the structure of a nanotube. Other quantities, such as the translation vector for the unit cell of the nanotube along the nanotube axis T, the symmetry vector R, and the chiral angle θ, may be calculated directly from m and n. Of particular interest are the forms of the chiral angle θ and the nanotube diameter d:

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}m}{2n+m}\right) \tag{2.14}$$

$$d = \frac{|C_h|}{\pi} = \frac{\sqrt{3}a}{\pi}\sqrt{n^2+m^2+nm} \tag{2.15}$$

The diameter of a nanotube is typically so small (~1-3 nm) that the electrons experience quantum confinement around the circumference of the nanotube. Thus, the reciprocal space states of the nanotube are a series of parallel lines, as opposed to an area like for graphene (see Figure 2-4). If these so-called cutting lines cross the Dirac points of the nanotube, then the nanotube will be metallic. If the cutting lines do not cross the Dirac points, then the nanotube will be semiconducting. A full development of this idea is presented in Reference [1], with the result that nanotubes with $2n + m$ equal to a multiple of 3 then the nanotube is metallic. Otherwise, the

nanotube is semiconducting, with a bandgap which depends inversely on the nanotube diameter:

$$E_g = \frac{|t|a}{d} = \frac{0.431 \text{ eV} \cdot \text{nm}}{d \text{ nm}}. \tag{2.16}$$

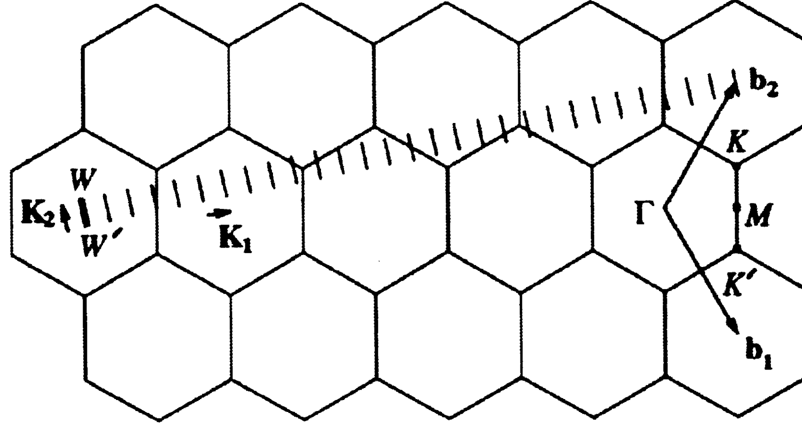


Figure 2-4: Reproduction of Figure 3.5 of Reference [1], showing the cutting lines in reciprocal space due to the quasi-one-dimensionality of nanotubes. These lines may be zone-folded to lie completely within the first Brillouin zone.

Counting all the possible chiral indices (n, m), it is found that there are twice as many indices which produce semiconducting nanotubes than there are indices which produce metallic nanotubes. It is this result which is taken as a starting point for the study of nanotube devices.

Chapter 3

Nanotube and Graphene Device Fabrication

This chapter describes the equipment and methods used to grow nanotubes and graphene, and to fabricate these raw materials into the field-effect transistors studied in subsequent chapters. A number of processing difficulties were encountered due to the nature of the carbon channel materials. Solutions, in both technique and device design, are presented which can serve as a starting point for future work with these materials.

Nanotubes and graphene can be produced by a variety of methods. Each of these methods, however, relies in some manner on the self-assembly of carbon atoms into a structure which minimizes the energy of the growth system. For the experimentalist, the trick is in finding the right system and conditions under which this self-assembly produces ordered structures instead of amorphous material. The specific methods used in this thesis are outlined below.

3.1 Nanotube Production: Thermal Chemical Vapor Deposition

Thermal chemical vapor deposition (CVD) refers to the use of heat to break apart gas phase molecules and the reassembly of these molecular components into a solid form. In the case of carbon nanotubes, both breakdown and reassembly are facilitated by catalyst nanoparticles. It has been shown in recent years that nanoparticles of nearly any composition may facilitate nanotube growth, though the traditional transition metals like iron, molybdenum, and cobalt have the largest and most reliable growth parameter windows. The most important parameters are the nanoparticle size and curvature, which are important for seeding nanotube growth. Specific combinations of substrates and catalyst precursor chemicals result in nanoparticles of appropriate size and dispersion. The specific recipes for the nanocatalyst preparation and for the growth of nanotubes used in this thesis are described below.

3.1.1 Catalyst Preparation

Several catalysts were prepared for nanotube growth. These catalysts consist of a metal compound (Fe, Mo, and/or Co) supported on an alumina nanoparticle (NP) scaffold. The catalyst is suspended in methanol, which allows it to be applied to a substrate easily and uniformly. These catalyst solutions are designated C00-C03, and have the compositions given in Table 3.1, following the nomenclature given in Table 3.2.

To prepare a catalyst solution, the solid components were measured using balance paper on a high-precision balance and these components were combined in a glass vial. Methanol was then measured and introduced into the vial using a 1 mL pipettor, after which the vial was capped and sonicated for one hour. The sonication fully disperses

C00	**C01**
15 mL Methanol 15 mg Al_2O_3 NP's 20 mg $Fe(NO_3)_3 \cdot 9H_2O$ 5 mg $MoO_2(acac)_2$	15 mL Methanol 15 mg Al_2O_3 NP's 20 mg $Fe(NO_3)_3 \cdot 9H_2O$ 1 mg $MoO_2(acac)_2$
C02	**C03**
15 mL Methanol 15 mg Al_2O_3 NP's 20 mg $Fe(NO_3)_3 \cdot 9H_2O$	15 mL Methanol 5 mg $MoO_2(acac)_2$ 15 mg $Co(NO_3)_2 \cdot 6H_2O$

Table 3.1: Catalyst recipes for nanotube growth.

Formula	**Name**
Al_2O_3	Alumina (Degussa, Aluminum Oxide C)
$Fe(NO_3)_3 \cdot 9H_2O$	Iron Nitrate Nonahydrate
$MoO_2(acac)_2$	Bis(acetylacetonato)dioxomolybdenum(VI)
$Co(NO_3)_2 \cdot 6H_2O$	Cobalt(II) Nitrate Hexahydrate

Table 3.2: Catalyst nomenclature, for use with Table 3.1.

the nanoparticles within the methanol. It was observed during initial work that the catalyst solutions would deteriorate with time, as evidenced by a color change, particularly in the solutions containing molybdenum. This color change is noticeable within 2-4 weeks of preparing the catalyst solutions, and is thought to be due to the formation of different metallo-organic complexes. Therefore, these solutions are best prepared fresh at least every week, so that consistent results can be obtained for nanotube growth.

In order to reduce the tedium of repeatedly preparing new catalyst solutions, stock solutions of each chemical component of the catalyst solutions were prepared. With only one metallo-organic chemical in each stock solution, there is less potential for ligand reorganization, and the stock solutions are stable for months. In addition, the preparation of more concentrated stock solutions reduces the error in diluted concentrations. The stock solutions are designated S00-S03, and have the compositions given in Table 3.3, following the nomenclature given in Table 3.2.

S00	**S01**
15 mL Methanol 75 mg Al_2O_3 NP's	15 mL Methanol 100 mg $Fe(NO_3)_3 \cdot 9H_2O$
S02	**S03**
15 mL Methanol 25 mg $MoO_2(acac)_2$	15 mL Methanol 75 mg $Co(NO_3)_2 \cdot 6H_2O$

Table 3.3: Stock solutions for carbon nanotube catalyst preparation.

C00	**C01**	**C02**	**C03**
1 mL S00	1 mL S00	1 mL S00	1 mL S00
1 mL S01	1 mL S01	1 mL S01	1 mL S02
1 mL S02	$\frac{1}{5}$ mL S02	3 mL Methanol	1 mL S03
2 mL Methanol	2 mL Methanol		2 mL Methanol

Table 3.4: Catalyst recipes using stock solutions. Recipes are the same as in Table 3.1 but use the prepared solutions described in Table 3.3.

Stock solution S00 is sonicated for one hour, and the other solutions are sonicated for five minutes. These stock solutions can then be combined to make each catalyst solution as needed using the ratios given in Table 3.4.

These solutions are prepared much more quickly because they can be measured using a pre-calibrated pipettor, instead of measuring powders on a scale. If the stock solutions have been allowed to settle before making the catalyst solution, the stock solutions are sonicated for five minutes before pipetting. The prepared catalyst solutions are also sonicated for 15 minutes after preparation in order to achieve a standard dispersion before catalyst deposition.

Another catalyst recipe was developed by fellow graduate student Mario Hofmann and was used primarily for growth of long aligned nanotubes. This catalyst, called Mcat (see Table 3.5), is primarily applied by the drawing method described below, and is based on the principle of using a surfactant (SDS) to stabilize an emulsion of tiny water droplets containing catalyst in an immiscible organic solvent (hexane).

	Mcat
1.	Dissolve 3 mg of Iron Chloride ($FeCL_3$) in 1 mL Water (H_2O)
2.	Add 30 mg Sodium Dodecyl Sulfate (SDS)
3.	Sonicate solution for 5 minutes
4.	Add 3 mL Hexane dropwise
5.	Stir (magnetically) for $\frac{1}{2}$ hour at 1 krpm

Table 3.5: Mcat recipe for preparation of catalyst for carbon nanotube growth.

3.1.2 Substrate Preparation

The substrates used for nanotube growth are p-doped silicon wafers covered with thermally grown silicon dioxide (typically of thickness 100 nm or 300 nm). The silicon is cleaved into chips approximately 1x1 cm^2. These chips are rinsed with acetone from a squirt bottle for 20 seconds, then immediately rinsed with isopropanol from a squirt bottle for 20 seconds, then immediately blown dry from above with nitrogen.

The silicon wafers used in nanotube experiments have a p-type (boron) doping of ~0.2 Ω·cm, though this value is not critical since the function of the silicon is as a mechanical support for nanotube devices and as an electrostatic back gate, for which the resistance at room temperature is not significant. For graphene devices, a transition was made to using very-highly-doped silicon wafers (~0.005 Ω·cm). This provides the possibility for measurement at liquid helium temperatures, since at the lower dopant densities the charges will be frozen out and the gating efficiency will be decreased as the gate electric field penetrates into the silicon to drive charge transport. All silicon wafers were purchased from Silicon Quest International (SQI).

An additional option for wafer choice is low-trapped-charge oxide. Such substrates would decrease the amount of charged impurity scattering in adjacent nanotubes or graphene (it is graphene on substrates for which this is the dominant scattering mechanism [31][32]). The existence of this option for wafers was unknown at the time of research, but will be a useful starting material for future work.

3.1.3 Catalyst Deposition

The catalyst solution is sonicated for 15 minutes before deposition in order to ensure a uniform concentration of all components, especially the alumina nanoparticles. Deposition is accomplished by a number of methods.

3.1.3.1 Dip-Coat

The prepared sample is inserted into the catalyst solution with a pair of tweezers, removed after a fixed amount of time, rinsed with methanol, and blown dry from above with nitrogen. The nanoparticles which encounter the sample surface during immersion remain on the surface through the rinsing and drying steps due to surface forces. This allows the concentration of catalyst across a surface to be increased by increasing the immersion time. The surface of the chip may also be scratched (for example, with a diamond scribe) to promote catalyst adhesion by creating surface features with are more attractive to the catalyst particles and which trap more catalyst solution by surface tension when the sample is removed from the solution.

3.1.3.2 Drop-Coat

The sample is placed on a flat surface, and a pipettor is used to place a drop of catalyst solution (typically 5 μL) onto the sample. The sample is then immediately blown dry from above with nitrogen (typically 3 seconds after drop placement). Similar to spin-coating, the blow drying causes the catalyst solution to become a thin film on the surface before drying completely. Most of the catalyst solution is pushed off the edge of the chip, but the catalyst caught in the progressing meniscus remains on the surface.

This method is especially useful for substrates covered with resist (usually PMMA) with small holes (on the order of 5x5 μm^2) opened to the substrate for patterned catalyst deposition. It was found that this method most reliably deposited catalyst uniformly across the entire chip. This is thought to be because the photoresist holes tend to trap a certain amount of solution (and therefore catalyst) in them by surface

tension as the sample is being dried, and since the catalyst solution is uniform the amount of material deposited is fairly uniform also. For patterned catalyst deposition, the following procedure is used:

1. Heat substrate on a hotplate at 150 °C for 5 minutes to remove residual sovent so the nanoparticles will adhere well to the exposed chip surface
2. Liftoff in Acetone for 150 seconds with gentle agitation, which will completely remove the PMMA mask and limit redeposition of catalyst as the liftoff releases it back into solution
3. Rinse in Acetone, then Isopropanol, for 15 seconds each, then blow dry from above with Nitrogen
4. (Optional) Anneal at 400 °C for 10 minutes in air in order to dry and activate the catalyst

3.1.3.3 Drawing

Catalyst can also be deposited manually in patterns on a chip. For this, the sharp end of a round wooden toothpick is dipped into the catalyst solution. Upon removal, the excess is removed by wiping on the rim of the vial, and the toothpick is lightly touched to the sample surface and drawn across it, producing a line of catalyst. This is used primarily with the Mcat immiscible catalyst for the growth of long aligned nanotubes.

3.1.4 Growth of Single Wall Carbon Nanotubes

Several growth recipes were used, and variations on the following recipes will be noted in the discussion of devices fabricated with methods similar to the following.

3.1.4.1 Catalyst Recipe C02

This simple catalyst (containing only iron) was used primarily for achieving a lower yield growth of single wall carbon nanotubes for electrical cutting experiments. Cat-

alysts containing other metals (cobalt, molybdenum) produced too many nanotubes, which introduced unacceptable uncertainty into measurements. After deposition of catalyst through a PMMA mask, a typical growth procedure is as follows:

1. Sample is placed in the center of the sample holder tube, the sample holder tube is inserted into the growth tube, and the growth tube is attached to the gas inlet and exhaust lines
2. Furnace is pre-heated to 800 °C
3. Growth tube is flushed with 500 sccm Ar / 500 sccm H_2 for 5 minutes
4. Growth tube is inserted into the furnace and allowed to stabilize in temperature for 5 minutes
5. Gas flow is switched to 1000 sccm CH_4 / 500 sccm H_2 for 10 minutes
6. Gas flow is switched back to 500 sccm Ar / 500 sccm H_2 and the growth tube is immediately removed from the furnace and allowed to cool suspended from tube holders
7. After cooling for 10 minutes the gas inlet and exhaust lines are removed, the gas flow terminated, and the sample removed

3.1.4.2 Catalyst Recipe Mcat

Mario Hofmann's immiscible catalyst was used primarily for growing long aligned single-wall nanotubes (or often, small bundles of single wall nanotubes). It was deposited on substrates using the drawing method described above, since the catalyst leaves a large amount of residue on the chip surface, and areas clear of residue are required for nanotube measurement and fabrication of nanotube devices. The following growth method was therefore used:

1. Sample is placed in the center of the sample holder tube, the sample holder tube is inserted into the growth tube, and the growth tube is attached to the gas inlet and exhaust lines

2. Furnace is pre-heated to 900 °C

3. Sample is flushed with 600 sccm Ar / 440 sccm H_2 for 5 minutes

4. Sample is inserted into the furnace and allowed to stabilize in temperature for 5 minutes

5. Gas flow is switched to 1000 sccm CH_4 / 440 sccm H_2 for 20 minutes

6. Gas flow is switched back to 600 sccm Ar / 440 sccm H_2 and the growth tube is immediately removed from the furnace and allowed to cool suspended from tube holders

7. After cooling for 10 minutes the gas inlet and exhaust lines are removed, the gas flow terminated, and the sample removed

3.2 Graphene Production

There are several known methods of producing graphene. The first method employed, and the one still widely used by the research community, is mechanical exfoliation [2]. The most recently developed method, and perhaps the most promising in prospects of scalability, is chemical vapor deposition [22, 33, 34]. These two methods are used in the production of graphene for device fabrication in this thesis, and will be discussed in detail below. In brief, the other three major routes to graphene synthesis are mentioned in the interest of completeness.

First, there is the annealing of SiC [17]. When a crystal of this material is annealed under the right conditions, the Si atoms will evaporate leaving behind a carbon-rich surface. The carbon atoms will self-assemble into graphene sheets, guided by lattice matching with the SiC surface.

Second, there is the graphene oxide method [19]. A chemical treatment is used to oxidize HOPG graphite. The layers are then soluble in water, and are carried off in solution. This solution may be filtered or cast onto a substrate to recover the

graphene oxide material. Treatment with reducing chemical agents recovers much of the graphene to its original form.

Third, HOPG graphite may be sonicated in the presence of a solvent with a surface energy matching that of graphene [35]. After centrifugation, a large fraction of the material remaining in solution is graphene, and can also be filtered or cast onto a surface.

3.2.1 Mechanical Exfoliation

This method is the preferred way to obtain graphene for electronic devices and other basic research purposes because it is easy to implement and presently produces the highest quality graphene sheets. The quality is determined primarily by the starting material, which is most commonly highly-oriented pyrolytic graphite (HOPG). HOPG is produced by annealing a graphitic material at high temperature (~3300 K) under compressive stress [36]. The exfoliation method is described in detail elsewhere in the literature (see, for example, [2]).

A few modifications to the exfoliation method were attempted. First, a type of natural graphite (product NBF from Nacional de Grafite LTDA, Brazil) was used instead of HOPG. It was much more difficult to prepare a piece of tape which would deposit thin graphene layers with this material than with HOPG. This is because the natural graphite was more prone to fracture. Second, the substrate used was pre-patterned with metal alignment markers. Again exfoliation was more difficult, possibly due to the altered surface chemistry of a processed substrate compared to a clean substrate. Third, a Dremel tool was used in place of tweezers to rub the tape on top of the substrate. This seemed to produce good results initially, but was later determined to be less effective than the manual method as it produced single layer graphene in smaller pieces (<~5 nm) than typically achieved manually.

The graphene devices considered in this thesis were fabricated using Scotch brand single-sided transparent or double-sided tape. The substrate used was prime grade doped (~0.2 Ω·cm) SiO_2/Si wafer with either 300 nm or 100 nm of oxide, or prime grade highly doped (< 0.005 Ω·cm) SiO_2/Si wafer with 290 nm of oxide. The sub-

strates were factory-fresh, and were rinsed with acetone and isopropanol (IPA) and then blown dry with nitrogen before deposition of graphene. Optical inspection was performed using an optical microscope in Prof. Michael Rubner's lab in room 13-4080. Optimum contrast was achieved under the 20x objective with 10x ocular. Constrast is possible because the presence of the the graphene changes the interference condition for light passing through the silicon dioxide and reflecting off the silicon (for details about optical contrast imaging of graphene, see [37, 38]).

3.2.2 Thermal Chemical Vapor Deposition

This method was developed in the NME group at MIT, specifically by Alfonso Reina, and the methods of this section refer to his work [22, 39]. Other groups have also published similar results using nickel films [33] and copper films [34]. The earlier method, and the one used to fabricate devices studied in this thesis, utilizes nickel. However, there is growing interest in the use of copper for graphene growth because it employs a surface-limited reaction instead of a bulk diffusion process as in the case of nickel.

In brief, a Ni catalyst film is used to enhance the breakdown of carbon gases beyond that possible with heat alone, and to act as a template for the self-assembly of carbon atoms into graphene. This method is scalable to arbitrary sizes, limited by the size of continuous nickel films which can be produced and possibly limited by gas flow considerations over large surfaces. It utilizes inexpensive materials (gas, catalyst, and substrate) and is carried out at atmospheric pressure and only moderately high temperatures (~1000 °C, compared to ~3000 °C necessary to produce HOPG). The graphene produced has a high area fraction of few (1-3) layers (~70-85%), much of which is thought to be turbostratic, with the remainder being thicker graphitic regions (see following sections). The material has smooth surfaces interrupted by wrinkles which are a consequence of the variable grain structure of the nickel catalyst film and differences in the thermal expansion coefficients of nickel and graphene. Typical films have an average height of ~3-7 nm. Characterization by Raman and AFM is discussed in Reference [22, 39, 40].

3.2.2.1 Growth Method

The starting substrate is a 300 nm SiO_2/Si wafer with a 500 nm nickel film deposited on the surface by plasma enhanced CVD at a substrate temperature of 400 °C. This is cleaved to size (1 cm^2 to 1 in^2) and placed in the center of a 1" quartz tube which is sealed and flushed with a mixture of 600 sccm Ar and 400 sccm H_2 for five minutes. The tube is then inserted into a preheated furnace so that the sample is at the center of the heating zone and annealed at 900 °C for 20 minutes under the same gas flow conditions, during which time the average grain size of the film will increase. After this, the temperature is raised to 1000 °C and the gas flow is changed to ~3.5 sccm CH_4 and 1380 sccm H_2. The nickel film begins to catalyze the breakdown of methane and absorbs the resulting carbon. The sample is left at these conditions for five minutes, after which the gas flow is changed to ~3.5 sccm CH_4, 700 sccm Ar, and 700 sccm H_2 and the furnace is set to cool at a predetermined rate down to the temperature of 500 °C. During the cooling phase some of the carbon which is in solution in the nickel will condense onto the surface of the nickel film to form graphene. The furnace is then set to cool to 25 °C in 20 minutes, and is removed after this time is up. This final cooling step is not important; below 500 °C there is not enough thermal energy to drive the motion of carbon atoms in the nickel or to rearrange the graphene bonds to remove defects. A schematic of this growth procedure is shown in Figure 3-1. The exact CH_4 flow rate for optimal growth will change depending on the specific nickel film (wafer to wafer variance), and the best condition must be determined by experiment.

3.2.2.2 Growth Observations

Optical inspection of the growth substrate reveals whether, and in what quantity, graphene has grown on the nickel film. An example of this is shown in Figure 3-2(a). The presence of a graphene film is indicated by a uniform scattering of dark areas (right of Figure 3-2(a)) which are identified with thick graphene layers (up to ~15 nm). Between the dark areas is few layer graphene (~1-3 layers). This few layer graphene is identifiable by the way that it decreases the contrast of grain boundaries

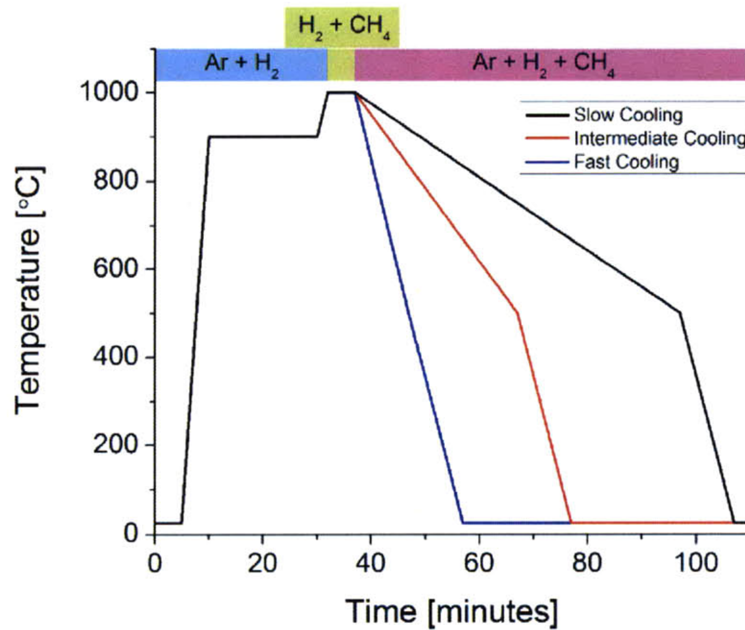
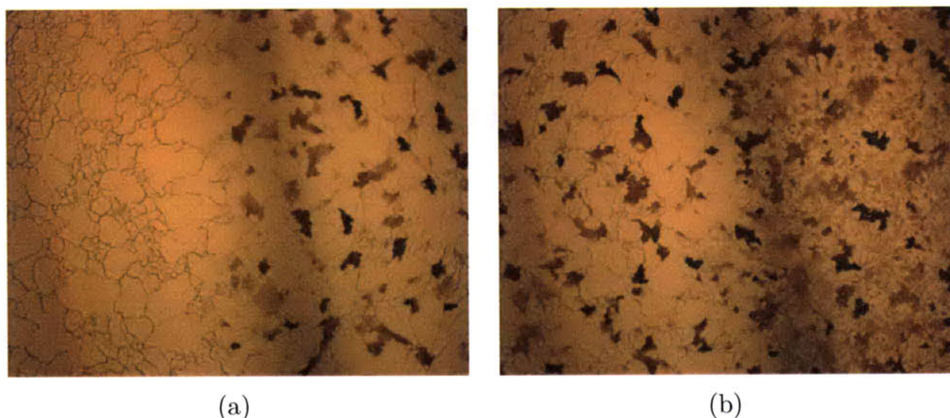


Figure 3-1: Sample temperature during graphene growth. The cooling rate can be varied to change the morphology of the graphene. The gases flowing during each time period are indicated. For specific flow rates, see the text.

(seen as grey lines), compared to that seen when there is no graphene present (left of Figure 3-2(a)). This effect is subtle but distinctive.

The images in Figure 3-2 are actually indicative of unoptimized growth conditions; for an optimized growth, the graphene film will be uniform and cover the entire nickel surface. In general, the areas without graphene are observed to form a rim around the edge of the nickel film extending ~1-3 mm toward the center of the chip, as well as to form circles up to ~3 mm in radius which are randomly positioned on the nickel film. Often, one or more point dewetting defects are observed at the center of these circles.

Additionally, a similar effect is seen where the boundary is between regions with different average graphene thicknesses (Figure 3-2(b)). The darkness of the image is proportional to the graphene thickness, so it seen that in the darker region, areas which should be few-layer areas are instead occupied by medium thickness areas. In addition, the shape of the medium thickness regions varies at a much smaller scale



(a) (b)

Figure 3-2: Graphene thickness boundaries formed by annealing with an Ar leak. (a) Boundary between no graphene (left) and normal graphene growth showing a dominance of few-layer areas (right). (b) Boundary between normal few-layer graphene film (left) and film dominated by the presence of tiny many-layer areas. The shadows at left, right, and center in the images are artifacts of the microscope, not an actual increase of material near the thickness boundary. Image sizes are 260 μm across.

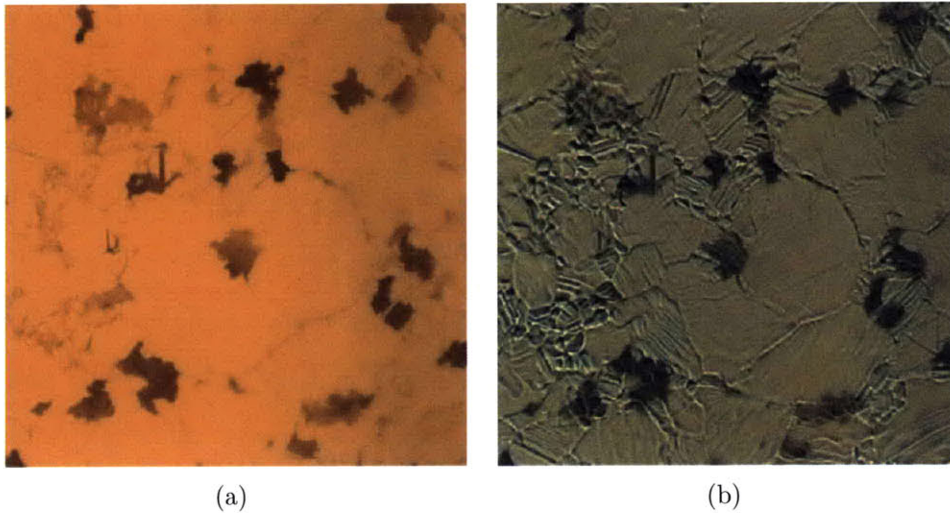
and with different shapes than for the few-layer or many-layer areas. Finally, it is notable that the density of many-layer regions does not noticeably change across the sample.

The mechanism that produces these highly ordered changes in film behavior is not known, though one likely mechanism is strain relaxation, proposed because the edges of the nickel film also behave like defects for the purposes of film dewetting. The condition that caused this behavior was a leak of Ar into the gas stream while the film was being annealed at 1000 °C. When the Ar leak was stopped by use of a solenoid valve, the graphene growth process again produced uniform graphene films. It is conclusive that contaminants in the Ar stream, or the small supply of Ar itself, cause these film boundaries to appear when they otherwise would not. It is interesting to note that a similar behaviour can be observed when the methane flow is lower than optimal. It is possible that one effect of contaminants is to reduce the partial pressure of methane, but there are likely additional effects because the similarity is not exact.

Another useful observation was that it is possible to observe the nickel surface even when it lies beneath a graphene film. This enables the correlation of the nickel grain morphology with graphene features. The method used is to constrict the illumination

aperture of the microscope so that only a nearly collimated beam of light is reflected from the nickel surface. Any angle of the surface with respect to the normal plane of the incident light will show up as a dark feature in the microscope image because the light is reflected away from the objective. By defocusing the image slightly, this effect can be enhanced. An example of this is shown in Figure 3-3. It is easily verified that thick graphene areas (darker) appear only where grain boundaries are present.

In addition, crystallographic steps can be seen on the surfaces of many grains in Figure 3-3(b), as indicated by lines of lighter contrast than the grain boundaries. These steps are arranged for the most part parallel to each other within a given grain, or as sets of parallel lines crossing at a fixed angle which is determined by the crystallographic orientation of the nickel grain. This is a feature not observed in the fully-illuminated optical image. Future studies might make use of this to quantify the grain structure of the nickel films during graphene growth optimization.



(a) (b)

Figure 3-3: CVD-grown graphene film on nickel. (a) Film under normal imaging conditions with fully-open microscope aperture A. Few-layer graphene covers the large areas of light color, while darker regions indicate thicker graphene and darker lines indicate grain boundaries. (b) Film as in (a) but with almost-closed microscope aperture A. Contrast is enhanced for the reflective nickel surface. The nickel grain boundaries are clearly seen as strong light or dark lines, while steps on the grain surface are seen as softer-contrast parallel lines. Note that the graphene film thickness is positively correlated to the density of grain boundaries. Image sizes are 90 μm.

3.2.2.3 Transfer Method

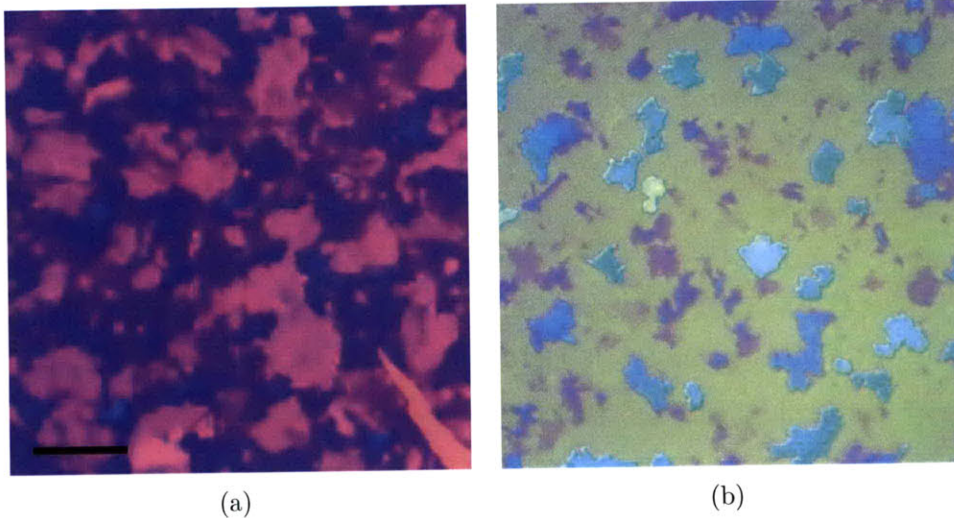
The graphene as grown on nickel film is transferred to arbitrary substrates by the following method. First, a supportive layer of PMMA is spun onto the graphene film (996k MW, 6% solution in anisole by weight). Next, a second layer is spun on top of the first (996k MW, 9% solution in anisole by weight). Two coats are used to provide a thicker PMMA film, and the lower concentration (less viscous) solution is applied first because it will more readily conform to the graphene surface. The chip is then baked in an oven at ~180 °C for 5 minutes. The chip is allowed to cool and transferred to a vial containing a 10:1 mixture of DI water and concentrated HCl (~1.13 M total). The vial is sealed and placed on a hotplate set at 90 °C for at least 1 hour, during which time the nickel film will be etched by the acid.

When the nickel is etched completely away, the chip is removed from the acid and placed in a beaker of DI water. The PMMA/graphene layer should float free of the substrate, and, if it does not, then careful use of the tweezer tip can coax it free. Care must be taken to remember which side of the PMMA film contains the graphene. The film can be carefully picked up with tweezers and laid down on a new substrate (typically a SiO_2/Si chip for device fabrication). A nitrogen gun is used to carefully blow away any residual water.

To adhere the graphene film to the new substrate, the following steps are repeated until the PMMA layer is nearly removed. First, a drop of acetone is placed on the sample, and more acetone is added as necessary to cover the PMMA film and substrate. After 20 seconds, a blow gun is used to apply a light stream of nitrogen gas perpendicular to the sample surface. The acetone should evaporate from the substrate, drawing the graphene toward the surface by capillary force, and softening the PMMA so that the film conforms to the new substrate. This gas flow is maintained for one minute, and then the process is repeated again.

The removal of PMMA is completed by immersion of the substrate into acetone for ~15 minutes. Upon removal the substrate is rinsed with acetone from a squirt bottle for 20 seconds, then rinsed with IPA from a squirt bottle for 20 seconds, then

blown dry with nitrogen. The final material appears as in Figure 3-4.



(a) (b)

Figure 3-4: Graphene on an SiO_2/Si wafer with 300 nm oxide thickness. (a) Film used for fabricating two-terminal devices studied in Chapter 5. Thicker graphene areas appear darker. Scale bar is 10 μm. (b) Film with increased coverage of few-layer regions, used for the fabrication of the devices studied in Chapter 6. Thicker graphene areas appear darker, but the thickest regions appear light (blue, white) again. Image size is 100 μm.

3.3 Fabrication Equipment and Procedures

The fabrication of electronic devices from carbon nanotubes and graphene draws strongly from conventional silicon processing and microfabrication. This section outlines the specific methods used to fabricate electronic devices considered in the remainder of this thesis, as well as the form of the devices produced and the unexpected challenges that had to be met.

The following include NMELAB systems and techniques as well as fairly standard microfabrication procedures which have been realized on specific equipment around campus. The techniques themselves have been studied extensively elsewhere, so the following sections detail the specific procedures and recipes used with this equipment.

3.3.1 Thermal Chemical Vapor Deposition

All CVD-grown nanotubes and graphene studied in this thesis were grown in the Nano Materials and Electronics Lab (MIT building 13, room 3065-A) on a custom-build CVD system. This system was the collaborative work of multiple students, and is described briefly below.

The system centers around a set of mass flow controllers. These devices are attached to an input gas line at moderate pressure (20-40 psi) and allow a fixed mass rate of gas to flow through them. The flow rate setpoint is controlled by an analog signal, and the actual flow rate is also read via analog signal. The outlets of multiple mass flow controllers may be manifolded together to a single gas line to achieve the mixtures of gases needed for nanotube and graphene growth. Such banks of manifolded mass flow controllers, along with an electronic control system which digitally produces and reads the signals for the mass flow controllers, can be seen in Figure 3-5(a) and Figure 3-5(b). As an additional control, there is a solenoid valve at the outlet of each mass flow controller, before the manifold. This prevents leaks associated with the mass flow controller from contaminating the output gases.

The gas from the mass flow controllers goes through a combination of stainless steel and low-density polyethylene lines which are attached to a quartz growth tube, as seen if Figure 3-5(c). The 1" quartz tube is chosen to fit the Lindberg model Blue M tube furnaces used for maintaining the temperature of substrate and gases during nanotube and graphene growth. The outlet gas from the tube is connected to a bubbler, which is used to verify gas flow and to maintain a pressure in the growth tube slightly higher than atmospheric pressure. The water level above the end of the outlet line is readjusted to 2 cm before every growth to maintain process consistency.

Finally, for nanotube growth, the chip is loaded into a smaller 1" long quartz tube which is placed inside the 1" growth tube. This smaller tube helps to reduce variations in growth conditions caused by convection when the growth tube is heated by the furnace (Figure 3-5(d)).

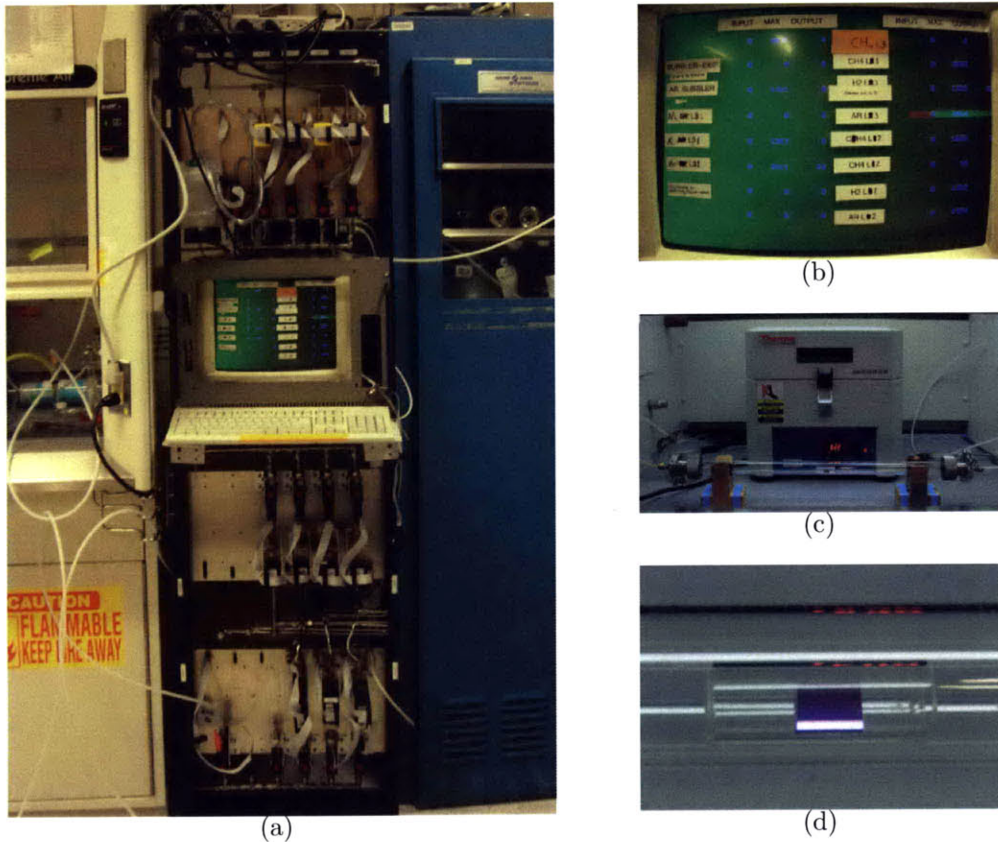


Figure 3-5: (a) Equipment rack. At center is a monitor and keyboard which are used to control gas flow rates. There are three gas lines, each composed of a bank of mass flow controllers and solenoids (arranged horizontally, one bank above the monitor and two below). Gas from supply cylinders enters the top of the rack and outlet gas exits at left toward the fume hoods where growth occurs. (b) Close-up of the screen in (a) showing the operational interface. (c) Furnace used for growth, with quartz growth tube in front. Growth gas enters from the right, flows through the tube, and exits at left through a bubbler. (d) Close-up of the tube in (c) showing a silicon chip in a tubular quartz chip holder inside of the 1" quartz growth tube.

3.3.2 E-Beam Lithography

E-beam lithography is a resist patterning technique. An electron beam (usually from an SEM column) is scanned across a surface in a pattern defined by a software file. The scanned beam exposes a resist which has been coated onto the surface. Immersion of the resist in a developing solution causes the pattern to be revealed in a manner depending on the type of resist used.

There are two common resists, both of which are used in the fabrication of devices in this thesis. First, poly(methyl methacrylate) (PMMA) is a positive resist (areas exposed to the electron beam develop away and are removed). Second, hydrogen silsesquioxane (HSQ) is a negative resist (areas not exposed to the electron beam develop away and are removed). Each of these are discussed in turn below.

There are three e-beam lithography tools available at MIT for general use. First, there is the Raith 150 system in the NSL (Room 38-181). This system is capable of very high resolution (~10 nm) and fine stage control, but is in high demand and has long load times. Second, there is the JEOL 5910 in the CMSE SEF (Room 13-1015). This machine is booked less often and has fast turnaround time, but has limited resolution (~100 nm) and requires manual stage control. For most fabrication goals in this thesis, though, the JEOL 5910 has proven adequate. Since the conduct of this thesis work started, another system has become available in the CMSE SEF; the XL-30, which uses the same lithorgraphy control system as the JEOL 5910, has fully manual stage control, and higher resolution.

3.3.2.1 PMMA E-Beam Resist

The resist used in this work is almost exclusively a 9% by weight solution of 996,000 molecular weight PMMA in an anisole solvent. As this produces a very thick resist layer, dilutions are prepared to reduce the concentration. The standard concentration for most lithography in this thesis is 6% (~640 nm when spun at 4krpm for 60 seconds), while concentrations down to 2% (~30 nm when spun at 4krpm for 60 seconds) have provided useful films. Film thickness is evaluated by AFM of a developed e-beam

lithography pattern, or if the film is unpatterned, of a scratch made in the resist layer on a dummy wafer.

When an appropriate concentration is chosen, the resist is spun as follows. First, the substrate to be coated is annealed at 175 °C for 5-15 minutes in order to remove surface adsorbates (mostly water). Then the substrate is transferred to a spin-coater. A bead of resist is deposited on the substrate using a pipette (~1 drop for a 5x5 mm^2 chip, ~3 drops for a 1x1 cm^2 chip). The chip is accelerated quickly ($\geq$ 5000 rpm/s) to the chosen spinning speed where it remains for the chosen spinning time. For process regularity, these values are almost always chosen to be 4000 rpm and 60 seconds, respectively. These values are assumed in every discussion in this thesis unless otherwise noted. After the spin-coater comes to a stop, the sample is removed and baked on a hotplate (or, more rarely, in an oven) at 175 °C for 5 minutes. Upon completion of the bake, the substrate is allowed to cool for ~2 minutes before further processing.

The choice of resist thickness is governed by application. As a mask for metal evaporation, the resist should be at least 3 times thicker than the metal layer to be deposited. Since typical metal film thicknesses are 30-100 nm, almost all devices use a 6% PMMA solution (assumed unless otherwise noted). However, for making very narrow device features, if the aspect ratio of the resist trench is too large (>~3, but dependent on the angle of evaporation) then the metal cannot reach the substrate, and thinner films must be used.

Exposure of PMMA by electron beam was performed primarily at 10 keV accelerating voltage. At this voltage, for the 6% PMMA film, metal features could be seen through the resist at low beam intensities, which allowed visual alignment to surface features. At this accelerating voltage and for the development procedure described below, a 640 nm PMMA film was found to have an optimum exposure dose of 150 $\mu C/cm^2$.

Development was always performed in a solution of 2 parts isopropanol (IPA) and 1 part methyl isobutyl ketone (MIBK). The sample is immersed in this solution for 60 seconds and immediately removed and rinsed with IPA from a squirt bottle for 20

seconds. The sample is then blown dry from above for 10 seconds with compressed nitrogen. The effectiveness of a development can be checked by AFM of the developed areas, which should appear like the original substrate (usually smooth, without bumps which are likely individual molecules of PMMA which still adhere to the surface).

Liftoff of the resist (e.g. after metal evaporation, or catalyst deposition) is accomplished by immersion in acetone for 150 seconds, followed by rinses from solvent squirt bottles of acetone for 10 seconds and IPA for 10 seconds. The sample is then blown dry from above for 10 seconds with compressed nitrogen. The bulk of the PMMA dissolves within the first ~10 seconds, but longer times are necessary to reduce surface residue and dissolve films which may have been thermally crosslinked, or which have a significant sidewall angle (cross-section for metal deposition) leading to a continuous metal film. In these cases a pipette is used to stream the solvent onto the resist. This helps alleviate mass transport limitations and provides the mechanical force necessary to break continuous metal films at their weak points (the sidewall). Note that it is also possible to remove any undesirable resist residue after liftoff by annealing the sample (see Section 3.5.3.4).

The standard process described above is for use of PMMA as a positive resist. However, PMMA can also be used as a negative resist. To achieve this, the above procedure is altered by increasing the dose by a factor of ~7 (at 10 kV SEM accelerating voltage). Instead of fracturing the PMMA chains into smaller units which are easier to dissolve, the excess dose deposits enough energy to cause the PMMA to extensively crosslink. The crosslinked PMMA is insoluble, even in strong organic solvents like acetone, and therefore acetone is used as the developer to remove the unexposed PMMA. The crosslinked PMMA can only be removed by harsh treatment such as oxygen plasma or high-temperature annealing (see Section 3.5.3.4).

One point that must be remembered is that the optimum dose for exposure will change with SEM accelerating voltage. For example, when the accelerating voltage is increased from 10 kV to 30 kV, the optimum dose increases from 150 C/cm^2 to ~300 C/cm^2. Whenever process parameters are changed, a new dose matrix should be made to find the new optimum conditions.

3.3.2.2 HSQ E-Beam Resist

The HSQ used in this work is XR1541 produced by Dow Corning (2% solution). The resist must be stored in a refrigerator to reduce the decomposition rate and should be left on the counter to warm to room temperature before use to prevent the formation of crystals in the bottle which can introduce defects into the film. The spinning procedure follows that described above for PMMA resists, except there is no post-spin bake. This produces films ~30 nm thick.

Exposure is performed as above with an optimal linear dose of 2 nC/m at 10 kV accelerating voltage on the JEOL 5910 SEM. Development is in MF-321, which is a metal-free developer containing tetramethylammonium hydroxide and surfactants in aqueous solution. The development time is 30 seconds, and the rinse is with water. The exposed HSQ is converted into SiO_2, so the exposed pattern cannot be removed except by treatments such as with CF_4 RIE or an HF wet etch.

Exposed HSQ resist has the advantage that it is strengthened by oxygen plasma etching (since it is an oxide itself) and is therefore the resist of choice in the literature for the patterning of exfoliated graphene devices, which are etched primarily by oxygen plasma. New etching recipes developed by Vitor Manfrinato (in the Berggren group) using a mixture of He and O_2 are promising in reducing the amount of defects introduced by oxygen etching.

3.3.2.3 JEOL 5910 SEM

The JEOL 5910 is the e-beam lithography workhorse for producing the devices in this thesis (Figure 3-6). It has a minimum resolution of ~100 nm and mechanical stage control to ~1 μm accuracy. The lithography aspect is controlled by a separate computer equipped with a commercial lithography-enabling system called NPGS, which was installed by Albert Wang, a former student in the Ashoori group.

There are several limitations of this lithography system which have to be considered during pattern generation and the lithography itself. The primary limitation among these is a lack of automated stage motion, beam blanking, and field stitch-

ing. Methods for efficient alignment, writing of large features, and stitching were developed and used during device fabrication. These are detailed in a standard operating procedure attached in Appendix A. Briefly, the following parameters were used: Accelerating voltage 10 kV, Aperature 2, Working distance 8-40 mm, Magnification 25-1000x, Spot Size 10-50, and Beam Current 50 pA to 4 nA.

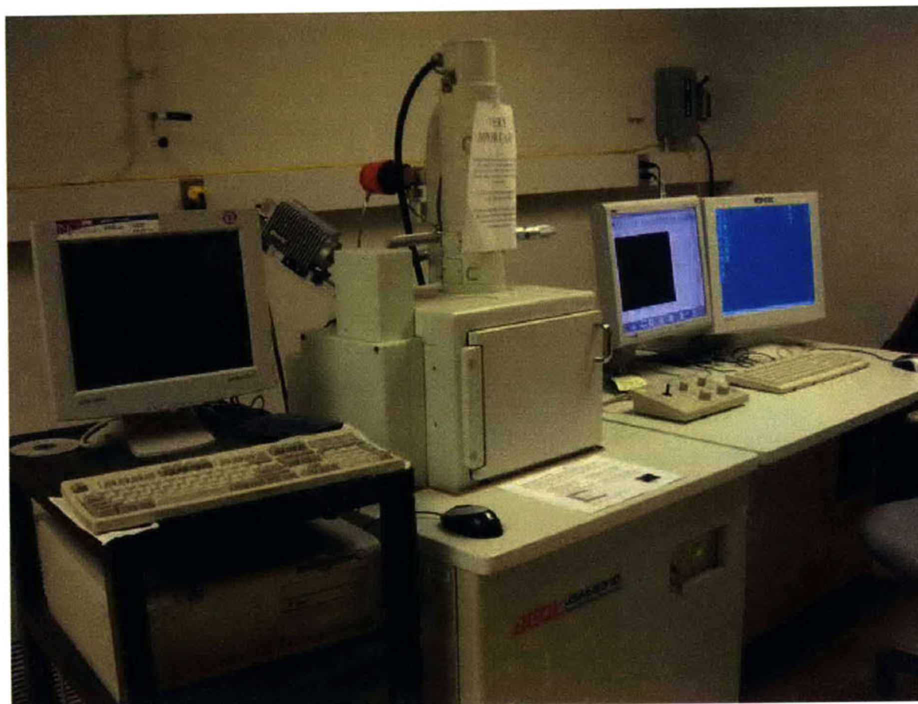


Figure 3-6: JEOL 5910 SEM with the NPGS lithography system in Room 13-1015.

3.3.3 Optical Lithography

Similar to e-beam lithography, optical lithography reproduces an image in a resist, but the exposure element is ultraviolet light instead of electrons, and the pattern is generated by a mask of opaque and transparent regions which is uniformly illuminated instead of a beam which is rastered.

Samples to undergo lithography are heated to 175 °C on a hotplate for 5 minutes before coating with resist, in order to remove adsorbates and promote adhesion of resist to the sample surface. After cooling for one minute, the sample is mounted on a spin-coater (machines used are variously in the EML, NSL, LOOE building 13

lab, and NME group lab). Resist is dispensed from a plastic syringe in an amount to cover the surface of the sample, and spun (unless otherwise noted) at 5,000 rpm for 60 seconds. The samples are then baked at a temperature described below for each resist.

Exposure takes place primarily in the LOOE building 13 yellow room on a contact UV exposure unit and in the EML on the broadband contact aligner. The EML broadband aligner has a positional accuracy of ~4 μm on the 1x1 cm^{2}chips usually used for device fabrication, limited by resist edge bead complications and microscope jitter. Alignment for the LOOE UV exposure unit is done by hand, either by estimating the sample location or by observing the mask and sample through an optical microscope as they are brought together, for which the accuracy is ~50 μm. For this exposure unit, it was also necessary to warm up the lamp before doing an exposure, in order to obtain reproducible results. This is accomplished by running the lamp for 100 units of exposure (a machine-specific dose estimation, roughly 3 minutes of exposure time) without a sample, within five minutes of performing the actual exposure. Exposure parameters are noted below for each resist.

After exposure, the samples are again baked on a hotplate, then developed in MF-321 for the times noted below. A post-development rinse by deionized water for 30 seconds is followed by blowing the chip dry with nitrogen. After metal evaporation or etching, liftoff is accomplished as for PMMA in Section 3.3.2.1. When possible, it is desirable to perform an anneal of the sample after liftoff to remove resist residue (see Section 3.5.3.4).

3.3.3.1 S1813 Positive Resist

This is used when only a standard positive resist is required.

Post-spin bake:	90 °C for 2 minutes
Exposure:	30 units on LOOE UV exposure unit, or
	30 seconds on EML broadband
Development:	90 seconds in MF-321

3.3.3.2 AZ5214-E Image Reversal Resist

This resist may be used as either a positive or negative resist. As a positive resist, it is processed exactly as above. As an image reversal resist, there are extra steps as noted below.

Positive resist mode:

Post-spin bake:	115 °C for 2 minutes
Exposure:	30 units on LOOE UV exposure unit, or 30 seconds on EML broadband
Development:	60 seconds in MF-321

Image reversal mode:

Post-spin bake:	90 °C for 45 seconds
Exposure:	5 units on LOOE UV exposure unit, or 2 seconds on EML broadband
Post-exposure bake:	115 °C for 2 minutes
Flood exposure:	30 units LOOE UV exposure unit, or 30 seconds EML broadband
Development:	2 minutes in MF-321 (1 minute in AZ-422 developer)

The post-exposure bake causes the initially-exposed area to cross-link, making it act as a negative resist. The flood exposure then makes susceptible to liftoff all areas which were not cross-linked during the post-exposure bake. The area of resist remaining is thus that which was initially exposed. The benefits to this approach are that the cross-linked resist is still soluble in acetone (useful for procedures requiring liftoff), and the sidewalls of the resist have a negative slope (the complement of the positive slope which is achieved by simple positive exposure).

The image reversal mode is very sensitive to certain parameters, namely the initial exposure dose and the post-exposure bake temperature. Optimal conditions were found for each lithography system by the methods detailed in the resist user manual.

3.3.3.3 Mask Fabrication

While chrome mask fabrication for optical lithography is a well-commercialized service, it is helpful to be able to create masks quickly in the lab. This can be done by e-beam lithography as follows.

First, a standard 5" chrome on soda lime blank was stripped of its photoresist layer and spun with PMMA (Section 3.3.2). An e-beam exposure was carried out to expose the desired pattern, and the pattern developed. A chrome etchant (CR-7 from Cyantek Corp.) was used as an etch bath, and the progress of the etch was monitored by eye to judge when the pattern cleared (typically ~2 minutes). It was discovered that the chrome etch was most reproducible when the bottle was shaken thoroughly before dispensing the etchant (assumed to be due to settling of the etchant solution; note that the expected etchant lifetime is ~1 year, and may need to be replaced thereafter if the shaking trick does not work). Afterward the mask is rinsed with water and blown dry.

As a useful note, it is possible to cut the chrome blanks with a Dremel tool if smaller masks are preferred (using a diamond studded steel abrasion wheel). The mask should be held on a soft, vibration-dampening surface (such as a stack of paper towels) to lessen the chance of premature or undirected fracture. Additionally, the cut should be made evenly across the surface (with the blade traversing the width of the mask so that the cut is of uniform depth across the mask). Cutting is best done before the mask is stripped of photoresist, so that the resist layer catches all the dust from the cutting process. In this case the resist should be removed in a flowing solvent to decrease the chance of particles settling on the surface of the blank, where they can interfere with lithography. These cleaved masks should be treated with special care because they are more likely to fracture under stress due to the propagation of tiny cracks from the cut edges created during the cutting process.

3.3.4 Metal Evaporation

Evaporation of metals is performed in three locations. First, the NanoStructures Laboratory (NSL) has an e-beam evaporator operated by Jim Daley, who has deposited Ni, Cr, Au, Pd, and SiO_2 on various devices studies in this thesis. Second, the LOOE group has an Angstrom thermal evaporator located in a Nitrogen environment in room 13-3135, used for evaporation of Cr, Au, and Al. Third, there is an NRE thermal evaporator in room 13-3024 belonging to Prof. Clifton Fonstad which was rehabilitated during the course of this thesis work and is now used for evaporations of Cr, Au, and Ni (Figure 3-7). In general, thicknesses deposited are less accurate than with the NSL or Angstrom evaporators, but for contact leads for the devices studied in this thesis, this is not such a concern, and the NRE evaporator is routinely used. Details of the evaporator troubleshooting, maintenance, and operation are maintained next to the evaporator.

Figure 3-7: Fonstad thermal evaporator in room 13-3024.

3.3.5 Oxygen Plasma

Oxygen plasma is a conventional method for cleaning chips of organic residue. It is commonly used in the literature to etch graphene and carbon nanotubes (which are organic molecules). Two oxygen plasma systems were used to prepare the chips discussed in this thesis.

First, the LOOE group has a Plasma-Preen oxygen plasma system in room 13-3031. The relatively high pressures (~1-100 Torr estimated) and high power (100-1000 Watts) can cause polymer materials to extensively crosslink before they are etched completely away (see Section 3.5.3.2). Nevertheless, this system can be used to remove graphene from a surface, which is still practical when a metal, oxide, or other hard etch mask is used. Complete etching of CVD graphene films (~15 nm in the thickest regions) can be accomplished with ~2 minutes of etching at 1000 W power and 2.5 sccm oxygen gas flow. Few layer graphene regions can be etched in ~15 seconds under these conditions.

The Plasma-Therm reactive ion etcher (RIE) in the NSL is the preferred method of graphene removal. It operates at much lower temperatures and powers and applies a DC bias to accelerate ions toward the sample. Typical CVD graphene films (15 nm maximum thickness) are removed with the following parameters.

Gas Pressure:	10 mTorr
Gas Flow:	16 sccm He, 8 sccm O_2
Purge Time:	1 minute
RF Power:	100 W (DC Bias ~200 V)
Etch Time:	4 minutes

However, soft resists are still crosslinked in the Plasma-Therm, albeit to a lesser degree. It is advisable to use a hard etch mask instead. Both Cr and Ni (~25 nm) have been used effectively, with wet acid etches used to remove the masks after oxygen plasma removal of graphene. After this procedure there is no visible damage to the graphene either optically or by AFM. It would be beneficial to also perform a Raman characterization of this process in the future.

3.3.6 Atomic Layer Deposition

Atomic layer deposition (ALD) can be used to deposit high-quality metal oxides with excellent thickness control (1 to 100's of nm). An ALD machine was constructed as a joint project with students Mario Hofmann and Kyeong-jae Lee (Figure 3-8). This machine uses chemical precursors, water and tetramethylammonium hydroxide (TMAH) to deposit Al_2O_3 layers conformally over a surface.

In brief, the machine consists of a heated chamber into which is placed the sample, and through which is flown a combination of gases. These gases are supplied by a manifold of two lines, each regulated by a three-way solenoid valve. By default, nitrogen flows through these valves at a rate specified by a mass flow controller. When each valve is switched, it allows a supply of precursor or reactant gas to flow, which is supplied from an attached bottle. The exhaust of the chamber is connected to a vacuum pump, and the pressure of the chamber is monitored by a micropirani vacuum gauge.

A deposition process involves loading the sample, and stabilizing the chamber under a flow of ~10 sccm of nitrogen from each of the two lines (20 sccm total flow rate through the chamber) and under vacuum. The resulting chamber pressure is 1 torr (the base pressure is ~15 mtorr). The chamber is heated to ~200 °C by a surrounding resistive heating element. The solenoid valves are then pulsed at regular intervals (15 ms open valve time) to supply fixed amounts of precursors which are carried along the manifold through the chamber by the nitrogen flow. Typical intervals are 30 seconds between pulses, alternating between THAH and water. The TMAH will form a monolayer on all surfaces in the system, and the water will react with this monolayer to form aluminum oxide. Typical deposition rates achieved were 1.2 nm/cycle (one cycle is one pulse each of TMAH and then water).

3.4 Device Design and Fabrication

The fabrication of all electronic devices studied in this thesis utilized the equipment and procedures outlined above. Several design principles were developed and adhered

Figure 3-8: ALD system constructed by Mario Hofmann, Kyeong-Jae Lee, and Daniel Nezich.

to, as described below. In the development of these design principles and fabrication procedures, several complications arose, some of which are addressed in more detail in Section 3.5.

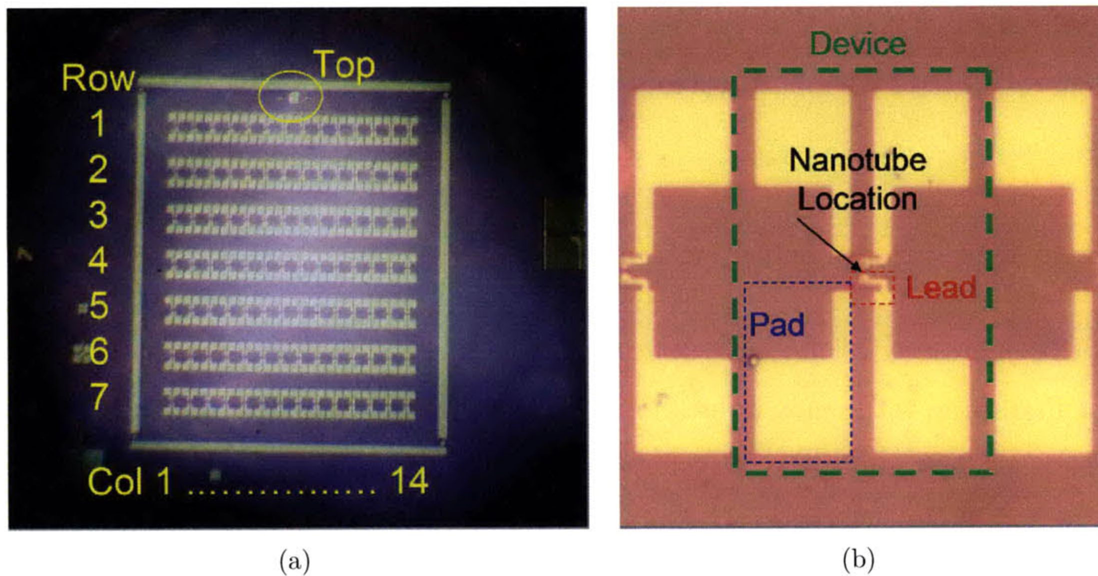
3.4.1 Nanotube Devices

Fabrication of electrical devices with carbon nanotubes has been described extensively in the literature, with many interesting techniques having been developed for making contacts, electrostatic gates, doped regions, suspended tubes, strained tubes, and so on. In this thesis, relatively simple nanotube devices are fabricated and studied. They consist of two metallic contacts on either end of a nanotube. The silicon chip on which the devices are fabricated acts as a backgate.

3.4.1.1 Substrate Description

The starting subsrate for all devices was obtained from Prof. Hongjie Dai at Stanford University (Figure 3-9). These chips are fabricated from SiO_2/Si wafers (300 nm of oxide, doped substrate ~2 $\Omega\cdot$ cm) with recessed metallization (30 nm Pt) which is nearly flush with the oxide surface. The metal Pt was chosen because, unlike gold, it will not de-wet from the surface when subjected to the high temperatures of a nanotube growth process (Section 3.1.4). The recession of the pads was chosen so that thin metal layers evaporated on top of the chip would remain continuous across the metal/oxide edge.

Each chip contains an array of device locations arranged in 7 rows and 14 columns.



(a) (b)

Figure 3-9: Optical images of fabricated nanotube device chips. (a) View of entire area of devices, with row and column labels. Distance between alignment marks which break the outer metallic rim is 3.8 mm. (b) Close-up of an individual device in (a). A device consists of four contact pads, upon two of which have been placed contact leads. The contact leads connect the contact pads to the nanotubes, which grow from a catalyst dot at the center of the image (too small to resolve). Width of the square features is 75 μm.

In this thesis, specific devices are referred to as "R-C" or "Location R-C" where R is a one-digit number specifying a device in row R from the top of the chip, and C is a two-digit number specifying a device in column C from the left of the chip. The grid on which the devices are arranged is 200 μm horizontal by 500 μm vertical. The top of the chip is defined by a set of alignment marks near the devices (Figure 3-9(a)).

Each device location consists of four metal pads (Figure 3-9(b)). The pads consist of squares 80 μm on a side, with 15 μm extensions oriented toward the center of the device location. The corners of these extensions closest to the center of the device region define an area 30 μm vertical x 18 μm horizontal.

The chips as received had also been covered with a PMMA resist layer, exposed by e-beam, and developed to open two 5 μm x 5 μm square holes per device. These holes extend to the SiO_2 substrate, and are located 8.5 μm above and below the center of the device. The purpose of the resist layer is to act as a mask for catalyst deposition.

3.4.1.2 Fabrication

Processing of these chips involved catalyst deposition and liftoff, nanotube growth, and an e-beam lithography/metal deposition/liftoff sequence to extend the metallic contact pads to the nanotube region. This second lithography step is preferred over growing nanotubes directly on the recessed metal pads for two reasons. First, the nanotube growth chemistry can be different when the catalyst is on top of metal as opposed to oxide. Second, much better electrical contact is made to nanotubes which have metal evaporated on top of them as opposed to tubes which are grown above and fall into contact with a metal surface.

Catalyst deposition is detailed in Section 3.1.3. Briefly, a drop of alumina-supported catalyst solution is placed on the substrate, left for a brief time and blown dry. After a short bake, the PMMA resist is removed and the device is ready for nanotube growth. Nanotube growth recipes are detailed in Section 3.1.4, and are carried out between 750 and 800 °C in an $Ar/H_2/CH_4$ atmosphere.

The lithography step follows the procedures described in Section 3.3.2. The pattern used varies from device to device, but there are a few common features. First,

the leads are at least 5 μm wide in order to be mechanically robust against any variances in the lithography e-beam intensity, focus, and control. Second, the leads have significant (5-10 μm) overlap with the contact pad extensions, in order to allow for lithography misalignment and to ensure a low contact resistance between the two metals. Third, the leads always overlap the catalyst dots by at least 2 μm past each side of the catalyst dot. This is done to prevent the catalyst particles from detaching from the surface and fouling an AFM tip, and to ensure that all nanotubes which grow away from the catalyst dots are contacted directly by the metal leads. Fourth, the top and bottom contact leads approach each other near the center of the device, and have a constant minimum separation. This is done to minimize the chance of having catalyst in the device channel, to minimize the distribution of tube angles with respect to vertical (minimize the solid angle that the gap between metal pads subtends with respect to the catalyst dots while staying on an axis of symmetry), and to ensure that the channel length of multiple nanotubes in the channel is as equal as possible.

Metal evaporation was performed on an Angstrom evaporator in the Laboratory of Organic Optics and Electronics (LOOE) group, or by Jim Daley in the NSL. Liftoff is detailed in Section 3.3.2. The metals used are 30 nm Pd or a bilayer of 5 nm Cr/30 nm Au. The Cr/Au sticks well to the chip surface, while Pd has a work function which better matches that of the nanotube valence band, allowing very low Schottky barrier height for p-type conduction.

The finished devices may be annealed to remove resist residue and improve (lower) the contact resistance. Residue removal behaved similarly to that for graphene detailed in Section 3.5.3.4. However, it was often found that the annealing step degraded the adhesion of the leads and pads, so that the contact metal was easily scratched away. The origin of this effect is not known, and was not observed for all annealings. A possible explanation is the presence of resist residue below the metal layer. An example of a finished device is shown in Figure 3-10.

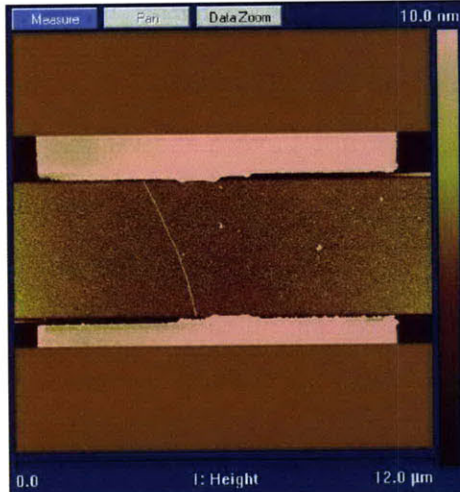


Figure 3-10: AFM image of a nanotube device channel (flattened for clarity). The contact leads are the tall features at top and bottom. A single nanotube (bright line) bridges the two contact leads. The nanotube height is about 3.5 nm, and the distance between leads is 4 μm.

3.4.2 Exfoliated Graphene Devices

Starting with individual graphene sheets which have been located on a SiO_2/Si chip (or other substrate) as described in Section 3.2.1, fabrication of a graphene FET is usually accomplished by a single lithography/metal evaporation sequence. For this, e-beam lithography is used because of its superior resolution and capability for alignment, which is important because graphene flakes are often only a few microns in size. Additionally, e-beam lithography allows facile modification of the device pattern, which is important because the size and shape of each graphene flake, as well as the arrangement of other graphene flakes and tape residue around it, are unique.

3.4.2.1 Fabrication

To begin, individual graphene flakes are located on a substrate (Figure 3-11(a)). The (x,y) position of the flake is recorded with respect to a reference location, usually chosen as the upper-right corner of the chip. Coordinates are chosen so that x increases to the left and y increased downward. This choice is made so that the coordinate system of the chip matches that of the JEOL 5910 SEM. The typical number of useful locations on a chip may range from 0 to ~12.

On a microscope with a computer-enabled stage, the (x,y) positions of each graphene flake may be read directly. However, the readily-accessible optical microscope in the Rubner lab does not have a digital readout of the stage position, though it does have the capability for digital image capture. An (x,y) position for each graphene flake is then obtained by the following procedure.

First, a series of images at low magnification (2.5x objective) is acquired so as to record the entire surface of the chip. These images are stitched together using image editing software (Photoshop) and then rotated so that the edges of the chip lie vertically and horizontally. At the microscope, individual graphene locations are found by searching the surface of the chip at medium magnification (20x objective). This magnification offers a good tradeoff between throughput, resolution, and contrast. The resolution is such that flakes detected by eye are of a sufficient size to fabricate devices, and the contrast for single layer graphene is slightly better because the objective lens has a lower numerical aperture.

When an appropriately sized (>5 μm) and isolated graphene flake is found, a series of images at different magnifications (2.5x, 5x, 20x, 50x, and 100x if available) are acquired. These are used to locate the graphene flake on the composite image previously assembled. A simple measurement of the pixel location of the graphene flake can be converted to a distance offset from the reference location. The conversion factor for the Rubner microscope with 10x eyepiece magnification is $4.024 \times 10^{-3} \cdot M_O$ [μm/pixel], where M_O is the objective magnification, as determined by pixel measurements of known chip sizes.

Once the graphene flake locations are known, PMMA resist is spun on the surface and a marker pattern is exposed by e-beam. The marker pattern used is pairs of 5 μmsquares (or right triangles) arranged in a 100 μmgrid (Figure 3-11(b)). The pairs of squares/triangles are arranged so that they meet at one corner, allowing effective judging of the location of their common vertex even if the pattern is overexposed or underexposed. The total size of the grid is 0.5 mm, which allows for plenty of uncertainty in the objective power, image distortion, pattern stitching, pixel approximation, or SEM axis calibration. Each SEM exposure location is found by identifying

the reference corner of the chip and then translating relative to this corner by (x,y) distances calculated from the composite image. Exposure is performed as described above in Section 3.3.2.

The chip is then developed for a fraction of the full development time (~5-10 seconds). This is done to expose the silicon dioxide in the marker regions, which can then be seen and used for alignment in the SEM. It is also, of course, visible under the optical microscope (Figure 3-11(b)). A new optical image is acquired, and used for device pattern generation (this technique was described by Professor Pablo Jarillo-Herrero).

Patterns are designed as described in Appendix A (also see Figure 3-11(c)). The generated patterns are written as were the markers, except that an alignment step is used so that the new pattern coincides with the markers. A full develop is then performed (Figure 3-11(d)).

Metal is then evaporated onto the chip. The target thickness is 5 nm Cr / 30 nm Au for most devices. This thickness is chosen as a compromise between the strength and conductivity of the film and the film stress which can cause delamination (see Section 3.5.2.1). Liftoff is performed as described above to complete the fabrication (Figure 3-11(e), 3-11(f)). Finally, an annealing step is often performed (400 °C, 20 minutes) to clean the device of any photoresist residue prior to electrical measurement or acquisition of AFM images or Raman spectra. This process is described in Section 3.5.3.4.

3.4.3 CVD Graphene Line Devices

Fabrication of CVD graphene devices begins with a film of CVD graphene which has been transferred to an insulating substrate (e.g. SiO_2/Si, see Section 3.2.2). Because CVD graphene can cover a much larger surface area than exfoliated graphene, there are a wider variety of fabrication techniques to explore. All of these, except the most trivial, focus on patterning the graphene, so that measurements may be made on a simple channel geometry. The two methods used to produce the devices studied in this thesis are detailed below.

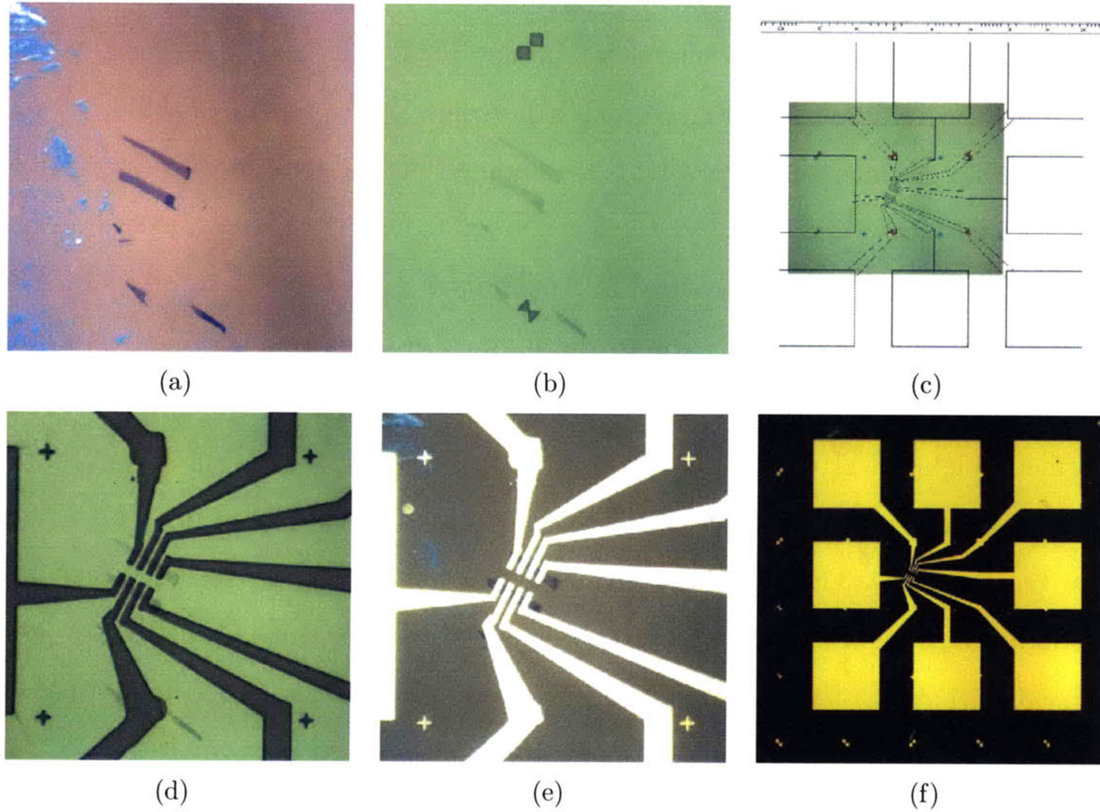


Figure 3-11: Fabrication of an exfoliated graphene device as seen through an optical microscope. (a) The location of a prospective graphene sheet is identified by optical contrast. After generation of markers at the found position, (b) another image is acquired, with the markers in view. (c) The image with markers is used to design an e-beam pattern in DesignCAD LT. The pattern is written on the chip, making use of the alignment marks to precisely place leads on the graphene. (d) The device after development, showing exposed lead areas. (e) The finished device after metal evaporation and liftoff. (f) The finished device from a far view, showing contact pads and the remainder of the marker field (small gold dots). Image size for (a), (b), (d), and (e) is 125 μm. Size of metal pads in (c) and (f) is 100 μm.

The first method considered is when graphene patterning is performed as the initial fabrication step. This has several advantages. First, it can be used to expose a large area of substrate to allow adhesion of other materials to the substrate surface instead of to the graphene (see Section 3.5.2). Second, this allows cleaning procedures (specifically annealing, see Section 3.5.3.4) to be applied without concern for metals or other materials which may react poorly to the cleaning treatment, since only graphene remains on the chip surface after the initial patterning step. Third, it avoids subjecting other device components (metal layers, etc.) to the graphene etchant (usually O_2 plasma, as in Section 3.3.5, which may enhance metal oxide formation and increase contact resistances). In this thesis, this process is used to fabricate the two-terminal line devices discussed in Chapter 5.

The second method considered is when graphene patterning is performed after the deposition of the metal contacts. The advantages of this method are that the graphene-metal contact area may be larger, there is less potential for graphene quality degradation due to the etching process, and negative resists (which often cannot be easily removed, e.g. HSQ or overexposed PMMA) may be used to pattern the graphene device channel and provide a dielectric layer for a top gate without the need for etching to expose a graphene contact area. This method is used to fabricate multiterminal edge devices.

3.4.3.1 Fabrication

Line devices were fabricated in this work using optical lithography, as opposed to e-beam lithography, which is conventionally used to process exfoliated graphene (see Section 3.4.2). This is because a goal of the research was to develop a process to produce arrays of many devices, which is too time-consuming to accomplish with e-beam lithography. Also, eventual integration of graphene into conventional silicon processing will utilize optical lithography; it is explored here for the first time to gain experience with the process and begin identifying processing issues which will need to be resolved. A brief overview of fabrication follows and is illustrated in Figure 3-12, with the details discussed below.

Beginning with a CVD graphene film on an SiO_2/Si chip, an etch mask is deposited onto the graphene. The etch mask may be the photoresist itself, or it may be a deposited layer (e.g., a metal layer deposited by thermal evaporation, as in Section 3.3.4). The graphene is then etched with oxygen plasma (see Section 3.3.5) and the etch mask removed to leave lines of graphene on the surface of the chip. The chip is then annealed to remove residue from the photolithography process (see Section 3.5.3.4). A second photolithography step is used to open rectangular holes in the photoresist through which metal is deposited directly onto the graphene lines and surrounding oxide. The metal deposited in this work is a Cr/Au bilayer, with target thicknesses of 5 nm and 30 nm, respectively (for the consequences of thicker metal layers, see Section 3.5.3.1). Liftoff, followed by an annealing step to again remove any resist residue, completes the device fabrication.

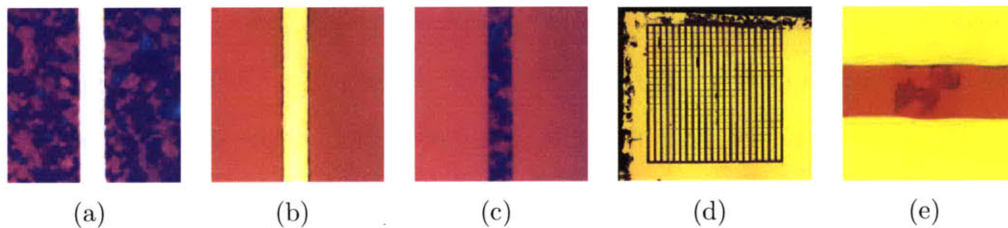


Figure 3-12: Graphene line device fabrication. (a) A metal line (Cr/Au) on top of graphene as deposited by optical lithography/metal evaporation/liftoff for use as an etch mask. (b) The same area after exposure to oxygen plasma. The exposed graphene is completely removed, showing the SiO_2 beneath (pink). (c) The same area, after removal of the metal line by a wet etch (CR-7 chromium etchant). The graphene remains adhered to the surface. (d) Finished chip. The metal peels at the edge of the chip due to a resist edge bead. (e) A finished graphene device. The yellow areas are metal pads (Cr/Au). Line width in (a)-(c) is 7.9 μm. Pattern size in (d) is 3.2 mm. Line width in (e) is 9.6 μm.

For a photoresist etch mask, resist S1813 may be used with a bright field chrome mask, or resist AZ5214E may be used in positive mode with a bright field chrome mask, or in image reversal mode with a dark field mask (for details of these procedures see Section 3.3.3). A positive process is easier to perform, but an image reversal process allows the thinner lines to be achieved due to the presence of a negatively sloped resist sidewall. Because nonuniformities in the chrome mask and lack of collimation during exposure tend to create a ribbon which varies in width on the order of

~0.5 μm, the lower limit for line width was not explored, and for most processing the S1813 resist was used. Removal of a photoresist etch mask is performed in the same manner as liftoff (Section 3.3.3), though a resist residue due to crosslinking caused by the plasma may be a concern (see Section 3.5.3.2).

For a hard etch mask, resist S1813 may be used with a dark field chrome mask, or resist AZ5214E may be used in positive mode with a dark field chrome mask, or in image reversal mode with a bright field mask. This exposes a line of graphene, onto which a metal mask is evaporated (e.g. as in Section 3.3.4). Metals used have been Ni, Cr, and a Cr/Au bilayer. Liftoff leaves just lines of metal behind on the surface (Figure 3-12(a)). After treatment with oxygen plasma (see Section 3.3.5) to remove the exposed graphene (Figure 3-12(b)), the metal etch mask is removed by a wet etch appropriate to the metal used. For Cr the standard etchant CR-7 (from Cyantek Corp.) is used, and for Ni a 1.2 M aqueous solution of HCl is used (10x dilution by volume of concentrated HCl). This leaves behind a graphene line (Figure 3-12(c)) which is used in the rest of the fabrication process described above.

The chrome masks used during lithography were fabricated by e-beam patterning as described in Section 3.3.3.3. For the lines mask, a dark-field pattern was generated, and for the pads mask a bright-field pattern was generated. This was done to allow faster writing of the mask by e-beam because the respective patterns occupied a lesser area than their inverse, and because the e-beam is scanned through the channel area directly (as opposed to creating the channel by subtraction) which creates a more reliable pattern by removing the complications of long-term beam drift and charging. To obtain the inverse type of mask from the mask produced by e-beam, an image reversal lithography step was performed using AZ5214E photoresist to transfer the pattern onto a new chrome mask (Section 3.3.3.2).

3.4.3.2 Device Design

The two important parameters for a two-terminal device are the channel (graphene) width and length (distance between edges of the graphene line and distance between contacts, respectively). The width of the lines is defined by the first lithography step,

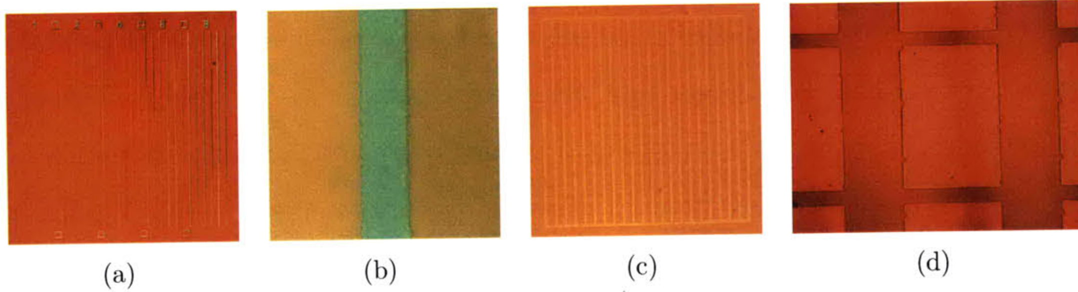
and may in principle be of any size. For this work, the width was chosen to be 1-8 μm because these values approach the minimum resolution achieved by our lithography system. This is limited by the roughness of the pattern edge of the chrome mask (Section 3.3.3.3) and the wide collimation angle of the exposure unit (Section 3.3.3). It is desirable to have the channel as narrow as possible because this increases the likelihood that a single thickness region will span the entire width of the channel, which simplifies the modeling of device properties.

The length of the graphene channel is defined by the second lithography step which produces the contact pads, and again may in principle be of any size. For this work, the length was chosen to be 3-20 μm. In practice, only gaps $\geq$3 μm were found to reliably produce devices, with the same limitations as above. It is desirable to have devices which vary both in length and width in order to sample devices with many aspect ratios. The size of the rectangular contact pads which create the gaps are chosen to be 100 μm x 150 μm, which provides ample space to position a probe pin using a micropositioner without endangering the channel regions on either side of a pad.

A benefit of optical lithography is that processing can be done after hours in the labs in Building 13. There are no alignment facilities present, so a simple solution was devised to produce devices reliably without using alignment equipment to register the two patterns used in this fabrication process. The two patterns were designed with a different pitch, so that a Moire interference pattern guarantees that ~80% of device locations always have a graphene channel. The chrome mask of lines was written with a field size of 3.5 mm. Six lines each of widths 1, 2, 4, 6, and 8 μm were written with a separation of 110 nm. The chrome mask of pads was written also with a field size of 3.5 mm. Here, the distance between adjacent columns of pads was chosen to be 150 μm. An image of the masks is shown in Figure 3-13.

3.4.4 Edge Devices

The second device design paradigm is to pattern the graphene as late as possible in the fabrication process. This usually means immediately before deposition of a top



(a) (b) (c) (d)

Figure 3-13: (a) Chrome mask for defining graphene lines. Spacing between lines is 100 μm and etched areas are light blue. (b) Close-up of (a). Line width is 8 μm. (c) Chrome mask for defining contact pads. Exposed chromium before etching is lighter yellow. (d) Close-up of (c). Pad width is 100 μm and exposed chromium before etching is darker red.

gate, and after fabrication of metal contact to the graphene. This is appropriate in situations where the graphene in small in size, otherwise contact delamination becomes a concern (see Section 3.5.2.2). This is the method almost universally employed in the literature for patterning of exfoliated graphene (Section 3.4.2).

The advantage of this procedure is that the graphene can be patterned to small dimensions and be precisely placed with respect to the materials of previous processing steps, and can therefore eliminate a lithography/metal evaporation step from the fabrication process. In this thesis, this process is used for fabricating Hall bar devices at the edge of a CVD graphene sheet.

Fabrication proceeds as for exfoliated graphene in Section 3.4.2 with three modifications. First, of course, the starting material is a CVD graphene film which has been deposited on a portion of the surface of a SiO_2/Si chip (see Section 3.2.2.1 for details). Second, the location of the contact pads must be chosen to not overlap the graphene film. This means that the area of graphene on the boundary of the film should be chosen for device fabrication, so the distance that leads travel over the graphene is minimized. Third, the design of the e-beam lithography device patterns is different.

A standard design was chosen for the contact pad and device lead sections of the pattern, as seen in Figure 3-14. Six contact pads enable multiple Hall and Van der Pauw measurements to be made in each device region. Metal leads travel between

the two columns of contact pads so that all leads emerge on one side of the collection of contact pads. This is done so that all contact pads are accessible on the edge near the device, and the pads are oriented vertically so that a maximum number of devices may be fabricated next to each other along a given edge of a CVD graphene sheet. The wires that extend each contact pad are protected in the center of the pad region, since it is common for probe pins to approach the pads from outside the device region. The leads that contact the graphene device region are designed to extend beyond the graphene and onto the oxide in as short a distance as possible to minimize the possibility of delamination (Section 3.5.2.1). A standard device region bounded by the contact leads was chosen to be 6 μm x 8 μm. The pad and lead patterns are stitched together by hand with polygons of a shape appropriate for the lead and pad pattern placement and orientation. This may require avoidance of surface features such as alignment marks or regions of CVD graphene.

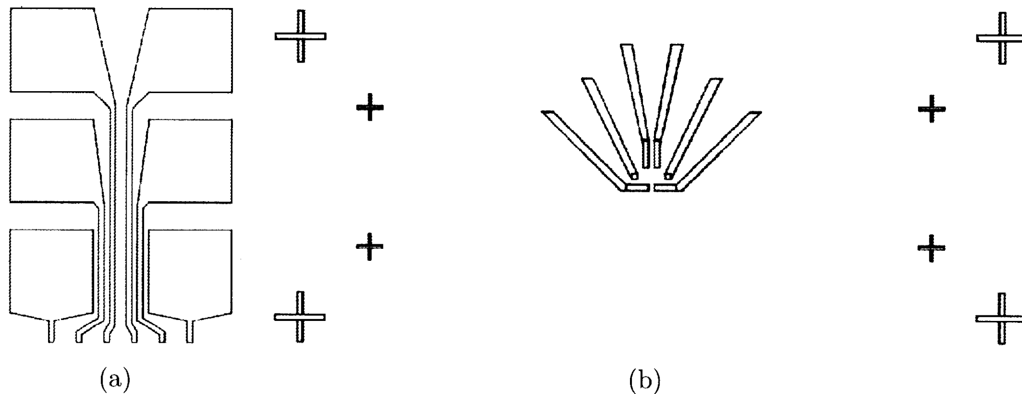
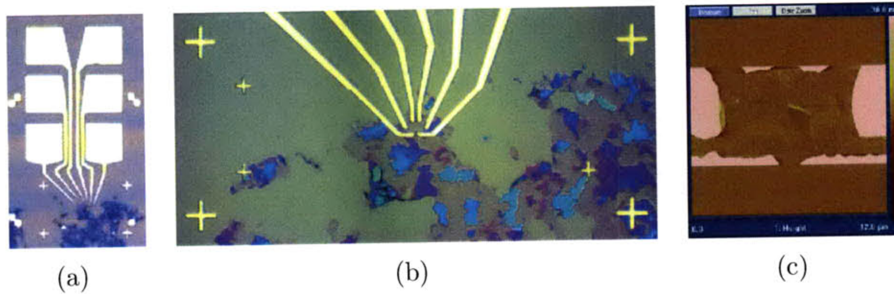


Figure 3-14: (a) Hall edge device contact pad pattern. Length of each square is 150 μm. (b) Hall edge device channel lead pattern. The device region is surrounded by the six contact leads. The graphene is expected to lie in the lower half of this pattern. Crosses are alignment marks centered on the device region. The device region is 6 μm x 10 μm.

After the metal contact and pads are fabricated, the device looks similar to Figure 3-15(a). A 5 minute anneal (Section 3.5.3.4) is performed to clean the surface, and AFM images are acquired of the device region, an example of which is shown in Figure 3-15(b). Using this image as a guideline, the shape of the Hall bar channel is designed. Care must be taken to design around holes, wrinkles, or other features in

or on the graphene sheet. An e-beam patterning of this channel design is performed using HSQ resist (Section 3.3.2.2). After development, a silicon dioxide etch mask remains. An oxygen plasma etch (Section 3.3.5) removes all graphene on the surface of the wafer, except for that beneath the oxide etch mask and metal contacts.



(a) (b) (c)

Figure 3-15: (a) Finished Hall bar device, with pads clearly visible. (b) A close-up of the device region of (b) showing the leads and alignment marks. (c) AFM of the cleaned graphene surface of a device before covering with the HSQ etch mask. A hole in the graphene is visible as a darker region near center.

The device is now ready to test. Usually, the oxide etch mask is not removed. If removal is desired, a quick HF etch (Section 3.3.2.2) is sufficient, though consideration must be given to the effects of undercutting (Section 3.5.1.1). More commonly, the oxide mask is used as a gate dielectric for top-gating of the graphene channel. To deposit a top-gate, a standard e-beam lithography/metal evaporation/liftoff sequence is performed using the alignment marks centered on the device region (see Figure 3-15(b), Section 3.3.2.1, and Section 3.3.4). For the device area design of Figure 3-15(b), it may be necessary to either use a very narrow gate lead, to cover sections of the existing lead pattern with exposed HSQ during the etch mask lithography, so that the leads in contact with the graphene do not become shorted to the gate, or to leave one lead unattached to the graphene in order to be contacted by the gate metal.

3.5 Fabrication Challenges for Graphene

3.5.1 Graphene Enhancement of Wet Etch Rates

When a material which is to be removed by a wet etch is in contact with graphene, lateral etching of this material proceeds much faster than expected. Estimates for this rate increase are up to 100 times for HF etch (Bolotin, unpublished) and approximately 70 times for chromium etch from experimental data presented below. This large increase in rate must be taken into account when designing a device fabrication process.

3.5.1.1 Hydrofluoric Acid Etching

One very relevant wet etch is the use of hydrofluoric acid to remove silicon dioxide. Silicon dioxide is the standard graphene device substrate, but is also used as an etch mask for graphene (in the form of hydrogen silsesquioxane (HSQ), an e-beam resist) because it is unaffected by the oxygen plasma etch used to remove graphene. It has been observed that any silicon dioxide that is in contact with the graphene will begin to etch almost immediately, as if being in contact with graphene were equivalent to being in contact with the etchant solution. This has been used to great effect in the suspension of HOPG graphene flakes [11], but it complicates fabrication with CVD graphene because the CVD graphene covers such a large portion of the substrate.

To illustrate this, a chip of graphene line devices was prepared as described in Section 3.4.3.1 in the text above. The chip was then etched in a buffered HF solution for 2 minutes and dried in a critical point dryer (ethanol to carbon dioxide solvent exchange) in the NSL. AFM of the resulting devices gives the following measurements: the thickness of the metal pads as 54 nm, the 2 minutes of HF etch removed 189 nm of silicon dioxide substrate, and the CVD graphene reaches up to 14 nm in height above the surrounding silicon dioxide. From AFM images and optical images of the devices, we observe two immediate consequences of the unique properties of a wet etch in the presence of graphene, which are discussed below.

First, any graphene not mechanically anchored to the substrate is liable to detach

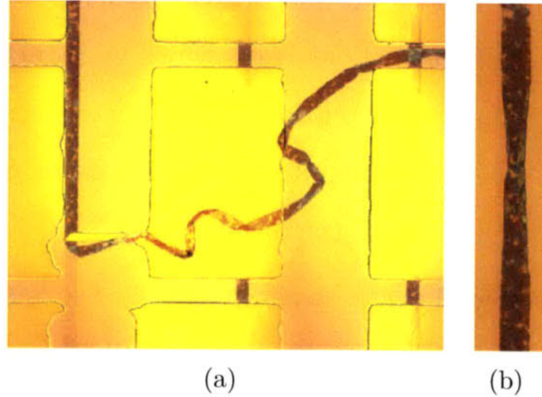
from the substrate and float away into the etchant solution or exchange solvent after the silicon dioxide substrate immediately beneath it is etched away. An example of this is shown in Figure 3-16.

The graphene line originally in a vertical orientation at left detached during the etch or solvent exchange and later fell to the surface again in a haphazard manner, crossing over metal pads, oxide, and another graphene ribbon (top right). The ribbon delaminated up to the point that it was mechanically anchored to the substrate by a finger of Cr/Au. This shows that the fluid forces which might act to pull the graphene away from the surface (as one would pull on one end of a piece of tape to detach it from a table) are both not strong enough to rip the graphene and not strong enough to tear or detach the metal layer from the oxide.

A light purple shadow is seen where the graphene used to lie. The shadow appears because the oxide below the graphene line (presumably before it detached during the turbulent critical point drying step) did not etch as quickly as the rest of the oxide which was exposed directly to the etchant. The thickness difference is only 5.2 nm above the surrounding oxide, so that the etching rate is decreased in the presence of graphene only by an average of 2.8%. For graphene protected by metal, the thickness difference may be as high as 17 nm which corresponds to an etch rate decrease of 9%. These differing rates may be due to the early detachment of the graphene line (after which the etch would continue at the normal pace, implying that the graphene line detached about 40 seconds into the etch) or to the additional restrictions of solvent motion under the metal (solvent may only enter under the graphene, which is restricted by the line width under the metal but may enter anywhere along the length of an exposed line). The graphene itself is assumed to be impermeable to liquid and gas [41, 42]. This assumption has yet to be verified for CVD graphene which may have stacking faults and a significant defect density, but is certainly valid at least on small single-crystal graphene domains.

Not only may graphene lines delaminate dramatically as in Figure 3-16(a), but they may also delaminate subtly as in Figure 3-16(b). The lines shown there has lifted and redeposited slightly to the right, so that casual inspection would not suggest

delamination. However, the narrowing of the ribbon and the presence of regions of higher reflection (thicker graphene) along the edges indicates that the edges of this ribbon have folded over on themselves. This is only possible with complete delamination of the folding region. Additionally, the original location of the graphene line is again visible as a light purple shadow, indicating that the delamination here also occurred after etching.

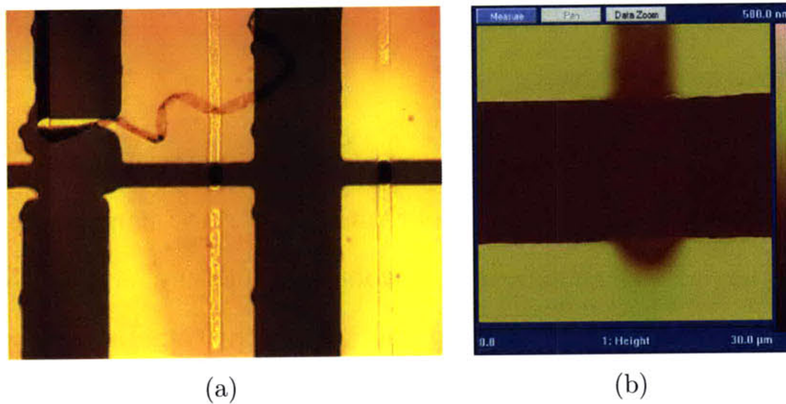


(a) (b)

Figure 3-16: Graphene line devices after HF etch. (a) This is a composite image taken at two illumination intensities so that the graphene line may be tracked across both the oxide and the highly reflective metal pads. The bright yellow rectangles are Cr/Au contact pads (100 μm wide), the peach background is the SiO_2 substrate, and the mottled purple/pink ribbons are CVD graphene lines (~9.5 μm wide). Note that where the CVD graphene overlaps, it appears blue due to the increased thickness. The light purple shadow that appears where the graphene ribbon used to lie (in the bottom left corner) is an area of silicon dioxide which is thicker than the surrounding oxide. (b) 50x image of graphene line that has shifted from its original position (indicated by the light purple shadow) and having edges which have folded over (blue edges along narrow region of the line).

The second observation is that etching can cause the mechanical support of graphene to be compromised. An example is shown in Figure 3-17. When the oxide under the graphene is removed and the aspect ratio of graphene width or length to etch depth is large (in this case, 8 μm / 189 nm = ~42), collapse of the graphene region and its metal support is likely to occur. This collapse may be initiated by surface tension, vibrations, or turbulent flow in the solvent rinse. The collapse indicates that the interaction of graphene with the silicon oxide surface is stronger than the graphene/solution and solution/oxide interactions.

Collapse may be complete or partial, in that some regions of the device may remain suspended while others are collapsed. In Figure 3-17(a), the collapsed regions can be identified optically by using a closed aperture to accentuate the contrast of curved metal surfaces (this is the same process which allowed detailed imaging of nickel grains in Section 3.2.2.2). In Figure 3-17(b) an AFM height image clearly shows that the high-contrast regions in Figure 3-17(a) correspond to a fully-collapsed structure, and that the absence of high-contrast regions indicates a non-collapsed structure.



(a) (b)

Figure 3-17: (a) Optical image of the region in Figure 3-16 with optical microscope aperture A in the closed position, which enhances the contrast of metal edges. The position of the vertical graphene line (dark on the underlying oxide) where it lies under the Cr/Au pads (yellow) is clearly marked by high-contrast lines (dark borders with brighter yellow interior). Note that some regions do not show this contrast (immediately below center device, above right device). (b) AFM height image of the center device in (a). The yellow areas at top and bottom are the Cr/Au contact pads, and the graphene line is seen vertically as a slightly lighter shade of red in the center. The graphene channel and parts of the metal pads have collapsed where the silicon dioxide was etched away underneath the graphene (top contact and edge of bottom contact). The bottom contact is partially suspended, as indicated by the uniform height at the bottom of the image.

The presence of suspended regions between collapsed regions is somewhat surprising. It might be possible to estimate the adhesion force of graphene to the etched oxide surface necessary to maintain this balance, or to achieve the observed contact angle of the gold pads at the edges of the collapsed regions. However, because collapse may have occurred due to surface tension as the sample was moved between etch, rinse, and solvent liquids, more careful experiments will be required for a conclusive calculation.

The message from this is that care must be taken when etching the substrate on which graphene is deposited. If not in contact with another material which is impervious to the etch (such as Cr/Au contact pads), the graphene will be liable to lift off the substrate. Though the graphene maintains a light contact with the surface during the etch, as evidenced by the slightly decreased etching rate immediately below the graphene which shows a height profile exactly matching the shape of the graphene, it may be dislodged by normal processing and handling.

3.5.1.2 Chromium Etching

The ability of graphene to promote quick wet etching of materials it is in contact with makes practical a new and interesting fabrication route for nanofluidic devices. In addition, this ability also suggests that transport of fluids in channels with graphitic walls may be different from transport in channels with walls made of conventional materials such as oxide or polymer. Specifically, the zero-velocity condition imposed at channel walls for fluid flow modeling may not hold when the walls are graphitic. The following is a first step toward investigating these phenomena and characterizing graphene-derived nanochannels.

We begin with an example of a fabrication step that is compromised by the wet etch rate increase of chromium, a common adhesion layer used when depositing metal. Chromium is also useful as a hard etch mask for graphene (see Section 3.4.3.1). Suppose that we wish to use chromium for both these purposes.

Consider a stripe of graphene on an oxide surface upon which lies a chromium etch mask (which was used to define the stripe). A gold contact pad with a chromium adhesion layer is then deposited on the graphene-chromium line and the device is put in a chrome etch solution. One would naively expect the exposed chromium to etch away normally, while the chromium sandwiched between the gold and graphene can only etch laterally (e.g., the 25 nm thick layer of chromium not covered by the gold would etch in ~1 minute, while in that time the chromium covered by gold would etch the same 25 nm laterally underneath the gold. This undercut is insignificant compared to the size of a typical contact pad of ~100 μm and so is not a concern for

this process).

What actually happens is that any chromium in contact with the graphene will etch away, including that which is underneath the gold contact pad layer. This can lead to a collapse of the gold contact onto the graphene, which should result in poor electrical contact compared the original evaporated Cr/Au stack. It also makes the underetched gold more liable to be torn or scraped away, since it no longer has an adhesion layer. In this respect the results are similar to the HF etch discussed in the previous section, where materials that should conventionally remain in place are instead lifted off in the presence of graphene. An example of the beneficial use of this behavior is as a novel way to fabricate nanochannels.

Nanochannel devices are fabricated following the flowchart in Figure 3-18. The starting material is a Si wafer with 300 nm of thermal oxide on top, onto which CVD graphene has been transferred. Photolithography is used to expose lines of graphene, and a layer of chromium ~25 nm thick is evaporated. After liftoff, lines of chromium remain on the graphene, and these are used as a hard etch mask. The etch used to remove graphene is performed in the NSL Plasmatherm reactive ion etcher. The recipe used is 8 sccm O_2 and 16 sccm He with a total pressure of 10 mTorr for 4 minutes at RF power 100 W and DC bias 200 V. After this, graphene remains only underneath the chrome etch mask. Such a long etch time was used to ensure that even thick graphene regions are fully removed. Then a layer of 100 nm SiO_2 is evaporated onto the chip, completely covering the graphene/chromium lines. The final step is a chromium etch, which leaves an empty channel where the chromium used to be.

This fabrication technique is interesting because of the control it allows in the choice of channel dimensions. For the channels considered in this thesis, the width as defined by the optical lithography step is ~10-20 μm. This could easily be increased or decreased, even so far as replacing optical lithography with e-beam lithography to create channels down to 10 nm across. The height of the channels is exactly the thickness of the evaporated chromium layer, and could conceivably be pushed thinner to the few-nm range. Unlike methods of nanochannel fabrication that involve the bonding of two surfaces (one patterned with indentations and one flat), the channel

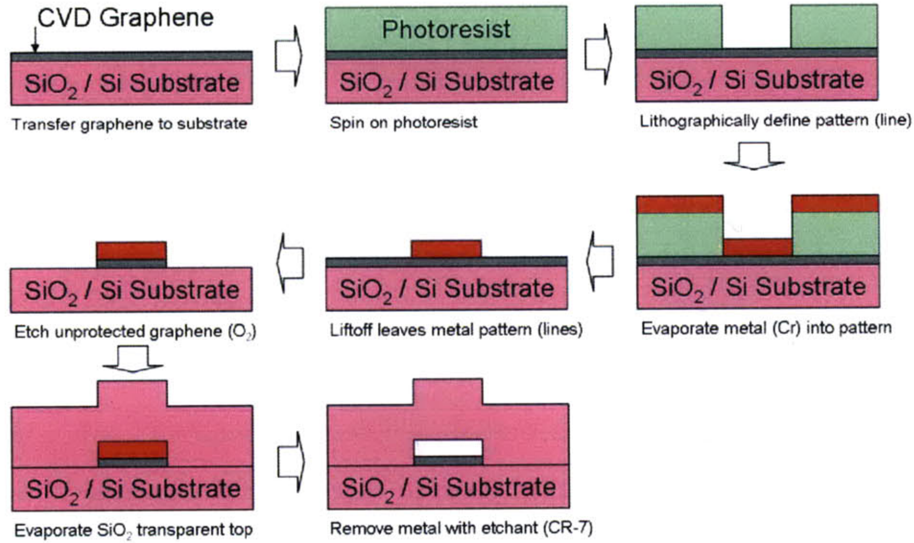


Figure 3-18: Fabrication flowchart for graphene-assisted nanochannel fabrication. Images depict the cross-section of the device.

height of graphene-derived nanochannels is as uniform as the height of the evaporated metal layer.

In addition there are no issues with wafer-scale bend as there might be with a bonding process, and one could conceivably fabricate matching top and bottom gates without the need for two substrate alignment. The top of the channel (evaporated SiO_2) may be made of arbitrary thickness, and very thin membranes might be useful for fabrication of sensor electronics on top of the channel device, as this would allow efficient electric field penetration into the channel. It would also be possible to fabricate electrodes as the channel wall, if direct electrical contact to the fluid is needed. The graphene itself may be used as a transparent electrode. Thin, flexible membranes may be used as the top wall of the channel to make a surface with strain which can be varied hydrostatically, or thick top layers may be deposited after the initial evaporation to achieve a stiff channel top which is not as liable to collapse. Channel supports, fluid mixing barriers, or elaborate channel geometry may be designed in during the lithography step. And of course, a variety of different materials can be used with this fabrication outline, including different metals or insulators for the hard mask and hard or soft materials for the channel top.

A chip of graphene line devices was prepared as described above, and cleaved in half to expose the cross-section of graphene lines and allow the etchant to enter the channel. The chip was secured using double-sided tape to the bottom of a glass dish which was secured to the stage of an optical microscope. Using a 100x objective with long focal length, the sample was brought into focus and immersed in a chromium etch solution (CR-7 from Cyantek Corp., composed of 9% ceric ammonium nitrate and 6% perchloric acid in aqueous solution). Video of the progress of the etch was recorded using a webcam mounted on the microscope eyepiece. Two behaviors are observed and will be discussed in turn: etching of chromium over graphene, and etching of chromium without graphene.

Etching of chromium on top of graphene proceeds very quickly, so images were taken as the chip was immersed in the etchant (Figure 3-19). The images shown are taken two seconds apart, and the width of the line is 10.7 μm. The blurriness is due to the meniscus of the chrome etch being at an angle with respect to the microscope's optical axis. There are several observations to be made.

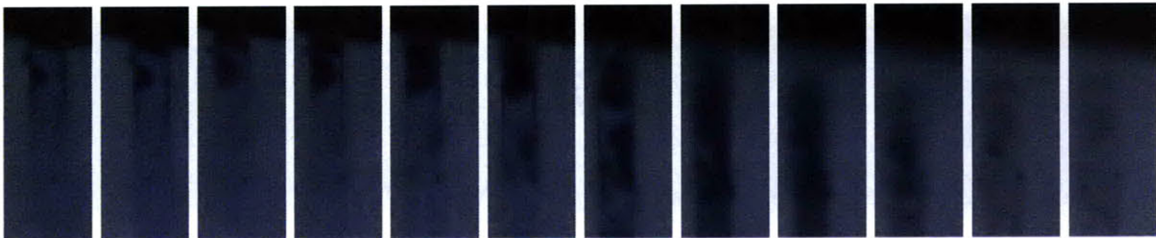


Figure 3-19: Time-series of an etch of a chromium nanochannel with graphene. Interval between frames is 2 seconds (initial figure at left), and the width of the channel is 10.7 μm. The chromium (bluish pink) becomes partially etched (dark grey) before being removed completely (darker pink). The etching rate accelerates as more chromium is etched.

The chromium appears as a smooth bluish line in the first images, and when etched transitions first to a dark grey color before being removed completely to expose the graphene underneath, which appears beige. By comparison with the etching of chromium lines without graphene (discussed below) it is concluded that the etching of chromium occurs as the etchant infiltrates the interface between chromium and graphene, since the intimate contact of the chromium and silicon dioxide top layer

does not allow etchant penetration. In the intermediate images it is clear that the graphene is etching not only from the cleaved end (seen at the top of each image); but also from multiple points on the edges of the line, as evidenced by the dark grey areas which are not contiguous with the edge of the chip but which always nucleate at the edge of the line. This is likely due to pinholes in the top layer of oxide, caused by points of chromium metal sidewall which were not removed completely during the metal liftoff step.

The partially-etched areas (dark grey) are consistent with the partial etching of chromium films seen during the fabrication of photolithography masks in Section 3.3.3.3. The partially-etched areas grow in size and cover the whole channel before the etching is completed. This occurs with 22 seconds of the beginning of the etch. The speed at which the areas of partial etching grow is measured by tracking the motion of the edge of the dark regions in Figure 3-19, and is found to accelerate from ~0.6 μm/s at the beginning of the etch to ~1.9 μm/s at the end of the etch. Similar acceleration is observed and discussed in more detail in the section about the etching of chromium lines without graphene.

The completion of the chromium etching is indicated by a transition from dark grey to light color in the channel. This transition is more gradual than the darkening described above, as expected for a chemical etch. Rough estimation of the speed of the transition front gives an etch rate of ~2 μm/s which is similar to the initial etch edge rate. Completion of the etch happens within 7 seconds of the channel turning completely dark grey, for a total etch time for the chromium channel with graphene of ~29 seconds.

Etching of chromium without graphene, in contrast, proceeds very slowly. Figure 3-19 shows images spaced 1 minute apart, where the width of the line is 19.3 μm. The chromium here is the lighter pink region in the center of the images, while the silicon dioxide is seen at either side. Unlike the chromium lines with graphene, the side of the channel cannot be easily distinguished because there is no material remaining after the etch (graphene) to significantly alter the interference conditions with the substrate.

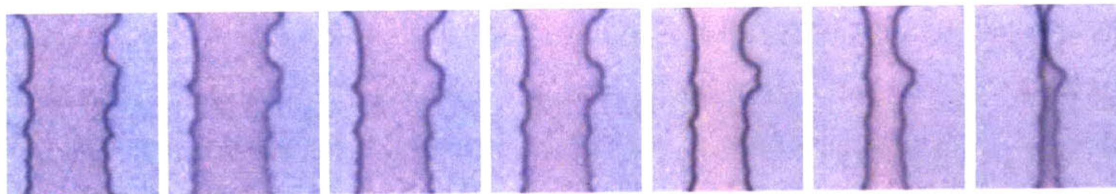


Figure 3-20: Time-series of an etch of a chromium nanochannel without graphene. Interval between frames is 1 minute, and the width of the channel is 19.3 μm. The chromium (lighter pink at center of images) becomes fully etched (darker pink/purple) as chromium etchant enters through small pores in the top oxide layer at the edges of the film (this causes the uneven and circular edges). Complete etching of the chromium takes 11 minutes, and the movement of the etching front accelerates, from ~9.5 nm/s at the beginning of the etch to ~26 nm/s at the end of the etch.

The first marked difference from the etching of chromium lines with graphene is the absence of the dark grey areas which indicate partial etching of chromium. This is because the chromium adheres well to the SiO_2 both above and below it, so that etching can only occur laterally. The equivalent of the dark grey regions for the etch of chromium lines with graphene is the edge between chromium and the channel, which may contribute to the good contrast of that boundary in the optical images.

The edges of the chromium lines also show arcs that indicate that etching begins at pinholes on the edges of the line. This behavior is similar to that of the chromium lines with graphene, confirming that this is a result of an unoptimized fabrication process which leaves rough metal edges at the boundaries of the lines. However, it is clear that the etch proceeds isotropically, because once the entire edge of the channel is open to the etchant, any roughness in the line wall is gradually reduced as the etch proceeds.

The etch rate is more easily calculated for this slower etch and is found to accelerate as the etch proceeds, just as for the chromium lines with graphene. To calculate the etch rate, a series of 63 optical images taken at intervals of 6 seconds were analyzed (an example image is Figure 3-21(a)). A horizontal cross-section was chosen, and for each image the positions of the edges of the chromium line were detected by using a threshold fitting function to find the center of each dip in intensity. Missing points indicate a failed fit and are ignored during subsequent analysis. These posi-

tions are plotted in Figure 3-21(b). The general upward trend is due to meniscus drift as etchant solution evaporates, which causes the image to shift position according to Snell's Law. The distance between these two intensity dips is the width of the unetched chromium line and is plotted as black dots in Figure 3-21(c). Small excursions of the width data from their average are due to adjustment of the camera focus to correct for meniscus drift.

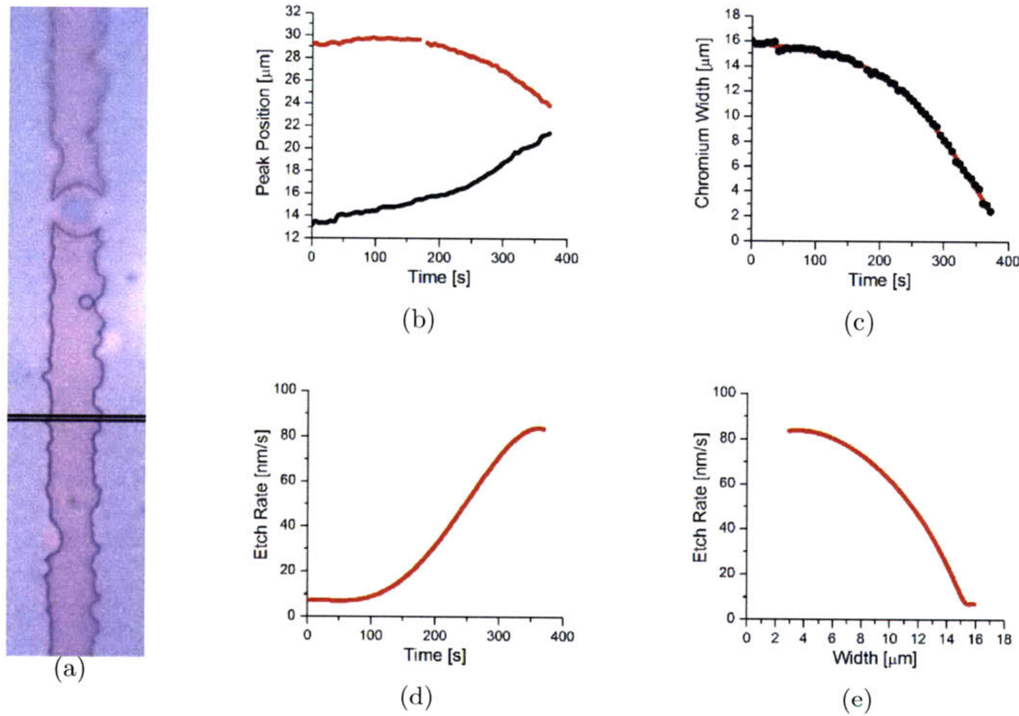


Figure 3-21: (a) Optical image of a partially etched Cr line without graphene (width 19.7 μm). The horizontal line indicates the image slice used for etch rate analysis. (b) Position of intensity dips in the optical image indicating the edge of the chromium line as a function of time for 63 consecutive images taken at intervals of 6 seconds. (c) Width of the unetched chromium, calculated as the difference between the values in (b) (black dots). A polynomial fit of order 5 is used to smooth the data (red line). (d) Etch rate as calculated by differentiating the polynomial fit in (c). (e) Etch rate as a function of the width of chromium.

The etch rate can be calculated as the difference of consecutive widths plotted in Figure 3-21(c), but this accentuates the noise in the data and is not very informative. Instead, a fitted polynomial is used to smooth the width data. A polynomial of order 5 was found to be the minimum order to adequately fit the data. The resulting

polynomial is shown as a red line behind the data. The etch rate calculated from this derivative is shown in Figure 3-21(d) and shows interesting behavior.

The etch rate is initially constant, with an average value of 3.68 nm/s = 220 nm/min on each side (the rate in the figure is twice this because the chromium is etched from both sides). After about 100 seconds of monitoring (~6 minutes total since immersion in the etchant solution), the etch rate transitions to be linearly increasing with time with a slope (from four cross-sectional analyses) of 0.214 nm/s^2 = 770 nm/min^2. This increase of etch rate with time is interesting because it indicates that etching is not limited by diffusion of etchant molecules to the chromium. If this had been the case, the rate would have decreased with time, since the molecules would have further to diffuse after entering the channel from the pinholes in the sides. However, it is notable that the initial constant etching rate is what is expected for a lateral chromium etch limited by chemical reactions at the chromium surface (~170 nm/min from [43], which is an excellent source for expected etch rates of common microfabrication materials).

To understand the etch rate increase, it is instructional to plot the etch rate as a function of the channel width (Figure 3-21(e)). The constant etch rate appears only for widths above ~15 μm, below which it increases drastically. This crossover point corresponds approximately to the width at which the chromium becomes completely separated from the wall of the channel due to the merging of etched regions along the channel edge generated by pinholes in the oxide.

It is hypothesized that the increase in etch rate seen below a width of ~15 μm is caused by an upward osmotic pressure in the channel. This pressure is generated by the higher concentration of etch reactants in the channel and causes the oxide to be deflected upward. The upward force on the oxide helps to delaminate the oxide/chromium layer from the graphene at a small length scale, which allows attack by the chromium etchant and an observed increase in the etch rate. An exact model for this behavior is left for future work, but supporting observations are noted below. (It is also possible that the etch rate increase is due to the increase in diffusion which can occur with increased channel height due to the upward bending of the thin top of

the channel due to osmotic pressure. This possibility should be considered in future modeling.)

First, the formation of so-called etch bubbles was observed. Figure 3-22 shows etch bubble formation in a series of images from the same line as in Figure 3-21, spaced 6 seconds apart, while the chromium width was still >15 μm. These bubbles form primarily during the initial portion of the etch, and are either localized near the edge of the chromium or extend across the entire width of the channel (see Figure 3-22 for an example of the latter). The bubbles form initially as a dark grey region of partially etched chromium, and completely etch within ~30 seconds, which is exactly the behavior observed during the etching of chromium with graphene discussed above. The boundaries of these bubbles are always circular. Upon complete etching of the bubble, the etching proceeds at the usual rate.

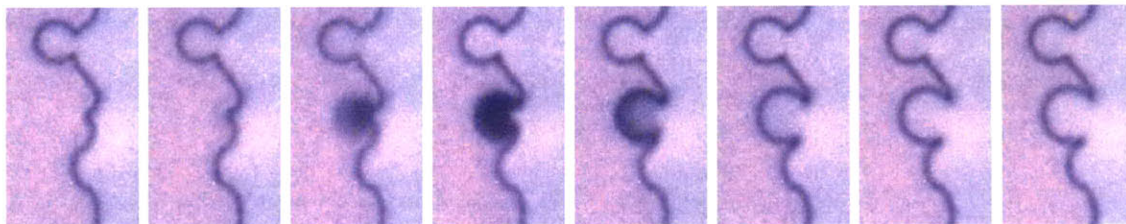


Figure 3-22: Time-series of an etch bubble. Interval between frames is 6 seconds, and the width of the bubble is 5.6 μm. The chromium (darker pink) becomes partially etched (dark grey) before being removed completely (lighter pink).

These etch bubbles are thought to be formed when the oxide layer delaminates from the chromium, allowing etchant solution to permeate the gap and begin etching the chromium nearly simultaneously across the entire area. This 'bubble' formed between the chromium and oxide delaminate is the origin of the name 'etch bubble'. The force that drives the delamination is not known, but might be osmotic pressure resulting from the increased concentration of reaction products in the channel or is perhaps due to simple liquid-solid surface energy considerations. In any case, the circular area of these etch bubbles suggests that there is a uniform pressure delaminating the oxide from the chromium. If the contact angle of the oxide with the chromium changes with bubble size and the adhesion energy of the oxide to chromium is spatially uniform, then the circular shape of the bubbles can be explained. This

model is left for future work.

Second, interference fringes are observed after the release of the oxide, as seen in Figure 3-23. A completely etched bubble spanning the width of a chromium line is seen at center. Pink and blue interference rings are seen concentric with the bubble. As the etch proceeds, the interference rings become less pronounced and more elongated. The elongation occurs because the bubble is constrained perpendicular to the line by the sides of the channel, but may extend along the line as the etch progresses. When the chromium is completely etched, the bubble is cylindrical. The decrease in intensity may be due to a decrease in pressure as the etch progresses or a relaxation of strain induced in the oxide by the initial pressure during bubble formation. The latter is more likely in the case of osmotic pressure, which is expected to be proportional to the etch rate. The osmotic pressure and will be highest when the bubble is etched, then it will drop sharply and increase again proportional to the etch rate shown in Figure 3-21(e).

The formation of bubbles and their corresponding interference fringes thus suggest that there is a pressure which tries to delaminate chromium from its attached layers, and that when delamination does occur, then etching proceeds quickly. The similarity of this behavior with that observed for the etching of chromium over graphene strongly suggests that chromium much more readily delaminates from graphene than it delaminates from oxide. This is not surprising in light of the weak interlayer bonding in graphite. Because the mechanical separation of graphene and chromium, readily driven by a hydrostatic pressure inherent to a wet etch, explains all observations made with these nanochannel devices, it remains an open question whether graphene has any purely chemical effect on etching.

There are several improvements to be made to the graphene nanochannel technique to address issues and questions raised in this study.

First, the presence of pinholes effectively limited the channel length to 10 μm for the purposes of studying the etch rate. To achieve closed channels, three techniques may be used. 1) A bilayer resist or other technique may be used to prevent sidewall formation during metal evaporation. This should remove the cause of the pinholes

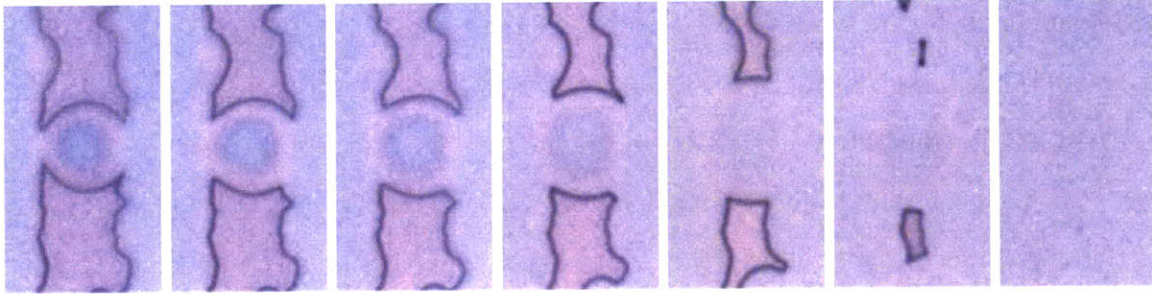


Figure 3-23: Time-series of the interference pattern generated after a bubble etch. Interval between frames is 1 minute, and the initial width of the line is 19.3 μm. The chromium (darker pink) is etched away (lighter pink). The circular bubble at center, after complete etching of chromium, shows concentric rings of interference indicating that the oxide layer is bowed outward. Over time, the shape of the bubble changes, and the interference becomes less pronounced as more area becomes delaminated from the chromium. Between the final two frames, barely visible, the bubble shape changes to an even higher aspect ratio to occupy the area recently held down by the thin line of chromium at the top in the second-to-last frame.

and should be employed in all fabrication. 2) A sealing layer can be deposited on top of the top oxide layer. Examples of appropriate sealing layers are ALD oxide and polymers such as PMMA or PDMS. ALD oxide is chosen because it conformally coats the surface, including any overhanging metal. PMMA and PDMS are suggested because they are clear, repellent of aqueous solutions, and thick, so as to provide some mechanical support for the channel wall. 3) The etchant solution can be constrained not to cover the top of the chip. This may be accomplished by rotating the microscope and chip by 90° so that the lines extend vertically out of the etchant solution, or by using a barrier to hold back the etchant from the inner region of the chip (such as a bead of PMMA around the edge of the chip).

Second, the width dependence of the etching rate (assumed to be due to bowing of the top oxide layer) obscures any channel height constraint of the etching rate (such as for 2D versus 3D diffusion of reactant and reaction product). For this reason it is desirable to have a rigid channel top, for which three methods are proposed. 1) A thicker layer of oxide may be evaporated. 2) A supportive polymer layer (such as PMMA or PDMS, as mentioned above) may be deposited on top of the evaporated oxide. 3) A thin polymer layer may be used as an adhesive to attach a glass coverslide.

This can maintain the optical accessibility of the nanochannel, which may degrade for thick evaporated layers or be inhomogeneous for thick polymer layers.

Third, the optical accessibility of the device may be improved by backside observation when the nanochannels are fabricated on a glass (or other transparent) substrate, instead of on a SiO_2/Si wafer. This would work especially well with the latter two methods described in the previous suggestion.

Fourth, the investigation of the effect of lining a nanochannel with graphene is not complete when using a channel with only one wall covered with graphene, as studied above. To remedy this, a second layer of graphene for the top of the channel may be deposited as follows. After the oxygen plasma step, another layer of CVD graphene may be transferred. A thin layer (~1-3 nm) of silicon dioxide is evaporated before spinning with HSQ and using e-beam lithography to expose the line pattern again directly on top of the previous lines. After development, the sample is again etched in oxygen plasma. The HSQ (now converted to silicon dioxide) protects the graphene, and what remains is a wafer/graphene/chromium/graphene/silicon dioxide stack. A final oxide layer is then evaporated as before to seal the channel. The chromium layer may then be etched as discussed previously, and the channel used in nanofluidics experiments.

This new nanochannel fabrication technique, enabled by the availability of large-area few-layer graphene and demonstrated for the first time in this thesis, provides interesting opportunities for the study of reaction kinetics and nano/micro scale fluid transport.

3.5.2 Weak Adhesion of Graphene to the Substrate

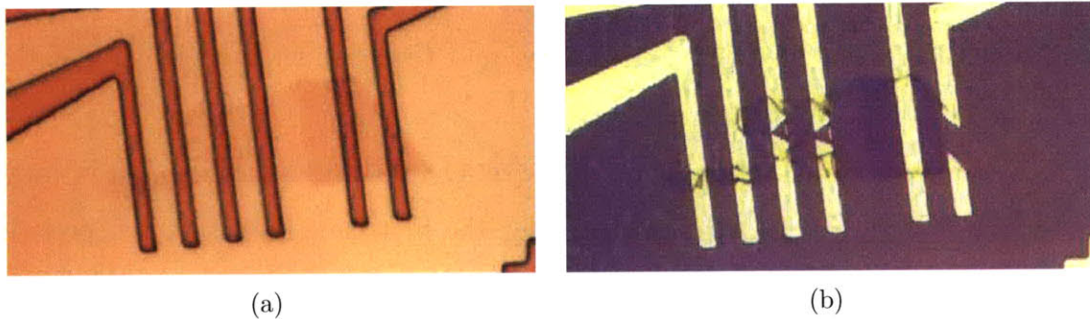
Graphite is a natural lubricant because the bonding between graphene layers is relatively weak, as evidenced by the large difference in bond lengths within the graphene plane (1.42 Å) and between graphene planes (3.35 Å). This weak interlayer bonding allows graphene layers to slide past each other with relatively little energy cost. It also means that the noncovalent bonding of graphite to other materials is often weak. This can be either detrimental or beneficial in the fabrication of graphene devices.

The possibility of weak surface adhesion as an aid to chemical etching was discussed above in Section 3.5.1, while the detrimental mechanical aspects are discussed below.

3.5.2.1 Delamination under Thin Film Stress

Evaporation of a thin metal film on top of graphene is a common procedure during graphene device fabrication. However, it has been observed that if the evaporated metal is too thick, film stress can cause the film to peel up from the surface. This usually removes the graphene from the substrate immediately below the metal, and destroys the device. The crossover thickness between adhesion and delamination for a Cr/Au film over graphene is estimated to be ~50-80 nm.

An example of this delamination by film stress is shown in Figure 3-24. Here, a 95 nm thick Cr/Au film was deposited on top of a large single-layer/bi-layer flake of HOPG graphene which had been deposited by mechanical exfoliation. Upon liftoff, the metal which was deposited on top of the graphene was visibly deformed and in some places completely removed along with the graphene beneath it.



(a) (b)

Figure 3-24: Peeling of thick metal pads over graphene. (a) Developed PMMA pattern used as a metal evaporation mask over a flake of single layer (left, lighter) and double layer (right, darker) graphene. (b) The same area as in (a) after evaporation of 94±5 nm of Cr/Au and liftoff. Stress in this thick metal film causes peeling over the graphene because of the low surface energy of graphene on the silicon oxide surface. Image width is 86 μm.

Note that metal in direct contact with the silicon oxide does not peel because the adhesion energy for Cr/SiO_2 (>250 meV/Å^2 [44]) is significantly larger than that for graphene/SiO_2 (0.4 meV/Å^2 [45]). Also, the Cr/graphene bond is stronger than the SiO_2/graphene bond, so that the graphene peels away with the metal (see rightmost

contact in Figure 3-24(b)).

The resolution of this issue has been to evaporate thinner layers of metal, so as to produce a film with less stress. After this problem was identified, the standard thickness for evaporations was chosen to be 5 nm Cr / 30 nm Au, which alleviated most delamination problems. The crossover thickness between delamination and adhesion of the metal film over graphene is ~50-80 nm, and is estimated by using only a few data points. Note that this crossover thickness will vary depending on the metal deposition parameters (which affect the film stress). Other evaporated metals should also show a different crossover point, depending on their relative adhesion energies to SiO_2 and graphene and on their tendency to exhibit film stress under given deposition conditions. The choice of substrate material, also, may affect the crossover thickness, inasmuch as different substrates may have a different adhesion energy for graphene.

3.5.2.2 Metal Delamination under Controlled Mechanical Force

The low adhesion energy of graphene to silicon dioxide mentioned in the previous section is also evidenced by delamination of the graphene film under an applied mechanical force. The specific force considered here is that applied by a probe pin on an electrical probe station. These probe pins are steel needles attached at the end of a plastic cantilever which is anchored to an xyz micropositioner. The micropositioner is operated manually, and contact of the probe pins with the surface is judged by observing the change in focus and deflection of the probe pin under an optical stereo microscope. The consequences of using this probe to make contact to metal pads deposited on top of graphene are shown in Figure 3-25.

Even the smallest force manually applied by an electrical probe pin (estimated to be ~0.01 N over a contact area of 10-100 μm^2) was sufficient to cause damage to thin Cr/Au pads, as seen in Figure 3-25(a)-3-25(b). The metal is easily scraped along the surface, as evidenced by the wrinkles in the film along the edges of the damaged area. The graphene is also removed from the damaged area, exposing the SiO_2 underneath. This indicates that the adhesion energy of chromium to graphene is greater than that of graphene to SiO_2.

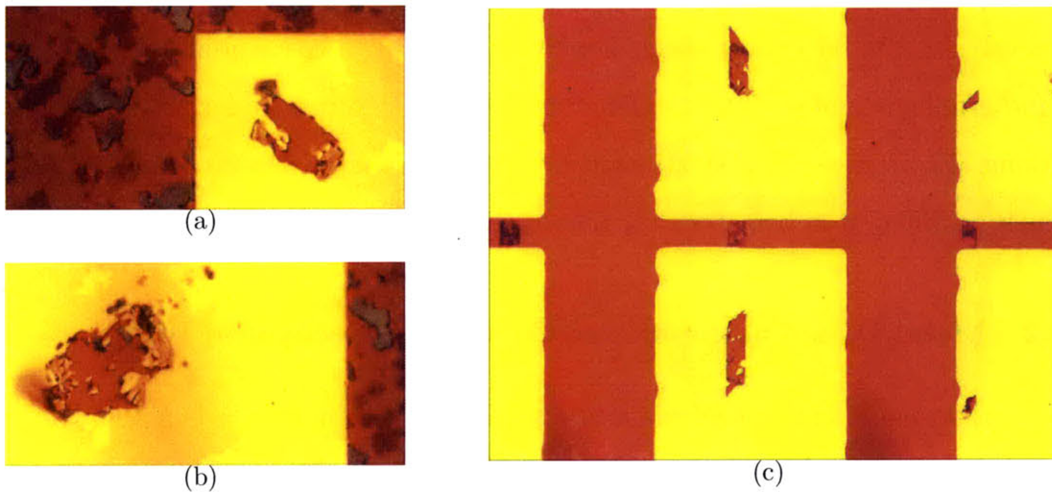


Figure 3-25: Damage sustained by metal contact pads on top of graphene during electrical probing. (a) Thin Cr/Au metal contact pad on top of CVD graphene, after light contact with a probe pin. The metal is clearly broken and wrinkled at the edges of the hole resulting from being shoved across the surface. Graphene is not seen within the hole in the metal, indicating that it adhered to the metal as the metal was scraped away. Image width is 130 μm. (b) Same as in (a) but in a different location. (c) Graphene line devices showing probe pin damage. The graphene line extends under the metal pads. It is only the metal which covers graphene which is removed by scraping with the probe pin. Width of the metal pads is 100 μm.

This behavior is markedly different from that of a metal film deposited directly on top of SiO_2. In Figure 3-25(c), a graphene line device is shown after having been probed. In this image, the location of the graphene line under the metal contact pad is clearly seen by the shape of the area damaged by the probe pins. The direction of pin travel is also seen from the angled edges of the scratched area, traveling on the upper pad from upper left to lower right, and traveling on the lower pad from lower left to upper right. The metal film to either side of the damaged area is not affected, though it experienced the same mechanical forces from the probe pin.

The conclusion to be drawn from this is that the design of devices with large areas of graphene must take into account the poor adhesion of graphene to substrate. Any areas which will experience lateral force should be placed away from the graphene. When graphene completely covers the substrate, as is the case for transferred CVD graphene films, the substrate must be revealed by the removal of graphene in order to obtain areas where upper layers can be anchored. Even when anchored, though, any upper films which cover the graphene must be thick enough to resist applied forces on their own, without relying on force transfer to the substrate.

3.5.2.3 Graphene Delamination under Controlled Mechanical Force

The graphene film itself can also be removed by direct scraping with a probe pin. This again is due to the low adhesion of graphene to silicon dioxide. It is typically accomplished by applying a large downward force with the probe pin, and while this pressure is applied, scraping the probe pin across the surface by moving either the pin or the sample stage in the xy plane. This technique is easy to apply and has several immediate uses.

First, it has proven useful for device isolation. During fabrication of graphene line devices, the graphene lines may often be offset with respect to the metal pads. This offset is often large enough so that the lines come into contact with the metal surrounding the device region, which is shorted to the doped silicon substrate when the evaporation extends to the side of the chip. Less common is when the graphene lines themselves extend over the edge of the chip to make contact with the doped

silicon substrate. In either case, this shorts the devices to the gate, which precludes electrical measurements.

To remedy this, the graphene can be scraped away so as to break the undesired electrical contact. Depending on the quality of the graphene, the substrate, the sharpness of the probe pin, and the applied force, this may require multiple passes in order to completely break the graphene film. Film breakage can be judged optically by use of the probe station microscope. Removal of the graphene film restores the appearance of the underlying silicon substrate, and electrical measurements show that the graphene devices are isolated.

Second, mechanical scraping is a fast and easy way to prepare sub-millimeter scale electronic devices with graphene. An example of this is shown in Figure 3-26, which shows a Van der Pauw cloverleaf pattern. A graphene sheet on a silicon dioxide surface was scrateched with four lines so that the sheet remained intact only in a small area in the center of the sheet, about 100 μm in size. The large quadrants of graphene are contacted at their outside corners using silver paint. This enables four-point measurements on a limited device area, which is useful if the graphene sample is inhomogeneous.

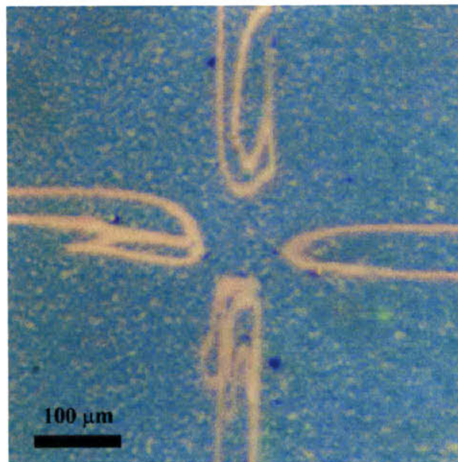


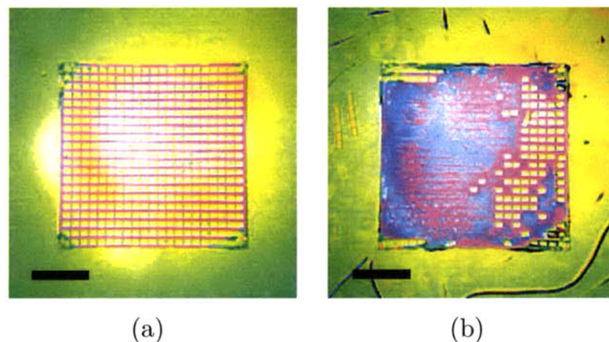
Figure 3-26: Four-terminal device fabricated by mechanical scraping. The blue-purple area is CVD graphene, and the pink lines are the underlying SiO_2 exposed by scraping with a metal pin operated by a micrometer. The four corners can be connected to measurement equipment by careful application of silver paint. The central bridge area is approximately 90 x 90 μm^2, and is suitable for four-terminal Van der Pauw measurements.

3.5.3 Lithography

Lithography is such a standard processing technique that it is often taken for granted, and recipes for resist application, exposure, and development are followed blindly. However, there were a number of unanticipated issues with both optical and e-beam lithography which had to be resolved in order to properly fabricate graphene devices.

3.5.3.1 Poor Photoresist Adhesion

If a photoresist layer is not well adhered to the wafer surface, then during the development step the developing solution can penetrate between the photoresist and the substrate. This causes the photoresist to bow upward and to crack (Figure 3-27(b)). The cracked photoresist is subject to fluid forces, which in a turbulent liquid can cause the photoresist film to be torn completely off the surface.



(a) (b)

Figure 3-27: (a) Properly developed photoresist. The photoresist appears yellow and green, while the underlying SiO_2appears pink. (b) Cracked and delaminated photoresist caused by poor substrate adhesion to a surface treated with acid. Scale bars are 100 μm.

Poor photoresist adhesion occurred frequently during the fabrication of graphene line devices while using a Cr/Au metal layer as an etch mask for defining lines of graphene. After a chip was subjected to oxygen plasma to etch the exposed graphene, the chip was immersed in CR-7 chromium etchant to release the metal lines. After a thorough rinse in DI water, the chip was blown dry and baked at 115 °C for 5 minutes before the lithography process. Lithography then resulted in delamination. The suspect step is the CR-7 etch, with possible activation by oxygen plasma. There

was one device processed with a Ni etch mask which used HCl as an etchant and showed a small amount of delamination. This supports the suspicion of the acid treatment step as the cause of the poor photoresist adhesion.

The solution employed to prevent resist cracking and delamination was to perform a standard cleaning anneal (600 sccm Ar / 400 sccm H_2 at 400 °C for 20 minutes). The assumption is that this passivates the chip surface which had been functionalized during the acid treatment. The exact chemistry of this process is not known, and no other annealing parameters have been attempted, though these would be useful investigations to support future fabrication.

3.5.3.2 Photoresist Crosslinking by Plasma

During the fabrication of graphene line devices, an etch is performed to remove graphene from the silicon dioxide surface of a chip, in order to allow the anchoring of contact pads and to define a narrow conducting channel for the graphene device (Section 3.4.3.1). Initially, photoresist was chosen as the etch mask because it was easily patterned and removed. However, in practice, it was found that exposure to plasma crosslinked the photoresist so that it formed a viscous, sticky film that could not be removed by a solvent bath.

Three example of crosslinked photoresist are shown in Figure 3-28. In Figure 3-28(a), photoresist lines on a bare SiO_2/Si chip were etched in the LOOE plasma-preen system at ~1 Torr pressure and 1000 W power under only oxygen flow. After etching, the chip was rinsed in acetone for 2 minutes and blown dry. Normally, acetone should dissolve away the photoresist, but what is observed is a thick, gooey substance which is identified as crosslinked photoresist. The bulk of the substance may detach from the substrate in certain regions, but even then it leaves behind significant residue (light blue). A scratch is seen at the bottom of the image which removes the light blue residue and fractures the bulk substance, but this is not a useful technique for device fabrication.

The resist residue was thought to be caused by the high thermal load delivered to the photoresist by a high-pressure plasma, so etching was carried out using the

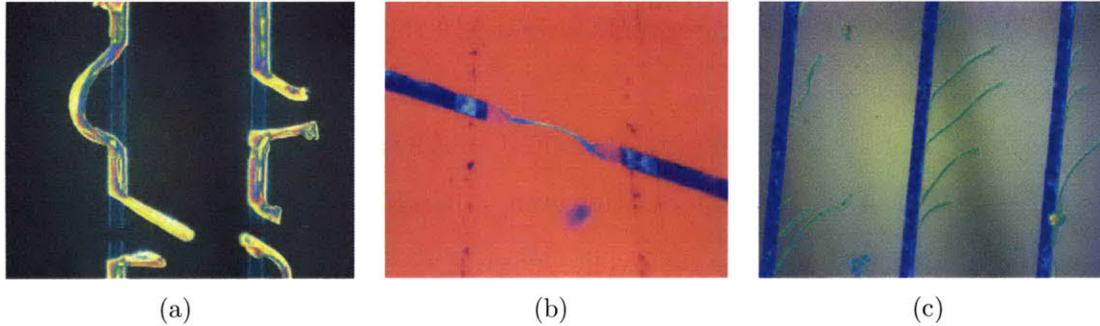


Figure 3-28: Plasma-baked phororesist. (a) Lines of photoresist on a plain SiO_2/Si wafer after etching and rinsing with acetone. The etching was done in the LOOE plasma-preen system at ~1 Torr pressure and 1000 W power. Line spacing is 110 μm. (b) Lines of photoresist on graphene after etching and rinsing with acetone. The etching was done in the NSL RIE according to the graphene etching recipe described in Section 3.3.5. Line width is 4 μm. (c) Attempts to remove the resist residue in (b) by immersion in hot NMP with ultrasonic agitation met with limited success, as the residue was elongated, but remained stuck to the chip surface. Line width is 8 μm.

Plasma-Therm reactive ion etcher (RIE) in the NSL. The process parameters used are described in Section 3.3.5. Even at these reduced pressures and powers, a resist residue is formed (Figure 3-28(b)). Here, the residue is much thinner, and when on top of graphene, it can be hard to discern (sides of image). However, where there is no graphene (center of image), due to a tear in the graphene film, the residue film is clearly visible (light blue, collapsed laterally in center). Lowering the thermal load on the sample by breaking up the plasma etching step into small intervals of etching separated by much longer times of allowing the sample to cool (15 seconds etch followed by 45 seconds cooling time) did not eliminate the formation of these residue films.

Attempts were made to remove this residue by aggressive solvation and agitation (Figure 3-28(c)). A chip with graphene lines and residue from the etching process was put in hot NMP (80 °C) for 20 minutes and sonicated on the highest power setting before being rinsed with H_2O and aggressively blown dry. The result is that the residue is deformed into streaks as it is blown dry, indicating that the solvent has somewhat penetrated the residue and caused it to become more soft and deformable. However, the residue does remain on the surface. It is possible that even longer

solvent soaks at high temperature might eventually remove the residue completely, but this was not investigated.

A chemical photoresist residue stripper (EKC 265) was also used to try to remove the residue on top of graphene lines. However, a handful of trials proved unable to remove the residue without also removing the graphene (a hotplate setting of 65 °C warming the stripper solution and an immersion time of 20 minutes was not sufficient to remove the residue, while a hotplate setting of 85 °C and an immersion time of 35 minutes removed the graphene as well as the residue). It is unclear whether the graphene delaminated and floated off into solution or was etched by the basic resist residue stripper. A systematic study was not conducted. But since other students have reported some success with the use of this same resist residue stripper, its effective parameter space may warrant further investigation.

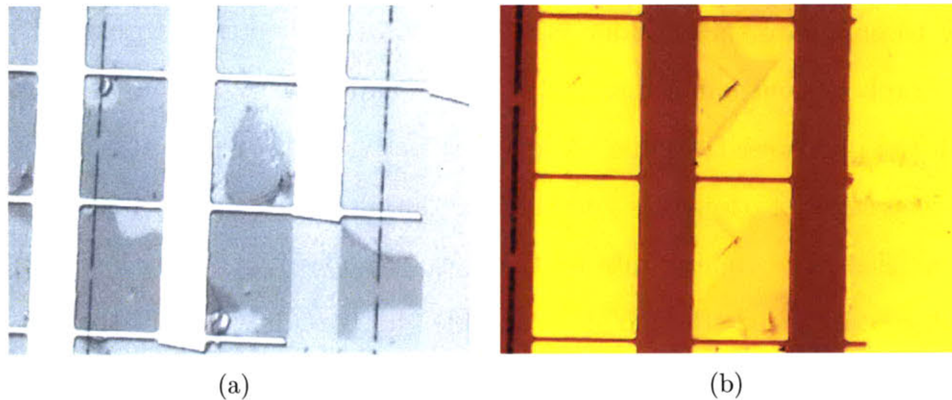
The resolution of this resist residue issue was to anneal in air at 400 °C for 20 minutes. This completely removed the bulk of the resist residue. A difficulty with this is that exposure to oxygen at high temperatures can also damage the graphene, but defects are not expected to form until at least 450 °C for the timescales considered here [46]. It is also possible to anneal in an inert atmosphere, which is described in more detail below in Section 3.5.3.4.

3.5.3.3 Photoresist Crosslinking by Overexposure

Photoresist crosslinking into a residual film which cannot be removed by normal solvation is also observed when the resist is overexposed. This effect was primarily observed with the AZ5214E image reversal photoresist, but was also seen for the NR71 image reversal photoresist and S1813 positive photoresist.

Figure 3-29 shows the consequences of an overexposure. A crosslinked film is formed on the surface of the photoresist. During development the exposed photoresist is removed, except for the film which may remain suspended over the developed areas. Upon drying, the film falls to the surface of the substrate where it remains. In Figure 3-29(a), the film can be seen to cover nearly the full area of some of the developed rectangles. This residual film forms a soft layer between the evaporated

metal and the graphene/substrate, making the metal pad more easily scratched and degrading the electrical contact to the graphene. This is shown in Figure Figure 3-29(b), which is the same chip as in Figure 3-29(a), but after metal evaporation and liftoff. The film shows up as a darker area of the metal because the roughness of the film is larger than that of the substrate, and roughness decreases the metal reflectivity.



(a) (b)

Figure 3-29: Residual photoresist film from a suspected overexposure. (a) Chip after development. The light grey is the substrate, the white area is unexposed photoresist, the dark lines are graphene, and the dark grey areas are the crosslinked photoresist film. Some areas of unexposed photoresist are missing (lower right), which is suspected to be due to poor adhesion resulting from the surface treatment with acid, as in Section 3.5.3.1. (b) The same chip as in (a) but after metal evaporation and liftoff. The bright yellow is a Cr/Au contact metal layer that adhered well to the substrate, while the darker gold color is due to the residue film underneath the metal. Applying pressure with a probe pin scratches the metal preferentially in the areas where the residue film is present (diagonal lines from lower left to upper right).

The thickness of the overexposed film is suspected to be proportional to the amount of overexposure. For proper exposure, there may be a thin film, but this film is likely to be ripped by the turbulent fluid flow of the development process, and will generally not deposit on the surface. However, for very small features (on the order of ~1-2 μm) even a thin film may pose a problem. The only practical solution to avoiding this problem with the film is to fully characterize each exposure and development process before processing devices, in order to discover the parameter range at which films will not form. If such parameters cannot be found, this may require changing the resist used. Other options commonly employed for dealing with this type of resist film residue problem (and why these other options are not useful when

fabricating graphene devices) are discussed in the next section.

3.5.3.4 Lithography Residue Removal by Annealing

Lithography resist residue is a common problem in microfabrication, and was encountered numerous times during the fabrications steps mentioned in this Chapter. The usual way to eliminate such residue is to perform a short etch with oxygen plama. However, graphene and nanotubes are organic compounds also, and will etch away along with the photoresist residue. A less destructive method is to use UV-ozone (a small concentration of ozone gas generated by an ultraviolet lamp) to remove small organic particles. The etching rate by this method, however, is very low, and is not practical for resist films (though it is notable that ozone will not strongly attack graphene as long as the temperature is kept below ~480 °C) [47].

Solvent rinses are also a common method used to remove resist residue, but these were generally found not to leave a pristine surface. Liftoff of both photoresist and PMMA e-beam resist leaves a residue on both the silicon dioxide substrate and the graphene film which can be seen by AFM (and sometimes optically). This residue typically consists of small (<30 nm) dots of material, generally considered to be resist polymer. Liftoff of the bulk of the resist happens within one minute of immersion in a solvent (typically acetone, but NMP and DCE have also been used with similar results). Use of longer liftoff times and hot solvents can improve the surface cleanliness, but only by a limited amount (Figure 3-30(a)). The use of NMP was found to be slightly more effective than acetone, but to still leave the surface rough (Figure 3-30(b)). Only when the sample was annealed at or above 400 °C in a mixture of Ar and H_2 was almost all of the resist residue removed (Figure 3-30(c)).

The standard annealing process used for graphene device fabrication is as follows. The sample to be annealed is placed in the center of a 1" diameter quartz tube, and the tube is sealed and purged with 600 sccm Ar and 400 sccm H_2 for five minutes to eliminate oxygen which might damage the graphene at high temperatures. Then the tube is inserted into a preheated furnace at 400 °C with the chip positioned at the center of the heating zone (the same gas flow is continued). The anneal is timed from

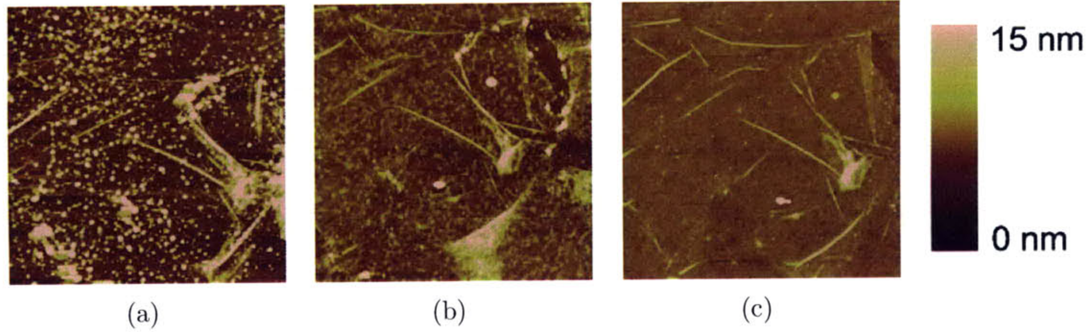


Figure 3-30: AFM height images of the cleaning of graphene. Image width is 2 μm. (a) Surface after liftoff of PMMA following metal deposition. Liftoff was in acetone for 10 minutes followed by hot acetone (90 °C hotplate) for 10 minutes. (b) Same surface as in (a) after rinse in hot NMP (90 °C hotplate) for 10 minutes. (c) Same surface as in (a) and (b) after annealing in Ar and H_2 at 400 °C for 5 minutes. Additional annealing shows no significant improvement.

the insertion of the tube into the furnace, and will typically last from 5-20 minutes. At the end of the annealing the tube is removed from the furnace and allowed to cool in air for 5-10 minutes, at which time the tube is warm but not hot to the touch. The gas flow is turned off and the chip is removed from the tube.

It is desirable to perform an anneal for as short a time as possible, for two main reasons. First, it is possible that trace amounts of oxygen (often present as an impurity in the Ar gas cylinder) can react with graphene and degrade its quality [46]. This may be mitigated, however, by the presence of hydrogen, which will reduce the partial pressure of oxygen by reacting to produce water. It is also possible that the annealing of graphene and removal of photoresist may cause graphene defects that had been "bridged" by a particle of photoresist to become more noticeable in their effect on transport.

Second, other materials on a chip may be affected by the heat load of an anneal. For example, gold will begin to dewet from the silicon oxide if kept at 400 °C for extended periods of time ($\geq$30 minutes). It is possible to use other materials for contacts (such a Pt or Pd) which are more stable at higher temperatures, but this may be undesirable for other reasons. Thus it is useful to know the removal rate of resist material at given annealing conditions, so that the minimum necessary annealing time may be estimated for a given amount of residue.

To achieve this, a series of annealings according to the above procedure were carried out for different annealing times and temperatures using a silicon wafer which had been coated (4,000 rpm for 60 seconds) with a thin layer of PMMA (996,000 molecular weight, 2% by weight in anisole). The silicon chips were heated at 175 °C for 5 minutes before spinning to remove adsorbates from the wafer surface, and again after spinner to remove solvent from the resist. The chips were cleaved in half, with one half reserved for measurement of the initial film thickness. The other half was annealed as described above, and inspected using the optical ellipsometer in the NSL (incident angle 70°, wavelength 632 nm). The observed etch rates are plotted in Figure 3-31.

An activation energy of 948 meV = 91.5 kJ/mol is sufficient to explain the measured etch rates. This is slightly below the activation energy of anionically polymerized PMMA (120-200 kJ/mol), though not as low as free-radical polymerized PMMA [48]. Since the resist residue remaining after liftoff of PMMA is generally ~30 nm in height, the necessary anneal times appear to be very short, as indicated by the efficacy of a 5 minute anneal in Figure 3-30.

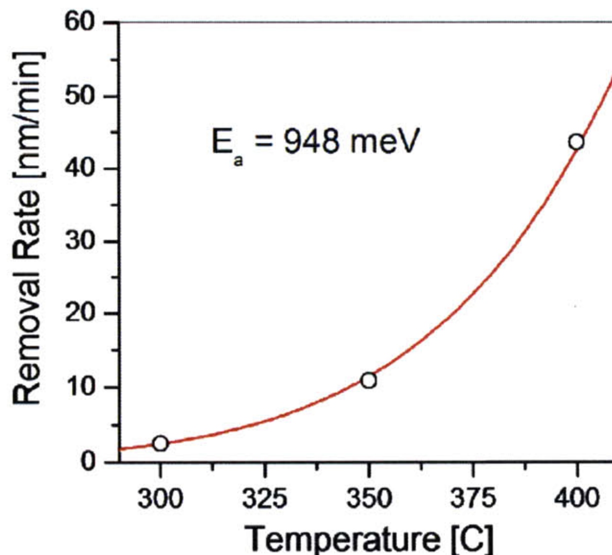


Figure 3-31: Removal rate of PMMA (996k MW) at various annealing temperatures under a flow of 400 sccm H_2 / 600 sccm Ar. Experimental data is shown with circles, and the activation energy E_a fit is shown by the red line.

There are a few considerations regarding the etch rates calculated in this manner. First, the rates are calculated for uniform films, and may be either higher for monolayer coverage because there is less material to be removed, or slower because the resist residue that remains after liftoff is somehow stabilized. Second, there is a finite time necessary to raise the temperature of the quartz tube and the gas and sample inside. It takes up to a minute for the temperature to recover to its preset value after insertion of the tube. And third, the temperature of the furnace may fluctuate during the anneal due to improperly set feedback parameters for the temperature controller. Etch rates for optically sensitive photoresists have not been collected, and are a suggestion for future work.

The result of this work is that annealing times for the removal of resist residue were limited to 5 minutes at 400 °C, as opposed to the 20 minutes used before this study. As seen in Figure 3-30(c), this adjustment still ensured sufficient resist removal, and additionally led to more reliable contact pad adhesion.

The annealing process can also be extended to remove the thick PMMA films (>500 μm) used in the graphene transfer process. An annealing procedure as described above, using an annealing time of 5-10 minutes (with the longer time used for thicker films), replaces the solvent rinse and dry steps as well as the annealing step described in Section 3.2.2.3. The results of this process are shown in Figure 3-32.

The graphene transferred by annealing is intact and clean, and indistinguishable by optical microscope and AFM from graphene transferred using the solvent PMMA removal method and a final annealing step. The annealing transfer process furthermore has several advantages over the solvent transfer process. First, the graphene film is transferred entirely even if there is an inital gap between the graphene/PMMA film and the chip. This is thought to be because the PMMA goes through a glass transition before decomposing, and therefore conforms to the chip surface. The solvent transfer process, by comparison, may fail if the PMMA film is completely dissolved before the graphene comes completely into contact with the chip surface, which may occur when solvent is trapped underneath the graphene/PMMA film. This failure is fairly common if great care is not taken to blow dry the solvent repeately, and to use

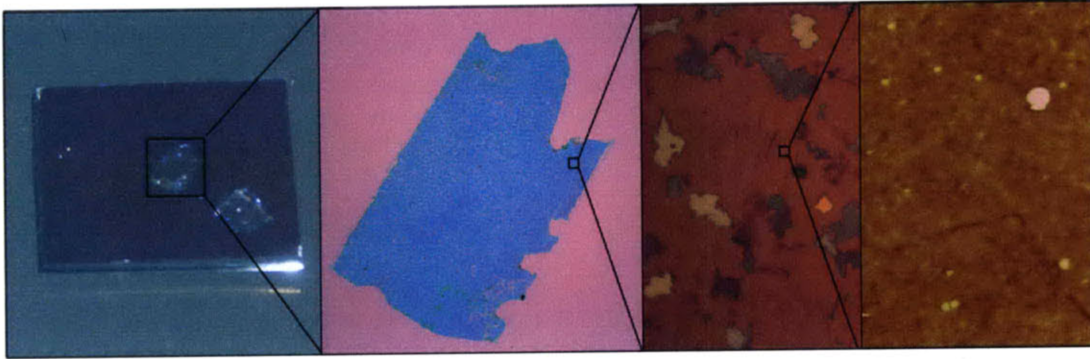


Figure 3-32: Graphene transfer by annealing. (Far left) Optical image of Si/SiO_2 chip (1×1 cm^2) with PMMA/graphene film placed on top, graphene side toward the chip. (Center left) Close-up of graphene transferred to chip after annealing. The entire graphene area is intact. (Center right) Close-up of transferred graphene, appearing identical to graphene transferred by the usual solvent method. (Far right) AFM image of transferred graphene, showing a relatively clean surface. The image size is ~1 μm, and the height scale is 10 nm, with lighter regions being higher than darker regions.

the pressure of the nitrogen gun to force the film into contact with the chip, all the while taking care that the applied air pressure does not tear or blow away the film.

Second, the annealing process has a higher potential throughput than the solvent transfer process. One way in which this is realized is through the reduction of processing time required by, roughly, the amount of time required for the solvent steps (drop/blow dry cycles and final solvent rinse). More importantly, however, is the ability to perform many annealing transfers in parallel by loading multiple samples into one furnace. This contrasts with the serial processing of solvent transfer, where each sample requires skilled attention throughout the time-consuming solvent drop/blow dry cycles.

A final benefit is that the conditions of annealing transfer are completely controllable, as opposed to solvent transfer where technique may vary from person to person or from one transfer attempt to another. The annealing transfer technique is thus scalable and readily optimized, two properties desirable for industrial implementation.

Chapter 4

Nanotube Devices

Carbon nanotube devices were fabricated into field-effect transistors, the electrical conductance of which was used to gain insights into both the nanotube growth and device fabrication process. Electrical cutting of nanotubes was used to evaluate the effect of different catalysts on the number of semiconducting and metallic tubes which are grown. The ability to grow one type of tube selectively is technologically important. In the process of making electrical cutting measurements, a number of different observations were made regarding abnormal device conduction. This points the way toward improved nanotube device fabrication techniques.

4.1 Electrical Cutting

A major goal of the nanotube field is to obtain ensembles of tubes of a given metallicity (metallic or semiconducting character) in order to create large numbers of devices with similar, useful behaviour. This has been partially accomplished through growth [49, 50] and fractionation methods [51, 52]. Often the techniques of Raman spectroscopy or fluorescence spectroscopy are used to determine the ratio of the number of metallic tubes (abbreviated M) to the number of semiconducting tubes (abbreviated S), which is called the "metal to semiconductor ratio" (abbreviated M:S). These methods often have the limitation of availability of only a few laser energies, which when combined with resonance energies, resonance window widths, and scattering matrix elements,

which in turn may vary between tubes of each chirality, results in a large uncertainty [53].

An alternative measurement of the M:S ratio can be made by observing the conductivity of a nanotube transistor as a function of the gate voltage. Semiconducting nanotubes will show depletion, while metallic nanotubes will show constant conduction. This is complicated, though, by the lack of reliable techniques for producing devices consisting of a single nanotube. Device yield (fraction of devices for which at least one nanotube bridges source and drain) and the average number of nanotubes comprising the channel of each device are directly related. In the case of independent tube positioning, the number of nanotubes per device N follows a Poisson distribution $P(N)$, and the device yield as defined above is $1 - P(0)$. Thus for high device yield based on a stochastic thermal CVD growth mechanism, most devices are expected to be comprised of multiple tubes. The gate sweeps of such devices will show some combination of metallic and semiconducting behaviour, and the metallicity and even the number of tubes cannot necessarily be determined with certainty. The solution to this problem of multiple tubes is the technique of electrical cutting, which is described below.

4.1.1 Method

Electrical cutting of nanotubes was first described by [54]. This technique makes use of the fact that nanotubes often fail independently when a large drain-source bias is applied (~1 V/μm). A gate sweep is acquired before and after each nanotube fails, and these sweeps are subtracted to determine the amount of current which the failed tube carried before it failed, independent of any other nanotubes in the device. This difference can be treated as a single-tube gate sweep for the purposes of deciding metallicity of the failed tube. Tube failure is induced by sweeping the drain-source bias toward a high voltage. The measurement is stopped once a current drop occurs, in order to avoid sequential nanotube failures in a single sweep. These bias sweeps also provide a check on the number of tubes that break, because nanotubes will saturate at 20-25 μA per tube. Current drops larger than this amount are likely due

to simultaneous failure of multiple tubes. An example of the measurements involved for the cutting of a single tube is shown in Figure 4-1.

The electrical cutting analysis is repeated for each observed current drop. For example, in Figure 4-1(c) there is another current drop at ~38 V drain-source bias. Sweeps (c) and (d) may thus be treated as inital sweeps (taking the place of sweeps (a) and (b)). For this device, the current drops to zero, and there is no conduction for the after sweeps.

The location at which a nanotube is cut can be observed by AFM (Figure 4-2). There is a gap along the length of the tube where it has reacted with atmospheric oxygen, with length ~100 nm. Multiwall tubes may have the outer tube(s) removed up to 1 μm away from the location of the cut.

4.1.2 Statistical Results

Nanotubes were grown on a number of chips by the procedures described in Chapter 3. Briefly, the procedure is as follows. Beginning with a chip from Stanford of 500 nm SiO_2 on a doped silicon substrate with embedded Pt contacts and PMMA resist layer with 5 μm openings, a catalyst solution was drop-cast and allowed to dry. After liftoff in acetone the chips were baked at 400 °C in air to anneal the catalyst. The nanotubes were then grown (Section 3.1.4.1). E-beam lithography with PMMA resist was used to define metal leads (30 nm Pd, or 5nm Cr / 50 nm Au) with a gap of 4 μm to make contact between the nanotubes and the contact pads. More details and images of a chip and devices are given in Figure 3-9. Slight differences in fabrication between chips are noted below. The results of electrical cutting for seven chips are given in Table 4.1.

Chips H25-7 and H25-8 were prepared concurrently under identical conditions, except for the difference of catalyst. The resulting M:S ratios are the most statistically certain, equal to 1:4.3 $\pm$ 1.1 and 1:2.3 $\pm$ 0.5, respectively. The probability that these or more extreme values would arise from a true distribution of M:S = 1:2 for the given total number of tubes is 8% and 74% respectively. Thus with over 90% confidence the M:S ratio of the iron-only catalyst C02 does not produce a uniform distribution of

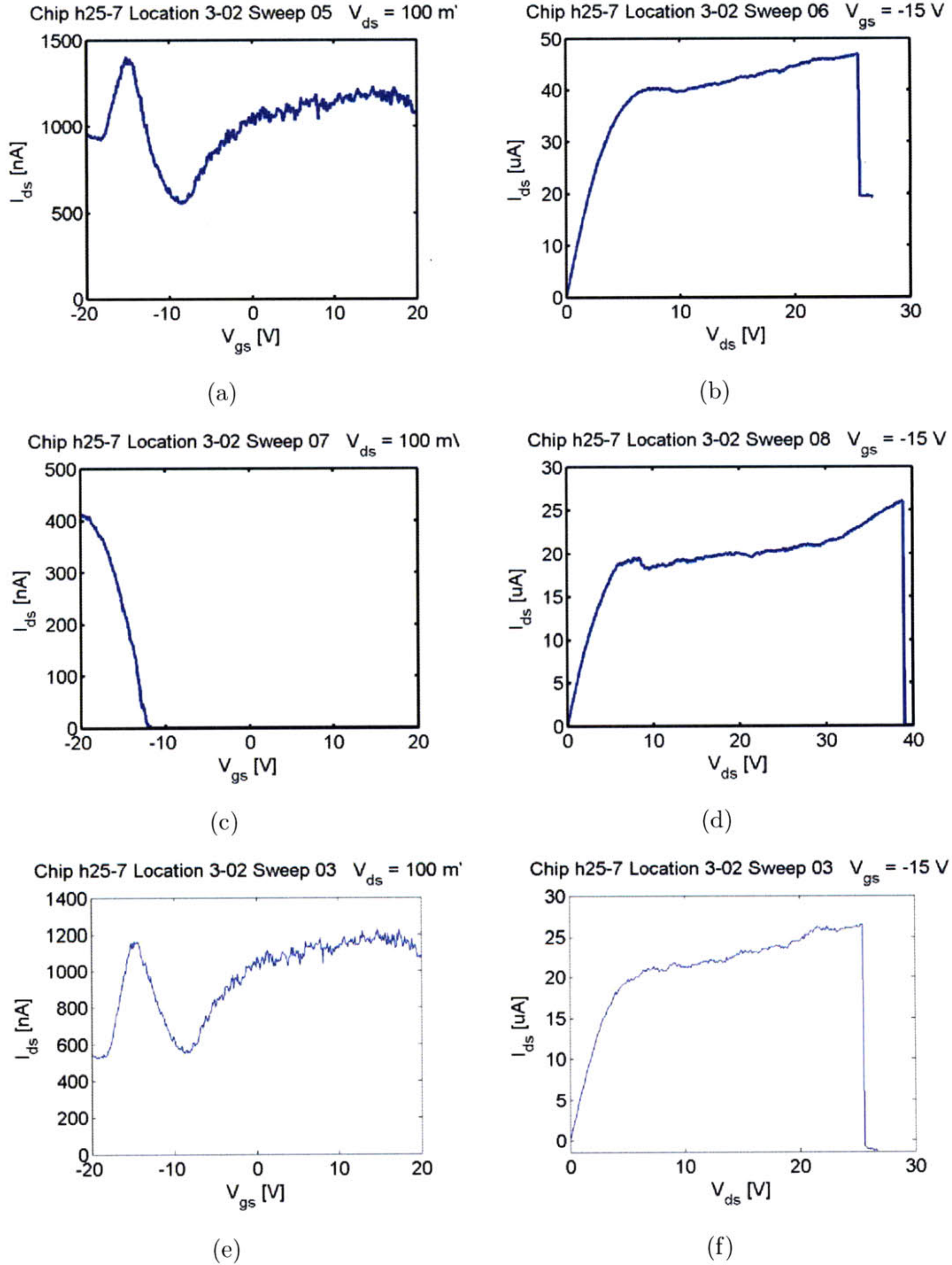
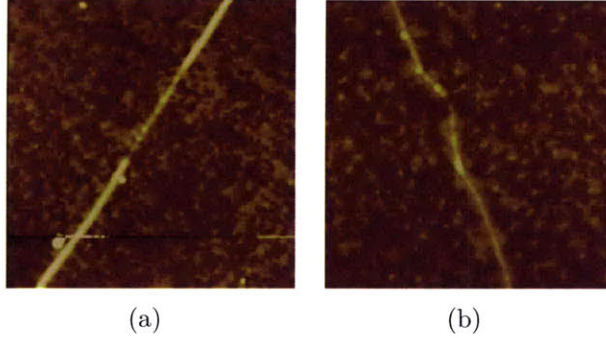


Figure 4-1: Deduction of metallicity by the method of electrical cutting. Gate sweeps before (a) and after (c) cutting yield a difference (e) which is clearly metallic. Bias sweeps before (b) and after (d) cutting yield a difference (f) which shows saturation consistent with a single nanotube. The cutting event is recorded as the vertical line at ~25 V bias in (b). A second cutting event can be seen in (d).



(a) (b)

Figure 4-2: AFM images of electrically cut nanotubes. Color scale is 10 nm, with light colors being higher. Image widths are: (a) 2 μm and (a) 1 μm.

Chip	Catalyst	M	S	M:S	Delay	LCD	M+S	LDC:M+S
J07	C02	16	10	1:0.6	17	8	18	44%
J08	C02	7	15	1:2.1	5	3	27	11%
J09	C02	14	10	1:0.7	5	3	23	13%
H25-7	C02	18	78	1:4.3	5	8	96	8 %
H25-8	C00	30	68	1:2.3	5	12	98	12%
H28-4	C00	11	27	1:2.5	0	0	38	0 %
H29-5	C02				11	18	38	47%

Table 4.1: Summary of electrical cutting results. Catalysts are described in Section 3.1.1. The number of metallic (M) and semiconducting (S) tubes is determined by the electrical cutting method described in the text. The ideal ratio of the number of semiconducting to the number of metallic tubes (M:S) is 1:2. Delay is the number of days between mixing of the catalyst solution and deposition/growth. The number of large current drops (LCD) counts current drops >30 μA. The ratio of large current drops to total number of tubes (LCD:M+S) is interpreted as a measure of the bundling of nanotubes during growth.

nanotubes during growth, instead producing a higher proportion of semiconducting tubes.

Another significant and unexpected observation regards the observation of so-called large current drops (LCD), which are defined as electrical cutting events where the current drop exceeds 30 μA. Since most nanotubes saturate and cut at currents 20-25 μA (closer to 15 μA for tubes with high resistance), observation of an LCD can be interpreted as the simultaneous cutting of two or more tubes. Typically, this means the tubes are in a bundle or comprise a multiwall nanotube. This may indicate, respectively, a high density of tubes or a larger catalyst size. The number of

LCDs (which are not counted for either M or S) in comparison to the total number of distinguishable tubes (M+S) is found to be dependent on the age of the catalyst solution.

For chip H28-4, the catalyst was prepared immediately before catalyst deposition and nanotube growth, and resulted in no LCDs. The four chips which were grown five days after catalyst preparation have an LDC ratio of 8-13%, and the two chips which were grown longer than 10 days after catalyst preparation have an LDC ratio of ~45%. Though the statistics are sometimes low, it is remarkable how well these values agree. These three data points imply that LDCs are dependent primarily on the age of the catalyst solution in a manner which accelerates with time and saturates at around 50% for the growth process used here. This seems to be independent of the presence of molybdenum in the catalyst, as judged from the available data. The aging of the alumina nanoparticles and iron nitrate must then account for this observation. One explanation is that the alumina nanoparticles bond together over time. This might be investigated by observing the residues of catalysts of various age by AFM to observe an increase of particle height with age. Another explanation is that the iron begins to react with the alumina and perhaps forms a complex with it, leading to larger iron nanoparticle sizes and more multiwall nanotubes, which could be measured as a changing height distribution with catalyst solution age.

The results of devices J07, J08, and J09 are more difficult to explain. These chips were grown under slightly different conditions from the other chips; J08 and J09 were grown without a catalyst anneal, while J07 was grown with an extra catalyst anneal (600 °C for 10 minutes) and was grown at a lower temperature (770 °C). Certainly, the lower density of nanotubes in these chips must result from some experimental factor not accounted for in the recorded parameters, or it may be a result of statistical fluctuations. Another possibility is that the density of active catalyst (assumed to be proportional to the number of nanotubes) affects the gas composition around the surface of the chip, and thus also the rate of nanotube growth and perhaps the type of nanotube grown. These catalyst density effects have been observed in other instances, but further work would be needed to isolate this effect, if present.

4.2 High-Bias Annealing

During the electrical cutting measurements described above, it was noticed that some devices showed a change in conduction after a bias sweep, even if there was no cutting event. This led to an investigation of a number of effects, including the removal of resist residue and the joining of crossing tubes. The results are detailed below.

4.2.1 Lithography Residue

The presence of residue on graphene devices after e-beam lithography was always observed. The initial approach to removing this residue was through additional solvent treatment. An example of this is shown in Figure 4-3. Both additional rinsing and hot solvent rinsing were found to assist in the residue removal, though residue agglomeration was an issue (round white feature in (b) through (d)).

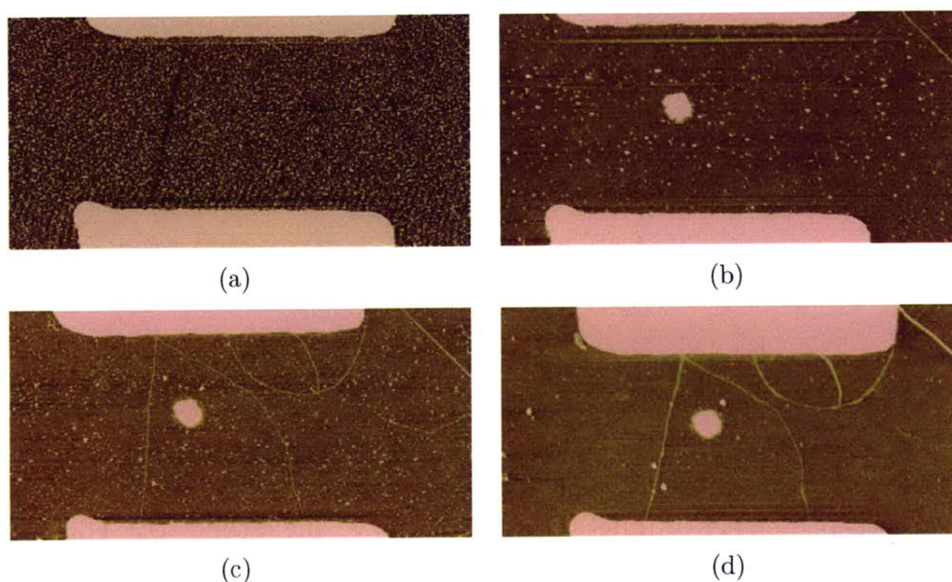


Figure 4-3: Residue removal by solvent rinse. (a) After liftoff in hot acetone for 2.5 minutes. (a) After additional rinsing with room-temperature acetone and dichloroethane, alternating between solvents for five iterations of ten seconds immersion for each solvent. (c) After repetition of the same procedure as in (a). (d) After repetition of the same procedure as in (a) and (c) with hot solvent (~56 °C). The tube which appears to the right of the large residue dot does not reach the bottom contact, so transport is only through the tube to the left of the residue dot. Color scale is 10 nm with height increasing from dark to light..

It is interesting to note that in Figure 4-3(a) the nanotube is visible as a depressed region. This is because previous electrical testing at high bias caused heating of the nanotube, which in turn caused thermal decomposition of the photoresist residue in contact with the nanotube. The corresponding measurements are presented in Figure 4-4.

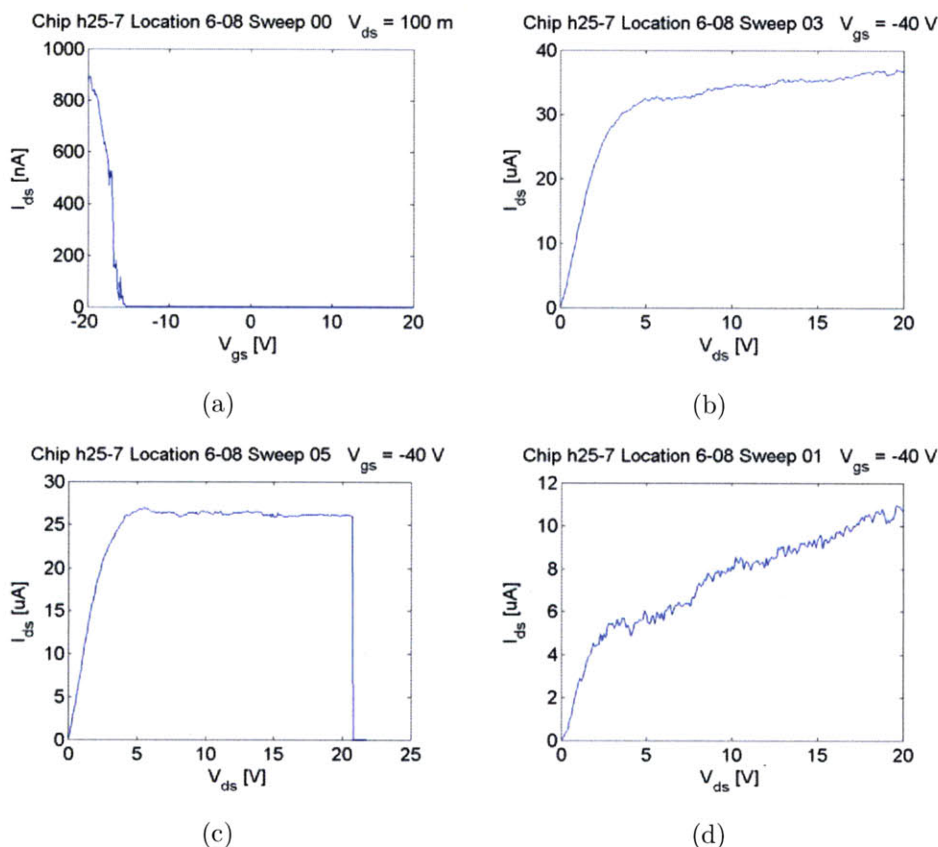


Figure 4-4: Residue removal by high bias annealing for the same device as in Figure 4-3. (a) Gate sweep showing that the tube is semiconducting. (b) Initial drain-source sweep showing conduction higher than that expected for a single tube. (c) A second drain-source sweep showing conduction expected for a single tube. (d) The difference between (b) and (c), corrseponding to the drain-source current lost from an electrically cut outer tube. The outer tube conduction is degraded due to interaction with the resist.

This high bias current annealing of nanotube devices as a way to remove residue was employed two years before the publication of a similar effect in graphene by Moser *et. al.* [13], though for the purpose of this thesis it was not studied in depth. This device consists of two tubes, thought to comprise a double-walled carbon nanotube,

with bias sweeps given by Figure 4-4(c) for the inner tube and Figure 4-4(d) for the outer tube (both are semiconducting).

The bias sweep of the outer tube shows a very low saturation current (~5 μA) compared to the saturation current of the inner tube (~26 μA). This saturation current suppression is thought to be due to the interaction of the outer tube with the residue. As the tube heats up, the residue will melt and flow around it. The tube may react with the residue causing increased scattering (resistance) and decreased saturation current due to the greater abundance of perturbative potentials which couple electrons to optical phonons.

4.2.2 Crossing Nanotubes

It was found on several occasions that a device would saturate at a very low current (≤ 5 μA), and that at high bias the same device would experience a large increase in current before breaking. This was correlated with AFM images of the devices, with the observation that this behaviour occurs when crossed nanotubes form the only conducting channel between contacts. An example of this is shown in Figure 4-5.

As seen in the AFM image of Figure 4-5(a), one nanotube comes from the contact at upper left, and the other nanotube comes from the contact at lower left, making contact only at the cross near upper right. The net behaviour of these nanotubes is semiconducting (Figure 4-5(b)), though the implication of this I-V characteristic is that *at least one* of the two tubes is semiconducting. The metallic conduction of one of the tubes would be limited by the semiconducting behaviour of the other, since the conductance (proportional to the current) adds reciprocally for nanotubes in series, resulting in an observed semiconducting behaviour for the entire device. Each of four devices for which this behaviour was observed displayed a net semiconducting gate sweep.

This crossing behaviour was interpreted as the formation of an improved junction between nanotubes. Over half of the normal saturation current for a typical nanotube is obtained, even though the total device has a crossing junction as well as ~4 times the lenghth of a typical nanotube which bridges the contacts directly. This may be

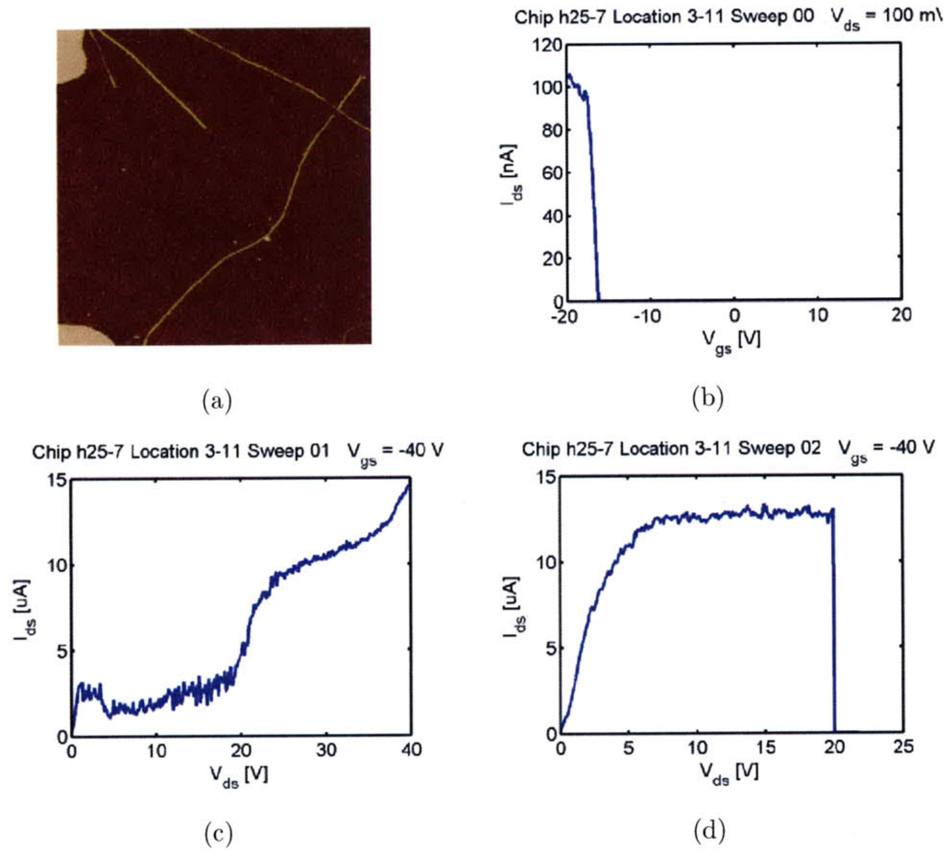


Figure 4-5: High bias annealing of crossing nanotubes. (a) AFM image of the device, showing crossing tubes. Contacts are the white regions at the upper and lower left, and they contact the nanotubes beyond the edges of the image. Image width is 5 μm. (b) Gate sweep of the device, showing semiconducting behaviour. (c) Initial drain-source sweep showing premature saturation at 2-3 V, onset of annealing at 20 V, annealed saturation at ~30 V, and linear current rise indicating impending cutting at 37 V. (d) Another drain-source sweep taken after the one in (c) showing the irreversible current increase due to high-bias annealing. The saturation curve shows the ideal form of that of an isolated tube (but with lower saturation current of 12.5 μA). The tube is electrically cut at V_{ds} = ~20 V. Tube height is 3.3 $\pm$ 0.5 nm. The drain-source voltage sweep rate was 1 V/s.

partly due to the presence of residue which, just as it may bond to an outer tube to decrease conductivity, it might also bond in the junction region and bridge the two nanotubes together. The high current during the annealing process is also thought to assist the formation of a stable final junction configuration. The possibility of studying the nanotube junctions thus formed, and the possibility of their use as ballistic logic devices, provided the initial proposal for this thesis. Since time and budget constraints dictated a move toward study of graphene devices as opposed to nanotube devices, this direction of research remains open.

4.3 Tier Effects

The saturation of the drain-source current of a nanotube device will ideally look like Figure 4-4(c) or Figure 4-1(f). However, a number of different abnormal shapes of the saturation curve were also observed. In addition to the annealing effects shown in Figure 4-5(c) for crossed nanotubes, bias sweeps (along with their corresponding gate sweeps) can be used to determine whether a double-walled tube is present, the diameter of the tube through impact ionization, and the appearance of p-n junctions within the nanotube.

4.3.1 Double-Walled and Bundled Nanotubes

Saturation of the drain-source current of a device at values well above 20 μA typically indicates the presence of multiple nanotubes. Often, an AFM image of the device will show only "one" nanotube crossing between contacts. In this case there are two possibilities: multiple nanotubes are bundled (lie side by side, held together by van der Waals forces) or together form a multiwalled nanotube. Typically, these possibilities cannot be distinguished by AFM due to its limited resolution, and can only be distinguished by Raman spectroscopy if the laser energy falls within the resonance window of both nanotubes. However, bias sweeps may provide an indication of the nanotube arrangement as indicated in Figure 4-6.

Here are considered only devices which saturate or cut at ~40 μA, indicating

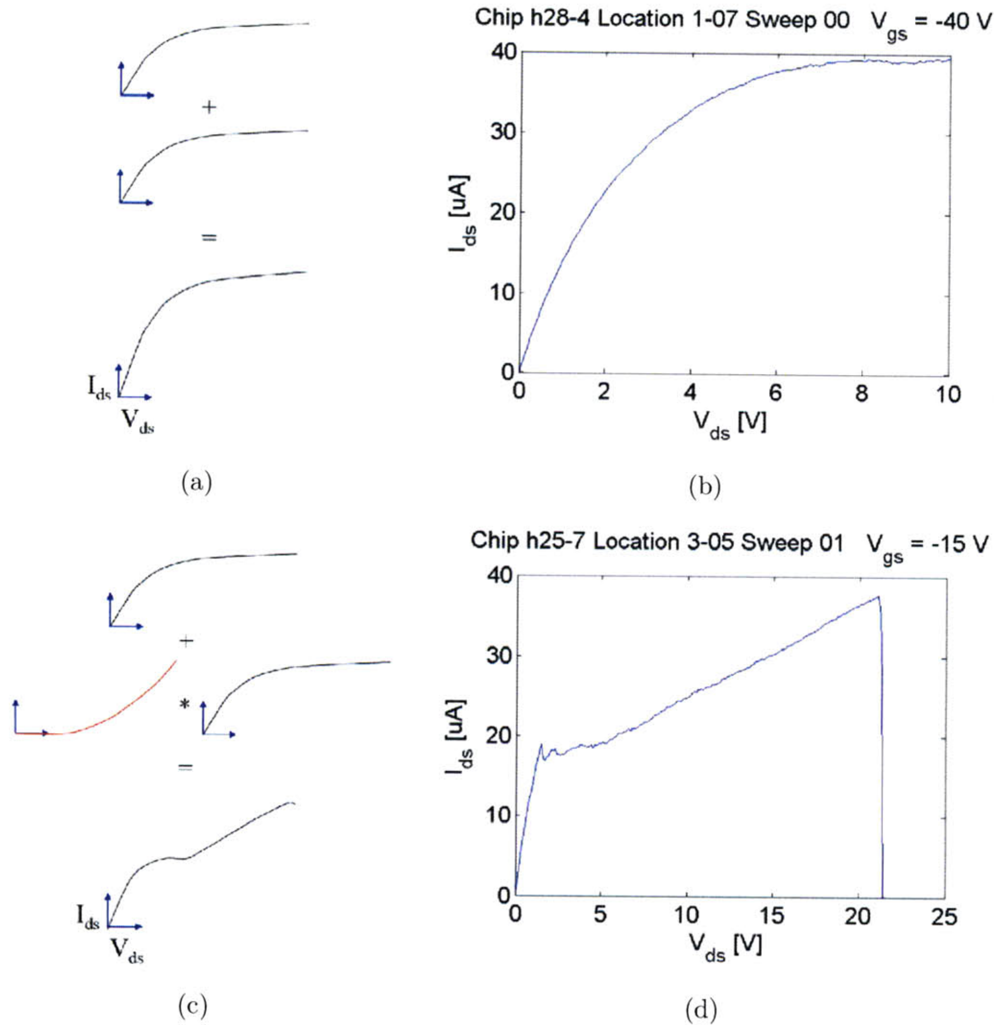
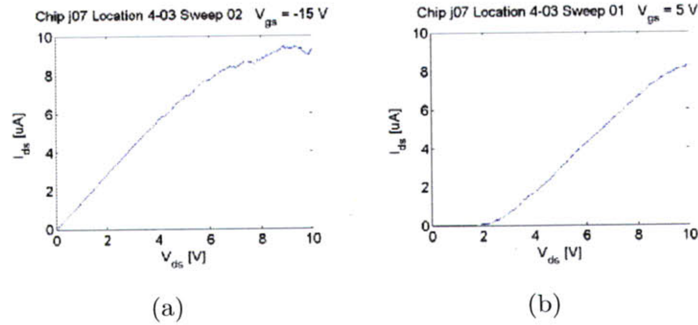


Figure 4-6: Diagrams of bias sweeps for different combinations of nanotubes. (a) Independent or bundled tubes, where each tube (top and center) contributes independently to the total conduction (bottom). (b) Bias sweep for a device corresponding to the diagram in (a), consisting of one metallic and one semiconducting tube (as determined from the gate sweep, not shown). Low-bias resistance is 59 kΩ and saturation current is 39 μA. (c) In a double-walled nanotube made of two semiconducting tubes, the outer tube (top) contributes normally, but there is a resistance between nanotubes. The voltage drop across the inner tube is therefore less than that along the outer tube (center), leading to a shift to higher bias voltages of the conduction curve of the inner tube. In the combined conduction (bottom), the contribution of the outer tube dominates at low bias, while the contribution of the inner tube is visible as a second rise in conduction at higher bias voltages. (d) Bias sweep for a device corresponding to the diagram in (c), consiting of two semiconducting tubes (as determined from the gate sweep, not shown). The low-bias resistance is also 59 kΩ and the maximum current is 38 μA.

that the device is likely composed of two nanotubes. In a bundled arrangement, the nanotubes are each gated equally, and so the current through the device is the sum of the currents through each nanotube if they were isolated. The metallic or semiconducting character may be judged from a gate sweep of the device. If the gate sweep shows depletion, both tubes are semiconducting. If the gate sweep does not show depletion but shows a large p-type conduction (typical for devices made from a single semiconducting nanotube using the fabrication and testing process described in this thesis), the device has one metallic and one semiconducting tube. If the gate sweep shows no depletion and no such asymmetry, the device is likely composed of two metallic nanotubes. Alternatively, the difference in bias sweeps between positive and negative (or zero) gating may be used to differentiate between semiconducting and metallic components. A naturally p-doped semiconducting tube like the ones produced in this thesis will have a threshold drain-source voltage at positive voltages but not at negative voltages, while a metallic tube will have no threshold voltage in either case (see Figure 4-7).



(a) (b)

Figure 4-7: Bias sweeps showing a threshold voltage for a single semiconducting nanotube. (a) Bias sweep at negative gate voltage, in the dominant p-type conducting region. (b) Bias sweep at positive gate voltage, showing a threshold for n-type conduction of ~2 V. This can be used to distinguish a semiconducting tube from a metallic tube, which for all gating voltages will have no threshold as in (a).

For multiwalled nanotubes, transport occurs primarily through the outer wall of the nanotube [54]. The inner tubes are coupled to the outer tubes through an intertube resistance. This coupling does not appear to be dependent of the metallicity of the nanotubes. Thus, the current flowing through the inner tube is lower than that

for an outer tube at a given drain-source voltage due to the voltage drop between the outer and inner tubes. This manifests itself as a very skewed contribution to the total bias sweep; often the inner nanotube will not saturate before the limit of the measurement is reached, or the device is electrically cut.

4.3.2 Impact Ionization

The linear rise in current at high bias voltages seen in Figure 4-6(d) (due to the inner tube of a double-walled nanotube), at first appears similar to another phenomenon noted in a number of devices. It was noted that before the electrical cutting current drop, the current would begin to increase linearly. This linear region of the bias sweep displays decreased noise, and often there is a small decrease in current at the beginning of this linear increase. Two examples of this behaviour are shown in Figure 4-8.

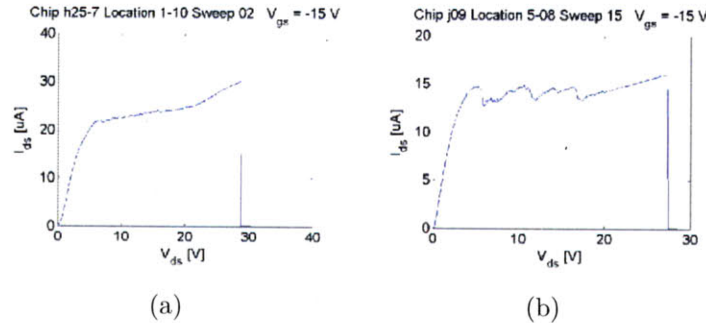


Figure 4-8: Two bias sweeps from different single semiconducting nanotubes showing impact ionization as a linear current increase at high bias voltages. (a) Impact ionization begins at about 22 V bias. (b) Impact ionization begins at about 20 V bias. The saturation before ionization is very noisy, but the noise is eliminated at the onset of impact ionization.

The analysis explaining this transport feature was published three years after these measurements, by Liao *et. al.* [55]. The linear current rise at high bias is due to the impact ionization of carriers as the third subband of the nanotube becomes populated by current injected from the drain. These high-energy carriers can scatter into lower bands, resulting in many more charge carriers.

The benefit of the impact ionization process is that it is an indicator of impending electrical cutting due to high temperature reaction with atmospheric oxygen. As

such, it is notable that after impact ionization is observed, the low-bias saturation of the nanotube often exhibits less variability and higher saturation current. This makes sense in light of the cleaning effects of high nanotube temperatures noted previously in Section 4.2.1.

4.3.3 Optical Bump

The term "optical bump" is used to describe a feature of the bias sweep at the onset of saturation, where the current decreases sharply after the onset of optical phonon scattering. This type of feature is not reported elsewhere in the literature, and is thought to be due to residue remaining on the nanotubes after device fabrication. The optical bump appears in numerous forms as illustrated in Figure 4-9.

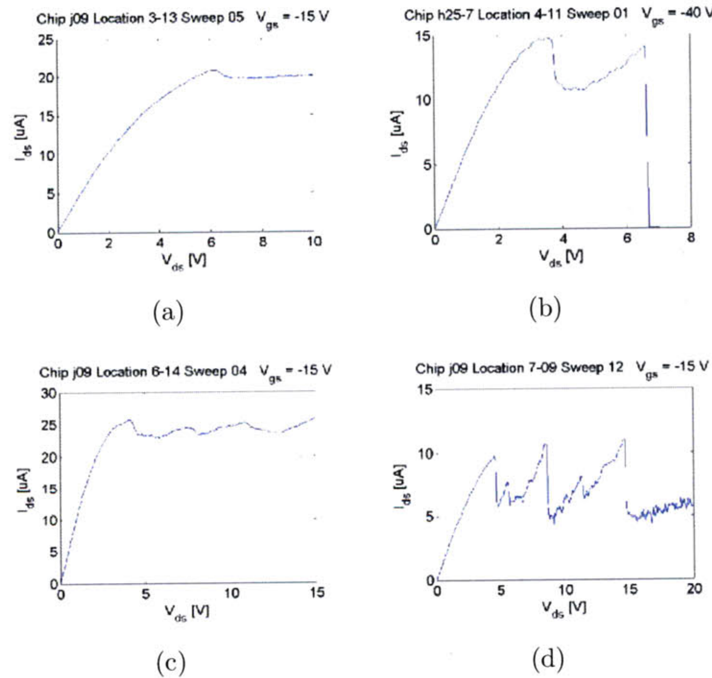


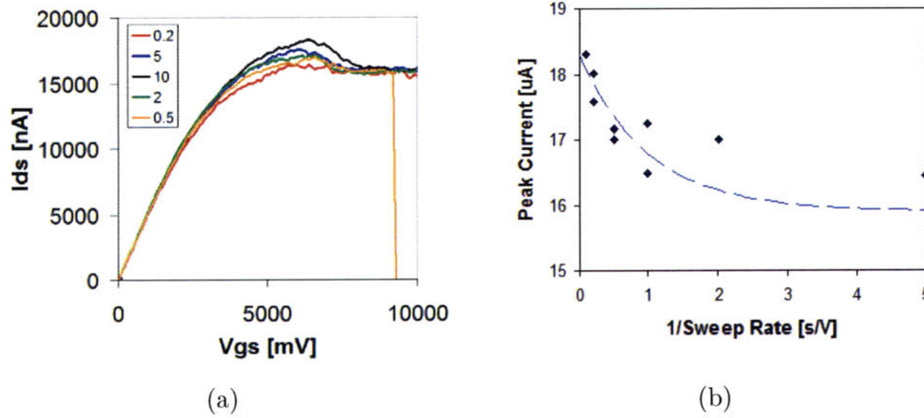
Figure 4-9: Various forms of optical bumps in bias sweeps, indicated by local maxima in the draon-source current. (a) A single metallic tube. (b) A single semiconducting tube showing a very large fractional current decrease. (c) A single semiconducting tube showing three bumps and an impact ionization linear increase of current (far right). The peaks are spaced at an interval of ~4 V. (d) A single semiconducting tube remaining after cutting of two nanotubes (semiconducting and metallic). The peaks are spaced at an interval of ~5 V, but the peaks vary significantly in height and slightly in position between successive bias sweeps.

The optical bumps of a device's bias sweeps may vary from sweep to sweep, and may be annealed away by application of very high bias. This indicates that the optical bump is due to something that may be thermally decomposed, such as resist residue. The periodic behaviour of the optical bump is intriguing, and requires another explanation. One possibility is that the optical bumps are due to incomplete conduction channels, such outer or adjacent nanotubes which were previously cut, or additional nanotubes which only lie along the conducting nanotube for a portion of the channel length, or additional nanotubes which simply cross the conducting nanotube. In this schema, sections of additional tubes contribute to the conduction at low bias, but the transfer of current to the main conducting nanotube is interrupted with the onset of optical phonon generation. The mechanism of such a process requires further development.

The other interesting feature of the optical bump is the possibility for a very high negative differential conductance, as in Figure 4-9(b) and Figure 4-9(d). These steep slopes suggest a mechanical origin of the conductance decrease, occurring as a result of increased heat generation due to optical phonon scattering. Another possibility is a phase transition of the residue polymer in contact with the nanotube, since wetting of the nanotube by a melted polymer would increase scattering due to increased deformations of the nanotube [56]. Evaluation of this method will require concurrent evaluation of the surface state by AFM or Raman spectroscopy.

When the bias was not increased into the annealing regime, the optical bump was found to be reproducible. It was also found to vary with the sweep rate, as indicated for one semiconducting device in Figure 4-10(a). This is strong evidence that the optical bump is a low-temperature effect. The temperature increase of a nanotube above its surroundings at fixed position and at (dynamic) thermal equilibrium is proportional to the power dissipated in the tube. However, the surroundings of the nanotube are not in thermal equilibrium, since the time scales of measurement are short compared to the time scale of heat transfer by the thermal conductivity of the silicon dioxide and metal contacts. Thus, over the course of seconds to minutes, the surroundings of the nanotube will heat up, and the nanotube temperature will

increase accordingly.



(a)

(b)

Figure 4-10: (a) Optical bumps for various drain-source bias sweep rates, given in the legend in units of V/s. The bump is reproducible; the sweeps were acquired in the order listed in the legend. (b) Plot of the maxima in (a) as a function of the sweep rate (with additional data for curves not shown). An exponential decay with decay constant $\tau \approx 1$ s/V (blue dashed line) fits the data.

The temperature increase of the surroundings of the nanotube should be proportional to the total energy dissipated in the nanotube during a characteristic time scale. In the case of a linear relation between the bias voltage and the current (as is the case at low bias), the power dissipated is proportional to the square of the bias voltage, and the total energy deposited is proportional to the bias voltage multiplied by the time interval. For a fixed bias voltage (e.g., the peak of the optical bump), the time interval to reach this bias voltage is inversely proportional to the sweep rate. If the optical bump height varies linearly with the temperature, then it should also vary with the inverse sweep rate in the same manner as the temperature. The appropriate form of variation is a decaying exponential, since the thermal conductivity provides heat transfer to remove the heat generated by the nanotube. This is verified in Figure 4-10(b), where a decaying exponential with constant $\tau \approx 1$ s/V is found to fit the data well. This time constant, evaluated for the relevant voltage values of the optical bump peak of ~6 V, gives $\tau \approx (1 \text{ s/V})(6 \text{ V}) = 6$ s.

A possible explanation of the optical bump arises from the results of Section 4.3.4, where hysteresis is found to play a major role in high bias measurements. The optical

bump is interpreted as due to a change in the effective gating of the nanotube due to charge trapping around it (in the oxide or in the nearby residue). When charge leaks into the oxide, the effective potential of the nanotube moves closer to zero. Since for most devices the conductance approaches a minimum around zero gate voltage, the shift in effective gate voltage is associated with the current decreases of the optical bump. The two behaviours seen in Figure 4-9 can be interpreted as due to differing methods of charge trapping. The smooth decrease of the conductance of Figure 4-9(a) and Figure 4-9(c) is due to independent traps with a relatively low energy barrier for population by charge. The modulation can be thought of as due to multiple trap energy levels, perhaps due to the population of a single trap by multiple carriers, which is especially appropriate if the charge tunnels to nearby pieces of resist residue. The other behaviour, the sharp conductance decrease of Figure 4-9(b) and Figure 4-9(d), can be thought of as due to an avalanche breakdown which changes the effective gating by a large amount. Both effects could be facilitated by the temperature increase which results from applying a high bias.

This explanation could be checked by EFM measurements of the potentials surrounding the tube during high-bias transport. The most likely candidate for charge trapping is the photoresist residue on the surface of the chip, because 1) devices in the literature do not exhibit this effect and are also in general free of such residue, and 2) high-bias annealing will remove residue adjacent to the nanotube, as well as eliminate the optical bump.

4.3.4 P-N Junction Formation and Hysteresis

During the course of electrical cutting measurements an unexpected behaviour was observed for metallic nanotubes. The saturation current was found to be dependent on the gate voltage at which a bias sweep was taken. An example of this is shown in Figure 4-11. While a similar behaviour had been observed in and explained for semiconducting nanotubes [57], an explanation for the metallic case was not formalized until three years later. In 2008, Meric *et. al.* explained that for graphene, which also behaves metallically, a similar saturation could be observed as a result of doping

of the graphene by the metal contacts [58]. This causes the equivalent of the Fermi level pinning seen in semiconducting nanotubes, and results in the formation of p-n junctions. As a p-n junction is forming at one contact, the bias current levels off for a short while, before increasing again as the full carrier density is regained on each side of the junction.

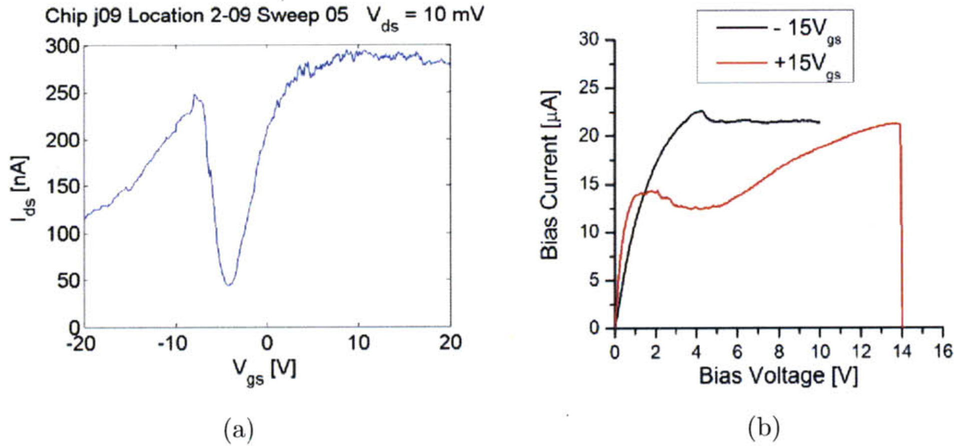
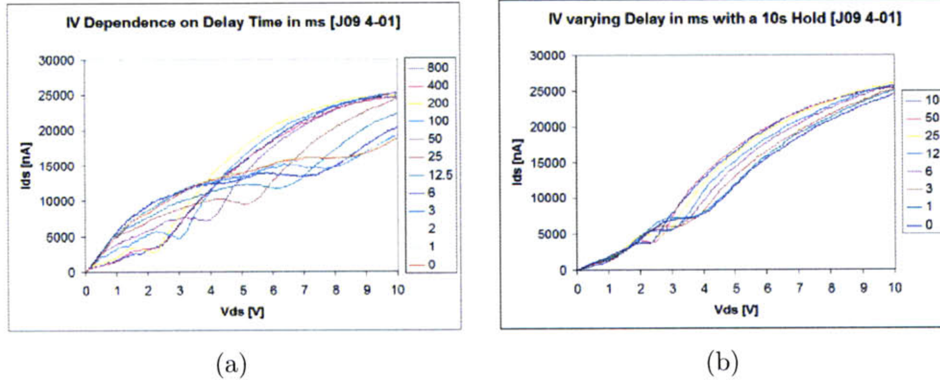


Figure 4-11: Metallic tier behaviour as demonstrated in a single metallic nanotube device. (a) Gate sweep showing metallic behaviour. (b) Bias sweeps at negative (black, p-type) and positive (red, n-type) gate voltages. The n-type conduction displays nominal saturation behaviour, but the p-type conduction has a different low-bias resistance and an initial saturation at currents much lower than for the p-type sweep, though the current begins to rise again at higher bias voltages until the same saturation is reached as for p-type conduction.

However, in the process of examining this tier behaviour, a bias sweep-rate dependence of the tier was observed which was not accounted for by the interpretation of p-n junction formation (Figure 4-12). Bias sweeps were acquired by first applying the gate voltage (but no bias voltage) to the device for a specified amount of time (0 seconds in Figure 4-12(a), 10 seconds in Figure 4-12(b)), and then beginning to sweep the gate voltage with fixed step size but varying the delay time between sweeps, while measuring the drain-source current. Measurements were taken several minutes apart to ensure that the sweeps were independent.

The sweep rate is proportional to the inverse of the delay time. With fast sweep rates, the tier is most pronounced, attaining its highest current values (Figure 4-12(a)). With slower and slower sweeps, the bias sweep behaviour converges to a



(a) (b)

Figure 4-12: Bias sweeps illustrating the time dependence of the metallic tier for a single nanotube. (a) Bias sweeps with no hold time; sweeps begin as soon as the gate voltage is applied. (b) Bias sweeps with 10 s hold time; sweeps begin 10 seconds after the gate voltage is applied. The primary cause of variation between sweeps is the length of time that the gate voltage is applied. The gate voltage is 10 V for both figures.

linear increase in current followed by a normal saturation curve, so that the peak or plateau of current all but disappears. The time dependence suggests that the heating of the tube may be the cause of this variation, just as for the optical bump discussed in Section 4.3.3.

However, the hold time, during which no bias is applied, will not affect the heating of the nanotube. Therefore the altered behaviour of Figure 4-12(b) cannot be due to nanotube heating. Instead it was determined that a time-varying hysteresis must be the cause of this behaviour.

Hysteresis was noted during the first electrical measurements performed in the course of this thesis work. It manifests as a shift of a gate sweep curve depending on whether the gate voltage is being swept upward (toward positive voltage) or downward (toward negative voltage). It was quickly determined that, to simplify analysis and focus on the matters at hand, that gate sweeps would only only be acquired as upward sweeps, and the corresponding downward sweep would be ignored. Upon the realization that hysteresis might be involved with the sweep rate dependence, new measurements of the extent of hysteresis in these nanotube devices were taken. The hysteresis turns out to be significant, as demonstrated by measurements on metallic tubes in Figure 4-13.

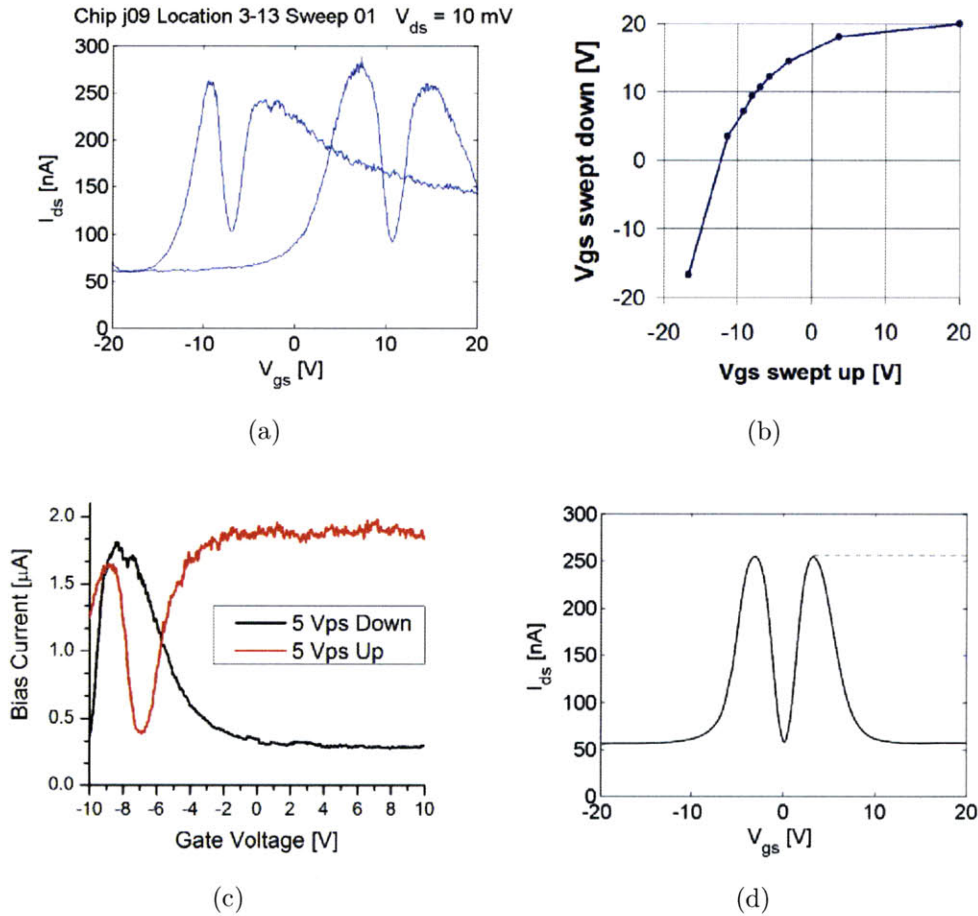


Figure 4-13: Hysteresis in a metallic nanotubes. (a) Upward and downward gate sweeps show the conduction curve of each gate sweep shifted toward the initial gate voltage. (b) Hysteresis plot of the corresponding features (maxima, minima, and midpoints) between up and down sweeps in (a). (c) Upward and downward gate sweeps for another metallic device, with 10 s hold time. Here current is pinned at the maximum and minimum value, respectively. (d) Diagram of the conduction of the device in (a) (and similarly for all other metallic nanotubes) in the absence of hysteresis. The grey line in (d) shows the conduction at positive gate voltage if the defects are instead subtractive.

By varying the sweep direction, an estimate of the hysteresis can be obtained by comparing equivalent features of the conduction curves. For example, the gate voltages at corresponding local maxima in each sweep can be equated, and similarly for local minima, and the midpoints between these extrema. Doing so allows construction of a hysteresis curve such as that shown in Figure 4-13(b) from the data in Figure 4-13(a). A numerical value for the hysteresis is given by the intercepts of the hysteresis curve (~12-15 V) added together. The device shown in Figure 4-13 exhibits a hysteresis of ~25 V, and thus has an effective gating range of $40 - 25 = 15$ V. Most devices tested exhibit larger hysteresis. This large deviation from the ideal of no hysteresis means that care must be taken when calculating mobilities or observing any feature of the gate sweeps near the end of the sweep.

By varying the hold time, it is shown that even metallic conduction which seems to have only one peak with differing values of drain-source current on either side (such as Figure 4-1(e) or Figure 4-11(a), seen for the majority of metallic nanotubes), has the double-peaked character of Figure 4-13(a). This is because an extended hold time allows the effective gating range to be extended. The expected gate sweep, then, looks like that presented in Figure 4-13(d). There is a uniform baseline of conduction, with peaks attributed to impurities. The peaks can be of significant height compared to the baseline of conduction, with the field-effect mobility in the trough of Figure 4-13(a) calculated to be 12,000 cm^2/Vs. This is comparable to or higher than the mobility of many semiconducting nanotubes from the same chip, and indicates that these peaks may be useful from a device perspective.

However, if the uniform baseline happens to be specific to only the few devices measured, the conduction curves may instead be interpreted as follows. At large negative and positive gate voltages there is constant conduction, but having different values depending on the various contributions to the resistance to p-type and n-type conduction. Near $V_{gs} = 0$, the conduction varies smoothly between these two extremes. In some cases as in Figure 4-13(a), the two regions of conduction may overlap, giving a net conduction near $V_{gs} = 0$ which is the sum of the baseline conduction at either extreme of gate voltage. Defects or residue then cause the reduction

in conduction (a "trough") such as to make the remaining heightened conduction on the negative gate voltage side appear to be a conduction peak, and similarly with the positive gate voltage side.

A final alternative is that the "trough" is due to an actual transport gap in the metallic nanotube and not to residue or impurities. Experiments designed specifically to determine which interpretation is true are needed. In any case, it is the reality of hysteresis (and not the interpretation of specific gate sweep features) which is of most interest.

The hysteresis may be modeled as mentioned previously in Section 4.3.3, as charge leaking into the substrate or nearby residue. At low gate voltages such as are used in the current measurements, the leakage rate may be modeled as linear in the effective voltage difference between the nanotube and the gate. This is shown schematically in Figure 4-14(a).

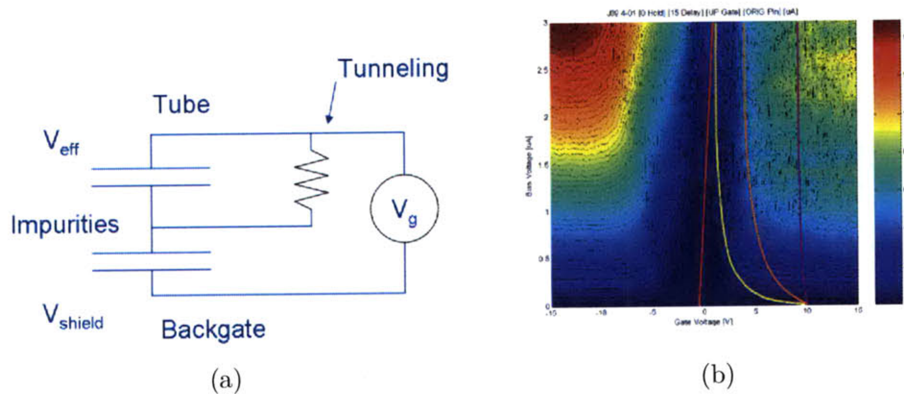


Figure 4-14: (a) Circuit diagram for charge tunneling onto traps near the nanotube. The charging time constant is $\tau = RC$. (b) Conduction map for the same device as in Figure 4-12 which shows sweep-rate dependent tiers. Bias voltage varies vertically from 0 (bottom) to 3 V. Gate voltage varies horizontally from -15 V (left) to 15 V. The color scale indicates drain-source current from 0 (blue) to 15 (dark red) μA. The minimum conduction point follows the line $V_{gs} = V_{ds}/2$, marked in red. The yellow, orange, and purple lines plot the effective gate voltage as a function of bias voltage for consecutively shorter times for the model given in (a), for an applied gate voltage $V_{gs} = 10$ V. This conduction map was obtained using fast sweep rates, to mitigate the effects of hysteresis. A p-n junction is formed to the right of the conductance minimum, and shows a lower saturation current than the left side where carriers are of a single type.

With this model, the effective gate voltage experienced by the nanotube (actual

gate voltage screened by nearby charge) should decay toward zero (or because of nonlinear effects, some constant value) with a characteristic time constant $\tau = RC$, where R is the effective resistance for the movement of charge to the traps, and C is the capacitance of the traps with respect to the nanotube. The impact that this has on gate and bias sweeps depends on the value of τ and the actual conductivity of the device as a function of gate and bias voltages. An approximation of this behaviour is shown in Figure 4-14(b). The curved yellow, orange, and purple lines indicate the effective gate voltage for a given bias voltage, assuming the bias voltage is swept at a constant rate, for consecutively shorter delay times (faster sweep rates). The current along such lines should reproduce the behaviour in Figure 4-12(a), while the behavour in Figure 4-12(b) should be reproduced by similar lines with a starting effective gate voltage of $V_{gs,eff}(\mathrm{V}_{ds} = 0) = \mathrm{V}_{gs} \exp(-(10 \text{ sec})/\tau)$.

This interpretation can be tested by making the following more detailed assumptions:

1. The ideal potential of the nanotube V_{nt} is related to the gate voltage V_{gs} by the gating efficiency α: $V_{nt,max} = \alpha V_{gs}$.

2. The potential of the nanotube V_{nt} is midway between the potentials of source and drain. Since the source is fixed at ground, $V_{nt} = V_{ds}/2$.

3. The gate voltage V_{gs} is held constant and the bias voltage V_{ds} is swept upward at a constant rate R [V/s], so that $V_{ds} = Rt$ where t is the time elapsed since the start of the sweep.

4. The effective nanotube potential $V_{nt,eff}$ varies with time according to the model of Figure 4-14(a) (*i.e.* an exponential decay with time constant τ), with an asymptotic value $V_{nt,eff}(t = \infty) = V_{nt,0}$ which is interpreted as a threshold voltage for charge tunneling into charge traps. That is, $V_{nt,eff} = V_{nt,0} + (V_{nt,max} - V_{nt,0})e^{-t/\tau}$.

5. The minimum current $I_{ds,min}(R)$ and voltage $V_{ds,min}(R)$ which define the right edge of the tier (before the rise to final saturation) are due to the passage of the

effective voltage through the conduction minimum for that gate voltage (*i.e.* $\alpha V_{gs,eff,min} = V_{nt,eff,min} = V_{ds,min}/2$).

With these assumptions, the nanotube potential can be used to find a linear relation

$$\begin{aligned}
(V_{nt,eff} - V_{nt,0}) &= (V_{nt,max} - V_{nt,0})e^{-t/\tau} \\
(V_{ds,min}/2 - V_{nt,0}) &= (\alpha V_{gs} - V_{nt,0})e^{-t/\tau} \\
(V_{ds,min} - 2V_{nt,0}) &= 2(\alpha V_{gs} - V_{nt,0})e^{-t/\tau} \\
\ln(V_{ds,min} - 2V_{nt,0}) &= \ln\left(2(\alpha V_{gs} - V_{nt,0})\right) - t/\tau
\end{aligned} \tag{4.1}$$

where the constants $V_{nt,0}$, α, and τ can be found by fitting the data of Figure 4-12(a). From this figure the local minimum of current at the right of each tier is found. The drain-source voltage corresponding to each minimum is used along with the sweep rated to calculate the time t from the beginning of the sweeps as

$$t = \left((40\ [\text{measurements}/\text{V}_{ds}])V_{ds,min} + 1\right)\left((D\ [\text{ms}]) + 5\ [\text{ms}]\right)\left(10^{-3}\ [\text{s}/\text{ms}]\right) \tag{4.2}$$

where D is the delay time between measurements in milliseconds. The constant 40 [measurements/V_{ds}] is the resolution of the bias sweep, and the constant 5 [ms] is the duration of each measurement. The results of the fitting are shown in Figure 4-15.

The parameters of the fit are $V_{nt,0} = 0.9$ [V], $\alpha = 0.52$, and $\tau = 6.4$ [s]. The asymptote of the effective graphene voltage, $V_{nt,0}$, has a large value compared to the thermal voltage spread $kT/e \approx 0.026$ [V]. Thus the thermal population and depopulation of charge traps is not possible, and instead the change must be transferred by controlling the nanotube voltage. The gating efficiency α, determined experimentally, is at least a reasonable value (recall that $0 \leq \alpha \leq 1$). While typical values for a bottom-gated device are $\alpha = 0.1$ to 0.2, larger values are observed for thinner oxide layers and for liquid dielectric gates (in both cases, larger gating capacitance). The value of τ is the most accurate and relevant of the parameters, as it indicates the timescale over which hysteresis will begin to dominate transport. Notably, it has the

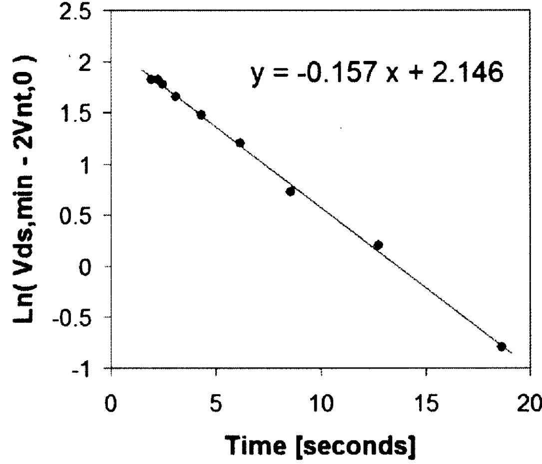


Figure 4-15: Fit of the data in Figure 4-12(a) to the model of Equation 4.1. The parameter $V_{nt,0}$ was adjusted to obtain the linear relation between $V_{ds,min}$ and t, with the best fit obtained for $V_{nt,0} = 0.9$ V. The intercept is used to calculate the gating efficiency $\alpha = \left(e^{\text{intercept}} + V_{nt,0}\right)/2V_{gs} = \left(e^{2.146} + 0.9\right)/(2 \times 10) = 0.52$. The slope is used to calculate the time constant $\tau = -1/(-0.157\ [1/\text{s}^{-1}]) = 6.4$ [s].

same value as the time constant found in Section 4.3.3, indicating that both effects likely have the same charge transfer origin.

Despite the simplifying assumptions made in this analysis, the quantitative results are reasonable and the qualitative interpretation provides a useful basis for designing experiments around the effect of hysteresis. When acquiring gate or bias sweeps, the most accurate results will be those for which the sweep rate is as high as possible. If slow measurements are required, the above analysis outlines how to convert from experimental gate voltages to effective gate voltages. And when taking multiple measurements at nearby voltages (such as when mapping the conductance as a function of gate and bias voltages by sweeping one voltage and stepping the other), it may be advisable to pause and zero the applied voltages for at least $5\tau \approx 30$ seconds between steps in order to counteract the charging that happens during the sweep. An even better approach would be to make zero-quiescent pulse measurements instead of DC sweeps.

The above model is also basic in that it assumes a linear resistance with a cutoff as the method for populating charge traps, when in reality an exponential tunneling or

some other more strongly varying function of effective voltage may be more accurate. It also ignores the effect of resistive heating of the device, which may or may not also affect the charge trap resistance. Indeed, this last effect was evoked in the qualitative explanation of the optical bump phenomenon in Section 4.3.3. Additionally, individual features of the conduction, such as the peaks attributed to impurities in Figure 4-13(d) may require special treatment to model accurately.

4.4 Conclusion

Electrical measurements at high drain-source bias were used to draw a number of useful conclusions about nanotube growth and transistor behaviour. The electrical cutting of carbon nanotubes was used to find the metal to semiconductor ratio M:S for two types of catalyst. For reliable production of nanotubes with an M:S ratio near the ideal ratio of 1:2, the bimetallic catalyst C00 (see Section 3.1.1) should be used. On the other hand, the single metal catalyst C02 was able to achieve selectivity for either metallic or semiconducting tubes by a factor of 2-4 (though not reliably). For both catalysts, however, there appears to be an aging effect where older catalyst produces more bundled and/or multiwall nanotubes. This is attributed to agglomeration of the alumina support material in the catalyst solution, and indicates the practical necessity of preparing fresh catalyst solutions within a few days of nanotube growth.

It was discovered that normal device fabrication leaves an organic residue on the surface of the chip and in contact with the nanotubes. This is thought to explain a number of interesting phenomena: 1) Anomalous peaks in the gate sweeps of metallic tubes are caused by impurity states or charge donation associated with residue attached to the nanotube. 2) Large hysteresis is attributed to charge leakage from the nanotube to nearby residue. 3) The optical bump (a negative differential conductance associated with the onset of optical phonon scattering) is also attributed to charge leakage from the nanotube to nearby residue. The time constant for this leakage was found to be 6 s. 4) The sweep rate dependence of the p-n junction-formation tier which is observed in the bias sweeps of metallic nanotubes was also

due to charge leakage, with the same time constant as the optical bump (6 s). From this it is concluded that measurements should be taken at high sweep rates and with long times between measurements in order to mitigate the effects of charge leakage onto the residue. While organic residue on a transistor is generally undesirable, it was found in the case of nanotubes to generate interesting behaviours (especially the metallic conduction peaks and optical bump) which might be exploited in future device designs.

Electrical conduction at the highest bias voltages (close to the failure point of the nanotube) also demonstrates several interesting features. The power dissipated at these high voltages and currents causes heating of the nanotube, which in turn is able to burn away organic residue in contact with the nanotube, or to weld together two crossing nanotubes. This results in an irreversible current increase, and this technique can also be applied to great effect in graphene devices. Impact ionization is caused by current injection from the contacts into the third subband of the nanotube, and is observed as a linear increase in the conduction which also exhibits decreased current noise. Observation of the onset of impact ionization is useful in predicting the imminent electrical cutting of the nanotube, and therefore is also useful in determining when to stop a high-current anneal so that the nanotube is not destroyed. Finally, the shape of the bias sweep, in conjunction with a gate sweep, can be used to differentiate between a bundle of two nanotubes and a double wall nanotube.

Chapter 5

Two-Terminal Graphene Devices

5.1 Introduction

Recently the Nano Materials and Electroncis group at MIT has have developed a new method to synthesize large area single- to few-layer graphene films by a chemical vapor deposition (CVD) method using substrates coated with nickel [39] (for similar methods from other groups, see [33, 59]). Afterward the Ni can be removed and the graphene films can be transferred to an insulating substrate for device fabrication [22]. In this chapter, a preliminary electrical characterization of these thin films of CVD graphene is performed using two-terminal devices.

Measurements are made of the conductivity of the graphene as modulated by a back gate at fixed and varying temperatures. From these measurements can be extracted the field-effect mobility μ, a quantity of great interest in the design of electronic devices. The modeling of the transport behaviour is discussed, with focus on the graphitic nature of the first-generation CVD graphene films. The measured device properties are compared to the literature for conventional exfoliated graphene devices, as an evaluation of the quality of the CVD graphene material.

Special acknowledgement is given to Joel Yang, who provided instruction in the use of the fabrication equipment and who assisted in the fabrication of the devices studied in this chapter.

5.2 Device Fabrication

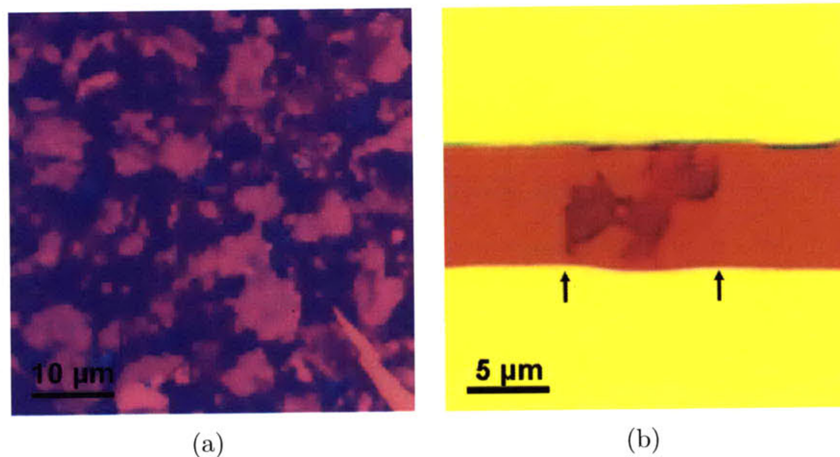
Arrays of two-terminal back-gated devices were fabricated using CVD graphene as the channel material by the following procedures. First, the CVD graphene was grown (for more details, see Section 3.2.2.1) and transferred (Section 3.2.2.3) to a SiO_2/Si substrate (300 nm SiO_2) following [22, 39]. Figure 5-1(a) shows the optical image of a transferred film on the SiO_2/Si substrate. Due to the optical interference effect modulated by the graphene layers on the SiO_2 surface, one- to few-layer graphene flakes can be recognized under the optical microscope [37, 38]. Each color corresponds to a different thickness of the graphene film. The thinnest regions are single- or bi-layer graphene and appear light pink under the optical microscope, while the thickest regions appear light blue and consist of approximately 19 layers of graphene. The purple regions are of intermediate thickness. The average thickness of the graphene film is 6.9 $\pm$ 1.3 nm as determined by atomic force microscopy (AFM). One large chip containing this transferred graphene was cleaved into three pieces (labeled as chips A01-8C, A01-8D1, and A01-8D2) for further processing. Thus, for all devices subsequently discussed, the graphene material is essentially identical because it came from the same growth and transfer steps.

Device fabrication continues as described in Section 3.4.3 by creating an etch mask of lines on top of the graphene designed to be 2, 4, 6, and 8 μm wide. These lines are produced by optical lithography using photoresist AZ5214E by either one of two methods: 1) an image reversal lithography process which leaves lines of resist on the graphene as the etch mask (used for chip A01-8D1), or 2) a positive lithography process followed by metal evaporation (5 nm Cr / 30 nm Au for chip A01-8D2 or 30 nm Ni for chip A01-8C) and liftoff to leave lines of metal on the graphene as the etch mask. After the lithography step, the unprotected graphene region is then etched by oxygen plasma in the PlasmaTherm in the NSL (Section 3.3.5) with the following etch conditions: 8 sccm O_2 with 16 sccm He under 10 mTorr pressure and 200 V bias, using 100 W power.

Following the etch step, the etch mask is removed by acetone rinse (photoresist

mask, chip A01-8D1), by chromium wet etch (Cyantek CR-7, chip A01-8D2), or by nickel wet etch (9% dilution of HCl in H_2O, chip A01-8C) to expose the stripes of graphene. It is worth noting that the wet etch for chromium removal was observed to be more effective because the presence of graphene enhances the etch rate by about 70 times in our experiments as determined by time-lapse optical inspection (see also [41], with experimental results in Section 3.5.1.2). The choice of etch mask affects some of the properties of the resulting devices, but not others, as discussed below.

Next, contact pads are deposited onto the graphene lines. A layer of AZ5214E photoresist is spun onto the chip and patterned with rectangular openings of 100 x 150 μm^2 which overlap the graphene lines and are designed with distances between openings of 3, 5, 10, and 20 μm. Metal is then thermally evaporated (5 nm Cr / 30 nm Au) onto the chip, and liftoff of the resist leaves rectangular metal contact pads overlaid on top of the graphene lines. Pairs of pads connected by a graphene line form the source and drain of a two-terminal device, while the doped Si substrate underneath the oxide layer provides a back gate. An optical image of the channel region of such a field-effect transistor-like device is shown in Figure 5-1(b).



(a) (b)

Figure 5-1: (a) Optical image of CVD Graphene film as transferred to a SiO_2/Si substrate. Graphene thickness domains appear as regions of uniform color. The thickness decreases from blue to purple to pink, with the pink regions being one or two monolayers. (b) Optical image of a two-terminal device. The arrows serve as guides to the eye showing the sides of the device. The conduction channel is composed of a network of monolayer and multilayer thickness regions. The contrast of the single layer regions is reduced from that in (a) due to increased magnification.

5.3 I-V Measurements

5.3.1 Measurement Procedure

Measurements were made of I_{ds}-V_{ds} (bias sweeps) and I_{ds}-V_{gs} (gate sweeps). The bias sweeps are generally linear up to at least 1 volt V_{ds}, showing simple ohmic behaviour with a resistance which was dependent on V_{gs}. The gate sweeps were made from -40 to +40 V gate-source bias V_{gs} and back again with 100 mV constant drain-source bias V_{ds} and show a conductance minimum at a gate voltage V_0 identified as the Dirac point of graphene, as well as a sub-linear slope on either side identified with p-type ($V_{gs} < V_0$) and n-type ($V_{gs} > V_0$) conduction, respectively.

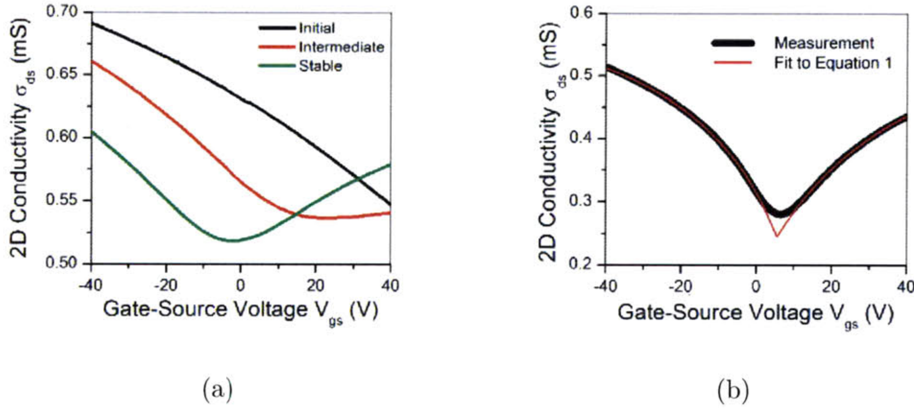
The devices were annealed before carrying out electrical measurements. Two methods were used here: either thermal annealing at 200 °C for 15 hours under vacuum (<10^{-1} Torr) or by electrical current annealing using high drain-source bias (9-12 V_{ds}) under vacuum (<10^{-5} Torr) in a different chamber where there is no heating stage [13]. For both methods, the annealing step resulted in a shift of the Dirac point to near $V_{gs} = 0$ (Figure 5-2(a)). Current has been converted to sheet conductivity by the relation

$$\sigma_{ds} = (I_{ds}/V_{ds})(L/W) \tag{5.1}$$

where L and W are the length and width of the graphene channel, respectively, as determined from optical and AFM measurements. We note that during the high drain-source bias annealing, current densities of up to 3.40 x 10^7 A/cm^2 were observed. This value, within an order of magnitude of values obtained for exfoliated graphite, serves as the first indicator of the highly graphitic and stable quality of CVD graphene films [2, 13].

5.4 Analysis Models

The gate voltage dependent conductivity of the CVD graphene devices studied here, having channels composed of regions of differing thickness, can be expected to exhibit



(a) (b)

Figure 5-2: (a) Typical gate sweeps taken before annealing (top curve at y-axis, black), between successive anneals when the device is partially cleaned (middle curve at y-axis, red), and after complete cleaning (bottom curve at y-axis, green). Annealing shifts the Dirac point to near $V_{gs} = 0$. (b) Another gate sweep which shows even more clearly the effect of the residual resistivity, which makes the conductivity sublinear. Measured data is shown by the black line, and the best fit using Equation D.1a (in Appendix D) is shown by the red line. Fit parameters used are: $V_0 =$ -5.52 V, $\sigma_{bg} =$ 0.245 mS, $\mu_n = 844$ cm^2/Vs, $\mu_p = 1275$ cm^2/Vs, $\rho_r = 2.24$ kΩ.

some combination of behaviours ranging from that of single-layer graphene to that of bulk graphite. Indeed, as Figure 5-2 shows, the measurements show a V-shaped conduction characteristic of single-layer graphene, but also a very large minimum conductivity, characteristic of the more metallic graphite. We examine each of these behaviours in turn before considering their combination, which reveals that the conductivity can take the same functional form in each of these very differnet cases.

5.4.1 Single-Layer Graphene

To begin, the behaviour of single-layer graphene has been reported by many groups [2, 17, 60, 61, 62, 63, 9], and theoretical studies [64, 65, 66, 67, 32, 68, 69, 70] have predicted charged impurity scattering in graphene to produce a conductivity variation of the form

$$\sigma_{ds}(V) = \sigma_{res} + C_g \mu_k |V_{gs} - V_0| \tag{5.2}$$

where V_0 is the gate voltage corresponding to the Dirac point, μ_k is the field-effect mobility (Appendix C) for electrons (k = n, $V_{gs} > V_0$) or holes (k = p, $V_{gs} < V_0$), and C_g is the gate capacitance of the device ($C_g = 1.15 \times 10^{-8}$ F/cm^2 for our 300 nm SiO_2 dielectric in the absence of quantum capacitance, see Appendix B for a more detailed discussion), and σ_{bg} is the so-called background conductivity, which is the minimum conductivity located at $V_{gs} = V_0$. This equation gives a linear conductivity around the Dirac point.

There are several necessary additions to the above description. First, there are gate voltage-independent scattering mechanisms, such as short-range (lattice defect) scattering and phonon scattering. These are included as a resistivity in series with the channel. And second, a contact resistance is also expected to be in series with the channel. Because two-terminal measurements cannot distinguish between these last two contributions, they are lumped together into the so-called residual resistivity term ρ_r (residual in the sense that it is the resistance contribution that is "left over" after the linear long-range electrostatic scattering is accounted for). Thus the full conductivity model for single-layer graphene is given by:

$$\sigma_{ds}(V) = \left[\left(\sigma_{bg} + C_g\mu_k \left|V_{gs} - V_0\right|\right)^{-1} + \rho_r\right]^{-1} \tag{5.3}$$

The addtional resistivity term ρ_r causes the linear conductivity of Equation 5.2 to become sublinear, a behaviour which is often significant in our devices (see Figure 5-2(b)). It is assumed that ρ_r is independent of V_{gs}. We note that for single-layer graphene it has been shown that, at low charge densitites, the contact resistance may vary with gate voltage due to modification of the widths of regions of charge induced by the contacts [71]. However, the devices considered in this investigation are composed primarily of multilayer regions and are not subject to charge depletion (see Section 5.4.2). This may be reflected in the good fittings obtained with the data in Figure 5-2(b).

5.4.2 Many-Layer Graphene

The electrical conductivity of thick graphene regions is here considered. In recent studies of thin exfoliated graphite samples [72, 73], transport was found to be well described by a simple two-band (STB) model, which is often adopted for graphite [74]. It is expected that CVD graphene, with an average thickness only a factor of two less than the thinnest samples in references [72, 73], can also be analyzed using a STB model. The premise of this method is that the interaction between the graphite layers causes the dispersion relation to become parabolic (as compared to the linear dispersion in single-layer graphene (dotted line in Figure 5-3(a)), and causes the valence and conduction bands to overlap by an energy Δ (Figure 5-3(b)). In the limit of complete screening (screening length $\lambda_s \ll d$, the graphite thickness), equation (1) of reference [72] can be integrated to obtain a functional form for the normalized conductivity (to first order in $|V_{gs} - V_0|$):

$$\frac{\sigma_{ds}(V_{gs})}{\sigma_{ds}(V_0)} = 1 + \frac{1}{d}\left[\left(\beta + \frac{1}{E_0}\right)\frac{\kappa\lambda_s^2}{t}\right]|V_{gs} - V_0| \tag{5.4}$$

where $\beta = 4.8\ \text{eV}^{-1}$ gives the energy dependence of the density of states normalized to the minimum density of states, while $E_0 = \Delta/2 = 0.017$ eV is half the band overlap (determined from the temperature dependence discussed in Section 5.7), $\kappa = 3.9$ is the relative dielectric constant of the oxide, and t = 300 nm is the thickness of the oxide.

Like the equation from which it is derived, Equation 5.4 is valid for graphene with Fermi energies in the range $|E_F| < 300$ meV, well within the range of values achieved in this work ($|E_F|$~200 meV for a gate voltage of $\pm$40 V). The value of λ_s = 0.4 nm is used for consistency with [72], though values of up to 1.2 nm have been reported for top-gated devices [75]. We note, however, that the condition $d \geq \lambda_s$ is sufficient to justify Equation 5.4 to better than 4% for any λ_s up to 1.2 nm. This is acceptable, since our graphene thicknesses, as determined by AFM, are in general much larger, and for $d < 1.2$ nm the graphene must be analyzed as single-layer or bi-layer graphene, since the STB model is no longer appropriate.

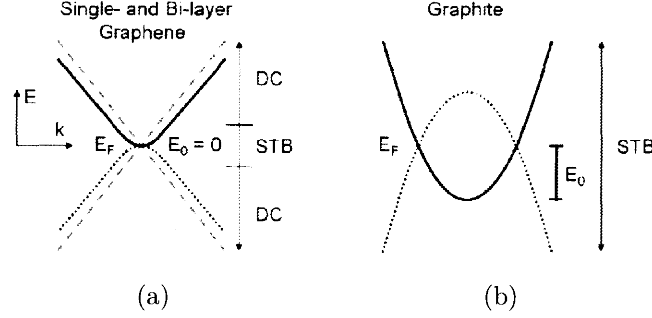


Figure 5-3: Energy band diagrams showing valence bands (dotted lines) and conduction bands (solid lines) for bi-layer graphene (a) and graphite using the simple two-band model (b). The linear dispersion of single-layer graphene is shown for reference as a dashed grey line in (a). Band overlaps ($\Delta = 2E_0$) and Fermi levels (E_F) are indicated. The simple two-band (STB) model is applicable at all energies for graphite, while for bi-layer graphene it is applicable only to energies near the Fermi energy. At energies far from the Fermi energy, the dispersion $E(\vec{k})$ behaves like a Dirac cone (DC) as for single-layer graphene.

The term in brackets in Equation 5.4 is a constant, and using the quantities quoted above, it may be evaluated as $M_0 = 0.132$ nm/V. The term $\sigma_{ds}(V_0)$ can be identified as the background conductivity σ_{bg}. Finally, since the contact resistance and scattering will also affect the many-layer graphene conduction, it is appropriate to include a residual resistivity term ρ_r, so that the full conductivity for two-terminal many-layer graphene devices is given by

$$\sigma_{ds}(V) = \left[\left(\sigma_{bg} + \sigma_{bg} \frac{M_0}{d} \left| V_{gs} - V_0 \right| \right)^{-1} + \rho_r \right]^{-1}. \tag{5.5}$$

5.4.3 Single-Layer and Many-Layer Model Correspondence

It turns out that the expressions for the conductivity for single-layer graphene (Equation 5.2) and many-layer graphene (Equation 5.4) are functionally equivalent under the identification

$$C_g \mu_k = \frac{\sigma_{bg} M_0}{d} \tag{5.6}$$

The result is that the conduction of the graphene channel in the absence of residual scattering obeys the same functional form whether composed of a single layer or of

many layers, though the interpretation of the fitting parameter σ_{bg} differs. Namely, in many-layer graphene the background conductivity may be thought of as intrinsic to the graphene, primarily due to metallic-like conduction in the upper layers which are screened from the gate by the lower layers [76], while for single-layer graphene the causes are mostly extrinsic, as noted above.

The behaviour of bi-layer and few-layer graphene will fall somewhere between the range of that of single-layer graphene and many-layer graphene. In Figure 5-3(a), the band structure of bi-layer graphene shows a zero gap ($\Delta = 0$), which at modest energies $|E| \leq k_B T$ will behave very similar to the STB model because the dispersion relation can be approximated by a parabola in this range. For energies beyond this range, the bands are best approximated by a Dirac cone, and the behaviour of single-layer graphene is qualitatively recovered. This crossover behaviour is clearly seen in figure 4 of Reference [9]. Thus we expect that Equation 5.2, and therefore Equation 5.3, are applicable to bi-layer and few-layer graphene also, though the crossover between the regimes may confuse the analysis. This crossover region of few-layer graphene is an interesting regime for future theoretical consideration.

5.4.4 Two Equivalent Analytic Forms

It should be noted that in the preceding analyses it was assumed in both cases that the residual resistivity acts upon the entire ideal conductivity of the graphene channel. However, if the main contribution to ρ_r is not contact resistance but rather is a mechanism which only applies to the gate-modulated portion of the conductivity, then the expressions given above must be altered. Specifically,

$$\text{Equation 5.3} \rightarrow \qquad \sigma_{ds}(V) = \sigma_{bg} + \left[\left(C_g \mu_k \left| V_{gs} - V_0 \right| \right)^{-1} + \rho_r \right]^{-1} \tag{5.7a}$$

$$\text{Equation 5.5} \rightarrow \qquad \sigma_{ds}(V) = \sigma_{bg} + \left[\left(\sigma_{bg} \frac{M_0}{d} \left| V_{gs} - V_0 \right| \right)^{-1} + \rho_r \right]^{-1} \tag{5.7b}$$

where the quantities have basically the same physical interpretation as mentioned above.

It turns out that the two ways of applying ρ_r are actually *equivalent* under the proper transformation of the parameters σ_{bg}, μ_k, and ρ_r. This situation is considered in detail in Appendix D, where Equation 5.7 corresponds to the so-called "Model 1", while Equation 5.3 and Equation 5.5 correspond to the so-called "Model 2". The relevance of this lies in the fact that either functional form may be used in a numerical fitting procedure to extract the parameters σ_{bg}, μ_k, and ρ_r for a given device, with optional post-conversion of the parameters between the two models depending on which interpretation is preferred. Justification of this in an experimental context is given in Section 5.6.1.

5.4.5 Model Choice

With freedom to choose either Model 1 or Model 2 (Appendix D) for extraction of fitting parameters from the data, it was decided that Model 1 should be used due to its simpler analytic form, which led to more reliable numerical fits (see Section 5.6.1).

Model 1 and Model 2, however, were not the only ones considered for use in fitting the gate voltage sweeps. What follows is a brief discussion of some of these other models (presented in Equation 5.8), and why they were not chosen.

$$\text{Model 3:} \quad \sigma_{ds}(V_{gs}) = \sigma_{bg} + \left[\left(\mu_k\left[(C_g\left|V_{gs}-V_0\right|)^2 + n_0^2\right]^{1/2}\right)^{-1} + \rho_r\right]^{-1} \tag{5.8a}$$

$$\text{Model 4:} \quad \sigma_{ds}(V_{gs}) = \sigma_{bg} + \left[(C_g\mu\left|V_{gs}-V_0\right|)^{-1} + \rho_{r,k}\right]^{-1} \tag{5.8b}$$

Model 3 is similar to Model 1, but includes an additional charge density n_0 identified as the induced charge present in charge puddles similar to the same term in [58] and n^* in [32] (though the latter is a more accurate treatment). The fits produced with Model 3 can often perfectly fit the data. However, at the beginning of the analysis it was suggested that the use of too many fitting parameters would dilute the results. In hindsight, it would be preferable to use this form of the fitting function because it more accurately represents the physics of graphene transport, and eliminates the need for truncation of data around the Dirac point.

Model 4 is also similar to Model 1, but considers the n-type and p-type conduction to have identical mobilities, but possibly different residual resistivities. This is physically reasonable, since electrons and holes are symmetric in graphene, and the scattering mechanisms which differentiate between charge carriers are not significant, while at the same time there are reasonable explanations for resistivity differences, namely the doping of graphene at metallic contacts (an extension of Fermi level pinning to the graphene system with linear bands) which can introduce additional resistance as charge inversions are traversed. It also satisfies the observation that in actual conductivity sweeps the asymptotic saturation value at high gate voltages is different for electrons and holes (the other models cannot do this, since ρ_r is inversely proportional to this saturation value, and singly-valued). The complication with this model occurs when one tries to consider the analogue of the Model 1/Model 2 correspondence detailed in Appendix D, which introduces a discontinuity at the Dirac point unless additional parameters are introduced. Thus, the circuit interpretation for this model requires further work.

Variations on the four models discussed so far can also be obtained by removal of parameters to simplify the fitting. For example, to fit only the n-type or the p-type conduction (a so-called one-sided fitting), the opposite μ_k or $\rho_{r,k}$ may be removed and the domain restricted to end at the conductivity minimum. This has proven useful where only one side of the conductivity curve appears within the gate voltage measurement range, or when half of the sweep is malformed for whatever reason (though one may also consider reflecting the acceptable region around the conductivity minimum to produce a well-formed conductivity curve). When considering that to each of these may be applied the same transformations which convert Model 1 in to Models 2, 3, and 4 (that is, considering the residual resistivity to act on the background conductivity, the introduction of a smoothing term for fitting the region around the Dirac point, and alternating which parameter takes on different values for different charge carriers), there are a large number of possible models to choose from.

Yet it remains that Model 1 has the simplest, relatively complete explanation of the gate sweep behaviour, with a straightforward interpretation in terms of a circuit

diagram, and therefore was chosen as the model for this analysis.

5.5 Analysis Procedure

The goal of the analysis was to apply the analytic Model 1 the the experimentally obtained gate sweeps in order to obtain the device parameters σ_{bg}, μ_k, and ρ_r. This was accomplished by the following method.

5.5.1 Data Selection

Gate sweeps were taken of a total of 288 graphene line devices on three chips (comprising all of the conducting devices). Of these, 126 were selected for full analysis. The following criteria were used for this selection:

1. **Optical Inspection.** Images of the chips were taken on an optical microscope and assembled into a composite image of the chip. The location of each device, for which a gate sweep was acquired, was found in an image, and each device that did not show a standard appearance was discarded. Examples of nonstandard appearance are: extra or missing or nonrectangular graphene, damaged or offset metal pads, photoresist residue or metal islands on top of the graphene channel. For the devices which are acceptable, the conversion between optical pixels and distance was calibrated from the dimensions of the metal pad array. This calibration is in turn used to measure the width and length of the graphene channel for each designed line width and gap length. These values are then used as the width W and length L for calculation of the conductivity for each device according to Equation 5.1.

2. **Gate Sweep Noise.** The gate sweeps were then qualitatively categorized based on both the type of noise present (Random, Shot, Step) and its magnitude in comparison to the modulation due to the gate (Nominal, Low, Medium, High). Sweeps showing step noise, high amplitude random noise, or medium density shot noise were rejected. Sweeps containing nominal to medium random noise

and a low density of shot noise were provisionally accepted as likely to produce a useful fitting result.

3. **Hysteresis.** Hysteresis was largely absent due to annealing and measurement in vacuum. Gate sweeps exhibiting hysteresis of 10% or more of the gate voltage range ($\geq$8 V for -40 to +40 V measurements) were rejected. Although some of these rejected gate sweeps looked like they would be amenable to correction by a horizontal averaging process, the algorithm for this was not implemented in the interest of time and in the face of doubts about how appropriate and reliable such a correction would be.

4. **P-Type and N-Type Conduction.** Gate sweeps were discarded which did not show both p-type and n-type conduction at least into the linear regime. It is preferable to observe conduction into the sublinear regime, but often this is possible only for one type of carrier due to the nonzero Dirac point voltage V_0.

5. **Other Abnormalities.** Various other abnormalities in the gate sweeps were taken as cause for rejection, including lack of modulation by the gate voltage, shorted channels, and gate leakage.

6. **Quality of Model Fitting.** Most gate sweeps which survived to this stage could be easily fit to Equation 5.3. Those for which a fit would not converge, usually due to noise or a broad conductivity minimum, were rejected. Additionally, those which were provisionally accepted on the grounds of marginal p-type or n-type conduction linearity, and which did not show convincing linearity in the resulting fit, were also rejected. If a fitting would not converge due to different apparent saturation conductivities for electrons and holes, the section which saturates too early was removed from the fitting input as due to contact related effects [77].

5.5.2 Model Fitting Technique

Model fitting was carried out using custom Matlab scripts and functions. This analysis architecture was designed to process many devices in a sequential and automated manner. Useful functionality includes reading in and conditioning arbitrary numbers of files (or subgroups of files) within a directory, fast switching between upwards of two dozen fitting functions, automatic estimation of initial conditions for each fitting function, iterative fitting to abritrary tolerance using user-selected algorithms, and automatic graph preparation and output saving. Each of these functionalities was abstracted to allow quick and easy restructuring of the code to handle any arbitrary applications.

For the two-terminal graphene devices considered here, the fitting proceeds as follows. First, the data is loaded and $\sigma(V_{gs})$ is computed. Then the data for the upward sweep is taken (and the downward sweep is discarded). At this point, the standard deviation of the data is computed by using a 12-order polynomial fit as a baseline (found to be appropriate for the range of forms of the conductivity curve). Next, limits of model applicability are applied to remove portions of the data that are not incorporated into the model. These include regions around the Dirac point (where the charge impurity concentration n_0 induces charge in the graphene which is not accounted for in the ideal linear model considered here) and regions near the beginning of the data set (which may contain small errors due to hysteresis, if present). The regions taken are specific to each device and determined by hand in order to produce an acceptable fit, through multiple fitting iterations. Finally, the data is automatically analyzed to determine appropriate initial conditions and uncertainty for the fitting algorithm.

The uncertainty must be estimated, not calculated, since independent measurements to obtain the uncertainty were not performed for each device at the time the gate sweeps were acquired. The uncertainty in conductivity can be extracted from a conductivity curve under the assumption that the uncertainty is identical for each data point. In this case, if one knows the true conductivity curve, then this may

be subtracted from the data, resulting in normally distributed residuals from which the standard deviation may be taken as the uncertainty in the data. While the true conductivity curve is not known, it may be approximated by some "smooth" function, which varies on a scale much larger than the spacing between data points. For this purpose, a polynomial form was chosen, and order 12 was selected as the best compromise between fitting accuracy and complexity.

The fitting itself uses a Levenberg-Marquardt algorithm [78] with numerical derivatives, set to terminate when χ^2 varies by less than 0.01 between steps. Step size is 1/1000 of the initial values, and $\lambda = 1/1000$. This fitting is iterated up to 15 times to refine the result, with a target maximum normalized variation of parameters between iterations of 10^{-10}. The output of the fitting algorithm contains both the model parameters and their uncertainties.

The mobility is also calculated directly from the slope of the conductivity curve for comparison to the fit parameters, and because this is the quantity which comes into play in the performance of any electronic device and therefore is the mobility value most often presented in the literature. Due to the density of data points and the uncertainty in each data point, calculating the slope of a conductivity curve for use in Equation C.2 by a difference method is impractical due to error amplification. As for the case of calculation of the uncertainty in the data, a smoothing function can be employed to enable the calculation. Again, a 12-order polynomial was fit to each curve, then analytically differentiated, and the maximum and minimum were found, corresponding to the largest positive and negative slopes (n- and p-type conduction), respectively. Because the edges of a polynomial are not well fit, the outer 10 points were excluded from this evaluation. This is not considered an issue since the conductivity curves, for the most part, become sublinear before reaching the ends of the gate voltage range. Note that other acceptable solutions would be to downsample the data until the ratio of uncertainty to spacing is more acceptable, or to extrapolate the data beyond the edges of the graph to allow a more convergent fitting at the ends.

5.6 Fitting Results

Because the graphene device channels are composed of multiple regions of different thickness, the fitting parameters obtained by application of Equation 5.7 to measurements are understood as average values for the channel. Additionally, since the actual method by which ρ_r should be incorporated is unknown, and may indeed correspond to some combination of Model 1 and Model 2 behaviour, the fitting parameters are presented in both their Model 1 and Model 2 forms, with the understanding that the true behaviour lies somewhere between these extremes.

5.6.1 Model Correspondence

The correspondence between Model 1 and Model 2 described in Appendix D was used as a check of the validity of the method of curve fitting described in Section 5.5. Fitting was performed on 13 gate sweeps first with Model 1 and then with Model 2. The fittings were distinguished only by the use of different model-dependent functions as arguments to the Levenberg-Marquardt fitting algorithm [78]. It was found that Model 1 converged more readily than Model 2; five gate sweeps did not converge under Model 2, but all gate sweeps converged under Model 1.

The non-convergence of Model 2 occurred mostly for gate sweeps which had higher relative uncertainties when fit with Model 1 (Table 5.1). It is interesting to note that the dominant dependence was found to be on the *relative* uncertainty of parameters, not on the actual values of the parameters or the model-independent conversion factor γ or even the uncertainty of the data points δ_{dat} in a particular measurement. Thus the difficulty of fitting a given gate sweep is more readily mitigated by Model 1 than Model 2. If the parameters obtained by fitting to one model are identical to that predicted by conversion of parameters obtained by fitting to the other model according to Table D.1, then it is clear that Model 1 should be used to fit the data, and these values converted as necessary.

To demonstrate that this conditional is satisfied, the fitting parameters were compared for the seven gate sweeps in which fitting converged for both models. The

	1 & 2	1 only
σ_{bg} [mS]	0.72 ± 0.57	0.92 ± 0.41
V_0 [V]	-7.9 ± 2.7	-11 ± 18
μ_n $[\frac{\text{cm}^2}{Vs}]$	628 ± 504	243 ± 96
μ_p $[\frac{\text{cm}^2}{Vs}]$	398 ± 257	121 ± 32
ρ_r [kΩ]	1.6 ± 1.0	1.1 ± 1.5
γ [#]	1.78 ± 0.52	1.64 ± 0.58
δ_{dat} [μS]	0.64 ± 0.47	0.29 ± 0.39

[%]	1 & 2	1 only
$\delta(\sigma_{bg})/\sigma_{bg}$	0.08 ± 0.05	0.29 ± 0.32
$\delta(V_0)\ /V_0$	0.9 ± 0.6	4.6 ± 4.0
$\delta(\mu_n)\ /\mu_n$	0.9 ± 0.8	2.7 ± 1.0
$\delta(\mu_p)\ /\mu_p$	1.0 ± 0.9	14 ± 10
$\delta(\rho_r)\ /\rho_r$	2.1 ± 1.6	58 ± 70

Table 5.1: Average uncertainties (left) and average relative uncertainties (right) in Model 1 fit parameters when fitting to Model 2 converges (1 & 2, 7 devices) and diverges (1 only, 5 devices). Note that one device is excluded which gives the same parameters in Model 2 as in Model 1. Higher relative uncertainties in Model 1 parameters correlate with difficulty in fitting to Model 2.

parameters from Model 1 were used to compute the expected values for the parameters in Model 2, and these values were compared to the actual fitting results for Model 2. Four of the seven gate sweeps had identical parameters ($<10^{-5}$ variation). The remaining three gate sweeps showed variation of parameters of 1-5%. The uncertainties in the parameters were also compared in a similar manner. It was found that conversion of uncertainties from Model 1 to Model 2 overestimated the uncertainty by a factor of 1-13, with an average overestimation factor of 3.3. While this factor is significant, the uncertainties still remain small compared to the parameter values (1-3%, roughly comparable to the values seen for Model 1 parameters in Table 5.1).

To judge whether this uncertainty is acceptable, fitting was performed for a single gate sweep according to Model 1 under a restricted range of gate voltages. It was observed that the resulting variations in the fitting parameters were at least as large as the uncertainties in the fitting parameters.

The conclusion is that it is unimportant whether model parameters are obtained from direct fitting to that model or from conversion of the parameters of a different model. For the gate sweeps under consideration in this thesis, the uncertainty in parameters due to the cropping of the data are larger than the uncertainties from the fitting algorithm. Because Model 1 results in more robust fits, all gate sweeps are analyzed using this model in the fitting algorithm.

5.6.2 Fitting Parameter Distributions

Gate sweeps from a total of 126 devices were fit, and a typical result is shown in Figure 5-2(b) (black and red curve for data and fit, respectively). The fitting parameters for these devices are shown in Figure 5-4 and Figure 5-5 and the transconductance field effect mobilities are shown in Figure 5-6 as statistical distributions, and a summary of the distribution parameters is given in Table 5.2. The region near the Dirac point is excluded from the fit, because the model in Equation 5.3 does not account for the increased scattering due to decreased screening or the effects of charge puddle percolation [63, 79].

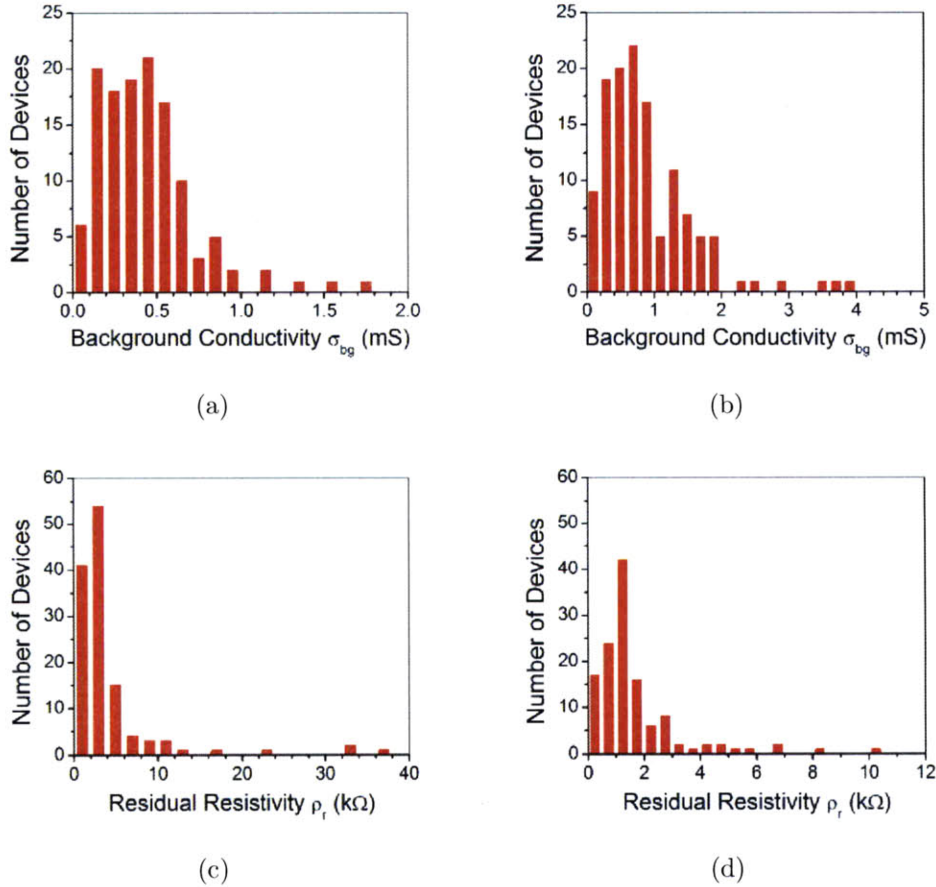


Figure 5-4: Histogram of fitting parameters σ_{res} and ρ_r for 126 graphene line devices (Equation D.1). (a),(c) Model 1 parameters. (b),(d) Model 2 parameters, as calculated from the Model 1 parameters according to Table D.1 in Appendix D. Histograms for the other parameters appear in Figure 5-5. The mean and standard deviations are summarized in Table 5.2.

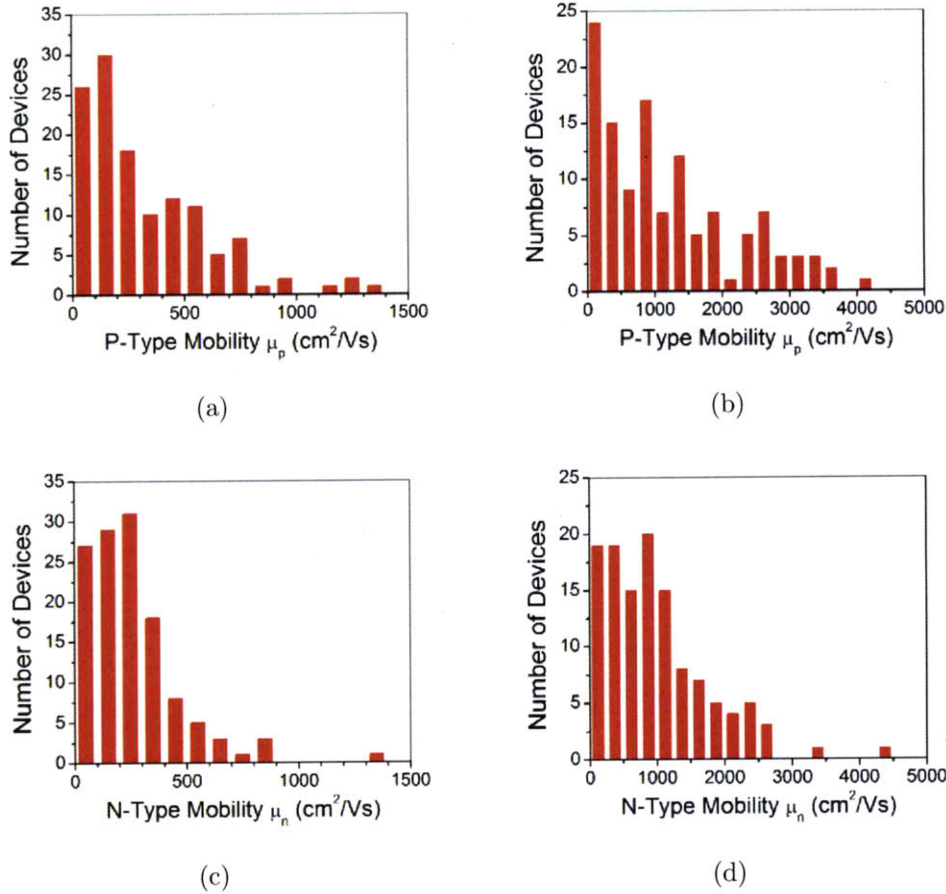


Figure 5-5: Histogram of fitting parameters μ_p and μ_n for 126 graphene line devices (Equation D.1). (a),(c) Model 1 parameters. (b),(d) Model 2 parameters, as calculated from the Model 1 parameters according to Table D.1 in Appendix D. Histograms for the other parameters appear in Figure 5-4. The mean and standard deviation are summarized in Table 5.2.

The background conductivity σ_{bg} is distributed with a mean value of 0.435-0.906 mS and a standard deviation of 0.288-0.705 mS (Figure 5-4(a) and Figure 5-4(b), where the given range corresponds to Model 1 - Model 2 parameter values). We consider the two contributions to this value. First, contact-induced states are expected to be relevant in devices with low aspect ratios (L/W $\leq$ 1) [71, 80, 81]. This is the case for most of the considered devices (aspect ratios range from 0.42 to 6.9 with an average of 1.7, and 41% of devices have an aspect ratio below 1.0). The contact-induced states set a lower bound for σ_{bg} of $4e^2/\pi h = 0.0493$ mS [80]. However, this is insufficient to account for the observed σ_{bg}. The proposed resolution of this is that

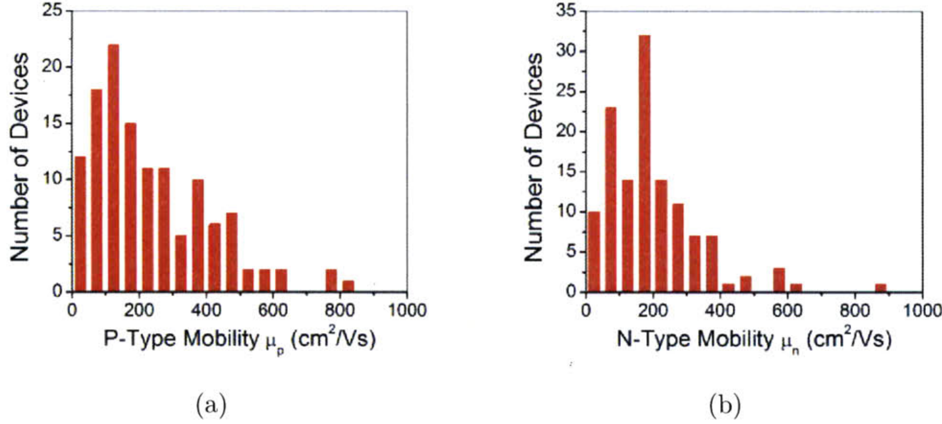


Figure 5-6: Histograms of mobilities μ_p and μ_n calculated from the transconductance for 126 graphene line devices. (a) P-type mobility. (b) N-type mobility. The mean and standard deviation are summarized in Table 5.2.

Parameters	σ_{bg} [mS]	ρ_r [kΩ]	μ_p [cm^2/Vs]	μ_n [cm^2/Vs]
Model 1	0.435 $\pm$ 0.288	4.00 $\pm$ 5.75	-329 $\pm$ 285	261 $\pm$ 200
Model 2	0.906 $\pm$ 0.705	1.65 $\pm$ 1.59	-1440 $\pm$ 1480	1160 $\pm$ 1210
γ	σ_{min} [mS]	V_0 [V]	$\mu_{p,slope}$ [cm^2/Vs]	$\mu_{n,slope}$ [cm^2/Vs]
2.09 $\pm$ 0.85	0.0184 $\pm$ 0.0143	8.30 $\pm$ 7.92	-233 $\pm$ 173	198 $\pm$ 138

Table 5.2: Summary of device fitting parameters and uncertainties for Model 1 and Model 2 shown in Figure 5-4 and Figure 5-5.

σ_{bg} is due mostly to transport through thick graphene, as described in Section 5.4.3 and Section 5.6.6.

The residual resistivity ρ_r is distributed with a mean value of 4.00-1.65 kΩ and a standard deviation of 5.75-1.59 kΩ (Figure 5-4(c) and Figure 5-4(d)). A question of interest is how much of this value is due to the contact resistivity and how much is due to scattering within the channel. The observed ρ_r is much greater than the expected acoustic phonon scattering resistivity (~30 Ω at T = 300 K), and at high gate voltages long-range charge scatterers are screened, so it is expected that the additional resistivity in our data is due primarily to contact resistance [71, 82], SiO_2 phonon scattering [10, 83] and short-range scattering by defects in the graphene [69].

Typical values for SiO_2 scattering resistivity are relatively low (30-400 Ω at T = 300 K). Typical contact resistances in the literature are 0.5-1 kΩ m, and will be process-dependent. The magnitude of short-range scattering may vary widely

between graphene samples from various sources, and different fabrication techniques may preferentially produce specific lattice defects at specific densities. For CVD graphene, if the single crystalline graphene domain size is smaller than the device dimension (as is certainly the case here), it is possible that defects at the domain boundary interfaces will contribute to increased short-range scattering over that found in exfoliated graphene devices (200-400 Ω at T = 300 K) [69]. The nonzero D-band in the Raman spectra of CVD graphene (see Figure 3 in Reference [39]) suggests that short-range scattering may be even more important in this material. Therefore we conclude the majority of the scattering is probably due to short range defect scattering and contact resistance.

The average p-type and n-type field-effect mobilities are 329-1440 and 261-1160 cm^2/Vs respectively (Figure 5-5). These average mobilities are below the mobilities of top-gated devices fabricated using the similarly grown CVD graphene (~2000 cm^2/Vs) [84]. The current measurements show a larger background conductivity and lower mobility because the films are on average thicker than in [84], being from an earlier stage of research into the growing of graphene. Compared to the high mobilities reported for exfoliated graphene devices on SiO_2 (>20,000 cm^2/Vs) [10, 85], there is significant room for improvement of the material quality of CVD graphene.

5.6.3 Fitting Parameter Correlation

While histograms are useful for viewing distributions of a single variable, they fail at presenting the covariance of pairs of variables, which may provide insight into the appropriateness of a given model. A useful characterization in this case is the correlation. The Pearson product-moment correlation coefficient ρ_{XY} of two variables X and Y is defined in terms of the covariance σ_{XY} and the standard deviations of the two variables σ_x and σ_Y as

$$\rho_{XY} = \frac{\sigma_{XY}}{\sigma_X \sigma_Y} = \frac{\langle \left(X - \bar{X}\right)\left(Y - \bar{Y}\right) \rangle}{\langle X - \bar{X} \rangle \langle Y - \bar{Y} \rangle}$$

Correlation	σ_{bg}	V_0	μ_n	μ_p	ρ_r	**Model 1**
σ_{bg}		-0.16	0.19	-0.12	-0.40	σ_{bg}
V_0	-0.06		-0.05	-0.26	0.14	V_0
μ_n	0.57	0.02		-0.77	-0.30	μ_n
μ_p	-0.49	-0.28	-0.80		0.28	μ_p
ρ_r	-0.37	0.12	-0.16	0.17		ρ_r
Model 2	ρ_r	μ_p	μ_n	V_0	σ_{bg}	

Table 5.3: Correlation of device fitting parameters for Model 1 (upper right half) and Model 2 (lower left half). Note that in calculating the correlation the sign of the mobilities (sign of the slope of the conductivity curve) was maintained.

where the mean values of the variables X and Y are $\bar{X}$ and $\bar{Y}$, respectively. The correlation between all fitting parameters and additional variables extracted from the data are presented in Table 5.3.

For the number of data points (126), correlations above ~0.18 are distinguishable from the null hypothesis at the 95% confidence level, and are discussed in turn. In both models it is seen that μ_n and μ_p are most strongly correlated, as expected (in ideal graphene the correlation is -1 since electrons and holes are symmetric). The correlation between μ_p and V_0 for both models appears to be an artifact of the use of three different chips, since each chip has a different average value for V_0 (Figure 5-7(a)).

This dependence of the Dirac point voltage on which chip the devices are on is due to the different processing to which the chips were subjected. These three chips were processed concurrently in an effort to see which method yielded the best devices. Chip A01-8C used Ni as the graphene etch mask, which was removed by nickel etchant in the NSL. Chip A01-8D1 used a photoresist etch mask with acetone removal, but is suspected to have organic residue from the photoresist between the graphene and the metal contact pads. Chip A01-8D2 used a Cr/Au bilayer as the graphene etch mask, which was removed by CR-7 chrome etchant in the NME group lab. Clearly, the acid etchants dope the graphene devices n-type, while the organic residue has the opposite effect of doping the graphene devices p-type. This serves to illustrate the importance of a consistent procedure when fabricating many devices, and indicates that it may be possible to achieve considerable control of the Dirac point voltage

in practical devices, though whether this degrades other device properties is still an open question.

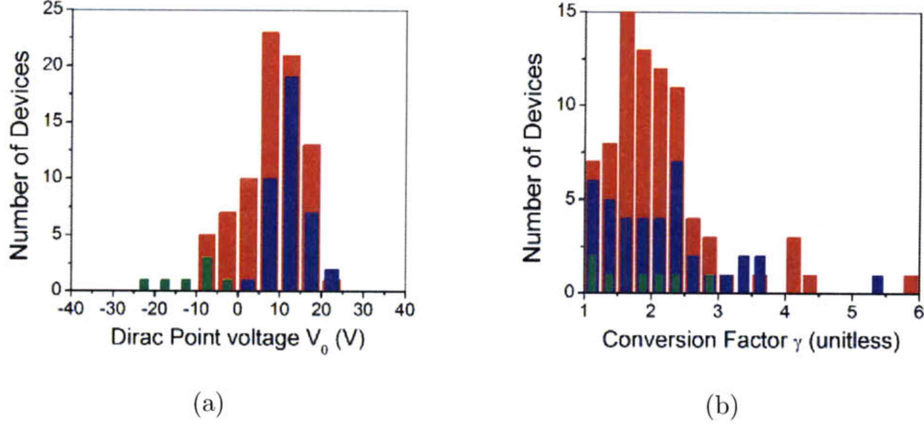
It is interesting to note that there is also a slight correlation between V_0 and μ_p, but not between V_0 and μ_n. Due to the dependence of V_0 on which chip the device comes from, however, the correlation between V_0 and μ_p is judged to be coincidental. By looking at figures similar to Figure 5-7, it is observed that the parameters μ_n and μ_p have no discernible difference between chips. However, there are obvious relations $\rho_r(\text{A01-8D1}) < \rho_r(\text{A01-8D2}) < \rho_r(\text{A01-8C})$ and $\sigma_{bg}(\text{A01-8D1}) < \sigma_{bg}(\text{A01-8D2}) < \sigma_{bg}(\text{A01-8C})$ which are valid for both the Model 1 *and* the Model 2 parameters.

This variation is not due to the CVD graphene itself, as each of these three chips was cleaved from the same starting wafer after the deposition of graphene. A possible interpretation is that ρ_r is due mainly to short-range scattering in the graphene, which is enhanced when the acidic etchant solutions create additional defects in the graphene. Then, the σ_{bg} ordering indicates the amount of parallel conducting channels. It is considered unlikely that the acidic etchant actually removes layers of the graphene material, which according to the simple tight binding model discussed below will decrease the gate voltage-independent density of states in the graphene. It is possible that moderately conducting photoresist residues remain after processing on chip A01-8C. It is also concievable that the acid treatment affects the band structure of the graphene, altering the density of states in the energy range of interest. These possibilities are left to address in future work.

The sign of the covariance of ρ_r with μ_n and μ_p in Model 1 indicates a contravarying relationship; indeed, plots of these variables suggests a reciprocal relationship. This makes sense considering that in Model 1, this is exactly the form that the conductivity takes. Similarly, the covariance of σ_{bg} with μ_n and μ_p in Model 2 arises from their direct combination in the conductivity formula.

The only remaining correlation to consider is that of σ_{bg} and ρ_r. It turns out that since the product of these variables is a constant (independent of choice of model, see Appendix D), the form of their variation should be reciprocal. Calculating the conductivity-based correlation of σ_{bg} and $\sigma_r = 1/\rho_r$ gives values of 0.49 for Model 1

and 0.57 for Model 2. These are clearly significant values, and indicate that σ_{bg} varies inversely, not directly, with ρ_r.



(a) (b)

Figure 5-7: Histogram of fitting parameters (a) V_0 and (b) γ for 126 graphene line devices which are the same for Model 1 and Model 2. Colors describe which chip a device comes from: (Red) A01-8C, (Blue) A01-8D2, or (Green) A01-8D1. Note that V_0 depends on the chip, indicating that the different chemical treatment during fabrication resulted in different doping levels. The mean and standard deviation for each chip are: (Red) 8.1 $\pm$ 7.0 V, (Blue) 12.1 $\pm$ 4.0 V, and (Green) -10.7 $\pm$ 5.8 V. The distributions for γ are parameter independent to within their uncertainty. Mean and standard deviations for the parameters, ignoring differences between chips, are given in Table 5.2.

5.6.4 Model-Independent Parameter Correlation

There are also several parameters which can be extracted from the conductivity curves and fitting curves which are the same for both models. These include the modulation factor γ (see Appendix D), the minimum conductivity of the gate sweep σ_{min}, the difference between the background conductivity and minimum conductivity σ_{min-bg}, the mobilities calculated directly from the slope of the conductivity curves (see Section 5.5.2), the uncertainty of each conductivity data point δ_{dat} (see Section 5.5.2), and the Dirac point voltage V_0. Note that $\sigma_{min-bg} = \sigma_{min} - \sigma_{bg,1} = \sigma_{min} - \sigma_{bg,2}/\gamma$ where the numerical subscript refers to the model from which the parameter is taken. Though expressed in different manners, because the fit curves for Model 1 and Model 2 are identical, σ_{min-bg} refers to the same point on the conductivity graph. The

Correlation	γ	σ_{min}	σ_{min-bg}	$\mu_{p,slope}$	$\mu_{n,slope}$	δ_{dat}
V_0	0.19	-0.15	0.12	-0.23	-0.09	-0.18
δ_{dat}	0.03	0.51	0.27	-0.38	0.47	
$\mu_{n,slope}$	-0.20	0.29	0.74	-0.83		
$\mu_{p,slope}$	0.21	-0.23	-0.86			
σ_{min-bg}	-0.19	0.27				
σ_{min}	-0.02					

Table 5.4: Correlation of parameters of the conductivity curves which are applicable to both Model 1 and Model 2. Note that in calculating the correlation the sign of the mobilities (sign of the slope of the conductivity curve) was maintained.

correlations between all these parameters are given in Table 5.4.

To begin, both γ and V_0 are not significantly correlated with the other parameters. δ_{dat} is moderately correlated with σ_{min} and to a lesser extent with $\mu_{n,slope}$ and $\mu_{p,slope}$, which makes sense if the relative uncertainty when measuring the current is fixed. The significant correlation of mobilities $\mu_{n,slope}$ with $\mu_{p,slope}$ is interpreted in the same manner as a manifestation of the symmetry between electrons and holes.

The most important correlations, from an analysis perspective, are the correlations of σ_{min-bg} with $\mu_{n,slope}$ and $\mu_{p,slope}$. This behaviour is a reversal of that observed in [10] for single layer graphene at variable doping. Clearly, σ_{min-bg} is due not simply to charge impurities near the graphene. Rather, it points to the dominance of short-range scatterers which affect the transport of both gate-induced and charge-puddle carriers in the thin graphene regions (according to a Model 1 view of transport). This makes sense, as CVD graphene is expected to be more defective than HOPG grapene.

5.6.5 Mixed Correlation

The final set of correlations to consider is between the fitting parameters of the models and the model-independent parameters, presented in Table 5.5. Many of the previous results for model-independent parameter correlations follow, once it is noted that high degrees of correlation with Model 1 parameters give $\sigma_{bg} \approx \sigma_{min}$, $\mu_n \approx \mu_{n,slope}$, and $\mu_p \approx \mu_{p,slope}$. Again, δ_{dat} correlates with the magnitude of the conductivity, while ρ_r is mixed in to a number of parameters. It is interesting to note that γ is independent of

Model 1	γ	σ_{min}	σ_{min-bg}	$\mu_{p,slope}$	$\mu_{n,slope}$	δ_{dat}
σ_{bg}	-0.01	1.00	0.22	-0.19	0.26	0.50
μ_n	-0.11	0.23	0.77	-0.80	0.96	0.43
μ_p	0.13	-0.17	-0.89	0.95	-0.73	-0.33
ρ_r	0.63	-0.41	-0.34	0.35	-0.36	-0.16
Model 2	γ	σ_{min}	σ_{min-bg}	$\mu_{p,slope}$	$\mu_{n,slope}$	δ_{dat}
σ_{bg}	0.50	0.77	0.14	-0.10	0.18	0.46
μ_n	0.40	0.31	0.46	-0.43	0.60	0.41
μ_p	-0.38	-0.25	-0.61	0.59	-0.45	-0.32
ρ_r	0.41	-0.59	-0.36	0.37	-0.38	-0.24

Table 5.5: Correlation of model-dependent parameters (left) with model-independent parameters (top).

σ_{bg} even though it is a factor. Instead, γ is only dependent on ρ_r. This implies some measure of correlation between σ_{bg} and γ, which is verified explicitly in Table 5.3. The reason that this model should present such a fortuitous dependence is unknown.

The correlations for Model 2 are not as easily interpreted as in the Model 1 case. Correlations between all parameters are significant, exemplified by the dependence of γ even on μ_n and μ_p, which do not appear in its analytic formula. There is thus no clear mapping between the natural (model-independent) parameters parameters and the parameters of Model 2; all Model 2 parameters are nontrivial combinations of the set of model-independent parameters.

The exact dependence of the Model 1 mobility parameters on the mobility calculated from the slope of the conductivity curves is particularly interesting, and shown in Figure 5-8(a). At low mobilities the parameters obtained by both methods are nearly equal, while at high mobilities there is a noticeable divergence due to the effect of ρ_r becoming more pronounced. The corresponding correlation for Model 2 is shown in Figure 5-8(b)

The result of this investigation is that analysis according to Model 1 provides a more clear interpretation of the fitting parameters, as expected from the model derivation. However, simply from this it is not clear which model more accurately represents the physical situation in graphene ribbons. To determine this, additonal measurements must be made. An attempt in this direction is discussed below.

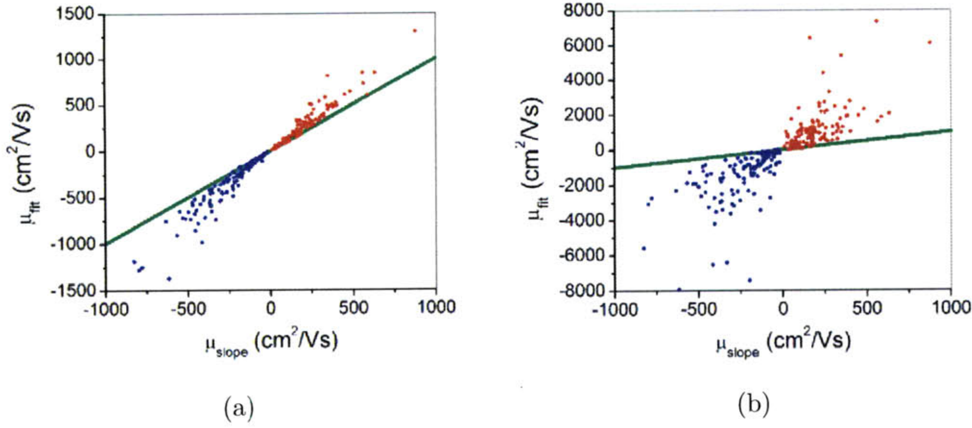


Figure 5-8: Comparison of mobilities from the fitting models $\mu_{fit} = \{\mu_n, \mu_p\}$ to mobilities obtained directly from the slope of the conductivity curves $\mu_{slope} = \{\mu_{n,slope}, \mu_{p,slope}\}$. (a) Mobility from Model 1, correlation ~0.96. (b) Mobility from Model 2, correlation ~0.60. Electron mobilities are marked in red, and hole mobilities in blue. The green line is a guide to the eye with unit slope. Note that the difference in the correlation between parameters is very noticeable.

5.6.6 Thickness Calculation

Conduction through multilayer regions of graphene requires a correlation between σ_{bg}, μ_k, and d which is described by Equation 5.6. From the fitting parameters we can calculate the expected thickness for each device, which is expected to match the thickness measured by AFM if the background conductivity is explained by the STB model:

$$d = \frac{M_0 \sigma_{bg}}{C_g \mu_k}. \tag{5.9}$$

The distribution of thicknesses d calculated from Equation 5.9 is shown in Figure 5-9. A log-normal distribution is observed using both Model 1 and Model 2 parameters. The log-normal distribution function is

$$f(x; \mu, \sigma) = \frac{A}{x\sigma\sqrt{2\pi}} e^{-\frac{\left(\ln \frac{x}{\mu}\right)^2}{2\sigma^2}}$$

where parameters are interpreted as follows:

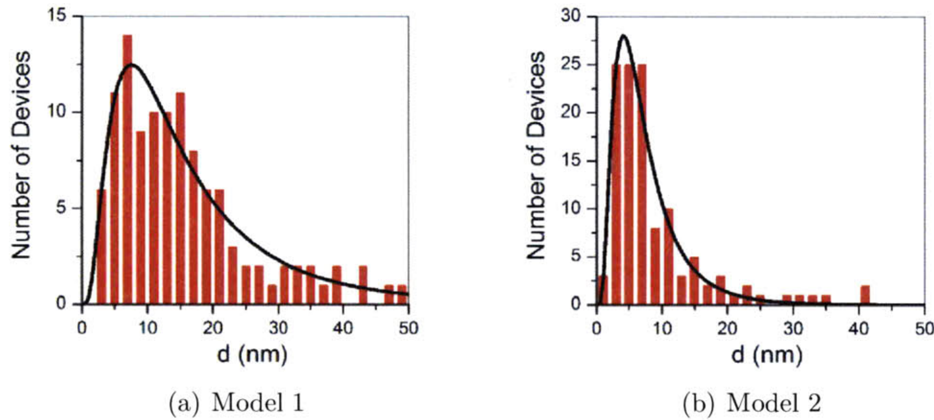
$x =$ Ordinate point $\qquad$ Mean $= \mu e^{\sigma^2/2}$

$$A = \text{Amplitude (integral)} \qquad \text{Median} = \mu$$

$$\mu = \text{Centering parameter} \qquad \text{Mode} = \mu e^{-\sigma^2}$$

$$\sigma = \text{Widening parameter} \qquad \text{Variance} = \left(e^{\sigma^2} - 1\right)\mu^2 e^{\sigma^2}$$

and is the multiplicative analogue of the normal distribution. Since the fitting parameters are fairly randomized over a broad range of values, and are combined as factors in Equation 5.9, this functional form for the distribution of d is not surprising. The parameters of these log-normal fitting curves are given in Table 5.6.



(a) Model 1

(b) Model 2

Figure 5-9: Log-normal distribution of the graphene film thickness d calculated using Equation 5.9 for (a) Model 1 parameters and (b) Model 2 parameters. The black line is a best-fit log-normal distribution. Distribution parameters are given in Table 5.6. These values correspond well to the thickness measured by AFM (6.9 nm) and justify the analysis of these CVD graphene ribbons as thin graphite films according to a simple two-band model.

These calculated thicknesses are both very close to the average film thickness measured by AFM of $d = 6.9 \pm 1.3$ nm. This is a strong indication that the STB model is applicable even for our thin CVD graphene films. The wide variation observed in calculated thickness d is justified by the random variations in average thickness and in the random arrangement of thickness regions in each device. Also, there is always the expectation that the mobility will vary under the influence of a random distribution of charged impurities trapped in the substrate and on top of the graphene film.

It is emphasized, though, that the ensemble behaviour clearly suggests that the

	Model 1	Model 2
A	235 ± 13	226 ± 13
μ (Median)	13.2 ± 0.9	6.2 ± 0.3
σ	0.75 ± 0.05	0.64 ± 0.05
Mean	17.6 ± 1.9	7.6 ± 0.6
Mode	7.5 ± 1.1	4.1 ± 0.4
St. Dev.	15.4 ± 3.1	5.4 ± 0.9
d (AFM)	6.9 ± 1.3	

Table 5.6: Thickness fitting parameters for log-normal distributions represented in Figure 5-9. Mean, Median, and Mode are given in units of nanometers. The true distribution should lie somewhere between the extremes given by Model 1 and Model 2. The distribution of heights as determined by AFM is shown at the bottom of the table, and more closely matches the predictions of Model 2.

CVD graphene behaves like a thin graphite film in the simple two-band approximation because the thicknesses calculated correspond to the thickness measured by AFM. Additionally, it appears that the Model 2 parameters more closely match the values for film thickness, implying that the Model 2 interpretation of the residual resistvity ρ_r is more likely to be correct. This implies that the intrinsic mobility of the graphene is much higher than that which is measured directly from the slope of the conductivity curves. While this approach is likely viewed with skepticism, it is the best that can be done with graphene that is so far from ideal.

5.7 Temperature Dependence

Gate sweeps in single-layer graphene, bi-layer graphene, and bulk graphite have characteristic temperature dependencies [9, 69, 86, 87, 61]. In order to compare the CVD graphene material to the literature, temperature dependent electrical characterization of seven CVD graphene devices was performed. For each device, gate sweeps at temperatures from T = 80 to 320 K in steps of 20 K were acquired. The system used was a vacuum-sealed (10^{-6} torr) cryogenic insert from Janis Research Company, inserted into a dewar of liquid nitrogen. All seven devices showed very similar behaviour, and the measurements for one of these devices are shown in Figure 5-10(a).

For CVD graphene, the conductivity at all gate voltages increases with tempera-

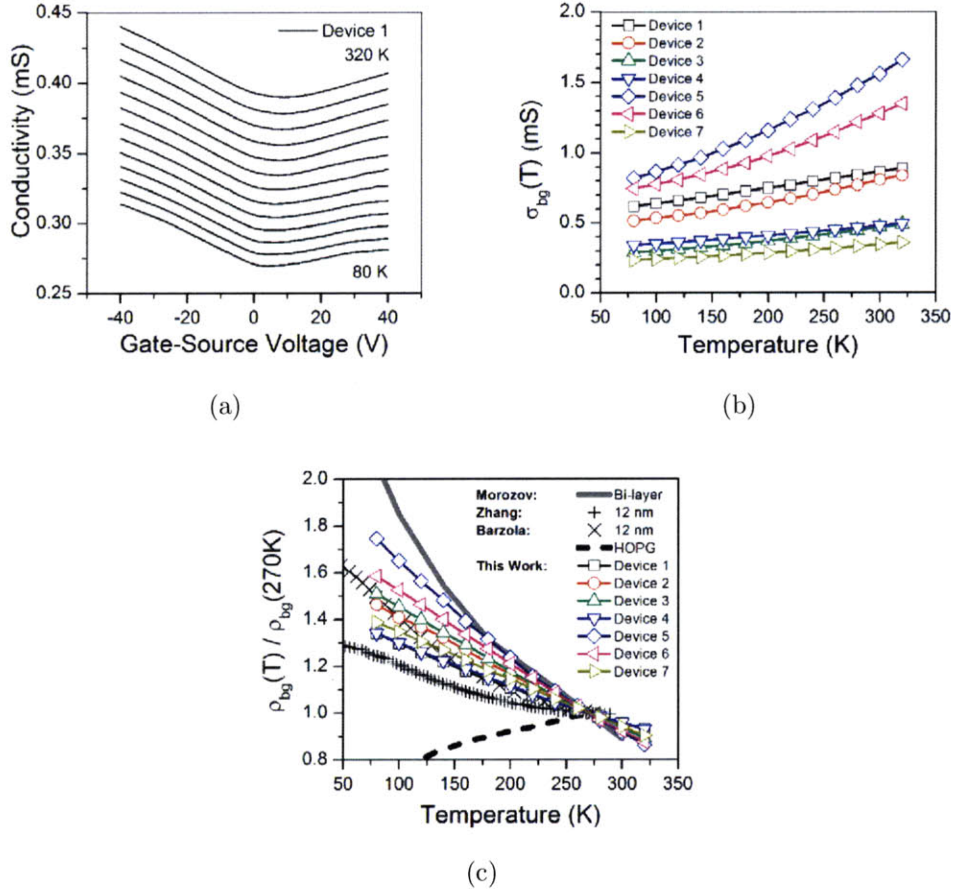


Figure 5-10: (a) Gate sweeps taken with 100 mV bias at temperatures ranging from 320 K (top) to 80 K (bottom) in increments of 20 K for Device 1 after high-bias annealing. Note that there is no offset for clarity; the background conductivity changes significantly with temperature. (b) Background conductivity values as a function of temperature for seven devices. (c) Normalized resistivity as a function of temperature. Colored symbols and lines indicate our devices. The other lines and crosses are data adapted from Morozov [9], Zhang [72], and Barzola-Quiquia [73]. Our devices, with mean thickness 6.9 nm, show a semiconductor-like behaviour similar to that seen in bi-layer graphene and thin ($\leq$12 nm) HOPG graphite.

ture. The magnitude of the change for a single device is essentially the same for all gate voltages, so Figure 5-10(b) plots the changing background conductivity σ_{bg} as a representative value. This is markedly different from the behaviour of exfoliated single-layer graphene or bi-layer graphene devices [9, 61, 60], which have a linear conductivity far from the Dirac point which changes negligibly with temperature (after removal of the constant residual resistivity term ρ_r). The only similarity is with bi-layer graphene near the Dirac point, where the conductivity shifts upward with temperature for $|E| \leq k_B T$ (see figures 3 and 4 of [9]). This is precisely the region where the STB model is valid (Figure 5-3(a)), which is an expected behaviour in light of the applicability of the STB model for the CVD graphene devices discussed previously.

The expected temperature behavoiur of CVD graphene, then, should be the behaviour of the STB model. This has been evaluated for the resistivity at the Dirac point [72, 88] as:

$$\rho(T) = \frac{1}{e\mu(T)n(T)} = \frac{1}{e}\frac{1 + \mu_i A_0 T}{\mu_i}\frac{1}{2C_0 k_B T ln\left[1 + exp(E_0/k_B T)\right]} \tag{5.10}$$

where e is the electron charge, μ is the mobility, n is the charge carrier density, μ_i is the mobility limited by static scatterers, A_0 is a constant proportional to the strength of acoustic phonon scattering, C_0 is a constant proportional to the effective mass of the charge carriers, E_0 is half the band overlap (i.e., $E_0 = \Delta/2$), k_B is the Boltzmann constant, and T is the temperature.

In order to compare the behaviour of CVD graphene to Equation 5.10, the conductivities of each device in Figure 5-10(b) are inverted and plotted as resistivities in Figure 5-10(c), normalized to the resistivity at 270 K. For comparison, the maximum resistivity of bi-layer graphene [9], the maximum resistivity of a 12 nm thick HOPG graphite film [72], and the maximum resistivities of 12 nm thick and 17 μm thick HOPG graphite films [73] are also shown in this plot. In general, a thinner graphite film will show a larger semiconductor-like increase of maximum resistivity with decreasing temperature. All seven CVD graphene devices vary like graphite

films with thickness at or below 12 nm, which is consistent with the AFM thickness measurements and calculated thickness distributions discussed above.

The resistivities of each device in Figure 5-10(c) are fit to Equation 5.10 using free parameters $\mu_i A_0$, $\mu_i C_0$, and E_0. The curvature of $\rho(T)$ is determined primarily by E_0, which for these seven devices ranges from 13 to 22 meV with an average value of 17 meV. This is within the range expected for thin graphite films (~10-20 meV for <95 nm thickness [72]), but much larger than the values found for the bi-layer graphene and 12 nm graphite films (~6-7 meV).

This larger than expected band overlap may be due to the presence of regions of different thickness in each CVD graphene device, which may require a more sophisticated analysis than Equation 5.10. Alternatively, the band overlap may actually be as large as described, due to a higher density of defects in CVD graphene compared to HOPG graphene, which will increase coupling between layers thereby increasing the band overlap. This uncertainty should be resolved when measurements are made on regions of uniform thickness, which will also remove any variation caused by the junctions between regions of different thickness. The use of four-probe techniques in future work is also highly desirable, and will aid comparison of results to the extant literature.

5.8 Conclusion

In summary, arrays of two-terminal FET-like devices with channels made of graphene grown by chemical vapor deposition have been fabricated and their conductivities as a function of gate voltage and temperature has been analyzed. A simple two-band transport model commonly used to describe bulk graphite has been demonstrated to apply also to the thin 6.9 ± 1.3 nm CVD graphene films. This is justified by analysis of the magnitude of the background conductivity versus mobility for 126 devices, as well as by the temperature dependence of the Dirac point conductivity for seven devices. This was accomplished by the use of a fitting model which has the same functional form as for both single-layer graphene and thin bulk graphite. The

extracted field effect mobility has an average value of about μ = 1200-1400 cm^2/Vs for electrons and holes, which is similar to other measurements on CVD graphene using a different fabrication process. This mobility is also similar to that of the first microcleaved HOPG graphene devices ($\geq$ 3000 cm^2/Vs [2]). It is anticipated that just as has been demonstrated for microcleaved HOPG graphene, the transport properties of CVD graphene can be improved with refined synthesis, transfer, and device fabrication methods.

Chapter 6

Lincoln Laboratory CVD Graphene Devices

Measurement and analysis of a number of different CVD graphene device geometries was carried out as a collaborative project with Jakub Kedzierski in Group 88 (Advanced Silicon Technology) at Lincoln Laboratory. The purpose of this research was to characterize the CVD graphene devices fabricated at Lincoln Laboratory to see if their fabrication method was superior to the method used at MIT (Chapter 5). The conductivity and mobility of the graphene was used as the main point of comparison, and the ability to top-gate the devices allowed additional investigation of surface effects.

The analysis presented here presents results for a multitude of different device geometries, enabled by the more advanced processing carried out by Paul Healey at Lincoln Laboratory. In short, the devices were fabricated from a single piece of CVD graphene which was grown and transferred to a silicon wafer having 100 nm thermal oxide coating, according to the procedures in Section 3.2.2. Optical lithography was then used to pattern the graphene. Metal contact pads were deposited, and the entire wafer was uniformly coated with 40 nm of HfO_2 ($\kappa = 18$) by atomic layer deposition at 200 °C. This top oxide layer was patterned and etched to expose the underlying metal contact pads, and a final lithography step allowed deposition of metallic contact pads as top gates over graphene channels of some devices. The final devices were annealed

at 400 °C for 20 minutes in a 9:1 mixture of N_2:H_2, and measured within the following weeks.

6.1 Measurement Description

Measurements were performed on a commercial probe station with an optical microscope mount and with tungsten probe pins mounted on 3-axis micropositioners. The pins were connected to a HP4156 semiconductor parameter analyzer, and gate sweeps were acquired.

A number of different gate sweep parameters were used. They are abbreviated in Table 6.1:

B	=	Top gate sweep from +3 V to -3 V in 0.2 V increments, at V_{ds}= 0.1 V then V_{ds}= 1.0 V, with back gate (chuck) at 0 V
C	=	Back gate sweep from +30 V to -30 V in 2 V increments, at V_{ds}= 0.1 V then V_{ds}= 1.0 V, with top gate at 0 V
Z	=	Top gate sweep from +4 to -3 V, at back gate voltages of +30 V to -30 V in steps of 5 V, at V_{ds}= 0.1 V

Table 6.1: Measurements performed on the Lincon Laboratory devices.

These ranges and values were chosen so that full modulation of the drain-source current was seen, including the Dirac point and sublinear p-type and n-type conduction.

As usual, the measured current is converted into conductivity using the equation

$$\sigma = \frac{I_{ds}}{V_{ds}} \frac{L}{W}$$

where device length L and width W are given by the pattern design.

6.1.1 6-Terminal Devices

With a six-terminal device in a Hall bar geometry, there are a number of conductivity measurements which can be made. While such geometries are designed for measurement in a magnetic field in order to calculate charge carrier density and mobility,

it was found that the devices available did not survive to give good conduction for such measurements. Specifically, the Dirac point for the available devices was shifted out of the gate voltage scan range. This, combined with breakage of devices during previous electrical probing, made it necessary to make do with a combination of Van der Pauw measurements.

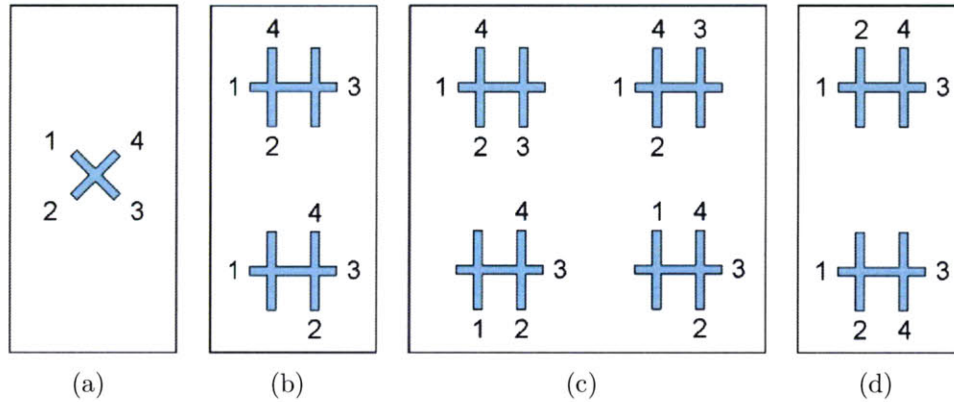


Figure 6-1: Lead identification for Van der Pauw measurements, with contacts 1 to 4. (a) Ideal arrangement of four symmetric leads. (b) Arrangement of pins for principal measurements of left and right cross regions (top and bottom respectively). (c) Alternate arrangements of the pins which should give identical measurements as the corresponding top and bottom arrangements in (c). (d) Principal lead arrangements for Hall measurements of the central section of the device. Alternate geometries are not enumerated.

6.1.2 Van der Pauw Measurements

The Van der Pauw method uses a series of 4-terminal measurements to find the resistance of a small region of material which forms the junction between four leads (of the same material). The measurement is geometry-independent (as long as the width of the leads is less than the distance from the contacts to the junction), eliminating the effects of contact resistance and lead resistance [89]. The measurement is made as follows.

The four leads of a typical device are labeled consecutively with the numbers 1-4, as in Figure 6-1(a). Letting the letters a-d stand for some permutation of these numbered leads, one can measure the general resistance as the voltage difference developed between two adjacent leads when current flows between the other two

leads

$$R_{ab,cd} = \frac{V_{cd}}{I_{ab}} = \frac{V_d - V_c}{I_{a\to b}},$$

where the arrow indicates the direction of current flow.

For a symmetric device, there are two symmetries which should be obeyed. First, switching the terminals used for current and voltage should produce the same resistance value ($R_{ab,cd} = R_{cd,ab}$). Second, reversing the polarity of measurements should produce the same resistance value ($R_{ab,cd} = R_{ba,dc}$). In the case of a nonsymmetric device (either in geometry or material properties), this may not be the case. However, the sum of the symmetry-related resistances are invariant quantities. Defining these sums with subscripts denoting the relation between pairs of V and I labels in Figure 6-1(a),

$$R_{vertical} = \tfrac{1}{4}(R_{12,34} + R_{34,12} + R_{21,43} + R_{43,21})$$
$$R_{horizontal} = \tfrac{1}{4}(R_{23,41} + R_{41,23} + R_{32,14} + R_{14,32}).$$

Again, the quantities $R_{vertical}$ and $R_{horizontal}$ should be equal for symmetric device, but in the absence of symmetry are related by

$$e^{-\pi R_{vertical}/R_S} + e^{-\pi R_{horizontal}/R_S} = 1 \tag{6.1}$$

where R_S is the average sheet resistance of the junction area of the device. Equation 6.1 is transcendental, so R_S must be solved for numerically. The exception to this is the symmetric case $R_{vertical} = R_{horizontal} = R$, where it is found that $R_S = \frac{\pi R}{\ln 2}$. The coefficient $\frac{\pi}{\ln 2}$ arises from the geometry of current spreading through a conductive sheet.

Similar to the description of the sheet resistance measurements described above, the Hall resistance can be measured by defining the resistances (with reference to Figure 6-1(a) for lead numbering)

$$R_{ac,db,X} = \left.\frac{V_{db}}{I_{ac}}\right|_X = \left.\frac{V_b - V_d}{I_{a\to c}}\right|_X$$

where the subscript $X \in \{\uparrow, \downarrow\}$ denotes the direction of the magnetic field perpendicular to the plane of the device. The measurements are assumed to be done with constant magnetic field magnitude.

The previous symmetries still hold ($R_{ac,db,X} = R_{db,ca,X}$ and $R_{ac,db,X} = R_{ca,bd,X}$), but in addition there is a symmetry with relation to the magnetic field: $R_{ac,db,X} = -R_{db,ca,-X}$. This allows one to write the average resistances based on the magnetic field direction as

$$R_{\uparrow} = \tfrac{1}{4}\left(R_{13,42,\uparrow} + R_{42,31,\uparrow} + R_{31,24,\uparrow} + R_{24,13,\uparrow}\right)$$
$$R_{\downarrow} = -\tfrac{1}{4}\left(R_{13,42,\downarrow} + R_{42,31,\downarrow} + R_{31,24,\downarrow} + R_{24,13,\downarrow}\right)$$

and to define the average Hall resistance as

$$R_H = \tfrac{1}{2}\left(R_{\uparrow} + R_{\downarrow}\right). \tag{6.2}$$

The Hall resistance is related to the magnetic field B and sheet charge density n_S through

$$B = qn_S R_H$$

where the sign of n_S indicates the type of charge carrier. Finally it is noted that the Hall voltage is defined as $V_H = IR_H$ where the current I is that used to make all of the above measurements.

6.1.3 Capacitance Approximation

As noted in Appendix B, the quantum capacitance will become important when these devices are gated through the HfO_2 top gate. However, the analysis in this section makes the assumption that there is no quantum capacitance; only the electrostatic capacitance is used for the computation of mobilities through the transconductance. The error introduced by this approximation is estimated as follows.

Using Equation B.2, the quantum capacitance $C_q(V_{ch})$ is calculated for a range of graphene channel potentials V_{ch}. This is combined in series with the electrostatic capacitance listed in Table B.1 to compute the total capacitance $C_{tot}(V_{ch})$. Because of the charge balance equation for capacitors in series, the gate voltage V_{gs} corresponding to a given V_{ch} can be calculated as $V_{gs} = (C_q(V_{ch})/C_{tot}(V_{ch}))\,V_{ch}$. Since the total capacitance C_{tot} and gate voltage V_{gs} are now known (for each value of V_{ch}), these values can be considered in the case of a field effect mobility measurement. In Equation C.2 the gate capacitance appears in the denominator. To convert from a mobility value calculated with the electrostatic capacitance $\mu_{fe}(C_g)$ to the correct mobility $\mu_{fe}(C_{tot})$ requires correction of the former by a factor of $\beta = C_g/C_{tot}$.

The value of the correction factor β is shown in Figure 6-2. The asymptotic bound is of course unity, but the maximum values are 1.041 for the back gate and 1.473 for the top gate. In fact, for the ranges given, the top gate ratio is always above 1.09, indicating that the top gate mobility will be underestimated by at least 9%! To obtain an estimate of the actual change of peak mobility values, the capacitance ratio may be evaluated at the average gate voltage which corresponds to the mobility peak. For bottom and top gates, these gate voltages are 6 and 0.6 V respectively, for a high-mobility device. This leads to correction factors of 1.017 for the back gate mobility and 1.19 for the top gate mobility.

There is one major complication to the method presented above, and that is the presence of charge puddles in the graphene. These charge puddles are induced by charge impurities surrounding the graphene, and are indicative of a variation of the Dirac point voltage throughout the graphene sheet [90]. A full treatment of this issue will involve the calculation of the induced charge density n* due to the charge impurities [32], and accommodation of this value when computing the charge density induced by the gate. The first-order effect of this will be to convolute the capacitance correction factor (as a function of the gate voltage) with the distribution of induced potentials (converted to be in terms of V_{gs} through use fo C_{tot}). This will lower and broaden the peak in β. The manner in which this affects the correction factor for a particular device will depend on the specific form of the convoluting function and

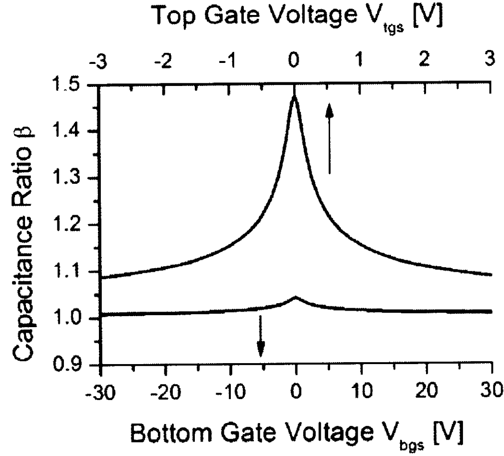


Figure 6-2: Capacitance correction ratio β for the mobility, used for converting between calculations without and with the quantum capacitance. Horizontal axes correspond to the measured range of gate voltages, and roughly to equal induced charge densities.

the location of the mobility peak. However, it is a good estimate that the correction factor will increase due to charge inhomogeneity, based on the curvature of the ratio curve in the region around the peak values quoted previously.

6.2 Two-Terminal Devices

A total of 220 two-terminal devices were measured. Of these, 95 devices had a back gate only, while 125 devices had a back gate and a top gate. Results of a typical measurement with both top and back gate are shown in Figure 6-3. Results for devices with only a back gate are similar to the corresponding back gating measurements for devices with both top and bottom gates. The mobility is calculated using the slope between consecutive data points and the electrostatic capacitance. The conversion between gate voltage and charge density is $n = C_{g,top}V_{g,top} + C_{g,bottom}V_{g,bottom}$ which gives a correspondence between gate voltages of $V_{g,bottom} = \left(C_{g,top}/C_{g,bottom}\right)V_{g,top} = \left(3.984 \times 10^{-3}/3.453 \times 10^{-4}\right)V_{g,top} = 11.5V_{g,top}$ for Figure 6-3 in the electrostatic capacitance approximation. Thus the ranges shown are roughly equivalent in terms of charge density. A few general trends are observed:

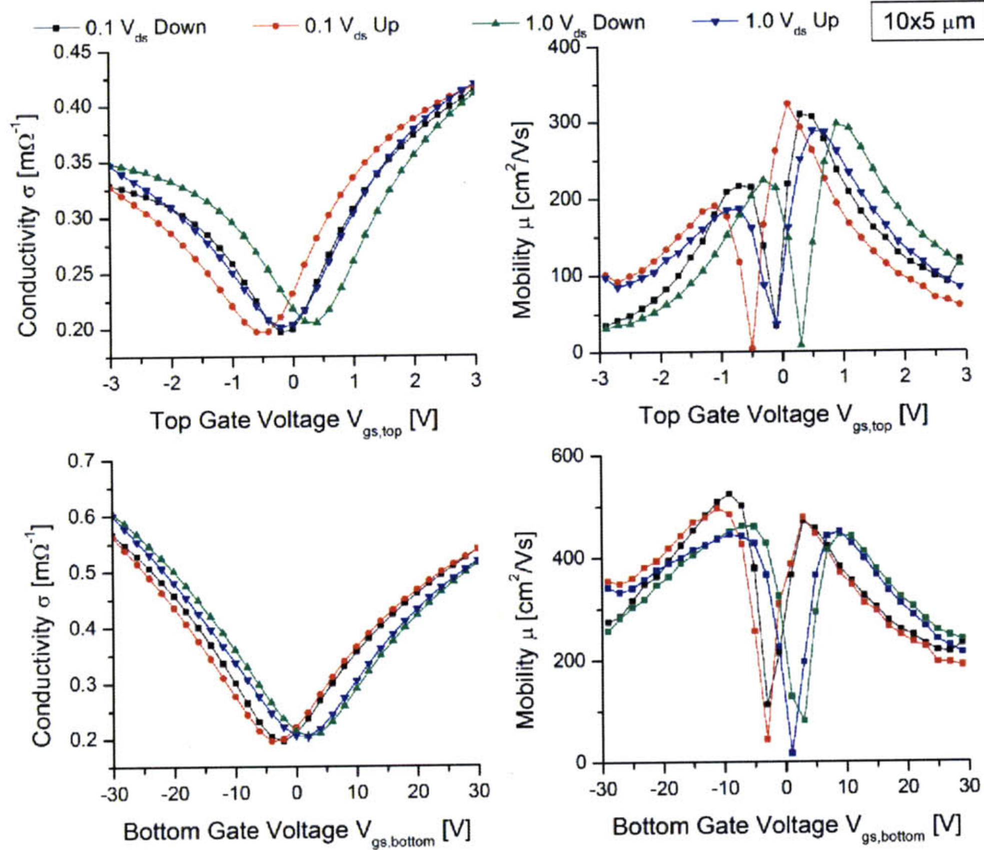


Figure 6-3: Conductivity (left) and mobility (right) for a typical deviced with top-gating (top) and bottom-gating (bottom). In each case, the other gate is held at 0 V. The four lines consist of up and down sweeps of the gate voltage at each of two drain-source voltages, 0.1 V and 1.0 V, as indicated by the legend at top. The device dimensions are 10 μm long by 5 μm wide.

1. **Dirac point shift.** The gate voltage at which the minimum conductivity occurs, which is a good estimate for the Dirac point of the graphene, increases by ~1-5 V for the back gate and ~0.1-0.5 V for the top gate as the drain-source voltage V_{ds} increases from 0.1 V to 1.0 V. This is larger than the expected shift, which is ~0 to V_{ds}V, and which arises from considering the graphene potential to lie between that of the source and drain. The reason for the larger than expected Dirac point shift is not clear.

2. **Hysteresis.** Hysteresis is much more pronounced in top-gated sweeps than in bottom-gated sweeps. The typical example in Figure 6-3 shows hysteresis of ~0.5 V for top gating and ~1.5 V for bottom gating, while the lowest values

observed are ~0.2 V and ~0 V respectively. The physical reasoning for hysteresis as an adjustment of local charges or dipoles (*e.g.* oxide charge traps or adsorbed polar molecules such as water molecules). This suggests that the voltage shifts are caused by additional oxide charge trapping which differs between bottom and top gating materials. The top gate HfO_2 dielectric can be considered to be more defective than the back gate SiO_2 dielectric, allowing more charge to leak in and out of the oxide interface during each sweep of the gate voltage. Measurements of this phenomenon at different voltages or sweep rates might illuminate the charge trap density or energy barrier, which would be useful for finding high-quality fabrication materials.

3. **Similar minimum conductivity.** The minimum conductivity is noted to be the same for both top and bottom gating. Since most devices which demonstrate a clear conductivity minimum have their Dirac point near 0 gate voltage (where both top and bottom gates are at 0 V, according to the conditions of Figure 6-3), this result is not surprising, and amounts to an observation that for a large number of devices the graphene is not chemically doped. This is discussed in more detail in Section 6.2.2, where it is found that some small variations in the minimum conductivity are expected which are often less than 5%.

4. **Top-gating saturation.** The top gating conductivity saturates more strongly than that for bottom gating. In Figure 6-3, p-type conductivity for top gating saturates at ~0.35 mS with a minimum conductivity of ~0.20 mS, giving a modulation of ~0.15/0.20 = 75%. Corresponding values for n-type conductivity (the more strongly saturated) for back gating are saturation at ~0.60 mS (estimated by extrapolating the visible section of the curve), minimum conductivity of ~0.20 mS, giving a modulation of ~0.60/0.20 = 300%. This is indicative of a greater amount of scattering at high charge densities with top gating versus bottom gating. Since this difference must arise from some source extrinsic to the graphene, and since at high charge densities it is short-range scattering which dominates transport, it is concluded that the HfO_2 top dielectric is more

defective than the thermally grown SiO_2 bottom dielectric.

5. **Higher bottom-gating mobility.** The right panels of Figure 6-3 clearly indicate that mobilities are suppressed for top gating with respect to bottom gating. This may also be due to the increased scattering which gives rise to the lower saturation for top gating mentioned previously.

The most striking difference between the two methods of gating is the mobility observed for each gating method. Histograms of the observed mobilities are shown in Figure 6-4. The mobility should theoretically be dependent only on the graphene material, because device geometric effects are accounted for in the calculation of the conductivity and in the normalization by the gate capacitance. But since the mobility is limited by long-range Coulomb scattering, and the top gate dielectric has a higher permittivity, it is hypothesized that the mobility may be decreased due to increased gate voltage-dependent charge trapping in the less perfect HfO_2 dielectric, compared to the SiO_2 dielectric. This is consistent with the observations of hysteresis and saturation mentioned above, but requires further work to make a quantitative verification.

The effect of top versus bottom gating in a single device is summarized in Figure 6-5. Here, only devices for which a clear mobility maximum was observed for both p-type and n-type conduction were selected. The ratio of mobilities is $\mu_{top}/\mu_{bottom} \approx 0.6$. This ratio is very different from the ideal 1.0 expected. One source of approximation is the assumption of dominance of the electrostatic capacitance. As discussed in Section 6.1.3, the quantum capacitance is significant for these devices with a thin oxide and a high-κ dielectric.

The correction factor β converts from mobility in the electrostatic approximation to mobility calculated using both electrostatic and quantum capacitance as $\mu_{eq} = \beta\mu_e$. As seen in Figure 6-2, the value for the back gate $\beta_{bg} \approx 1$, while the value for the top gate $\beta_{tg} \leq 1.5$ (with a more likely estimate of $\beta_{tg} \approx 1.3$). This can be used to correct

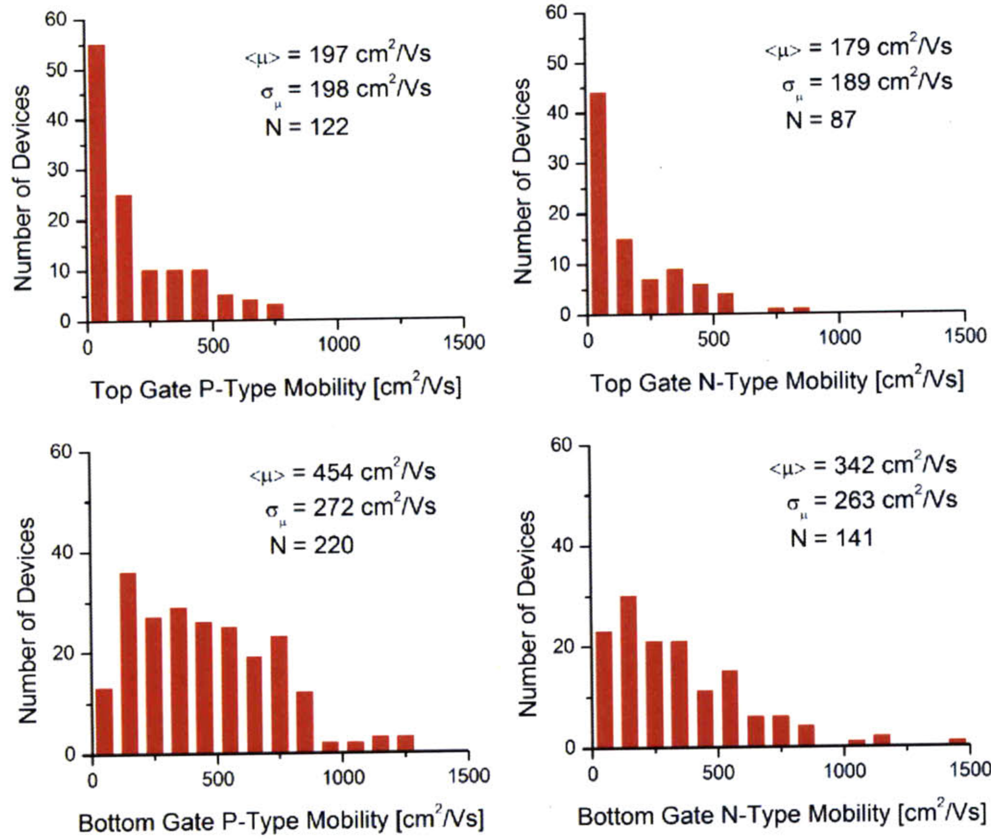


Figure 6-4: Histograms of mobilities for p-type (left) and n-type (right) conduction for top-gating (top) and bottom-gating (bottom). The mobilites used to construct these histograms are the average of the maximum mobilities observed for each of the four sweeps depicted in Figure 6-3. Mean mobility $\langle\mu\rangle$, standard deviation of the mobility σ_μ, and total device count N are indicated in the respective plots.

the observed mobility rato as

$$\frac{\mu_{top}}{\mu_{bottom}} \rightarrow \frac{\beta_{tg}\mu_{top}}{\beta_{bg}\mu_{bottom}} = \frac{1.3-1.5}{1}\frac{\mu_{top}}{\mu_{bottom}} = (1.3-1.5)0.6 = 0.8-0.9$$

Thus the quantum capacitance correction accounts for half to three-quarters of the mobility difference. However, the remainder is still significant and unaccounted for.

It is notable that the remaining 10-20% suppression of the top-gated mobility with respect to the back-gated mobility is opposite to the behaviour observed with the introduction of a high-κ dielecric seen in [91, 92] (which demonstrate a mobility enhancement). However, in these works the dielectric behaves as a liquid, thereby

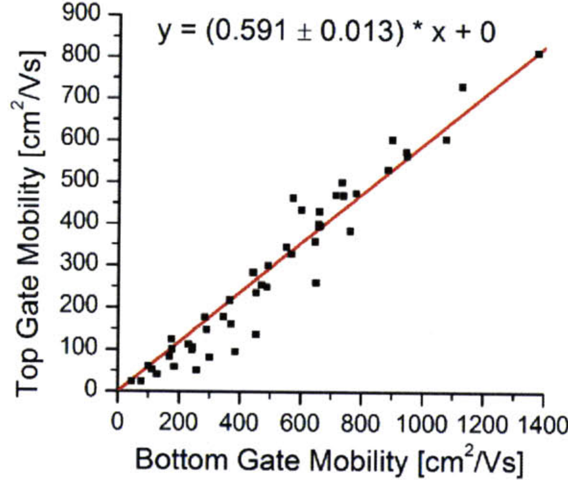


Figure 6-5: Top-gated versus bottom-gated maximum mobility for 48 devices for which both p-type and n-type conduction showed a clear mobility peak. The equation for the best linear fit to the data (red line) is shown at top. The peak mobility from top-gated measurements is on average only 60% that of the bottom-gated measurements. Accounting for quantum capacitance increases this to approximately 80%.

precluding its own introduction of charge impurities, while for the Lincoln Laboratory devices the dielectric is deposited as a solid. Without the ability to reconfigure, the solid may trap additional charge impurities and lead to increased scattering and decreased mobility. This view is supported by a number of studies of the deposition of top gate dielectrics (most unpublished, for an example see [93]). This line of investigation concludes that a dielectric buffer layer is necessary to mitigate the effects of charge traps at the graphene-dielectric interface. Since the Lincoln Laboratory devices have no such buffer, it is reasonable to assume that the remaining mobility suppression arises from the imperfect graphene-top dielectric interface.

6.2.1 Comparison to Graphene Line Devices

It is worth noting the similarities and differences between the current Lincoln Laboratory devices and the graphene line devices discussed previously in Chapter 5. The distributions of transconductance mobilities presented in Figure 6-4 and Figure 5-6 may be compared (the latter having mean and standard deviation of 233 ± 173 (p-type) and 198 ± 138 (n-type) as given in Table 5.2). The behaviour of the graphene line

devices falls somewhere between the top and bottom gate behaviour for the Lincoln Laboratory devices, though much closer to the top gate behaviour.

This similarity can be justified by considering the effects that processing has on a graphene channel. First, it is noted that even for thick graphene which can be analyzed by the simple two-band (STB) model, the variation of the density of states with gate voltage is independent of the thickness of the graphene. Because of this, there should be no variation of the transconductance mobility with graphene thickness. However, this conclusion assumes that the screening lenghth of the electric field in graphene is small compared to the thickness of the graphene. It is therefore noted that the majority of the charge density induced in the graphene must be localized at the graphene/oxided interface nearer to the gate (this situation is discussed further in Section 6.2.2). The scattering which occurs in the graphene due to short-range scatterers such as defects in the graphene or adjacent oxide are thus dependent on the quality of the appropriate interface.

In the Lincoln Laboratory devices, the graphene/HfO_2 interface is thus interpreted to be of lower quality than the graphene/SiO_2 interface. There may be several reasons for this. First, the CVD graphene may be intrinsically asymmetric, an example of which would be if the connectivity between thick and thin regions of graphene occurs near the nickel catalyst or away from it, or if the first layer of graphene which is formed is more defective than the subsequent layers which are stabilized by the first. Second, the chemical action during transfer of graphene may affect the quality of graphene. For example, the nickel catalyst etchant may also attack the graphene in contact with the nickel, while the polymer protects the opposite side. Third, the processes of device fabrication might affect the graphene interface. Most notably, graphene interfaces with oxides deposited by atomic layer deposition are known to be degraded compared to those without, and a uniform interface layer is necessary to mitigate these inhomogeneities. This last reason is considered the most likely. However, since the entire wafer was coated with HfO_2, there are no control devices to compare to in order to definitively observe the effect of the deposition of the top gate dielectric. It is expected, though, that the mobility degradation occurs for the

bottom gate measurements as well as for the top gate measurements, but to a lesser extent, due to the dielectric screening of the graphene.

For comparison, the graphene line devices presented in Chapter 5, which have no top gate dielectric interface, exhibit roughly half the mobility of the corresponding back-gated Lincoln Laboratory devices, and mobility roughly comparable to the top gated-Lincoln Laboratory devices. Thus the line devices are interpreted as more defective, with a defect density roughly equal to that introduced by the application of a top dielectric layer for the Lincoln Laboratory devices (at least; it may be more when considering that a defect at the top must affect the observed change at the bottom of the graphene layer). Barring the possibility of a difference in the CVD graphene material (which is reasonable since the growth process is only slightly changed), this is likely due to the etching process used to define the graphene lines. The metal deposited may bond occasionally to the graphene, which results in additional defects when the metal is etched away by an acid, or in metal scattering centers stuck to the graphene if they cannot be etched away. In the case of a photoresist etch mask, the same issues may arise from hard-baked residue which falls on or may adhere to the graphene.

However, if one considers the processing of the CVD graphene into devices to introduce a negligible defectiveness, then the Lincoln Laboratory devices are clearly made from a better quality material, exhibiting roughly twice the mobility of the graphene line devices made from the previous generation of graphene material. This is a significant improvement over the course of the year between fabrication of these two types of devices.

6.2.2 Top and Bottom Gating

The orthogonal sweep measurements of Figure 6-3 and the subsequent conclusions indicate some correspondence between the Dirac point voltages and mobilities observed for each gate sweep. To investigate this further, conductivity maps were obtained by sweeping the top gate voltage and stepping the back gate voltage as described by measurement Z of Table 6.1. Corresponding measurements were taken by sweeping

the back gate voltage and stepping the top gate voltage, and this procedure gave similar results.

6.2.2.1 Conductivity Map

Results from a typical top gate/back gate measurement are shown in Figure 6-6(a). This shows a clear V-shaped conductance for all top and back gate voltage sweeps.

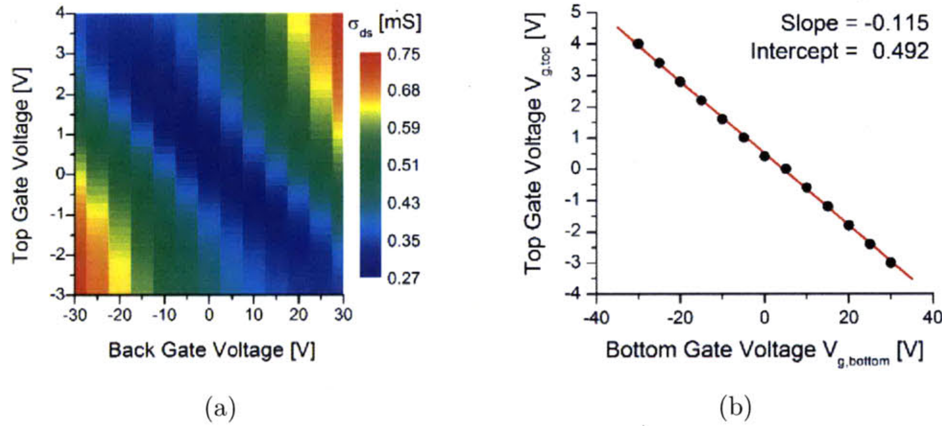


Figure 6-6: Conductivity dependence on top and bottom gate voltages for a typical two-terminal device fabricated at Lincoln Laboratory. (a) Intensity map of the conductivity for different top and bottom gate voltages. Top gate voltage was swept and then the bottom gate voltage stepped. (b) Plot of the position of the minimum conductivity for each top gate sweep used to construct (a) (black dots). The magnitude of the slope of the best linear fit (red line) is the ratio of the capacitance of the top and bottom gate electrodes, called the gating efficiency α. For this device, $\alpha = 0.115$.

The most noticeable characteristic of the conductivity map is the diagonal of low conductivity. This corresponds to the position of the Dirac point, where the potentials induced by the top and bottom gates cancel to bring the graphene to the same potential as the source and drain. The slope of this curve gives the relative gating efficiency α for top and bottom gates:

$$\alpha = \left.\frac{\partial V_{g,top}}{\partial V_{g,bottom}}\right|_{\sigma_{min}} = -0.115$$

as shown in Figure 6-6(b). This can be compared with the expected value for α in the electrostatic gating approximation through the condition that the induced charge

n in the graphene is zero.

$$\begin{aligned} n_{g,top} + n_{g,bottom} = C_{g,top}V_{g,top} + C_{g,bottom}V_{g,bottom} = 0 \rightarrow \\ \alpha_e = \left.\frac{\partial V_{g,top}}{\partial V_{g,bottom}}\right|_{n=0} = -\frac{C_{g,bottom}}{C_{g,top}} \\ = \frac{3.453 \times 10^{-4}}{3.984 \times 10^{-3}} = -0.087 \end{aligned}$$

The discrepancy between α and α_e can be accounted for by a quantum capacitance correction β to the top gate capacitance in the manner discussed previously. The required value is

$$\beta = \frac{\alpha}{\alpha_e} = \frac{-0.115}{-0.087} = 1.32$$

This is essentially the value estimated for the mobility correction in the previous analysis. Though the expected value for β from Figure 6-2 is ~1.5 at zero charge density, the broadening effects of a nonuniform channel can account for this difference if the broadening function has a width of 0.5 to 1 V top gate equivalent. This is quite reasonable based upon the width of the minimum conductivity "plateau" observed for most devices.

6.2.2.2 Gate Voltage Series

If the measurements are plotted as series instead of as a map, as in Figure 6-7, two observations are readily made. First, the mobility of p-type and n-type carriers changes between series lines. And second, the minimum conductivity also varies between series lines, and indeed becomes a lower bound for the mobility. This latter result is quite surprising and will be explained shortly. For now, the former observation is addressed.

The one-gate mobility, which is the mobility calculated from varying one gate voltage while keeping the other gate voltage fixed, can be visualized in an easier manner by removing the offset of the Dirac point between series lines. This is done using the relation expressed in Figure 6-6(b), with the result presented in Figure 6-8.

It is observed that the top gate sweeps of Figure 6-8(a) are all coincident along

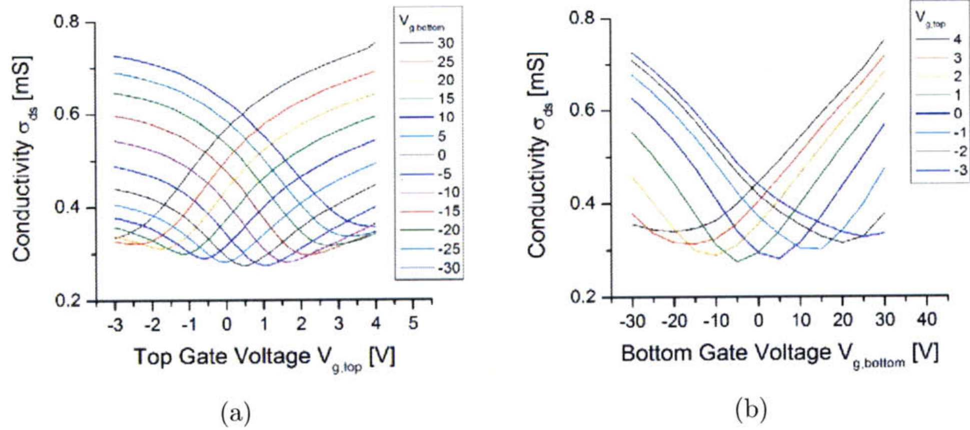


Figure 6-7: Top and bottom gate sweeps for the device of Figure 6-6. The data is the same but is plotted in an alternate manner to emphasize the varying mobility and varying minimum conductivity.

some portion of their domain with other sweeps. The regions of coincidence appear as high densities of parallel lines, and define a nearly-ideal V-shaped conduction curve. The choice of the bottom gate voltage affects how the top gate sweeps differ from this common conduction curve, manifested mainly as residual resistivities for p-type and n-type conduction which causes the conductivity to saturate at different values (and which also affects the mobility).

The bottom gate sweeps of Figure 6-8(b) manifest a somewhat different behaviour. The residual resistivity and mobility are relatively constant between top gate voltage series, but there is a broadening of the minimum conductivity region and a shift of the sweeps away from the Dirac point as the magnitude of the top gate voltage increases. This is indicative of the onset p-n junction formation in the graphene channel and adjacent to the metal contact. Though this behaviour is expected for devices where the top gate is shorter than the bottom gate, it is possible to achieve the same effect with top and bottom gates which cover the entire graphene channel. Because of the differing electrostatic capacitances and fringing pattern around the metal contacts, the top gate should be more effective at gating the graphene regions close to the metal contacts, though a finite element modeling of the field line distribution should be used to confirm this.

The mobility variations mentioned above may be quantified for both series of top

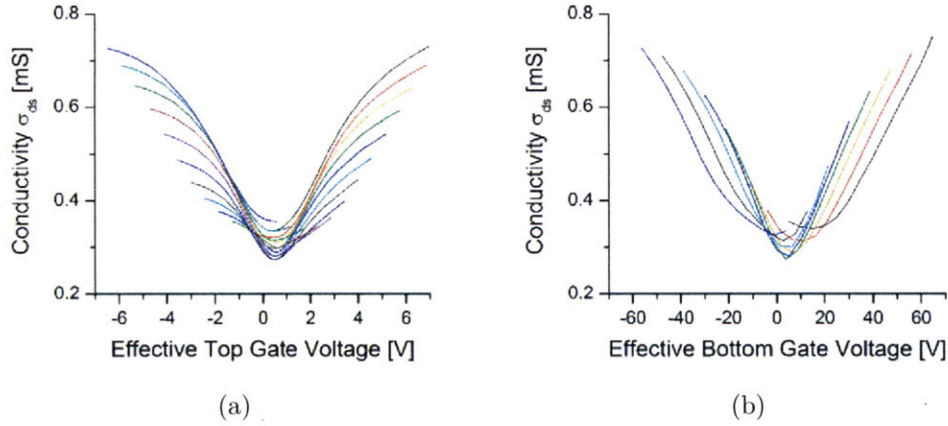


Figure 6-8: Gate sweeps for the device of Figure 6-6, with Dirac points offset to coincide. (a) Top gate sweeps at different bottom gate voltages, from -30 V at upper left to +30 V at upper right in steps of 5 V. The overlap of these sweeps defines a nearly-ideal V-shaped conduction curve. (b) Bottom gate sweeps at different top gate voltages, from -3 V at upper left to +4 V at upper right in steps of 1 V. The overlay is less perfect than in (a), and the lateral shifting is likely due to the formation of p-n junctions.

gate sweeps and bottom gate sweeps, as shown in Figure 6-9. Calculation of the mobility was performed according to Equation C.2, using the electrostatic bottom gate capacitance $C_{g,bottom} = 3.453 \times 10^{-4}$ F/m^2, and the top gate capacitance found from the Dirac point variation

$$C_{g,top} = \frac{C_{g,bottom}}{\alpha}\ , \ \alpha = 0.115 \tag{6.3}$$

where α is determined in Figure 6-6(b). What is unexpected is that, though a visual inspection appears to show the mobility saturating at a single value, there are instead peaks in the maximum mobility values as shown in Figure 6-9.

These peaks of mobility might correspond to the best tradeoff point between the mobility-reducing effects of charge inhomogeneities of the channel near the Dirac point and charge trapping in the oxide at high gate voltages. Oxide charge trap population can be identified as a precursor to electrical breakdown of the oxide, which is observed in these devices at higher gate voltages.

The magnitude of variation of mobility is also very different between top and

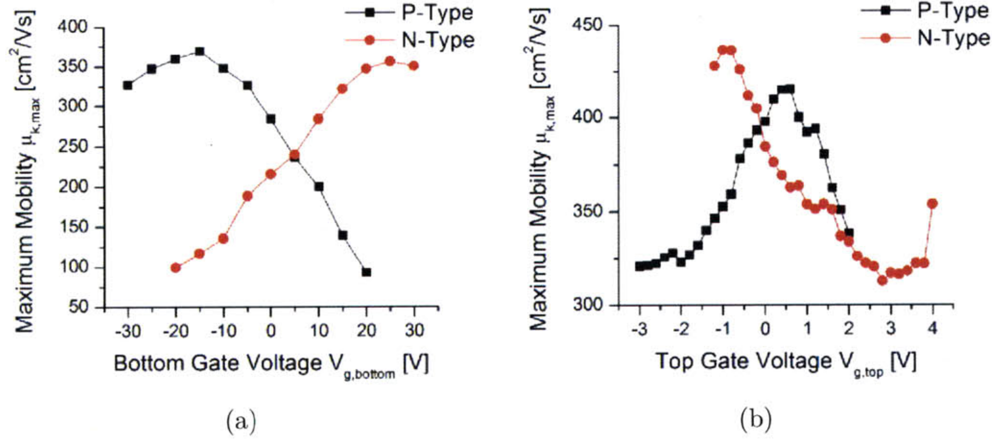


Figure 6-9: Maximum mobilities for each gate sweep in Figure 6-7/Figure 6-8. (a) Top gate sweep mobility dependence on the back gate voltage. (b) Bottom gate sweep mobility dependence on the top gate voltage.

bottom gate sweeps. For top gate sweeps the mobility varies widely, over nearly 80% of its range. For bottom gate sweeps, the mobility only varies about 30%. This is consistent with the obsrevations noted previously.

For both methods of gating, the peaks in the mobility maxima are offset from their crossing point near $V_g = 0$. This provides an interesting device behaviour, where the p-type and n-type mobility can be continuously tuned in a reciprocal manner. By varying the top gate voltage as in Figure 6-9(b), the bottom gate mobility can be tuned to differences of ~10% in a linear manner. The corresponding range shown in Figure 6-9(a) for tuning of top gate mobility is ~65%. This effect could concievably be used to create configurable logic gates out of graphene, though with the present material such designs would not be very efficient due to large minimum conductivity and relatively low mobilities. The origin of this difference is likely the region of overlap of charge densities induced by either gate, discussed below in Section 6.2.2.3.

Finally, it is notable that the mobilities are very different in magnitude for top versus bottom gating (370 vs. 440 cm^2/Vs, which is a difference of ~15%). This was an unexpected result, since the mobility should be independent of the method of measurement. It is uncertain how this should be reconciled, though a likely candidate is the choice of α. Indeed, there is some indication that there is a second diagonal in Figure 6-6(a), the cause of which is unknown but which manifests as a slight shift in

the data points of Figure 6-6(b) around zero gate voltage.

The other likely explanation concerns the graphene-dielectric interface. When the top gate is varied, the induced charges reside primarily at the graphene/HfO_2 interface due to the screening effects of graphene layers. Since it has been argued that this interface is more defective than the graphene/SiO_2 interface, there should be more scattering leading to a lower mobility.

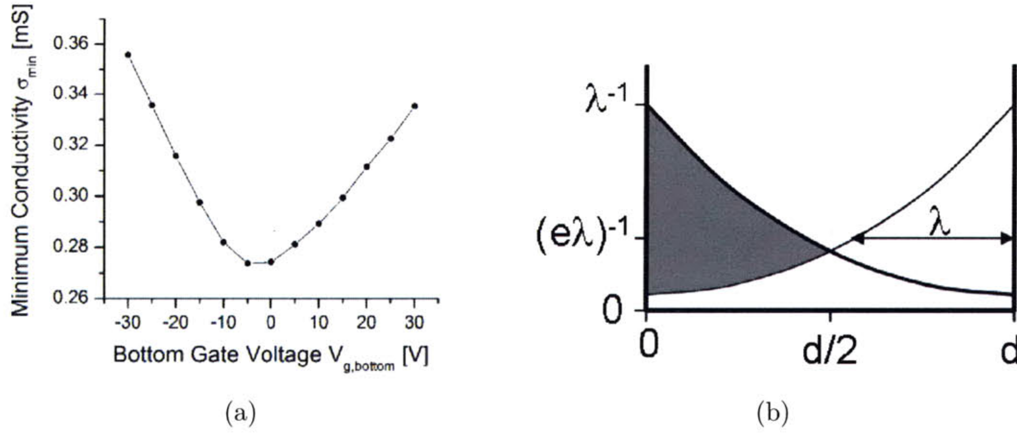
6.2.2.3 Dirac Point Conductivity and Graphene Thickness Estimation

The previous sections suggest that screening plays an active role in the CVD graphene devices under study, spatially separating the charges induced by top and bottom gates and leading to their asymmetric behaviour. It will here be shown that this screening can be used to explain the variation of the Dirac point conductivity.

The Dirac point conductivity was noted in Section 6.2.2.2 to vary with the applied gate voltage. This dependence is shown in greater detail in Figure 6-10(a). It is seen to have a V-shaped behaviour, with a linear variation in the conductivity at large positive and negative gate voltages. These linear regions are connected by a rounded minimum, just as the other conductivity curves discussed previously. This rounding at the minimum, as well as the large offset of the conductivity from zero, are attributed to charge inhomogeneities and to multilayer transport.

The interesting behaviour is the linear variation, which occurs with a slope of 4.0×10^{-3} [mS/V] for negative bottom gate voltages and a slope of 2.4×10^{-3} [mS/V] for positive bottom gate voltages. These slopes could be converted to mobilities if the correct charge density were known. This quantity is found as follows.

At the Dirac point, the top and bottom gates induce equal but opposite charge densities in the graphene. But because of screening, these induced charges are separated on opposite sides of the graphene. Here it is assumed that the graphene is more than one layer thick, and may be treated as a continuous medium. Thus, one half of the graphene will transport holes, and the other half will transport electrons. The total amount of charge which contributes to transport will depend on the specific distribution of charges in the channel.



(a) (b)

Figure 6-10: (a) Minimum conductivity corresponding to each point in Figure 6-6(b). There is linear variation on either side of the global minimum. (b) Electric field screening in graphene. The thickness of the graphene is d, and the screening length is λ. Curves represent the electric field magnitude (proportional to the induced charge) for the two gates, one at left and one at right, with equal initial electric field magnitudes. At the Dirac point, the fields will induce opposite charges. The shaded area represents the amount of net charge induced near the left gate.

It is assumed that graphene, being treated as a continuous medium, has a screening length λ_s over which the incident normal electric field is attenuated, and that the form of this attenuation is exponential (Figure 6-10(b)). That is, the magnitude of the electric field E as a function of depth x into the graphene from the interface near the inducing gate is given by

$$E(x) = E_0 e^{-x/\lambda_s}. \tag{6.4}$$

It is noted that the induced volume charge density $\rho(x)$ and total induced areal charge density $n(x)$ are given by

$$\rho(x) = -\epsilon_0 \kappa \frac{d}{dx} E(x) \tag{6.5}$$

$$n(x) = \int_0^x \rho(x')dx' = \epsilon_0 \kappa \left(E(0) - E(x)\right) = \epsilon_0 \kappa E_0 \left(1 - e^{-x/\lambda_s}\right). \tag{6.6}$$

It is useful to denote the total charge induced by the complete screening of field E_0 by $n_0 \equiv n(\infty) = \epsilon_0 \kappa E_0$.

For two gates acting in equal and opposite manners, there are two electric fields

of interest. For a graphene thickness d, $E(x)$ and $-E(d-x)$ from the two gates must be summed to give the net electric field throughout the graphene. At the center the fields will cancel, but to either side, the difference between the field magnitudes will leave a net field, indicated by the gray area in Figure 6-10. Considering just one half of the graphene, from $x=0$ to $x=d/2$, the charge due to the left gate is $n(d/2)$ and the charge removed by the right gate is $n(d)-n(d/2)$. Thus it is found that the total charge induced on one side of the gate n_s is given by

$$\begin{aligned} n_s &= n(d/2) - (n(d) - n(d/2)) = 2n(d/2) - n(d) \\ &= n_0 \left[2\left(1 - e^{-d/2\lambda_s}\right) - \left(1 - e^{-d/\lambda_s}\right)\right] \\ &= n_0 \left[1 - 2e^{-d/2\lambda_s} + e^{-d/\lambda_s}\right] \\ &= n_0 \left[1 - e^{-d/2\lambda_s}\right]^2 \\ \frac{n_s}{n_0} &= \left[1 - e^{-d/2\lambda_s}\right]^2. \end{aligned} \tag{6.7}$$

Equation 6.7 may be inverted to express the normalized thickness d/λ_s in terms of the charge fraction n_s/n_0 as

$$\frac{d}{\lambda_s} = -2\ln\left(1 - \left(\frac{n_s}{n_0}\right)^{-\frac{1}{2}}\right). \tag{6.8}$$

However, the quantity n_0 is slightly artificial since in thin graphene the electric field will never be fully screened. A more natural quantity is $n_d = n(d)$, the total charge which can be induced by the left gate when there is no contribution from the right gate:

$$\begin{aligned} n_d &= n(d) = n_0\left(1 - e^{-d/\lambda_s}\right) \\ n_0 &= \frac{n_d}{1 - e^{-d/\lambda_s}}. \end{aligned} \tag{6.9}$$

This can be substituted into Equation 6.7 to obtain

$$n_s = \frac{n_d}{1 - e^{-d/\lambda_s}}\left[1 - e^{-d/2\lambda_s}\right]^2$$

$$
\begin{aligned}
\frac{n_s}{n_d} &= \frac{\left[1 - e^{-d/2\lambda_s}\right]^2}{1 - e^{-d/\lambda_s}} \frac{e^{d/2\lambda_s}}{e^{d/2\lambda_s}} \\
\frac{n_s}{n_d} &= \frac{\left[e^{-d/4\lambda_s} - e^{-d/4\lambda_s}\right]^2}{e^{-d/2\lambda_s} - e^{-d/2\lambda_s}} \\
\frac{n_s}{n_d} &= \frac{2^2 \sinh^2(d/4\lambda_s)}{2 \sinh(d/2\lambda_s)} \\
\frac{n_s}{n_d} &= \frac{\cosh(d/2\lambda_s) - 1}{\sinh(d/2\lambda_s)}.
\end{aligned} \tag{6.10}
$$

This is a transcendental equation, which can be solved graphically as shown in Figure 6-11. As could have been deduced from a Taylor expansion of the right hand terms in Equation 6.10, the expression for n_s/n_d is linear up to $d/\lambda_s \approx 2$ and achieves an asymptotic value of 1 above $d/\lambda_s \approx 6$ (each to within ~10%). The inital slope is exactly $\frac{1}{4}$.

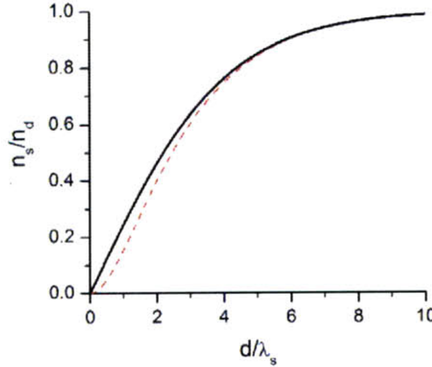


Figure 6-11: Plot of Equation 6.10 (solid black line) and Equation 6.7 (dashed red line, with $n_d = n_0$) for the relation between the fractional induced charge n_s/n_d and the normalized graphene thickness d/λ_s. The initial slope for the solid curve is $\frac{1}{4}$. The asymptote at large normalized thickness for both curves is 1.

It is now possible to make an estimate of n_s/n_d from the conductivity data in order to estimate the thickness of the graphene material, with the expectation that this value will match independent observations.

To begin, an assumption is made that the mobility of the charge carriers in the graphene is independent of the charge carrier density. Thus, at a conductivity minimum where equal and opposite charge densities are induced by the two gates, the net charge n_s remaining in the channel has the same mobility as when both gates

induce charge cooperatively, and give the high mobility values seen in Figure 6-9. In other words, the reason that the mobility calculated from an anti-balanced gate sweep like Figure 6-10(a) is different from the mobility calculated from normal single-gate sweeps like Figure 6-7(b) is that there are fewer carriers by excactly the factor given in Equation 6.10.

With this assumption, the charge density n is related to the transconductance g as follows, where the subscript m refers to measurement along the line of minimum conductivity, and subscript n refers to measurement in the normal single-gated manner. First, the constant mobility can be related to the two transconductances by a gate capacitance

$$\mu = \frac{1}{C_{g,bottom,eff}} \frac{\sigma_{ds,m}}{V_{g,bottom}} = \frac{g_m}{C_{g,bottom,eff}}$$
$$\mu = \frac{g_n}{C_{g,bottom}}$$

where the effective gate capacitance $C_{g,bottom,eff}$ is introduced to account for the charge cancellation discussed above. The gate capacitance is of course related to the charge density

$$n_m = C_{g,bottom,eff} V_{g,bottom}$$
$$n_n = C_{g,bottom} V_{g,bottom}$$

which leads to the conclusion that

$$\frac{g_m}{C_{g,bottom,eff}} = \frac{g_n}{C_{g,bottom}}$$
$$\frac{g_m}{n_m} = \frac{g_n}{n_n}$$

The total charge contributing to conduction along the line of minimum conductivity in terms of the previous analysis is $n_m = 2n_s$, since there are two sides (gates) involved. Similarly, the identification is made that $n_n = n_d$, since the top gate voltage can be fixed at zero so that it induces no charge in the graphene. This allows the

experimental determination of

$$\frac{n_s}{n_d} = \frac{n_m/2}{n_n} = \frac{1}{2}\frac{g_m}{g_n}. \tag{6.11}$$

The transconductance g_m was mentioned previously as 4.0×10^{-3} and 2.4×10^{-3} [mS/V] for negative and positive bottom gate voltages, respectively. The corresponding values for g_n can be estimated directly from the gate sweeps (Figure 6-7(b)) or from knowledge of the bottom gate capacitance and the bottom gate mobilities (Figure 6-9(b)). Taking this latter method, the mobilities for negative and positive bottom gate voltages are equal at $V_{g,top} \approx 0$ V with a value of 395 cm^2/Vs, giving a transconductance with respect to the bottom gate of $g_n = (395 \times 10^{-4}[\text{m}^2/\text{Vs}])(3.453 \times 10^{-4}[\text{F/m}^2])(1 \times 10^3 \text{mS/S}) = 13.64 \times 10^{-3} \text{mS/V}$. Using this value with the maximum value of g_m gives a value of $g_n/g_m = 3.41$ and thus

$$\frac{n_s}{n_d} = \frac{1}{2}\frac{g_m}{g_n} = \frac{1}{2}\frac{1}{3.41} = 0.147.$$

Because the value for n_s/n_d is so small, the linear approximation holds (Figure 6-10) yielding a normalized thickness of

$$\frac{d}{\lambda_s} = 4\frac{n_s}{n_d} = 4 \times 0.147 = 0.59.$$

It is concluded that nearly 55% of the electric field coming from the gate does not induce charge in the graphene but instead passes right through it, since the graphene thickness is only a fraction of the screening length. This value is significant, and serves to emphasize the importance of taking into account the thickness of graphene materials in device design and testing. Indeed, this suggests that the mobility values reported using conventional capacitance models (nearly universal in the literature) underestimate the mobility by a factor of two or more (this refers to the mobility per carrier in the graphene; the mobility per carrier in the gate remains unchanged, and it may be argued that this is the more important quantity for device characterization since it determines the charging rate of the gate). This view is supported by electro-

static force microscopy (EFM), where it is seen that the electric field penetrating the graphene depends on the graphene thickness [94]. One way to resolve this would be Hall measurements to independently determine the charge density in the graphene.

The thickness of the graphene determined by this method is dependent on the screening length λ_s. Multiple values have been reported ranging from 0.4 ([72], used in Section 5.4.2) to 1.2 [75], with a common consensus of 0.6 [95]. This gives a range of thicknesses $d = 0.59\lambda_s = 0.24$ to 0.71 nm with the consensus value of $d = 0.35$ nm. The interlayer spacing in graphene is ~0.34 nm, so the measured films are estimated to be 1-2 layers thick. The additional consideration that single-layer graphene cannot be treated in this manner leads to the conclusion that the CVD graphene must be 2 layers thick. This is exactly the range of film thickness (few-layer graphene, 1-3 layers) which comprises 85% of the CVD graphene area [40].

This result points to the above method as an easy way to use top and bottom gate conductance measurements to check the thickness of a graphene film, or as a first estimation in the absensce of Raman or AFM measurements. There are a number of comments to be made regarding this method.

First, it was found that a similar approach had been employed by Miyazaki *et. al.* [75]. The above analysis takes the approach of treating the top and bottom gates symmetrically, while Miyazaki treats them asymmetrically, holding one fixed while varying the other. The conductivity minima which are tracked are thus different in the two analyses, though the amount of this difference is small for thin films such as those considered here (compare the non-alignment of the minima in Figure 6-8). Furthermore, the amount of this variation can be related to the transconductance of the conductivity minimum and to the curvature of the conductivity minimum, which is inversely related to the charge impurity doping. The final difference is that the two analyses calculate the variances of different quantities. More work is needed to illuminate the exact correspondence between these two approaches and to determine in what way they complement each other.

It has recently been demonstrated that top and bottom gating of bilayer graphene can open a bandgap, resulting in a minimum conductivity which exponentially decays

with increased gating [96], in contrast to the linear increase seen in this work. This is explained by considering the device size and impurity doping. For large impurity doping, the induced charge puddles have Fermi level shifts larger than the bandgap, and transport behaves as if the bandgap were not present. The effect of large devices is to allow larger-scale charge inhomogeneities, contributing to the charge inhomogeneity effect. Only at very large gate voltages where the induced bandgap overwhelms the magnitude of the charged impurity fluctuations does the bandgap manifest as an inversion of the "dirty" linear behaviour. The work of Oostinga *et. al.* [96] demonstrated a bandgap in a small device (~200 nm gate length) with low impurity concentration. However, the phenomenon was demonstrated in micron-sized devices in the work of Miyazaki *et. al.* [75] in Figure 3, where at low gate voltages the linear behaviour is observed, giving way to the bandgap opening at very large gate voltages. In a similar manner, the devices studied here, being 5-10 μm in size and measured only in a low gate voltage range, demonstrate the linear behaviour.

The question may be raised whether the continuum model of few-layer graphene films is appropriate, since in this region the energy bands of graphene change significantly with the number of layers. It is noted that though the band structure changes, the density of states still varies linearly around the conductivity minimum with an effective density of states equal to that of single layer graphene (see Chapter 5). This view is supported by EFM measurements in commensurate graphene [94] and by conductivity measurements in incommensurate graphene [76]. The latter case applies to the CVD graphene considered here, as supported by Raman measurements [39].

The model presented does not account for the differing transconductances of the minimum conductivity point at positive and negative gate voltages. This difference, shown by the differing slopes in Figure 6-10(a), shows that when electrons are induced near the back gate, the conductivity per charge carrier is increased or the amount of charge induced is lower than expected. This behaviour is seen for each of two devices analyzed in this manner, and is concluded to be a real effect. One possible explanation is that the graphene/oxide interfaces scatter electrons and holes differently, though it is not clear what scattering mechanism might cause this. Another possibility is

that charge traps at the interfaces might trap only one type of charge carrier. If the traps are located mainly at the top interface (supported by the decreased top gate mobility), the traps would have to hold holes and be populated in proportion to the top gate voltage. This would also result in a kink in the locations of the conductivity minima in Figure 6-6(b), which is not observed. Thus the true explanation remains an open question.

An alternative explanation of the variation of minimum conductivity with gate voltage relies not on screening between layers but on the fringe effects of gating near the contacts. Because of the differing thicknesses and dielectric constants of the top and bottom oxides, the electrostatic profile of the top and bottom contacts is expected to be different in the vicinity of the metal gates, at which the potential is fixed. Thus, while the bulk of the graphene channel may be gated equally and oppositely by the top and bottom gate leading to the conductivity minimum, the area near the contacts may be dominated by the field from the top gate, leading to an increase in conductivity for that region which is dependent on the gate voltage. If this is the case, the transconductance of the conductivity minimum should be related to the mobility of the graphene by a geometric factor. This appears to not be the case for the two devices analyzed in this manner, though further analysis will be necessary to conclusively determine this.

6.2.2.4 Converted Charge Coordinates

Following from the previous section, it is noticed that the behaviour of the conductivity of a graphene device is dependent primarily on the net charge density of the graphene, which in a dual-gated device can be calculated as a combination of the top and bottom gate voltages using factors specific to the surrounding dielectric and the device geometry, which are contstant for a given device. With this in mind one can define another set of variables against which it is more instructive to plot the data:

$$\Sigma = \frac{1}{2}\left(n_{top} + n_{bottom}\right) = \frac{1}{2}\left(C_{g,top}V_{g,top} + C_{g,bottom}V_{g,bottom}\right) \tag{6.12a}$$

$$\Delta = \frac{1}{2}\left(n_{top} - n_{bottom}\right) = \frac{1}{2}\left(C_{g,top}V_{g,top} - C_{g,bottom}V_{g,bottom}\right) \tag{6.12b}$$

$$V_{g,top} = \frac{1}{C_{g,top}} (\Sigma + \Delta) \tag{6.13a}$$

$$V_{g,bottom} = \frac{1}{C_{g,bottom}} (\Sigma - \Delta) . \tag{6.13b}$$

Here Σ is the average charge density of one side of a multilayer graphene sheet, and Δ $(-\Delta)$ is the deviation from Σ of the charge density of the top (bottom) sheet. An illustration of this dependence is shown in Figure 6-12. This is especially useful because of the electronic screening between layers which tends to decouple the charge densities of the opposite sides. The total charge induced at the conductivity minimum as discussed above in Section 6.2.2.3 is thus given by 2Δ, and these coordinates are a natural system for discussing the behaviour of the conductivity minimum.

--	-	0	+	++
--	-	0	+	++
Σ = -2 Δ = 0	Σ = -1 Δ = 0	Σ = 0 Δ = 0	Σ = 1 Δ = 0	Σ = 2 Δ = 0

(a)

++	+	0	-	--
--	-	0	+	++
Σ = 0 Δ = 2	Σ = 0 Δ = 1	Σ = 0 Δ = 0	Σ = 0 Δ = -1	Σ = 0 Δ = -2

(b)

Figure 6-12: New potential coordinates related to top and bottom gate voltages. (a) The variable Σ is the effective net potential of the multilayer graphene sheet, and varies as the sum of the two gate voltages. (b) The variable Δ is the effective potential difference between the top and bottom graphene layers, and varies as the difference of the two gate voltages. By convention, positive Δ corresponds to a more positive top gate voltage.

To see this, it is noted that an electric field is continuously attenuated when passing through multilayer graphene, giving rise to a charge density which varies between layers through Gauss's Law

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\epsilon} \tag{6.14}$$

$$\frac{d|\vec{E}|}{dh} = \frac{\rho(h)}{\epsilon} \tag{6.15}$$

$$d|\vec{E}| = \frac{\rho(h)\, dh}{\epsilon} = \frac{dn(h)}{\epsilon} \tag{6.16}$$

where the latter relations are appropriate for the parallel-plate approximation which

is valid for most graphene devices (including the ones under consideration here). The variable h is the spatial distance along the direction of the electric field $\vec{E}$ (perpendicular to the graphene plane), and n is the areal charge density.

Classically this effect leads to a "skin depth" over which the perpendicular electric field impinging on a conductor is attenuated. Graphene however can be thinner than the skin depth, so that an impinging electric field induces charge in all layers, and leaves the material with a reduced amplitude. This partial screening of graphene has been documented experimentally [76], and is taken as a general assumption in the more complete theoretical treatments of graphene and graphite electrostatics (e.g. under light interference conditions [37], for calculation of inter-layer screening [75], and for determination of the gating efficiency α [72]).

Any combination of charge densities induced in the graphene $\{n_t,n_b\}$ may be decomposed into the new charge coordinates $\{\Sigma,\Delta\}$. This is done for the device of Figure 6-6 with results shown in Figure 6-13. The conversion makes use of the electrostatic bottom gate capacitance $C_{g,bottom}$ (a good approximation to the total capacitance according to Figure 6-2), and a top gate capacitance found using Equation 6.3. It also re-centers the graph around the global conductivity minimum at $V_{g,top} = 0.8$ V and $V_{g,bottom} = -2.75$ V. The new conductivity values are obtained as a cubic interpolant of the original data, and are plotted with a higher resolution to better visualize the underlying variations. The graphene is assumed to completely screen the gate voltages in order to simplify the analysis, though this constraint should be removed in future analyses in light of the results of Section 6.2.2.3.

Using these new coordinates, the lines of constant Σ correspond to constant total charge carrier density. The conductivity as a function of Σ is shown in Figure 6-14 at various Δ, corresponding to horizontal lines in Figure 6-13.

The variation between sweeps reiterates the results seen previously in the discussion of offset top gate sweeps in Section 6.2.2.2 (Figure 6-8(a)). Namely, the mobility varies strongly as a function of the charge difference between top and bottom gates, with the most noticeable change occurring when Σ and Δ have the same sign. This corresponds to the top gate being more highly doped than the bottom gate, so that

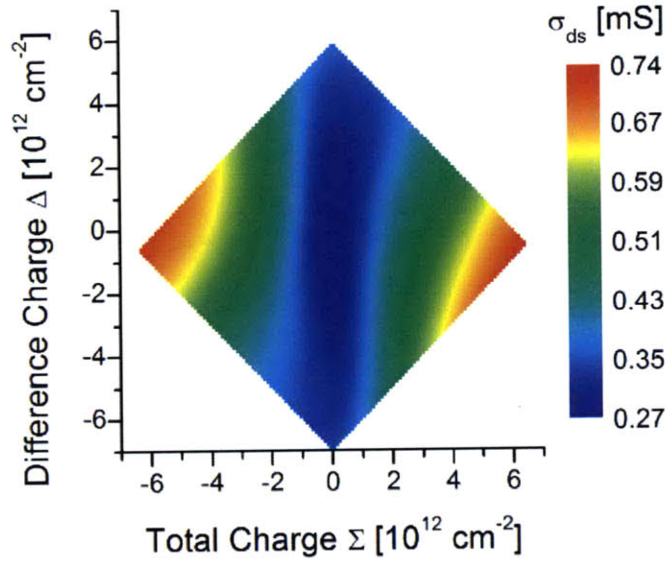


Figure 6-13: Conductivity dependence on average charge densities Σ and Δ for the device of Figure 6-6. It is principally the total charge density Σ which modulates the Fermi level of the graphene, while the difference charge density Δ modulates the asymmetry between electron and hole conduction.

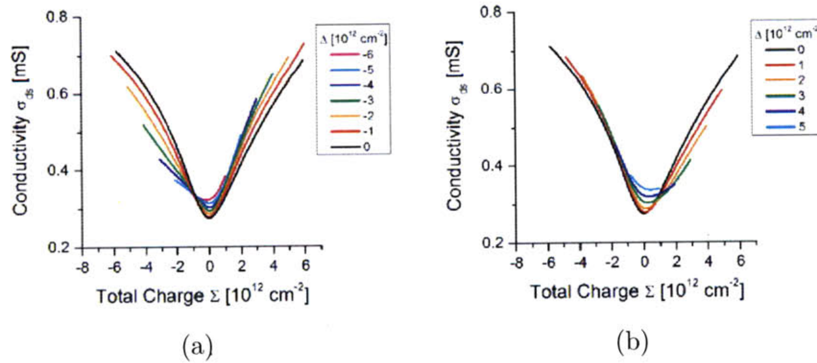
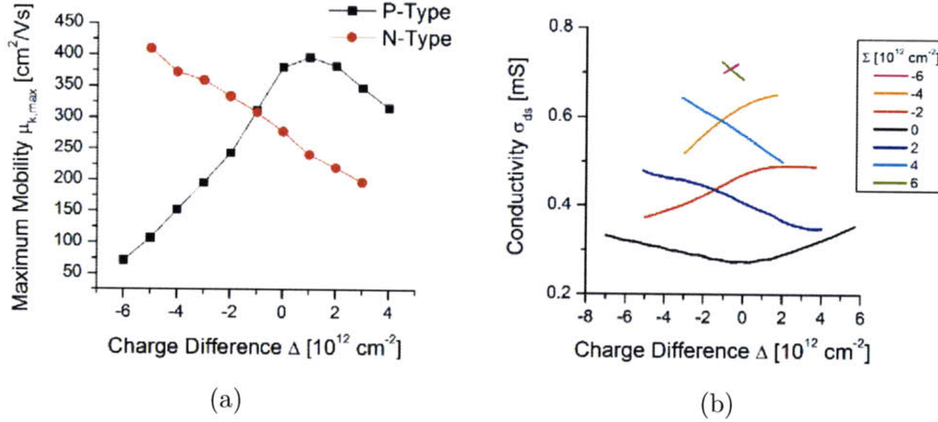


Figure 6-14: Conductivity as a function of the total charge coordinate Σ for (a) $\Delta \leq 0$ and (b) $\Delta \geq 0$. A clear variation of the mobility is seen without noticeable alteration of the saturation behaviour.

the mobility decrease might be linked to the graphene/HfO_2 interface. However, the saturation variation which was seen in the top gate sweeps is not noticeably present in the Σ sweeps. The variation of the mobility is shown quantitatively in Figure 6-15(a).



(a) (b)

Figure 6-15: (a) Maximum mobility upon variation of total charge Σ as a function of the differential charge Δ. (b) Conductivity as a function of the differential charge Δ at various Σ. The curve for $\Sigma = 0$ reproduces the minimum conductivity curve of Figure 6-10(a).

The variation of the charge mobility over the available range appears most similar to the mobility calculated from the variation of the top gate voltage, as seen in Figure 6-9(a). Both the range and the magnitude of the mobilities are more similar than for the variation of the bottom gate voltages of Figure 6-9(a). The p-type and n-type mobility curves are roughly mirror images of each other around $\Delta = -1$, which is expected from the antisymmetry of the charge densities in the definition of Δ in Equation 6.12b (though from the definition of Δ, the symmetry point is predicted to be $\Delta = 0$, not -1). The large variation of mobility with Δ is due to the formation of p-n junctions, which increase the resistance and therefore decrease the mobility, when there is an excess of induced charge in the graphene on the side near the top gate. The n-type mobility varies at a noticeably smaller rate (slightly more than two times smaller) than the p-type mobility. The cause of this variation is unknown, but might be related to the asymmetry in the transconductance of the minimum conductivity that was noted previously in Section 6.2.2.3.

The variation of the conductivity with Δ for fixed values of Σ is shown in Figure 6-

15(b). These series correspond to vertical lines in Figure 6-13. The line for $\Sigma = 0$ precisely reproduces the minimum conductivity trace of Figure 6-10(a). The other lines illustrate a conductivity decrease as one of the gate voltages approaches zero.

In summary, this method decomposes the conductance of a top and bottom gated device into its most orthogonal behaviour, and should serve as a starting point for future analysis. Refinements to this method should include accounting for the screening length in the graphene (for multilayer graphene) and the possibility of charge traps.

6.3 Hall Bar Devices

Eleven devices in a 6-terminal Hall bar geometry were tested using the methods described in Section 6.1.2. The devices are from two wafers, at three different stages of annealing. The annealings were performed to remove chemical and adsorbate doping of the graphene, shifting the Dirac point into the range of gate voltages probed, though this was not always successful. The doping stages were undoped, after a first anneal of 20 minutes of annealing at 400 °C in a 90:10 mixture of N_2:H_2, and after a second annealing under identical conditions as the first annealing. Though these devices had no top gate, they were still covered by the HfO_2 dielectric layer.

6.3.1 Cross Measurements

A typical device is shown in Figure 6-16(a), with the junction being probed circled in green. The results of a measurement on this device are shown in Figure 6-16(b). The four measurements which were averaged to give $R_{vertical}$ and $R_{horizontal}$ were identical to within the noise uncertainty. These two averages, however, differ by up to a factor of two, emphasizing the inhomogeneity of the device. This is most likely due to the left contact being quite close to the junction (distance from the junction $<$ graphene width) or the multilayer graphene regions which approach the junction from the top and bottom contacts. The computed average sheet resistance is calculated using Equation 6.1.

In total, six devices with a total of nine active junctions were probed in this man-

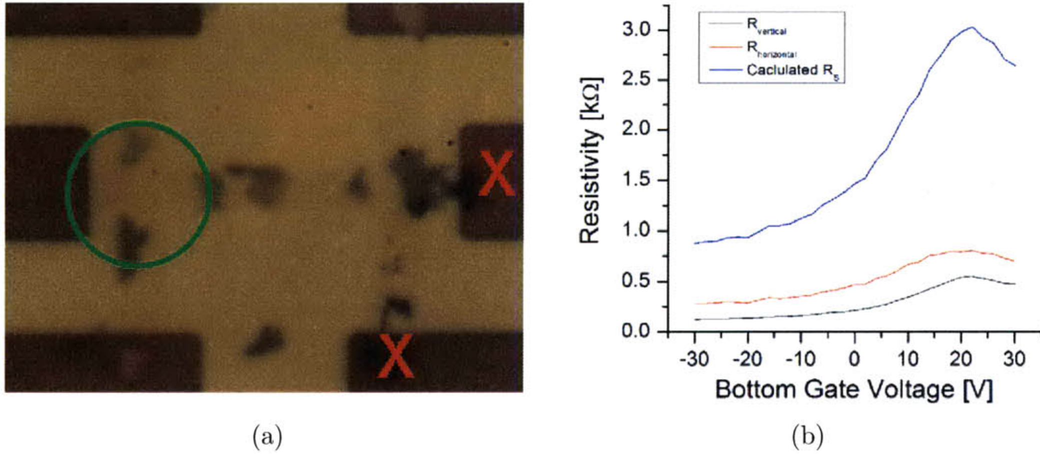


Figure 6-16: Van der Pauw cross measurements on a Hall bar geometry device. (a) Image of a typical device. Few-layer graphene is slightly darker than the tan background, while thicker regions of graphene appear as dark splotches. Metal contacts to the graphene are the dark rectangles at left, right, and the diagonals. Width of graphene lines is 5 μm. Red X's mark nonfunctional contacts, accompanied by dark spots on the graphene where damage occured to the device. Green circle indicates the region being measured. (b) Measurement of the sheet resistivity R_S according to the method of Section 6.1.2. Maximum mobility is 690 cm^2/Vs.

ner. The remaining three junctions were inaccessible because one or more contacts was open, as for the right junction of Figure 6-16(a). The device shown in Figure 6-16 was atypical in that it showed a clear Dirac point where the sheet resistance is a maximum. The remaining devices had a Dirac point which was shifted above the maximum gate voltage of the sweeps (+30 V). One device with two active junctions showed a factor of 3 modulation in the sheet resistance while the Dirac point was still above the maximum gate voltage, but the other devices showed a modulation of a factor of 1 or less, indicating extreme right shifting of the Dirac point. The mobility was calculated from the sheet resistance and is shown in Table 6.2.

Several observations can be made. First, the mobilities of the devices with 10 μm width are generally low, and the sheet resistance shows poor modulation (0.5$\times$ is the maximum, for device 3-L). This is likely due to the nearby presence of the right or left contact, which may unintentionally dope the junction since the distance of the contact from the junction is much less than (~1/4) the width of the graphene. Future device designs should incorporate much longer graphene leads.

Device-Junction	W [μm]	L [μm]	1st Ann. [cm^2/Vs]	2nd Ann. [cm^2/Vs]	Comments
1-L	5	5	*†1690	250	
2-R	5	5		450	
3-L	10	5		700	
3-R	10	5		230	
4-L	5	5	†800	†1020	3× modulation (1st & 2nd)
4-R	5	5	†1500	300	2× modulation (1)
5-L	5	5	†690	†730	Dirac peak visible
6-L	10	5		300	
6-R	10	5		210	
* Before 1st anneal † Likely the maximum mobility					

Table 6.2: Mobility for cross measurements on nine junctions in six devices after first and second anneal. Junction designation refers to the left (L) or right (R) juntion of a 6-terminal Hall bar device. Width (W) and length (L) specify the dimensions of the rectangular junction area. Entries lacking the † identifier do not show a resitance peak due to extreme shifting of the Dirac point.

Second, the effect of additional annealing is generally detrimental, increasing the mobility for two devices by a maximum of ~20%, but decreasing the mobility for two devices by a minimum of ~80%. The form of this decrease is in the doping of the graphene so that the Dirac point lies well above the gaté voltage range. A possible mechanism for this is the failure of the overlying HfO_2 layer by pinholes or cracks due to thermal cycling, which allows air to penetrate to the graphene layer and dope it. However, for the two devices that did not experience this failure, the mobility is slightly increased, indicating that annealing might eventually be a beneficial processing step if the failure rate can be overcome.

Third, the mobility values for the four cross regions attaining maximum mobility give an estimation of mobility for the CVD graphene as 1240 ± 440 cm^2/Vs. This average is three times the average bottom-gated mobility, and the individual values span the highest range observed among two-terminal devices. This is a significant result, indicating that the Van der Pauw method of measurement gives much more accurate mobilities, and that contact effects are significant in the measurement of two-terminal devices. A further study of interest in this regard would be the analysis

of the residual resistance of Van der Pauw and two-terminal devices after the method of Chapter 5 to verify that the larger resistance is seen in two-terminal devices. If such a resistance effect is absent, the mobility change is likely due to contact-induced states in the graphene, which can penetrate into the graphene layer by a distance equal to the graphene width.

6.3.2 Linear Measurements

A typical device is shown in Figure 6-17(a). This is the same type of device used for the cross measurements above, but the region in which transport is measured is the linear section of graphene between the two junctions. The results of a measurement on this device are shown in Figure 6-17(b). The measurement applies a current between left and right electrodes and measures the voltage at the four upper and lower electrodes. The upper and lower left electrodes are found to read the same potential, as are the upper and lower right electrodes. The three regions of graphene through which the current travels are designated as Lead 1 for the section between the left contact and the left vertical stripe of graphene, the Center region for the section between the left and right vertical stripes of graphene, and Lead 2 for the section between the right vertical stripe of graphene and the right contact. The total device refers to all three regions combined, that is, to the horizontal line of graphene between left and right contacts.

What is surprising in this measurement is that the resistance peak appears not for the center region but for one of the lead regions. This indicates that doping may vary widely across the channel, or more likely that the leads are doped by the metal contacts, altering the Fermi level for a small region of graphene. The resistance peak occurs in Lead 1 (source) in two devices and in Lead 2 (drain) in one device; all other resistance measurements for lead and center show a monotonic character similar to the Center and Lead 1 lines in Figure 6-17(b). This indicates that the Dirac point lies above the maximum gate voltage, and that the reported mobilities are to be interpreted as minimum values. In total nine devices were measured in this manner, with results presented in Table 6.3.

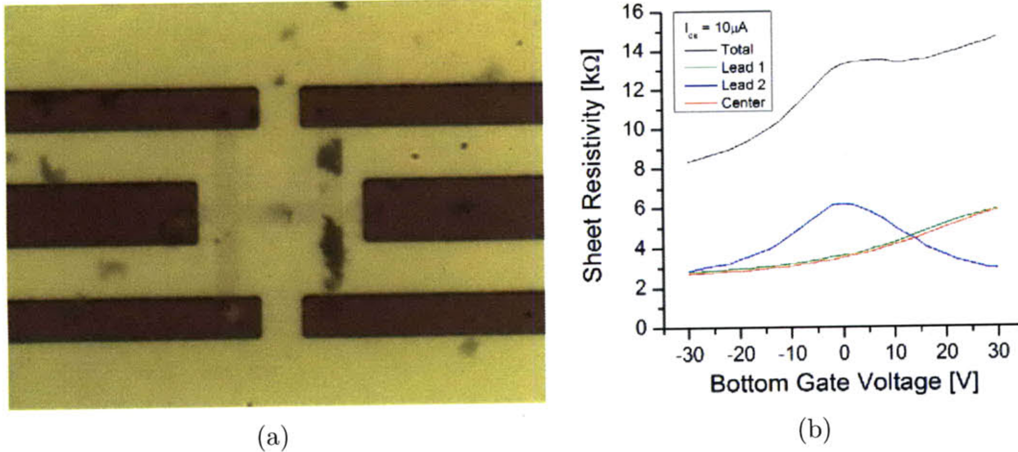


Figure 6-17: Linear four-point measurements on a Hall bar geometry device. (a) Image of a typical device. Width of the graphene lines is 5 μm. (b) Measurement of the sheet resistivity R_S according to the method of Section 6.1.2. The maximum mobility for the center region is 700 cm^2/Vs.

The reliability of a mobility value is judged by the shape of the resistance curve. Since no resistance peaks indicating the Dirac point are visible, the high-resistance end of the curve is judged for linearity. If the curve appears to be linear or nearly so, this is taken as a reliable measurement, since the linear section of the curve marks the inversion of curvature as the slope (proportional to the mobility) decreases toward the peak at the Dirac point, at which the slope is zero.

The two devices with reliable measurements have mobilities on par with the average value noted above for the cross devices. An additional device (3) shows a mobility of at least this high (1300 cm^2/Vs), though the true value is expected to be higher. This indicates that the cross and linear measurements are comparable in the values they produce.

An interesting comparison between cross and linear measurements can be made with Device 4. Measurements after the first anneal indicate that the linear mobility is in the midrange between the cross mobilities, indicating that the linear region, which contains both junctions (at its endpoints), might be thought of as producing a measurement which is a weighted combination of the response of each subregion that comprises it. More interestingly, after the second anneal the right cross mobility is significantly reduced (Dirac point is significantly upshifted), while the linear mobility

Device-Junction	W [μm]	L [μm]	No Ann. [μm]	1st Ann. [cm^2/Vs]	2nd Ann. [cm^2/Vs]	Ratio R_{max}/R_{min}
1	5	25	†1300	†700		3.0, 2.1
2	5	35			900	1.6
3	10	35			1300	1.4
4	5	25		1100	†1250	2.9, 3.7
6	10	35			600	1.7
7	5	25	750			1.5
8	5	35	670			1.7
9	10	35	650			1.6
10	5	35	800			1.8
† Likely the maximum mobility						

Table 6.3: Mobility for linear measurements on nine devices before annealing and after first and second anneal. Devices 1-6 are the same as in Table 6.2. Width (W) and length (L) specify the dimensions of the central graphene region. No entry shows a clear resistance peak, but entries displaying the † identifier are estimated to be close to the true value because the Dirac point is approaching the gate voltage range. The R_{max}/R_{min} ratio gives the modulation over the measurement gate voltage range, and is inversely related to the magnitude of the shift of the Dirac point voltage.

is not significantly changed (it even increases). This indicates that the mobility degradation occurred within the cross junction itself, not through any extended region of graphene. The cause and extend of this local mobility degradation, possibly due to localized defects in the oxide, would be an interesting subject for future study.

Devices 3 and 6 after the second anneal show linear mobilities which are greater than the mobilities of the cross regions by about a factor of 2. This might be explained in part by the width of these devices, which is greater than the distance from the contact to the junction, indicating that the cross measurement can be affected by contact induced states. Device 2 also exhibits this behaviour, though only one cross could be measured. Thus for the specific geometry of these devices, the linear measurement is preferable because the greater portion of the channel over which transport is averaged is far from the contacts. However, for an optimized geometry it is the cross measurements which are expected to give the largest mobility values, because over the smaller junction regions inhomogeneities are minimized. Indeed, the highest mobilities in the present measurements are from the cross geometry.

The remaining devices 7-10 were from a separate wafer that was unannealed. In these devices the Dirac point was strongly upshifted, highlighting the importance of the annealing step for downshifting the Dirac point, which was necessary for definitive measurements of device mobility of the other wafer. This annealing process is not perfect, however, because the Dirarc point should ideally be brought to near zero gate voltage. The two-terminal devices presented in Section 6.2 show a different behaviour, with nearly 65% of the devices measured showing a Dirac point within the gating range. By contrast, only one cross device of the nine measured showed a Dirac point within the gating range. Clearly something is different between all these two types of devices.

Two candidate explanations for this difference in Dirac point shift are as follows. First, the size or aspect ratio of the graphene (or a combination of the two) may limit the shift. This would be expected if the HfO_2 top gate dielectric is impermeable to gaseous dopants, which must migrate along the graphene to the metal. This is considered unlikely, since the top oxide is of lower quality than the thermal $SiO_2$and likely more permeable. The method of doping reduction is expected to be decomposition and/or migration of the dopants through the oxide. A second possibility is that the annealing affects the bonding of the metal contacts to the graphene, and that it is the regions of graphene which are doped by the contacts which affect the conductance modulation of the device. This is supported by the observation that only the lead areas in the linear measurement show a Dirac point resistance peak, as well as by the dependence of the magnitude of modulation of the two-terminal device conductance on the size and aspect ratio of the device. These effects could be differentiated by further device geometry studies or by direct EFM or Kelvin probe measurements on devices without a top gate or top dielectric in an inert atmosphere.

Appendix A

SOP: E-Beam Lithography

This section describes the use of the Nanometer Pattern Generation System (NPGS) (http://www.jcnabity.com/) attached to the JEOL 5910 SEM in the CMSE Electron Microscopy Shared Experimental Facilities in room 13-1015. Instruction in the use of this SEM was provided by Anthony Garrat-Reed (who has since left MIT; see current staff for training) and is required prior to equipment use and is therefore covered only briefly below, with the intention of being a quick reference when performing lithography. Instruction in use of the NPGS system was provided by Albert Wang (graduate student under Professor Ray Ashoori, and who has since left MIT). The NPGS system was installed by the Ashoori group and is currently maintained by the Jarillo-Herrero group. An image of the SEM and lithography computer is presented in Figure 3-6.

A.1 Overview

The lithography system is run from a dedicated computer located to the left of the SEM on a rolling cart. Installed in the computer is an NPGS input/output card which communicates with the SEM system across three cables. Two cables, labeled "X" and "Y", allow the lithography system to control the beam position via ±10 V analog signals. The third cable allows the SEM detector intensity to be read by the lithography system. Supposedly, both the motorized stage and beam blanker of

the SEM can also be controlled by the NPGS system, which would make the JEOL 5910 much more desirable as a research tool by allowing automated writes of multiple fields. This would involve investigating the necessary drivers and settings adjustments through contacting the NPGS system manufacturer, and would make a good project for future process improvement.

The lithography process consists of:

1. Preparing the chip
2. Designing the lithography pattern
3. Preparing the NPGS
4. Preparing the SEM
5. Writing the lithography pattern
6. Post-processing the chip

Steps 1 and 6 are described in Section 3.3.2. Steps 2, 3, and 5 require use of the lithography portion of the system, and are described below. Step 4 involves the standard operation of the SEM (sample loading, focusing, stigmating, etc.) as well as a few additionial steps described briefly below.

A.2 Pattern Design

The patterns used by the NPGS system are **.dc2** files, which are DesignCad ASCII 2D files created by the DesignCad LT 2000 program. This program is integrated into the NPGS system and is therefore the preferred program for pattern design. The following design requirements arise from how the files are interpreted by the NPGS software and hardware:

- pattern units are μm (unless another convention is adopted, see Section A.7).
- Each pattern should be centered on (0,0) to make most efficient use of the SEM write field, which extends equally along each axis.

- Pattern elements (lines and polygons) can exist in different Layers and have different Colors and Line Types:
  - Each layer can be written with different magnification, offset, point spacing, and alignment (or each layer may be disabled, to allow for notes or multiple-use files). Layer 1 should be empty, and pattern elements should remain in layers 2-16.
  - Each color in a layer can be written with different dose.
  - The line type determines how a shape is written. Lines with line type 1 (solid) are traversed by the beam. Lines with line type 2 (dashed) must form closed polygons, and the polygons as well as their interior are exposed by rastering of the electron beam. It is recommended that the line types be given separate colors so that line and area doses may be specified appropriately.
- For alignment, a separate convention is adopted for pattern elements:
  - Polygons of line type 2 (dashed) will be scanned by the electron beam. The resulting image will be displayed on the NPGS alignment screen. Typically these scan windows will be square or rectangular, slightly larger than the alignment mark, and centered on the alignment mark.
  - Lines of line type 1 (solid) will appear as an overlay on the scanned image on the NPGS alignment screen, and can be moved around (as described in Section A.5) to indicate the position of alignment marks. Typically these lines are the outline of the alignment mark at the center of the scan window.
  - Each Layer used for alignment, containing a dashed window and solid overlay, will occupy a portion of the NPGS alignment screen. It is better to put widely-spaced alignment windows in separate layers, so that they will not appear too small on the screen when each layer is scaled to fill its allotted area.

- Best alignment is obtained by using a minimum of three alignment markers. Using one marker allows NPGS to apply an XY offset, using two markers allows NPGS to apply an additional rotation, and using three or four markers allows NPGS to apply an additional XY scaling matrix (which includes skew). Four alignment window are preferred.
- The best alignment marker design will employ both positive and negative transitions to define its coordinate along each axis. Crosses have proven to be quite reliable.

A.3 NPGS Setup

Setup of the NPGS system is often done prior to loading the sample in the SEM in order to be able to prepare files (and make corrections if necessary) without tying up the SEM.

- Boot up the lithography computer to the left of the SEM. No login is required.
- For new users:
  - Open the NPGS.exe program shortcut on the desktop.
  - Create a new project folder from the menu bar by navigating to the command **Project → Create New Project or File → Copy Current Project**. Use your name or username to identify your project. Copying an existing project (for example, **danezich**) ensures that all settings particular to the SEM and assumed in this appendix are preserved.
  - Afterward, close the NPGS program.
  - Alternatively, a copy of an existing project folder may be created through Windows Explorer. Navigate to **C:\ → Program Files → NPGS → Project Files** and copy a folder named by a current user (for example, **danezich**). Rename the copy with your username. This is the easiest method to ensure that all files and settings needed by the NPGS system to

operate as described in this appendix are preserved. Run files and pattern files are not necessary for proper operation, so these may be deleted from the new folder (**.rf4**, **.dc2**, and **.dc** files).

- Load the lithography files to be written
  - Insert a zip disk containing your files into the zip drive on the computer table by the keyboard and monitor. Alternatively, there are USB ports on the back of the computer which may be used if care is taken to avoid disturbing the attached cables and cards.
  - Copy the files from the inserted medium to your project folder in **C:** → **Program Files** → **NPGS** → **Project Files**.
- Open the NPGS.exe program shortcut on the desktop.
- Make sure your project is selected in the pull-down menu at the top of the NPGS window.
- Make sure the files you just copied show up in your project. Select the type of file to be viewed using the selection box in the upper-right corner of the NPGS window. Note: if the files are not in dc2 format, they can be converted in DesignCAD LT 2000 by selecting the file, opening them using the button for DesignCAD LT on the left, and going to **NPGS** → **Save To Current Project** in the menu bar.
- For each file you want to write, a runfile can be created. Select the .dc2 file you want to write and on the left-hand menu of buttons click "Create Run File". To edit an existing runfile, select that runfile and click "Edit Run File". This is useful for limiting the number of runfiles present, if many patterns are to be written.
- In the runfile editor, make sure the number of entities is correct. Use one entity for alignment and one for writing a pattern. Using an entity **Command** → **Set DAC** allows you to specify where the beam idles while not writing, in order

to avoid overexposing a specific area of your wafer. See the NPGS manual for descriptions of the other, less-used commands.

- If using alignment:
  - Create an "Alignment" entity and double-click on the *File Name* field. Select the .dc2 file containing the alignment marks. This brings up new fields on the right of the runfile editor were one may set various exposure parameters.
  - For each layer that contains alignment marks, select "Alignment". For each layer that does not contain the alignment marks, select "Skip".
  - If the intent is to minimize exposure, set the "Dwell" time to the minimum allowed (3).
  - Note the magnification. If this different than the magnification used to write the pattern as determined later, change this value so that it matches that of the pattern (note: if the alignment marks extend further than the pattern, the pattern magnification will have to be decreased instead).
- Make an entity of type "Pattern". If there is alignment, place the pattern entity after the alignment entity.
- Make sure the settings on the left are reasonable (default is usually OK) and then double-click on the *Pattern Name* field. Select the .dc2 file containing the pattern you wish to write. This brings up new fields on the right of the runfile editor where one may set various exposure parameters.
- For each layer to be written set the "Layer Prompt" to either "Normal" or "Continuous" (the latter might work better since there is no beam blanker installed). Set each layer which should not be written to "Skip".
- Set the *Magnification* to 100,000. This should be a higher magnification than actually needed, and the NPGS program will substitute the maximum magnification which will allow the entire pattern to be written. Round down this new

number to the next SEM magnification step if no alignment is to be performed. If alignment is used, decrease the number by 10-20% and then round down to the next SEM magnification step. This accounts for pattern shifting during the alignment step. Record this magnification as the SEM will be set to this value later.

- For the *Beam Current* entry, use the value of beam current measured by the picoammeter if available, or the target beam current if the SEM will be engaged later (remember to update this value later once the beam current is measured).
- Choose the dose desired. The pull-down menu lets you select the units (charge per distance for a line or charge per area for filled shapes, as appropriate for your pattern), and the number can be highlighted and edited.
- Save the runfile and exit the runfile editor.
- To write a pattern, select the appropriate runfile in the NPGS window and click the "Process Runfile" button that appears on the list of buttons on the left of the NPGS window. Choose "Yes" at the prompt. This will load the runfile and bring you to a prompt that pauses the write just before execution.

Note that the runfile may be executed even when not controlling the SEM; this is useful in order to gauge the time that a write will take and to make sure that there are no errors when writing the pattern.

A.4 SEM Setup

It is useful to record the following parameters for later reference, which include the SEM settings, for each pattern written, in order to go back at a later date after observing the results of a given write and to adjust the settings for future writes as necessary:

On this SEM there are three apertures, numbered from largest (1) to smallest (3). Larger apertures give a higher maximum beam current. There is a tradeoff between

SEM Parameters		NPGS Parameters	
Accelerating Voltage	10 kV	Magnification	25 or 300 or 1000 x
Aperture	2	Beam Current	50 or 1000 pA
Spot Size	~25-55	Dose	150 μC/cm^2
Working Distance	40 or 25 or 10 mm	Files	alignment/pattern
Magnification	25 or 300 or 1000 x		

Table A.1: E-beam lithography parameters that should be recorded for each write, along with their most common values.

beam current and spot size; for the finest features, aperture (3) can give the best imaging and write results with the allowance of longer integration time. For this thesis, imaging and writing were performed with aperture (2), and a spot size of 20 was chosen as a standard for focusing, corresponding to a beam current of about 10 pA.

For imaging, the magnitude of the beam current is not very important, but it must be controlled during lithography to supply the correct dose to the resist. The beam current is measured by means of a Faraday cup. A Faraday cup is a metallic cavity into which the electron beam can be focused and which will thus collect nearly the entirety of the beam current (including secondary electrons). The Faraday cup is attached to the SEM chuck which is in turn electrically isolated from the SEM enclosure and connected to an ammeter, which will read the collected beam current. Note that the actual electron dose supplied to a resist is roughly 1.5 to 2 times larger than the measured beam current due to backscattered secondary electrons which result from collisions of the high-energy primary beam. The exact factor depends upon the target material. In all descriptions below, the beam current, as read by the ammeter, is used, so as to simplify note-taking. Faraday cups may vary in form; examples include a small hole drilled into the metallic SEM chuck, a small nut secured to the SEM chuck with conductive paint and covered with aluminum foil with a pinprick in the center, and the gap between the inner and outer chucks of the JEOL 5910 chuck assembly (in the case that one of the other methods is not available).

The steps for setting up the SEM for lithography are:

- Sample preparation. After application of the lithography resist (Section 3.3.2)

there should be some focus features present on the sample; for example, a drop of gold nanosphere colloid may be deposited on the sample and allowed to dry before placing in the SEM. Nanospheres used for this thesis work were 100 nm in diameter, near the limit of resolution of the JEOL 5910.

- Adjust the coarse focus, align the aperture using the knobs on the SEM column, then focus on the sample and correct the astigmatism as detailed in the JEOL 5910 instruction manual and covered during equipment training. These adjustments may need to be iterated to obtain optimal focus.

- Measure the beam current with a Faraday cup. Move to the Faraday cup and go to a high magnification while looking into the hole. Change the spot size to adjust the current to the desired level. Record both the spot size and the current as read off the picoammeter.

- Adjust the spot size to a low value (e.g., 0) for these next steps to avoid unintentional exposure of the resist.

- Adjust the SEM chuck rotation. Set the scan rotation to zero, then find a horizontal (or vertical) feature (e.g., a previously written metal line, or the edge of the chip), center it in the screen, and use the stage control to translate by a known distance d away (e.g., 1 mm) along the feature. Make note of the new coordinates, and translate so that the feature is again centered on the screen. Make note of these coordinates and compute the shift distance s that was required to recenter the feature. Correct the angle by $\tan^{-1}(s/d)$.

- Adjust the scan rotation as needed until the wafer image is completely aligned.

- Fine-tune the focus and stigmation if the chuck rotation or scan rotation have been adjusted.

A.5 Writing the Pattern

This involves coordination of the SEM and NPGS systems. The SEM controls are used to navigate to the write location and set the beam current and beam blanking. The NPGS controls are used to direct the beam during the pattern write.

To switch between SEM and NPGS control of the XY position of the beam, there is a toggle switch (blue box near or on top of the picoammeter) with two settings, "SEM" and "NPGS". The switch is spring-latched, so to operate it, one must pull up on the toggle before flipping it to the opposite position. The switch should always be set back to "SEM" at the end of each session so as to not cause a problem for SEM users who do not do lithography. Note that beam blanking, spot size, and stage control are available on the SEM control program even when in the "NPGS" mode.

Beam blanking (blocking of the electron beam from the sample by a physical barrier or by deflection) is important because it protects the sample from unintended exposure while the sample is being moved to a new write position or while the beam is settling after large changes in deflection. Currently the beam blanker is available only by manual control. It can be turned on (blank the beam) or off (unblank the beam) via the menu bar with the mouse (**Tools → Beam Blanking**) or keyboard (**Ctrl-T** then **B**). The beam blank may also be turned off by clicking the "Beam Blank Off" button at top right of the image area of the SEM control program.

General procedures for writing the pattern are as follows:

- Ensure that the toggle is in the "SEM" position.
- If aligning by hand, ensure that the spot size on the SEM is set as low as possible while still being able to distinguish features necessary for alignment. Minimize time spent translating to a location and centering on the write field. If aligning by stage motion with reference to a chip corner (without visual verification), ensure that the beam is blanked during translation.
- Translate to and zoom in on the feature that is going to be the center of the pattern.

- Blank the beam.
- Adjust the SEM magnification to that determined for the write in the runfile. (100 x = 1 mm write field, 1000 x = 100 μm write field, etc.)
- Adjust the SEM spot size to that desired for the write.
- Make sure the NPGS runfile magnification is set to the SEM magnification and the NPGS beam current corresponds to the SEM spot size. Save the runfile if any parameters are updated.
- Flip the toggle switch from "SEM" to "NPGS".
- On the SEM disable beam blanking
- On the NPGS computer, press the space bar to continue the write that was initiated by processing the runfile.
- The runfile will now execute. If there is an alignment entity, then the following steps will be taken:
  - The sample will be scanned as indicated in the alignment file, and the resulting image will be displayed on the NPGS computer. See Additional Notes regarding the scan mode and other alignment options.
  - Move the overlays to best match the image within each alignment window.
    - Overlays can be moved by the arrow keys.
    - The "insert" and "delete" keys will switch between alignment windows. In addition, the "insert" key will switch between shifting all overlays and scaling the position of all overlays at once.
    - To increase or decrease the step size of the overlay move, press "+" or "-" respectively.
    - To accept the current offset and rescan the alignment windows press "space". This allows one to verify that the offset is correct, or to make finer adjustments based on areas of the scan window which were not

seen previously. This will only work if at least one overlay position has changed since the previous scan. It is not necessary to do this if there is no need to rescan.

  - Once the alignment is acceptable, press "enter" three times (with a slight pause between each press). This accepts the alignment and proceeds to the write step.
  - At this point the NPGS system is paused, and any adjustments to beam current may be made (see Additional Notes section).
  - Press "space" to unpause the write entity execution and begin writing the pattern.

- The pattern is now written by the NPGS software. A progress indicator will be shown, giving the percent complete. This percent corresponds to the fraction of polygons or lines which have been written, which will not correspond to the time required for the write if the pattern elements vary greatly in size and are relatively few in number.
- At the end of the write, the lithography computer will chime and display a message indicating complection.
- Blank the beam on the SEM.
- Respond to the NPGS prompts. The lithography computer will prompt for a keypress and then ask if the pattern should be written again. If the pattern is to be written again, press "y", translate the SEM stage to the new location, and repeat the process from the beginning of this section. Otherwise, pressing the "space" or "enter" key will exit the pattern write mode and return to the NPGS main window.

A.6 Additional Notes

- **CleWIN.** CleWIN is a lightweight CAD program which can be used to generate

lithography pattern files. It has a simpler user interface than DesignCAD LT 2000, but is not able to save files in the necessary dc2 file format. The solution is to export the CleWIN design as a dxf file. When this is done, the user is prompted to enter a scaling factor for units of the new file in terms of the CleWIN units (which are intended to be μm). Since NPGS assumes a unit of μm also, this factor should be set to 1. The dxf file should be imported into DesignCAD LT 2000 and then saved as a dc2 file after the pattern elements are changed to the appropriate line type, layer, and color.

- **Sample Preparation.** The sample should have a small drop of gold colloid solution (ca. 100 nm diameter spheres, near the resolution limit of the JEOL 5910) placed on the surface and allowed to dry before insertion into the SEM. This provides reliable features for focus and astigmatism adjustment. The drop should be placed away from the resist edge bead in an unimportant area of the chip, since it will be overexposed during focusing. Best results are obtained when focusing on small clusters containing a few spheres, usually found around the periphery of the dried droplet.

- **Mitigating Stage Control Freezing.** The stage motion is controlled through a pop-up window. It was noticed that occasionally this window would freeze and therefore the position of the stage could not be read, and the stage could not be translated by measured amounts (necessary for alignment marks for Hall bar graphene devices). To recover stage control, it is necessary to shut down and restart the SEM control program. This also requires one to again focus, adjust the astigmatism, and measure the beam current, which can become tedious.

  To avoid this problem, it was found sufficient to control the transfer of focus between SEM and stage control windows: Before interacting with a field on the stage control window, focus is shifted to the stage control window by clicking on the title bar. After the stage motion is performed and before any field of the SEM control window is accessed, focus is similarly shifted to the SEM control window by clicking on the title bar (or any non-interacting area) of the SEM

control window.

- **Rotation Control.** The stage rotation often will not engage when the angle being rotated through is less than ~4 degrees, and this will be reflected in the rotation angle display not achieving the target value. To reliably accomplish small angle rotations, make two rotations of angle >5 degrees such that the sum of these rotations is the desired rotation.

- **Multiple Runfile Entities.** Make sure that each pattern entity (alignment and write, as well as each component of each write) has the same magnification setting and beam current setting.

- **Alignment Exposure.** During alignment the areas around the alignment marks are scanned by the electron beam. In order to prevent the dose from reaching levels required for exposure, two methods may be used.

  First, the beam current may be lowered for alignment and increased for exposure. This should be done while the beam is blanked. The complication is that often there is an offset in the beam position when the spot size is changed. This can be corrected for by observing the shift during focusing and setting the offset in the runfile to account for this. (Center on feature at alignment spot size, record (x_i,y_i), recenter on same feature at new spot size, record (x_f,y_f), calculate difference (x_f-x_i,y_f-y_i) and set the origin offset to this value.) However, this method is limited in its corrective ability to the resolution of the stage position reading, which is about 1 μm. This method also requires more manual interaction per pattern written. Care should be taken that the beam is unblanked after any change in intensity is made, immediately prior to any alignment or pattern write step, lest the alignment scan be blank or the pattern not actually written by the beam.

  Second, the center-to-center and line-to-line spacing can be increased for the alignment entity. The tradeoff is that the resolution of alignment image is correspondingly decreased. Additionally, if the beam intensity is above a critical

value (beam current * minimum dwell time * beam area $\geq$ critical dose) then the resist will be exposed anyway, albeit in a pattern of sparse dots. Thus this method should be used only at relatively low beam currents.

- **Alignment Scan Mode.** To minimize exposure of the resist during alignment, ensure that the alignment program is in "Single Scan Overwrite" mode, which should be indicated at the top left of the screen. Otherwise, the beam will scan continuously during the entire time that the alignment is performed. To put the program in this mode, press "s" to ensure that the acquisition mode is SEM, and then press "shift-S". There are also additional commands available during alignment that are not listed by pressing the help '?' button. These additional commands are listed in the NPGS manual, which is available online or on the lithography computer. A commonly used command is "p" to enlarge the images of the alignment windows.

- **Pg.sys.** This is a most useful NPGS settings file. To access it from the NPGS window, change the view to "All Files", find and right click on the pg.sys file, and select the "edit" option. See the NPGS manual for descripyions of all variables. Perhaps the most relevant is the "mag scale" setting which limits the write field size. Note that there is no way to adjust the aspect ratio of the write field through the NPGS program. The best workaround seems to be to adjust the "mag scale" so that one axis is correct, and then to scale the other axis in the pattern layout appropriately. For the JEOL 5910, it was found that the difference in axis scaling is negligible (<1%). Because of this, the error due to scan rotation is similarly low.

- **Blank Alignment Screen.** If one is certain they should see an alignment mark but the scanned area is blank, first make sure that the beam is not blanked. Often the problem is with the SEM contrast and brightness. View the spot used for focus and stigmation at the beam current which is used for alignment. Adjust the SEM contrast and brightness until the image displays properly. If this does not solve the problem, try adjusting the contrast limits of the alignment

display on the lithography computer by pressing "[" or "]" or using the numeric keypad. This may be especially important, for example, when aligning visually on the SEM and switching to a much larger beam current for fine alignment and writing. An important indicator that this is the problem is a small range (<10) of scanned intensity values, as displayed in the upper right corner of the alignment screen.

- **Write Error.** If there is an error during the lithography write, a short segment of the Funeral March Sonata by Chopin will play. Usually this is due to the alignment offset causing elements of the pattern to fall outside of the write field. Solutions are to reposition the sample so as to decrease the necessary alignment offset, or to decrease the magnification of the write so as to allow for a larger alignment offset. Sometimes the error is due to mistakes in the pattern file itself, such as redundant vertices, non-closed polygons, or improper line designation. In this case, the pattern file must be edited in Design CAD LT and the corrected version saved. The runfile must then be opened so that the new pattern file may be loaded, and the updated runfile must be saved again.

  Note, however, that portions of the pattern which were exposed during the first write will be exposed again during a second write, and if alignment was used, then the alignment may be slightly different between writes. This may be especially complicating for small devices, and it might mean the device should be abandoned.

- **End-of-Session.** Ensure that the toggle switch is set to "SEM" and that the spot size is set to "1". This ensures transparency for users who do not use the lithography system, and allows remote operation of the SEM, respectively.

- **System Location.** Since the work done in this thesis, the JEOL 5910 has been moved to a new location. See the CMSE Shared Electron Facilities staff for training and orientation.

A.7 Alternate Runfile and Pattern Settings

The initial method taught for writing patterns of varying size was different than the method described above. Whereas the current method involves adjusting the pattern magnification setting within NPGS while keeping the beam current fixed, the initial method involved adjusting the beam current setting while using a fixed pattern magnification. While these two methods are functionally equivalent, the current method is much easier to implement. The initial method is presented here because of its relevance to pattern size, magnification, and write time.

The following notational conventions are used

Shorthand	Subscript	Description
DXF	d	Denotes values for the NPGS lithography computer files
SEM	s	Denotes values for the SEM computer, or CleWIN CIF files

The quantities which come into play are then

Variable	**Description**
F_s	Field of view of the SEM [μm]
M_s	Magnification of the SEM [x]
Z_s	Size of a feature in the SEM [μm]
I_s	Beam current measured by the picoammeter [pA]
F_d	Field of view of the pattern file [file units]
M_d	Magnification needed to write the pattern file at proper size [x μm/file units]
Z_d	Size of a feature in the pattern file [file units]
I_d	Beam current entered into the NPGS runfile
S	Scaling parameter to convert from [μm] to [file units] (CIF to DXF)
T	Scaling parameter to convert beam current from value read to NPGS entry
P	Power of the SEM = 90,000 [x μm] for the JEOL 5910

The magnification power P of the SEM is a constant which depends on the construction of the SEM

$$P = F_s \cdot M_s = F_d \cdot M_d$$

This means that at a magnification of M_s = 1000x the field of view of the SEM is $F_s = P/M_s = 90$ μm on a side.

Let the pattern file parameters remain fixed at $F_d = 90$ μm and $M_d = P/F_d =$ 1000x. The motivation for this is that files will always be designed within the same bounding rectangle (± 45 μm) and the NPGS magnification will always be 1000x, reducing the mistake of not updating this value for every pattern file. Thus each pattern designed in units of μm will need to be scaled so that the pattern fits within the field size F_d. The scaling factor applied for this conversion is

$$S = \frac{F_s}{F_d} = \frac{M_d}{M_s} = \frac{P}{F_d \cdot M_s} = \frac{P}{F_d \cdot M_s}.$$

and the size of features in the pattern file related to that in the CIF file are

$$Z_d = \frac{Z_s}{S}$$

that is, each unit in the DXF is equal to S μm.

It is also necessary to scale the beam current in order to assure that the dwell times are calculated so as to produce the correct dose. The actual dose D supplied to the resist is an independent constant, and allows computation of the current scaling factor T

$$\begin{aligned} D &= \frac{Current}{Area} Dwell = \frac{I_s}{Z_s^2} Dwell = \frac{I_d}{Z_d^2} Dwell \\ T &= \frac{I_d}{I_s} = \frac{Z_d^2 \cdot Dwell}{Z_s^2 \cdot Dwell} = \frac{Z_s^2/S^2}{Z_s^2} = \frac{1}{S^2} \end{aligned}$$

where the factor (~2) which accounts for the increased dose due to scattered electrons is assumed to be subsumed into the value of the critical dose D.

As an example, let there be a pattern file 1,350 μm in size. Then the maximum

magnification for writing is given by

$$\begin{aligned} S &= \frac{F_s}{F_d} = \frac{1,350\ \mu\text{m}}{.\ 90\ \mu\text{m}} = 15 \\ M_s &= \frac{M_d\text{x}}{S} = \frac{1000}{15} = 66.67 \end{aligned}$$

The next lowest SEM magnification is 60 x, and this lower magnification allows ~10% margin of error for alignment. Starting again from this new magnification,

$$\begin{aligned} M_s &= 60\text{x} \\ S &= \frac{M_d}{M_s} = \frac{1000\text{x}}{60\text{x}} = 16.67 \\ F_s &= S \cdot M_d = 16.67 \cdot 90\ \mu\text{m} = 1500\ \mu\text{m} \\ T &= \frac{I_d}{I_s} = \frac{1}{S^2} = \frac{1}{16.67^2} = 0.0036 \end{aligned}$$

which gives both the scaling factor S for conversion between units in NPGS and the SEM, as well as the corresponding scaling factor T for the beam current.

Appendix B

Gate Capacitance

The gate capacitance of a graphene device has two components, electrostatic and quantum.

Electrostatic Capcacitance

The electrostatic capacitance of a graphene device is specific to its geometry, which in most cases is well-approximated by a parallel-plate capacitor model. The graphene and doped silicon wafer serve as the conductors, and an oxide layer serves as the dielectric. For devices with a lateral size L and a separation d such that $L/d \gg 1$, this is an appropriate approximation. In the devices considered in this thesis, typcial dimensions are $L \geq 2\ \mu$m and $d = 300$ nm, so that $L/d > 6$, and so the parallel-plate approximation is used.

The capacitance for a parallel plate capacitor is given by the equation

$$C_{p-p} = C_g A = \frac{\epsilon_0 \epsilon_r A}{d} \tag{B.1}$$

where

$$\begin{aligned} C_g &= \text{Gate capacitance per unit area of the graphene} \\ \epsilon_0 &= \text{The permittivity of free space } \left(\frac{1}{\mu_0 c^2} = 8.854 \times 10^{-12} \frac{\text{F}}{\text{m}}\right) \\ \epsilon_r &= \text{The relative permittivity (dielectric constant, 3.9 for SiO}_2\text{, 18 for HfO}_2\text{)} \\ A &= \text{Area of the graphene} \end{aligned}$$

$$\begin{aligned} C_g(\mathrm{SiO_2}, 300 \text{ nm}) &= 1.151 \times 10^{-4} \text{ F/m}^2 \\ C_g(\mathrm{SiO_2}, 100 \text{ nm}) &= 3.453 \times 10^{-4} \text{ F/m}^2 \\ C_g(\mathrm{HfO_2}, 40 \text{ nm}) &= 3.984 \times 10^{-3} \text{ F/m}^2. \end{aligned}$$

Table B.1: Values of the electrostatic capacitance for device parameters in this thesis.

d = Thickness of the dielectric

For the devices in this thesis, the values used are thus:

Quantum Capacitance

The quantum capcacitance is determined by the band structure and dimensions of the graphene, with the conventional interpretation as the derivative of charge with respect to potential. Following [97], the quantum capacitance C_q is given by

$$C_q = \frac{\partial Q}{\partial V_{ch}} = q^2 \frac{2}{\pi} \frac{kT}{(\hbar \nu_F)^2} \ln \left[2 \left(1 + \cosh \frac{qV_{ch}}{kT} \right) \right] \tag{B.2}$$

where

$$\begin{aligned} q &= \text{Electron charge } (1.6022 \times 10^{-19} \text{ C}) \\ V_{ch} &= \text{Shift in Fermi level of the graphene} \\ \hbar &= \text{Planck's constant over } 2\pi \ (1.055 \times 10^{-34} \text{ Js}) \\ \nu_F &= \text{Fermi velocity of electrons in graphene } (1 \times 10^6 \text{ m/s}) \end{aligned}$$

which has a minimum at $V_{ch} = 0$ of $C_{q,min} = 8.47 \times 10^{-3}$ F/m^2.

Note that for potentials $V_{ch} \gg kT$, the quantum capactiance becomes linear in the potential

$$C_q \approx q^2 \rho_{gr} = q^2 \frac{2}{\pi} \frac{qV_{ch}}{(\hbar \nu_F)^2} = 0.235 \ V_{ch} \left[\frac{\text{F}}{\text{m}^2} \right].$$

Capacitance Comparison

For the back-gated devices above (SiO_2 dielectric), the quantum capacitance C_q is greater by at least an order of magnitude than the electrostatic capacitance, and so

the electrostatic capacitance dominates the calculation of the induced charge. For the top-gated devices above (HfO_2 dielectric), the quantum capactiance is at least twice the electrostatic capacitance. The electrostatic capacitance still dominates, but it is more necessary to include the quantum capacitance correction. The total capacitance which combines the electrostatic and quantum capacitances is given by

$$C_{tot} = \left(C_g^{-1} + C_q^{-1}\right)^{-1}. \tag{B.3}$$

Capacitance Considerations

In the above discussion it was assumed that the graphene acts as a perfect conductor, so that all field line generated at the gate terminate on the graphene. In reality this is not the case; graphene is semi-transparent to the electric field. The skin depth has been variously reported as 0.4 - 1.2 nm [72, 75], with the former result being taken for consistency. The thickness of a single graphene layer is only 0.335 nm. Thus above a handful of layers the conductivity assumption above is appropriate, though in all cases the distribution of induced charges within the graphene may be nonuniform.

For the two-terminal graphene line devices of Chapter 5, the combination of electrostatic and quantum capacitance gives a minimum capacitance, according to Equation B.3, of

$$C_{tot} = \left((1.151 \times 10^{-4})^{-1} + (8.47 \times\ 10^{-3})^{-1}\right)^{-1} = 1.136 \times 10^{-4}\ \mathrm{F/m^2}.$$

This differs from C_g by only 1.3%, and gives a lower limit on the uncertainty of the mobility values derived from conductivity measurements. This indicates that the gate capacitance can be treated as a constant for these devices, and can be approximated by the pure electrostatic capacitance.

It is worth noting that the full expression for the capacitance as a function of gate voltage has a minimum at the Dirac point and asymptotically approaches the value of the electrostatic capacitance as the distance from the Dirac point increases. This must be taken into account with the thin HfO_2 dielectric devices by using the full expression for the gate capacitance $C_{tot}(V_{gs})$ given by Equation B.3 in place of C_g.

Appendix C

Drift and Field-Effect Mobilities

It is useful here to note the difference between *drift* mobility μ_d and *field-effect* mobility μ_{fe}, two different quantities which are often referred to simply as the *mobility* μ in the literature. The original quantity is the drift mobility, defined as the net velocity response of charge carriers to an applied electric field:

$$\mu_d \equiv \frac{v_d}{E_{ds}} = \frac{\left(\frac{J_{ds}}{en}\right)}{(V_{ds}/L)} = \frac{\left(\frac{I_{ds}/W}{en}\right)}{(V_{ds}/L)} = \frac{1}{en}\left(\frac{I_{ds}}{V_{ds}}\frac{L}{W}\right) = \frac{1}{en}\sigma_{ds} \quad \text{(C.1)}$$

where

v_d = Drift velocity of charge carriers

E_{ds} = Drain-source electric field accelerating the charge carriers

J_{ds} = Current density in the device

e = Charge per carrier (charge of electron)

n = Areal density of carriers in the device $n(V_{gs})$

V_{ds} = Electric potential between drain and source

W = Device width

L = Device length (distance between source and drain)

σ_{ds} = conductivity of the graphene $\sigma_{ds}(V_{gs})$

The critical link between the calculated mobility and measured conductivity lies in the form of the areal charge carrier density $n(V_{gs})$. In early works in the literature [97, 67, 98], this was taken to be simply the charge induced by the gate in a parallel-plate capacitor model $n(V_{gs}) = C_g|V_{gs}|$, where C_g is the capacitance per unit area, and the Dirac point of graphene is assumed to be at $V_{gs} = 0$. The trouble with this approach is that in actual devices there is a finite conductivity minimum even when $V_{gs} = V_0$, leading to an abnormal divergence of the drift mobility.

The solution to this is to refine the definition of $n(V_{gs})$. The conductivity minimum is caused primarily by charge puddles induced in the graphene by charge impurities in the material surrounding the graphene [32], but also by natural rippling of the graphene film [4] and by thermal carrier excitation. While this apporach is adequate for clean single-layer graphene films, the territory of multi-layer graphene is not as well charted. Interaction between layers (as well as the random arrangement of regions of different thickness) preclude using an analytic form for the charge density $n(V_{gs})$.

The field-effect mobility μ_{fe}, however, provides a solution to this. Instead of considering the average velocity over all charge carriers to an applied electic field, it considers the average velocity of charge carriers which are added to or taken away from the channel at each gate voltage. The change in charge carriers is given by the electrostatics of the situation through the capacitance (see Appendix B):

$$\mu_{fe} \equiv \frac{\partial \sigma_{ds}}{\partial en(V_{gs})} = \frac{\partial \sigma_{ds}}{\partial e\left(\frac{1}{e}C_g V_{gs}\right)} = \frac{1}{C_g}\frac{\partial \sigma_{ds}}{\partial V_{gs}} \tag{C.2}$$

where it is understood that the capacitance C_g should be the series combined electrostatic and quantum capacitance if these two capactiance values are comparable. The last step in Equation C.2 assumes that C_g is constant. This condition fails when the quantum capacitance contributes significantly, and therefore C_g must be kept within the differentiation.

This differential measurement has become the *de facto* standard for discussion of graphene and nanotube mobilities in the literature. It is useful to note that since the quantity $\partial\sigma_{ds}/\partial V_{gs}$ is called the transconductance, the field-effect mobility is

also known as the "transconductance mobility". Within this thesis, any reference to mobility implies the field-effect mobility unless otherwise stated.

Appendix D

Two Conductivity Fitting Models for Single-Layer Graphene

We first consider two physical models for current transport through a graphene sheet, and seek to relate the parameters of the models to the measured data for thin graphene films. The models are a semi-qualitative adaptation of the single layer graphene conduction discussed extensively in the literature. There are two basic adjustments which can be made to Equation 5.2 for ideal single-layer graphene. The first is to include the effects of contact resistance and internal resistance from mechanisms other than long-range coulomb scattering. The second is to include the effects of conduction channels parallel to that of the ideal graphene. Both these modifications have also been discussed in the literature. They may be combined with Equation 5.2 in two ways as shown in Figure D-1 and described by the two equations

$$\text{Model 1:} \qquad \sigma_{ds}(V_{gs}) = \sigma_{bg} + \left[(C_g \mu_k |V_{gs} - V_0|)^{-1} + \rho_r\right]^{-1} \tag{D.1a}$$

$$\text{Model 2:} \qquad \sigma_{ds}(V_{gs}) = \left[(\sigma_{bg} + C_g \mu_k |V_{gs} - V_0|)^{-1} + \rho_r\right]^{-1} \tag{D.1b}$$

where the quantities

$\sigma_{ds}(V_{gs})$ = Measured conductivity (Equation 5.1)

σ_{bg} = Background conductivity (interpreted below)

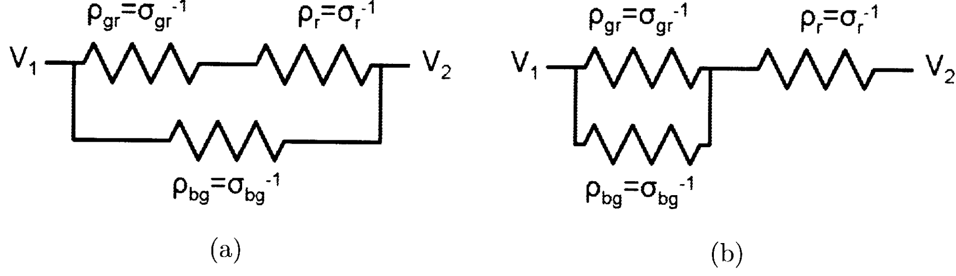


Figure D-1: Resistor models of few-layer graphene conduction. Contacts are held at potentials V_1 and V_2. (a) Background conductivity treated as an independent parallel channel. (b) Residual resistivity acting on both the linear and background conductivity equally. The actual behaviour will be somewhere in between these two extremes.

$$\sigma_{gr}(V_{gs}) = C_g \mu_k |V_{gs} - V_0| = \text{Conductivity of the ideal graphene channel}$$

$$C_g = \text{Gate capacitance per unit area (Appendix B)}$$

$$\mu_k = \text{Mobility of the graphene}$$

$$V_0 = \text{Gate voltage of the Dirac Point}$$

$$\rho_r = \text{Residual resistivity (interpreted below)}$$

The ideal graphene conductivity $\sigma_{gs}(V_{gs})$ is due to long-range scattering from charge impurities in the graphene channel. The residual resistivity ρ_r is taken to be independent of gate voltage V_{gs}, a condition which is satisfied by other types of scattering in the graphene channel (such as acoustic phonon scattering) as well as by contact resistance (for caveats, see [71]). The background conductivity σ_{bg} may be due to regions of thick graphene which shunt the contacts, to evanescent field overlap between contacts, or to nonidealities in the band structure of graphene.

Model 1 supposes that thick graphene acts as a shunt, and that the interesting effects of the contact resistance and various scattering summarized by the residual resistivity ρ_r affect primarily the thin graphene regions. Model 2 declares that the ρ_r acts equally on the entire graphene channel, including both thin ($\sigma_{gs}(V_{gs})$) and thick (σ_{bg}) graphene regions which are taken to be in parallel (note that combination in series can be subsumed into the ρ_r term. In reality, lines of graphene with regions of varying thickness are not so simply connected, and should be modeled through

continuum mechanics. Nonetheless, these models are instructive, fit the data, and provide a physical interpretation. The true behaviour may be expected to lie between the predictions of these two models, which are the limiting cases of combining a uniform conductivity region with a varying conductivity region.

As it turns out, these two models are isomorphic (as demonstrated below). One can be converted into the other by means of parameter substitution. This means that each parameter in one equation can be expressed in terms of the parameters of the other equation, and implies that the physical arrangement of a device's component channels (thin and thick graphene regions) cannot be determined from source-drain measurements alone. Consequently, the true values of the physical parameters σ_{bg}, $C_g\mu_k$, and ρ_r are indeterminate between the bounds set by the two models. A possible way to lift this uncertainty is to work from optical images, dividing the graphene channel into thin and thick regions, computing the relative contribution of series and parallel connectivity, and using this to interpolate between the fit parameters for the two models. This task is left for future work.

The model equivalence can be demonstrated as follows by finding the explicit correspondence between parameters in each model. Let the drain-source conductivity $\sigma_{ds}(V_{gs})$ be abbreviated as σ, and let the gate voltage variation from the Dirac Point $|V_{gs} - V_0|$ be Δ and the parameters for the model fits be labeled with the model number as a subscript under the correspondence $\sigma_{bg} \equiv A$, $C_g\mu_k \equiv B$, and $\rho_r \equiv C$. Equations D.1 thus read

$$\text{Model 1:} \qquad \sigma = A_1 + \left((B_1\Delta)^{-1} + C_1\right)^{-1} \tag{D.2a}$$

$$\text{Model 2:} \qquad \sigma = \left((A_2 + B_2\Delta)^{-1} + C_2\right)^{-1}. \tag{D.2b}$$

The two models must correspond to the same experimental conductivity curve, which gives the constraint $\sigma = \sigma$ for the two models:

$$A_1 + \left((B_1\Delta)^{-1} + C_1\right)^{-1} = \left((A_2 + B_2\Delta)^{-1} + C_2\right)^{-1}$$
$$A_1 + \frac{1}{\frac{1}{B_1\Delta} + C_1} = \frac{1}{\frac{1}{A_2+B_2\Delta} + C_2}$$

$$A_1 + \frac{B_1\Delta}{1+C_1B_1\Delta} = \frac{A_2+B_2\Delta}{1+C_2(A_2+B_2\Delta)}$$
$$\frac{A_1 + A_1C_1B_1\Delta + B_1\Delta}{1+C_1B_1\Delta} = \frac{A_2+B_2\Delta}{1+C_2A_2+C_2B_2\Delta}$$

which gives a straight product of terms as

$$(A_1 + A_1C_1B_1\Delta + B_1\Delta)(1 + C_2A_2 + C_2B_2\Delta) = (A_2 + B_2\Delta)(1 + C_1B_1\Delta)$$

with corresponding expansion

$$\begin{aligned} A_1 + A_1A_2C_2 + A_1B_2C_2\Delta + A_1B_1C_1\Delta + A_1A_2B_1C_1C_2\Delta \\ + A_1B_1B_2C_1C_2\Delta^2 + B_1\Delta + A_2B_1C_2\Delta + B_1B_2C_2\Delta^2 \\ = A_2 + A_2B_1C_1\Delta + B_2\Delta + B_1B_2C_1\Delta^2. \end{aligned} \quad (D.3)$$

Since this equality must hold for all gate voltages (and therefore all values of Δ), the equality must hold for each power of Δ which appears above. Collecting terms we have

For Δ^2:

$$\begin{aligned} A_1B_1B_2C_1C_2\Delta^2 + B_1B_2C_2\Delta^2 &= B_1B_2C_1\Delta^2 \\ A_1C_1C_2 + C_2 &= C_1 \\ (A_1C_1+1)C_2 &= C_1 \\ C_2 &= C_1/(1+A_1C_1) \end{aligned}$$

For Δ^1:

$$\begin{aligned} A_1B_2C_2\Delta + A_1B_1C_1\Delta + A_1A_2B_1C_1C_2\Delta + B_1\Delta + A_2B_1C_2\Delta &= A_2B_1C_1\Delta + B_2\Delta \\ A_1B_2C_2 + A_1B_1C_1 + A_1A_2B_1C_1C_2 + B_1 + A_2B_1C_2 &= A_2B_1C_1 + B_2 \end{aligned}$$

For Δ^0:

$$A_1 + A_1 A_2 C_2 = A_2$$
$$A_1(1 + A_2 C_2) = A_2$$
$$A_1 = A_2/(1 + A_2 C_2).$$

By multiplying together the results for Δ^2 and Δ^0 we obtain the condition

$$A_1 \frac{C_1}{1 + A_1 C_1} = \frac{A_2}{1 + A_2 C_2} C_2$$
$$\frac{A_1 C_1}{1 + A_1 C_1} = \frac{A_2 C_2}{1 + A_2 C_2}$$
$$A_1 C_1 = A_2 C_2$$

This allows the results for Δ^2 and Δ^0 to be rewritten as

$$C_2 = C_1/(1 + A_1 C_1) \qquad A_1 = A_2/(1 + A_2 C_2)$$
$$C_2 = C_1/(1 + A_2 C_2) \qquad A_1 = A_2/(1 + A_1 C_1)$$
$$C_2(1 + A_2 C_2) = C_1 \qquad A_1(1 + A_1 C_1) = A_2$$

Thus each of the terms A_1, A_2, C_1, and C_2 can be expressed in terms of the parameters of the opposite model. Using these results, the terms B_1 and B_2 are more easily found from the Δ^1 equation as

$$A_1 B_2 C_2 + A_1 B_1 C_1 + A_1 A_2 B_1 C_1 C_2 + B_1 + A_2 B_1 C_2 = A_2 B_1 C_1 + B_2$$
$$A_1 B_2 C_2 + A_1 B_1 C_1 + B_1 + A_2 B_1 C_2(A_1 C_1 + 1) = A_2 B_1 C_1 + B_2$$
$$A_1 B_2 C_2 + A_1 B_1 C_1 + B_1 + A_2 B_1 C_1 = A_2 B_1 C_1 + B_2$$
$$A_1 B_2 C_2 + A_1 B_1 C_1 + B_1 = B_2$$
$$B_1(A_1 C_1 + 1) = B_2(1 - A_1 C_2)$$
$$B_1(A_1 C_1 + 1) = B_2 \left(1 - A_1 \frac{C_1}{1 + A_1 C_1}\right)$$

$$B_1(A_1C_1 + 1) = B_2\left(\frac{1}{1 + A_1C_1}\right)$$
$$B_1(1 + A_1C_1)^2 = B_2$$
$$B_1 = B_2/(1 + A_2C_2)^2$$

Thus conversion between the corresponding parameters in the two models involves only the quantities $(1 + A_1C_1)$ and $(1 + A_2C_2)$, which were shown previoulsy to be equivalent, and because of their utility are defined as the parameter γ. Indeed, the quantity $A_1C_1 = \sigma_{bg}\rho_r = \sigma_{bg}/\sigma_r$ is just the ratio of the background conductivity to the conductivity range over which the graphene modulates (in the asymptotic limit), which is essentially a minimum off/on ratio (inverse of the maximum on/off ratio) for the graphene device. The conversion factor γ is thus singly-valued for a given experimentally measured conductivity curve, and characterizes how much the observed curve differs from that expected for ideal graphene. A value of 1 indicates that the measured device behaves like ideal graphene, while a larger value indicates increasing contributions from scattering (acoustic phonon, contacts) and/or parallel conducting channels (evanescent fields, thick graphene regions).

The results for model equilavlence are summarized in Table D.1.

Model 1 → 2	Model 2 → 1
$\gamma = (1 + A_1C_1) = (1 + A_2C_2)$	
$A_2 = A_1\gamma$	$A_1 = A_2/\gamma$
$B_2 = B_1\gamma^2$	$B_1 = B_2/\gamma^2$
$C_2 = C_1/\gamma$	$C_1 = C_2\gamma$

Table D.1: Isomorphic functions for converting conductivity model parameters between Model 1 and Model 2 for CVD graphene line devices. The parameter γ is a model-independent constant.

Appendix E

Abbreviations

AFM	Atomic force microscope (or microscopy), uses a probe tip to measure the height of a surface to nanometer precision
ALD	Atomic layer deposition, conformally deposits a chemical one atomic layer at a time, see Section 3.3.6
sccm	Standard cubic centimeters per minute, a flow rate of gas measured at STP
CR-7	Chromium etchant from Cyantek Corp., composed of 9% ceric ammonium nitrate and 6% perchloric acid in aqueous solution
CVD	Chemical vapor deposition, a method of using heat to break down gases to obtain the precursors of a chemical synthesis
DC	Dirac cone
DCE	Dichloroethane, an organic solvent often used for photoresist liftoff
DWNT	Double-walled carbon nanotube
EFM	Electrostatic force microscopy, a variant of AFM which senses the magnitude of the electric field
Faraday Cup	A metallic cavity into which an electron beam (e.g. within an SEM) can be focused and which will collect the entirety of the beam current (including secondary electrons) by enclosing the beam impact point within a nearly complete metallic cavity

IPA	Isopropyl alcohol, an organic solvent used as a slow-acting developer for e-beam lithography with PMMA
LL	Lincoln Laboratory
MIBK	Methyl isobutyl ketone, an organic solvent used as a fast-acting developer for e-beam lithography with PMMA
NME	Nano Materials and Electronics (Group), a research group and associated laboratory space under the direction of Professor Jing Kong at MIT
NPGS	Nanometer Pattern Generation System, created by Joe Nabity (http://www.jcnabity.com/), used to enable electron beam lithography on an SEM
NSL	Nanostructures Laboratory, a research group at MIT which allows collaborative access to microfabrication and metrology equipment
NT	Nanotube
PMMA	Poly(methyl methacrylate), a transparent polymer, also known as acrylic when heavily cross-linked, used as an e-beam resist in positive (low dose) or negative (high dose) modes
psi	Pounds per square inch, a unit of pressure equal to 6895 Pa or 1/14.7 atmosphere
SEM	Scanning electron microscope, see Section 3.3.2 for lithography applications
SDS	Sodium dodecyl sulfate, a nanotube surfactant
STB	Simple two band, a model for the density of states in graphite
STP	Standard temperature and pressure, 0 °C and one atmosphere of pressure (101325 Pa)
SWNT	Single-walled carbon nanotube

Appendix F

Publications

1. D. Nezich, A. Reina, J. Kong. Electrical Characterization of CVD-Grown Graphene. In Preparation.

2. H. Wang*, D. Nezich*, J. Kong, T. Palacios. Graphene Frequency Multipliers. *IEEE Electron Device Letters* **30**, 547-549 (2009). * These authors contributed equally to this paper.

3. A. Reina, X. T. Jia, J. Ho, D. Nezich, H. B. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong. Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition. *Nano Letters* **9**, 30-35 (2009).

4. M. Hofmann, D. Nezich, A. Reina, and J. Kong. In-Situ Sample Rotation as a Tool to Understand Chemical Vapor Deposition Growth of Long Aligned Carbon Nanotubes. *Nano Letters* **8**, 4122-4127 (2008).

5. F. Villalpando-Paez, H. Son, D. Nezich, Y. P. Hsieh, J. Kong, Y. A. Kim, D. Shimamoto, H. Muramatsu, T. Hayashi, M. Endo, M. Terrones, and M. S. Dresselhaus. Raman Spectroscopy Study of Isolated Double-Walled Carbon Nanotubes with Different Metallic and Semiconducting Configurations. *Nano Letters* **8**, 3879-3886 (2008).

6. S. G. Chou, F. Plentz, J. Jiang, R. Saito, D. Nezich, H. B. Ribeiro, A. Jorio, M. A. Pimenta, G. G. Samsonidze, A. P. Santos, M. Zheng, G. B. Onoa, E.

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