A Zero-Crossing Based Pipelined Analog-to-Digital Converter with Supply Voltage Scalibility

by

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Abstract

A zero-crossing based pipelined analog-to-digital converter (ADC) has been designed and is fabricated in a 65nm CMOS process. The highly digital implementation characteristic of the zero-crossing detection technique enables energy efficient operation and voltage scaling. Supply voltage scaling based on the required sampling frequency and resolution provides high energy efficiency over a wide range of sampling frequencies and resolutions. A two phase charge transfer scheme (course charge transfer and fine charge transfer) is used to achieve high speed and high resolution. Using switched capacitor circuit, two phase charge transfer scheme is implemented without increasing power and circuit complexity.

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Chapter 1

Introduction

Analog to digital converters (ADCs) are important building blocks in many electronic systems which require digital signal processing and storage of analog input signals. Examples include instrumentation systems (digital oscilloscopes, spectrum analyzers, and medical imaging), wireless communication systems (IF sampling, software radio, base stations,) and consumer electronics (digital cameras, display electronics, DVD and high-definition TV).

Among the various metrics of ADCs, signal bandwidth (or conversion frequency), resolution (or signal to noise and distortion ratio) and power consumption are the key metrics to describe performance of ADCs. Due to the fundamental trade-off between speed (conversion frequency) and accuracy (resolution), numerous ADC architectures are developed to achieve different performance target. Flash ADCs are suitable for fast operation. However, because the design complexity of flash ADCs is exponentially increasing with resolution, flash ADCs are limited to low to medium resolution applications. In contrast, noise shaping property of delta-sigma ADCs provides high resolution at the cost of significant signal bandwidth. Successive Approximation Register (SAR) and pipelined ADCs are efficient for wide range of bandwidth and resolution. Because SAR ADCs require multiple comparisons which take time proportional to the resolution, internal operation must be much faster than conversion frequency, which limits bandwidth of SAR ADCs relatively low. In case of pipelined ADCs, pipelined operation through the stages makes it faster, and high resolution

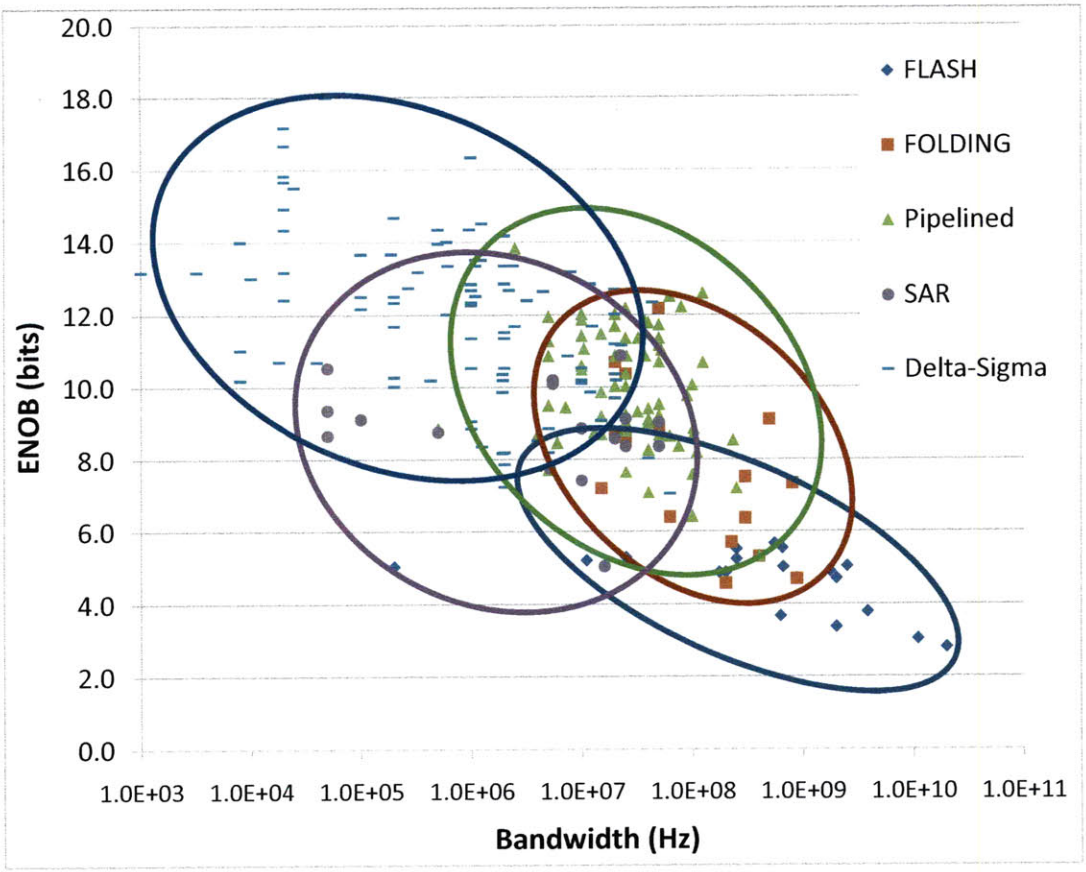

Figure 1-1: ADC architectures

can be achieved by accurate amplification. Figure 1-1 shows efficiently achievable performance range for different ADC architectures with actual ADC performance data published at International Solid-State Circuits Conference and Symposium on VLSI Circuits [1].

1.1 Conceptual Pipelined ADC Operation

As shown in Figure 1-2, general pipelined ADCs have multiple stages which are functionally similar. Each stage is composed of sub-ADC, DAC, and multiplier. The sub-ADC of jth stage quantizes the input to N_j bits and gives digital outputs(D_j). Digital outputs of the sub-ADC are fed into a DAC to generate equivalent analog signal. Then, the difference between the input and the output of the DAC is amplified

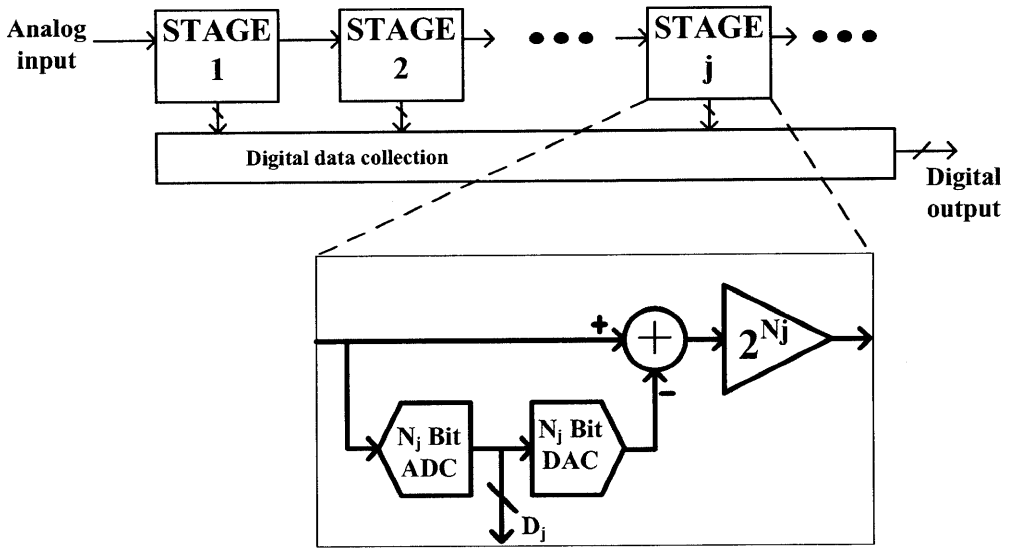

Figure 1-2: Conceptual block diagram of pipelined ADCs

by a factor of 2^{N_j} to recover the full input signal range. The output of the amplifier is called the residue of the jth stage. Since the residue of the jth stage has the same signal range as the input signal, an identical stage can be used for the next stage. In short, the analog input of one stage is converted to digital output codes and a residue which have mathematically the same information. Next, the residue of a stage is further processed by the following stage. Because one stage does not keep any information after passing the residue to next stage, all stages can operate in a pipelined fashion.

Digital outputs of each stage are combined together after the last stage quantizes the input signal. Considering the LSB of the jth stage is worth 2^{N_j} times of LSB of next stage, the combined digital output can be expressed as following.

$$x = (((D_1 2^{N1} + D_2)2^{N_2} + D_3)2^{N_3} + \cdots \quad (1.1)$$

$$= \sum_{i=1}^{k} D_i 2^{N_i + N_{i+1} + \cdots + N_k} \quad (1.2)$$

1.2 Op-amps in Pipelined ADCs

Most of pipelined ADCs rely on op-amps for linear multiplication of analog input signal. It is mainly because multiplication using op-amps is robust and well predicted when the gain of op-amp is large. In addition to high gain requirement, op-amps are expected to have wide bandwidth to settle fast for high speed operation. However, op-amps with high gain and wide bandwidth consume a lot of power. Thus, ideas to reduce power consumption of op-amps have been developed, such as op-amp sharing [2] [3], turning off idle op-amp [4], incomplete settling of op-amp [5], op-amp current reuse [6].

Regardless of these efforts to reduce power consumption of op-amps, continuous transistor scaling made it even harder to implement high gain due to the reduced supply voltage and small intrinsic gain of scaled transistors. To overcome the reduced gain of op-amps, creative techniques have been designed : cascode transistor at the expense of reduced output signal range, cascading multi stage with nested-miller compensation [7], correlated doubling sampling (CDS) [8] and correlated level shifting (CLS) [9] with additional phase. In spite of disadvantages mentioned previously, transistor scaling continues because it provides higher f_t transistors with small parasitic which enables fast operation with low power consumption indigital circuits. Also, increased transistor density with scaled devices enables integrating more complicate functions in a small area, which leads to cost reduction.

The overall device scaling effects on pipelined ADCs can be found from ADC performance trends. On average, conversion frequency increase 1.3 times per process node [10] and Figure of Merit (FoM) decreases 1.8 times per process node, but ENOB decreases 0.3 bits per process node [11]. These performance trends imply that speed and power efficiency of analog circuits can be improved in a nano scaled process. However, it also shows the difficulties of designing accurate analog circuits in a modern CMOS technology.

Chapter 2

Pipelined ADCs without op-amp

Because the power consumption of op-amp based pipelined ADCs is dominated by op-amps, power efficient op-amp design is a key to reduce power consumption. Along with efforts to design power efficient op-amps, several methods to eliminate op-amps in pipelined ADCs have been developed. These methods are common in that more energy efficient circuits replace op-amps. This chapter provides a brief overview of these ideas focusing on the residue amplification without op-amps.

2.1 Open Loop Amplification

One method of eliminating op-amps in pipelined ADCs is using open-loop amplifiers [12]. Unlike the op-amp based closed-loop amplification, sampled charges on capacitors are not redistributed onto feedback capacitors. Instead, capacitors are connected to the DAC to generate the residue and the residue is fed into a resistively loaded amplifier to produce the residue output. In this circuit, no high gain and wide bandwidth amplifier is required, which is power inefficient and difficult to design in nano-scale CMOS technology. Figure 2-1 shows a stage in pipelined ADC using open-loop gain amplifiers.

The major disadvantage of the open-loop amplification in pipelined ADC is the inaccuracy of amplification. The gain of open-loop amplifier is generally transconductance (G_m) times load impedance (R_o) which are not well controlled. Considering

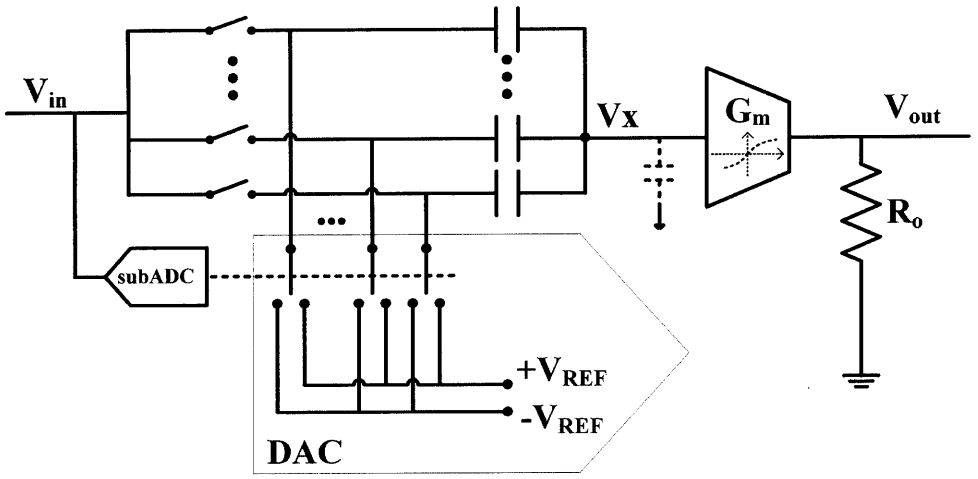

Figure 2-1: A stage in pipeliend ADC using open-loop residue amplification

process variations, the gain must be made tunable, and additional circuits to track the temperature variation are required. The gain compression of open-loop amplifier is another big souce of non-linearity. Also, the non-linear parasitic capacitance at the input of amplifier(V_x node) gives non-ideality, because, unlike op-amp based closed-loop amplification, V_x node voltage varies with input signal.

To improve the accuracy of open-loop amplification, a sophisticated calibration technique is developed [12]. However, it is based on the simple I-V characteristic equation of the transistor which is not suitable for modern process [13]. Additional quantization levels required for digital calibration is another disadvantage.

2.2 Dynamic Source Follower Residue Amplification

Residue amplification using dynamic source follower is another method to eliminate op-amps in pipelined ADCs [14]. The principle of this residue amplification technique is shown in Figure 2-2. During sampling phase, the input signal is sampled on parasitic capacitors C_{gd}, $C_{gs} + C_{gb}$ and $C_{gs,ext}$. When the transistor is configured as a source

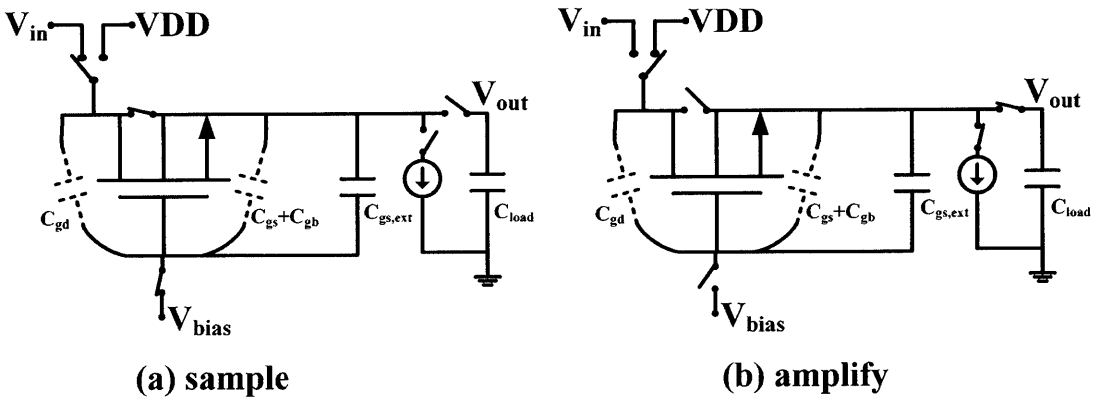

Figure 2-2: Residue amplification using dynamic source follower. (a) sampling phase, (b) amplification phase

follower, V_{gs} converges close to V_T regardless of the sampled charges in the capacitors. Thus, the sampled charges on C_{gd}, $C_{gs} + C_{gb}$ and $C_{gs,ext}$ are transferred to C_{gd}. This is similar to the charge transfer in op-amp based pipelined ADCs where sampled charges in sampling capacitors are transferred to feedback capacitors. Compared to op-amps, source followers are simple, and consume much less power.

However, many disadvantages result from the fact that the gain depends on the parasitic capacitance. First, heavy digital calibration scheme for gain correction is required, because the parasitic capacitance is not well controlled. Also, the non-linearity of parasitic capacitors limits the linearity. In addition, the finite impedance of transistor (r_o) causes V_{gs} to settle to different values at the end of amplification phase which increase non-linearity. Thus, the resolution of pipelined ADCs using this technique is limited to a relatively low range.

2.3 Capacitive Charge Pump

This technique makes use of a capacitive charge pump for amplification [15]. The voltage gain is achieved by sampling an input voltage on multiple capacitors, and

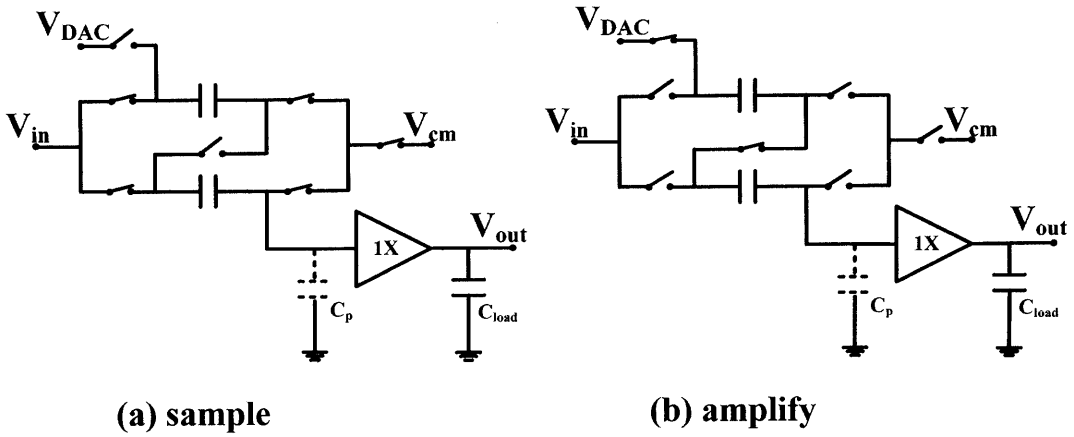

Figure 2-3: Residue amplification using a charge pump. (a) sampling phase, (b) amplification phase

subsequently connecting each capacitor in series to yield the sum of individual voltages sampled on each capacitor, as shown in Figure 2-3. The unity gain buffer in Figure 2-3 is necessary to drive the load capacitor without charge sharing between the sampling capacitors and the load capacitor. Because the gain is set by passive switches and unity gain buffers can be implemented by source followers, significant power savings can be achieved compared to op-amp based residue amplification.

However, similarly to other techniques replacing op-amps in pipelined ADCs, it also suffers from inaccuracies and sensitivity to many design parameters. The parasitic capacitor at the input of unity gain buffer causes gain error and non-linearity. The parasitic capacitors of the switch connecting input capacitors in series are another source of non-linear errors, because the voltage of that node varies with the input.

2.4 Charge-to-Digital Converter(CDC) Using Charge-Coupled Device(CCD)

Figure 2-4 shows the functional block diagram of a CDC based on CCDs [16]. The elements labeled D indicate delays and physically correspond to a set of CCD gates. The additive elements indicate charge summation and correspond to CCD wells that accept charge from two sources. The pairs of elements labeled 1/2 indicate fixed-ratio charge division and are implemented as CCD gates that transfer charge into two receiving wells in equal proportions.

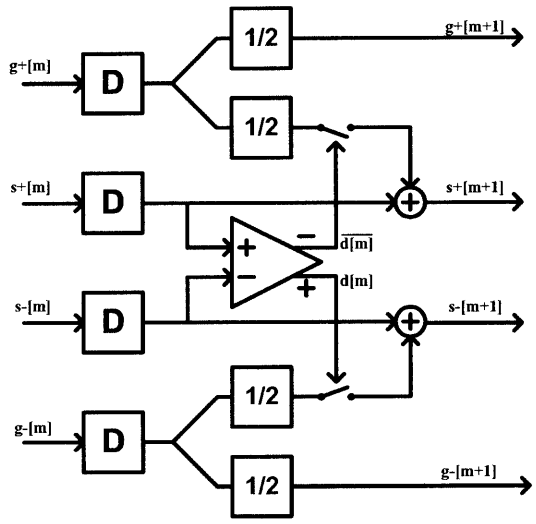

Figure 2-4: Functional block diagram of the charge-to-digital converter using CCDs

With a charge generation circuit at the input, the CDC can operate as an ADC. Based on the comparator output, the divided scaling charges ($\frac{1}{2}$g+[m], $\frac{1}{2}$g-[m]) are added to either positive input (s+[m]) or negative input (s-[m]) to generate outputs (s+[m+1], s-[m+1]). Although it operates in pipelined fashion using the characteristic of CCD opearion, it resolves digital outputs similar to successive approximation by the conditional summation of scaling charges.

The primary source of error in this ADC is the charge splitting inaccuracy. The charge splitting ratio changes due to threshold nonuniformity and geometric mis-

match. Because of the lack of subtracting operation, the common-mmode charges accumulate with each pipelined stage. Although charge-mode amplification can suppress commom-mode, it still degrades resolution. The non-linearity of the input charge generation circuit is another source of error.

2.5 Charge-Domain Operation Using Bubket-Brigade Device(BBD)

In this techinique, bucket-brigade devices are used for charge domain operation [17]. A simplified circuit describing charge-transfer stage is shown in Figure 2-5. Initially, the charge-transfer clock voltage (V_T) is high and the input is precharged to V_{PCH}. Then, the injected input charge (Q_{IN}) is stored on capacitor (C). A charge-trasnfer starts when V_T goes low. A negative V_T step is coupled to the input of amplifier via C and the $M1$ is turned on by the amplifier output. The amplifier drives the gate of $M1$ until V_S settles to the reference voltage (V_o). The charge trasnferd to the output which is calculated in Figure 2-5 is equal to the injected input charge (Q_{IN}) plus a constant offset ($C(V_{TL} - V_{TH} + V_{PCH} - V_O)$).

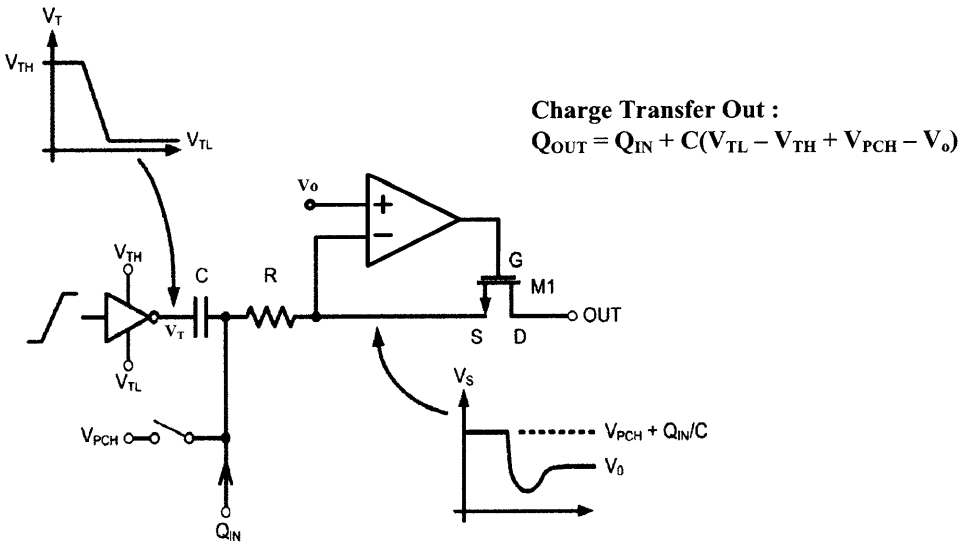

Figure 2-5: Boosted BBD charge-transfer stage and operating equation

For actual ADC implementaton, a comparator should be added at the input and the reference siganl should be added based on the output of the comparator. Because the transfered charge to the output is the same the injected charge at the input, the gain of pipelined stage can be implemented by scaling the capacitor (C) size. However, due to the parasitic capacitance at the V_s node, the gain can be diffent from ideal value. Also, V_PCH and V_O should be chosen properly to control the offset of the transfered charge at the output.

2.6 Summary

In this chapter, several ideas to implement pipelined ADCs without op-amps have been described. These methods are common in that more energy efficient circuits replace op-amps for redisue amplification. However, compared to the op-amp based amplification, these techniques suffer from inaccuracies and sensitivity to many design parameters. A technique which is robust and capable to replace op-amps in pipelined ADCS will be introduced in the next chapter.

Chapter 3

Comparator Based Switched Capacitor Circuits

Comparator based switched capacitor (CBSC) circuits, are another technique to remove op-amps in pipelined ADCs [18] and other analog circuits. Because it only replaces op-amps and maintains the whole structure of op-amp based pipelined ADC, this technique is robuster than any other techniques explained in Chapter 2. Also, other techniques developed for op-amp based pipelined ADCs can be applied, such as offset cancellation[19], correlated level shifting (CLS)[20]. In this chapter, basic ADC operations of comparator based switched capacitor circuit, prior works done based on this technique, and new ideas for better performance and high efficiency are described.

3.1 Comparator Based Switched Capacitor Operation

Comparator based switched capacitor circuits, shown in Figure 3-1 with timing diagram, operate similarly to op-amp based switched capacitor circuits. The sampling phase of a comparator based circuit is identical to the sampling phase of the op-amp based circuit. For bottom plate sampling, ϕ_{1e} opens sampling switch earlier than in-

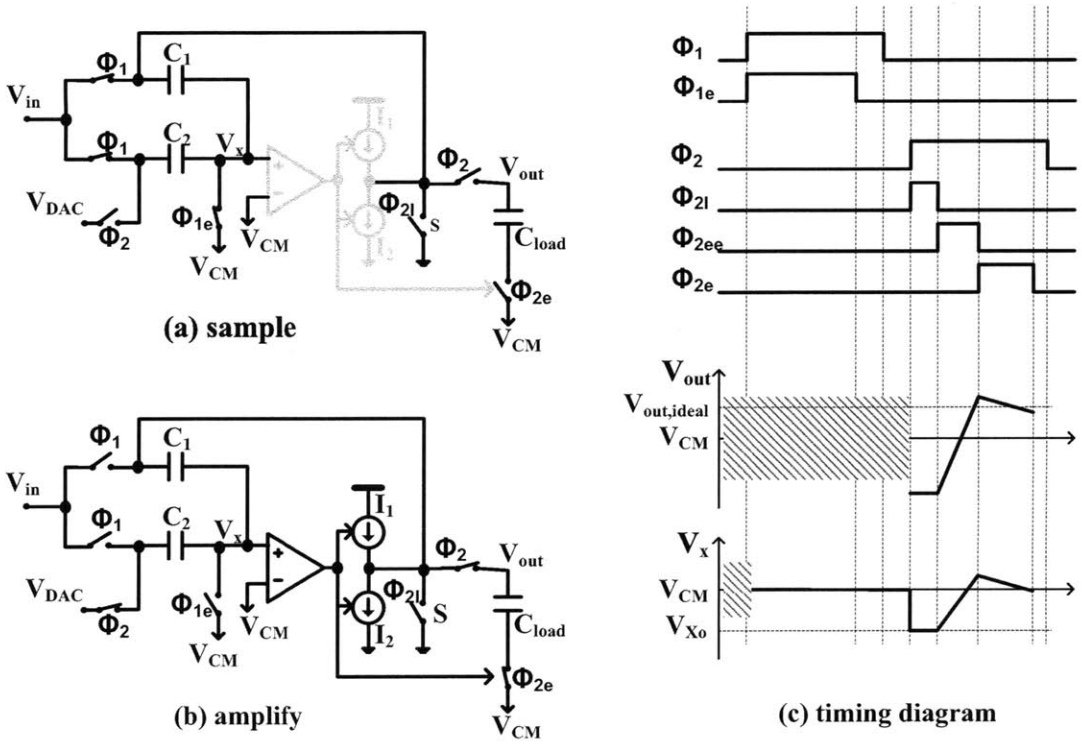

Figure 3-1: Comparator based switched capacitor operation

put switches. The charge transfer for amplification is divided into three sub-phases: a preset phase ϕ_{2I}, a coarse charge transfer phase ϕ_{2ee}, and a fine charge transfer phase ϕ_{2e}.

During the preset phase, C_2 is connected to the DAC output voltage (V_{DAC}) and the output of the stage is connected to the lowest system voltage through switch S. This causes V_x to step down and results in V_{Xo} being less than V_{CM} over the entire range of input voltages. When the coarse charge transfer phase ϕ_{2ee} starts, a coarse current source I_1 is turned on and charges the output for a fast and rough estimate of the output voltage and virtual ground condition. When the comparator detects virtual ground condition, the current source I_1 is turned off. The finite delay of the comparator and the high output ramp rate results in a significant overshoot of the correct value. During the fine charge transfer phase ϕ_{2ee}, a fine current source I_2 discharges the output to get a more accurate measurement of the virtual ground

condition and consequently a more accurate value for the output voltage. The fine phase current I_2 is much smaller than the coarse phase current I_1 and in the opposite direction. This relieves strict constrain on comparator delay without causing a large final overshoot. When the comparator detects the second threshold crossing, the sampling switch of the load capacitance C_{load} is opened. This defines the end of amplification and locks the sample charge on the load capacitance. The I_2 current source is turned off slightly after the sampling switch opens, but the extra current it sinks does not disturb the sampled charges because it only discharges the parasitic capacitance at the output node.

3.2 Error Source of Comparator Based Switched Capacitor Circuits

When a CBSC circuit detects the virtual condition, all the circuit node have the same condition as op-amp based amplification. However, every circuit node condition at that instance is changing unlike op-amp based amplification where all circuit nodes are settled to final condition. Thus, error sources are different from op-amps based amplification and steady state analysis for noise is not applicable under certain conditions.

One of the major sources of error is the output overshoot cause by finite delay of the comparator. In the first order, the overshoot is the product of ramp rate at the virtual ground condition and the delay of the comparator. The average of the overshoot over the output range corresponds to a fixed offset, and the variation of the overshoot over the output range is considered as non-linearity.

$$V_{overshoot}(V_{out}) = \frac{dV_{out}}{dt}(V_{out}) \times t_{delay}(V_{out}) \quad (3.1)$$

$$= V_{offset} + V_{non-linearity}(V_{out}) \quad (3.2)$$

$$V_{offset} = \overline{(V_{overshoot})}_{V_{out}} \quad (3.3)$$

$$V_{non-linearity}(V_{out}) = \frac{dV_{out}}{dt}(V_{out}) \times t_{delay}(V_{out}) - \overline{(V_{overshoot})}_{V_{out}} \quad (3.4)$$

Generally, a fixed offset of ADCs is more tolerable than non-linearity of ADCs, because it can be removed by analog or digital means. In equation 3.4, compared to the output ramp rate($\frac{dV_{out}}{dt}(V_{out})$), the comparator delay ($t_{delay}(V_{out})$ is relatively weak function of the output, because the comparator input is always the same when charge transfer ends, regardless of output. Thus, non-linear ramp rate caused by finite impedance of current source is the dominant source of non-linearity.

$$V_{offset} \approx \overline{(\frac{dV_{out}}{dt}(V_{out}))}_{V_{out}} \times t_{delay} \quad (3.5)$$

$$V_{non-linearity}(V_{out}) \approx (\frac{dV_{out}}{dt}(V_{out}) - \overline{(\frac{dV_{out}}{dt}(V_{out}))}_{V_{out}}) \times t_{delay} \quad (3.6)$$

More detailed analysis on non-linearity of CBSC technique can be found in [21]. In [10], effects from the finite impedance of current source are analyzed and compared with op-amp based amplification.

The dominant noise source of CSBC circuit is the comparator. A power efficient comparator design for a given noise requirement is studied in [22]. The noise from current source is only effective during the delay of comparator, because the noise of current source before the virtual ground condition does not affect the final value of the output. In [23], noise from switches in CBSC is analyzed using impulse sensitivity function (ISF).

3.3 Prior works based on CBSC

The first prototype of the CBSC pipelined ADC was demonstrated in [18]. It replaced the op-amp with a threshold detection comparator and current source. To achieve high gain in the comparator, several gain stages were cascaded together. Even though the op-amp was eliminated, the power consumption in the multi-stage comparator was considerable. Due to the single-ended implementation, the resolution was limited by the noise from the power supply and the substrate. The overall performance was 8 MS/s with 10b resolution (8.6 effective number of bits (ENOB)) consuming 2.5mW in a 0.18um process.

In a later design, a more power efficient zero-crossing detector was used to replace the comparator in the original CBSC design [24]. The dynamic zero-crossing detector almost completely removed the static current and significantly improved power efficiency. However, the implementation was still single-ended, once again limiting the resolution. In this design, each capaciot had a current source for sampling and charge transfer. Thus only the mismatched current between the stages flows through the switch, and the voltage drop across the switches with finite on-resistance which causes non-linearity is reduced. This resulted in a 200MS/s, 8b (6.4b ENOB) pipelined ADC which consumed 8.5mW in a 0.18um process.

To improve the robustness against substrate, power supply, and common-mode noise, a differential design was implemented [25]. Thanks to the differential implementation, the input range was doubled in spite of the lower power supply voltage. The differential zero-crossing detector was composed of a preamplifier followed by a dynamic threshold-detecting latch. This approach increased the resolution at the expense of static current. For high-speed operation, a large current source was required with high output impedance. However, there was a strong trade-off between current sourcing capacity and output impedance, especially in the single-phase charge transfer scheme. This design achieved 50 MS/s, 12b (10 ENOB) resolution, and 4.5mW power consumption in a 90nm process.

Recently, to solve the problem of finite current source output impedance, a new

Table 3.1: Performance table of prior ADCs based on CBSC

	[18]	[24]	[28]	[29]	[25]	[27]	[30]	[31]	[20]	[32]	[33]
Architecture	pipe	pipe	pipe	Σ-Δ	pipe	Σ-Δ	pipe	pipe	pipe	pipe	pipe
Resolutoin	10b	8b	10b	12b	12b	12b	8b	10b	12b	12b	8b
Technology(nm)	180	180	65	180	90	45	180	180	180	90	90
Conv. Rate(MS/s)	7.9	200	23	2.56	50	50	20	10	20	100	60
SNDR(dB)	52	40.3	54.3	65.3	62	47.7	44.2	53.3	68.3	64.4	44.2
Power(mW)	2.5	8.5	1.78	0.42	4.5	0.63	4.64	1.95	17.7	6.9	5.9
FoM(pJ/step)	0.8	0.51	0.16	6.98	0.088	1.9	1.6	0.51	0.41	0.051	0.7

type of current source was explored to the achieve ramp linearity [26]. Instead of biasing the gate with a static voltage from a current mirror, a dynamic bias voltage is generated on the gate to compensate for the decreasing ramp rate at the output node. The simulation results showed improved ramp linearity without increasing power consumption or circuit complexity.

Besides the aforementioned zero-crossing based pipelined ADC, the zero-crossing based circuit technique has also been applied to other types of ADCs. A delta-sigma ADC employed zero-crossing-based integrators to achieve low power operation in [27]. The technique has also been used with an op-amp to make a hybrid correlated level-shifting (CLS)-opamp/ZCBC pipelined ADC [20], which removes the effect of the finite impedance of the current sources.

Table 3.1 summarizes recently published ADCs based on CBSC.

3.4 Possible Improvements

Originally, the CBSC technique was developed with two phase charge transfer (course/fine charge transfer) scheme for high accuracy. After that, however, even single phase charge transfer could achieve medium to high resolution at high conversion frequency [24], [25], [28], [32]. However, a strong trade-off between current sourcing capacity and output impedance of current source limits the performance in single phase charge transfer design. In two-phase charge transfer, saved time through fast and rough estimation of the output voltage in course charge transfer phase can be utilized for accurate charge transfer. Thus, two phase charge scheme is reconsidered in this

project.

While the zero-crossing detector in [24] is more power efficient than the general purpose comparator in [18], it can not be used for two phase charge transfer (course/fine charge transfer) explained in Section 3.1. It is because while the zero-crossing detector in [24] can detect virtual ground condition only uni-directionally, the dual phase charge transfer scheme shown in Figure 3-1 requires to detect bi-directional virtual ground condition. It is possible to use two separate zero-crossing detectors for two different directions, but it consumes more power and increases circuit area and complexity. Thus, a uni-directional two phase charge transfer scheme is proposed for this project. In uni-directional two phase charge transfer scheme, both coarse and fine current sources charge the output node in the same direction. The conceptual difference between uni-directional two phase charge transfer scheme and bi-directional two phase charge transfer scheme is shown in Figure 3-2. This modification also requires two zero-crossing detectors in the same direction but different detection level, but it can be easily implemented without increasing power comsumption and circuit complexity. Detail explanation on the zero-crossing detector design is described in Chapter 5.

There are other side benefits from uni-directional two phase charge transfer scheme. First, transient effects from turning on and off current source can be reduced. In the uni-directional two phase charge transfer scheme, both coarse and fine current sources (I_1 and I_2) are turned on at the beginning of the coarse phase, and only I_1 is turned off at the end of coarse phase. However, the bi-directional two phase charge transfer requirs to turn off I_1 and to turn on I_2 at the end of coarse phase. Thus, the transient disturbance from turning on I_2 can be reduced. Another benefit is the trajectory of output voltage is shorter than the bi-directional two-phase charge transfer scheme. It not only saves power unnecessarily consumed to charge/discharge output voltage but also increases conversion frequency.

Another possible improvement can be achieved by supply voltage scaling. For digital circuits, voltage scaling is a powerful tool to minimize switching energy at optimal operating frequency [34]. However, voltage scaling has not been investigated

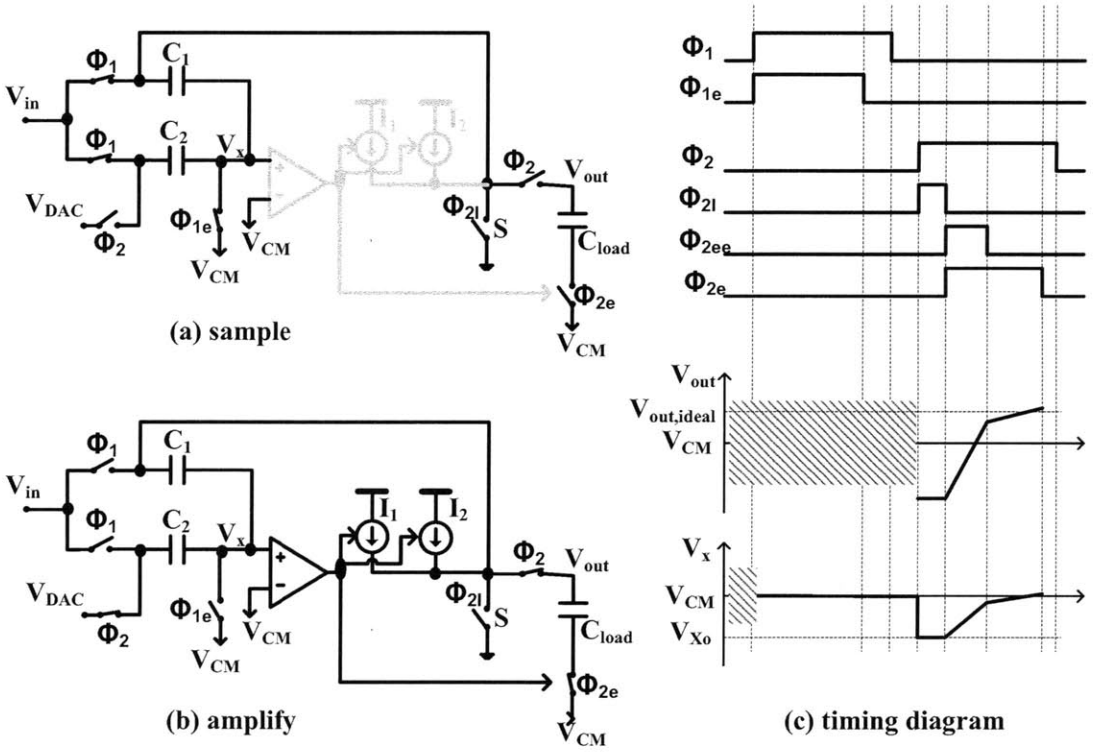

Figure 3-2: proposed uni-directional two phase charge transfer technique

actively in pipelined ADCs. In this project, eliminating op-amps enables highly digital implementation of pipelined ADC and allows to take advantage of voltage scaling. More detail voltage scaling effects on ADC are covered in the next Chapter.

Chapter 4

Voltage Scaling

A small voltage swing in modern CMOS process reduces switching power (CV^2f) significantly in digital circuits. When the operating speed requirements are relaxed, further supply voltage scaling improves energy efficiency and leads to minimum energy dissipation for given function [34]. However, this benefit from supply scaling is generally not applicable for ADCs. This chapter explains supply voltage scaling effects on general ADCs and how the ADC proposed in Chapter 3 scales supply voltage for better energy efficiency.

4.1 Voltage Scaling Effects on ADCs

Generally, motivations of voltage scaling of analog circuits including ADCs are different from digital circuits. First, voltage scaling enables analog circuits to be integrated with digital circuits. By integrating analog circuits with digital circuits, the cost for the entire system can be reduced and either numerous I/O pins or high-speed I/O design can be avoided. Also, supply voltage is sometimes constrained by other design factors. For example, utilizing a single solar cell for energy scavenging requires as low voltage operation as 400mV, unless a DC-DC converter is integrated in the design [35].

In spite of the motivations mentioned before, supply voltage scaling of ADCs has not been pursued actively. The main reason is that it is very difficult to design

ADCs operating at low supply voltage. Due to voltage headroom, cascode structure, which is essential for analog building block, such as bias circuits, current sources and op-amps, can not be widely used at low supply voltage. Non-ideal switching operation at low supply voltage is another problem. Reduced overdrive voltage of switches decreases on/off resistance ratio, which can not be solved by proper sizing of switches. Bigger on-resistance causes significant voltage drop across switches and slow transient responses. Smaller off-resistance causes leakage current and degrades sampled signal.

The signal to noise ratio (SNR) is another aspect to consider when voltage scaling is applied to analog circuits. While outputs of digital circuits have the same quality unless there is error, the output signal quality of analog circuits measured by SNR is affected by noise. As supply voltage is scaled, maximum signal output power is also scaled. Assuming the noise power does not depend on power supply, relative signal power to noise is worse at low supply voltage. Thus, voltage scaling of analog circuits degrades output quality when output quality of analog circuits is limited by supply voltage independent noise, such as thermal noise of sampling capacitor (kT/C).

Minimizing energy dissipation per function is the major motive of voltage scaling in digital circuits. Similar effects on ADCs can be analyzed through Figure of Merit (FoM) which is a measure of energy efficiency of ADCs. A widely accepted FoM is [36]

$$FoM = \frac{P_{diss}}{f_s \times 2^{ENOB}} \tag{4.1}$$

where $ENOB = \frac{SNDR(dB)-1.76}{6.02}$, $SNDR$ is the signal-to-noise (and distortion) ration and f_s is the sampling frequency.

Power consumption of ADC can be divided into analog static power and digital switching power.

$$FoM = \frac{P_{static} + P_{switching}}{f_s \times 2^{ENOB}} = \frac{V_{DD} I_{static} + \alpha C V_{DD}^2 f_s}{f_s \times 2^{ENOB}} \quad (4.2)$$

wherer α is activity factor of digital circuits.

When the output quality is limited by thermal noise,

$$2^{ENOB} = SNR = \sqrt{\frac{\overline{v_{sig}^2}}{\overline{v_n^2}}} \quad (4.3)$$

The signal power($\overline{v_{sig}^2}$) and noise power($\overline{v_n^2}$) are

$$\overline{v_{sig}^2} = K_{sig} {V_{DD}}^2 \quad (4.4)$$

$$\overline{v_n^2} = S_i(f) \times f_n = m8kT\frac{\gamma}{g_m} \times (N+1)\ln(2) f_s = K_{noise}\frac{1}{g_m} f_s \quad (4.5)$$

where K_f is $\frac{1}{8}$ in single ended input or $\frac{1}{2}$ in differential input case, $S_i(f)$ is noise power spectral density, f_n is noise bandwidth, m accounts for noise from devices other than the input devices, γ is noise factor, g_m is the transconductance of the input transistors and N is the targetting accuracy of ADCs in bits [11].

Defining $V_p \equiv I_D/g_m$ for the input devices, the static power consumption is

$$P_{static} = I_{static} V_{DD} = K_{pow} I_D V_{DD} = K_{pow} g_m V_p V_{DD} \quad (4.6)$$

where K_{pow} reflects the power consumption in the other parts than the input stage.

From Equations 4.2 $\sim$ 4.6

$$FoM = \frac{V_{DD}I_{static} + \alpha C V_{DD}^2 f_s}{f_s \times 2^{ENOB}} \tag{4.7}$$

$$= \frac{K_{pow} g_m V_p V_{DD} + \alpha C V_{DD}^2 f_s}{f_s \sqrt{\frac{K_{sig}{V_{DD}}^2}{K_{noise}\frac{1}{g_m} f_s}}} \tag{4.8}$$

$$= K_{pow}\sqrt{\frac{K_{noise}}{K_{sig}}}\sqrt{\frac{g_m}{f_s}} V_p + \sqrt{\frac{K_{noise}}{K_{sig}}} \alpha C \sqrt{\frac{f_s}{g_m}} V_{DD} \tag{4.9}$$

If the sampling frequency (f_s) is limited by the unity gain grequency (f_t),

$$f_s = K_f f_t = K_f \frac{g_m}{K_{ft}} \tag{4.10}$$

where K_f is the ratio between the f_s and f_t and K_{ft} is the ration between f_t and g_m which is typically gate-source capacitance C_{gs}.

From Equations 4.9 and 4.10

$$FoM = K_{static} V_p + K_{switching} \alpha C V_{DD} \tag{4.11}$$

The first term on the right side of equation 4.11 is from the analog static power and is not scaled by supply voltage. However, the second term on the right side of equation 4.11 results from digital switching power which is proportional to V_{DD}. This implies that supply voltage scaling of ADC can improve energy efficiency of ADC only when the digital power is dominating analog power. Recently, mostly digital ADCs, such as SAR ADC [37],[38], stochastic flash ADC [39], flash ADC with comparator redundancy [40] and ring VCO based sigma-delta ADC [41],[42], show good energy efficiency at low supply voltage. However, the architectures chosen for digital implementation, such as SAR and flash ADC, limit the resolution relatively low. Table 4.1 summarizes recently published ADCs operating at low supply voltage.

Table 4.1: Performance table of ADCs operating at low supply voltage

	[41]	[37]	[43]	[40]	[39]	[38]
Architecture	Σ-Δ	SAR	pipe	flash	flash	SAR
Supply Voltage(V)	0.2	0.5	0.5	0.4	0.9	0.6
Resolutoin	8b	6b	8b	6b	6b	10b
Technology(nm)	90	90	90	180	180	130
Conv. Rate(MS/s)	3.4	1.5	10	0.4	18	10
SNDR(dB)	44.2	35.3	48.1	32.5	33.6	51.8
Power(uW)	0.44	14	2400	1.66	631	46
FoM(fJ/step)	57	240	1150	125	900	9.6

4.2 Voltage Scaling for This Project

A pipelined ADC is a good candidate for better resolution at low supply voltage. However, it is extremely difficult to design op-amps at low supply voltage and energy efficiency (FoM) can not be improved by supply voltage scaling because the static op-amp power dominates overall power consumption [43]. In this project, a highly digital pipelined ADC is implemented using zero-crossing based circuit technique. Zero-crossing based circuit technique is simple and easy to design at low supply voltage. Also, unlike other op-amp based pipelined ADCs, supply voltage scaling can improve energy efficiency (FoM) because overall power consumption is dominated by digital power.

The proposed zero-crossing based pipelined ADC operates at normal voltage when high performance is required. When performance requirements are relaxed, supply voltage can be scaled down for better energy efficiency until either conversion frequency or resolution requirement limits further voltage scaling. This supply voltage scaling based on the required performance provides high energy efficiency over a wide range of sampling frequencies and resolutions.

Chapter 5

Zero-crossing Based Pipelined ADC

A fully differential zero-crossing based ADC is designed. The uni-directional two phase charge transfer, explained in the previous chapters, is used for high speed and high resolution. Supply voltage scaling for better energy efficiency is another feature of this ADC. This chapter focuses on the detail implementation of the proposed zero-crossing based pipelined ADC.

5.1 Block Diagram

The block diagram of the ADC designed for this project is shown in Figure 5-1. There are 7 stages for the entire ADC. The first stage is composed of a 3.3-bit flash subADC and multiplying digital-to-analog converter (MDAC) which multiplies the residue by a factor of 4. The subsequent stages (stage 2 to stage 6) are identical, consisting of a 2-bit flash subADC and x4 MDAC. Compared to the first stage, the subsequent stages are successively scaled down by a factor of 2 to reduce power. Stages 3 to 6 are not scaled down further because the power consumption in the second stage is already small, so further scaling does not have a large effect on the overall power consumption. Also, further scaling may exacerbate the mismatch. In the last stage, only a 2-bit flash ADC is required. However, to match the ramping speed of the last

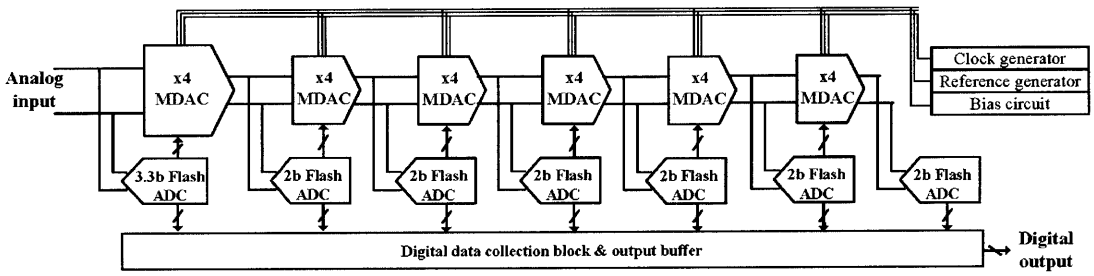

Figure 5-1: Block diagram of the proposed ADC

stage with the other stages, dummy capacitors and current sources are added.

5.2 Sampling Network

In this ADC, dedicated sample and hold (S/H) circuits are not used. Instead, sub-ADCs have separate capacitors for their S/H function. This can save power consumed in S/H circuits. However, sampled voltage in the MDAC can be different from the sampled voltage in the subADCs. To reduce the difference between the sampled voltage in MDAC and in subADCs, the same unit capacitors and switches are used. Figure 5-2 shows the sampling network. The unit sampling capacitor in the first stage is $C = 90fF$ and the total sampling capacitor is $12 \times 90fF = 1.08pF$ single ended and $0.54pF$ differential. This capacitance corresponds to $88\mu V_{rms}$ of thermal noise (kT/C), which correspones to ENOB of 12.4 bits at $1.67V_{pp}$ input range.

To lower the on-resistance of switches, bootstrapped input switches are used [44]. By applying constant V_{gs}, input range of the ADC can be increased without reliability issues. Also, bootstrapped switches are required for supply voltage scaling.

5.3 Flash ADC

Typically, flash ADCs are used for subADCs in pipelined ADCs. The flash ADC of the first stage in this project is shown in Figure 5-3. The subADC of the first stage has 9 bit decision comparators, which gives 3.3bits.

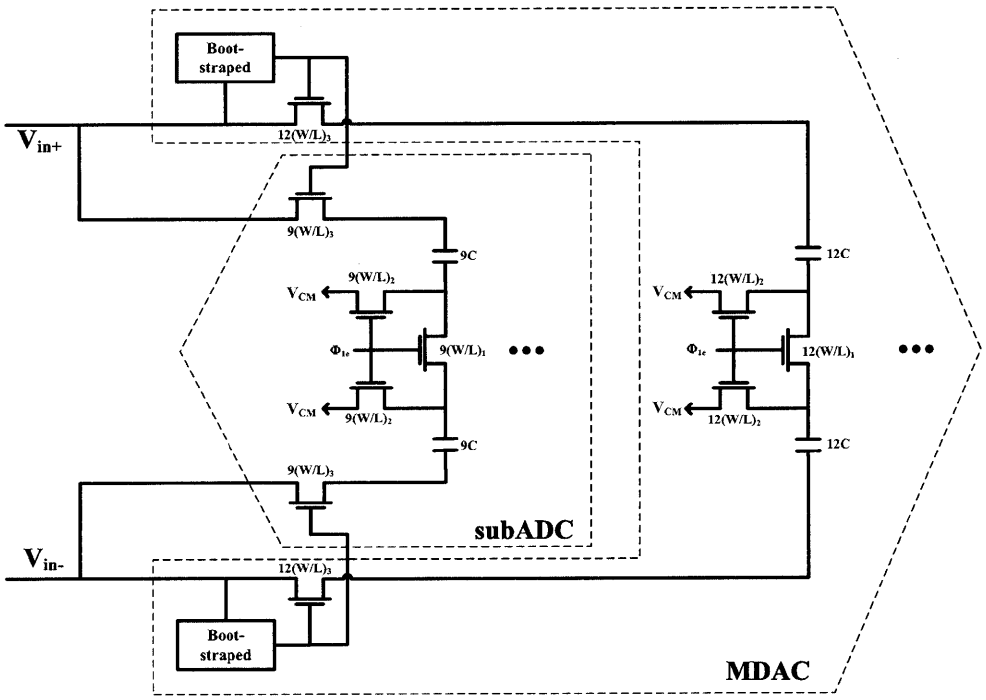

Figure 5-2: Sampling switches and sampling capacitors in the proposed ADC

The input signal is sampled on capacitors by bottom plate switches when ϕ_{1e} goes down. This sampled signal must be resolved by subADC before the amplification phase (ϕ_2) starts. After bottom plate sampling, the top plate of each capacitor is connected to the reference voltage generated by resistor ladder. This sets the input reference to the comparators. When the input voltages of comparators have settled, all comparators are enabled, and they produce digital thermometer output code corresponding to input voltage. In this design, comparator enable signals are triggered when ϕ_1 goes down so that the output of comparator becomes valid before the amplification phase (ϕ_2) starts. These digital codes are sent to the MDAC to generate proper DAC reference voltages and combined with digital codes from other stages.

The subADCs in the following stages have the same structure as the first stage, but have less comparators due to small input range. Ideally, only 3 comparators are required in the later stages for 2bit decision. However, offsets in the bit deci-

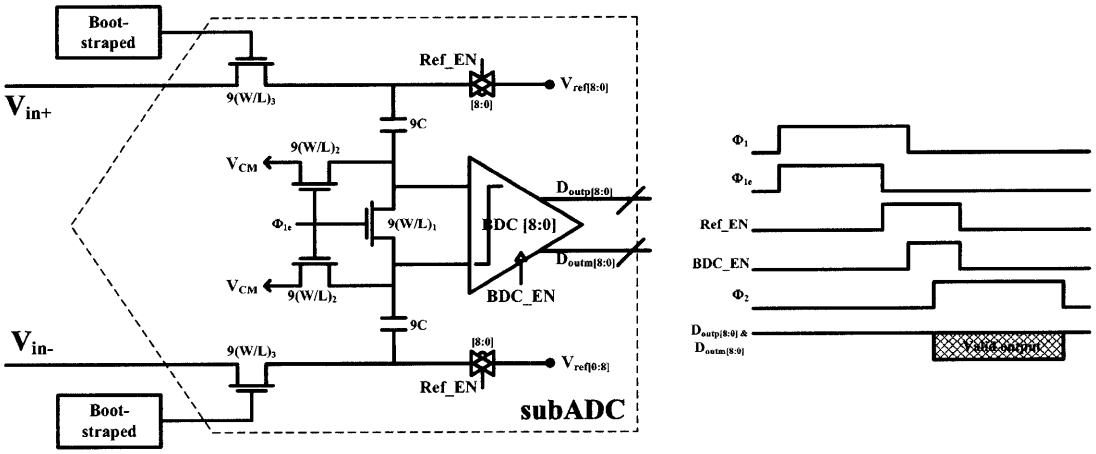

Figure 5-3: schematic of subADC for the first stage

sion comparators increase output range of the MDAC. For the over-range protection, additional 4 comparators are added. Thus, subADCs in the later stages have 7 comparators, but resolve nominally 2bits per stage.

5.3.1 Bit Decision Comparator

For bit decision comparators (BDCs), latched comparators are used. A latched comparator is composed of cross-coupled inverters, a differential input pair and enable switches. The schematic diagram of BDC is shown in Figure 5-4. When the BDC is not enabled, both D_{outp} and D_{outm} are pulled up to V_{DD} by PMOS switches. This resets all internal nodes and eliminates memory effects from the previous states. When the enable signal goes up, the NMOS transistors of cross-coupled inverters are connected to ground through input differential transistors. Based on the input voltage polarity, one of the input differential pairs pulls down the NMOS transistor of cross coupled inverters more strongly. This causes regenerative process in the cross-coupled inverters and latches the outputs (D_{outp} and D_{outm}).

The size of transistors in BDC is determined by the latch speed requirement and tolerable offsets. The latch speed is determined by regeneration speed, which is proportional to transconductance of inverters and inversely proportional to load capacitance [45]. For a fixed width of transistors, shorter lengths give higher transcon-

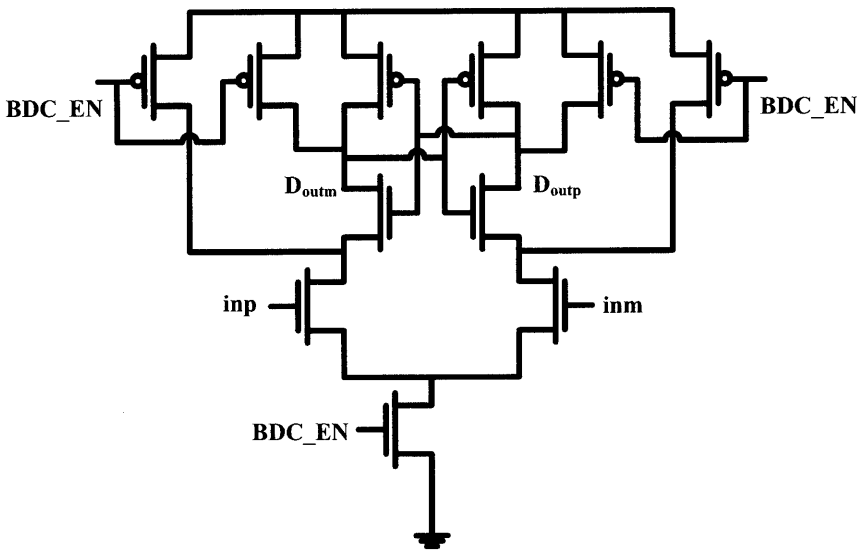

Figure 5-4: Schematic of bit decision comparator

ductance and smaller load capacitance. Thus, it is advantageous to use minimum length device for high speed operation. It is also true for input differential pairs. However, small devices have relatively poor matching between devices, which leads to larger offset. Especially, the mismatch between the input differential pair causes significant offset in BDC. The offsets in BDC increase the output range of MDAC which makes the current source more non-linear at the expanded output range.

In this design, proper size for both high speed and small offset is chosen based on the Monte Carlo simulation. The cross-coupled inverters are designed with minimum length device for fast operation, but 2x longer devices are used for the input differential pair to reduce offsets.

5.3.2 Voltage References for Flash ADC

The voltage references for flash ADC are generated by a resistor ladder, shown in Figure 5-5. The power consumed by this resistor ladder is static. As explained in Chapter 4, static current need to be scaled proportional to conversion frequency for high energy efficiency when supply voltage is scaled. While the conversion frequency

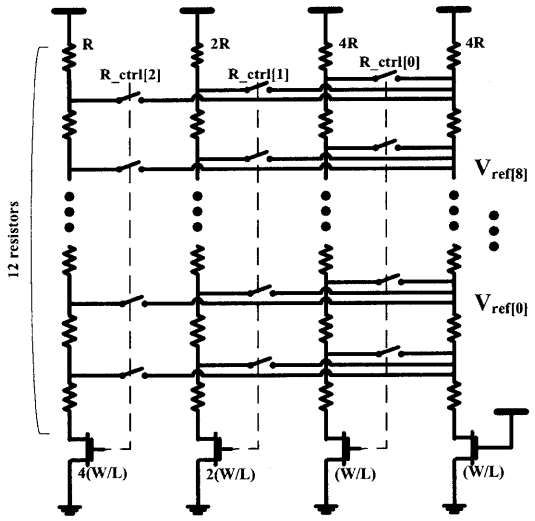

Figure 5-5: Schematic of voltage reference for flash ADC

goes down much faster than linear to supply voltage, the static current through the resistor is scaled linearly with the supply voltage. Thus, the power consumption in the resistor ladder becomes significant at low supply voltage.

To handle this problem, the binary weighted resistor ladders are designed. At normal supply voltage, all the switches in Figure 5-5 are shorted to reduce output resistance of reference voltages for faster settling time. By opening switches between resistor ladders, effective output resistance can be increased at low supply voltage and unused resistor ladder can be turned off to save power. Ideally, this resistor ladder provides 8x scaling for both static currents and the output resistance of voltage references.

5.4 Multiplying Digital-to-Analog Converter

The multiplying digital-to-analog converter (MDAC) is a main block of a pipelined stage. Conceptually, it subtracts the sampled input signal from DAC voltage, which is a rough estimate of the input signal, and generates a residue and amplifies the residue to recover the full signal range. A block diagram of MDAC for the proposed ADC is shown in Figure 5-6. In this project, sampling capacitors are split and connected to

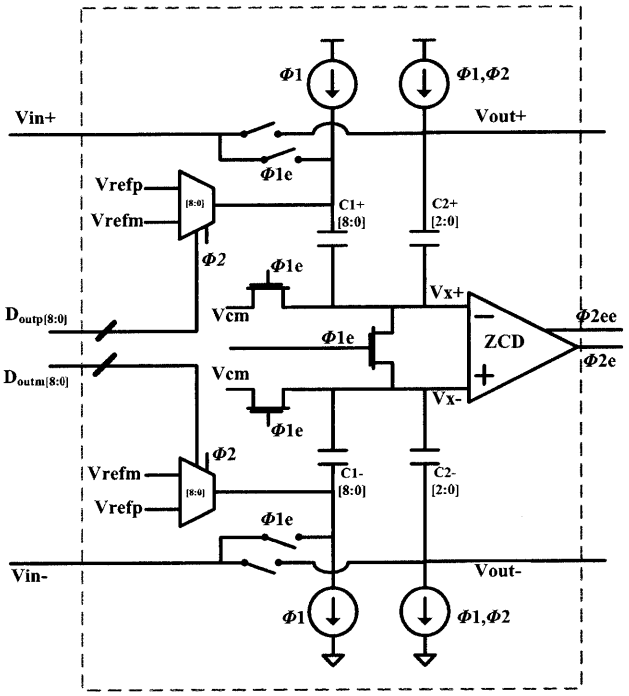

Figure 5-6: Schematic of MDAC for this project

either V_{refp} or V_{refm} based on the subADC output to generate the equivalent DAC voltage [10]. The ZCD and current sources are used to amplify residue by transferring sampled charge to feedback capacitors.

The residue plot of MDAC is shown in Figure 5-7. Since the first stage input is charged by external signal sources or buffers, a relatively large input range is used and 3.3 bits are resolved. The output range of first stage is reduced for improved linearity. The subsequent stages resolve 2bits per stage and have the same input and output range. However, input range of the subsequent stages is increased by adding additional comparators in subADCs. These additional bits from subADCs provide over range protection. When the supply voltage is scaled, the residue is also scaled linearly to the supply voltage by reducing the reference voltages.

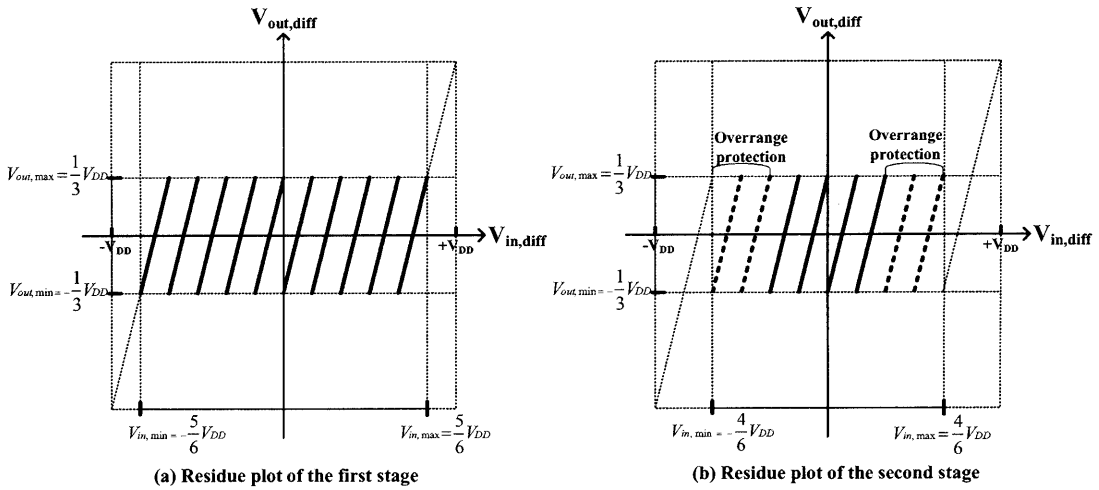

Figure 5-7: Residue plot of MDAC of the (a)first stage, (b)second stage

5.4.1 Zero-crossing Detector

The zero-crossing detector (ZCD) is composed of a preamplifier, inverters, and a level shifting capacitor. The preamplifier amplifies the input signal and converts the differential input to a single ended output. The inverters are used for threshold level detection. The schematic of ZCD is shown in Figure 5-8.

During the sampling phase (ϕ_1), the preamplifier and inverters are turned off by $M15$, $M16, M17$ to save power, and the capacitor ($C1$) for level shift is charged by a external voltage reference ($vset$). When the amplification phase starts (ϕ_2), the ZCD is turned on and the charged level shifting capacitor is connected between the two inverter inputs. When the input of ZCD ramps up, the output of preamplifier ($v1$) goes down and the capacitor ($C1$) shifts $v2$ down by the precharged voltage($V_{DD} - vset$). Thus, the output ϕ_{2ee} make an early decision than ϕ_{2e}. This ϕ_{2ee} tells the input of ZCD is close to virtual ground condition. On ϕ_{2ee}, the fine phase starts for accurate charge transfer. By adjusting the precharged voltage ($V_{DD} - vset$) across the level shifting capacitor, the ratio between coarse and fine charge transfer phases is determined. A typical timing diagram is shown in Figure 5-9.

The metrics to consider for the preamplifier are gain, noise, and the bandwidth. The gain of preamplifier reduces the effect of noise in the inverters and improves

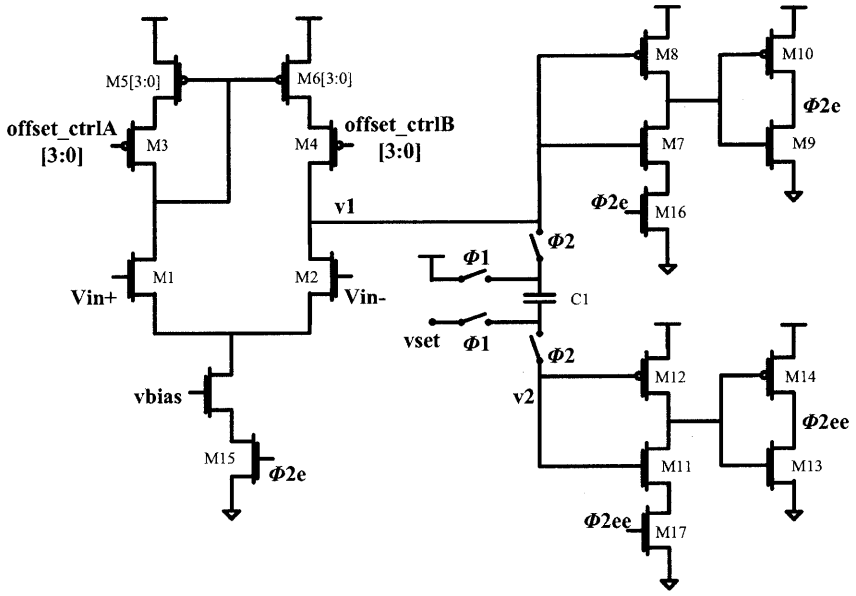

Figure 5-8: Schematic of ZCD for two phase charge transfer

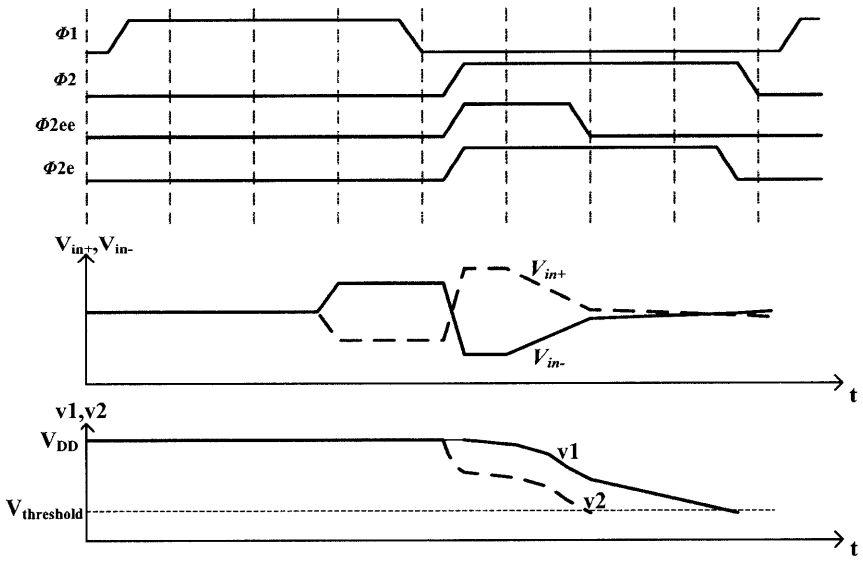

Figure 5-9: Timing diagram of ZCD operation

power supply and commom-mode rejection. The length of M1, M2, M5, and M6 are increased to achieve enough gain. Thus, high W/L ratio transistors are used for M1 and M2, but low W/L ratio transistors are used for $M5$ and $M6$ to reduce the input referred noise. Wide bandwidth of preamplifier is preferred, because it makes the ZCD response fast and reduces overshoots which cause offset and non-linearity. However, the bandwidth requirement is relaxed significantly by using the two-phase charge operation. It is because when the ZCD detects virtual condition during the fine charge transfer phase, the ramp rate is much slower than single phase charge transfer. The PMOS load of preamplifier (M5,M6) is composed of binary weighted transistors. Each binary weighted transistor is switched on/off by offset control signal ($offsetctrlA[3:0], offsetctrlB[3:0]$). By changing the relative size of PMOS transistor, the offset of the preamplifier can be adjusted [10].

When the required speed or resoultion is relaxed, the supply voltage is scaled for better power efficiency. In this design, as explained in Chapter 4, the static current is also scaled proportionally to the conversion frequency. In this case, the gain of preamplifier (A_v) and input referred noise ($\overline{v_{n,ir}{}^2}$) can be written as following.

$$A_v = g_{m_n}(r_{o_p}||r_{o_n}) \tag{5.1}$$

$$= K_{g_m}\sqrt{I_{static}}(\frac{1}{\lambda_p I_{static}}||\frac{1}{\lambda_n I_{static}}) \propto \frac{1}{sqrtI_{static}} \quad \text{(in strong inversion)} \tag{5.2}$$

$$= K_{g_m} I_{static}(\frac{1}{\lambda_p I_{static}}||\frac{1}{\lambda_n I_{static}}) \propto constant \quad \text{(in weak inversion)} \tag{5.3}$$

$$\overline{v_{n,ir}{}^2} = 2(\overline{v_{n,n}{}^2} + (\frac{g_{m_p}{}^2}{g_{m_n}})\overline{v_{n,p}{}^2}) \tag{5.4}$$

$$\propto (\frac{1}{g_{m_n}} + \frac{g_{m_p}}{g_{m_n}{}^2}) \times bandwidth \tag{5.5}$$

$$\propto (\frac{1}{g_{m_n}} + \frac{g_{m_p}}{g_{m_n}{}^2}) \times \frac{1}{C_{out}(r_{o_p}||r_{o_n})} \tag{5.6}$$

$$\propto \sqrt{I_{static}} \quad \text{(in strong inversion)} \tag{5.7}$$

$$\propto constant \quad \text{(in weak inversion)} \tag{5.8}$$

As shown in equation 5.3 and 5.8, static current scaling proportional to conversion frequency does not hurt the preamplifier performance in terms of gain and input referred noise.

The inverters are optimized for threshold detection in one direction. Because $v1$ and $v2$ always goes down in this design, the size of M8, M9, M12, and M13 are made much larger than the size of M7, M10, M11, and M14.

5.4.2 Current Source

For the two-phase charge transfer operation, each current source in Figure 5-6 must be able to adjust the current sourcing capacity. The current sourcing capacity can be changed by either changing bias voltage of current sources or by turning on/off part of current sources. Changing the bias voltage of current sources saves area, because one current source can be used for both coarse and fine charge transfer. However, changing the bias voltage of current sources causes transient effects which limit current source linearity. For this project, current sourcing capacity is changed by turning on/off part of current sources. As shown in Figure 5-10, each current source is consist of 6 identical unit current sources. All 6 current sources are used for the coarse charge transfer phase, and 5 current sources are turned off at the end of the coarse charge transfer phase so that only one current source is used for the fine charge transfer. This enables current sourcing capacity adjustment by 6x. To increase the current sourcing range further, the bias voltage of the current source used for fine charge transfer is separated from other current sources. By applying smaller bias voltage to the current source for fine charge transfer, the current for fine phase can be reduceed significantly without changing the current for coarse phase much. It gives additional 2x-4x current sourcing range.

Each unit current source has a NMOS current source and a PMOS current source, but only one of them is enabled during operation and the other current source is always kept off. This improves supply noise rejection [10] and makes the layout more symmetric at the cost of increased area. Though two phase charge transfer reduces the output impedance requirement, longer than minimum length transistors are cascoded

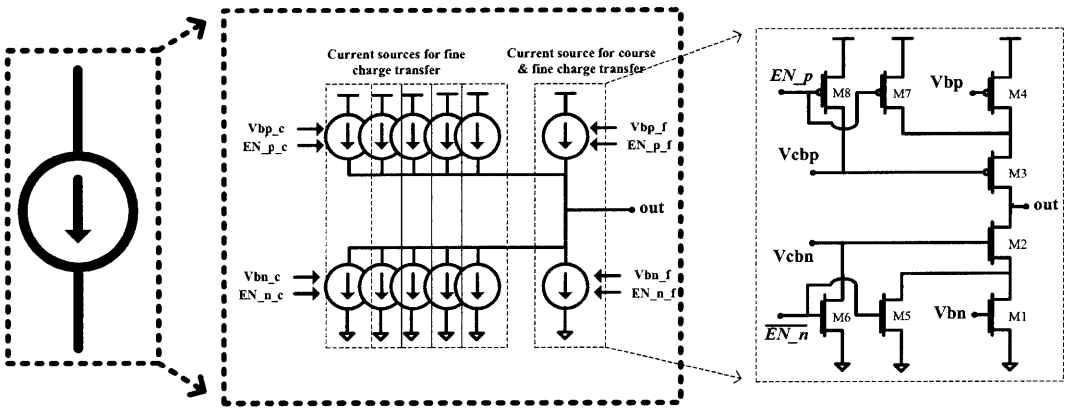

Figure 5-10: Schematic of current source for two phase charge transfer

for better output impedance.

In the uni-directional two phase charge transfer, the delay in turning off the coarse current sources is important. Until the coarse current sources are turn off after the ZCD makes coarse decision (ϕ_{2ee}), the coarse current sources still charges/discharges the output voltage. It can affect the fine charge transfer phase accuracy, because the fine charge transfer phase needs enough time to settle transient effects from turning off the coarse current sources. In this design, current sources are turned off by switching cascode voltage (V_{cbp}, V_{cbn}) using $M6$ and $M8$. It allows the bias voltages (V_{bp}, V_{bn}) to reamin constant so that the transient effect of turning on/off can be reduce. However, for example, when V_{cbp} is switched to V_{DD} by $M8$, C_{gs} of $M3$ raise the source voltage of $M3$ higher than V_{DD}. It keeps $M3$ turned on and increases turn off time of the current source. Thus, additional switches ($M5, M7$) are added to the source of cascode transistors. These switches prevent the source voltage of cadcode trasnsistors ($M2, M3$) to be higher than V_{DD} or lower than ground, which helps to turn off the current sources fast.

5.4.3 Voltage References

Based on the output of the subADC, the DAC reference voltage is generated and subtracted from the input voltage to generate a residue. The number of required DAC

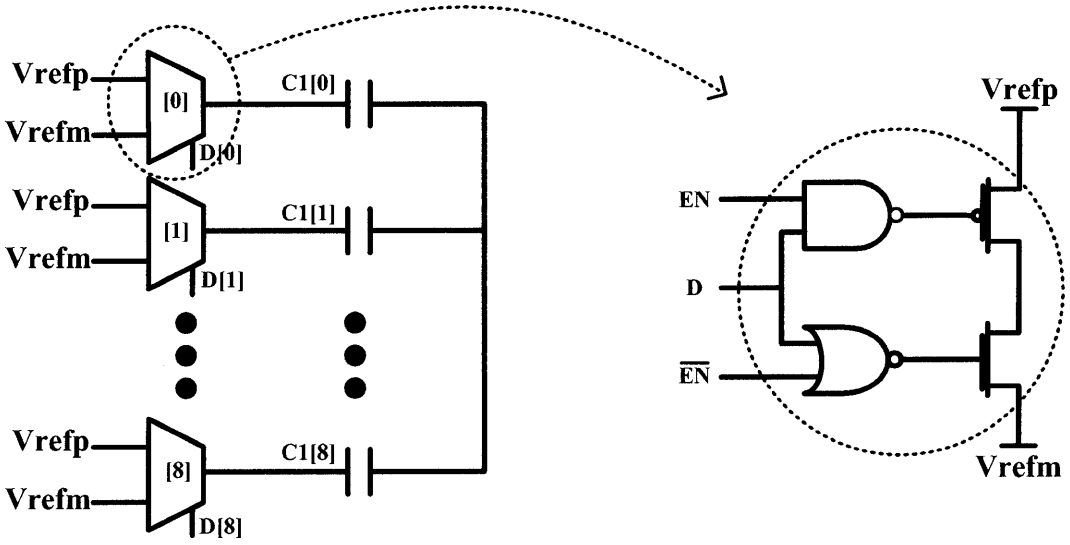

Figure 5-11: DAC reference voltages using splitted capacitors

reference voltages increases exponentially with the subADC resolution. Thus, when the subADC resolve multi-bits, the linearity of the DAC can limit the overall linearity performance. In this design, the DAC reference voltages are generated by split capacitors. Instead of connecting all capacitors to the corresponding DAC voltage, split capacitors are connected either V_{refp} or V_{refm}. It is shown in Figure 5-11.

Using this technique, highly linear DAC voltage can be avoided. However, this design depends on the capacitor matching, because the mismatch in capacitors causes equivalent non-linearity [10]. Considering modern nono scale processes provides excellent capacitor matching, it is a reasonable technique. Switches for V_{refp}, V_{refm} are implemented as analog multiplexer, shown in Figure 5-11.

5.4.4 Optimization of Uni-directional Two Phase Charge Transfer

As explained in Section 5.4.2, this design can adjust current sourcing capacity more than 20x. Based on this wide range of capacity, the ratio between the coarse charge transfer current and the fine charge transfer current can be optimized. The goal of

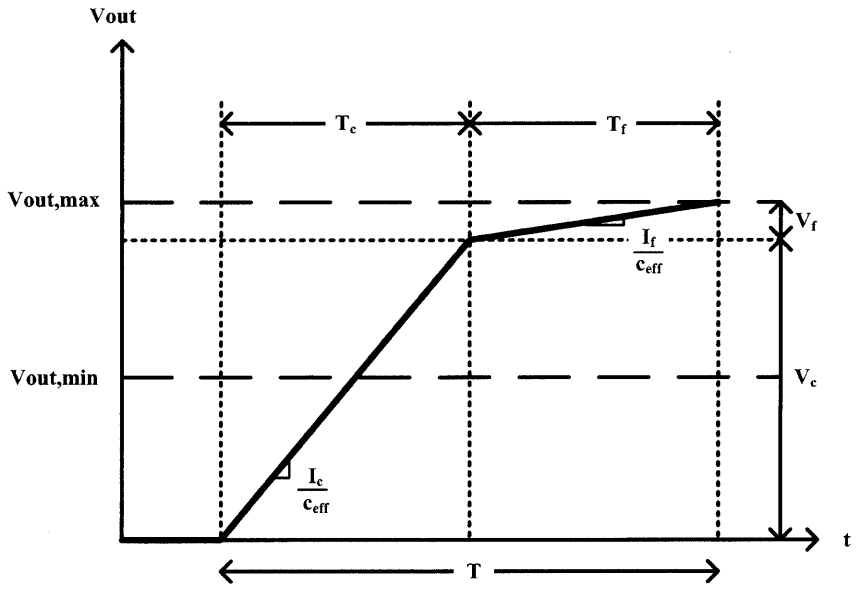

Figure 5-12: Output voltage during charge trasnfer phase

the optimization is to complete the charge transfer as accurately as possible for given time for the charge transfer, for the given performance (delay, gain, and noise) of the ZCD. The accuracy is estimated from the fact that lower ramp rate (small current) for the fine charge transfer phase gives better accuracy. Figure 5-12 shows the single ended output voltage during the charge transfer phase.

To complete the charge transfer within the given time T,

$$V_c + V_f = V_{out,max} \tag{5.9}$$

$$\frac{V_c}{\frac{I_c}{C_{eff}}} + \frac{V_f}{\frac{I_f}{C_{eff}}} < T \tag{5.10}$$

where V_c and V_f are the output voltage changes during coarse and fine charge transfer phase respectively, I_c and I_f are the current during coarse and fine charge transfer phase respectively, and C_{eff} is the effective capacitance at the output node.

At the end of the coarse phase, the ramp rate of the output voltage varies with the output voltage due to the finite output impedance of current sources. Because

the output impedance of the current source is inversely proportional to I_c, it is reasonable to assume that variation of output voltage at the end of the coarse phase is proportional to I_c. Also, the larger I_c causes more transient effects from turning off I_c. Thus, to cover this variation and transient effects, V_f must be made proportional to I_c.

$$V_f = K_{vf} I_c \tag{5.11}$$

Assumming $V_c \gg V_f$, Equation 5.9 becomes,

$$V_c \approx V_c + V_f = V_{out,max} \tag{5.12}$$

From Equations 5.10, 5.11, and 5.12,

$$T \geq \frac{V_c}{\frac{I_c}{C_{eff}}} + \frac{V_f}{\frac{I_f}{C_{eff}}} \approx \frac{V_{out,max}}{\frac{I_c}{C_{eff}}} + \frac{K_{vf} I_c}{\frac{I_f}{C_{eff}}} \tag{5.13}$$

$$\geq 2\sqrt{\frac{V_{out,max}}{\frac{I_c}{C_{eff}}} \frac{K_{vf} I_c}{\frac{I_f}{C_{eff}}}} \tag{5.14}$$

$$\geq 2C_{eff}\sqrt{\frac{V_{out,max} K_{vf}}{I_f}} \tag{5.15}$$

$$\tag{5.16}$$

Thus,

$$I_f \geq \frac{4{C_{eff}}^2}{T^2} V_{out,max} K_{vf} \tag{5.17}$$

$$I_{f,min} = \frac{4{C_{eff}}^2}{T^2} V_{out,max} K_{vf} \quad \text{when} \quad \frac{V_c}{\frac{I_c}{C_{eff}}} = \frac{V_f}{\frac{I_f}{C_{eff}}} = \frac{T}{2} \tag{5.18}$$

Above analysis shows that I_f can be minimized when the time for coarse charge transfer and fine transfer are equal.

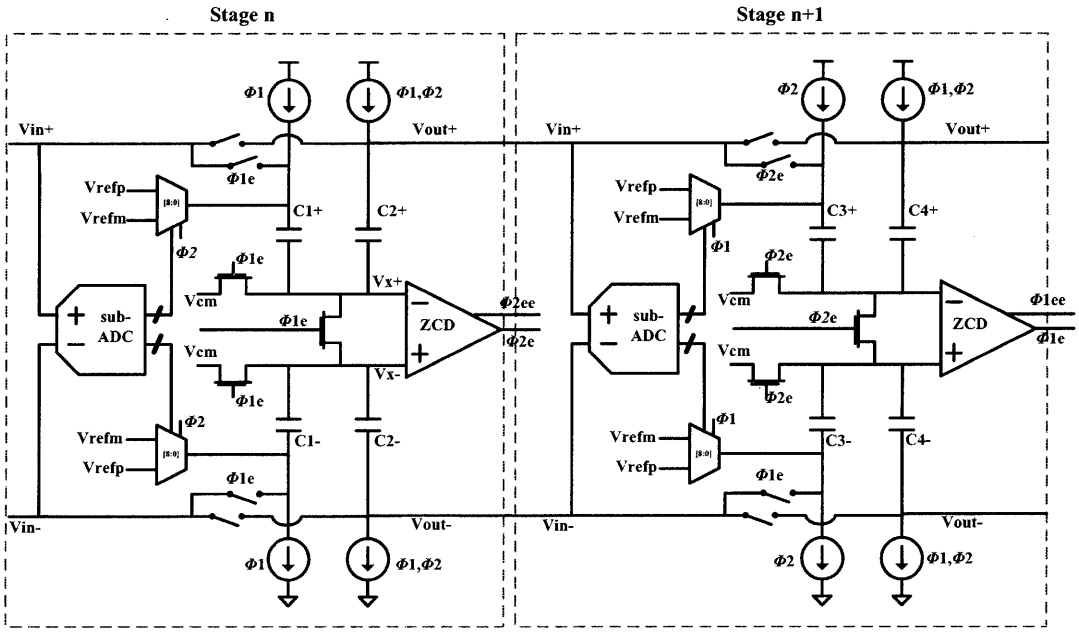

Figure 5-13: Pipelining two stages

5.5 Pipelined Stages

In pipelined ADCs, the sampled input is partly resolved in each stage and the output of one stage goes to goes the next stage. In op-amp based pipelined ADCs, all stages operats based on the clock signal and one stage hands over only the output to the next stage. However, in zero crossing based pipelined ADCs, one stage gives the output and the sampling signal to the next stage. Figure 5-13 shows the connection between two stages with brief timing information.

5.6 layout

Because ADCs are very sensitive to matching of devices and noise, the floor plan and the detail layout should be done carefully. Overall layout of the proposed ADC is shown in the Figure 5-14. It is implemented on a $2mm \times 2mm$ die. The actual size of the ADC is only $1450\mu m \times 500\mu m$. All stages are placed in a row so that signals can go through all stages in a short distance. Other peripheral blocks, such as BIAS,

subADC reference voltages, and the digital data collecting circuit, are placed close to the ADC core. Pad rings are separated in two segments. One of them is for analog signal, such as input signals, reference voltages, analog supply voltages, and the main clock. The other pad ring is for digital outputs and other digital signals, such as clock and data for configuration. Empty space is filled with decoupling capacitors on analog supply voltage and reference voltages.

The layout of the first stage is shown in Figure 5-15. Sub-blocks in a stage are placed in such way to maximize symmetry and to minimize interconnect lengths. Differential circuits, such as BDCs and ZCDs, are carefully laid out for symmetry. Also, deep-Nwell and Nwell guard rings are placed around ZCDs which are sensitive to noise.

Metal-oxide-metal (MOM) capacitors are used for capacitor arrays (sampling and feedback capacitors). In the process used for this project, MOM capacitors using all metal layers have about 3x bigger capacitance per area than MIM capacitors. The high capacitance density of MOM capacitor helps to minimize the layout area. However, due to the proximity to the substrate, MOM capacitors have larger parasitic capacitance at both terminals. To reduce parasitic capacitance, metal1 (M1) layer is not used for capacitor array. Also, to improve matching between the capacitors, dummy capacitors surround the capacitor arrays.

Subsequent stages have almost the same layout as the first stage, except they are scaled down 2x.

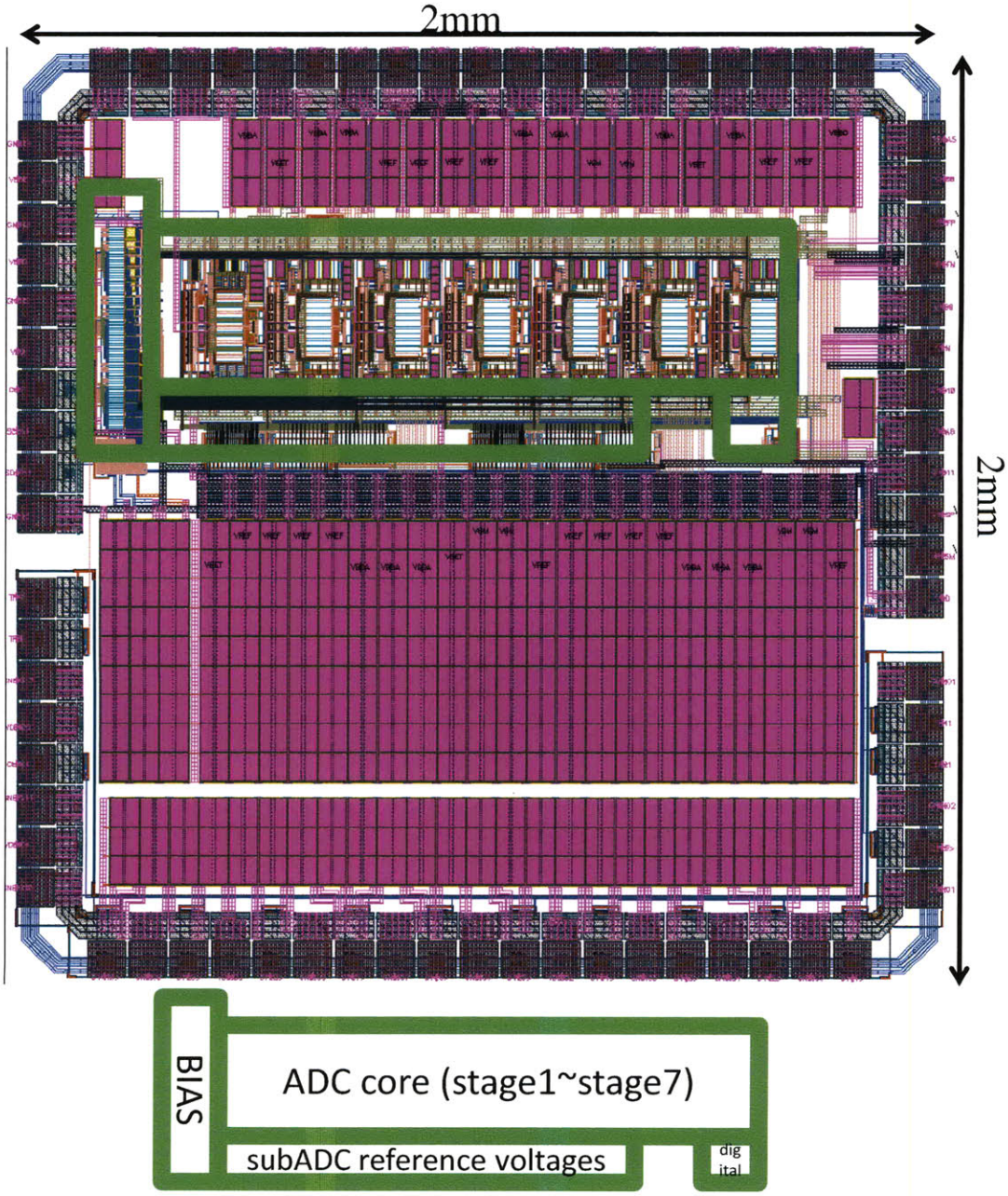

Figure 5-14: Top layout of proposed ADC

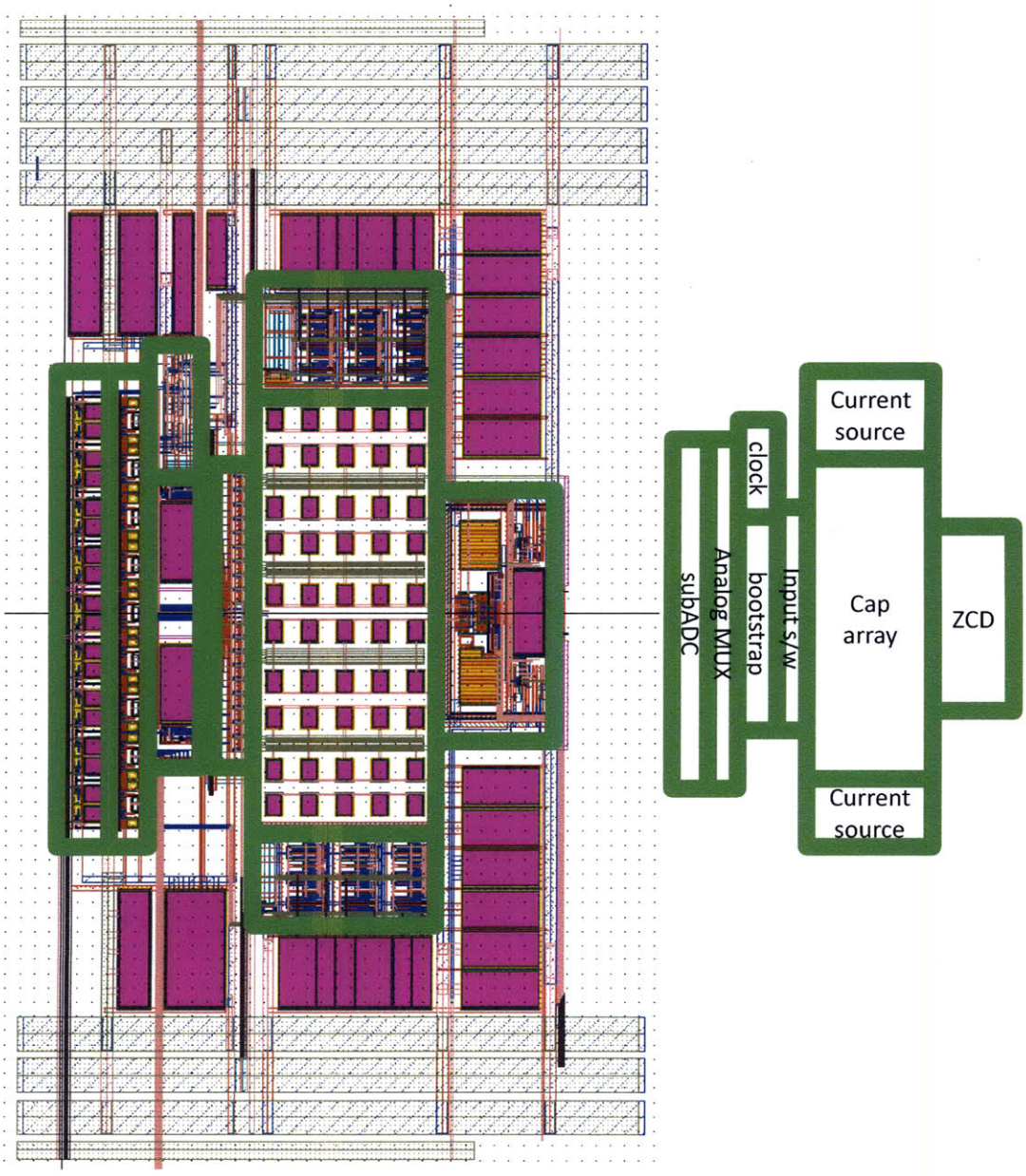

Figure 5-15: First stage layout of proposed ADC

Chapter 6

Simulation Result

In this chapter, simulation results of the proposed zero-crossing based pipelined ADC are presented. Each sub-block of the first stage is simulated first, and the entire first stage is then simulated, and finally the entire ADC is simulated. To show the supply voltage scalability, all simulation is done both at normal supply voltage ($1V$ V_{DD}) and the low supply voltage limit($0.5V$ V_{DD}).

6.1 Sampling Network

The sampling network is simulated with a sinusoid at input signal. The clock generation circuit, input capacitors, bootstraping input switches and bottom plate sampling switches are included in this simulation. 512 input samples are exported to MATLAB to analyze the frequency spectrum. The input frequency is chosen for coherent sampling around the Nyquist frequency. Figure 6-1 shows the result at $200MS/s$ with a $89.45MHz$ input signal at $1V$ V_{DD}. Figure 6-2 shows the result at $10MS/s$ with a $4.48MHz$ input signal at $0.5V$ V_{DD}. Both SNDR and SFDR calculated from sampled signal exceed for the target performance.

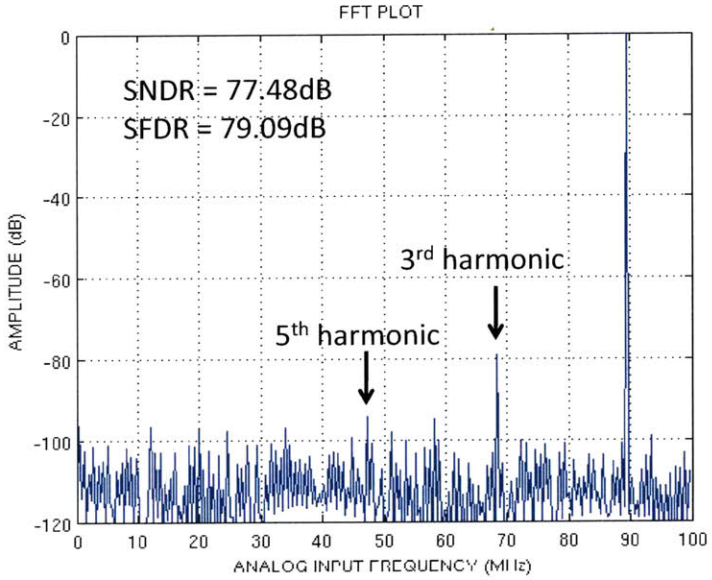

Figure 6-1: Simulation result of sampling network at $1V$ V_{DD}

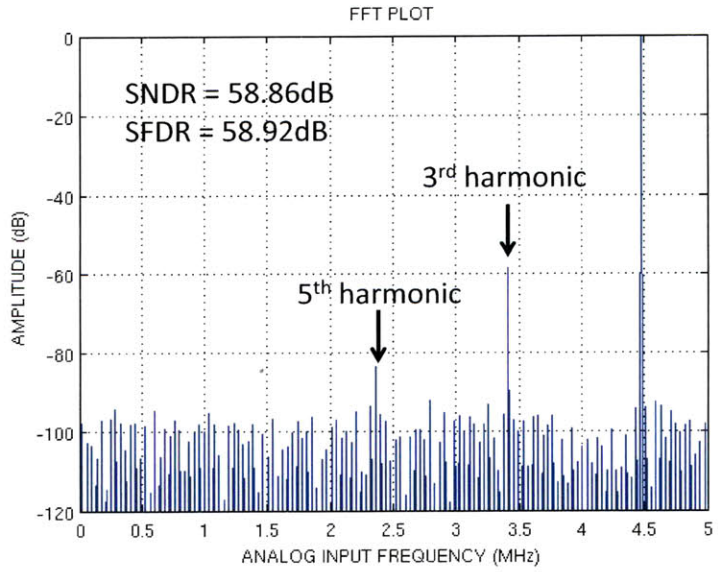

Figure 6-2: Simulation result of sampling network at $0.5V$ V_{DD}

6.2 BDC

As mentioned in Section 5.3.1, the offsets in BDC increase the output range of MDAC which makes the current source more non-linear at the expanded output range. The BDC offset is analyzed by Monte Carlo simulation. With the input voltage changing slowly, the BDC is enabled multiple times. When the BDC output trips, the input voltage is recorded. Simulation result is shown in Figure 6-3. The mean (mu) of offset is about $1.2mV$ and the standard deviation (sd) is about $5mV$. Because mismatch between the devices is the main reason for the offset, this mean and standard variation of offset does not change much according to supply voltage. Assuming normal distribution, more than 99% of the BDC offset is in the ± 3 standard deviation, which is about $\pm 15mV$. In this design, $\pm 20mV$ offset of the BDC is tolerable without degrading linearity.

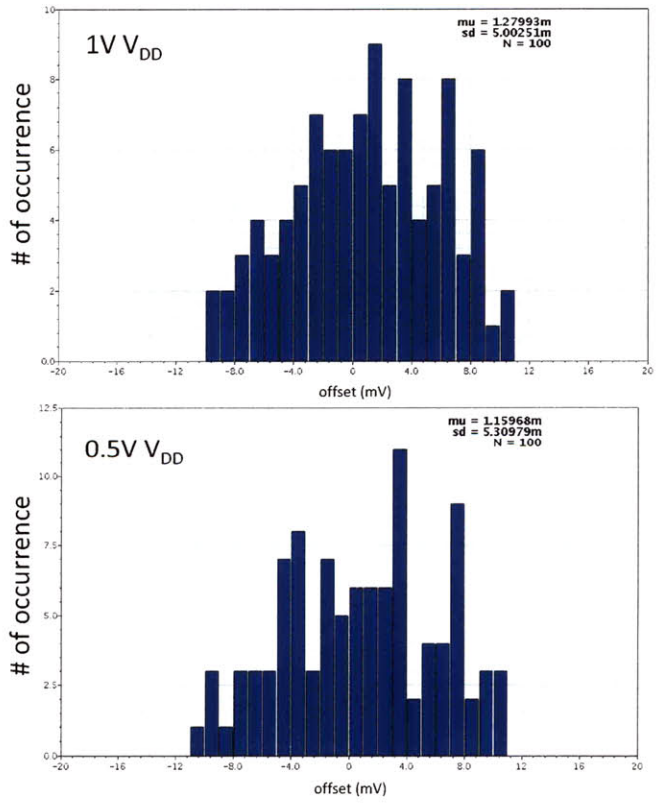

Figure 6-3: Monte Carlo simulation result of BDC offset at $1V$ V_{DD} and $0.5V$ V_{DD}

6.3 ZCD

In this design, the performance of the ZCD is mostly determined by the preamplifier in the ZCD. The gain and bandwidth of the preamplifier is simulated and shown in Figure 6-4. The bias current is adjusted according to the supply voltage. Gain is about 19(dB) at both $1V$ V_{DD} and $0.5V$ V_{DD}. The CMRR is about 28(dB) at $1V$ V_{DD} and 32(dB) at $0.5V$ V_{DD}. The CMRR is limited by the finite output impedance of the current mirror. Based on the simulation result, the input referred noise is about $0.17mV$ at $1V$ V_{DD} and $0.19mV$ at $0.5V$ V_{DD}. Considering the input full-scale range of $1.67V$ at $1V$ V_{DD} and $0.83V$ $0.5V$ V_{DD}, noise of preamplifier does not limit ADC performance. Another function of preamplifier is offset control. Offset is controlled by changing the width of PMOS load transistor pair. Figure 6-5 shows the input vs. output curves of the preamplifier with different offset control signal. Considering that the output is charging during the delay from the ZCD input to the sampling switches, a slight negative offset is necessary to compensate overshoot and keep the output range in the middle of the supply rails. Thus, the center of offset range is in the negative side.

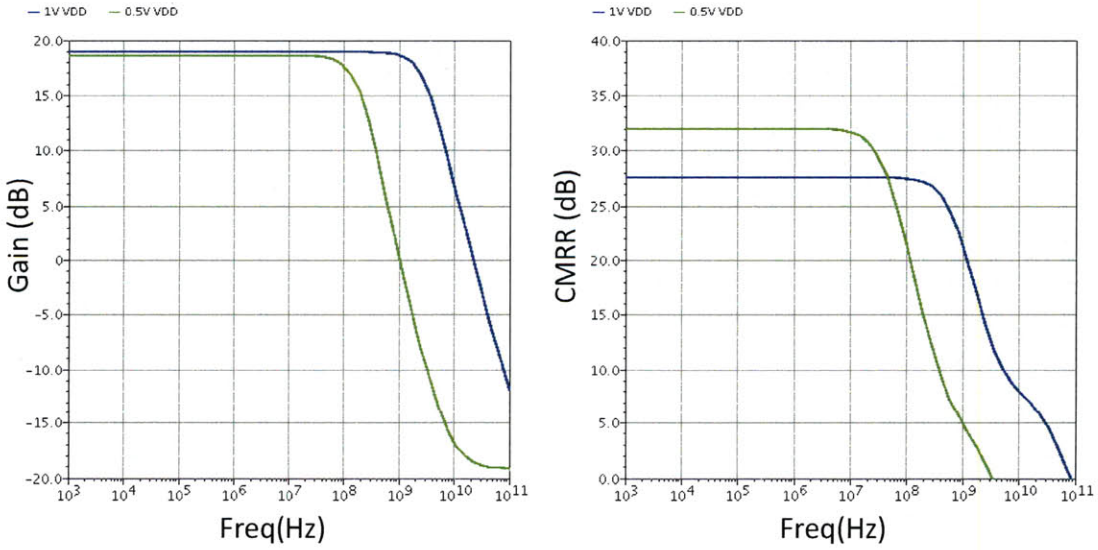

Figure 6-4: Simulation result of preamplifier gain and CMRR at $1V$ V_{DD} and $0.5V$ V_{DD}

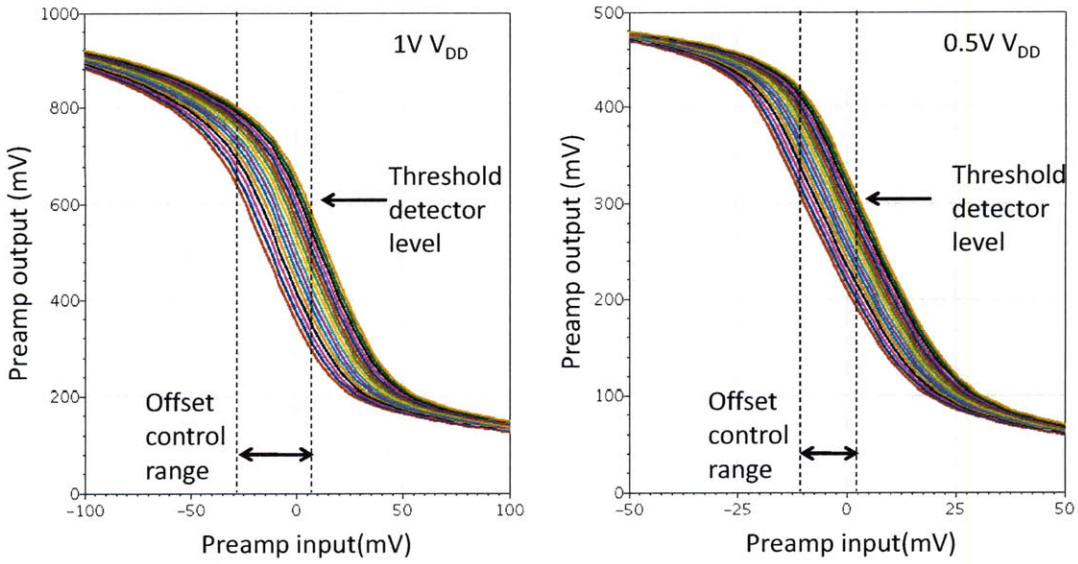

Figure 6-5: Simulation result of preamplifier offset control at $1V$ V_{DD} and $0.5V$ V_{DD}

6.4 MDAC

For simulation, the 2nd stage is modified to show the sampled 1st stage output accurately. The input voltage is swept linearly and the corresponding residue of the 1st stage is measured. About 100 points are sampled and plotted. Figure 6-6 shows the result of $150MS/s$ at $1V$ V_{DD}. To check the result more accurately, the residue differences between two consecutive samples are calculated later and shown in the bottom of the Figure 6-6. Because the input signal is linearly increasing by $20mV_{diff}/sample$, the MDAC, which has gain of 4, increases the residue by $80mV_{diff}/sample$. Based on the simulation result, the average step is about $79.96mV/sample$, which indicates the gain of MDAC is about 3.998. The variation of the step, which shows the non-linearity of the output, is about $0.4mV$. Considering the 4x gain of the first stage MDAC, this correspond to $0.1mV$ non-linearity error referred to the input, which exceeds the target performance. The same simulation result at $5MS/s$ at $0.5V$ V_{DD} is shown in Figure 6-7.

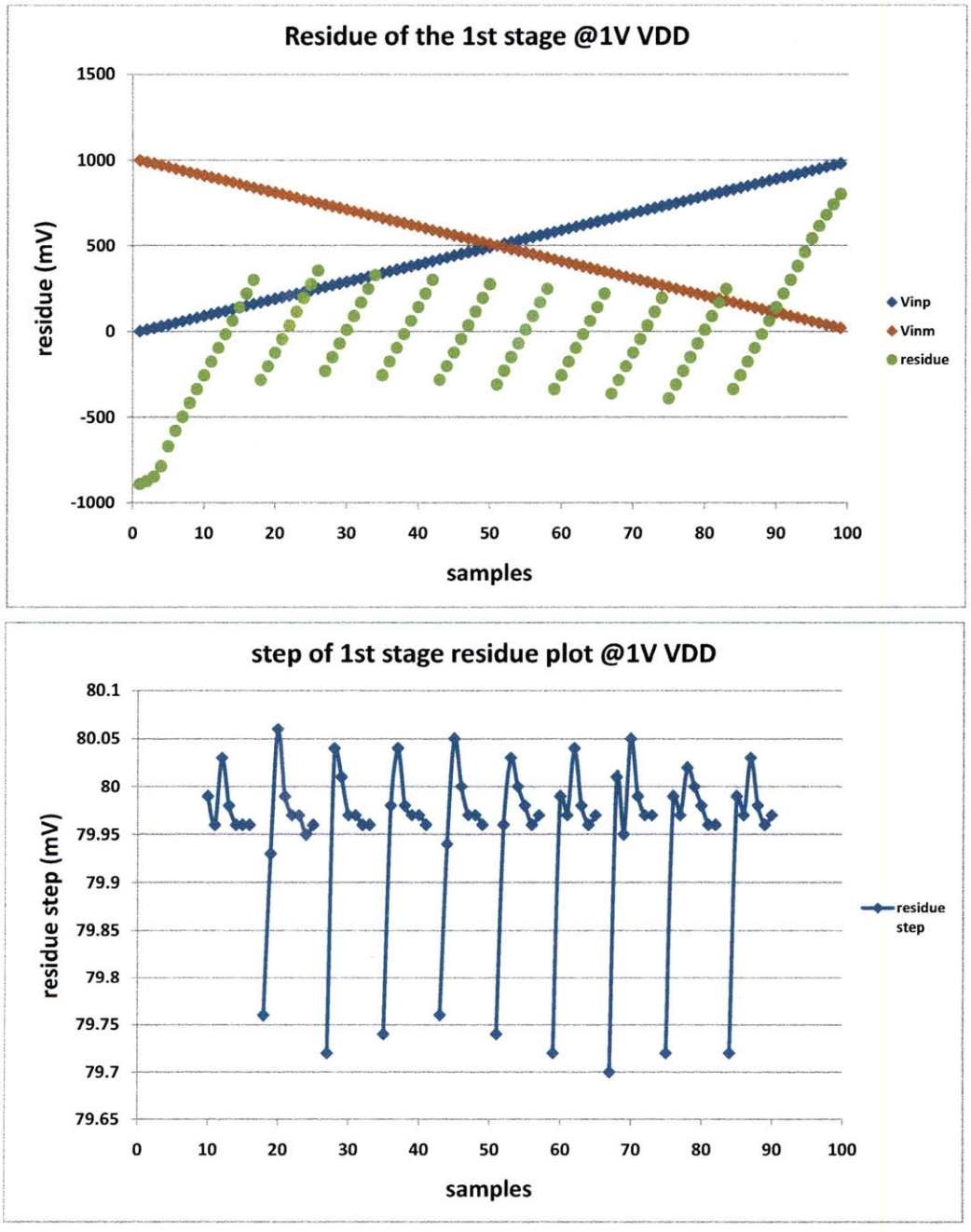

Figure 6-6: Simulation result of 1st stage at $1V$ V_{DD}

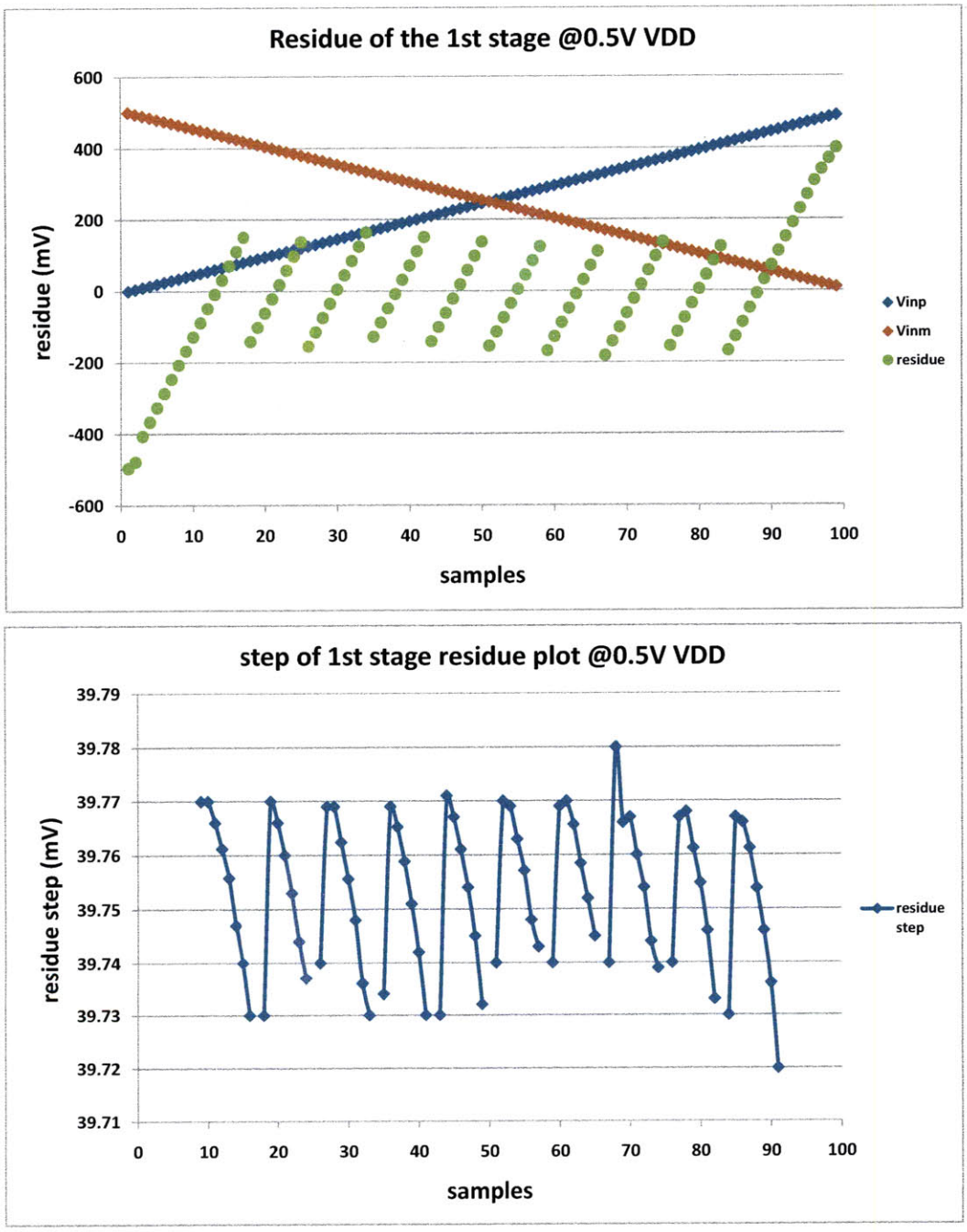

Figure 6-7: Simulation result of 1st stage at $0.5V$ V_{DD}

6.5 Overall ADC

To estimate the ADC performance accurately, all stages are simulated. All circuits designed for this project, such as hte bias, voltage references, the clock generation circuit, and the digital data combining circuit are included in this simulation. Similar to the MDAC simulation in the previous section, the input voltage is swept linearly and the digital data from all stages are combined and plotted. Figure 6-7 shows the result of $150MS/s$ at $1V$ V_{DD}. To check the result more accurately, the digital code differences between two consecutive samples are calculated and shown in the bottom of the Figure 6-7. Ideally, $20mV_{diff}/sample$ input step corresponds to $\frac{inputstep}{inputrange} \times$ (entire code range) $= \frac{20mV}{1.667V} \times 2^{15.3}(codes) = 492(codes)$. The simulation results match to this calculated value well. The variation of step is about ± 7(codes) $\approx 3bits$, which can be analyzed about 12.3 bit linearity. This simulation can not be performed at $0.5V$ V_{DD}, because it takes too much time and resources.

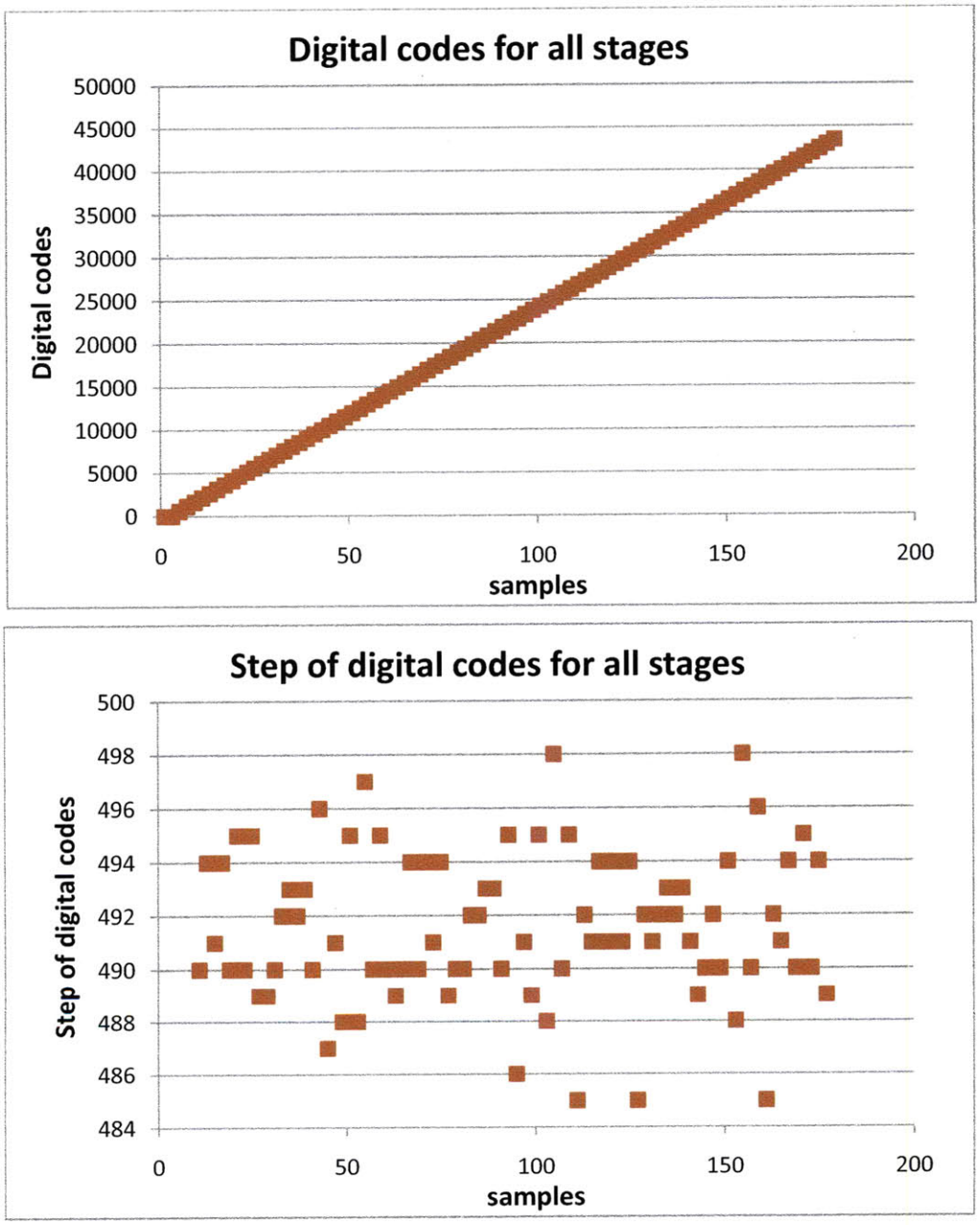

Figure 6-8: Simulation result of all stages at 1V V_{DD}

Chapter 7

Conclusion

7.1 Thesis Summary

In this thesis a zero-crossing based pipelined ADC with supply voltage scalability is described. Two main contributions of this thesis are 1) a modification of the zero-crossing based circuit techinique to achieve better performance and 2) an idea to apply supply voltage scaling to ADCs for better power efficiency.

Zero-crossing based circuits, which are recently develped circuit technique to replace power inefficient op-amps in analog circuits, are used for the pipelined ADC. To overcome the major source of the performance limit of zero-crossing based ciurcuits, which is a strong trade-off between current sourcing capacity and output impedance of current source, a uni-directional two phase charge trasnfer scheme is proposed. Also, the side benefits we can get from this proposed charge trasnfer scheme, such as improved power efficiency and accuracy, are shown in the thesis.

Voltage scaling is a powerful tool to minimize switching energy of digital circuits. The highly digital implementation characteristic of the zero-crossing based circuits enables voltage scaling. It is shown that the supply voltage scaling based on the required sampling frequency and resolution provides high energy effiency over wide range of sampling frequencies and resolutions.

To demonstrate these ideas, this thesis presents the design and implementation of a prototype IC. It is fabricated in a 65nm CMOS process and will be packaged,

targeting 13bit (11 ENOB) $200MS/s$ at $1V$ V_{DD} with 8mW power consumption and 11 bit (9 ENOB) 5MS/s at $0.5V$ V_{DD} with 0.11mW power consumption. This gives about $20fF/step$ to $40fF/step$ FOM, which is approximately 10 times better than state of the art in the same frequency and resolution range.

7.2 Future Work

The proposed ADC relies on voltage scaling to achieve high energy efficiency in wide range of frequencies and resoultions. Thus, an efficient on-chip DC-DC converter capable of delivering power at voltages from 1V down to 0.5V is needed in order to make the ADC a more integrated subsystem.

In this design, when supply voltages are scaled, conversion frequency goes down quickly, because of the increased resistance of sampling switches. New ideas for better switches at low supply voltage are required for aggressive voltage scaling.

Also, the zero-crossing based circuit techniques can be modified and optimized for the various ADCs which are targeting different performance. For example, for higher performance, more than two SAR ADCs can be pipelined and zero-crossing based circuit techniques can be used for residue amplification between two SAR ADCs. Also, for low performance, zero-crossing techniques can pipeline stages asynchronously in one-shot fashion, which enables to finish conversion statistically faster and gives better FOM.

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