Chapter 7. High-Frequency InAlAs/InGaAs Metal-Insulator-Doped Semiconductor Field-Effect Transistors (MIDFETs) for Telecommunications

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7.1 Introduction

Sponsors

Charles S. Draper Laboratory
Contract DL-H-418488
Joint Services Electronics Program
Contract DAAL03-89-C-0001

The goals of this project are to design, fabricate, test, and model submicron InAlAs/InGaAs Heterostructure Field-Effect Transistors (HFETs) on InP. These devices are of great interest for applications in long-wavelength lightwave communication systems and ultra-high frequency microwave telecommunications.

Metal-Insulator-Doped semiconductor Field-Effect Transistors (MIDFETs) in which the InGaAs channel is heavily doped but the InAlAs insulator is undoped were pioneered by del Alamo and Mizutani at NTT Laboratories.[1] These devices have been found to display a performance comparable to InAlAs/InGaAs Modulation-Doped FETs (MODFETs) of similar gate length. They additionally offer unique benefits not found in other device structures: reduced g_m and f_T collapse, higher breakdown voltage, and enhanced freedom for optimization of gate insulator parameters.

During the past year, we have studied the effect of increasing the InAs composition in the channel of the device in an effort to enhance its performance. In the process of carrying out this research, we have uncovered serious isolation problems that will need dedicated process technology work in the future. We have also continued our study of strain-insulator MIDFETs and examined the impact of dislocations on device performance. A detailed description of these experiments is presented in this report.

7.2 Strained-channel InAlAs/n$^+$-InGaAs MIDFETs

In this work, we investigated the effect of increasing the InAs mole fraction (x) in the $In_xGa_{1-x}As$ channel from that required to lattice match to InP (x=0.53). This work is motivated by the expected improvement in electron transport

[1] J.A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET with a Heavily-Doped Channel," *IEEE Electron Device Lett.* EDL-8 (11): 534-536 (1987); J.A. del Alamo and T. Mizutani, "Bias Dependence of f_T and f_{max} in an $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET," *IEEE Electron Device Lett.* EDL-9 (12): 654-656 (1988); J.A. del Alamo and T. Mizutani, "A Recessed-Gate $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIS-type FET," *IEEE Trans. Electron Devices* ED-36 (4): 646-650 (1989).

properties[2] and the enhanced conduction band discontinuity between the channel and the insulator[3] as the InAs composition increases.

Three wafers were grown by molecular-beam epitaxy in MIT's Riber 2300 system with cross sections shown in figure 1. The InAs mole fraction in the $In_{0.53}Ga_{0.47}As$ channel and subchannel were 0.53, 0.6, and 0.7. The 100Å subchannel is undoped and the 100Å channel is Si doped to a level of about 4.5×10^{18} cm^{-3}. The $In_{0.52}Al_{0.48}As$ gate insulator and buffer are undoped as is the $In_{0.53}Ga_{0.47}As$ cap. Device fabrication is similar to that described by del Alamo and Mizutani.[4]

I-V characteristics were measured for devices with a nominal gate length of 1 μm and width of 30 μm. The gate diode characteristics were measured with the drain and source shorted. Specially designed gate-diode structures were also measured in order to investigate the gate-channel leakage paths.

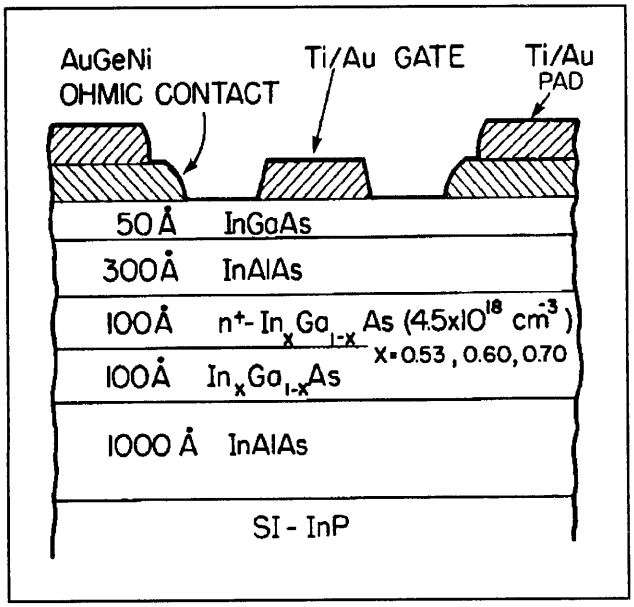

Figure 1. Cross section of $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ MIDFETs.

Figure 2 shows a plot of the tranconductance versus gate-source voltage of representative devices from the three wafers at a drain-source voltage of 3 V. For devices with x=0.53, 0.6, and 0.7, the peak g_m's measured (averaged over 10 devices) were 200 ± 22, 250 ± 14, and 296 ± 15 mS/mm respectively. The threshold voltages are −1.05 ± 0.09, −1.28 ± 0.20, and −2.09 ± 0.24 V respectively. Figure 3 shows the drain current versus V_{gs} at $V_{ds} = 3$ V. The peak drain currents measured over 10 devices were 320 ± 42, 424 ± 37, and 656 ± 69 mA/mm respectively, demonstrating the tremendous improvement in electron transport properties as the InAs mole fraction in the channel increases. However, as x increases, as seen in figure 3, the leakage current below threshold increases, preventing the transistor from shutting off.

Figure 4 shows the gate diode characteristics for $V_{ds} = 0$ V (for a clearer presentation, the forward scale has been expanded). The increased InAs mole fraction in the channel results in larger forward and reverse currents. In forward bias, this is contrary to what is expected from the enhanced ΔE_c between channel and insulator. The values of reverse breakdown voltage are −12.6,

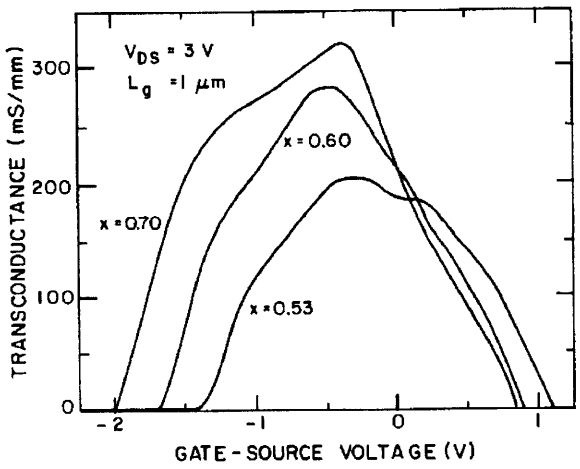

Figure 2. g_m versus V_{gs} with $V_{ds} = 3$ V for the three InAs mole fractions.

[2] U.K. Mishra, A.S. Brown, and S.E. Rosenbaum, "DC and RF Performance of 0.1μm Gate Length AlInAs-GaInAs Pseudomorphic HEMTs," *Proceedings of the International Electron Devices Meeting,* 1988, pp. 180-183.

[3] F.L. Schuermeyer, P. Cook, E. Martinez, and J. Tantillo, "Band-Edge Alignment in Heterostructures," *Appl. Phys. Lett.* 55 (18): 1877-1878 (1989).

[4] J.A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET with a Heavily-Doped Channel," *IEEE Electron Device Lett.* EDL-8 (11): 534-536 (1987).

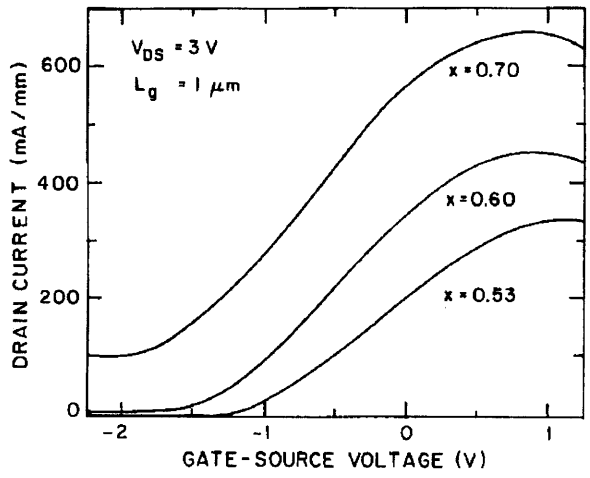

Figure 3. I_D versus V_{gs} with V_{ds} = 3V for the three InAs mole fractions.

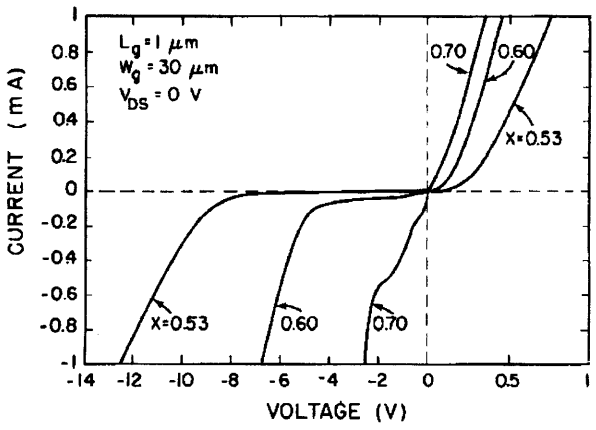

Figure 4. Forward and reverse diode characteristics of 1-μm MIDFETS for the three InAs mole fractions.

−6.7, and −2.6 V for x=0.53, 0.6, and 0.7 respectively. We have defined breakdown at a reverse gate current of 1 mA, which is about 10 percent of the peak drain current carried by the reference (x=0.53) device. The increased gate leakage current represents a serious shortcoming of enhanced InAs channels devices.

We have investigated the origin of this extra leakage current, and we attribute it to the presence of a direct leakage path between the gate and the channel at the edge of the mesa, as shown in figure 5. At the mesa edges, where the gate metal goes onto and off the mesa, there is no isolation between the edge of the channel and the gate metal. The problem exists for $In_{0.53}Ga_{0.47}As$ because it has a Schottky barrier height of 0.2 eV with the metal. As x increases, this gets smaller, about 0.1 eV for x=0.6, and 0.03 eV for x=0.7,[5] and this isolation problem becomes even more severe.

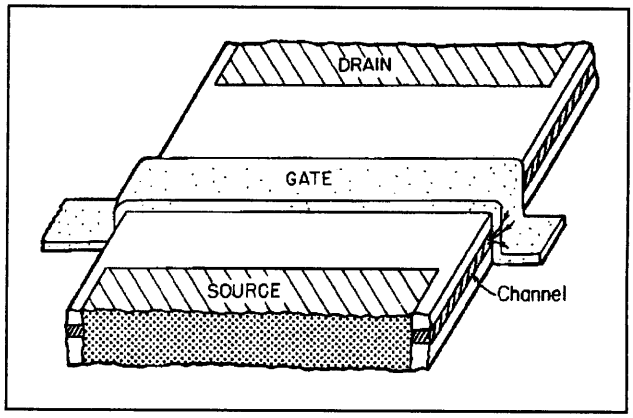

Figure 5. Perspective of the intrinsic device region.

To investigate this *edge leakage* path, we have fabricated heterojunction diodes with an inner square gate area of 10,000 μm^2. In one diode there is no gate-edge overlap, i.e., the gate is entirely on the mesa. In another diode, a 600 μm long edge overlap has been obtained by producing three cuts of the mesa structure underneath the gate. In this manner, the only difference between these diodes is the gate-edge overlap.

Figure 6 shows the forward and reverse characteristics of these two diodes. Without edge overlap, the forward current decreases with increasing x, as expected from the larger ΔE_c. With edge overlap, however, we see a marked increase in the forward current and a reversal in x dependence. This implies that edge leakage dominates the forward characteristics in the actual FETs. In the reverse characteristics of these diodes, for x=0.53, the edge overlap marginally contributes to the total reverse current. At x=0.6, the presence of three regions in the reverse characteristics becomes evident: pre-threshold, plateau, and breakdown. The edge overlap influences the reverse current in the pre-threshold region and then saturates at the threshold voltage, i.e., when the channel gets totally depleted underneath the gate. Far into the breakdown region, the reverse characteristics of both the structures with and without edge overlap at x=0.6 do not differ much either. For the x=0.7 diodes, edge leakage strongly affects the entire reverse characteristics. For this device, the edge

[5] H.H. Wieder, "Fermi Level and Surface Barrier of GaInAs Alloys," *Appl. Phys. Lett.* 38(3): 170-171 (1981).

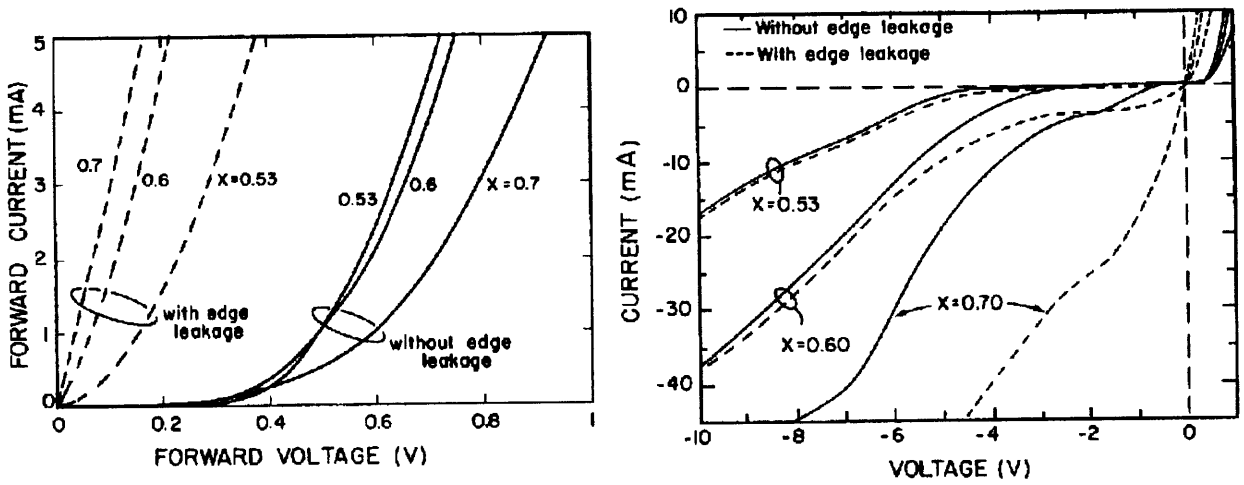

Figure 6. Forward (left) and reverse (right) diode characteristics with and without edge overlap.

leakage definitely exacerbates the loss of pinchoff. Significant gains could be made in pinchoff quality and reverse breakdown voltage by using some form of isolation that prevents edge gate-mesa overlap.

In conclusion, $In_{0.52}Al_{0.48}/n^+\text{-}In_xGa_{1-x}As$ MIDFETs have shown markedly improved peak currents and transconductances as the InAs mole fraction in the channel is increased. Devices with $L_g = 1\mu m$ and x=0.7 display an unprecedented I_D of 656 mA/mm and g_m of 296 mS/mm. As x is increased, however, there is an increase in the gate current, a dramatic decrease in the breakdown voltage, and a degradation of pinch-off. Leakage at the gate-mesa edge overlap is found to be partially responsible for these effects. To achieve the substantial gains in transport that higher InAs fractions offer, better isolation technology is required.

7.3 Orientation Dependence of Mismatched-Insulator InAlAs/n⁺-InGaAs MIDFETs

In this work,[6] a device perspective is applied to the issue of critical layer thickness and the impact of strain relaxation on electrical characteristics. The critical layer thickness of a strained semiconductor layer is ultimately determined by its application. For devices, performance is the ultimate goal. In many III-V semiconductor devices, the use of intentionally mismatched layers has the potential of significantly improving device characteristics. The appearance of misfit dislocations, however, is expected to degrade device performance, but to determine how much and in what manner, there is no substitute to studying the devices fabricated using these mismatched layers.

In an effort to increase the conduction band discontinuity in the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ system (lattice-matched to InP), we have strained the $In_xAl_{1-x}As$ layer to negative mismatch by reducing its InAs fraction. This results in many benefits to the device characteristics of $In_xAl_{1-x}As/n^+\text{-}In_{0.53}As_{0.47}As$ HFETs.[7] Here we focus on the effect of mismatch on device performance. Our main result is the finding of strong orientation

[6] S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Orientation Dependence of Mismatched $In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ HFETs," *J. Cryst. Growth,* forthcoming.

[7] J.A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+In_{0.53}Ga_{0.47}As$ MISFET with a Heavily-Doped Channel," *IEEE Electron Device Lett.* EDL-8 (11): 534-536 (1987); S.R. Bahl, W.J. Azam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+\text{-}In_{0.53}Ga_{0.47}As$ Heterostructure Field Effect Transistors," submitted to *IEEE Trans. Electron Devices.*

dependence in device characteristics beyond the Matthews-Blakeslee critical layer thickness.[8]

A cross section of the device structure is shown in figure 7. Four wafers were grown by MBE in MIT's Riber 2300 system with InAs mole fractions in the $In_xAl_{1-x}As$ gate insulator layer of 0.52 (lattice-matching), 0.48, 0.40 and 0.30. The starting material was S.I. (100) InP. The device structure consists (from bottom to top) of a 1000Å undoped $In_{0.52}Al_{0.48}As$ buffer layer, a 100Å undoped $In_{0.53}Ga_{0.47}As$ subchannel, a 100Å heavily Si doped ($N_D = 4 \times 10^{18}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ channel, a 300Å undoped $In_xAl_{1-x}As$ gate insulator layer, and an undoped 50Å $In_{0.53}Ga_{0.47}As$ cap. The four wafers were grown subsequently, and device processing was carried out simultaneously. Device processing is described by Bahl et al.[9]

HFETs were fabricated with gate-widths of 30 μm and gate lengths of 1.5 μm with current flow along the [01$\bar{1}$] (defined here as 0° with respect to the flat), [001] (45°), and [011] (90°) directions.

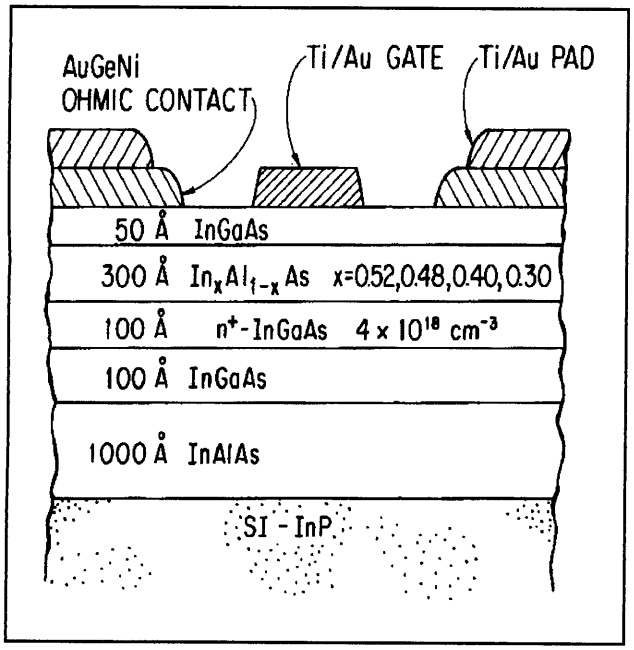

Figure 7. Schematic cross-section of the fabricated $In_xAL_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFETs.

Figure 8 shows the channel sheet resistance, R_{sh}, on each of the four wafers as a function of orientation. R_{sh} was measured using the actual MIDFETs by the all-electrical Floating Gate Transmission-Line Model (FGTLM).[10] Each point represents an average over five FGTLMs. For wafers with InAs mole fractions, x, of 0.52, 0.48, and 0.40, R_{sh} remains constant at approximately 850 Ω/□ independent of orientation. However, upon decreasing x from 0.40 to 0.30, the channel sheet resistance increases for all three orientations, showing a very pronounced orientation dependence with $R_{sh}[011] > R_{sh}[001] > R_{sh}[0\bar{1}1]$.

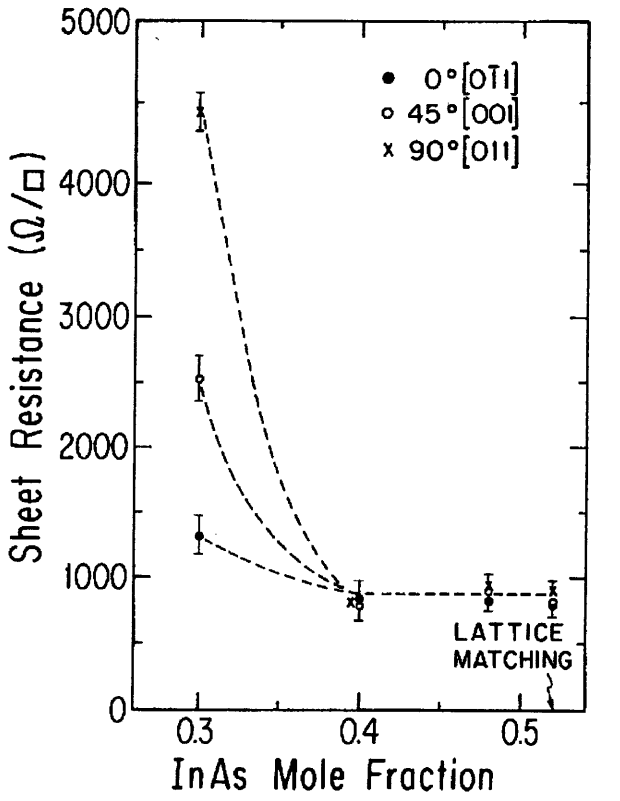

Figure 8. Channel sheet resistance versus InAs mole fraction, x, in the $In_xAl_{1-x}As$ insulator layer, for current flow along the various directions.

[8] J.W. Matthews, A.E. Blakeslee, and S. Mader, "Use of Misfit Strain to Remove Dislocations from Epitaxial Thin Films," *Thin Solid Films* 33: 253-266 (1976).

[9] S.R. Bahl, W.J. Azam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+$ - $In_{0.53}Ga_{0.47}As$ Heterostructure Field Effect Transistors," submitted to *IEEE Trans. Electron Devices*.

[10] W.J. Azzam and J.A. del Alamo, "An All-Electrical Floating-Gate Transmission Line Model Technique for Measuring Source Resistance in Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Devices* 37(9): 2105-2107 (1990).

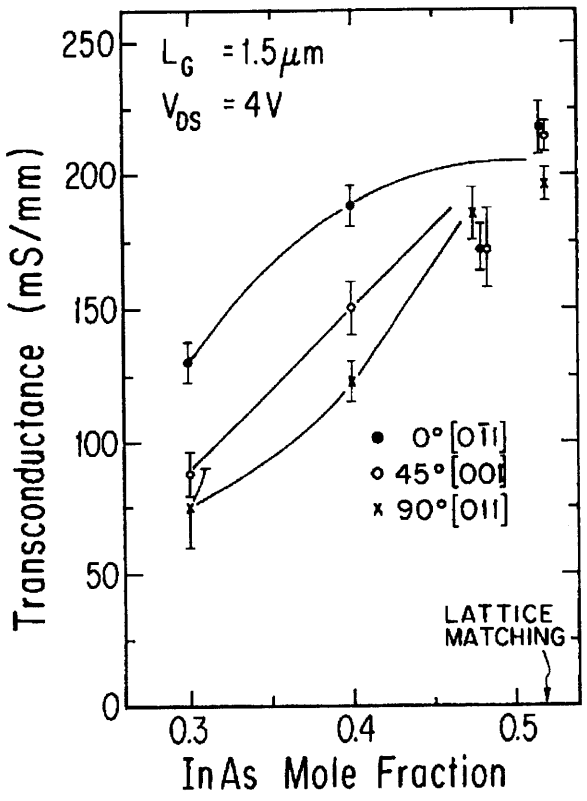

Figure 9. Peak transconductance versus x along the various directions at V_{ds}=4 V.

Figure 9 shows the average peak transconductance, g_m, over ten devices versus x for the three orientations measured at $V_{ds} = 4$ V. The x=0.52 and 0.48 devices do not show any orientation dependence (the x=0.40 devices have a high source resistance and are anomalously low in g_m). A pronounced orientation dependence is seen for devices with both x=0.40 and 0.30, with the 0° device being the best and the 90° device the most degraded. An additional significant result is that g_m (0°, x=0.40) is 189 mS/mm, which is very close to the average $g_m = 209$ mS/mm of the x=0.52 sample.

The x=0.40 and 0.30 devices were grown with thicknesses greater than the Matthews-Blakeslee critical layer limit.[11] This suggests that, in these devices, misfit dislocations may be responsible for the decrease in g_m and the appearance of orientation dependence. Since the presence of misfit dislocations has been correlated to the appearance of a cross-hatched surface,[12] we have taken dark field microscope images of the surface of the four wafers (figure 10). Figures 10(a) and 10(b) are the surfaces of the x=0.52 and x=0.48 wafers respectively. There are no ridges or cross-hatches on the surface. Figures 10(c) and 10(d) are the surfaces of the x=0.40 and x=0.30 wafers respectively. We see the appearance of a unidirectional array of surface ridges, faint and short, in figure 10(c), and brighter and longer in figure 10(d), running along the [0$\bar{1}$1] direction. This is the direction of current flow in the better (0°) devices. We could not distinguish any ridges along the [011] direction, neither in the Nomarski, nor in the dark-field mode of the microscope. The ridges could not be imaged at higher magnification, so a density count was impossible. Brighter and longer streaks would result from greater surface relief, indicating a higher dislocation density, with a greater bunch of dislocations associated with each surface streak.[13] The unidirectional hatch observed is consistent with that reported[14] for thin strained samples.

In III-V semiconductors, orthogonal 60° dislocations in the zinc-blende lattice occur on different sublattices and show an asymmetry relative to each other.[13] The so-called α dislocations have an extra half plane ending on a row of group-III atoms, and the β dislocations have an extra half plane ending on a row of group-V atoms.[15] For strained (100) InGaAs/GaAs, it has been shown

[11] J.W. Matthews, A.E. Blakeslee, and S. Mader, "Use of Misfit Strain to Remove Dislocations from Epitaxial Thin Films," *Thin Solid Films* 33: 253-266 (1976).

[12] K.H. Chang, R. Gibala, D.J. Srolovitz, P.K. Bhattacharya, and J.F. Mansfield, "Crosshatched Surface Morphology in Strained III-V Semiconductor Films," *J. Appl. Phys.* 67(9): 4093-4098 (1990).

[13] M.S. Abrahams, J. Blanc, and C.J. Buiocchi, "Like-Sign Asymmetric Dislocations in Zinc-Blende Structure," *Appl. Phys. Lett.* 21(5): 185-186 (1972).

[14] K.L. Kavanagh, M.A. Capano, L.W. Hobbs, J.C. Barbour, P.M.J. Maree, W. Schaff, J.W. Mayer, D. Pettit, J.M. Woodall, J.A. Stroscio, and R.M. Feenstra, "Asymmetries in Dislocation Densities, Surface Morphology and Strain of GaInAs/GaAs Single Heterolayers," *J. Appl. Phys.* 64 (10): 4843-4852 (1988).

[15] A.L. Esquivel, S. Sen, and W.N. Lin, "Cathodoluminescence and Electrical Anisotropy from α and β Dislocations in Plastically Deformed Gallium Arsenide," *J. Appl. Phys.* 47(6): 2588-2603 (1976).

that the first dislocations to form are 60° α dislocations along the [011] direction.[16] For our samples, in contrast, the dislocations run unidirectionally along the [0$\bar{1}$1] direction, perpendicular to the preferred dislocation direction we have seen reported in the literature. However,

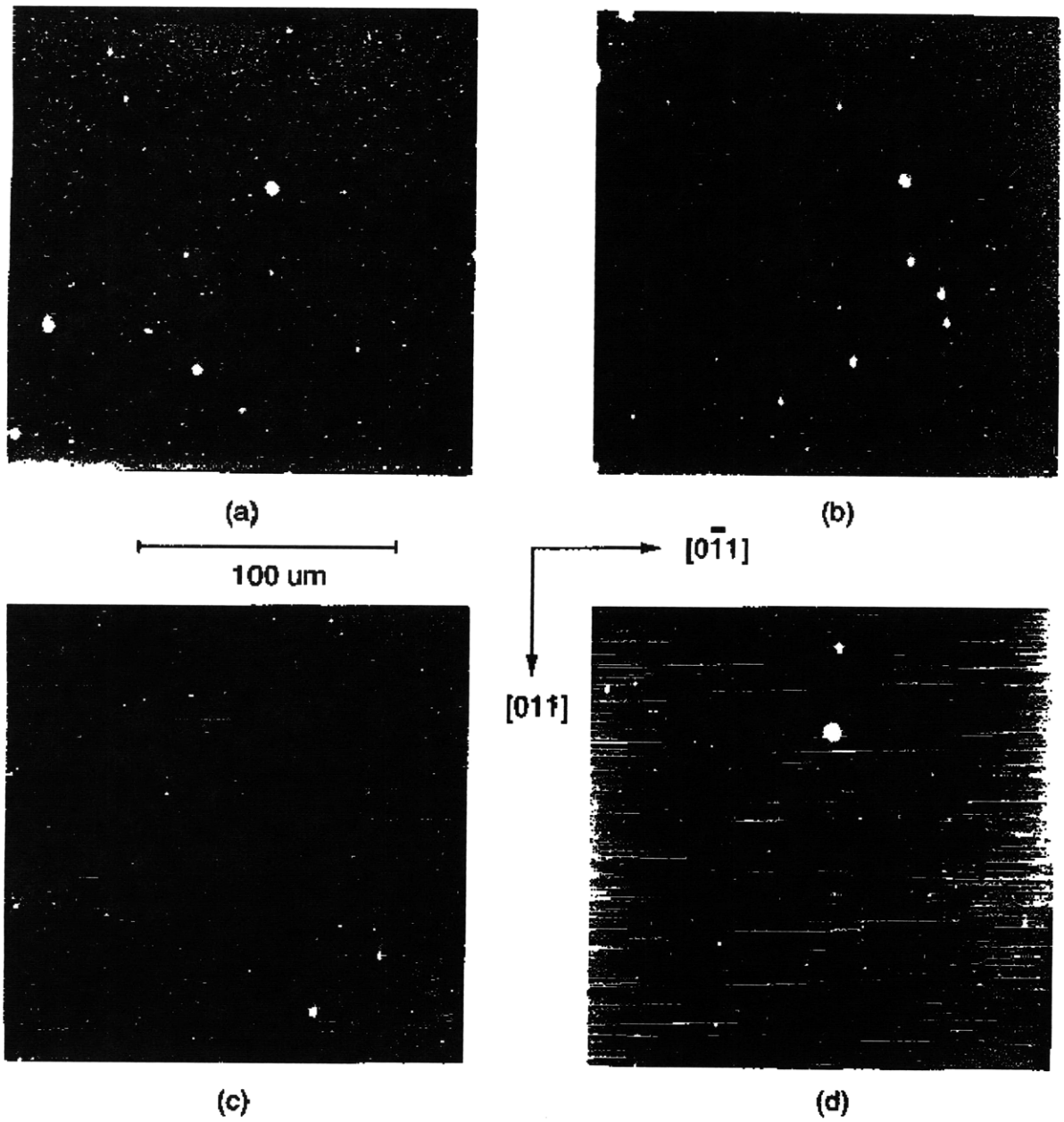

Figure 10. Dark-field optical microscope photographs of the surface of the MIDFET layer structure for (a) x=0.52, (b) x=0.48, (c) x=0.40, and (d) x=0.30.

[16] K.L. Kavanagh, M.A. Capano, L.W. Hobbs, J.C. Barbour, P.M.J. Maree, W. Schaff, J.W. Mayer, D. Pettit, J. M. Woodall, J.A. Stroscio, and R.M. Feenstra, "Asymmetries in Dislocation Densities, Surface Morphology and Strain of GaInAs/GaAs Single Heterolayers," *J. Appl. Phys.* 64(10): 4843-4852 (1988); E.A. Fitzgerald, G.P. Watson, R.E. Proano, D.G Ast, P.D. Kirchner, G.D. Pettit, and J.M. Woodall, "Nucleation Mechanisms and the Elimination

these reports[16] have been done for epilayers under compression, i.e., the relaxed lattice constant for the epilayer is larger than that of the substrate. It has also been suggested that the 60° α and β dislocations should interchange directions when the epilayer is grown in tension,[17] which is consistent with our results, assuming that the α dislocations still nucleate preferentially. We believe we are the first to report observations of this behavior.

Our 0° devices, which have current flowing along the dislocations, are better than our 90° devices, which have current flowing perpendicular to them. The 45° devices fall in between. Our results are in agreement with the findings of Esquivel et al.[15] who show a decrease in mobility for current flow perpendicular to the α dislocations.

Woodall et al.[18] have proposed that misfit dislocations pin the Fermi-level, depleting a cylindrical region around them. Figure 11 shows a schematical cross-section of the dislocation depletion regions in a semiconductor slab with misfit dislocations running along the [0$\bar{1}$1] direction. Based on this figure, we can hypothesize an explanation for our observations. For our 0° devices, current flows along the dislocation direction [0$\bar{1}$1], while for our 90° device, current flow along [011] is normal to it. If the dislocation density is low, as in the x=0.40 sample, a dislocation would be associated with a small depletion region in the channel. If this depletion depth is smaller than the equilibrium depletion associated with Fermi-level pinning at the wafer surface or underneath the gate, then R_{sh} should not be affected by the presence of the dislocations. However, the pinning at the dislocation would prevent the gate voltage from modulating the portion of the channel underneath it. This should result in the more severe degradation of g_m for current flow perpendicular to the dislocations, because of their constricting effect, than for flow parallel to them. For a higher misfit (such as in the x=0.30 sample), the surface relief becomes more pronounced, indicating a greater bunching of the dislocations,[19] and producing depletion regions that exceed the depth of the one associated with the wafer surface. This should result in an asymmetry in both R_{sh} and g_m.

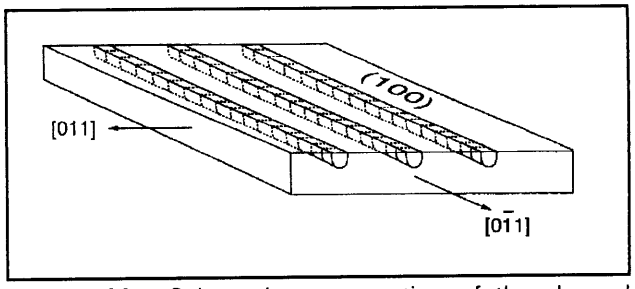

Figure 11. Schematic cross-section of the channel region of the MIDFET under tension, showing the effect of the depletion regions of misfit dislocations on current flowing parallel and perpendicular to them.

$In_{0.40}Al_{0.60}As/n^+$-$In_{0.53}Ga_{0.47}As$ devices with $L_g = 1.5\ \mu m$ and current flow along the [0$\bar{1}$1] direction show excellent characteristics in spite of the presence of misfit dislocations: a reverse breakdown voltage of 23 V, a maximum drain current of 308 mA/mm, a peak transconductance of 189 mS/mm and reduced real-space transfer of hot electrons from the channel to the gate.[20] Our result shows that although dislocations degrade device performance, excellent devices may be obtained by orienting the current parallel to them, if they are sufficiently sparse.

In conclusion, we have studied the electrical properties of strained-insulator $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ HFETs with the insulator composition below and above the Matthews-Blakeslee criteria for dislocation formation. For devices with the $In_xAl_{1-x}As$ layer above its critical thickness, we see a unidirectional array of surface ridges and measure a strong orientation dependence of peak transconductance. By aligning the current in the direction of the ridges, the impact of dislocations is greatly minimized, resulting in excellent devices, if their density is not too high.

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of Misfit Dislocations at Mismatched Interfaces by Reduction in Growth Area," *J. Appl. Phys.* 65(6): 2220-2237 (1989).

17 W.J. Bartels and W. Nijman, "Asymmetry of Misfit Dislocations in Heteroepitaxial Layers of (001) GaAs Substrates," *J. Cryst. Growth* 37: 204-214 (1977).

18 J.M. Woodall, G.D. Pettit, T.N. Jackson, and C. Lanza, "Fermi-Level Pinning by Misfit Dislocations at GaAs Interfaces," *Phys. Rev. Lett.* 51(19): 1783-1786 (1983).

19 M.S. Abrahams, J. Blanc, and C.J. Buiocchi, "Like-Sign Asymmetric Dislocations in Zinc-Blende Structure," *Appl. Phys. Lett.* 21(5): 185-186 (1972).

20 S.R. Bahl, W.J. Azam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+$ - $In_{0.53}Ga_{0.47}As$ Heterostructure Field Effect Transistors," submitted to *IEEE Trans. Electron Devices*.

7.4 Publications and Conference Papers

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Bahl, S.R., W.J. Azzam, and J.A. del Alamo. "Orientation Dependence of Mismatched $In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ HFETs." Paper presented at Sixth International Conference on Molecular Beam Epitaxy, San Diego, California, August 27-31, 1990. *J. Cryst. Growth*. Forthcoming.

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Professor Henry I. Smith (left) observing an x-ray lithography experiment being carried out by graduate students Anthony Yen and William Chu.