# **Chapter 8. Novel Superconducting Tunneling Structures**

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## **8.1 Project Description**

#### **Sponsor**

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In this program, we seek to examine the behavior of electronically-gated resonant tunneling structures with superconducting source and drain electrodes. Specifically, we will examine whether superconducting Cooper pairs can participate in<br>the resonant-tunneling channel. These threethe resonant-tunneling channel. terminal hybrid superconducting/semiconducting structures represent the first attempt at Josephson coupling via resonant tunneling. A significant potential technological consequence of this approach is that quantum confinement levels, not the semiconducting gap, set the characteristic energy scale for modulating the Josephson current. In addition, such structures may provide important insight into the behavior of "conventional" (i.e., single electron) resonant tunneling structures, as the Josephson channel is inherently coherent.

In previously fabricated electronically-gated hybrid superconducting/semiconducting devices, the energy scale in the semiconducting region was set **by** the semiconducting gap energy  $(E_{semi} \approx 0.1$ -1eV), while the energy scale for the Josephson coupling (and hence the output voltage) was set **by** the superconducting gap energy  $(\Delta \approx 10^{-3} \text{ eV})$ . It is important to recognize that it is this energy mismatch which fundamentally leads to less than unity gain in such devices. As a result, the output voltage  $\Delta$  is insufficient to drive the gate of another device downstream  $(V_{gate} \approx E_{semi}/e)$ . On the contrary, the characteristic energy scale for a quantum confined structure is instead set by the device size, and is therefore tunable. For device dimensions on the scale of 10-100 nm, now experimentally accessible via advanced lithographic patterning techniques, these energies can thus more easily approach that of the superconducting gap energy.

The novel geometry of our hybrid resonant tunneling device is shown schematically in figure 1. The semiconducting quantum well is made of single crystal silicon, the tunnel barriers are ultrathin thermally-grown layers of  $SiO<sub>2</sub>$ , and the superconducting electrodes are vacuum-deposited niobium (Tc(Nb)=9 K).

The Si quantum well is a high-aspect ratio structure and is etched into the surface of a singlecrystal Si wafer using a highly anisotropic wet etch. A top view of this kind of wall is displayed in figure 2. Please note that this is a novel geometry, because the semiconducting well is oriented vertically and not horizontally. The fact that it is patterned via wet etching from single crystal silicon leads to almost no reduction in the electron mobility as compared to the starting bulk material. The patterning of this walled structure was produced via x-ray lithography. In order to fabricate such a structure, the mask must be aligned to crystalline axes of the silicon wafer with high precision. The anisotropic etch (in a potassium hydroxide solution) produces essentially atomically smooth surfaces, leading to parallel faces on either side of the quantum well. This is an essential ingredient for a resonant tunneling device, because

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**Figure 1.** Schematic of device structure (not to scale) displaying Nb superconducting electrodes, SiO<sub>2</sub> tunneling barriers, and Si wafer and quantum well. Note quantum well is vertical and composed entirely of single-crystal Si. The gate (not shown) is offset laterally and is attached to the Si surface layer.

there are close analogies between it and an optical Fabry-Perot interferometer.

The ultrathin oxide tunneling barriers are grown thermally at 800°C in a dilute (0.8%) oxygen atmosphere. Using this technique, we can produce oxide thicknesses down to **15A,** and **C-V** analysis show them to be of very high quality. For our device to date, we have used **15-20A** oxide layers.

The **Nb** superconducting counterelectrodes are deposited in high vacuum via electron-beam deposition and are subsequently laterally patterned into cross-strips via standard lithographic processing techniques. The crucial and most difficult step is to remove the **Nb** over the top of the quantum well, in order to avoid superconducting shorts across the device. We have found that planarization is both convenient and appropriate for this task, and we reactively etch the top strip of **Nb** using chlorine gas (which stops at the ultrathin  $SiO<sub>2</sub>$  tunnel barrier).



Figure 2. Scanning electron microscope picture of the top of such a wall, showing the extremely smooth and straight faces produced **by** the anisotropic etching.

We have just completed the fabrication trials. We have tested every key step of device fabrication and have put all the steps together to fabricate several test devices on very lightly doped Si wafers. The devices made had quantum well thicknesses ranging down to **750A,** with Si wall heights on the order of **5000A.** These test devices have successfully verified all aspects of the device fabrication, but unfortunately were too lightly doped for resonant tunneling conduction. Thus, the next step will be to fabricate these devices onto wafers with doped high-mobility epitaxiallygrown Si layers. In collaboration with Dr. Bernard **S.** Meyerson at the IBM Thomas **J.** Watson Research Center, we are presently preparing to fabricate these devices using Si wafers on which high-mobility delta-doped epitaxial Si layers have been grown.