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N-Face GaN/AlGaN HEMTs Fabricated Through Layer Transfer Technology

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Abstract—We present a new method to fabricate N-face GaN/ AlGaN high electron mobility transistors (HEMTs). These devices are extremely promising for ultrahigh frequency applications where low contact resistances and excellent carrier confinement are needed. In this letter, the N-face of a Ga-face AlGaN/GaN epilayer grown on Si(111) is exposed by removing the Si substrate. To provide mechanical support, prior to the substrate removal, the Ga-face of the wafer is bonded to a Si(100) carrier wafer. The resultant N-face GaN/AlGaN heterostructures exhibited record transport properties ($\mu_e = 1670 \text{ cm}^2/\text{V} \cdot \text{s}$, $n_s = 1.6 \times 10^{13}/\text{cm}^2$, and $R_{\text{sh}} = 240 \ \Omega/\text{sq}$). These excellent transport properties rendered N-face HEMTs with 30% higher maximum drain current than Ga-face HEMTs and good RF characteristics ($f_T = 10.7 \text{ GHz} \cdot \mu\text{m}$ and $f_{\max} = 21.5 \text{ GHz} \cdot \mu\text{m}$), comparable to state-of-the-art Ga-face devices.

Index Terms—GaN, high electron mobility transistor (HEMT), hydrogen silsesquioxane (HSQ) adhesive bonding, layer transfer, N-face GaN, silicon substrate.

I. Introduction

NITRIDE-BASED transistors are revolutionizing power electronics and high-frequency amplifiers due to the combination of high current densities (2.9 A/mm) [1], large breakdown voltages (>200 V), and high-frequency performance ($f_T/f_{\max} = 153/198$ GHz) [2], [3]. Although most of the reported GaN devices have been fabricated on nitride structures grown along the c-direction (i.e., Ga-face), N-face GaN/AlGaN transistors, with their reversed polarization, have a tremendous potential to improve device performance [4], [5]. For example, a typical N-face GaN/AlGaN high electron mobility transistor (HEMT) structure has the AlGaN barrier underneath the GaN channel, opposite to what is common in Ga-face devices. This structure provides a natural back-barrier to the channel electrons when the transistor is biased near pinch-off, improving carrier confinement particularly in deep submicrometer devices. In addition, ohmic contact resistances can be reduced in N-face HEMTs, where the ohmic metals are deposited on the GaN layer instead of on the AlGaN. The narrower

bandgap of GaN minimizes the potential barriers to the electron flow in N-face HEMTs. Recently, Nidhi *et al.* have demonstrated ohmic contacts of $0.1 \ \Omega \cdot \text{mm}$ for N-face AlGaN/GaN HEMT structures, which is better than Ga-face ohmic contacts (0.3–$0.5 \ \Omega \cdot \text{mm}$) [6]. Finally, the AlGaN-free surface of N-face structures maximizes the activation yield in Si-implanted GaN. In Ga-face AlGaN/GaN structures, the activation yield of Si-implanted dopants in the top AlGaN barrier is extremely low, which increases the difficulty of fabricating ultralow contact resistances [7]. On N-face samples, on the other hand, the top layer is the GaN channel, where the activation yield is very high [8].

In spite of their very high potential, the performance of N-face devices is still lower than in Ga-face devices due to their inferior material quality and technology. Although N-face devices have been successfully grown by molecular beam epitaxy [4] and, recently, by metal–organic chemical vapor deposition (MOCVD) [9], the growth of N-face nitrides is much more challenging than the growth of the more stable Ga-face structure. For example, the growth of N-face GaN films is more sensitive to process conditions and often exhibits pyramidal hexagonal facets leading to rough surfaces [10], [11].

In this letter, we present a new method to fabricate N-face GaN/AlGaN HEMTs based on the substrate removal of a Ga-face AlGaN/GaN layer grown on a Si(111) substrate to expose the N-face surface. To provide mechanical support to the GaN epilayer after the substrate removal, the wafer is bonded through the Ga-face of the nitride epilayer to a Si(100) carrier wafer. After the wafer bonding process, the original Si(111) substrate is etched through a dry etching technique. This new technology exposes the N-face of the GaN wafer without degrading its original superior quality. By using this layer transfer technology, N-face GaN epilayers with record transport properties as well as HEMTs with good dc and RF performances are demonstrated.

II. Device Fabrication

The fabrication process of N-face GaN structures starts with the growth of state-of-the-art Ga-face AlGaN/GaN HEMT structures on Si(111) substrates by MOCVD at Nitronex Corporation [12]. In these samples, the AlGaN barrier had a total thickness of 175 Å and an Al composition of 26%, as determined by Hg-probe CV and photoluminescence, respectively. The structure is finished with a 20-Å-thin unintentionally doped GaN cap layer. A 2DEG carrier density (n_s) and electron mobility (μ_e) of $1 \times 10^{13}/\text{cm}^2$ and $1600 \text{ cm}^2/\text{V} \cdot \text{s}$, respectively, were measured at room temperature.
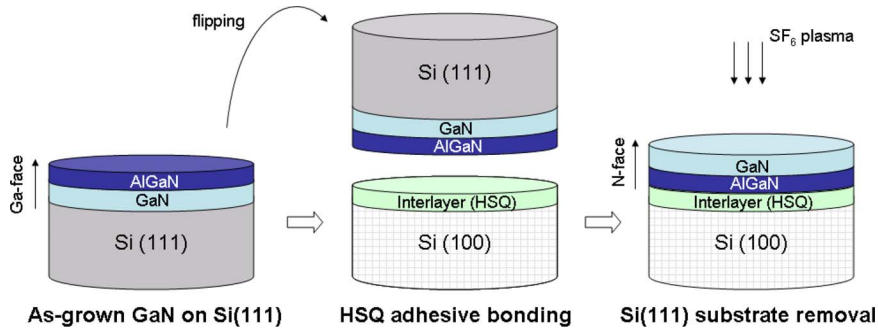
Fig. 1. Main processing steps of the layer transfer technology described in this letter. A thin GaN epitaxial layer (~ 2 μm) is transferred from the Si(111) to Si(100) substrate reversing its face from Ga- to N-face. Spin-coated HSQ is utilized for the adhesive bonding, and SF$_6$-based plasma is used to selectively etch the Si(111) substrate. It should be noted that other substrates, such as SiC and sapphire, can be used as carrier wafers.
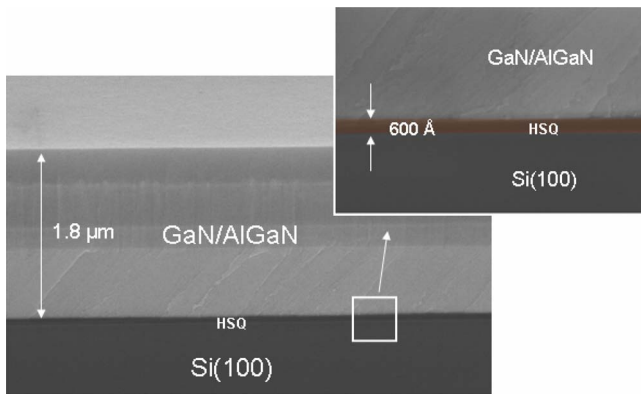

Fig. 2. Scanning electron micrograph of the cross section of an AlGaN/GaN layer transferred to a Si(100) carrier wafer. False color has been added in the inset to highlight the HSQ interlayer in the structure. Although the thickness of the HSQ layer after spin coating is 1000 Å, the thickness decreases to 600 Å by the end of the bonding process.

To have access to the N-face of these samples, we have developed the layer transfer technology shown in Fig. 1. First, the Ga-face surface is bonded to a Si(100) carrier wafer by using a hydrogen silsesquioxane (HSQ) (XR-1541, Dow Corning Corporation) interlayer. HSQ is a flowable oxide with excellent thermal stability, which stands the high thermal budget (~ 900 °C) required during the processing of GaN transistors. The HSQ film is spin coated on the Si(100) carrier wafer to a thickness of about 1000 Å and baked sequentially on hot plates at 150 °C and 200 °C for 1 min each. Then, the HSQ-coated Si(100) substrate is attached to the Ga-face of the as-grown AlGaN/GaN layer and thermally compressed at 400 °C for an hour. The elevated temperature hardens the HSQ layer and forms an extremely stable bond between the GaN wafer and the Si carrier wafer. After the wafer bonding, the original Si(111) substrate is completely removed by dry etching in a deep reactive ion etch system (Surface Technology Systems Multiplex Inductively Coupled Plasma system) using an SF$_6$-based plasma. The GaN buffer is an effective etch-stop layer for the SF$_6$ plasma etch, and a smooth N-face GaN surface ($R_{\mathrm{rms}} = 2 \sim 3$ nm) is obtained at the end of the etch. Fig. 2 shows a scanning electron micrograph of the AlGaN/GaN layer transferred to the Si(100) substrate. The N-face GaN epilayer is then etched to the desired thickness by using an electron cyclotron resonance reactive ion etching (ECR-RIE) with a Cl$_2$/BCl$_3$ gas mixture. At least 1 μm etch is desirable to completely remove the nucleation layer and reach the high-quality GaN buffer layer. Very low etch rates (~ 1 Å/s) are required to assure a smooth surface. The total remaining thickness in the GaN epilayer was measured with an optical interferometer (NanoSpec).

N-face GaN/AlGaN structures fabricated through the layer transfer technology described previously have been used in the fabrication of N-face HEMTs. In these samples, the distance between the N-face surface and the 2DEG was reduced to 1000 Å by ECR-RIE. A Ti/Al/Ni/Au multilayer (20/100/25/50 nm) was deposited for the ohmic contacts and annealed at 870 °C for 30 s in a N$_2$ atmosphere. Then, Cl$_2$/BCl$_3$ plasma was used for the mesa isolation. Finally, a 2.2-μm-length gate is defined by photolithography, and a Ni/Au/Ni metallization was deposited for the Schottky gate contact. As a reference, standard Ga-face HEMTs were fabricated on the same material prior to the substrate transfer.

III. RESULTS AND DISCUSSION

The effect of the GaN buffer thickness on the electron transport of N-face material was evaluated by four-point van der Pauw Hall measurements. Fig. 3 shows the measured values of electron mobility (μ_e), electron density (n_s), and sheet resistance (R_{sh}) at room temperature as a function of the remaining GaN buffer thickness. As shown in Fig. 3, no significant variation was observed in any of these electrical properties with the buffer thickness. However, while the electron mobility in the N-face material was almost the same than in the Ga-face reference ($\mu_e = 1670$ cm^2/V · s in N-face versus $\mu_e = 1600$ cm^2/V · s in Ga-face), the sheet electron density increased by 60% in the N-face material with respect to Ga-face material ($n_s = 1.6 \times 10^3$ cm^{-2} in N-face versus $n_s = 1.0 \times 10^3$ cm^{-2} in Ga-face). The change in the surface Fermi level pinning when the N-face surface is exposed, and possible piezoelectric charges induced by relaxing strain after the Si(111) removal are believed to be partly responsible for this improvement although additional experiments are needed to fully confirm their effect. The increased n_s in the N-face material is responsible for a 50% decrease in the sheet resistance, down to $R_{\mathrm{sh}} = 240$ Ω/sq. To the best of our knowledge, this sheet resistance is the lowest sheet resistance reported in AlGaN/GaN material systems.

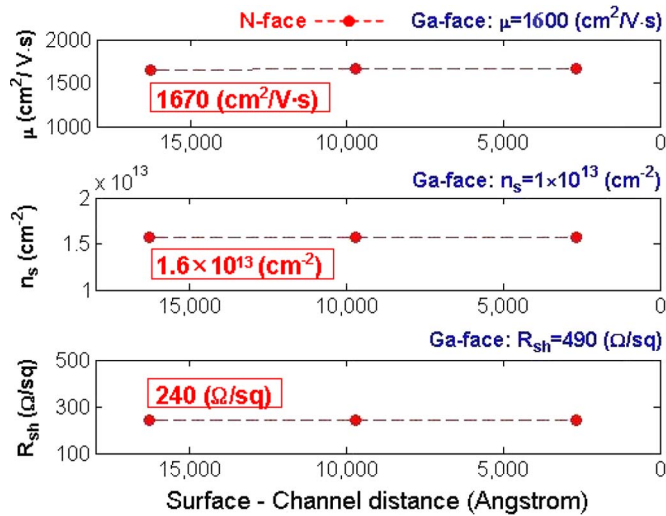Fig. 3. Electron mobility (μ_e), 2DEG density (n_s), and sheet resistance ($R_{\rm sh}$) of N-face GaN as a function of the distance between N-face surface and 2DEG channel. All these parameters where estimated by room-temperature Hall measurement. A record $R_{\rm sh}$ of 240 Ω/sq was also confirmed by transfer length method.
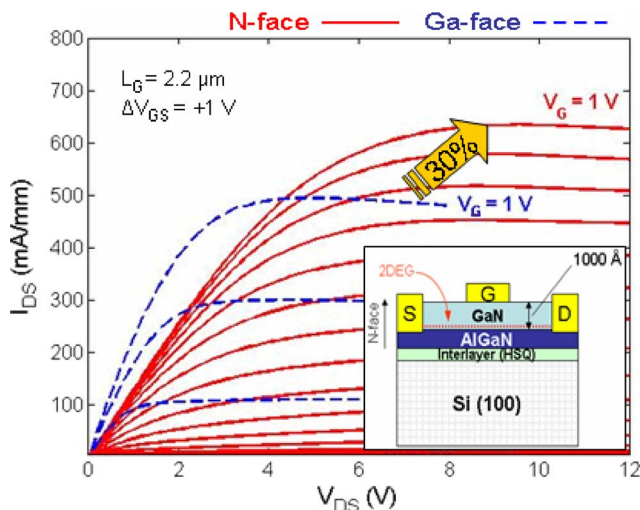

Fig. 4. DC current–voltage characteristics of (red solid line) N-face and (blue dashed line) Ga-face HEMTs with a gate length (L_G) of 2.2 μm. The schematic of the final N-face device structure is shown in the inset. Almost 30% higher maximum current at $V_G = 1$ V is achieved in N-face HEMTs due to the higher carrier density. The high on-resistance ($R_{\rm on}$) and lower transconductance (g_m) in N-face HEMTs are due to unoptimized ohmic contacts and large surface-to-channel distance, respectively.

Fig. 4 shows a comparison of the drain current versus drain voltage characteristics of a HEMT fabricated on the N-face GaN/AlGaN structure described previously and a standard HEMT fabricated on the Ga-face of the same material. The maximum current in the N-face device is almost 30% higher than in the Ga-face device. This improvement is mainly due to the higher charge density in the N-face device as previously described. The fabricated N-face HEMTs showed a high contact resistance ($R_c = 1.5$ Ω · mm) due to the use of an unoptimized metal stack and annealing temperature, as well as due to the larger surface-to-channel distance (1000 Å) when compared to the Ga-face transistor (195 Å) which also reduces the transconductance ($g_m = 50$ mS/mm). In addition, we also

found a softer pinch-off in the N-face device due to the higher gate leakage current. Other groups have also reported a higher gate leakage in N-face transistors due to the low barrier height of Schottky contacts on GaN [4]. We are currently developing a gate dielectric technology to reduce this gate leakage. The source access resistance (R_s) was estimated to be ∼1.8 Ω · mm in a device with a source-gate distance of 1.6 μm.

The small-signal high-frequency characteristics of the N-face HEMT were also characterized. A normalized unity current gain cutoff frequency (f_T) of 10.7 GHz · μm and power gain cutoff frequency ($f_{\rm max}$) of 21.5 GHz · μm were measured in long-gate-length devices (2.2×150 μm^2). These values are comparable to the RF performance of state-of-the-art Ga-face GaN HEMTs ($f_T = 12.4$ GHz · μm and $f_{\rm max} = 23$ GHz · μm) [3]. It should be highlighted, however, that there is still room for improvement in these new N-face devices since these initial results are based on unoptimized device geometry (i.e., a large surface-to-channel distance and source-to-drain spacing, a long gate length, unoptimized ohmic contacts, etc).

IV. CONCLUSION

We have successfully fabricated N-face GaN from state-of-the-art Ga-face material by using a new substrate removal and layer transfer technology. This technology has allowed us to have N-face nitride materials grown along Ga-face. Record transport properties have been achieved in N-face AlGaN/GaN structures. Also, the resultant HEMTs have demonstrated good dc and RF performance, showing its huge potential for future high-speed applications.

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