Prof. H. J. Zimmermann
Prof. R. B. Adler
Prof. S. J. Mason
M. F. Friedman
J. Gross
C. R. Hurtig

A. VOLTAGE-REGULATED SUPPLY

A voltage-regulated power supply employing transistors and diodes has been designed and tested. The circuit diagram of the complete supply is shown in Fig. XII-1. The regulator employs a transistor in series with the load and the rectifier. A shunt regulator was also considered; however, the efficiency of the shunt regulator proved to be very low when the variations of load current and input voltage were large.

The half-wave rectifier employs a General Electric type 1N91 diffused germanium diode. This diode is capable of delivering 200 ma at 30 volts at 65°C. In this circuit the maximum current is less than 100 ma. The effective resistance of the rectifier and filter is 68 ohms. The ripple at the input to the regulator is approximately 0.1 volt peak-to-peak at no load, and 3.9 volts at full load of 80 ma.

The regulator consists of a series transistor, a diode bridge used as a voltage reference, and a two-stage direct-coupled amplifier. The bridge circuit employs the breakdown voltage of silicon alloy junction diodes as a voltage reference. Since the input impedance of transistors is low, it is necessary to convert the error in the output voltage to a current with as large transconductance as possible. The silicon diodes satisfy this requirement, since the resistance of the diodes in the breakdown region is very low. The particular diodes used have breakdown voltages of 10 volts. When the output voltage exceeds the sum of the breakdown voltages of diodes D_1 and D_2, the emitter of the first stage of the transistor amplifier becomes forward-biased. The current flow through the first transistor is determined by the error voltage divided by the sum of the input resistance of the first stage and the sum of the diode resistances in the breakdown region.

Since the silicon diodes have a tendency to be excessively noisy at low currents in

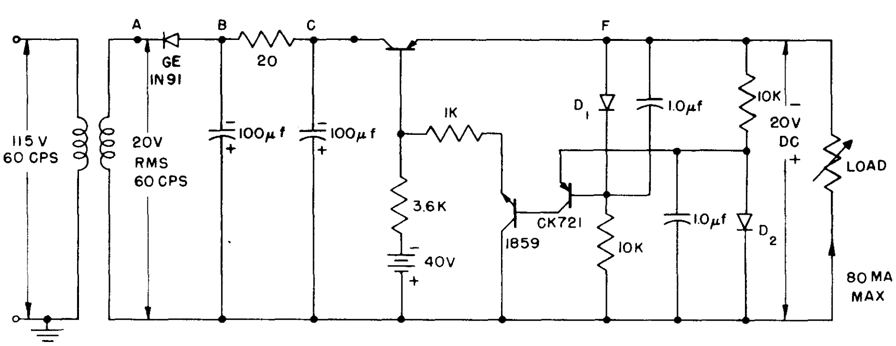

Fig. XII-1
Voltage-regulated power supply.

the breakdown region, the bridge is arranged to have approximately 1 ma flowing through each diode. The silicon diodes are by-passed with 1.0-μf capacitors. These capacitors act as filters to remove high-frequency noise. With the capacitors the noise at the output of the regulator is less than 1 mv rms. Without the capacitors the noise is greater than 10 mv rms.

The input stage of the amplifier employs a PNP transistor in a grounded-emitter connection. The current gain of the stage is a function of the output voltage, since the emitter resistance varies radically with the emitter current. The second stage employs an NPN transistor in a grounded-collector connection. The grounded collector is used to obtain the proper phase relation for negative feedback. The emitter of the NPN transistor and the base of the series transistor are connected through a high (3.6 K) resistance to an external supply. Although this arrangement requires an additional supply, the efficiency and range of regulation are greater than those obtained by using the output of the rectifier itself.

The regulator shown in Fig. XII-1 is stable. It is conceivable that the frequency responses of the three transistors could be nearly equal and thereby cause high-frequency oscillations. If this were the case, a corrective network in the form of a low-pass filter would be required. In its present form, the regulator has a flat-frequency response from dc to 5000 cps. Tables I and II list the regulation characteristics of the voltage supply.

The power dissipation across the series transistor is a function of the load current, the input voltage, and the generator resistance. A study of this problem has been made, but it is sufficient to give only a few of the results. The minimum rectified voltage for an 80-ma load is 27.5 volts. The transistor dissipation as a function of rectified voltage is shown in Fig. XII-2. Above 30.9 volts the curve is linear.

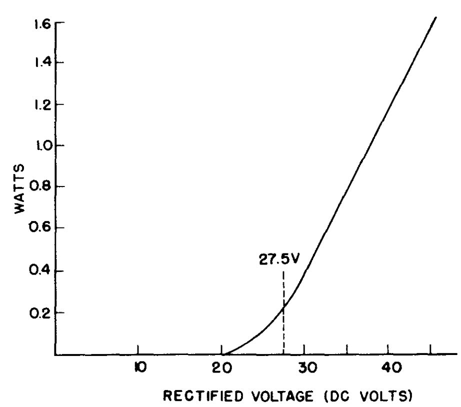

Fig. XII-2

Dissipation across series transistor as a function of input voltage.

Table I

Regulation Characteristics of the Transistor Supply with Load Variations

Load Current (ma)	dc Voltage (volts) B	C	F	Ripple (peak-to-peak volts) C	F
0	27.5	27.5	19.60	0.11	---
40	25.3	24.5	19.58	2.5	0.005
80	23.5	22.3	19.55	3.9	0.014

Table II

Regulation Characteristics of the Transistor Supply
with Input Voltage Variations

Input C (volts dc)	No Load F (volts dc)	Full Load F (volts dc)
22	19.60	19.55
30	19.60	19.58
40	19.62	19.60
50	---	19.62

The performance of the voltage supply has not been determined as a function of temperature. The expected variation of the output voltage is 0.08 percent/°C, caused principally by the temperature dependence of the breakdown voltage of the silicon diodes.

C. R. Hurtig

B. TRANSISTOR TIME MODULATOR

A transistor time modulator has been designed which uses the linear sawtooth sweep circuit described in the Quarterly Progress Report of April 15, 1954. The output pulses from the modulator are delayed with respect to the input pulses as a linear function of a dc voltage introduced externally.

The modulator consists of two basic components: a triggered sawtooth generator and a negative-resistance monostable multivibrator. The circuit diagram is shown in Fig. XII-3. The sawtooth generator employs a 1768 point-contact transistor and a PNP junction transistor. The sawtooth generator is biased in a monostable state and is

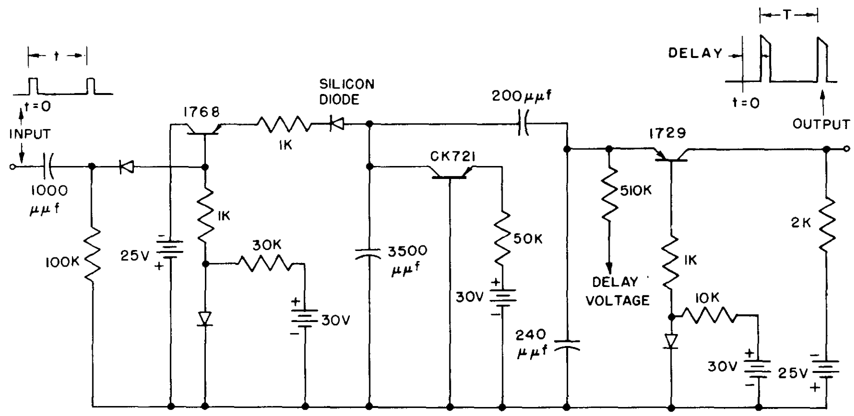

Fig. XII-3
Transistor time modulator.

triggered by applying pulses to the base of the point-contact transistor. The amplitude of the minimum trigger pulse is 3.0 volts. It has a 0.5-μsec duration. The sawtooth amplitude is 20 volts; the duration, 50 μsec.

The emitter of the monostable multivibrator, which employs a 1729 point-contact transistor, is returned to a negative variable dc voltage. When the sawtooth waveform exceeds the negative voltage at the emitter of the multivibrator, the circuit is triggered and an output pulse with a rise time of 0.08 μsec, an amplitude of 15 volts, and a width of 2.0 μsec is produced. The width of the pulse depends upon the emitter-to-ground capacitance.

The "nonlinearity" is defined as the percentage by which the minimum slope of the curve of pulse delay vs delay voltage falls below its maximum slope. For the present circuit this figure is less than 2 percent. The circuit sensitivity is 4.66 μsec/volt. The minimum delay of the circuit, limited by a tendency of the multivibrator to free-run, is 0.5 μsec. The time jitter of the output pulse is approximately 0.1 μsec for pulse delays from 1.0 μsec to 50 μsec, and approximately 0.2 μsec to 0.3 μsec for pulse delays less than 1.0 μsec.

M. F. Friedman