Lecture 39 - Bipolar Junction Transistor
(cont.)

December 6, 2002

Contents:

1. Non-ideal effects in BJT operation (*cont.*)
2. Evolution of BJT design
3. Bipolar issues in CMOS

Announcement:

Final Exam: Friday, Dec. 20, 1:30-4:30 PM at Walker. Covers entire subject, but will emphasize lectures #25-39 (MOSFET and BJT). *Calculator required.* Open book.

Reading material:

del Alamo, Ch. 11, §11.5 (§11.5.4) (only qualitatively)

Key questions

- Why does the performance of a BJT degrade at high collector current?
- How has BJT design evolved since its first integration? How is it likely to evolve in the future?
- Bipolar issues in CMOS???

1. Non-ideal effects in BJT (*cont.*)

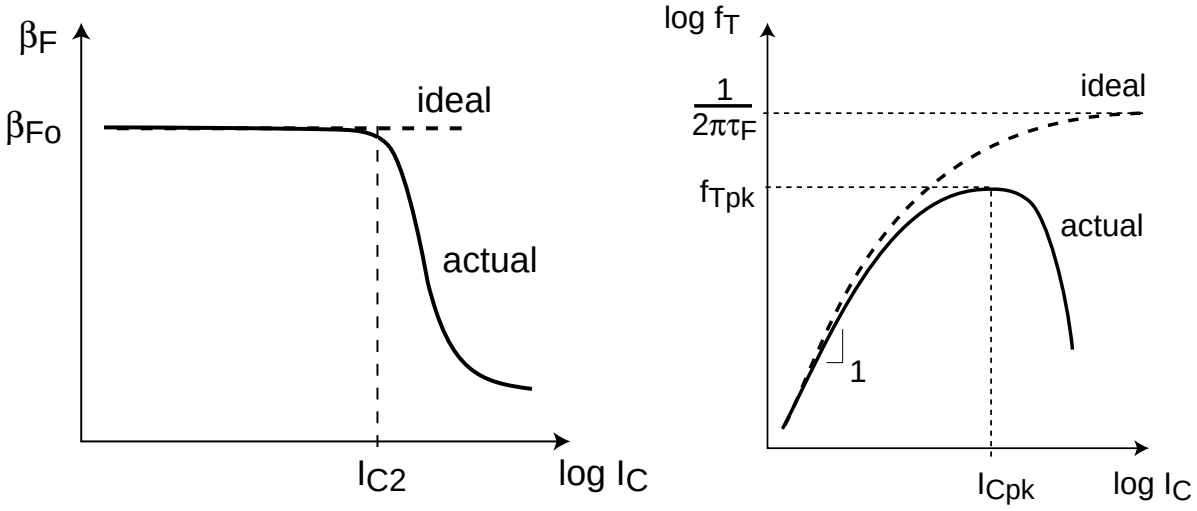
□ High collector current effects

As $I_C \uparrow$, electron velocity in collector $\uparrow$. But, there is a limit: v_{sat}.

Then, as I_C approaches:

$$I_{CK} = qA_E N_C v_{sat}$$

the electrostatics of the collector are profoundly modified $\Rightarrow$ transistor performance degrades:



To first order:

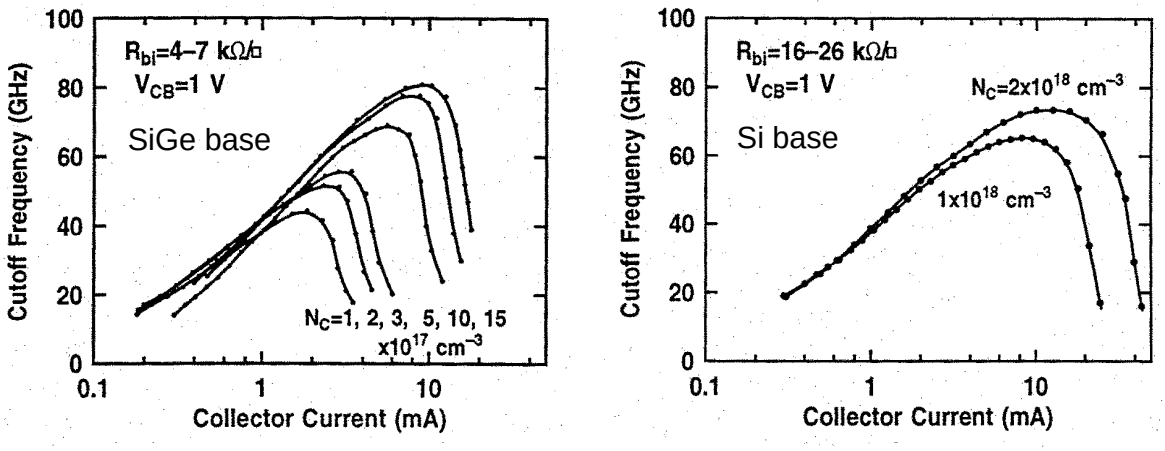
$$I_{C2} \simeq I_{Cpk} \simeq I_{CK}$$

Main origin: formation of *current-induced base* inside collector SCR $\Rightarrow$ effective quasi-neutral base width $\uparrow \Rightarrow \beta_F \downarrow \Rightarrow$ new delay component $\Rightarrow f_{Tpk} \downarrow$

Key design issue: N_C

$$N_C \uparrow \Rightarrow I_{CK} \uparrow \Rightarrow f_{Tpk} \uparrow$$

Experiments [Crabbé IEDM 1993]:

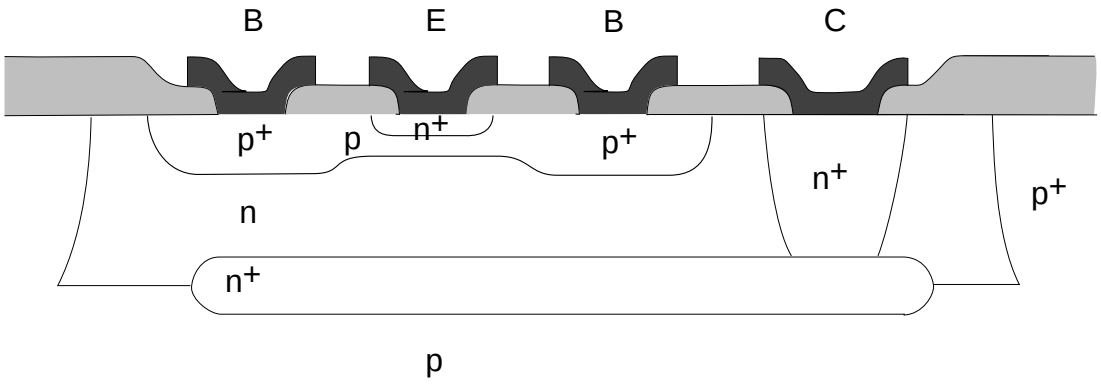


Key trade-off:

$$N_C \uparrow \Rightarrow BV \downarrow$$

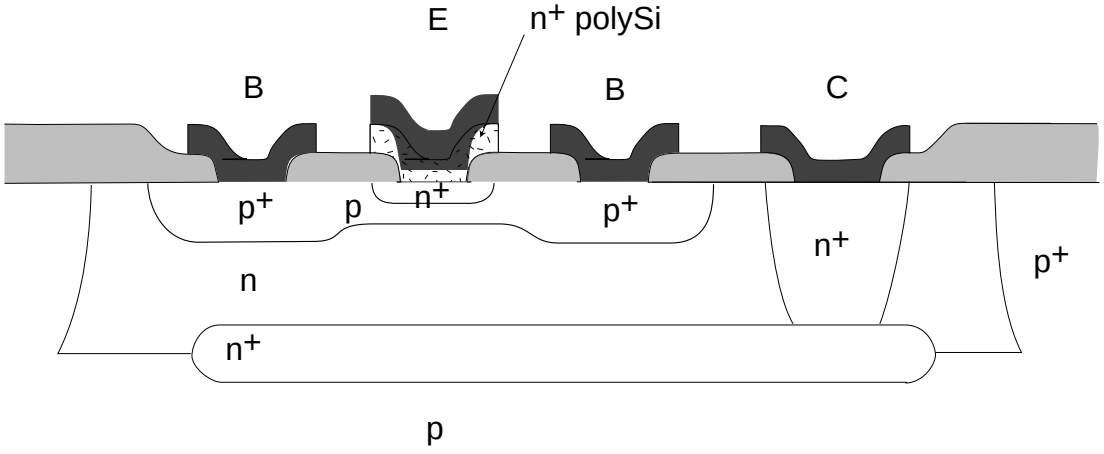
2. Evolution of BJT design

- *Junction-isolated BJT*

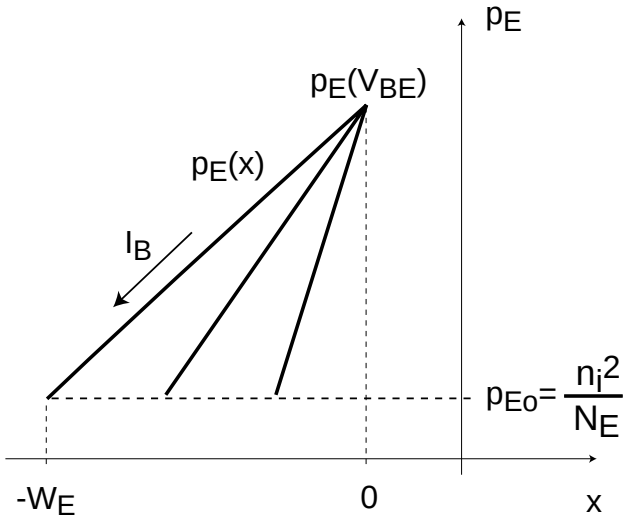


First integrated BJT.

- *Poly-Si emitter BJT*



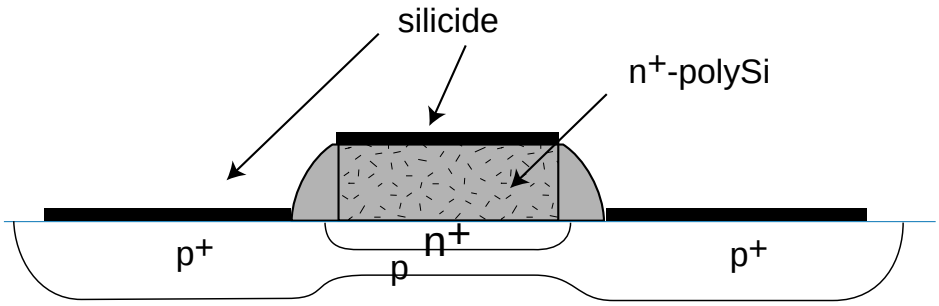
Problem of metal-contacted emitter: emitter thickness scales badly.



$$W_E \downarrow \Rightarrow I_B \uparrow \Rightarrow \beta_F \downarrow$$

Poly-Si extension effectively increases emitter thickness: β_F preserved when W_E scales down.

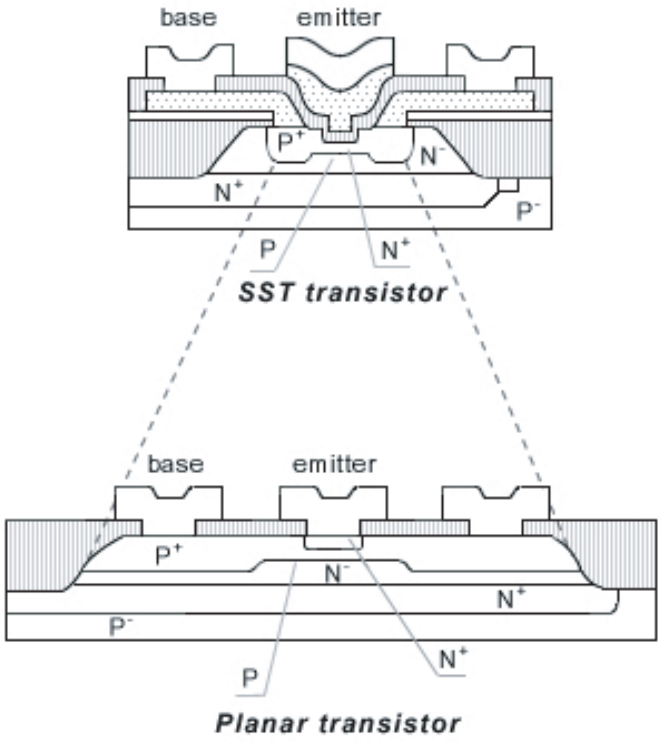
- *Single-poly self-aligned BJT*



Unique feature:

-extrinsic base self-aligned to intrinsic device $\Rightarrow \frac{A_C}{A_E} \downarrow, R_{Bext} \downarrow$

- *Double-poly self-aligned BJT*

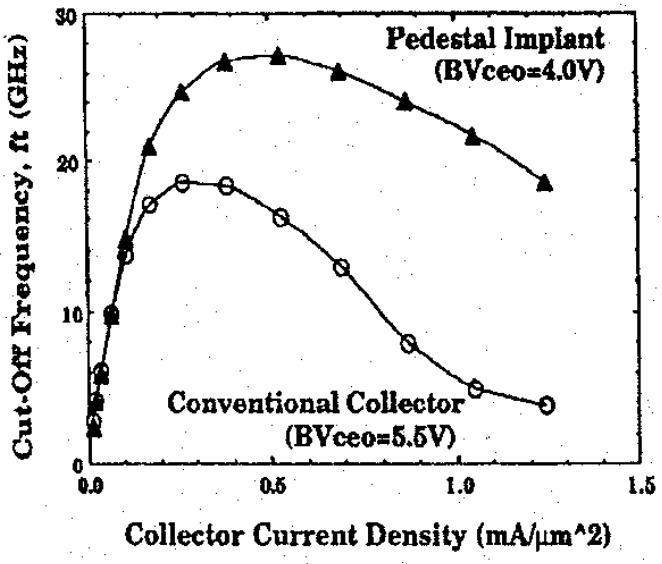


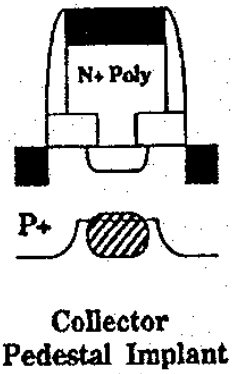
Bipolar transistor structure using Super Self-aligned Process Technology (SST). Adapted from T. Nakamura, ***IEEE Trans. Electron Dev. 42*** *(3), 390 (1995).*

Unique feature:

-base contacts made on polySi over isolation $\Rightarrow \frac{A_C}{A_E} \downarrow$, smaller footprint

• *Selectively-implanted collector (SIC) BJT*

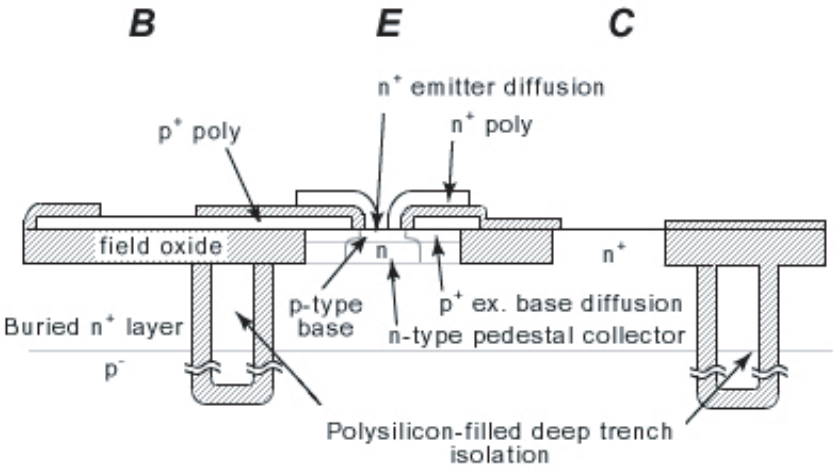




Unique feature:

-intrinsic collector doping level raised through self-aligned implant $\Rightarrow$ $J_{Cmax} \uparrow, f_T \uparrow$

- *Trench-isolated BJT*

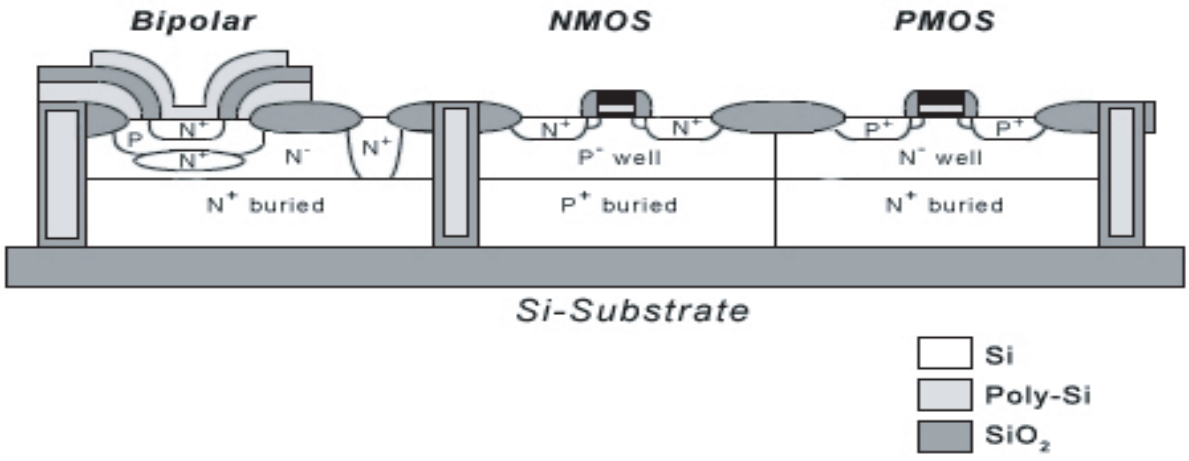


Schematic cross section of a double-polysilicon self-aligned bipolar device. Adapted from J. Warnock, ***IEEE Trans. Electron Dev. 42*** *(3), 377 (1995).*

Unique feature:

-deep-trench isolation $\Rightarrow$ $A_S \downarrow$

- *SOI-BJT*

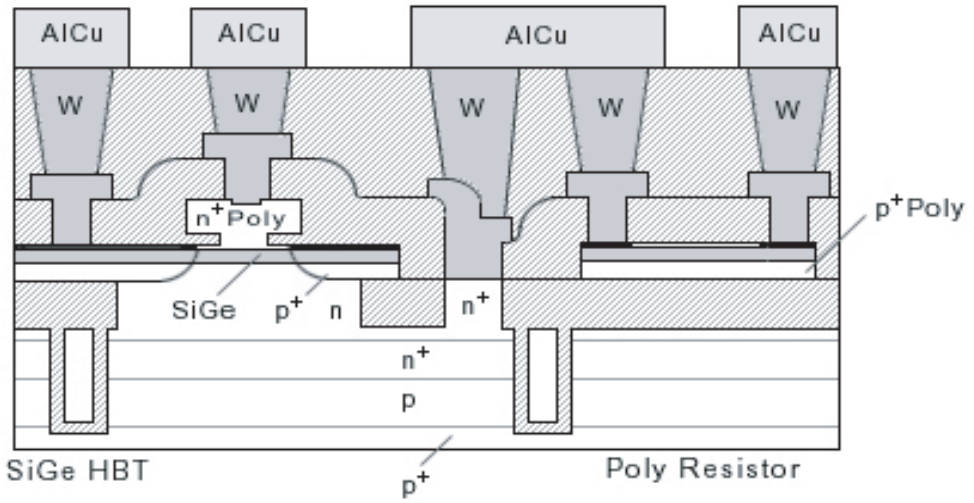


Adapted from T. Nakamura,
***IEEE Trans. Electron Dev. 42** (3), 390 (1995).*

Unique feature:

-silicon-on-insulator substrate $\Rightarrow$ $C_S \downarrow$, smaller footprint

- *Epitaxial SiGe HBT*



*Schematic cross section of the SiGe HBT used in this investigation. Adapted from J. A. Babcock et al., **IEDM**, 1995, p. 357.*

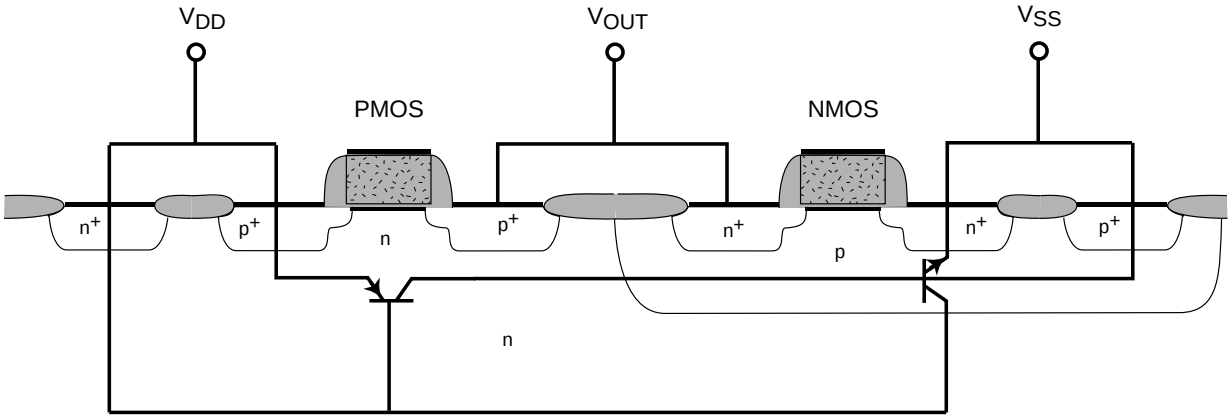
Unique features:

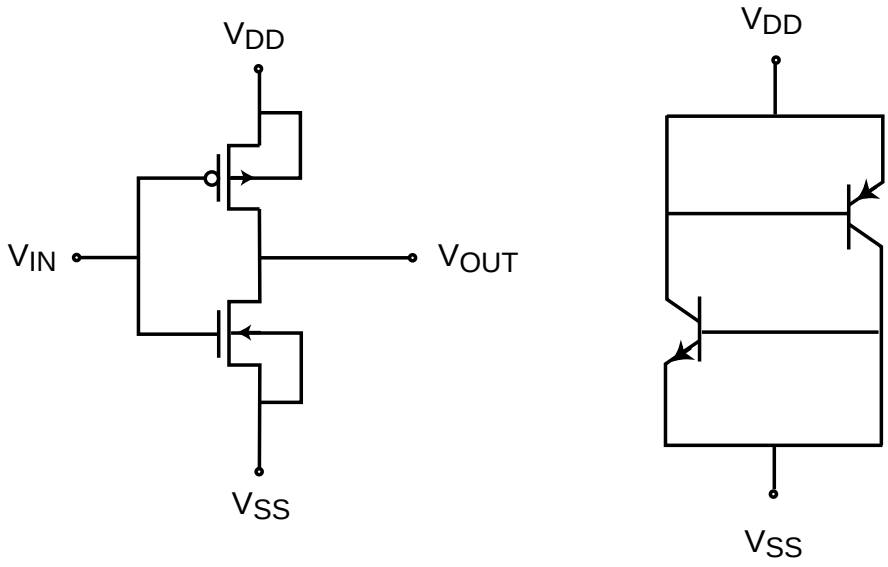
-epitaxial base: enhanced thickness and doping control $\Rightarrow W_B \downarrow$ $N_B \uparrow \rightarrow \ f_T \uparrow, R_B \downarrow$

-Ge in base: heterojunction effect, drift field in base (if gradient in Ge composition) $\Rightarrow I_S \uparrow, f_T \uparrow, R_B \downarrow, V_A \uparrow$

3. Bipolar issues in CMOS

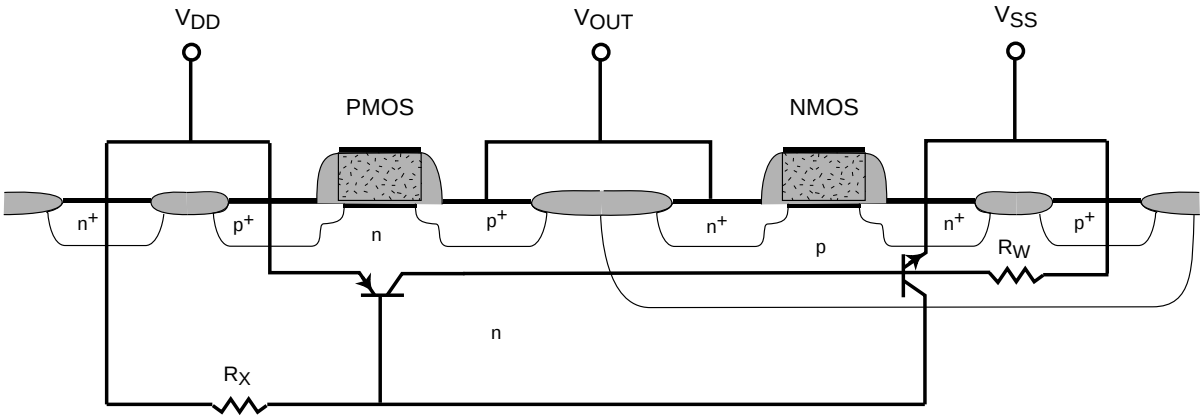
□ Latch up: interaction of two hidden BJT's inside a CMOS pair.



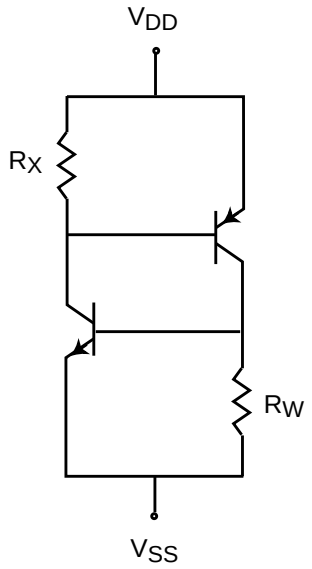


In principle, no problem because in both BJTs, $V_{BE} = 0$.

But there are also two parasitic resistors:



More complete equivalent circuit model:



Suppose for some reason, current flows through $R_X \Rightarrow$ pnp goes into FAR $\Rightarrow I_C(pnp) \uparrow \Rightarrow$ ohmic drop in $R_W \Rightarrow$ npn goes into FAR $\Rightarrow I_C(npn) \uparrow \Rightarrow$ more ohmic drop in R_X

POSITIVE FEEDBACK LOOP can cause device destruction.

Latch-up started by:

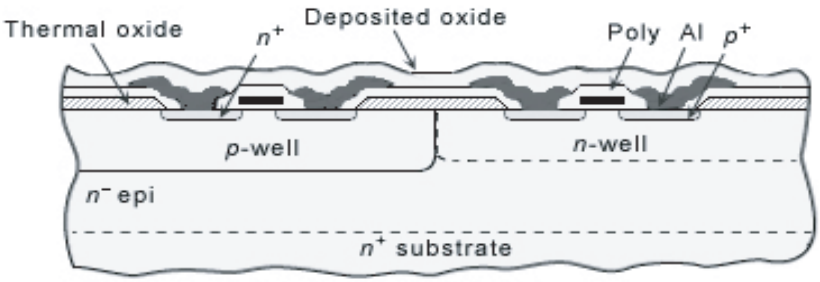
- minority carrier injection into substrate by transient forward bias on pn junctions (typically in input or output circuits)
- photogeneration by ionizing radiation
- impact ionization by hot carriers

Elimination of latch up:

- reduce R_X and R_W
- reduce β_{npn} and β_{pnp}

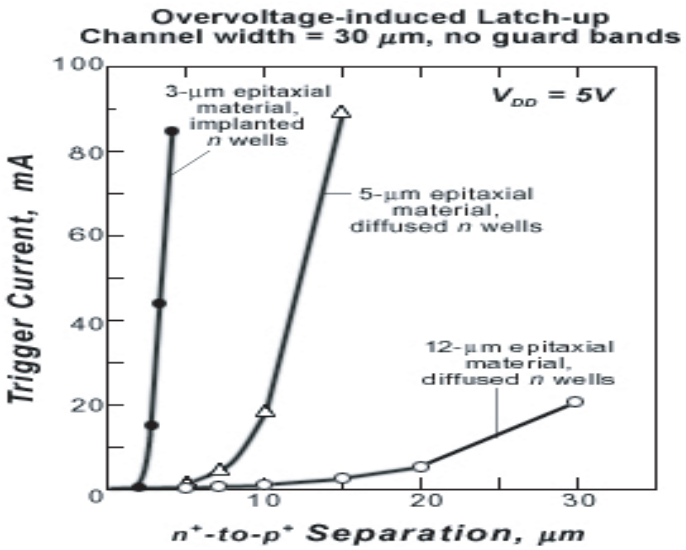
Then do:

- use heavily doped substrate (need lower doping epi layer on top for devices)
- sufficient transistor spacing
- guard rings at sensitive locations



An advanced twin-well process for VLSI CMOS applications. The high-conductivity substrate reduces susceptibilty to latch-up; the separately doped well regions provide precise control of MOSFET characteristics.

Adapted from R. S. Muller and T. I. Kamins, ***Device Electronics for Integrated Circuits, 2nd ed.****, Wiley, 1986, p. 463.*

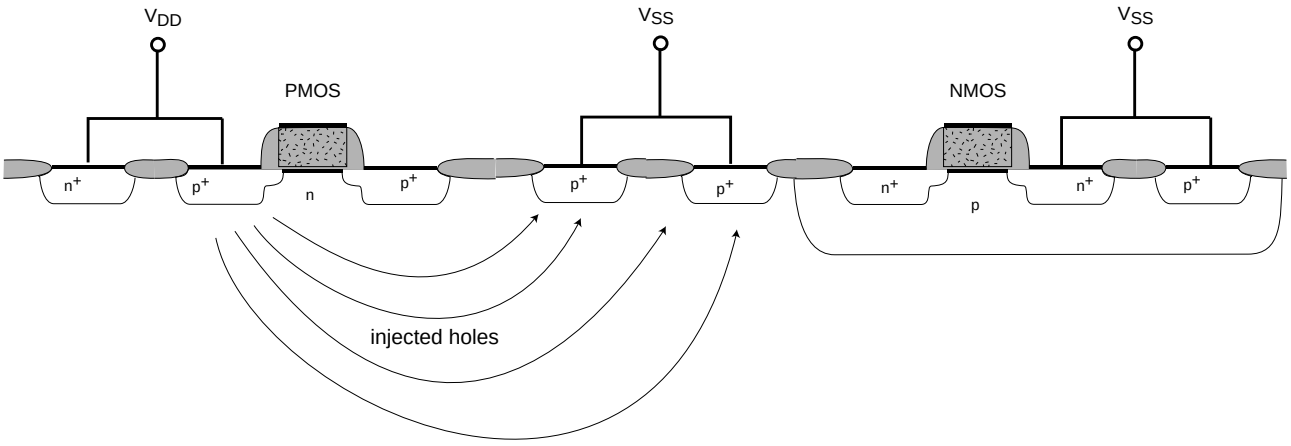


An n-well CMOS (a) structure with butted contacts and (b) triggering current vs. n+-to-p+ separation.

Adapted from E. S. Yang, ***Microelectronic Devices,*** *McGraw Hill, 1988, p. 315.*

- the higher the trigger current, the higher the immunity to latch-up
- thinner epi on top of n^+-substrate $\rightarrow$ better immunity
- larger n^+-p^+ spacing $\rightarrow$ better immunity

Guard ring: reverse-biased pn junction that collects injected holes.



Other bipolar effects in MOSFETs:

- Can't implement floating pn diodes in CMOS process
- Breakdown and snap-back (bipolar-induced breakdown)
- Floating-body effects in SOI MOSFETs

Key conclusions

- At high collector current, velocity saturation of electrons in collector $\Rightarrow$ performance degrades: $\beta_F \downarrow,\ f_T \downarrow$
- Maximum current:

$$I_{Cpk} \simeq qA_E N_C v_{sat}$$

- *Megatrends* of BJT development:
  footprint $\downarrow$, vertical dimensions $\downarrow$, $J_C \uparrow$, $f \uparrow$, $\tau \downarrow$, $BV \downarrow$.
- Bipolar effects pervasive in any device with multiple n and p regions.
- CMOS latch-up interaction of parasitic npn and pnp BJTs; can lead to device destruction.