Design Problem

Gate Material Options for Deep-Submicron CMOS Technology for High-Performance Microprocessor Applications

November 13, 2002
Due: December 2, 2002 at lecture

1. Introduction

In modern scaled-down CMOS, the gate material of choice for the n-channel MOSFET is n^+-polySi, while that of the p-channel MOSFET is p^+-polySi. As device scales down, a number of concerns with this approach are being raised. First, the resistance of the gate is increasing to the point that is starting to introduce a significant delay on the ability of wide devices to drive large interconnect lines. The resistance of the gate goes up in scaled-down devices because the gate length is getting shorter and because of edge effects, that is, narrow gate lines have a sheet resistance that is higher than wide gate lines.

The second problem with poly-Si gates is that even though they are heavily doped, a non-negligible fraction of the available gate voltage drops at its interface with the oxide. With the voltage budget and the oxide thickness going down, the fraction of the voltage lost in the gate is becoming significant. This phenomenon is called “poly depletion”.

A third concern is the diffusion of dopants from the gate to the channel during device fabrication. With a thick gate oxide, this is effectively suppresed. As the gate oxide is getting thinner, avoiding gate dopant diffusion through the gate oxide to the channel is starting to impose serious processing constraints that ultimately detract from performance.

All these problems point at the need to examine alternate gate materials for future deep-submicron generations of scaled-down CMOS. An attractive approach is a refractory metal gate. A metalic gate has a very small resistance with minimum RC time constant. A metal gate does not develop any surface potential and does not detract from the voltage applied to the inversion layer. Finally, since dopants are absent from a metal gate, dopant diffusion through the gate oxide is eliminated. There are certainly many issues to be worked out: process compatibility, fine-line definition, and reliability, among others.

The constraints imposed on a new gate technology are so severe that it would represent a great simplification if a single gate technology, as opposed to two (one for the n-MOSFET and another one for the p-MOSFET), is to be developed. In a unified gate approach, the gate should have a work function that lines up closely with the middle of the Si bandgap. This is likely to result in the

best compromise in performance for the n-channel and p-channel devices. A material with a work function close to this ideal one and with many attractive processing features is Tungsten. W has a work function of 4.54 eV. That is just 60 meV off the middle of the Si gap. W is a refractory material that is already extensively used in contact plugs in Si VLSI. Its use as a gate metal with ultra-thin gate oxides has already been demonstrated in the laboratory [1].

This exercise is about exploring the potential of W-gate CMOS for high-performance logic applications. This new technology is to be placed in contrast with the traditional approach based on dual n^+/p^+-polySi gates. This design problem illustrates key issues involved in CMOS device design for high-performance microprocessor applications.

2. Design Problem statement

You have been hired as a consultant by the CEO of an up-and-coming logic IC foundry firm to sort out options for the next CMOS generation: the 0.18 μm generation. The CEO does not have a technical background and needs help in choosing among several technology options that he has been presented with. The financial investment is very serious and only one of them can be pursued.

The VP for R&D is pushing for the development of a new W-gate technology that he has under research in the lab. In his opinion, this is a move that the company will eventually have to make anyway. By developing this technology early, he argues, the company will get ahead of its competitors and will put their company in the map as a hot-bed of new technology. If the company were to commit enough resources, he is confident that the technology can be completely developed and transferred to manufacturing in a timely way.

The VP for Manufacturing judges that the 0.18 μm generation is not the appropriate one for the deployment of a W-gate technology. The company has extensive experience on the dual n^+/p^+-polySi gate process. She claims she has a plan worked out to deal with the shortcomings of the traditional gate technology that allows its insertion in the 0.18 μm generation. She maintains that the expense of carrying this plan out is reasonable. She agrees that W might eventually be needed but introducing it with the 0.18 μm generation will be very expensive, will likely result in delays, and besides, it will not yield improved performance over the conventional approach.

The CEO wants you to study this matter and give him a recommendation. To understand the state of the art of VLSI technology in this company, the CEO has provided you with data regarding the 0.25 μm technology that his company is about to release to manufacturing. This is described in Appendix 1. This technology generation is characterized by a polysilicon gate length of 0.25 μm, a power supply of 2.5 V, an oxide thickness of 5 nm, and junction depths of 80 nm for the p- and n-channel devices.

The requirements for the 0.18 μm technology are as follows. As its name indicates, the physical gate length is going to be 0.18 μm. The tool set that is likely to be available for this generation limits the oxide thickness to values no smaller than 3.0 nm and junction depths no shallower than

[1] see, for example, D. A. Buchanan, F. R. McFeely, and J. J. Yurkas, "Fabrication of midgap metal gates compatible with ultrathin dielectrics", *Applied Physics Letters* **73**, 1676 (1998).

60 nm. The junction depths of the n-channel and p-channel devices need not be identical since the implanted species are different. The technology is to be used to make products that will operate at 1.8 V.

Since you have very limited time to submit your recommendation, on a first pass, you decide not to go into the lab with the VP of R&D to see how advanced his team is in the development of the new W-gate technology; you decide to give him the benefit of the doubt. You assume that he will be able to work things out and deliver the required technology on time. You decide to approach this task by evaluating the maximum potential of both a W-gate technology and the incumbent dual n^+/p^+-polySi gate technology and base your recommendation on what you find. Which ever one has the highest performance potential you will recommend that is selected for more detailed investigation.

Your assignment is to carry out a feasibility study of both technological options, to identify the one with the highest performance potential, and to write to the CEO with a recommendation for further study.

2.1 Detailed specifications

To complete this assignment, you have to carry out rough device design for a minimum-size logic inverter that is optimized for each gate technology. This calls for specifying the following attributes for the transistors:

- gate length, L_g (identical for n-MOS and p-MOS), is set at 0.18 μm;
- gate oxide thickness, x_{ox} (identical for n-MOS and p-MOS), no less than 3.0 nm; for the n^+/p^+-polySi gate technology, due to the presence of poly depletion, you should be limited to 3.5 nm; for the W gate technology, a limit of 3.0 nm is adequate;
- junction depth of n-channel device, x_{jn}, no less than 60 nm;
- junction depth of p-channel device, x_{jp}, no less than 60 nm;
- doping level of p-well, N_A;
- doping level of n-well, N_D.

The specs for the minimum-size device that the new technology has to meet are identical to the old technology that your client has just developed, *i.e.*:

- in order to maintain reliability, the *maximum gate oxide field*, $\mathcal{E}_{ox}^{max}$, for both devices should not exceed 6.0 MV/cm;
- also from reliability considerations, the *maximum channel field*, $\mathcal{E}_{m}^{max}$, should not exceed 0.50 MV/cm;
- to ensure manufacturability, DIBL should not exceed 60 mV/V;

- the static power consumption must be controlled by maintaining the *off current*, I_{off}, for each of the n- and p-channel devices below 100 pA.

The figures of merit to be optimized are:

- the dynamic power consumption in the minimum-size inverter (using two minimum-size transistors) as appraised by the *power-delay product*, (given in fJ);
- the device performance as appraised by the *inverter delay*, τ_{inv}, (given in ps).

The 0.18 μm technology is to operate at $V_{dd} = 1.8\ V$.

2.2 Approach

The best approach to accomplish this assignment in a short time is to use the first-order analytical relationships for the MOSFET presented in 6.720 to design optimized devices. For your convenience, these are summarized at the end of this document in Appendices 2 through 4. Appendix 5 lists the value of the fundamental constants that you need.

The device design process has two phases:

- In the first phase, the analytical approach is validated by applying it to the just developed 0.25 μm design (specs given in Appendix 1).
- In the second phase, the analytical approach is exploited to design optimized devices for the two gate technologies.

In the first phase, you have to program the analytical relationships in MATLAB, C, a spreadsheet program or any other software tool that you know. This should be done in a way that allows for quick change of inputs to get proper outputs. You should also be careful to provide enough intermediate results that help you to simplify the design process and validate the code.

2.3. Deliverables, rules, and grading

The deliverable is a package to the CEO that contains the following:

1. A *cover letter* stating your recommendation, summarizing the key reasons for it, and pointing out to the enclosed material that backs up your decision. Remember, the CEO is not a technical person. He understands dollars but not electrons (much less holes). The style of this letter should be business-like. It should show your professionalism. You might also want to use this opportunity to bill him for your work.

2. A *one-page technical abstract* that gives the details of the process you have followed in reaching your decision and the key technical arguments behind it. The abstract should indicate the physical mechanisms that limit the maximum performance that you can get out of each gate technology. The abstract should include up to two pages of figures with supporting technical material. Figures that you might consider are I_{off} vs. I_{on} (semilog scale) and $DIBL$ vs. I_{on} for the n-MOSFET and p-MOSFET for the three technologies considered in this work. The CEO is likely to use this abstract to argue his decision (yours, really!) in front of his technical people. The abstract has to be pitched to practicing engineers and it has to be able to convince them that your decision is well justified on technical grounds. The arguments have to be solid, otherwise, the decision of the CEO will be challenged. You might never be hired again.
3. The table of Appendix 6 should be included as an enclosure to the abstract. This table shows the detailed specs of the optimum designs that you have identified. No numerical figure should have more than two significant digits. We will check your results against our own code.

Here are the rules for carrying out this design problem. You can work in teams of two but every individual has to program the entire equation set. Working together will allow you to check each other's programming work and discuss together strategies for device optimization. If you work in teams, please indicate the name of your teammate at the top of the page of Appendix 6. The write up is an individual exercise. It should reflect the entire design process.

This exercise is worth 100 points. This maximum grade is broken down in the following way:

- *Cover letter: 20 points.* The cover letter will be judged for style and persuasiveness and for consistency with the findings summarized in the technical abstract.
- *Technical abstract: 30 points.* The technical abstract will be judged for technical accuracy and for clarity of presentation of the key points. Also the selection and clarity of the graphics will be taken into account.
- *Delivery of technical specifications*: 50 points. This reflects the technical correctness of your design as well as your success in optimizing device design for each gate technology.

Appendix 1: $L_g = 0.25\ \mu m$ **Technology**

Parameter	*units*	*NMOS*	*PMOS*
Device Specifications:			
Gate Oxide Thickness, x_{ox}	nm	5.0	
Junction Depth, x_j	nm	80	80
Well Doping, $N_{A,D}$	cm^{-3}	3.6×10^{17}	3.3×10^{17}
Gate work function, W_M	*eV*	4.04	5.16
Performance Targets:			
Off-state current, I_{off}	pA	90	92
Maximum Gate Oxide Field, $\mathcal{E}_{ox}^{max}$	MV/cm	5.0	5.0
Maximum Channel Field, $\mathcal{E}_m^{max}$	MV/cm	0.40	0.31
$DIBL$	mV/V	38	41
Power Delay Product, $C_{Load}V_{dd}^2$	fJ	108	
Inverter Delay, τ_{inv}	ps	38	
Other Outputs:			
Long Channel V_T, $V_T(long)$	V	0.39	-0.37
Drive Current, I_{drive}	mA	0.56	-0.57
Gate Delay, τ	ps	5.7	11
Subthreshold Slope, S	mV/dec	75	75
Load capacitance, C_{Load}	fF	17	

Table 1: Current Technology: $L_g = 0.25\ \mu m,\ V_{dd} = 2.5\ V$

Appendix 2: MOSFET definitions

Fig. 1 shows the cross-section and plan view of a typical MOSFET, defining the various geometrical parameters. The dimensions of the minimum-size transistor are related to each other as listed in Table 2. Note that once you fix the gate length, there are only two independent geometrical parameters that you have to determine, the gate oxide thickness, x_{ox}, and the junction depth, x_j. The remaining parameters, as seen in Table 2, are functions of these three. Note, in particular, that the width of the minimum size transistor is fixed and it scales with gate length.

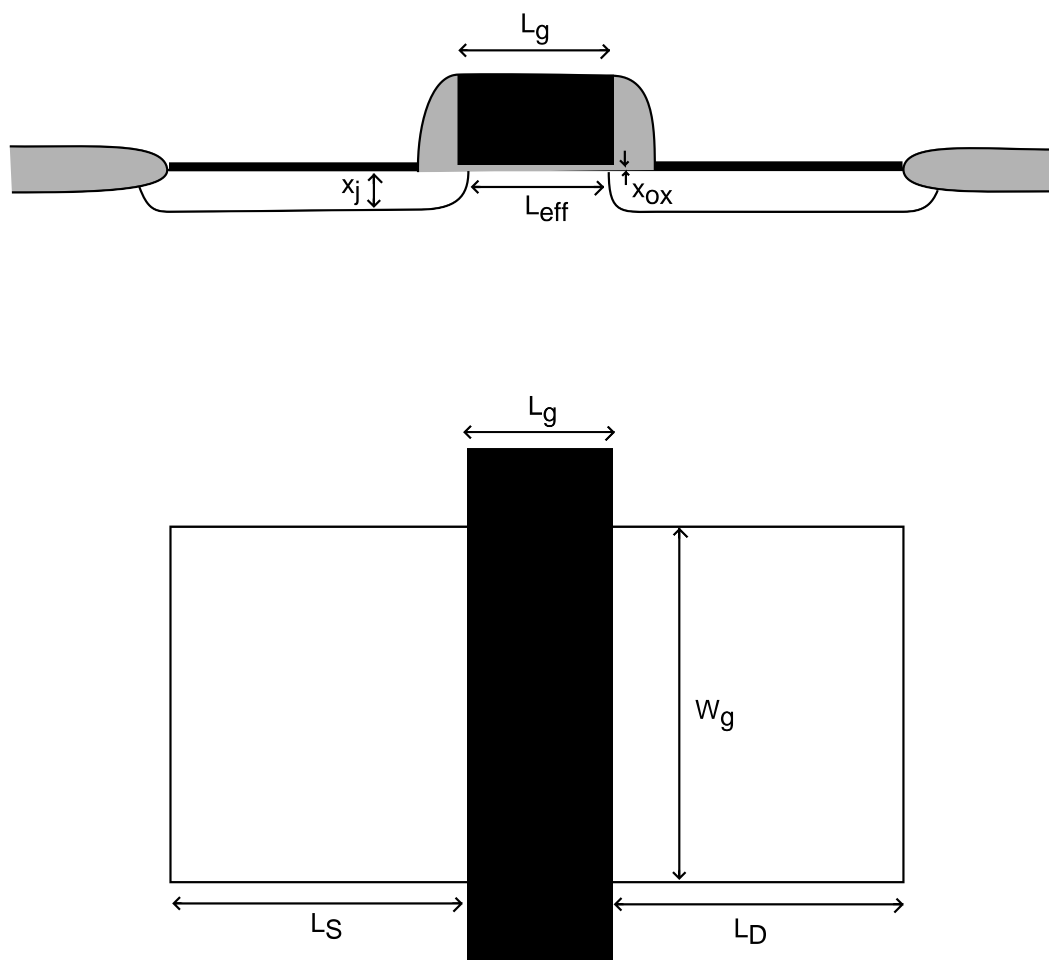

Figure 1: Cross-section and plan view of MOSFET indicating the various geometrical parameters.

Parameter	*Symbols*	*Value*	
		NMOS	*PMOS*
Gate Length	L_g	L_g	L_g
Effective Channel Length	L_{eff}	L_g - 1.4x_j	L_g - 1.4x_j
Junction Depth	x_j	x_j	x_j
Gate Width	W_g	3L_g	6L_g
Source Length	L_S	3L_g	3L_g
Drain Length	L_D	3L_g	3L_g
Gate Oxide Thickness	x_{ox}	x_{ox}	x_{ox}

Table 2: Minimum Size Device Dimensions

Additional considerations:

- The tubs are connected to the sources locally.
- All doping profiles are flat.

Appendix 3: MOSFET Equations

A. NMOS

Threshold Voltage

$$V_T = V_T(long) + \Delta V_T \tag{1}$$

where

$$\begin{aligned}
V_T(long) &= V_{FB} + \phi_{sth} - \frac{Q_{dmax}}{C_{ox}} && (2)\\
V_{FB} &= \frac{1}{q}(W_M - \chi_s - \frac{E_g}{2} - kT \ln \frac{N_A}{n_i}) && (3)\\
\phi_{sth} &= 2\phi_f + \frac{kT}{q} && (4)\\
\phi_f &= \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right) && (5)\\
Q_{dmax} &= -\sqrt{2\epsilon_s q N_A \phi_{sth}} && (6)\\
C_{ox} &= \frac{\epsilon_{ox}}{x_{ox}} && (7)
\end{aligned}$$

Total V_T shift

$$\Delta V_T = -[3(V_{bi} - \phi_{sth}) + V_{DS}]e^{-L_{eff}/\lambda} - 2\sqrt{(V_{bi} - \phi_{sth})(V_{bi} - \phi_{sth} + V_{DS})}e^{-L_{eff}/2\lambda} \tag{8}$$

where

$$\begin{aligned}
\lambda &= \sqrt{\frac{\epsilon_s x_{ox} x_{dmax}}{\epsilon_{ox}}} && (9)\\
x_{dmax} &= \sqrt{\frac{2\epsilon_s \phi_{sth}}{q N_A}} && (10)\\
V_{bi} &= \frac{E_g}{2q} + \phi_f && (11)\\
& && (12)
\end{aligned}$$

V_{bi} is the source or drain built-in potential of the source-drain /well junctions, E_g is the silicon bandgap in electron volts.

The $DIBL$ figure of merit is:

$$DIBL = |\frac{V_T(V_{DS} = V_{dd}) - V_T(V_{DS} = 0.05\ V)}{V_{dd} - 0.05}| \tag{13}$$

Drive Current

$$I_{drive} = I_{dsat}(V_{gs} = V_{dd}, V_{ds} = V_{dd}) \tag{14}$$

where

$$I_{dsat} = v_{sat} W_g C_{ox} \left[(V_{gs} - V_T) - V_{dsat}\right] \tag{15}$$

$$V_{dsat} = \sqrt{V_c^2 + 2(V_{gs} - V_T)V_c} - V_c \tag{16}$$

$$V_c = \mathcal{E}_c L_{eff} \tag{17}$$

$$\mathcal{E}_c = \frac{v_{sat}}{\mu_{eff}} \tag{18}$$

$$\mu_{eff} = \frac{\mu_{n0}}{1 + (\frac{|\mathcal{E}_{av}|}{\mathcal{E}_0})^\alpha} \tag{19}$$

$$|\mathcal{E}_{av}| = \frac{V_{gs} + V_T - 2(V_{FB} + \phi_{sth})}{6x_{ox}} \tag{20}$$

Gate Delay

$$\tau = \frac{C_g V_{dd}}{I_{drive}} \tag{21}$$

where

$$C_g = C_{ox} L_g W_g \tag{22}$$

Off-state Current

$$I_{off} = I_{sub}(V_{gs} = 0, V_{ds} = V_{dd}) \tag{23}$$

where

$$I_{sub} = \frac{W_g}{L_{eff}} \mu_{n0} (\frac{kT}{q})^2 C_{s,th} \exp \frac{q(V_{gs} - V_T)}{nkT} \tag{24}$$

$$n = 1 + \frac{C_{s,th}}{C_{ox}} \tag{25}$$

$$C_{s,th} = \sqrt{\frac{q\epsilon_s N_A}{2\phi_{sth}}} = \frac{\epsilon_s}{x_{dmax}} \tag{26}$$

Subthreshold Slope

$$S = n\frac{kT}{q}\ln 10 \tag{27}$$

Maximum Gate Oxide Field

$$\mathcal{E}_{ox}^{max} = \frac{V_{dd}}{x_{ox}} \tag{28}$$

Maximum Channel Field

$$\mathcal{E}_{m}^{max} = \mathcal{E}_m(V_{ds} = V_{dd}, V_{gs} = V_{dd}) \tag{29}$$

where

$$\mathcal{E}_m = \left[\frac{(V_{ds} - V_{dsat})^2}{l^2} + \mathcal{E}_c^2\right]^{1/2} \tag{30}$$

$$l^2 = \frac{\epsilon_s}{\epsilon_{ox}} x_{ox} x_j \tag{31}$$

The V_{gs} dependence of $\mathcal{E}_m^{max}$ arises from the V_{dsat} dependence on V_{gs}.

B. PMOS

Threshold Voltage

$$V_T = V_T(long) + \Delta V_T \tag{32}$$

where

$$V_T(long) = V_{FB} + \phi_{sth} - \frac{Q_{dmax}}{C_{ox}} \tag{33}$$

$$V_{FB} = \frac{1}{q}(W_M - \chi_s - \frac{E_g}{2} + kT\ln\frac{N_D}{n_i}) \tag{34}$$

$$\phi_{sth} = -2\phi_f - \frac{kT}{q} \tag{35}$$

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) \tag{36}$$

$$Q_{dmax} = \sqrt{2\epsilon_s q N_D |\phi_{sth}|} \tag{37}$$

$$C_{ox} = \frac{\epsilon_{ox}}{x_{ox}} \tag{38}$$

Total V_T shift

$$\Delta V_T = [3(V_{bi} - |\phi_{sth}|) + |V_{DS}|]e^{-L_{eff}/\lambda} + 2\sqrt{(V_{bi} - |\phi_{sth}|)(V_{bi} - |\phi_{sth}| + |V_{DS}|)}e^{-L_{eff}/2\lambda} \quad (39)$$

where

$$\lambda = \sqrt{\frac{\epsilon_s x_{ox} x_{dmax}}{\epsilon_{ox}}} \quad (40)$$

$$x_{dmax} = \sqrt{\frac{2\epsilon_s|\phi_{sth}|}{qN_D}} \quad (41)$$

$$V_{bi} = \frac{E_g}{2q} + \phi_f \quad (42)$$

The $DIBL$ figure of merit is:

$$DIBL = |\frac{V_T(V_{DS} = -V_{dd}) - V_T(V_{DS} = -0.05\ V)}{V_{dd} - 0.05}| \quad (43)$$

Drive Current

$$I_{drive} = I_{dsat}(V_{gs} = -V_{dd}, V_{ds} = -V_{dd}) \quad (44)$$

where

$$I_{dsat} = v_{sat} W_g C_{ox} [(V_{gs} - V_T) - V_{dsat}] \quad (45)$$

$$V_{dsat} = -\sqrt{[V_c^2 - 2(V_{gs} - V_T)V_c]} + V_c \quad (46)$$

$$V_c = \mathcal{E}_c L_{eff} \quad (47)$$

$$\mathcal{E}_c = \frac{v_{sat}}{\mu_{eff}} \quad (48)$$

$$\mu_{eff} = \frac{\mu_{p0}}{1 + \frac{|\mathcal{E}_{av}|}{\mathcal{E}_o}} \quad (49)$$

$$|\mathcal{E}_{av}| = |\frac{V_{gs} + V_T - 2(V_{FB} + \phi_{sth})}{6x_{ox}}| \quad (50)$$

Gate Delay

$$\tau = \frac{C_g V_{dd}}{|I_{drive}|} \quad (51)$$

where

$$C_g = C_{ox} L_g W_g \tag{52}$$

Off-State Current

$$I_{off} \quad = \quad |I_{sub}(V_{gs} = 0, V_{ds} = -V_{dd})| \tag{53}$$

where

$$I_{sub} \quad = \quad -\frac{W_g}{L_{eff}} \mu_{p0} (\frac{kT}{q})^2 C_{s,th} \exp \frac{-q(V_{gs} - V_T)}{nkT} \tag{54}$$

$$n \quad = \quad 1 + \frac{C_{s,th}}{C_{ox}} \tag{55}$$

$$C_{s,th} \quad = \quad \sqrt{\frac{q \epsilon_s N_D}{2|\phi_{sth}|}} = \frac{\epsilon_s}{x_{dmax}} \tag{56}$$

$$\tag{57}$$

Subthreshold Slope

$$S = n \frac{kT}{q} \ln 10 \tag{58}$$

Maximum Gate Oxide Field

$$\mathcal{E}_{ox}^{max} = \frac{V_{dd}}{x_{ox}} \tag{59}$$

Maximum Channel Field

$$\mathcal{E}_m^{max} = \mathcal{E}_m(V_{ds} = -V_{dd}, V_{gs} = -V_{dd}) \tag{60}$$

where

$$\mathcal{E}_m \quad = \quad \left[\frac{(V_{ds} - V_{dsat})^2}{l^2} + \mathcal{E}_c^2 \right]^{1/2} \tag{61}$$

$$l^2 \quad = \quad \frac{\epsilon_s}{\epsilon_{ox}} x_{ox} x_j \tag{62}$$

The V_{gs} dependence arises from V_{dsat} dependence on V_{gs}.

Apppendix 4: MOSFET capacitances

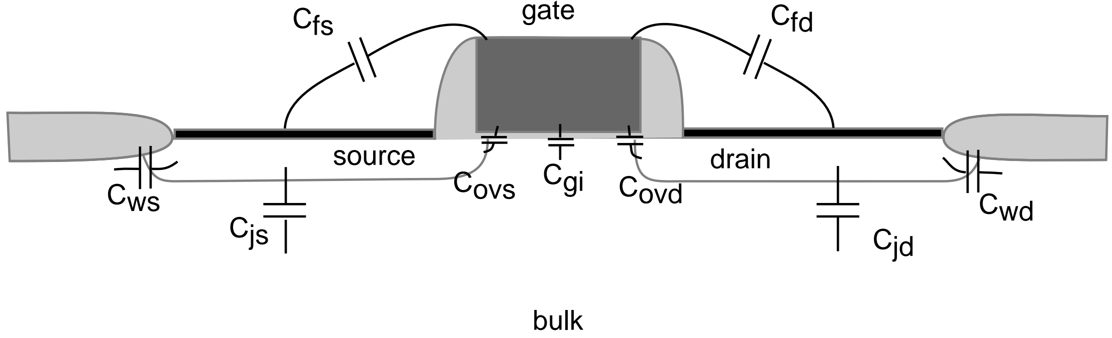

Figure 2: MOSFET Capacitors.

Summary of individual capacitances

Fig. 2 shows the various capacitances associated with a MOSFET. They are defined as follows:

- C_{gi}, the capacitance between gate and channel. To a first order, it is given by $C_{ox}L_{eff}W_g$.
- C_{fs}, the fringing capacitance between gate and source.
- C_{fd}, the fringing capacitance between gate and drain. Fringing capacitance is defined per unit gate width for a particular process. C_{fs} and C_{fd} are therefore each given by $C_{f0}W_g$ where C_{f0} is the fringing capacitance per unit width. For this design,

$$C_{f0} = 0.13 \text{ fF}/\mu m. \tag{63}$$

- C_{ovs}, gate-source overlap capacitance.
- C_{ovd}, gate-drain overlap capacitance. C_{ovd} and C_{ovs} are each given by $0.7x_jW_gC_{ox}$.
- C_{js}, the source-well junction capacitance.
- C_{jd}, the drain-well junction capacitance. Junction capacitance per unit area is given by:

$$C_j = \frac{\epsilon_s}{x_{dep}} \tag{64}$$

where

$$x_{dep} = \sqrt{\frac{2\epsilon_s(V_{bi} + V_{av})}{qN_{well}}} \tag{65}$$

and N_{well} is the well doping. V_{bi} is the source/drain-well built-in potential (see Appendix 3). V_{av} is the average reverse voltage across the junction in a switching event. For the source junction: $V_{av} = 0$; for the drain junction: $V_{av} = V_{dd}/2$.

- C_{ws}, the source-well sidewall capacitance.
- C_{wd}, the drain-well sidewall capacitance. Sidewall capacitance is defined per unit length for a particular technology. For this design,

$$C_{w0} = 0.33 \text{ fF}/\mu m. \tag{66}$$

Table 3 is a summary of the above capacitances.

Symbol	*Expression or Value*
C_{gi}	$C_{ox}L_{eff}W_g$
C_{fs}	$C_{f0}W_g$
C_{fd}	$C_{f0}W_g$
C_{ovs}	$0.7x_jW_gC_{ox}$
C_{ovd}	$0.7x_jW_gC_{ox}$
C_{js}	$C_jL_SW_g$
C_{jd}	$C_jL_DW_g$
C_{ws}	$C_{w0}(W_g + 2L_S)$
C_{wd}	$C_{w0}(W_g + 2L_D)$

Table 3: MOSFET Capacitances

Lumped Capacitance Model

Fig. 3 shows a lumped capacitance model that corresponds to the detailed capacitance picture of Fig. 2. The values of the capacitors shown in Fig. 3 depend on the regime of operation. Table 4 details the relationship between the various elements in the two figures for the case in which the MOSFET is in the saturation regime.

Symbol	*Expression*
C_{gs}	$C_{fs} + C_{gi} + C_{ovs}$
C_{gd}	$C_{fd} + C_{ovd}$
C_{sb}	$C_{js} + C_{ws}$
C_{db}	$C_{jd} + C_{wd}$

Table 4: Lumped MOSFET Capacitances in Saturation

Load Capacitance

The load capacitance C_{Load} is the total capacitance seen by a minimum-size inverter driving another minimum-size inverter. Fig. 4 shows the circuit. Table 5 shows the breakdown of the load capacitance in terms of the lumped capacitance model of Fig 3. A third subscript is added to denote the type of device. C_1, C_2, C_6 and C_7 are doubled their geometrical value because of the *digital Miller effect*. This arises from the fact that as the input voltage of an inverter swings up, the output voltage swings down at about the same rate. In consequence, the "effective" capacitance appears doubled.

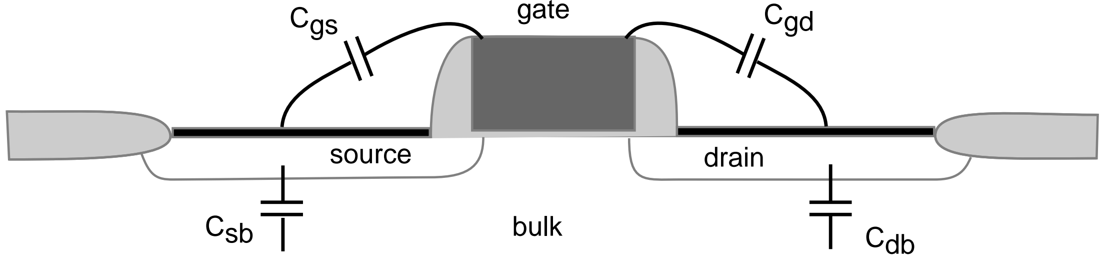

Figure 3: MOSFET Capacitors: Lumped Model

The load capacitance is typically broken into *input* and *output* capacitances. The input capacitance is associated with the inverter being driven, that is:

$$C_{Load}^{input} = C_5 + C_6 + C_7 + C_8 \tag{67}$$

The output capacitance is associated with the driving inverter:

$$C_{Load}^{output} = C_1 + C_2 + C_3 + C_4 \tag{68}$$

Strictly speaking, all junction capacitances depend on the voltage across. In a first-pass rough calculation of C_{Load}, this dependence can be neglected.

Typically, the input and output capacitances are of similar magnitude. In addition to these two

Symbol	*Expression*
C_1	$2C_{gdp}$
C_2	$2C_{gdn}$
C_3	C_{dbp}
C_4	C_{dbn}
C_5	C_{gsp}
C_6	$2C_{gdp}$
C_7	$2C_{gdn}$
C_8	C_{gsn}
C_{metal}	see text

Table 5: Breakdown of Components of Load Capacitance

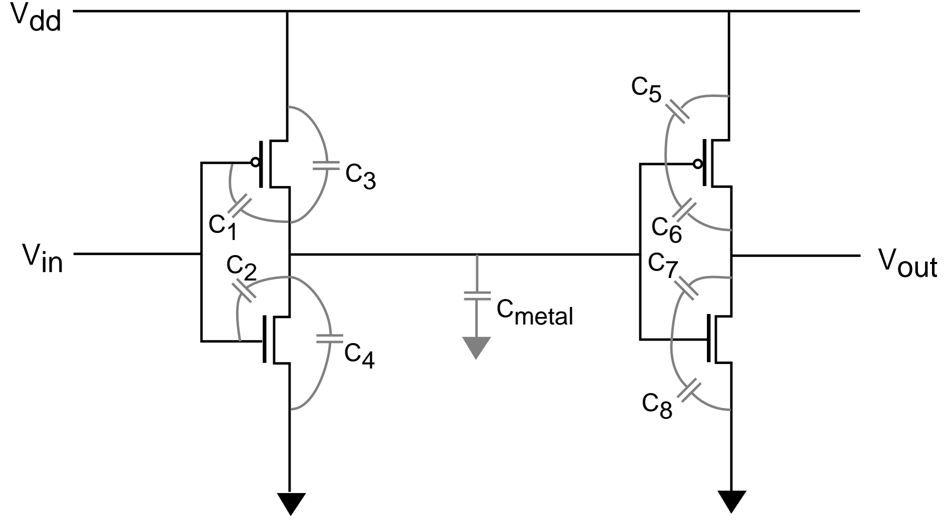

Figure 4: Capacitances in minimum-size inverter.

capacitances, there is the *metal capacitance* associated with the wiring of the two inverters. This has a magnitude similar to the input and output capacitances. For simplicity, then:

$$C_{metal} = \frac{1}{2}(C_{Load}^{input} + C_{Load}^{output}) \tag{69}$$

All together, the load capacitance is:

$$C_{Load} = C_{Load}^{input} + C_{Load}^{output} + C_{metal} \tag{70}$$

Inverter figures of merit

There are two key figures of merit for the minimum-size inverter: the *power-delay product* and the *inverter delay*. The power-delay product is given by:

$$PDP = C_{Load}V_{dd}^2 \tag{71}$$

The inverter delay can be approximated by:

$$\tau_{inv} = \frac{1}{4}C_{Load}V_{dd}(\frac{1}{I_{driven}} + \frac{1}{|I_{drivep}|}) \tag{72}$$

Appendix 5: Fundamental Constants

General:

$$q = 1\ e = 1.6 \times 10^{-19}\ C$$

$$kT\ (300\ K) = 0.0259\ eV$$

$$n_i\ (300\ K) = 1.07 \times 10^{10}\ cm^{-3}$$

$$\epsilon_s = 1.04 \times 10^{-12}\ F/cm$$

$$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$$

$$E_g\ (300\ K) = 1.124\ eV$$

$$\chi_s = 4.04\ eV$$

nMOS:

$$v_{sat} = 1 \times 10^7\ cm/s$$

$$\mu_{n0} = 670\ cm^2/V \cdot s$$

$$\mathcal{E}_0 = 0.67 \times 10^6\ V/cm$$

$$\alpha = 1.6$$

$$W_M(n^+ - polySi) = 4.04\ eV$$

$$W_M(W) = 4.54\ eV$$

pMOS:

$$v_{sat} = 7.5 \times 10^6\ cm/s$$

$$\mu_{p0} = 160\ cm^2/V \cdot s$$

$$\mathcal{E}_0 = 0.7 \times 10^6\ V/cm$$

$$W_M(p^+ - polySi) = 5.16\ eV$$

$$W_M(W) = 4.54\ eV$$

Appendix 6: Options for $L_g = 0.18\ \mu m,\ V_{dd} = 1.8\ V$ Technology

Name:

Teammate:

Parameter	*units*	*NMOS*	*PMOS*	*specification*
N+/P+ DUAL-GATE TECHNOLOGY				
Device Specs:				
Gate Oxide Thickness, x_{ox}	nm			≥3.5
Junction Depth, x_j	nm			≥60
Well Doping $N_{A,D}$	cm^{-3}			
Performance Targets:				
Off-state current, I_{off}	pA			≤100
Maximum Gate Oxide Field, $\mathcal{E}_{ox}^{max}$	MV/cm			≤6.0
Maximum Channel Field, $\mathcal{E}_{m}^{max}$	MV/cm			≤0.50
DIBL	mV/V			≤60
Power Delay Product, $C_{Load}V_{dd}^2$	fJ			optimize
Inverter Delay, τ_{inv}	ps			optimize
Other Outputs:				
Long Channel V_T, $V_T(long)$	V			
Drive Current, I_{drive}	mA			
Gate Delay, τ	ps			
Subthreshold Slope, S	mV/dec			
Load capacitance, C_{Load}	fF			
W-GATE TECHNOLOGY				
Device Specs:				
Gate Oxide Thickness, x_{ox}	nm			≥3.0
Junction Depth, x_j	nm			≥60
Well Doping $N_{A,D}$	cm^{-3}			
Performance Targets:				
Off-state current, I_{off}	pA			≤100
Maximum Gate Oxide Field, $\mathcal{E}_{ox}^{max}$	MV/cm			≤6.0
Maximum Channel Field, $\mathcal{E}_{m}^{max}$	MV/cm			≤0.50
DIBL	mV/V			≤60
Power Delay Product, $C_{Load}V_{dd}^2$	fJ			optimize
Inverter Delay, τ_{inv}	ps			optimize
Other Outputs:				
Long Channel V_T, $V_T(long)$	V			
Drive Current, I_{drive}	mA			
Gate Delay, τ	ps			
Subthreshold Slope, S	mV/dec			
Load capacitance, C_{Load}	fF			