Lecture 26 - The "Long" Metal-Oxide-Semiconductor Field-Effect Transistor *(cont.)*

November 4, 2002

Contents:

1. Inversion layer transport *(cont.)*
2. Current-voltage characteristics of ideal MOSFET

Reading assignment:

del Alamo, Ch. 9, §9.2

Announcement:

Quiz 2: November 5, Rm. 50-340 (Walker), 7:30-9:30 PM; lectures #13-24 (or Chapters 6-8 but excluding three-terminal MOS structure). Open book. *Calculator required.*

Seminar:

Nov. 5 - W. Gass (TI): *Digital Signal Processors: Past, Present, and Future.* Rm. 34-101, 4 PM.

Key questions

- What are the most important regimes of operation of a MOSFET?
- What are the key functional dependencies of the MOSFET drain current on the gate and drain voltage?
- Why under some conditions does the drain current saturate?

1. Inversion layer transport *(cont.)*

Inversion layer current equation:

$$J_e = \mu_e[Q_i(y) - \frac{kT}{q}C_{ox}]\frac{dV(y)}{dy}$$

Relative contribution of drift vs. diffusion:

$$Q_i(y) \quad \text{vs.} \quad \frac{kT}{q}C_{ox}$$

or

$$V_G - V(y) - V_{th} \quad \text{vs.} \quad \frac{kT}{q}$$

Two cases:

- *Strong inversion*: $V_G - V(y) - V_{th} \gg \frac{kT}{q}$, drift prevails over diffusion.

$$J_e \simeq \mu_e Q_i(y)\frac{dV(y)}{dy}$$

- *Close to threshold*: $V_G - V(y) - V_{th} \simeq \frac{kT}{q}$, diffusion significant

⇒ diffusion significant at pinch-off point and subthreshold regime.

☐ **Check assumptions** [see details in notes]:

- *Gradual-channel approximation*

$$\frac{\partial \mathcal{E}_x}{\partial x} \gg \frac{\partial \mathcal{E}_y}{\partial y}$$

Roughly ranslates into lateral field being much smaller than an effective vertical field.

Easily satisfied except around V_{th}, where $V_G - V(y) - V_{th} \simeq 0$

- *Sheet-charge approximation*

$n(x,y)$ must change with x much faster than $\mathcal{E}_y(x,y)$, or:

$$|\frac{1}{n}\frac{\partial n}{\partial x}| \gg |\frac{1}{\mathcal{E}_y}\frac{\partial \mathcal{E}_y}{\partial x}|$$

Equivalent to (see notes):

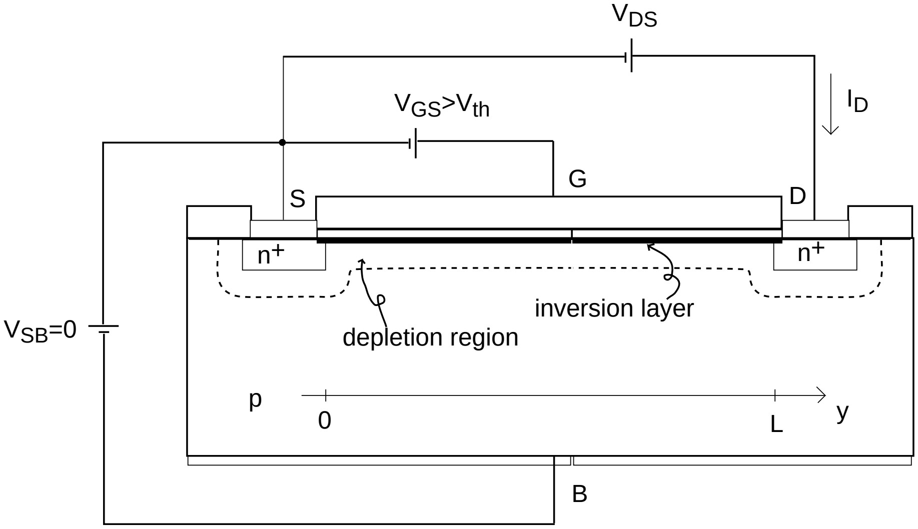
$$|Q_i| \gg \frac{kT}{q}C_{ox}$$

Statement of gradual-channel approximation!

Hence if GCA is fulfilled, SCA is also fulfilled.

2. Current-voltage characteristics of ideal MOSFET

□ Consider MOSFET in *linear regime* ($V_{GS} > V_{th}, V_{GD} > V_{th}$):



Current equation in strong inversion:

$$J_e = \mu_e Q_i \frac{dV(y)}{dy}$$

Charge control relation:

$$Q_i = -C_{ox}(V_{GS} - V - V_{th})$$

Combine into first-order differential equation:

$$J_e = -\mu_e C_{ox}(V_{GS} - V - V_{th})\frac{dV}{dy}$$

Separate variables:

$$J_e dy = -\mu_e C_{ox}(V_{GS} - V - V_{th})dV$$

Integrate from $y = 0$ ($V = 0$) to $y = L$ ($V = V_{DS}$):

$$J_e \int_0^L dy = -\mu_e C_{ox} \int_0^{V_{DS}} (V_{GS} - V - V_{th})dV$$

To get:

$$J_e = -\frac{\mu_e C_{ox}}{L}(V_{GS} - \frac{1}{2}V_{DS} - V_{th})V_{DS}$$

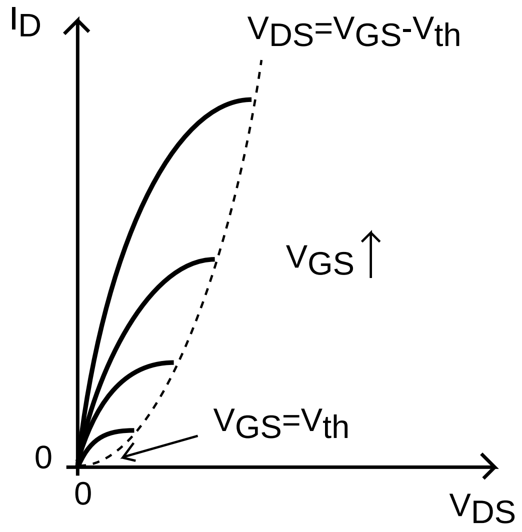
Terminal drain current:

$$I_D = -W J_e = \frac{W}{L}\mu_e C_{ox}(V_{GS} - V_{th} - \frac{1}{2}V_{DS})V_{DS}$$

Result valid as long as strong inversion prevails in all points of channel. Worst point: $y = L$, for which:

$$Q_i(y = L) = -C_{ox}(V_{GS} - V_{DS} - V_{th})$$

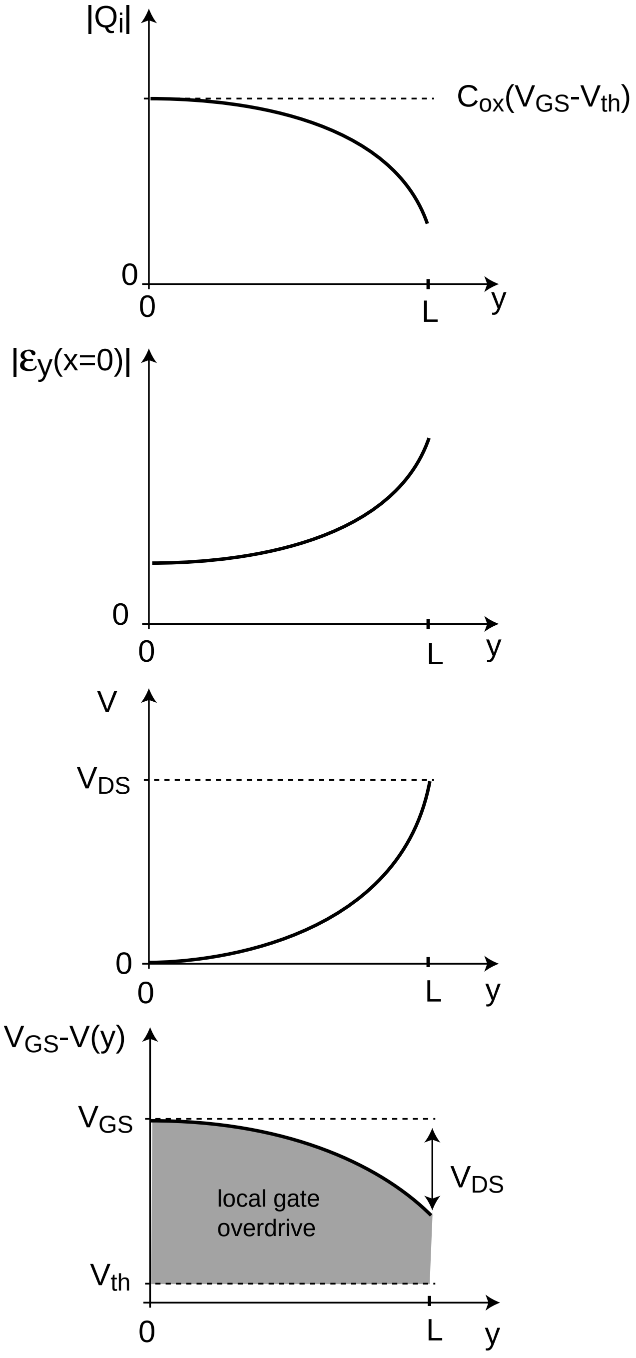
Therefore, need $V_{DS} < V_{GS} - V_{th}$, or $V_{GD} > V_{th}$.



$$I_D = \frac{W}{L}\mu_e C_{ox}(V_{GS} - V_{th} - \frac{1}{2}V_{DS})V_{DS}$$

Key dependences of I_D in linear regime:

- $V_{DS} = 0 \Rightarrow I_D = 0$ for all V_{GS}.
- For $V_{GS} > V_{th}$: $V_{DS} \uparrow \Rightarrow I_D \uparrow$ (but eventually I_D saturates).
- For $V_{DS} > 0$ and $V_{GS} > V_{th}$: $V_{GS} \uparrow \Rightarrow I_D \uparrow$.

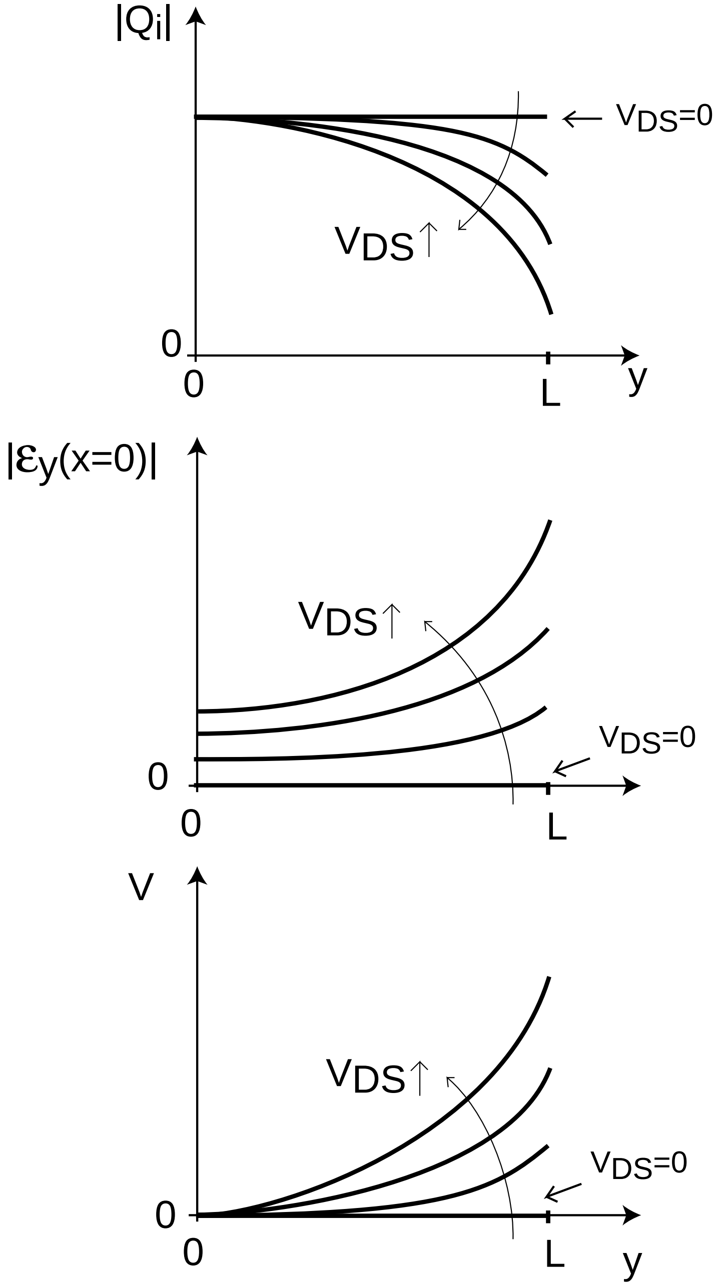


Along channel from source to drain:

$$V \uparrow \Rightarrow\ V_{GS} - V(y) - V_{th} \downarrow \Rightarrow\ |Q_i| \downarrow \Rightarrow\ |\mathcal{E}_y(x=0)| \uparrow$$

Local overdrive on gate reduced the closer to the drain.

Impact of V_{DS}:



As V_{DS} ↑ channel debiasing more prominent.

Problems with model as V_{DS} approaches $V_{GS} - V_{th}$.

Problems centered around $y = L$:

- Local gate overdrive goes to zero $\Rightarrow |Q_i| \rightarrow 0$. How can current be supported?
- Gradual-channel approximation becomes invalid.
- Sheet-charge approximation becomes invalid.
- Lateral field so large that linearity between field and velocity invalid.

Model that can handle V_{DS} values all the way up to $V_{GS} - V_{th}$ is rather complicated; but... actually, don't need new model!

Reason: when V_{DS} approaches $V_{GS} - V_{th}$, I_D changes very little due to prominent debiasing on the drain side of the channel.

Different question: how close can V_{DS} get to $V_{GS} - V_{th}$ before simple model fails?

Answer:

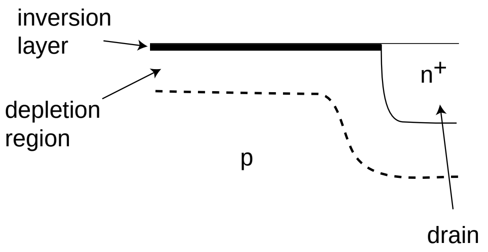
- up to about 80% of $V_{GS} - V_{th}$
- which means up to about 96% of I_{Dmax}.

Hence, simple model is pretty good up to $V_{DS} = V_{GS} - V_{th}$.

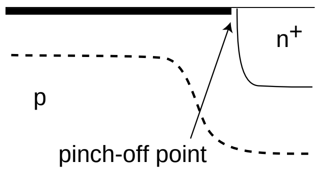
□ What happens if V_{DS} reaches or exceeds $V_{GS} - V_{th}$?

Electron concentration at $y = L$ drops to very small concentrations $\Rightarrow$ depletion region appears at $y = L$: *pinch-off*.

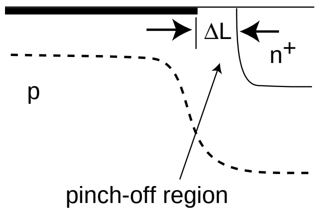
Depletion region is no barrier to electron flow: field "pulls" electrons into drain.



a) linear regime $V_{DS}<V_{DSsat}$



b) pinch-off $V_{DS}=V_{DSsat}$

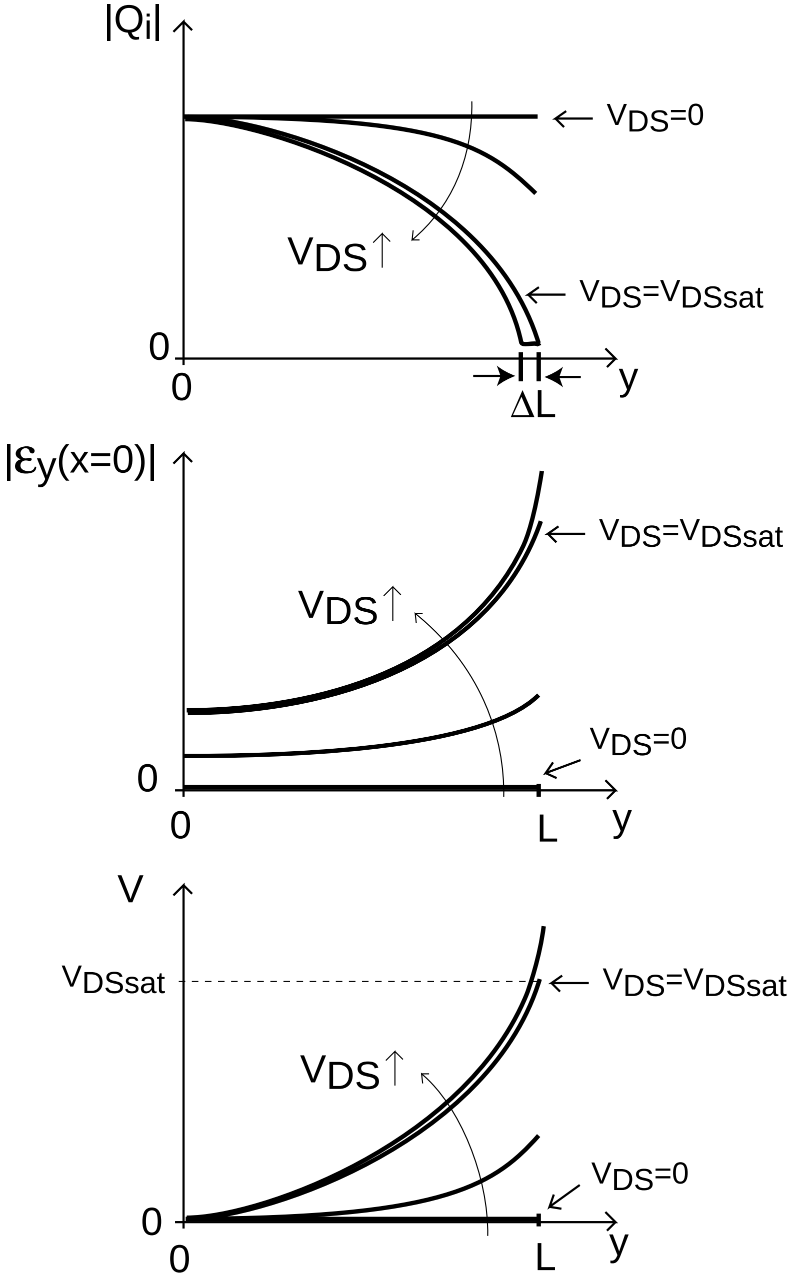


c) saturation regime $V_{DS}>V_{DSsat}$

As V_{DS} exceeds $V_{GS} - V_{th}$,

- depletion region widens into channel underneath gate;
- all extra voltage consumed in depletion region;
- electrostatics of channel, to first order, unperturbed;
- channel current unchanged $\Rightarrow$ MOSFET in *saturation*.

Lateral electrostatics in saturation:



Current model in saturation:

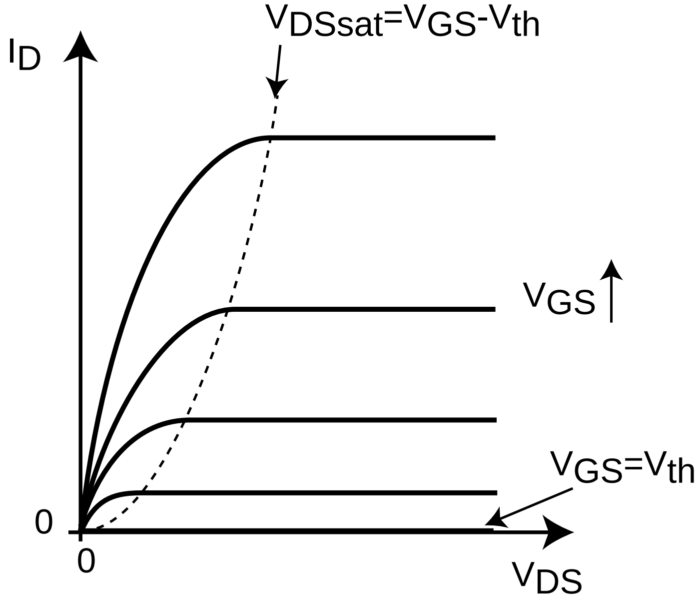
I_D does not increase passed $V_{DS} = V_{GS} - V_{th}$. Hence, I_{Dsat} is:

$$I_{Dsat} \simeq I_D(V_{DS} = V_{GS} - V_{th}) \simeq \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_{th})^2$$

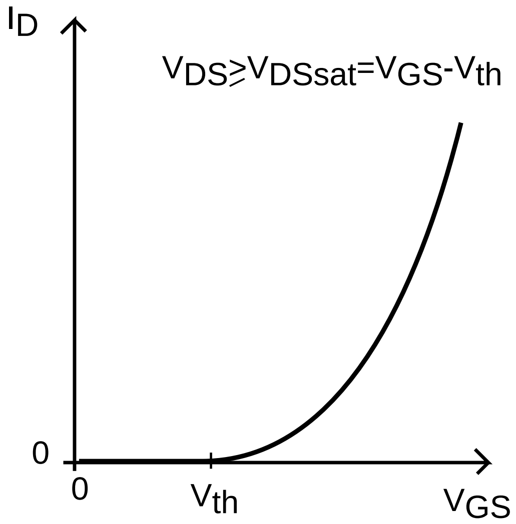
V_{DS} at which transistor saturates is denoted as V_{Dssat}:

$$V_{DSsat} = V_{GS} - V_{th}$$

Current-voltage characteristics:



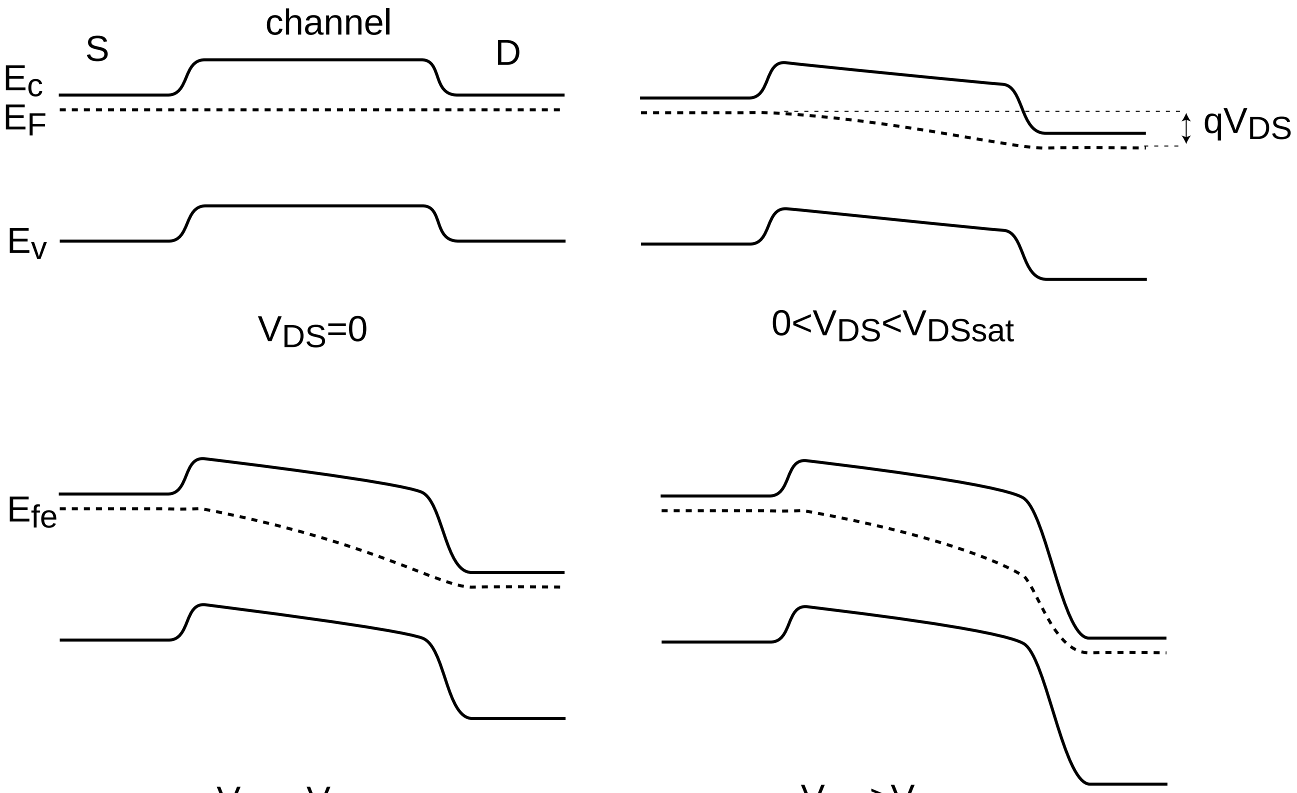
$$I_{Dsat} = \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_{th})^2$$



Why square dependence?

- $V_{GS} \uparrow \Rightarrow |Q_i| \uparrow$
- $V_{GS} \uparrow \Rightarrow V_{DSsat} \uparrow \Rightarrow$ higher lateral field in channel at saturation.

□ Energy band diagrams ($V_{GS} > V_{th}$):



$V_{DS}=0$

$0<V_{DS}<V_{DSsat}$

$V_{DS}=V_{DSsat}$

$V_{DS}>V_{DSsat}$

Pinch-off point: region of "free fall" of electrons.

Key conclusions

- In linear regime, I_D modulated by V_{GS} and V_{DS}:
  - V_{GS}, to first order, controlles electron concentration in channel
  - V_{DS}, to first order, controlles lateral electric field in channel
- MOSFET current in linear regime:

$$I_D = \frac{W}{L}\mu_e C_{ox}(V_{GS} - V_{th} - \frac{1}{2}V_{DS})V_{DS}$$

- In saturation regime, I_D modulated by V_{GS} but independent of V_{DS}:
  - V_{GS}, to first order, controlles both electron concentration in channel *and* lateral electric field in channel
  - V_{DS}, to first order, does not affect the lateral field in the channel due to *pinch-off*
- MOSFET current in saturation regime:

$$I_{Dsat} = \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_{th})^2$$

- Value of V_{DS} that saturates transistor:

$$V_{DSsat} = V_{GS} - V_{th}$$

Self study

- Validity of gradual-channel and sheet-charge approximations to inversion layer transport.