CAMERA-MICROCOMPUTER INTERFACE

by

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Chairman, Departmental Committee on Graduate Students

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in Electrical Engineering

ABSTRACT

A general interface was designed to receive an analog video signal from a Reticon solid state line scanner containing an array of 1728 photodiodes, process the signal, and pass it on to an SBC 80/20 single board computer via an Intel multibus. Processing on board the interface is controlled by the user via control words sent and received on the multibus. The user has a choice of eight CLOCK rates, three START pulses, sixteen quantizing levels (for analog to digital conversion), four modes of operation, and gate width and location. The four modes of operation make it possible to record video data in 4-bit digital form or in 1-bit digital form for each photodiode, or to record the addresses of the photodiodes where black/white transitions occur, or to record the string lengths of black data and of white data. The user also has a choice of three cameras from which to receive data.

The interface has been tested in all the different combinations of CLOCK, START, quantizing level, mode of operation, and gate width and location, and works well. Only one camera was used in the tests, but connections for the other two cameras were tested out.

Thesis Supervisor: Professor George C. Newton

Title: Professor of Electrical Engineering

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I. INTRODUCTION

Until recently, quality control of parts comprising an RCA picture tube was done by visual inspection. Now, however, in the interest of better and faster quality control during the manufacturing process, RCA is moving in the direction of greater mechanization. To this end, two systems have already been built and are in use - a matrix reader and a slit width reader. In development are a laser tab welder and a gun parts inspection system. These four systems have one thing in common - they each, at some point, process inputs to and outputs from a Reticon line scanning unit. Because of this common feature and because of the desire to have these systems under software control, it was proposed that a general interface be designed to connect the Reticon unit to an SBC 80/20, a single board computer, via an Intel multibus. This would make possible the conversion of much of the specialized hardware in each of the four systems to software and would allow the user much greater flexibility, as well as control. In fact, the user would be able to choose the CLOCK rate, the START signal, which of three cameras to use, the quantizing level (for generating 1-bit digital data), gate size and location, and one of four modes of operation, all of which will be explained later. Communication of control and command information between the SBC CPU (an 8080A single-chip 8-bit microprocessor located on the SBC 80/20 board) and the interface, and of scan data, scanner status, and interface status between the interface and the SBC CPU, would be via an Intel multibus. Input/output control would be in the form of control words and would be stored in special registers on the interface. The design and development of such an interface, to be used not only by the four above-mentioned systems, but also by future systems, was the proposed thesis project and is the subject of this paper.

This paper is divided into nine sections, this introduction being the first. Immediately following, in Sections II and III,

the two main characters, without whose contributions this project would never have been born, are introduced - the Reticon Unit and the SBC 80/20 single board computer. Enough is said about them so that in Section IV their go-between, the CAMERA-MICROCOMPUTER INTERFACE itself, can at last be presented, though, at this point, only in a general, block-diagram fashion. Finally, in Section V, the user is brought into the picture and shown how he can, with software, control the interactions among the three characters in this drama; he is also shown samples of the different kinds of outputs available to him.

Section VI (which really should be read before Section V) gets down to the nitty-gritty and gives a blow-by-blow description of the way the interface operates. Each subsection of Section VI deals with a subdivision of the interface circuitry and has associated with it a timing diagram of the same name. (For page numbers of the diagrams, see the List of Illustrations on page 4.) To fully understand Section VI, one may find helpful the accompanying Schematics, Board Layouts, and Cable Connections, and the Glossary, all of which are located in the Appendix, Section IX. The Glossary, which is helpful for understanding not only this section but the entire paper, lists most of the main signals (whose names appear in the text in all capital letters), along with their points of origin and functions, and a few abbreviations. Between Section VI and the Appendix are two other sections - Conclusions (Section VII) and References (Section VIII) - whose titles speak for themselves.

Now, before launching into the body of this paper, the reader should take note of the following points. (1) With a few exceptions, words in all capital letters are signal names and can be found in the Glossary. (2) Usually, but not always, signals having an overbar or a final "/" are negative true and signals without either an overbar or a final "/" positive true. (3) The overbar and final "/" are interchangeable - A21 and A21/ refer to the same signal.

II. THE RETICON UNIT

The Reticon unit, chosen for its high degree of linearity, as well as for the fact that it is a small, TTL-compatible solid-state unit with low power requirements, consists of a Reticon RL-1728H solid-state line scanner and an RC-100A series circuit; however, other Reticon systems could be used as well. The line scanner contains a row of 1728 silicon photodiodes on 15 um. centers. Each photodiode (see Fig. II-1) has its own storage capacitor, Cd, on which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit.

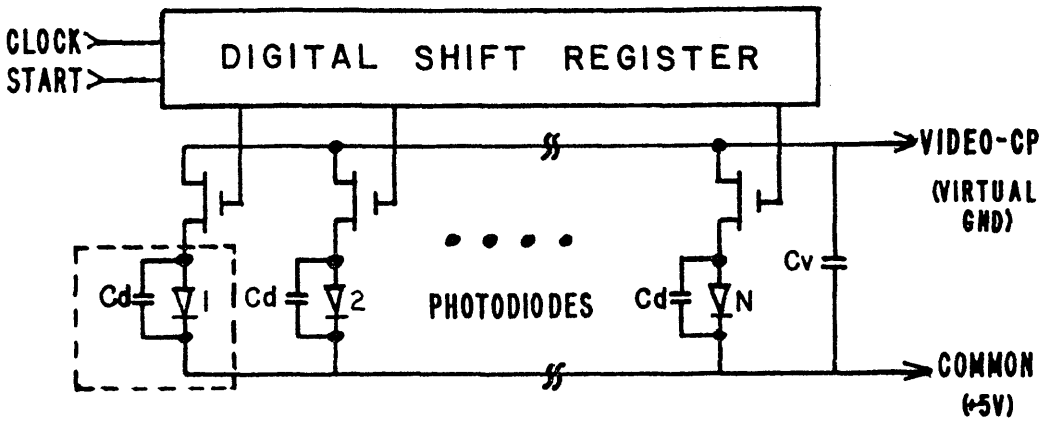


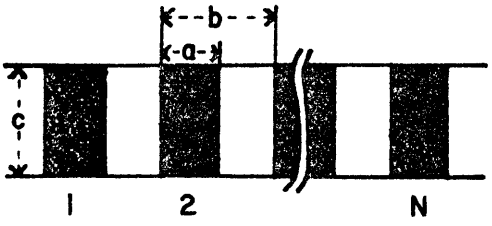
Fig. II-1 SIMPLIFIED SCHEMATIC OF RETICON LINE SCANNER

When the switch is turned on, once during each scan, the cell, which includes the photodiode and its parallel storage capacitor (dotted line delineates one cell), is charged to 5 volts (since the VIDEO-CP line is virtual ground), and approximately 1.8 pcoul. is stored on its capacitance. The switch is then turned off, and the charge on the capacitor is gradually removed by reverse

current flowing in the photodiode. This reverse current consists of dark leakage current, which at room temperature amounts to only about 1 pA and thus can be neglected, and photocurrent, which is proportional to the light intensity or irradiance. The amount of charge removed from the cell during line scan time is the product of the photocurrent and the line scan time. This amount of charge is replaced via the VIDEO-CP line, which is connected to an amplifier circuit (not shown), when the cell is sampled, one time per scan. All 1728 cells function the same way and are sampled one at a time in consecutive fashion at the CLOCK rate. Thus, since all 1728 cells are tied into the VIDEO-CP line, the VIDEO-CP output is a series of 1728 charge pulses each proportional to the light intensity on the corresponding photodiode.

The RL-1728H array also has a row of 1728 dark dummy diodes. Each dummy diode is sampled differentially with its corresponding photodiode so as to eliminate switching transients due to the multiplex switches and thus to improve the quality of the video signal.

The array geometry is as follows, with the darkened areas representing the bar-shaped photodiodes.



a = photodiode width = 7 um.
b = photodiode spacing = 15 um.
c = aperture width = 16 um.

Fig. II-2 RETICON PHOTODIODE ARRAY GEOMETRY

The entire aperture is photosensitive, so some light will fall between photodiodes. Photocurrent generated by such light will go

to the nearest diode. The spectral responsivity and uniformity of the RL-1728H line scanner are excellent for visible light, which is the type of light used. There is, however, a tradeoff between required light intensity and scanning speed.

One element influencing the choice of scanning speed is the presence of dark current, which is comprised of (1) integrated dark leakage current, (2) a fixed pattern due to incomplete cancellation of switching transients between sensing and dummy diodes, and (3) random pixel noise. (2) accounts for less than 0.5% of the saturated output signal for unprocessed video and (3) for less than 0.1% (depending on noise bandwidth and preamplifier used), but (1) is significant. Dark leakage current averages out to be about 0.5 pA per diode at room temperature and thus would yield the saturation output charge of 1.8 pcoul. in four seconds. If the line scan time were 40 ms., dark leakage current would contribute about 1% of the saturated output signal. Temperature also affects the dark current, causing it to double for every $7^{o}C$ rise in temperature, so at higher temperatures scanning times should be shorter. Looking at dynamic range, the saturated to dark current level ratio is 200:1, while the saturated to rms noise level ratio is 1000:1, for unprocessed video.

All drive and amplifier circuitry needed to operate the RL-1728H line scanner is contained on two printed circuit boards - an RC-100A motherboard, that contains clock and start pulse generators, a blanking circuit, a sample-and-hold circuit, and some buffer amplifiers; and an RC-108 array board, that contains a socket for the array (in this case, the RL-1728H line scanner, which is packaged in a 22-lead dual-in-line integrated circuits package with ground and polished optical windows), along with clock driver circuits, and a preamplifier. The RC-100A series circuit takes the VIDEO-CP output of the line scanner, which is a train of charge pulses, and converts it to a sampled-and-held boxcar video signal, put out on P2-N, with each sample being held for one CLOCK period.

The RC-100A motherboard contains an internal clock generator with frequency range depending on the selection of two capacitors and the particular frequency depending on the setting of a 50K pot. The range 300 KHZ to 2 MHZ was chosen, as it was the fastest and the only one including 500 KHZ and up. All other choices ranged from 300 KHZ down, too slow for most uses and covered anyway by other clocks generated by the interface. The RC-100A motherboard also provides for an external clock input, so the clocks generated on the interface can be used. The only constraint on the external clock is that it be an active high TTL pulse with a pulse width between 20 ns. min. and 200 us. max. This allows for square-wave clocks with frequencies ranging from 5 KHZ to 50 MHZ. However, as will be seen later, the interface can handle frequencies only as high as 576 KHZ. Thus all the internal and external clock choices ranging from 9 KHZ to 576 KHZ can be used. The only adjustment needed is the jumper connection to E1. To use the internal clock, one must jumper E1 to E2 and send the internal clock out on P2-C to the interface as RCLOCKx (x stands for the particular camera in use). To use the CLOCK from the interface, one must jumper E1 to E3 and receive CLOCK from the interface on P2-Z.

A similar situation exists for start pulses. The RC-100A motherboard has an internal start generator, but provides for an external start pulse to be sent in. For internal start generation, E5 would normally be jumpered to E4 and the three 4-bit rocker switches set to the count desired between start pulses; this count could be any number between 1736 (min. count is eight greater than the number of elements in the array) and 4096. Instead E5 is jumpered to E6, as for external operation, and E4 connected to P2-F, an unused edge connector, and then sent to the interface as RSTARTx (x being the number of the camera in use). With this arrangement, any count, up to 4096, can be put on the rocker switches. The minimum count of 1736, needed so that no start pulses can be sent while a scan is in progress, is no longer

a constraint because interface circuitry will not allow a START pulse to be generated except during the blanking period (the time between the last element of one scan and the first element of the next scan or, countwise, the count of the start pulse generator minus the number of elements in the array), when BLANK is high, and then only when the computer has finished its processing. (The BLANK signal, which is high during blanking time and low during scan time, is sent via P2-D to the interface.) One might, for example, set the count at a small number like 3, for the case where computer processing time varies considerably from scan to scan. This way a START pulse can be generated as soon as possible after processing is finished, whenever that happens to be, rather than having to wait the maximum amount amount of time likely to be needed for processing before sending another START pulse. For optimum operation, the count should be such that the scan time doesn't exceed 40 ms. - this is because dark current increases as integration time increases.

If an external start pulse is used, it must be an active high TTL pulse, with a minimum pulse width of one CLOCK pulse width plus 50 ns. and a maximum pulse width of less than one CLOCK period, synchronized with the negative-going edge of CLOCK, so that it envelopes one and only one positive transition of CLOCK, and sent to P2-A. In practice, a START pulse equal in width to one CLOCK period was used successfully.

III. THE SBC 80/20

The SBC 80/20, a single board computer made by Intel, is a complete computer system on a 6.75x12-inch printed circuit card that plugs into an Intel card cage. Included on the board are the CPU, system clock, read/write memory, non-volatile read-only memory, I/O ports and drivers, serial communications interface, interval timer, interrupt controller, and bus control logic and drivers. The 80/20 was selected for use with the interface because it was the standard system in use and because it was immediately available.

The CPU is an 8-bit n-channel MOS 8080A microprocessor with six 8-bit general purpose registers, addressable individually or in pairs, and an accumulator. The 8080A has a 16-bit program counter, so 64K bytes of memory can be addressed directly, and a 16-bit stack pointer to address an external last-in-first-out stack, locatable in any portion of memory. Finally, for interfacing memory or I/O, sixteen address and eight bi-directional data bus lines are provided.

Working with the 8080A control processor is an 8224 clock generator and an 8238 system controller. Together, these three generate address and control signals to access memory and I/O ports both on board and external to the SBC 80/20, respond to interrupts from on board or off, respond to WAIT requests from memory or I/O devices, fetch and execute 8080A instructions, and provide a stable timing reference for all other circuitry in the system.

Functioning of the bus is taken care of by a system bus interface, which includes a bus controller, an override flip-flop, bidirectional bus drivers, and circuits that generate the Bus Clock (BCLK/, P1-13) and Constant Clock (CCLK/, P1-31) signals. The bus controller arbitrates requests for use of the system bus, generates necessary I/O or memory command signals, gates addresses onto the address lines and data onto and off of

the data lines of the system bus, synchronously with respect to the Bus Clock.

As for memory, the SBC 80/20 has 2K 8-bit words of read/write memory, using Intel's 2113 static RAM'S, on board and sockets for up to 8K 8-bit words of non-volatile read-only memory. If 8708 EPROM'S and/or 8308 metal mask ROM'S, both Intel's and each adding 1K bytes of memory, are put in the four available sockets, only 4K 8-bit words of on-board read-only memory capacity can be provided. However, if 2716 EPROM'S or 8316 ROM'S, both Intel's but each adding 2K bytes, are used, then 8K 8-bit words of on-board read-only memory can be provided.

When the interface was built, an 80/20-4 was used instead of an 80/20. The 80/20-4 functions essentially the same way the 80/20 does, but it provides 4k 8-bit words of read/write memory by using Intel 2114 memories in place of the 2113's. There are other differences, but they won't be mentioned since they don't affect the functioning of the interface system.

The SBC 80/20 has two 8255 programmable peripheral interface devices providing 48 programmable parallel I/O lines; an 8251 USART (Universal Synchronous/Asynchronous Receiver/Transmitter), which is a programmable serial communications interface; and an 8253 interval timer, which can be programmed as a one-shot, as a rate generator, or as a square wave generator. None of these three features is utilized by the interface at the present time, but future applications of the interface may take advantage of them. The interface does, however, make use of the 8259 interrupt controller, which can be programmed to operate in any of four different modes.

The SBC 80/20 RAM can be assigned to any one of four 16K address blocks (within the 64K address space) and will reside at the end of the chosen block. The first block was chosen, arbitrarily, so RAM occupies locations 3000H-3FFFH. ROM/EPROM, on the other hand, always begins at memory location zero.

I/O port addressing includes the following dedicated ports:

D4 - Power Fail

D5 - System Bus Override

D6 - LED diagnostic indicator

D7 - (not used, but not available to the user)

D8-DB - 8259 Interrupt Controller

DC-DF - 8253 Interval Timer

E4-EB - Two 8255 Programmable Peripheral Interface Devices

EC-EF - 8251 USART

Other ports are available to the user for his own use.

IV. GENERAL OPERATION OF THE CAMERA-MICROCOMPUTER INTERFACE

While reading this section, the reader may wish to refer to the Block Diagram of the Camera-Microcomputer Interface, Fig. IV-1, on page 23 and to the Glossary on page 129. Discussion will start with CAM1, CAM2, and CAM3 (in the upper left-hand corner of Fig IV-1) and will trace the flow through to the SBC 80/20 along the right edge.

CAM1, CAM2, and CAM3 represent three separate Reticon camera units, all connected to the interface board. The Camera Director, under software control via a status register, broadcasts the START and CLOCK pulses to all three cameras, but allows onto the interface only the four outputs (VIDx, BLANKx, RSTARTx, and RCLOCKx, where x is the chosen CAM's number) of one Reticon camera. That's the ideal situation. In actuality, however, two or three cameras could have their outputs enabled at the same time. Since the corresponding outputs from the three cameras are wired together once they pass through the enabling switches, the four signals - VIDEO, BLANK, RSTART, and RCLOCK - are invalid if more than one camera's outputs are enabled. If, on the other hand, no camera's outputs are enabled, as is the case during initialization procedures, there is no problem - none of the four signals is generated.

The CLOCK signal sent out to the three cameras is the output of the Clocks Generator and CLOCK Selector, which takes the 9.216 MHZ Clock (CCLK/, P1-31) from the multibus and divides it down to make available seven clock rates - 576 KHZ, 288 KHZ, 144 KHZ, 72 KHZ, 36 KHZ, 18 KHZ, and 9 KHZ. In addition to these, RCLOCK, the Clock signal coming from the designated camera, is also available, so the user has eight clocks from which to choose. This is enough to accommodate the existing systems - the matrix reader, slit width reader, and gun parts inspection system require pixel rates of at least 500 KHZ, so the 576 KHZ rate will take care of them; the laser tab welder is happy with the 144 KHZ rate. The chosen

CLOCK signal, a TTL signal, is an inverted, delayed, level-shifted version of the CMOS signal ØB. Both CLOCK and ØB are sent to the Control Logic area of the interface.

The START signal sent to the three cameras and also to the Control Logic area is the output of the PRESTART Selector and START Generator. The PRESTART Selector chooses among three START pulses - RSTART, which comes from the chosen camera, COMP.START, and 60 HZ START. COMP.START is generated by the COMP.START Generator whenever a CPSTART signal is sent to the interface by the computer. The 60 HZ START Generator, on the other hand, uses the line voltage to generate a signal, 60 HZ START, every 8.33 ms. (i.e., at a rate of 120 HZ).

Two other signals coming from the chosen camera are BLANK and VIDEO. BLANK goes low just before the first piece of VIDEO data arrives at the interface and high just after the last piece of VIDEO arrives, so it signals the beginning and end of the scanning period. VIDEO is the signal of interest and is the one processed by the interface.

VIDEO passes, first of all, through an AGC (automatic gain control) circuit that adjusts its swings so that it comes out as ANALOG VID with a 0-+1 volt swing. In this form it is accepted by a 4-Bit A/D Converter that converts it from a 0-+1 volt analog signal to a 4-bit digital signal, 4-bit Data. If the user has chosen A/D mode (meaning that he wants gray level data), then this 4-bit Data will be stored in one of the four 4-Bit 3-State Latches. 4-bit Data for each photodiode is stored in a different latch, and every time all four latches have received new data, i.e., every fourth CLOCK period, these sixteen bits of new data are stored in memory as A/D Data.

4-bit Data coming out of the 4-Bit A/D Converter is also sent to the 4-Bit Magnitude Comparator and Latch. The comparator compares the 4-bit Data to a 4-bit quantizing level chosen by the user and yields a 1-bit digital value that gets latched as DIG VID. If the user desires a 1-bit digital video value for each

photodiode, in which case he will have designated PIXEL mode, then DIG VID will be shifted into the 16-Bit Shift-and-Store Register. Every time sixteen DIG VID values (corresponding to sixteen consecutive photodiodes) have been shifted into the register and stored there, these sixteen bits will be taken and stored in memory as PIXEL Data. Thus PIXEL Data gets stored in memory every sixteen CLOCK periods.

DIG VID also passes into a TRANSITION Detector and Control unit, which monitors the DIG VID signal and signals a change of state, i.e., a transition. If TRAN mode has been chosen, the arrival of a transition will cause the address (held in the STR.L or TRAN counters) of the first photodiode after last photodiode in a string of photodiodes of the same state, along with information indicating which camera and which memory were in use and the state of the video signal of the just-completed group of photodiodes, to be stored in four 4-Bit 3-State Latches. These sixteen bits of TRAN Data will then be transferred to memory during the same CLOCK period in which the transition was detected.

STR.L mode operates in the same way that TRAN mode does, except that instead of storing the address of the last photodiode in a group it stores the number of photodiodes in the group and then resets the STR.L or TRAN counters to zero, so they are ready to start counting for the next group. The counters are reset during the same CLOCK period as the occurrence of TRANSITION so that if a transition occurs during the next CLOCK period the counter will be set to 1. This makes it possible to give accurate string lengths even when a transition occurs every CLOCK period.

Now that we've seen how the four data modes are generated, let's compare their relative advantages. Note that sixteen data bits can hold PIXEL Data for sixteen photodiodes, A/D Data for four photodiodes, TRAN Data for one transition, or STR.L Data for one string. Thus, if the digital video signal were one that changed state every CLOCK period, it would take sixteen times as much space to record this in TRAN mode or in STR.L mode as in

PIXEL mode. If, on the other hand, the digital video signal were to change state less frequently than every sixteen CLOCK periods, it would take less space to record TRAN or STR.L Data than to record PIXEL Data. Thus, for digital data that changes state frequently, PIXEL mode is more economical, spacewise, whereas for digital data that changes state infrequently, either TRAN mode or STR.L mode is more economical. Data in any of these three modes can be converted into either of the other two forms. A/D mode however, is different - it stands alone as the only provider of gray-level data, providing, as it were, sixteen gray levels, and is useful when one wishes to see fine detail. The fact that A/D Data can be converted to any of the other three forms of data but can't be derived from them makes it, perhaps, the most useful single data mode.

The sixteen bits of data for A/D mode, for PIXEL mode, and for TRAN or STR.L mode are wired together and to the inputs of the appropriate memories. For proper operation only one of the four modes can have its selector bit in the status register high. There is no protection against the user's setting more than one of these mode selector bits high causing confusion not only on the sixteen data lines, but also elsewhere in the interface circuitry. On the other hand, the user might set none of the four mode selector bits high, in which case the sixteen data lines would remain at high impedance and no new data would be stored in interface memory.

The interface memory just mentioned actually consists of two sets of memories - the "A" Memories and the "B" Memories. During any one scan/process period, one of these sets of memories is having scan data (in one of its four forms) written into it while the other set of memories is having data that was written into it during the previous scan, read into the computer. Coordinating all of this are two sets of controls, the Memory Write Controls, which generate memory addresses, write pulses, and chip selects for the write cycle; and the Memory Read Controls, which generate

memory addresses, read signals, and chip selects for the read cycle. At the beginning of each scan/process period the memories switch roles so that during that scan/process period the memories that were written into during the last period will be read from and the memories that were read from during the last period will be written into. The Mux directs signals from the Memory Read Controls and the Memory Write Controls to the proper memories for each scan/process period.

When the computer wants to read from the interface memories, it executes an IN 86H command, i.e., it puts the number 86H (Hexadecimal) on the address bus. The Address Decoder decodes this address and sends it to the Control Logic area, which receives an I/O Read Command (IORC/, P1-21) from the bus controls at about the same time. The Control Logic sets the Memory Read Controls into action and also enables the Transceivers to receive data from the memories and to pass it on to the data bus. The Transceivers also receive data from two status registers, which are read by an IN 88H command. At any one time it is only possible for one pair of memories or one status register to have its outputs enabled; all the rest will have their outputs disabled, so there can't be contention on the data bus lines.

When the computer wishes to send control information or commands to the interface, it does so by executing an OUT command. Five registers must receive control information from the computer before the first scan begins in order for the system to function properly. The five registers and the control information they hold are:

Register 0 - CLOCK and START Selector bits
Register 1 - 4-bit Quantizing Level and
4 Mode Selector bits
Register 2 - 8-bit Start Gate
Register 3 - 8-bit End Gate
Register 5 - Camera Selector bits

(The Register number corresponds to the second digit of the output port that must be addressed in order to load that register, the first digit being the arbitrarily chosen base address of 8. Thus to load Register 0, for example, an OUT 80H command must be executed; for Register 1, an OUT 81H, etc.)

The choices available to Registers 0, 1, and 5 have already been discussed. Register 2 contains an 8-bit Start Gate, corresponding to the upper 8 bits of the 12-bit photodiode address of the first photodiode whose video information is of interest to the user. Similarly, the End Gate (in Register 3) corresponds to the upper 8 bits of the 12-bit photodiode address of the last photodiode of interest. Because the Start Gate and End Gate deal with only the upper 8 bits of the 12-bit address, the Gate area will always be a multiple of 16. Thus there won't be any A/D or PIXEL Data left dangling when the last 16 bits of data are stored in memory.

The Photodiode Address Counters feed into the Start Gate and End Gate Detectors (as can be seen on the Block Diagram), which feed their results into the PREGATE Detector and GATE's Generator. PREGATE marks the GATE area; it remains high as long as the upper eight bits of the the photodiode address contain a number larger than the Start Gate and smaller than the End Gate. The GATE's Generator synchronizes PREGATE to CLOCK and generates four GATE's that follow PREGATE on the first, second, third, and fourth CLOCK pulses thereafter. These GATE's are used to synchronize the Memory Write Controls so that a given piece of video data is matched up with the correct photodiode address.

At this point, a few words should be said about the amount of data that can be stored for each of the four modes of operation. As mentioned before, during one scan four memories, either the "A" Memories or the "B" Memories, are used for recording scan data. Since each memory has space for storing 255 4-bit words (location 0 is not used), 255 16-bit words may be stored for one scan. This means that in PIXEL mode the memories can store a 1-bit digital

video value for 255 x 16 or 4080 photodiodes. Since the array has only 1728 photodiodes, the whole scan may be stored in PIXEL form. For A/D mode, each group of sixteen bits stored at one memory address records a 4-bit digital value for each of four photodiodes. Thus the memories can store A/D Data for only 1020 photodiodes. Consequently, to operate in A/D mode one must designate a Gate area of 1020 photodiodes or less, or else be happy with A/D Data for the first 1020 photodiodes starting from the Start Gate address plus 17, as we shall see later. TRAN and STR.L modes both use all sixteen data bits at one memory address to store information about one transition. Thus, in either of these modes the memories can store information about 255 transitions or 255 photodiode groups.

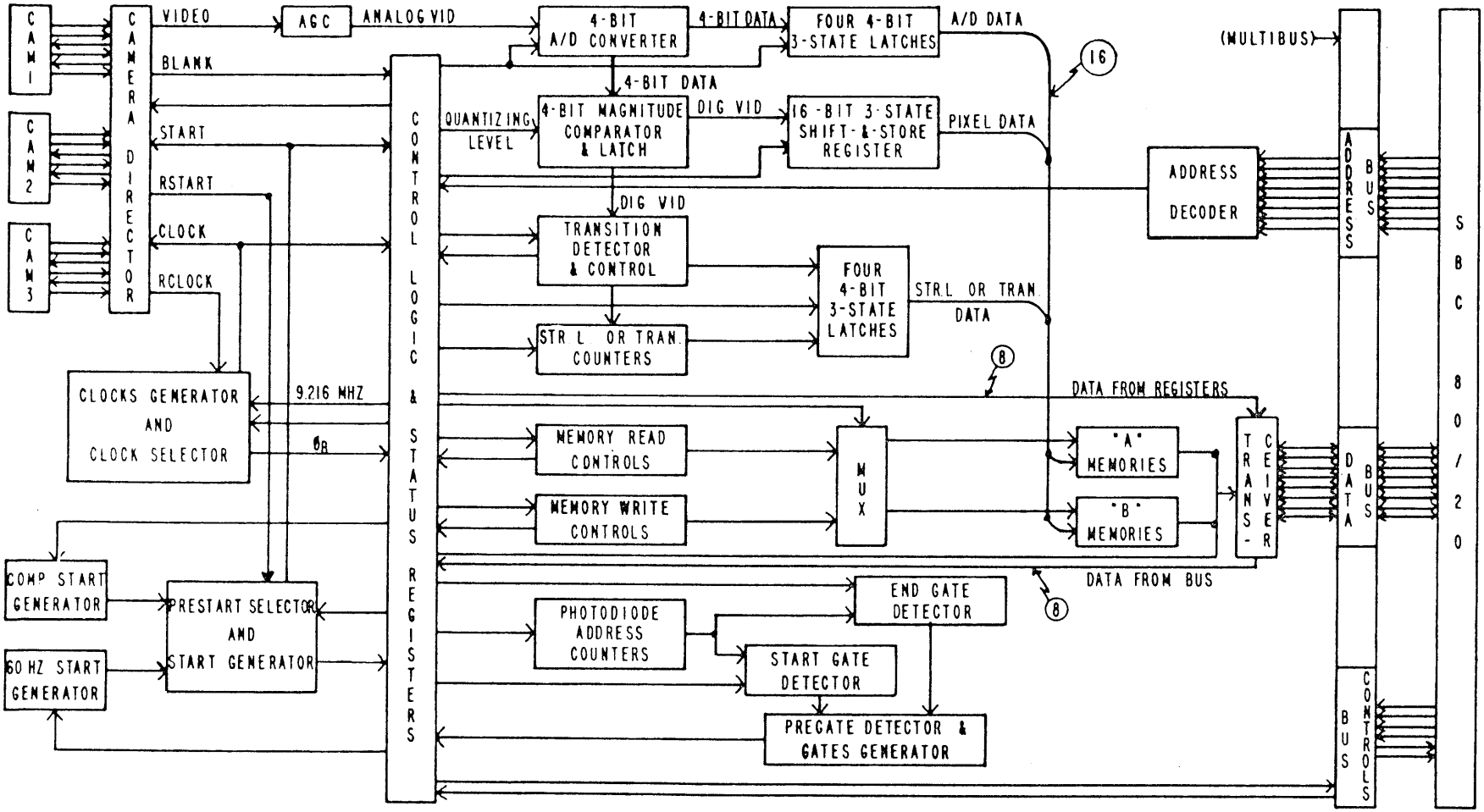


FIG IV-1 CAMERA-MICROCOMPUTER INTERFACE --- BLOCK DIAGRAM

V. SOFTWARE CONTROL

Software control will be explained by referring to Fig. V-1 (pages 29 and 30), one of the programs used to check out the system. During the discussion reference will be made to several signals generated by the computer and/or by interface. These signals are described in the Glossary (starting on page 129). Those signals generated by the computer are listed, along with their corresponding Port addresses, L41 outputs (see page 123), and functions, in Fig. V-4 on page 32. (For best understanding, one should read Section VI before Section V.)

The program shown in Fig V-1 initializes the interface boards, fills the SBC 80/20 memory locations 3000H-31FFH with "BB," and then sets scanning and processing in motion. While scanning is in progress, storing data in one set of interface memories, the computer reads the data that was loaded into the other set of interface memories during the previous scan into the SBC 80/20 memory starting at location 3000H. When scanning and processing are both completed, locations 3000H-31FFH are reloaded with "BB"'s and another scan/process period begins. Scanning and processing continue until the interrupt switch is depressed, at which point the user may display the contents of the SBC 80/20 memory locations 3000H-31FFH to see the most recent data. (Sample outputs are shown in Fig. V-6, pages 34 through 51.)

On lines 16 and 17, the interrupt mask is set to enable interrupts 1 and 4. Interrupt 1 is the manual switch interrupt, and interrupt 4 the signal indicating that data in the desired GATE area has been processed and recorded in interface memory. Any time after the arrival of an interrupt request, the computer may send a PROC.COMP. signal to switch the memories and to start processing the data that was just stored in the interface memories. The scan during which that data was stored may not yet be finished, but this isn't a problem since no more data can be written into the interface memories, once the gate has been closed

and interrupt 4 sent, until the gate opens again during the next scan. The next scan can't begin, however, until the present scan is finished because the generation of the START pulse to start the next scan can occur only when BLANK is high (i.e., after scanning is finished - BLANK goes high at the end of a scan and stays high until the next scan begins), unless a PREBLANK signal, to be explained later, is sent by the computer.

To initialize the interface boards, the computer, first of all, sends out a RESET signal. RESET sends an interrupt 4 request; sets PC and PCSYNC low blocking the generation of any START pulses; sets COMP.START low; loads the photodiode address counters with zeros in preparation for scanning; resets all the GATE's low and all the GATE/'s high, also in preparation for scanning; resets the outputs of Control Status Registers 0, 1, and 5 low, blocking the selection of the camera, of the start pulse, of the quantizing level, and of the mode of operation; resets 43SEL, 21SEL, and MEMA low; and disables the counter generating PIXAD. With all Mode Selector bits low, no writing operations can take place, and with 43SEL and 21SEL low, no read operations can take place. Thus, RESET disables read and write operations, while preparing various counters and flip-flops for the start of another scan. The 576 KHZ clock, by the way, is selected by default when RESET is sent.

Lines 19-28 hold the instructions for loading the five Status Control Registers - 0, 1, 2, 3, and 5, which must all be loaded at this time, though the order in which they are loaded doesn't matter. The bit configurations for these registers are shown in Fig. V-2 ("-" means don't care), page 31.

Starting with Register 0, F2, F1, and F0 comprise a 3-bit binary number, which selects the CLOCK. (CLOCK selections are shown in Fig.V-3, page 31.) S3, S2, and S1 - also in Status Control Register 0 - are the Start Selector bits. S3 selects COMP.START, a computer-generated start signal; S2 selects RSTART, the internal Reticon start signal; S1 selects 60 HZ START, a start

signal generated from the line voltage. One and only one of these three bits must be set high. If none is set high, no START pulse can be generated. On the other hand, if more than one is set high, meaning more than one switch feeding the same output line (STCMOS) is closed, there will be confusion on this line, which is sent to generate the START pulse.

In Register 1, Q3, Q2, Q1, and Q0 constitute a 4-bit binary number that selects one of sixteen quantizing levels for the conversion of the 4-bit digital video value to a 1-bit digital video value. The range of voltages corresponding to each quantizing level is shown in Fig. V-5, page 33.

The other four bits in Register 1 - - PIXEL, A/D, TRAN, and STR.L - are the Mode Selector bits for the modes of the same names. As with the Start Selector bits, one and only one of these mode selector bits must be set high. If none is set high, no data will be written into the interface memories. If more than one is set high, various strange things, all undesirable, will happen, what exactly, depending on which specific bits were set high.

Registers 2 and 3 hold the 8-bit Start Gate and End Gate addresses delineating the GATE, or window, area for the data. These addresses actually correspond to the upper eight bits of the 12-bit photodiode address, so the GATE area will always be a multiple of sixteen, as mentioned before.

In Register 5, CAM3, CAM2, and CAM1 are the Camera Selector bits. As with the Start and Mode Selector bits, one and only one of these three Camera Selector bits must be set high. The other 5 bits of Register 5 are no longer being used.

Continuing on with the program now that the interface boards are ready for action, a PREBLANK signal is sent (Line 29) to make possible the generation of a Start signal, by setting BLANK GATE high, just in case the BLANK signal powered up low. Next, interrupts are disabled (line 30) while a Gate Complete test byte (GC) is reset to 0 (Lines 31 and 32), while the SBC 80/20 memory locations 3000H-31FFH are loaded with "BB" (Lines 33-46), while

PROC.COMP./ and CPSTART are sent to the interface (Lines 47 and 48), and while interrupt 1 is disabled leaving only interrupt 4 enabled. The PROC.COMP./ signal does the resetting and setting that must be done between scans to prepare for a new scan. It loads the photodiode address counters with zeros, switches the memories, clears all four memory address counters to zero, removes the interrupt 4 request, and sets PC high. The next CLOCK pulse sets PCSYNC high, so, since GATE4/ and BLANK GATE are already high, all is ready to generate a START pulse. CPSTART (Line 48) is sent to the interface, and if COMP.START has been selected, then a START pulse will be generated. If not, a START pulse will be generated when the selected start pulse (either RSTART or 60 HZ START) is generated. Interrupt 1 is disabled (lines 49 and 50) at this time so that a scan can't be interrupted while the gate is still open, i.e., while write operations are still going on. Interrupt 4, only, is enabled.

The first step in the processing of the previous scan is the sending of an OUTRAN signal to the interface (line 56) to read from a status register the last memory address written into during the previous scan. The instructions on Lines 57-59 send this number out to the terminal using a Monitor routine called NMOUT. Since the computer now knows how many interface memory locations it needs to read, it proceeds to do so by executing the instructions (lines 60-72) for bringing the data from interface memory via port 86H to SBC 80/20 memory starting at location 3000H. Port 86H is read twice for each interface memory location filled because the multibus has only eight data lines and thus can bring in only eight of the sixteen data bits stored at a given memory location at one time. When all the interface memory locations written into during the previous scan have been read, a READ COMP./ signal (line 73) is sent to set 43SEL (which is already low) and 21SEL to 0 to assure that the memories just read from are disabled from being read from or written into anymore during that scan/process period.

At this point, computer processing is finished, so interrupts are disabled and the Gate Complete test byte (GC) checked (lines 74-77). If GC has been set to FF, meaning the writing of scan data into interface memories has been completed, then the computer will jump to NEXT, line 30, to prepare for the next scan. Preparations include resetting GC to zero, reloading SBC 80/20 memory locations 3000H-31FFH with "BB" and sending PROC COMP. to set the photodiode address counters to 0, switch the memories, clear all memory address counters to 0, remove the interrupt 4 request, and set PC high. By this time GATE4/ will be high (it went high one CLOCK after INT4/ was sent), so if BLANK GATE is high (meaning BLANK has gone high indicating the end of a scan), then a START signal will be generated when the next CPSTART, RSTART, or 60 HZ START is generated, depending on which Start Selector bit is set.

If the check on line 76 shows GC has not been set to FF, then interrupts 1 and 4 are enabled (lines 78-80). (This point is chosen for user interrupts because at this time the computer has finished reading data from the interface memories into its on-board memories, so the data in SBC memory locations 3000H-31FFH is the data from one scan. Had interrupt 1 been enabled all along, the sending of interrupt 1 could have occurred at any time, in which case the user couldn't have predicted whether he'd find data or "BB" or some combination of the two in locations 3000H-31FFH.) If no interrupt 1 has been sent, then interrupt 4 will cause the computer to jump to NEXT (line 30) and proceed as described above.

After PROC.COMP. has been sent (line 47), 618 computer clock cycles elapse before GC is checked on line 76. Since the monitor routine NMOUT called on line 59 takes 425 cycles and since one cycle lasts around 465 ns., this amounts to a lapse of .28 ms. Using the slowest CLOCK, 9 KHZ, which has a period of 111 us., it takes .19 seconds to complete the scan (of 1728 photodiodes). Using the 576 KHZ CLOCK, 1.736 us. per period, a scan takes about

3 ms. Depending on the gate size, interrupt 4 may or may not have arrived by the time GC is checked.

CPSTART signals, in the worst case, (i.e., when interrupt 4 arrives before GC is tested on line 76, in which case there is no waiting for interrupt 4 and no enabling of interrupt 1) occur about 4 ms. apart. If a slow CLOCK, such as 9 KHZ, and a narrow GATE were used, CPSTART (line 48) would be sent while a scan was still in progress. Since BLANK is low during scan time, BLANK GATE (which follows it except when PREBLANK is sent) would also be low, blocking the generation of a START pulse from CPSTART. The computer would continue on to line 76, discover that GC was still 0 and then halt waiting for either interrupt 1 or interrupt 4. The latter would never occur if COMP.START had been chosen, however, because CPSTART generates COMP.START only once per scan/process period and it would have done so while BLANK was still low. To obviate this type of problem it is necessary to add to the interface either an interrupt generated by the rising edge of the BLANK signal or else a BLANK status bit, as in a control register, that could be sampled by the computer to determine when to send a CPSTART signal. This problem doesn't arrise with RSTART or 60 HZ START because these signals are periodically generated in a continuous fashion.

No processing of the data moved to SBC 80/20 memory is done by the computer in this program. Anyone using the interface, however, would presumably wish to do some processing. Instructions of this nature would be inserted between lines 73, when reading is complete, and line 74. Also included somewhere between the arrival of interrupt 4 and the sending of PROC.COMP. would be any instructions to change the contents of the Status Control Registers 0, 1, 2, 3, and 5. These registers may be changed while scanning is still in progress, as long as the GATE area has been passed (signaled by the arrival of interrupt 4), after which no more data from that scan will be written into interface memory.

FIG. V-1 TEST PROGRAM

```
ASM80 :F1:TEST.ASM MACROFILE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  LOC  OBJ          LINE        SOURCE STATEMENT

                      1 ;
                      2 ;
                      3 TEST:
                      4 ;
  0520                5 NMOUT   EQU     0520H
                      6 ;
                      7         ASEG
  3900                8         ORG 3900H
                      9 ;
  3900 F3            10         DI
  3901 3E20          11         MVI A,20H        ;SEND OCW2 TO 8259 -
  3903 D3D8          12         OUT 0D8H         ;   NON-SPECIFIC EOI
  3905 310033        13         LXI SP,3300H     ;SET STACK POINTER AT 3300
  3908 219039        14         LXI H,INT4       ;VECTOR INT4
  390B 22F13F        15         SHLD 3FF1H       ;   TO 3990
  390E 3EED          16         MVI A,0EDH       ;SEND INTERRUPT MASK TO
  3910 D3D9          17         OUT 0D9H         ;   ENABLE INTERRUPTS 1 AND 4
  3912 D38A          18         OUT 8AH          ;SEND RESET TO INTERFACE
  3914 3E04          19         MVI A,04H        ;SEND CLOCK AND START
  3916 D380          20         OUT 80H          ;   SELECTIONS TO INTERFACE
  3918 3E00          21         MVI A,0H         ;SEND START GATE
  391A D382          22         OUT 82H          ;   TO INTERFACE
  391C 3E6C          23         MVI A,6CH        ;SEND END GATE
  391E D383          24         OUT 83H          ;   TO INTERFACE
  3920 3E20          25         MVI A,20H        ;SEND CAMERA SELECTION
  3922 D385          26         OUT 85H          ;   TO INTERFACE
  3924 3E88          27         MVI A,88H        ;SEND QUANTIZING LEVEL AND
  3926 D381          28         OUT 81H          ;   MODE TO INTERFACE
  3928 D38C          29         OUT 8CH          ;SEND PREBLANK TO INTERFACE
  392A F3            30 NEXT:  DI
  392B 3E00          31         MVI A,0H         ;RESET GATE COMPLETE TEST
  392D 32FF38        32         STA 38FFH        ;   BYTE TO ZERO
  3930 11FF01        33         LXI D,01FFH      ;DE GETS NUMBER OF MEMORY
                     34 ;                           LOCATIONS TO BE FILLED
  3933 210030        35         LXI H,3000H      ;HL GETS STARTING ADDRESS OF
                     36 ;                           MEMORY TO BE FILLED
  3936 36BB          37 LOOP1:  MVI M,0BBH       ;"BB" WILL BE STORED IN MEMORY
  3938 3E00          38         MVI A,0H
  393A 23            39         INX H            ;INCREMENT MEMORY ADDRESS
  393B 1B            40         DCX D            ;DECREMENT COUNTER
  393C BA            41         CMP D            ;IF REGISTER D IS NOT 0
  393D C23639        42         JNZ LOOP1        ;   JUMP TO LOOP1
  3940 BB            43         CMP E            ;IF REGISTER E IS NOT 0
  3941 C23639        44         JNZ LOOP1        ;   THEN REQUIRED NUMBER OF
                     45 ;                           MEMORY LOCATIONS HAVEN'T YET
                     46 ;                           BEEN FILLED, SO JUMP TO LOOP1
  3944 D387          47         OUT 87H          ;SEND PROC. COMP.  TO INTERFACE
  3946 D389          48         OUT 89H          ;SEND CPSTART TO INTERFACE
  3948 3EEF          49         MVI A,0EFH       ;ENABLE INTERRUPT 4 ONLY
  394A D3D9          50         OUT 0D9H
  394C 3E88          51         MVI A,88H
  394E D381          52         OUT 81H
  3950 3E20          53         MVI A,20H        ;SEND NON-SPECIFIC EOI
  3952 D3D8          54         OUT 0D8H         ;   TO 8259
```

```
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  LOC  OBJ          LINE        SOURCE STATEMENT

  3954 FB             55          EI
  3955 DB88           56          IN 88H            ;SEND OUTRAN TO INTERFACE
  3957 67             57          MOV H,A           ;PUT NUMBER OF MEMORY LOCATIONS
                      58 ;                             TO BE READ FROM IN REGISTER H
  3958 CD2005         59          CALL NMOUT        ;OUTPUT THIS NUMBER TO TERMINAL
  395B 110030         60          LXI D,3000H       ;1ST ADDRESS TO WHICH DATA FROM
                      61 ;                             INTERFACE WILL BE MOVED
  395E DB86           62 LOOP:    IN 86H            ;READ PORT 86
  3960 12             63          STAX D            ;STORE THIS DATA AT ADDRESS
                      64 ;                             HELD IN REGISTERS D AND E
  3961 13             65          INX D             ;INCREMENT MEMORY ADDRESS
  3962 DB86           66          IN 86H            ;READ PORT 86 AGAIN
  3964 12             67          STAX D            ;STORE THIS DATA AT ADDRESS
                      68 ;                             HELD IN REGISTERS D AND E
  3965 13             69          INX D             ;INCREMENT MEMORY ADDRESS
  3966 25             70          DCR H             ;DECREMENT NUMBER OF INTERFACE
                      71 ;                             MEMORY ADDRESSES NOT YET READ
  3967 C25E39         72          JNZ LOOP          ;   AND JUMP TO LOOP IF NOT 0
  396A D38B           73          OUT 8BH           ;SEND READ COMP TO INTERFACE
  396C F3             74          DI                ;DISABLE INTERRUPTS
  396D 3AFF38         75          LDA 38FFH         ;CHECK GATE COMPLETE TEST BYTE -
  3970 FEFF           76          CPI 0FFH          ;   IF SET TO FF, JUMP
  3972 CA2A39         77          JZ  NEXT          ;   TO NEXT
  3975 3EED           78          MVI A,0EDH        ;ENABLE INTERRUPTS 1 AND 4
  3977 D3D9           79          OUT 0D9H
  3979 FB             80          EI                ;ENABLE INTERRUPTS
  397A 76             81          HLT               ;WAIT FOR INTERRUPT
  397B C32A39         82          JMP NEXT          ;   THEN JUMP TO NEXT
                      83 ;
                      84 ;
                      85 ;
                      86 ;
  3990                87          ORG 3990H
                      88 ;
                      89 ;
  3990 C5             90 INT4:    PUSH B            ;PUSH CONTENTS
  3991 D5             91          PUSH D            ;   OF REGISTERS
  3992 E5             92          PUSH H            ;   ONTO STACK
  3993 F5             93          PUSH PSW
  3994 3EFF           94          MVI A,0FFH        ;SET GATE COMPLETE
  3996 32FF38         95          STA 38FFH         ;   TEST BYTE TO FF
  3999 F1             96          POP PSW           ;POP STORED
  399A E1             97          POP H             ;   REGISTER CONTENTS
  399B D1             98          POP D             ;   FROM STACK BACK INTO
  399C C1             99          POP B             ;   PROPER REGISTERS
  399D C9            100          RET               ;RETURN TO PROGRAM
                     101 ;
                     102 ;
  0000               103          END TEST
```

FIG. V-2 STATUS CONTROL REGISTERS (SCR) AND THEIR CONTENTS

SCR	7 2^7	6 2^6	5 2^5	4 2^4	3 2^3	2 2^2	1 2^1	0 2^0
0	F2	F1	F0	S3 COMP. START	S2 RSTART	S1 60 HZ START	-	-
1	Q3	Q2	Q1	Q0	PIXEL	A/D	TRAN	STR.L
2	L7	L6	L5	L4	L3	L2	L1	L0
3	H7	H6	H5	H4	H3	H2	H1	H0
5	CAM3	CAM2	CAM1	-	-	-	-	-

FIG. V-3 CLOCK SELECTIONS

F2	F1	F0	DECIMAL	CLOCK SELECTED
0	0	0	0	576 KHZ
0	0	1	1	288 KHZ
0	1	0	2	144 KHZ
0	1	1	3	72 KHZ
1	0	0	4	36 KHZ
1	0	1	5	18 KHZ
1	1	0	6	9 KHZ
1	1	1	7	RCLOCK

FIG. V-4 PORT ADDRESSES USED AND THEIR FUNCTIONS

PORT ADDRESS	L41 OUTPUT ENABLED	SIGNAL GENERATED	FUNCTION
80H	0	STROBE0	Loads SCR* 0 (U37) with CLOCK and START selections
81H	1	STROBE1	Loads SCR 1 (U9) with QUANTIZING LEVEL and MODE selections
82H	2	STROBE2	Loads SCR 2 (U39) with START GATE address
83H	3	STROBE3	Loads SCR 3 (U38) with END GATE address
85H	5	STROBE5	Loads SCR 5 (U13) with CAMERA selection
86H	6	MACR	Reads Interface memory
87H	7	PROC.COMP.	Prepares Interface for new scan
88H	8	OUTRAN	Reads SCR 8 (L47) or 9 (L48) to find number of Interface memory addresses filled during previous scan
89H	9	CPSTART	Sends a signal to Interface to generate a START signal
8AH	10	RESET	Initializes the Interface boards
8BH	11	READ COMP.	Disables the Interface memories read from
8CH	12	PREBLANK	Enables a START pulse to be generated, in case BLANK powered up low

*SCR = Status Control Register

Fig. V-5 A/D Calibration

Input (mv)		Output			
Lo	Hi	3	2	1	0
000	12	0	0	0	0
28	82	0	0	0	1
93	143	0	0	1	0
159	215	0	0	1	1
228	282	0	1	0	0
297	350	0	1	0	1
361	421	0	1	1	0
436	487	0	1	1	1
496	551	1	0	0	0
568	623	1	0	0	1
635	689	1	0	1	0
704	760	1	0	1	1
771	831	1	1	0	0
844	899	1	1	0	1
908	965	1	1	1	0
979	1000	1	1	1	1

Fig. V-6 SAMPLE OUTPUTS

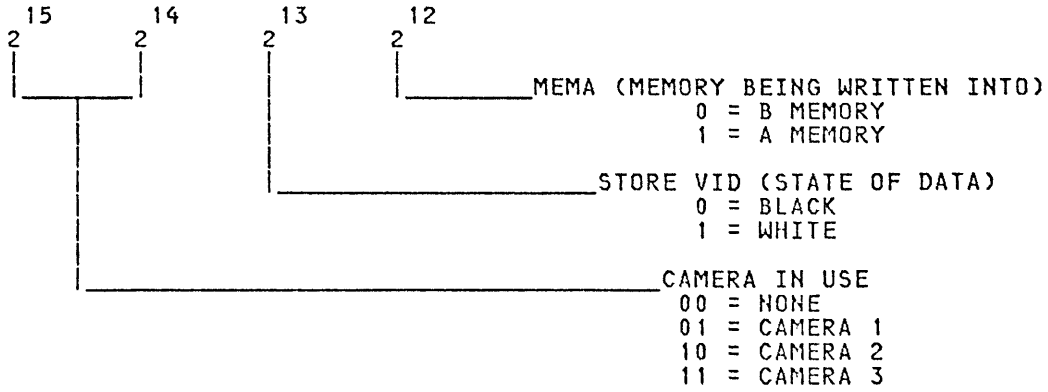
SAMPLE #	INPUT TO U20-12	START GATE	END GATE	QUANTIZING LEVEL	MODE
1	U58-3	00H	6CH	8H	PIXEL
2	U58-3	00H	6CH	8H	TRAN
3	U58-3	00H	6CH	8H	STR.L
4	U58-3	30H	32H	8H	PIXEL
5	U58-3	30H	32H	8H	TRAN
6	U58-3	30H	32H	8H	STR.L
7	U58-3	69H	74H	8H	PIXEL
8	U58-3	69H	74H	8H	TRAN
9	U58-3	69H	74H	8H	STR.L
10	U58-7	11H	29H	8H	PIXEL
11	U58-7	11H	29H	8H	TRAN
12	U58-7	11H	29H	8H	STR.L
13	U8-7	00H	6CH	8H	PIXEL
14	U8-7	00H	6CH	8H	TRAN
15	U8-7	00H	6CH	8H	STR.L
16	U8-7	00H	6CH	4H	PIXEL
17	U8-7	00H	6CH	4H	TRAN
18	U8-7	00H	6CH	4H	STR.L
19	U8-7	00H	6CH	2H	PIXEL
20	U8-7	00H	6CH	AH	PIXEL
21	U8-7	00H	6CH	AH	TRAN
22	U8-7	00H	6CH	AH	STR.L
23	U8-7	00H	6CH	CH	PIXEL
24	U8-7	00H	6CH	CH	TRAN
25	U8-7	00H	6CH	CH	STR.L
26	U8-7	00H	6CH	EH	PIXEL
27	U8-7	00H	6CH	8H	TRAN
28	U8-7	10H	6CH	8H	TRAN
29	U8-7	20H	6CH	8H	TRAN
30	U8-7	60H	6CH	8H	TRAN
31	U8-7	25H	45H	8H	TRAN
32	U8-7	00H	6CH	8H	A/D

In the following discussion are shown samples of the outputs whose specifications are shown in the table above. It will be noted that three different inputs to U20-12, the Data input to the flip-flop generating DIG VID, were used. For the first nine

samples U58-3, a signal that changes state each CLOCK period, was used to show that the interface resolution is good to one photodiode. Samples 10, 11, and 12 show various outputs when the input was U58-7, a signal that changes state every eight CLOCK periods, and samples 13 through 32 various outputs when the input was U8-7, the 1-bit digital version of the VIDEO signal coming from the Reticon as it scanned across 4 slits of a shadow mask. (A picture of this VIDEO signal is shown on page 45.) For all 32 samples, the 576 KHZ CLOCK and 60 HZ START signals were used.

Samples 1, 2, and 3 show outputs for PIXEL, TRAN, and STR.L modes, respectively, when the START GATE is 00 (corresponding to photodiode address 000) and the END GATE 6CH (corresponding to photodiode address 6C0H, or 1728 in decimal). Since the first 16 photodiodes in the GATE area are not recorded and since each SBC 80/20 memory location holds eights bits of PIXEL Data, then (1728-16)/8 = 214 (decimal) = D6 (hexadecimal) SBC 80/20 memory locations - 3000H-30D5H - are filled with "AA" (10101010 in binary) when PIXEL mode is chosen, as shown in sample 1.

TRAN mode and STR.L mode can store information for as many as 255 transitions or strings. For each transition or string, 16 bits of data, in the form of 4 hexadecimal digits, are recorded in memory. The upper 4 bits, which comprise the first of the 4 hexadecimal digits, give the following information:



The lower 12 bits, or 3 digits, give the photodiode address of the

first photodiode after the transition, for TRAN mode, or the length of the string, i.e., the number of photodiodes in a string of photodiodes of the same state, for STR.L (string length) mode.

Looking at sample 2, one can find in locations 3000H and 3001H information about the first transition - 6012H. The first digit, 6H, or 0110 in binary, indicates that camera 1 was in use, white data was received, and the "B" memory was written into. The last three digits - 012H - give the hexadecimal address of the first photodiode after the transition, meaning that the last photodiode in the group for which the state of the video was 1 was 011H. Locations 3002H and 3003H hold information about the second transition - 4013H. In this case, the first digit is 4H, or 0100 in binary, which differs from the first digit for the first transition only in the third bit, the state of the data, which this time is black. (The camera in use and memory being written into don't change during a scan, so, unless one is doing some unusual operation, the first, second, and fourth bits of the first digit don't change during a scan either.) Looking on through sample 2 one will see that the first digit of transition data alternates between 6H and 4H, corresponding to the state of the data's alternating between 1 and 0. (Had the "A" memory been the memory being written into, the first digit of transition data would have alternated between 7H and 5H, as in sample 8. Had camera 2 or camera 3 been used instead of camera 1 the alternation would have been between other pairs of digits; unfortunately, no examples of this type are available, as camera 1 was the only camera used to make samples.)

The last 3 digits of TRAN Data in sample 2 increase by 1 each time - 012H, 013H, 014H, etc. - duly recording the fact that a transition occurred each CLOCK period. One should note at this point, however, that the information in the 255th position, locations 31FCH and 31FDH, is not information about the 255th transition, but rather information about the final transition in the GATE area. This is because once the memory address counters

reach 255 (FFH) they stay there; thus location 255 in the interface memories has information overwritten into it for every transition from the 255th until the last in the GATE area, whose information is what gets transferred to SBC 80/20 memory.

Sample 3 shows STR.L Data, the first digit of which is loaded in the same way as the first digit of TRAN Data. However, the last three digits give the string length, i.e., the number of photodiodes in a string of photodiodes of the same state, as mentioned earlier. Thus, since the input data was changing state each CLOCK period, the string lengths recorded are each 001H. Note at this point, by comparing samples 1, 2, and 3, how much more economical is PIXEL mode than either TRAN mode or STR.L mode when transitions are many.

Notice should also be made here that the photodiode counters and GATE's miss being synchronized by 1 photodiode. The GATE's go up and come down one CLOCK (and thus 1 photodiode) too late with respect to the photodiode address counters. (This could be due to very slow functioning of the CMOS comparators, which generate the PREGATE signal, from which are generated the various GATE's.) This is why PIXEL, in sample 1, is "A"'s (1010), instead of "5"'s (0101) - the leading 0 is missed. This is also why, as in sample 2, the addresses of the transitions are 1 off - i.e., the first should be 011H, not 012H, and the last 6BFH, not 6C0H; and why, for example, the first string length is 007H, instead of 008H, in sample 12. Parallel coordination among the various data modes, however, is still synchronized - i.e., the first photodiode (in a GATE area) looked at in each of the four data modes is the same photodiode.

Samples 4, 5, and 6 differ from samples 1, 2, and 3 only in the GATE area, which, for samples 4, 5, and 6, extends from 30H (corresponding to photodiode address 300H, or 768) to 32H (corresponding to photodiode photodiode address 320H, or 800) and is thus 32 photodiodes wide. Since the first 16 photodiodes are not recorded, only 16 are, and their PIXEL values are recorded in

SBC 80/20 memory locations 3000H and 3001H, as seen in sample 4. Samples 5 and 6 show TRAN and STR.L Data for the same GATE area.

Sample 5 shows another peculiarity of the interface. The last transition arrives and advances the memory address counters (for the memories being written into), but the GATE falls before the transition data gets recorded at this address. The computer reads this address as the final memory address filled and so reads whatever happens to be stored there from before. This problem occurs, however, only if the END GATE is less than 6CH.

In samples 7, 8, and 9 the GATE area designated is 69H through 74H (i.e., photodiode addresses 690H-740H). 6C0H (corresponding to 1728), however, is the address of the last photodiode in the array, so output is not recorded beyond that point. The same output would appear, by the way, with any END GATE greater than 6CH, given the same START GATE, 69H. Again, the first 16 photodiodes are missed, so recording starts at 6A0H. Recording must stop before 6C0H is reached, so PIXEL Data for only 32 photodiodes is recorded in sample 7. Samples 8 and 9 give the corresponding TRAN and STR.L Data.

Samples 10, 11, and 12 show PIXEL, TRAN, and STR.L Data when the input to U20-12 is alternating groups of eight zeroes and eight ones. The GATE area is 11H through 29H (i.e., photodiode addresses 110H-290H).

Samples 13 through 32 are all data from the VIDEO signal coming from the Reticon, as shown in the picture on pages 45 and 46. The peaks correspond to the locations of the slits in the shadow mask. Samples 13, 14, 15, and 32 show PIXEL, TRAN, STR.L, and A/D Data for this VIDEO signal when the quantizing level was 8 and the GATE area 00H-6CH. Note how much less space is required to store either TRAN or STR.L Data than either PIXEL or A/D Data in a case such as this where the GATE area is large and the transitions few. PIXEL, TRAN, and STR.L modes of data have all been seen before, but sample 32, which shows A/D mode data, is one we haven't seen yet. A/D mode, which records gray level data,

gives more detailed information than does PIXEL mode (or either of the other modes), but it also requires more memory space - four times as much as for PIXEL mode. Since only 255 16-bit memory locations are available on the interface, and each location holds data for 4 photodiodes, data from only 1020 photodiodes can be stored, as mentioned in Section IV. Two SBC 80/20 memory locations are needed to store data from one interface memory location, so 510, or 1FE in hexadecimal, SBC 80/20 memory locations are needed. This can be seen in sample 32, where memory locations 3000H through 31FDH are filled.

Samples 16, 17, and 18; 20, 21, and 22; and 23, 24, and 25 show PIXEL, TRAN, and STR.L Data for quantizing levels of 4H, AH, and CH, respectively. Following these samples is a comparison of outputs made from the same VIDEO data, but with different thresholds, or quantizing levels - EH, 8H, 4H, and 2H. By looking at the A/D Data in sample 32, one can see that the VIDEO reached as high as EH only once and never got below 3H. When the quantizing level, or threshold, was set at EH no VIDEO was high enough to reach it and so all the PIXEL Data bits were zeros. On the other hand, when the quantizing level was set at 2H, no VIDEO was low enough to reach it, much less go below it, so all PIXEL Data bits were ones, causing all digits in the output to be "F"'s. (The fact that sample 32 has an EH in it and sample 16 doesn't show this could be due to the fact that the VIDEO output varied from scan to scan, as the shadow mask was not held very securely in place. It could also be due to the fact that the EH level coming out of the A/D converter might be slightly lower that the quantizing level EH.) Finally are shown several outputs using the same VIDEO data as input, but with different gates.

A final note concerning samples 13 through 32 _ the shadow mask was not tightly secured in place when these samples were made. As a result, the VIDEO signal from the Reticon varied from scan to scan causing what appear to be discrepancies between corresponding data in different modes, as well as between corresponding data in the same mode but from different scans.

1 PIXEL DATA

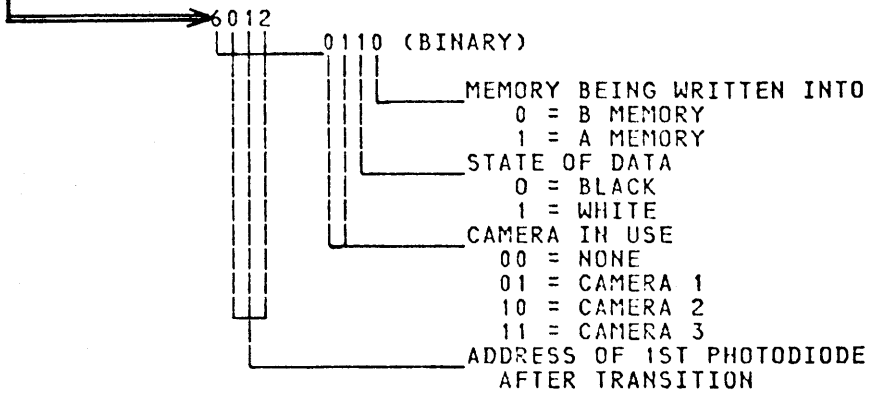
```
3000 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3010 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3020 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3030 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3040 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3050 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3060 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3070 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3080 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
3090 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
30A0 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
30B0 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
30C0 AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
30D0 AA AA AA AA AA AA BB BB BB BB BB BB BB BB BB BB
30E0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
30F0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3100 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3110 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3120 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3130 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3140 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3150 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3160 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3170 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3180 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3190 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
31A0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
31B0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
31C0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
31D0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
31E0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
31F0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB 31
3200 EC
```

AA AA (HEXADECIMAL) = 1010101010101010 (BINARY)

This sample shows PIXEL Data for a complete scan, since the START GATE is 00H and the END GATE 6CH, corresponding to photodiode addresses 000 and 1728, respectively. The first 26 photodiodes in the GATE area are not recorded, so, since each SBC 80/20 memory location holds eight bits of PIXEL Data, (1728-16)/8 = 214 = D6H SBC 80/20 memory locations - 3000H through 30D5H - are filled with "AA". The rest of the memory locations are filled with "BB" because before the interface data was transferred memory locations 3000H-3200H were all filled with "BB" by the program.

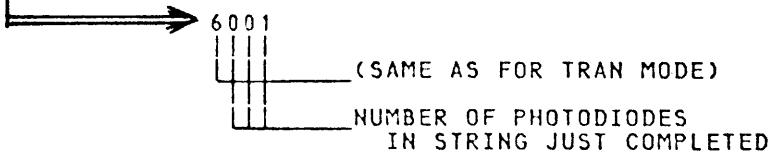
2 TRANSITION DATA

```
3000 60 12 40 13 60 14 40 15 60 16 40 17 60 18 40 19
3010 60 1A 40 1B 60 1C 40 1D 60 1E 40 1F 60 20 40 21
3020 60 22 40 23 60 24 40 25 60 26 40 27 60 28 40 29
3030 60 2A 40 2B 60 2C 40 2D 60 2E 40 2F 60 30 40 31
3040 60 32 40 33 60 34 40 35 60 36 40 37 60 38 40 39
3050 60 3A 40 3B 60 3C 40 3D 60 3E 40 3F 60 40 40 41
3060 60 42 40 43 60 44 40 45 60 46 40 47 60 48 40 49
3070 60 4A 40 4B 60 4C 40 4D 60 4E 40 4F 60 50 40 51
3080 60 52 40 53 60 54 40 55 60 56 40 57 60 58 40 59
3090 60 5A 40 5B 60 5C 40 5D 60 5E 40 5F 60 60 40 61
30A0 60 62 40 63 60 64 40 65 60 66 40 67 60 68 40 69
30B0 60 6A 40 6B 60 6C 40 6D 60 6E 40 6F 60 70 40 71
30C0 60 72 40 73 60 74 40 75 60 76 40 77 60 78 40 79
30D0 60 7A 40 7B 60 7C 40 7D 60 7E 40 7F 60 80 40 81
30E0 60 82 40 83 60 84 40 85 60 86 40 87 60 88 40 89
30F0 60 8A 40 8B 60 8C 40 8D 60 8E 40 8F 60 90 40 91
3100 60 92 40 93 60 94 40 95 60 96 40 97 60 98 40 99
3110 60 9A 40 9B 60 9C 40 9D 60 9E 40 9F 60 A0 40 A1
3120 60 A2 40 A3 60 A4 40 A5 60 A6 40 A7 60 A8 40 A9
3130 60 AA 40 AB 60 AC 40 AD 60 AE 40 AF 60 B0 40 B1
3140 60 B2 40 B3 60 B4 40 B5 60 B6 40 B7 60 B8 40 B9
3150 60 BA 40 BB 60 BC 40 BD 60 BE 40 BF 60 C0 40 C1
3160 60 C2 40 C3 60 C4 40 C5 60 C6 40 C7 60 C8 40 C9
3170 60 CA 40 CB 60 CC 40 CD 60 CE 40 CF 60 D0 40 D1
3180 60 D2 40 D3 60 D4 40 D5 60 D6 40 D7 60 D8 40 D9
3190 60 DA 40 DB 60 DC 40 DD 60 DE 40 DF 60 E0 40 E1
31A0 60 E2 40 E3 60 E4 40 E5 60 E6 40 E7 60 E8 40 E9
31B0 60 EA 40 EB 60 EC 40 ED 60 EE 40 EF 60 F0 40 F1
31C0 60 F2 40 F3 60 F4 40 F5 60 F6 40 F7 60 F8 40 F9
31D0 60 FA 40 FB 60 FC 40 FD 60 FE 40 FF 61 00 41 01
31E0 61 02 41 03 61 04 41 05 61 06 41 07 61 08 41 09
31F0 61 0A 41 0B 61 0C 41 0D 61 0E 41 0F 66 C0 BB 31
```



3 STR.L (String Length) DATA

3000	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3010	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3020	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3030	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3040	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3050	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3060	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3070	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3080	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3090	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
30A0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
30B0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
30C0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
30D0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
30E0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
30F0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3100	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3110	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3120	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3130	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3140	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3150	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3160	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3170	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3180	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
3190	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
31A0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
31B0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
31C0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
31D0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
31E0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	40	01
31F0	60	01	40	01	60	01	40	01	60	01	40	01	60	01	BB	31



ALTERNATING 0-1 DATA - DIFFERENT GATES - DIFFERENT MODES

GATES

30H 32H

4 PIXEL

```
3000 AA AA BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

5 TRAN

30H 32H

```
3000 63 12 43 13 63 14 43 15 63 16 43 17 63 18 43 19
3010 63 1A 43 1B 63 1C 43 1D 63 1E 43 1F 63 20 40 01
3020 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

6 STR.L

30H 32H

```
3000 70 01 50 01 70 01 50 01 70 01 50 01 70 01 50 01
3010 70 01 50 01 70 01 50 01 70 01 50 01 70 01 50 01
3020 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

7 PIXEL

69H 74H

```
3000 AA AA AA AA BB BB BB BB BB BB BB BB BB BB BB BB
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

8 TRAN

69H 74H

```
3000 76 A2 56 A3 76 A4 56 A5 76 A6 56 A7 76 A8 56 A9
3010 76 AA 56 AB 76 AC 56 AD 76 AE 56 AF 76 B0 56 B1
3020 76 B2 56 B3 76 B4 56 B5 76 B6 56 B7 76 B8 56 B9
3030 76 BA 56 BB 76 BC 56 BD 76 BE 56 BF 76 C0 BB BB
3040 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

9 STR.L

69H 74H

```
3000 60 01 40 01 60 01 40 01 60 01 40 01 60 01 40 01
3010 60 01 40 01 60 01 40 01 60 01 40 01 60 01 40 01
3020 60 01 40 01 60 01 40 01 60 01 40 01 60 01 40 01
3030 60 01 40 01 60 01 40 01 60 01 40 01 60 01 BB BB
3040 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

DATA = ALTERNATING GROUPS OF EIGHT ONES AND EIGHT ZEROS

START GATE = 11

END GATE = 29

10 PIXEL

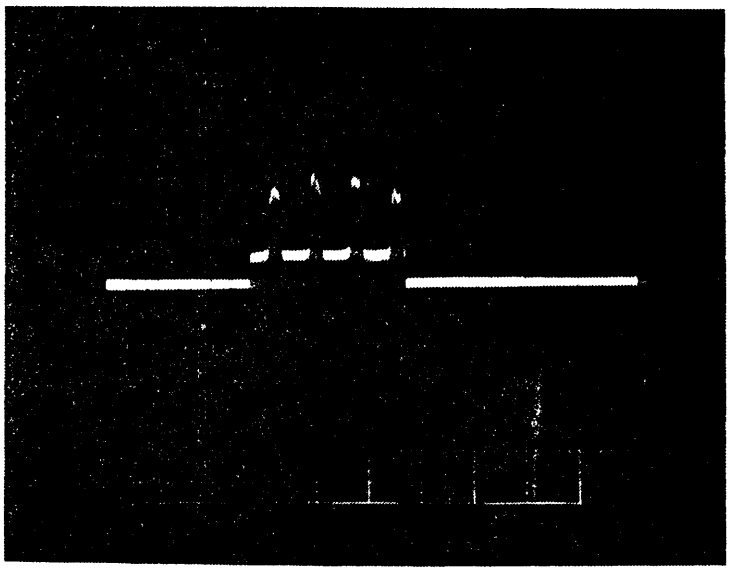
```
3000 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE
3010 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE
3020 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE 01 FE BB BB
3030 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

11 TRAN

```
3000 41 28 61 30 41 38 61 40 41 48 61 50 41 58 61 60
3010 41 68 61 70 41 78 61 80 41 88 61 90 41 98 61 A0
3020 41 A8 61 B0 41 B8 61 C0 41 C8 61 D0 41 D8 61 E0
3030 41 E8 61 F0 41 F8 62 00 42 08 62 10 42 18 62 20
3040 42 28 62 30 42 38 62 40 42 48 62 50 42 58 62 60
3050 42 68 62 70 42 78 62 80 42 88 62 90 BB BB BB BB
3060 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

12 STR.L

```
3000 50 07 70 08 50 08 70 08 50 08 70 08 50 08 70 08
3010 50 08 70 08 50 08 70 08 50 08 70 08 50 08 70 08
3020 50 08 70 08 50 08 70 08 50 08 70 08 50 08 70 08
3030 50 08 70 08 50 08 70 08 50 08 70 08 50 08 70 08
3040 50 08 70 08 50 08 70 08 50 08 70 08 50 08 70 08
3050 50 08 70 08 50 08 70 08 50 08 70 08 BB BB BB BB
3060 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```



VIDEO SIGNAL FROM RETICON

13 PIXEL

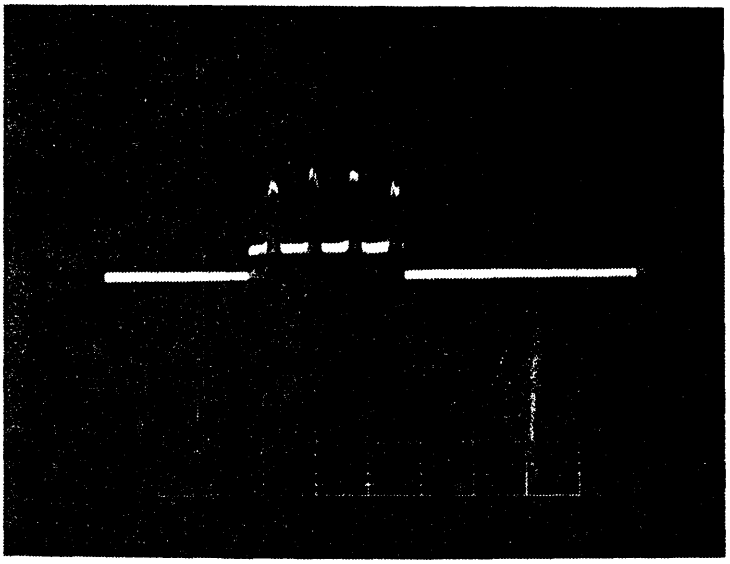
```
3000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3010 00 00 00 00 00 00 07 FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF F0 00 00 00 00 00 00 00 00 00
3030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3050 00 3F FF FF FF FF FF FF FF FF FF FF FF FF FF 00
3060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3080 00 00 00 00 00 00 00 00 FF FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FF 80 00 00 00 00 00 00 00
30A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30C0 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30D0 FC 00 00 00 00 00 BB BB BB BB BB BB BB BB BB BB
30E0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

14 TRAN

```
3000 40 C6 61 46 42 98 63 0C 44 59 64 DB 46 21 66 9F
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

15 STR.L

```
3000 40 B5 60 81 41 53 60 72 41 4E 60 81 41 47 60 7E
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```



VIDEO SIGNAL FROM RETICON

32 A/D

```
3000 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
3010 33 33 33 33 33 33 33 33 33 33 33 33 43 33 33 33
3020 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
3030 33 33 33 33 33 33 33 33 33 33 43 33 33 34 33 33
3040 34 34 34 34 34 44 34 34 44 44 34 34 44 44 44 44
3050 44 44 44 44 44 45 55 56 78 89 9A 9A AA AA AB AB
3060 BB BB AB AA BB CB BC BB BC BB BB BB BB BB BC BC
3070 CC CC BC BB BC CC CC CC CC CC CD CC CC CC CC BC
3080 CC CC CC CC CD DC CC CC CC CC CC CC CC CC CC CC
3090 CC CC CC BC BC BB 98 76 55 54 44 44 44 44 34 34
30A0 44 34 34 34 34 44 33 34 34 34 33 34 34 33 33 33
30B0 34 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
30C0 33 34 33 33 33 33 33 33 33 33 33 33 33 33 43 33
30D0 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
30E0 33 33 33 33 33 34 33 33 33 33 33 33 33 34 33 33
30F0 33 33 33 33 33 33 33 33 33 43 33 33 33 33 33 33
3100 33 33 33 33 33 34 33 34 34 34 33 34 34 33 33 33
3110 33 34 33 33 34 34 33 33 34 44 33 34 34 34 33 34
3120 34 34 34 34 34 34 34 34 44 44 34 34 44 34 34 34
3130 44 44 34 34 44 44 44 34 44 44 44 44 44 44 44 45
3140 56 67 78 78 99 99 AB AB BB BB BC BC CD DD CD CC
3150 DD CC DD DD DD DD DD DD DD DD DD DD DD DD DD DD
3160 DD DD ED CC CC BC CC BB BB BC CC BC CC CC CC CC
3170 CD DC CC CC CC CC BB 99 99 98 77 65 54 44 44 34
3180 44 44 34 34 34 44 33 33 33 33 33 33 33 43 33 33
3190 33 33 33 33 33 33 33 33 33 33 33 33 34 33 33 33
31A0 33 34 33 33 33 33 33 33 33 33 33 33 34 43 33 33
31B0 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
31C0 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
31D0 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
31E0 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33
31F0 33 33 33 33 33 34 43 33 33 34 34 34 33 33 BB FD
3200 ED
```

THRESHOLD = 4H

16 PIXEL

```
3000  00 00 00 00 00 00 00 00 18 00 00 00 00 00 01 11
3010  55 75 F5 FF FF FF FF FF FF FF FF FF FF FF FF FF
3020  FF FF FF FF FF FF F5 55 10 40 00 00 00 00 00 00
3030  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3040  00 00 00 00 10 00 14 00 15 51 55 55 F5 F5 F5 FF
3050  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF DC
3060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3080  00 10 55 75 FF FF FF FF FF FF FF FF FF FF FF FF
3090  FF FF FF FF FF FF FF FF F5 40 00 00 00 00 00 00
30A0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 15 77
30C0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30D0  FF DD 00 00 00 00 BB BB BB BB BB BB BB BB BB BB
30E0  BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

17 TRAN

```
3000  50 73 70 74 50 A0 70 A1 50 A2 70 A3 50 A4 70 A5
3010  50 A6 70 A7 50 A8 70 A9 50 AA 70 AD 50 AE 70 AF
3020  50 B0 70 B5 50 B6 71 4D 51 4E 71 4F 51 50 71 51
3030  51 52 71 53 51 54 71 55 51 56 71 57 51 5C 71 5D
3040  51 9B 71 9C 52 30 72 31 52 5C 72 5D 52 5E 72 5F
3050  52 60 72 61 52 62 72 63 52 64 72 65 52 66 72 67
3060  52 68 72 69 52 6A 72 6B 52 6C 72 6D 52 6E 72 6F
3070  52 70 72 71 52 72 72 73 52 74 72 75 52 76 72 77
3080  52 78 72 79 52 7A 72 7B 52 7C 72 7D 52 7E 72 7F
3090  52 80 72 83 52 84 72 85 52 86 72 87 52 88 72 8D
30A0  52 8E 73 15 53 3C 73 3D 54 2C 74 2D 54 2E 74 2F
30B0  54 30 74 31 54 32 74 35 54 36 74 37 54 38 74 3D
30C0  54 3E 74 47 54 48 74 DD 54 DE 74 DF 54 E0 74 E1
30D0  54 E2 74 E3 54 E4 74 E5 56 0C 76 0D 56 0E 76 0F
30E0  56 10 76 11 56 12 76 13 56 14 76 15 56 16 76 A5
30F0  BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

18 STR.L

```
3000  40 83 60 01 40 01 60 01 40 05 60 01 40 03 60 01
3010  40 C1 60 03 40 C1 60 01 40 C1 60 01 40 01 60 03
3020  40 01 60 01 40 01 60 9F 40 01 60 03 40 01 60 01
3030  40 C1 60 01 40 C1 60 01 40 C1 60 01 40 C1 60 01
3040  40 03 60 01 40 01 60 01 40 01 60 01 40 BF 60 01
3050  40 23 60 01 40 0B 60 01 40 07 60 01 40 C1 60 01
3060  40 01 60 01 40 01 60 01 40 01 60 01 40 01 60 01
3070  40 C1 60 01 40 C1 60 01 40 C1 60 01 40 C1 60 01
3080  40 01 60 01 40 01 60 01 40 01 60 01 40 01 60 01
3090  40 C1 60 01 40 C1 60 03 40 C1 60 01 40 C1 60 05
30A0  40 01 60 01 40 01 60 03 40 01 60 01 40 01 60 01
30B0  40 C1 60 83 40 C1 60 01 40 5B 60 01 40 BB 60 01
30C0  40 03 60 01 40 01 60 03 40 01 60 01 40 01 60 05
30D0  40 C1 60 01 40 01 60 9F 40 C1 60 01 40 C1 60 01
30E0  40 01 60 01 41 27 60 01 40 01 60 01 40 03 60 01
30F0  40 C1 60 01 40 C1 60 8F BB BB BB BB BB BB BB BB
```

THRESHOLD = AH

20 PIXEL

```
3000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3010 00 00 00 00 00 00 03 FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF E0 00 00 00 00 00 00 00 00 00
3030 00 C0 0C 00 00 00 0C 00 00 C0 0C 00 00 C0 0C 00
3040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3050 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF 80
3060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070 00 C0 0C 00 00 C0 0C 00 00 C0 0C 00 00 C0 0C 00
3080 00 00 00 00 00 00 00 01 FF FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FE 00 C0 0C 00 00 C0 0C 00
30A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0 00 C0 0C 00 00 C0 0C 00 00 C0 0C 00 00 C0 0C 00
30C0 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30D0 C0 C0 0C 00 00 70 BB BB BB BB BB BB BB BB BB BB
30E0 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

21 TRAN

```
3000 50 C6 71 44 52 99 73 07 54 57 74 D7 56 1F 76 9A
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

22 STR.L

```
3000 50 B4 70 7E 51 55 70 6F 51 4F 70 81 51 47 70 7B
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

THRESHOLD = CH

23 PIXEL

```
3000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3010 00 00 00 00 00 00 00 FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF C0 00 00 00 00 00 00 00 00 00
3030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3050 00 01 FF FF FF FF FF FF FF FF FF FF FF FF C0 00
3060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3080 00 00 00 00 00 00 00 00 00 FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FF FC 00 00 00 00 00 00 00
30A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30C0 00 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30D0 FF 00 00 00 00 00 BB BB BB BB BB BB BB BB BB BB
```

24 TRAN

```
3000 50 CA 71 43 52 9E 72 9F 52 A0 73 04 54 59 74 D7
3010 56 21 76 99 BB BB BB BB BB BB BB BB BB BB BB BB
3020 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

25 STR.L

```
3000 40 B8 60 7A 41 5D 60 63 41 56 60 7E 41 4A 60 78
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3020 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

PIXEL MODE - SAME INPUT DATA - DIFFERENT THRESHOLDS

THRESHOLD SAMPLE ↓

26 EH

```
3000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3080 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3090 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

13 8H

```
3000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3010 00 00 00 00 00 00 07 FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF F0 00 00 00 00 00 00 00 00 00
3030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3050 00 3F FF FF FF FF FF FF FF FF FF FF FF FF FF 00
3060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3080 00 00 00 00 00 00 00 00 FF FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FF 80 00 00 00 00 00 00 00
30A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30C0 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
```

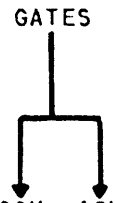
16 4H

```
3000 00 00 00 00 00 00 00 00 18 00 00 00 00 00 01 11
3010 55 75 F5 FF FF FF FF FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF F5 55 10 40 00 00 00 00 00 00
3030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3040 00 00 00 00 10 00 14 00 15 51 55 55 F5 F5 F5 FF
3050 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF DC
3060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3080 00 10 55 75 FF FF FF FF FF FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FF F5 40 00 00 00 00 00 00
30A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 15 77
30C0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
```

19 2H

```
3000 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3010 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3030 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3040 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3050 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3060 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3070 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3080 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30A0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30B0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30C0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
```

TRAN MODE - SAME DATA FROM RETICON - DIFFERENT GATES



27

00H 6CH

```
3000 40 C3 61 44 42 96 63 08 44 55 64 D7 46 1D 66 9B
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
3020 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

28

10H 6CH

```
3000 61 44 42 96 63 08 44 55 64 D8 46 1D 66 9C BB BB
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

29

20H 6CH

```
3000 42 98 63 0A 44 57 64 D9 46 1F 66 9D BB BB BB BB
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

30

60H 6CH

```
3000 46 1E 66 9D BB BB BB BB BB BB BB BB BB BB BB BB
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

31

25H 45H

```
3000 52 94 73 07 BB BB BB BB BB BB BB BB BB BB BB BB
3010 BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB BB
```

VI. DETAILED OPERATION OF THE INTERFACE

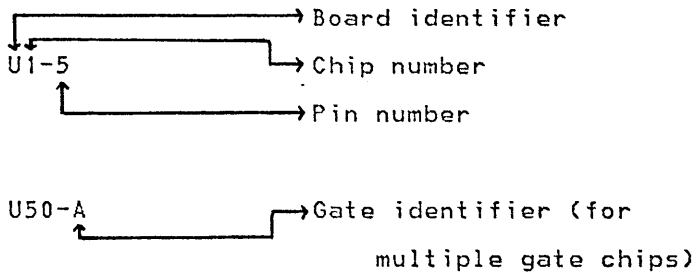
Now that the general operation of the system and the software related to it have been described, it is time to look at the nuts and bolts of the system, as shown in the schematics in the Appendix. The discussion is broken down into eleven subsections, each of which deals with one function of the system. Numbers in parentheses immediately following the title of each subsection give, in order of appearance, the sheet numbers of the schematics on which that subsection's circuitry is located. Then, at the end of Section VI, starting on page 100, are eleven timing diagrams, one for each subsection. The Figure number on each timing diagram matches its related subsection's number. The diagrams have been drawn for a CLOCK rate of 576 KHZ, since this is the fastest clock rate used, with one exception noted later for Fig. VI-0.

A few words should be said at this point about the development of the circuit, since one may wonder why the mixture of CMOS and TTL logic. Originally the interface was going to be designed using CMOS chips. There were several reasons for this choice. First of all, the hardware systems the interface was to replace were CMOS systems. Secondly, the memories available in the stockroom were CMOS memories. Thirdly, there was a large variety of CMOS chips available in the stockroom, whereas the selection of TTL chips could hardly have been called a selection there were so few. Fourthly, some functions available in CMOS chips were not available on TTL chips, as, for example, the 4024 7-state ripple-carry binary counter/divider. Fifthly, CMOS has lower power requirements than TTL logic.

CMOS logic, however, is much slower than TTL logic, so when timing constraints made it necessary and the stockroom made it possible (by this time the stockroom selection of TTL chips was growing at an admirable rate), TTL chips were substituted for CMOS chips. With such a mixture, it is advisable to attach pullup

resistors to TTL outputs that feed CMOS inputs, since the minimum value a TTL high output (Voh) may have is around 2.4 volts (though the typical value is around 3.4 volts) , whereas the input high voltage (Vih) for CMOS chips has a minimum of 3.5 volts. In practice things worked quite well without pullup resistors, so they don't appear in all TTL to CMOS connections; those already on board when this fact was discovered were not removed, however. The lows, on the other hand, aren't a problem since the maximum output low voltage (Vol) for TTL is around 0.4 volts, while the maximum input low voltage for CMOS is 1.5 volts. Going the other direction, CMOS to TTL, is another story; drivers are required since regular CMOS chips aren't powerful enough to drive TTL chips.

In the following discussions, the chip and pin identifiers are as follows:



The Board identifier may be "U" or "L," depending on whether the chip is on Board U (the upper board, i.e., the one in the top slot of the card cage) or on Board L (the lower board, i.e., the board in the third slot of the card cage, the second slot not being used). The sheet number of the schematics on which a chip is located is indicated on the Board U and Board L layouts on pages 124 and 125. On those layouts the number of each chip is encircled and included along with the chip type and schematic location in a box corresponding to the chip's position on the actual board. On the schematics, the Board identifier and the chip number are encircled together, as for example, (U60). A few

oddities appear, such as L33A, in which case 33A is the chip number. P1 indicates a multibus connection and J1, J2, and J3 cable connections.

VI-0. QAA-QHH (SH. 4)

In order to synchronize operations and to make timing features more precise, the CLOCK signal (U18-15 or 2) is fed into the A and B inputs of a 74LS164 8-bit parallel-out serial shift register (U15). At the beginning of a scan a START/ pulse, generated elsewhere in the circuit (L38-8), feeds the Clear input of the shift register (U15-9), which clears the Q outputs of that register (U15-3, 4, 5, 6, 10, 11, 12, and 13) to zero. After the START/ pulse goes high, disabling the Clear input, the shift register Clock, U15-8, fed by the 9.216 MHZ multibus Clock, causes the signal at the A and B inputs, i.e., CLOCK, to be shifted into QA and all the other Q outputs to be shifted one position in the direction from QA to QH every time it rises.

As can be seen in Fig. VI-0, QAA (subscripts - 1 for upper diagram and 2 for lower diagram - are left out in most of the following discussion) follows CLOCK on the first 9.216 MHZ Clock after CLOCK. QBB-QHH follow QAA 1-7 9.216 MHZ Clock periods, respectively, later. Thus QBB follows QAA by 108.5 ns.; QCC follows QBB by 108.5 ns.; etc. The 576 KHZ CLOCK is the fastest CLOCK that can be used in this system because exactly eight 9.216 MHZ Clock pulses occur while the 576 CLOCK is high and eight while it is low. As a result, QHH follows QAA high before QAA falls and follows QAA low before QAA rises again. It was on this basis that timing details were set up. Thus a signal lasting from the fall of QHH to the rise of QAA, for example, would last a minimum of 108.5 ns. If a much faster CLOCK were used, QAA would rise before QHH fell, so one would have to wait much of another CLOCK period

until QAA rose again. This would throw off any timing involving a rise of one signal and a fall of another signal, or vice versa.

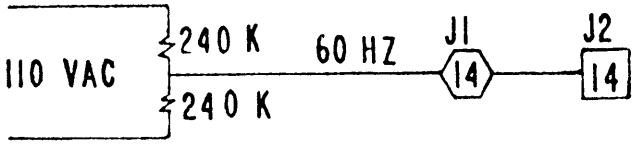
CLOCKS slower that 576 KHZ are fine. Fig. VI-0 shows the timing with a 576 KHZ CLOCK at the top and a slower CLOCK at the bottom. The timing between two rising, or two falling, signals as shown between the rise of QBB and the rise of QGG doesn't change, regardless of the CLOCK rate. A-1 and A-2 are the same length. However, the time between signals changing in different directions, as between the fall of QHH and the rise of QAA, varies with the CLOCK rate; note that B-1 is much shorter than B-2.

Timing was designed for the 576 CLOCK as the worst case. Slower CLOCK's would simply allow more time for things to settle, but events would occur in the proper sequence. Faster CLOCK's would wreak havoc in the system.

VI-1. CLOCK, START, CONTROL (SH.'S 2, 11, 10, 3, 4, 5)

This section of the circuit deals with coordination of control between the interface and the computer. Fig.VI-1 shows the situation when COMP.START is chosen for the Start signal. There are two other possible Start signals, the generation of which will be described before going on to explain Fig. VI-1

RSTART is simply the Start signal generated by the RC-100A motherboard and described in Section II, the Reticon Unit. 60 HZ START, on the other hand, is generated from the 60 HZ line signal. Not shown on the schematics is the following:



J2-14 feeds into a pair of 1N914 diodes that clamp that signal, 60 HZ, to vary between -5.6 volts and +5.6 volts. Farther down the line another pair of diodes clamp U23-2 to a peak of +0.6 volts and U23-3 to a low of -0.6 volts. The 27K resistors and the 0.05 uF capacitors give a time constant of 1.35 ms. Thus there is a 1.35 ms. long pulse at Vout (U23-6) every 8.33 ms.,i.e., making the signal frequency to be really 120 HZ. Vout is clamped to ground by the diode on U24 so that the Data input to the D flip-flop (U29-5) swings between ground and +5 volts.

ØB, of much higher frequency than 120 HZ, clocks the Q output of U29-A high following the rising edge on the 120 HZ pulse. The Q/ output of U29-A goes low removing the Reset from U29-B. Thus U29-1 and U29-12 are both high within 300 ns. of the rise of ØB, causing 60 HZ START (U27-4), the output of the AND gate into which they both feed, to go high within 550 ns. of the rise of ØB. The next rise of ØB causes U29-12 to go low and thus within 550 ns. of this rise of ØB, 60 HZ START falls. The result of this is that the 60 HZ START envelopes one and only one rising edge of CLOCK (which occurs within 250 ns. of the fall of ØB), as required by the Reticon for external Start pulses.

A note should be made here about RCLOCK also. As seen in Section VI-0, for proper functioning of the circuit, the CLOCK needs to have a positive pulse at least 868 ns. long. The RCLOCK sent out by the Reticon doesn't have that long a positive pulse, so it has to be put through a one-shot, U44. The negative output must be taken to feed U48 so that when the output of U48 is inverted by U36-B to form ØA and then later CLOCK, that CLOCK will have the needed positive pulse width.

With this, let us turn to the explanation of timing diagram VI-1 and the circuitry related to it. A RESET/ pulse (L69-12), sent out by the computer to initialize the interface boards, feeds one input of L23-A (sh. 10), a two-input AND gate. (The other input, EOS/ (U17-2), is unlikely to be low at the same time that a RESET/ pulse is sent since the functions set in motion by the

RESET/ pulse would invalidate the remainder of the scan in progress.) So, assuming EOS/ (L23-1) is high, the output of the AND gate, L23-3, feeds the clock input of a D-type flip- flop (L21-3) causing DATA READY/ (L21-6) to go low within 64 ns. of the rising edge of RESET/ and INT4/ (L35A-13) to go low within 35 ns. thereafter. The timing is similar when EOS/ arrives and clocks the flip-flop. Thus INT4/ goes low within 101 ns. of the rising edge of either RESET/ or EOS/, or of the latter of the two signals to rise should they both happen to be low at the same time, and remains low until 52 ns. max. after PROC.COMP./ (L69-2 and L21-1) goes low to clear the flip-flop (L21-A) and to disable INT4/.

The RESET/ pulse (L69-12) feeds into another AND gate, L33B-C, setting its output low within 24 ns. of the fall of RESET/. The fall of the other input, SSt/ (U54-2), similarly sets the output of L33B-C low. As with EOS/, SSt/ is not likely to be low at the same time as RESET/ is low. At any rate, the output of the AND gate, L33B-8, falls within 24 ns. of the fall of either SSt/ or RESET/ and rises within 24 ns. of the time when both signals are high again. The low appearing at the AND gate output, L33B-8, feeds the clear inputs of three D-type flip-flops (L35-1, L21-13, and L36-1) setting the Q outputs, PC (L35-5) and PCSYNC (L21-9) to zero and the Q/ output, BLANKSET/ (L36-6), high within 64 ns. of the fall of either SSt/ or of RESET/. BLANKSET/ and BLANK/ (L61-4) are the inputs to a NAND gate, L34-A, whose output, BLANK GATE (L34-3), goes high 20 ns. max. after either input goes low and low 20 ns. max. after both inputs are high. While BLANKSET/ is high, BLANK GATE is in the same state as BLANK, but delayed by 40 ns. max.

Another function of RESET/ is to clear U43, a 74LS175 quadruple D-type flip-flop, via its clear input (pin 1), causing the GATE outputs (U43-2, 7, 10, and 15) to go low within 35 ns. and the GATE/ outputs (U43-3, 6, 11, and 14) to go high within 25 ns. of the fall of RESET/. RESET, on the other hand, precedes RESET/ by about 20 ns. and feeds into an OR gate, U28-C, whose

output feeds the Reset input of a 4013 D-type flip-flop, U31-4, causing its Q output (U31-1) to go low within 650 ns. of the rise of RESET. RESET also directly feeds the Reset input of another 4013 D-type flip-flop, U31-10, setting its Q output, COMP.START (U31-13), low within 400 ns. of the rise of RESET.

Not shown on the timing diagram is the fact that RESET resets the outputs of several 4508 dual 4-bit latches (U9, U13, U37, U40, and U41) to zero. These latches are used as storage registers. Three of them - U9, U13, and U37 - are status control registers whose outputs govern various aspects of the scanning process. Thus, sometime between the RESET pulse and the start of scanning these three latches must be properly loaded from the computer or scanning won't take place at all. RESET has some other functions that are not shown on this timing diagram because they don't affect CLOCK, START, or control functions.

Once all the latches have been loaded and everything is ready for scanning, the computer sends out a PREBLANK pulse (L72-6). Within 40 ns. of the rise of PREBLANK, which feeds the Clock input of a D-type flip-flop (L36-3), BLANKSET/ (L36-6) goes low; 20 ns. max. later BLANK GATE (L34-3) goes high, as it must in order for the START/ pulse (L38-8) to be generated. Between scans BLANK (J2-43) is high and thus so is BLANK GATE. However, before the first scan, i.e., during power up, BLANK usually sits low, thus blocking generation of a START/ signal. As a result, no scanning would take place. To avoid such an occurrence, PREBLANK is sent to assure that BLANK GATE will be high and thus that a START/ signal can be generated.

Next, a PROC.COMP. signal (L54-6) is sent. Its rising edge clocks the D-type flip-flop, L35-A, setting its Q output, PC (L35-5), high within 25 ns. PC feeds the data input of another D-type flip-flop (L21-12), so once PC goes high the next rising edge of CLOCK (L21-11) causes PCSYNC (L21-9) to go high within 25 ns. Thus PCSYNC is synchronized to the CLOCK, as are GATE4/ (except during RESET) and PRESTART, as we shall see later. BLANK

GATE (L38-12) isn't necessarily synchronized to CLOCK, but it doesn't need to be since PREBLANK sets it high before PROC.COMP. sets PC high. Once PC goes high, three of the inputs to the 4-input NAND gate, L38-B, are high, and nothing more happens until the fourth input, PRESTART (L38-13) goes high.

PRESTART (U18-4) may come from one of three possible sources - COMP.START, a computer-generated signal; RSTART, a signal generated by the designated Reticon's motherboard; or 60 HZ START, a signal generated by the interface from the line voltage. The timing diagram shows the timing when a computer-generated signal, CPSTART (L37-8), is used. CPSTART feeds the clock input of a 4013 D-type flip-flop (U31-3), whose Q output (U31-1) rises within 300 ns. of the rise of CPSTART. U31-1 feeds the D input of another flip-flop (U31-9). Thus when U31-1 goes high, the next rising edge of ØB that occurs more than 340 ns. after the rise of CPSTART sets COMP.START high within 300 ns. Assuming that U42-A is enabled by a high on its control input, U42-13, and that U42-B and U42-C are both disabled, PRESTART (U18-4) goes high within 180 ns. of the rise of COMP.START (U31-13) and falls within 150 ns. of the fall of COMP.START. The high on COMP.START passes through a 4071 OR gate, U28-C, on its way to the Reset input of D-type flip-flop, U31-A. From the rise of the ØB (U31-11) that clocks COMP.START high, a maximum of 940 ns. may elapse before the Q output of the first flip-flop (U31-1), and thus the data input of the second flip-flop (U31-9), goes low. The fastest CLOCK that can be used by the system, as explained in Section VI-0, is 576 KHZ, which has a period of 1.736 us. Thus U31-9 is low in plenty of time to be clocked through to COMP.START on the next rise of ØB after the one that set COMP.START high. All this is done to assure that COMP.START and the START signal derived from it farther down the line are one CLOCK period wide, the apparently optimum START pulse width for the Reticon system.

PRESTART (U18-4 and L38-13) is the last of the inputs to the NAND gate, L38-B, to go high and the first to go low, so the

START/ pulse (L38-8) follows it by 20 ns., but in inverted form. Measured from the ØB that sets COMP.START high, START/ falls within 500 ns. of the rise of ØB and rises within 470 ns. of the next rise of ØB. START/ is inverted to form START, which sets the first scan underway. The first scan is different from other scans, however, because an SSt/ signal may not be generated. If BLANK goes high when power is turned on, SSt/ will be generated. However, BLANK usually stays low during power up and doesn't rise until the end of the first scan. This is the situation pictured on the timing diagram. The only problem caused by BLANK staying low is that PC (L35-5) and PCSYNC (L21-9) remain high, BLANKSET/ (L36-6) low, and BLANK GATE high, thus allowing through any PREGATE pulse that arrives after GATE4/ (L38-10) goes high whether scanning and processing are finished or not. In normal operation PROC.COMP. is not sent until scanning and processing are finished; thus PC and PCSYNC, which are cleared by SSt/ at the beginning of the scan, as we shall see, remain low until PROC.COMP. sets them high indicating a readiness for another START pulse to be sent.

The first scan is, therefore, most likely to be invalid, but the second scan is fine because BLANK goes high for the first time at the end of the first scan. From here on BLANK falls at the beginning of each scan and rises at the end of each scan. As will be seen in the discussion of the "A" memory address circuitry, SS (U51-9) is high for approximately the same time that CLOCK is low following the first rise of CLOCK after BLANK falls. SSt/, an inverted form of SS, falls 65 ns. max. after SS rises and rises 120 ns. max. after SS falls. Then, within 64 ns. after SSt/ falls, PC (L35-5) and PCSYNC (L21-9) fall and BLANKSET/ (L36-6) rises. Since BLANK/ (L61-4) is high during the scan, BLANK GATE (L38-12) is low. GATE4/ also is low during the gated part of the scan. No START/ pulses will be generated until PC (and thus PCSYNC), GATE4/, and BLANK GATE have all, once again, gone high. GATE4/ and BLANK GATE will go high at the end of the scan, PC when PROC.COMP. is sent following the end of processing for that

scan/process period, and PCSYNC following the first rise of CLOCK after PC goes high.

VI-2. STROBE0 (SH.'S 11, 10)

Much of the functioning of the interface boards is controlled by the computer via input and output ports. The input ports, 86H (MACR) and 88H (OUTRAN), bring information from the interface boards into the computer. The output ports - 80H, 81H, 82H, 83H, 85H, 87H, 89H, 8AH, 8BH, 8CH, and 8DH (see page 32) - carry information in the opposite direction, i.e., from the computer to the interface boards. As an example of output port functioning, let's look at port 80H operation.

The computer instruction - OUT 80H - causes the address 80H to be put on the multibus address lines (P1-52, 51, 54, 53, 56, 55, 58, and 57) in its negative true binary form and at the same time causes the data in the A register of the 8080A to be put on the multibus data lines (P1-68, 67, 70, 69, 72, 71, 74, and 73), also in negative true form. Thus the data and the address are valid on the multibus at the same time. From this time, a minimum of 50 ns. elapses before the command IOWC/ becomes active (low). Also, the data and address lines of the multibus remain stable a minimum of 50 ns. after IOWC/ goes away (high).

Details of the timing for BASE ADR/, READ, BOARD ENABLE/, and XACK/ are covered in the discussion of MACR generation, Section VI-10. Suffice it here simply to mention the results. BASE ADR/ falls within 58 ns. of when a valid address (i.e., its first hex digit is 8) is on the bus and rises within 58 ns. of when this address goes off the bus. In the generation of BOARD ENABLE/, IOWC/ plays the role played by IORC/ in MACR generation. This is correct because the signal of interest is the output of a two-input NAND gate (L33A-C) whose two inputs are IORC/ and IOWC/. Thus, BOARD ENABLE/ goes low 40 ns. max. after BASE ADR/ and IOWC/

are both low and high 40 ns. max. after either of these signals goes high. XACK/ goes low from between 796 and 931 ns. after IOWC/ goes low and rises 63 ns. after BASE ADR/ or IOWC/ rises. READ, however, remains low because one of the inputs to the NOR gate generating READ (L37-A), IORC/, remains high.

Because READ (pins 1 and 13 of L62 and L63) is low, information is passed through these two bus transceivers from A inputs to B outputs. Thus data on the multibus data lines passes through to the DOUT7-DOUT0 (J2-39, 38, 37, 36, 35, 34, 42, and 40) lines, which feed into the Data inputs of five 4508 latches (pins 4, 6, 8, 10, 16, 18, 20, and 22 of U9, U13, U37, U38, and U39), where they are stable within 18 ns. of the time they were stable on the bus. The data, however, will be strobed into only one of these latches, as we shall see.

Because we are dealing with port 80H, the second digit, 0, indicates which output of the L41, a 74154 4-line-to-16-line demultiplexer, will be enabled (low). (The 0 output of L41 is on pin 1, by the way. All other outputs of L41 will remain high.) L41-1 feeds into a NOR gate (L56-C), fed also by IOWC/. The output of this NOR gate, STROBE0 (L56-8), rises 20 ns. max. after IOWC/ and L41-1 are both low and falls 20 ns. max. after either (or both) of them goes high. Since the address and data remain on the bus a minimum of 50 ns. after IOWC/ goes away, STROBE0 goes away (low) before the data at the Data inputs of Register 0 goes away, thus assuring that the correct data was strobed into Register 0 (U37). None of the other four latches had this data strobed into them because they each require a different Strobe pulse for that purpose.

Once STROBE0 goes high, a maximum of 760 ns. may elapse before the desired data is at the outputs of Register 0. (Note that the Output Disable inputs of each of the five latches (U9, U13, U37, U38, and U39) are all tied low so that the outputs of these latches are enabled at all times.)

VI-3. PREGATE/DIG VID (SH.'S 2, 3, 1, 4)

To indicate the start of a new scan, BLANK (J2-43), which is sent out by the chosen Reticon's RC 100A board, goes low; it then stays low for the duration of the scan. BLANK feeds the data input of a 4013 D-type flip-flop (U50-5) whose Clock input (U50-3) is CLOCK (U18-2), whose Q output (U50-1) is SCAN/, and whose Q/ output (U50-2) is SCAN. Within 300 ns. of the first rise of CLOCK following the fall of BLANK, SCAN/ falls and SCAN rises. SCAN/ feeds the data input of another 4013 D-type flip-flop (U50-9), whose Clock input is again CLOCK and whose Q output (U50-13) is BLANK2X. BLANK2X falls within 300 ns. of the second rise of CLOCK following the fall of BLANK. Between the first rise and the second rise of CLOCK following the fall of BLANK, SCAN and BLANK2X, which are two of the inputs to U51-A, a 4073 three-input AND gate, are high and thus gate ØB through to the output where it appears as SS (U51-9). Because ØB is inverted by a 4069 inverter (U36-B), delayed 110 ns. max. by it, and then is delayed 110 or 140 ns. max. by a 4050 buffer/converter (U18-A) to form CLOCK, the fall of ØB occurs 250 ns. max. before the rise of CLOCK and the rise of ØB 220 ns. max. before the fall of CLOCK. The 4073 (U51-A) then delays the passage of the ØB a maximum of 250 ns. so that the positive SS pulse generated almost coincides, timewise, with the negative portion of CLOCK. Within 300 ns. of the second CLOCK rise, at which point SS falls, BLANK2X falls blocking the generation of any more SS pulses until the beginning of the next scan. It should be noted that at the end of the scan BLANK goes high, followed after the first CLOCK by SCAN/ (U50-1) and after the second CLOCK by BLANK2X. Thus BLANK, SCAN/, and BLANK2X are all high when the next scan starts.

Three 74LS191 synchronous 4-bit up/down counters (U58, U61, and U62) serve as photodiode address counters. Their outputs are loaded with zeros within 74 ns. of the fall of either RESET/

(L69-12) or of PROC.COMP./ (L69-2), both of which feed the Load inputs of the counters (pin 11 of U58, U61, and U62) via an AND gate (U70-C). Thus the counters are reset to zero before the start of a scan. They are not enabled for counting until their G inputs (pins 4) go low, which occurs within 110 ns. max. of the fall of SCAN/ or 410 ns. max. after the rise of the first CLOCK following the fall of BLANK. This is well before the arrival of the second CLOCK, (the fastest CLOCK used, 576 KHZ, having a period of 1.736 us), so the photodiode address counters start counting with the second CLOCK after BLANK falls. Since the counters' Down/Up inputs (pins 5) are tied to ground, the counters will only count up. This being the case, the first photodiode address will be 0, the second 1, and so forth. Counting will continue until SCAN/ rises, following the first CLOCK after BLANK rises.

The outputs of the photodiode address counters, PA11-PA0 (pins 7, 6, 2, and 3 of U58, U61, and U62), are stable 36 ns. max. after CLOCK rises. The upper eight bits of this photodiode address, PA11-PA4, are fed into the A inputs of two pair of 4063 4-bit magnitude comparators (U64 and U65; U66 and U67). U66 and U67 compare the upper eight bits of the photodiode address with L7-L0 (U39-5, 7, 9, 11, 17, 19, 21, and 23), the Start Gate address. If the photodiode address is larger than the Start Gate address, then U67-5, the A>B output, goes high. U64 and U65 compare the upper eight bits of the photodiode address with H7-H0 (U38-5, 7, 9, 11, 17, 19, 21, and 23), the End Gate address, and set U65-7, the A<B output, high if the photodiode address is smaller than the End Gate address. If U67-5 and U65-7 are both high, meaning the photodiode address is between the Start Gate and the End Gate, then the output of the AND gate into which they feed (U47-B), U65-7 via a 4050 buffer/converter (U68-C) and two 74LS04 delay inverters (U17-B and C) and U67-5 via a 4050 buffer/converter (U68-E), will go high. This sets one input to U47-C high. The other input to U47-C is high when either BLANK2X

(U50-13), via a 4050 buffer/converter, or SCANt/ (U68-10) is low forcing the output of the NAND gate into which they feed (U7-C) to go high. Thus PREGATE (U47-8) will go high when the photodiode address is between the Start Gate and the End Gate, as long as either SCANt/ (U68-10) or BLANK2X (U50-13) is low. This latter condition assures that PREGATE will go low at the end of each scan, regardless of whether the End Gate has been reached or not. The need for this will be seen later. At this point it should be noted, also, that the first seventeen photodiodes in the designated Gate area will not be seen, the first sixteen because only the upper eight bits of the photodiode address are considered in the generation of PREGATE and the seventeenth because the GATE opens one CLOCK late.

Turning to timing, from the rise of CLOCK that causes the photodiode address to fall between the Start Gate and the End Gate for the first time to the rise of PREGATE, a maximum of 2514 ns. may elapse. With any CLOCK slower than 397.77 KHZ, whose period is 2514 ns., PREGATE will go high before the next CLOCK rises. (With a faster CLOCK, PREGATE may not rise until after the next CLOCK rises, though the typical delay time is only 1257 ns., which is well within the period of the fastest CLOCK, 576 KHZ, whose period is 1.736 us.) A similar delay occurs between the rise of CLOCK and the fall of PREGATE resulting from that CLOCK, when the fall of PREGATE is due to the fall of U65-7. However, if PREGATE is set low by the rise of BLANK2X (which occurs one CLOCK later than the rise of SCANt/), this will happen 454 ns. after CLOCK rises.

PREGATE feeds the Data input of the first of four D-type flip-flops aboard a 74LS175, quadruple D-type flip-flops, (U43). RESET/ feeds the Clear input (43-1) causing the Q outputs - GATE1, GATE2, GATE3, and GATE4 (U43- 2, 7, 10, and 15) - to go low and the Q/ outputs - GATE1/, GATE2/, GATE3/, and GATE4/ (U43-3, 6, 11, and 14) - to go high within 35 ns. of the fall of RESET/. When PREGATE (U43-4) goes high, the Q output of the first flip-flop,

GATE1 (U43-2), follows PREGATE 30 ns. max. after the next rise of CLOCK. GATE2, GATE3, and GATE4 (U43-7, 10, and 15) follow GATE1 on the first, second, and third rises of CLOCK, respectively, thereafter. At this point it becomes apparent why PREGATE must fall at the end of the scan. EOS (U16-3), the output of an AND gate, (U16-A), fed by GATE3/ and GATE4, goes high within 24 ns. of the rise of GATE3/ and falls within 24 ns. of the fall of GATE4. If GATE3 and GATE4 don't fall, or if RESET/ arrives setting all the GATE's low simultaneously, then EOS is never generated and, consequently, neither is STROBE8 or STROBE9 (U16-6 and 8). Thus any operation triggered by one of these three signals, or by the falling edge of one of the GATE's, or by the rising edge of one of the GATE/'S never occurs.

Now that we've seen how the GATE's are generated, let's look at what happens to the video signal sent out by the Reticon 100A board. First of all, as many as three video signals may arrive at the interface board - VID3 (J1-38), VID2 (J1-40), VID1 (J1-32) from cameras 3, 2, and 1, respectively. They each enter one of the 4066 bilateral switches (L4-A, B, or C), but only the one from the camera designated will be allowed through. For proper functioning there can be a high on only one of the three camera designators - CAM3, CAM2, and CAM1 (U13 - 5, 7, and 9). These three designators enter input pins 13, 11, and 9 of a 4054 level shifter (L8), which converts them from signal swings of 0 to +5 volts to signal swings of -5 to +5 volts to match the signal swings on VID3, VID2, and VID1, and then sends them on to the control inputs (L4-13, 5, and 6) of the three bilateral switches into which VID3, VID2, and VID1 feed. The outputs of these switches (L4-2, 3, and 9) are wired together, so if more than one switch is enabled, the output, VIDEO, has a fight on its hands.

Assuming that only one video switch is enabled, VIDEO is the video signal from the designated camera. VIDEO passes, first of all, through an AGC (automatic gain control) circuit, starting at L2-1, that renders ANALOG VID (L10-15), a signal that swings

between 0 and +1 volt and thus falls in the range allowed for the Analog In input to the ADC-SH4B 4-bit A/D converter (U21). Conversions take place only during scan time, when BLANK is low and BLANK/ (U35-6), the Data input to a D-type flip-flop (U20-2), is high. While BLANK/ is high, START CONVERT, the Q output of the flip-flop (U20-5) rises within 25 ns. of the rise of QAA/, i.e., within 45 ns. of the fall of QAA. The rise of START CONVERT is inverted by inverter (U5-A) and delayed by it and by an AND gate (U70-D) on its way to Clear (U20-1) so that the START CONVERT signal falls between 20 ns. and 40 ns. after it rises, thus conforming to the 20 ns. min. - 40 ns. max. positive pulse width required by the ADC-SH4B for its Start Convert input (U21-6).

The analog to digital conversion takes a maximum of 400 ns. and occurs while CLOCK is low, i.e., from 45 ns. after QAA falls until 11 ns. after QEE falls. Depending upon when BLANK goes low in relationship to CLOCK, a conversion could occur before the first CLOCK after BLANK falls. Nevertheless, the first conversion of interest will be the one occurring when the first CLOCK, after BLANK falls, goes low.

The outputs of the ADC-SH4B converter (U21-9, 11, 13, and 15), which are valid from 11 ns. max. after QEE falls until the next QAA falls, are fed into the Data inputs of a 4042 quad clocked D latch (U3-4, 7, 13, and 14). The 4042 Clock (U3-5) follows the output of NAND gate U71-D and thus falls within 40 ns. of the fall of QFF and rises within 20 ns. of the fall of QHH. The Polarity input of the latch (U3-6) is tied low meaning that when the 4042 Clock is low the Q outputs - DI4, DI3, DI2, and DI1 (U3-2, 10, 11, and 1) - follow the inputs after a maximum delay of 220 ns. and that when the 4042 Clock rises data at the inputs is latched (until the 4042 Clock falls again). The latch outputs are valid within 450 ns. of the fall of the 4042 Clock and remain valid until the next 4042 Clock falls. Since A/D data from U21, which is valid at the inputs of U3 from 11 ns. after QEE falls until the next fall of QAA, is latched by the rise of the 4042

Clock, 20 ns. max. after QHH falls, (easily meeting the 50 ns. min. data setup requirement), the outputs of U3 - DI4, DI3, DI2, and DI1 - are valid from 490 ns. max. after the fall of QFF, or 56 ns. max. after the rise of the next QBB, until some time after the next QFF falls.

DI4, DI3, DI2, and DI1, the 4-bit digital video signal or A/D signal, enter a 4063 4-bit magnitude comparator (U8), where they are compared with a previously chosen 4-bit quantizing level. If the quantizing level is less than the 4-bit digital video signal value, then U8-7 (the A<B output) goes high; otherwise U8-7 is low. Thus U8 is the 1-bit digital version of the video signal. Since the propagation delay time for comparing inputs is 1250 ns. max, U8-7 is valid 1740 ns. max. after QFF falls (or by about the time the next QFF falls if a 576 KHZ CLOCK is used). U8-7 feeds the Data input of a D-type flip-flop (U20-12) that is clocked by QHH/. Thus 60 ns. max. after the next QHH falls the value of U8-7 is transferred to the Q output of the flip-flop as DIG VID (U20-9). As can be seen on the timing diagram, this transfer takes place at a time when the 4042 (U3) outputs could be changing, but when a change of state has not yet affected the 4063 (U8) outputs.

In sum, whatever ANALOG VID signal is present at the Analog In input of the ADC-SH4B 4-bit A/D converter when START CONVERT arrives will be available in 4-bit digital form at the outputs of the 4042 latch (U3) as DI4-DI1 from 56 ns. after the first rise of QBB after START CONVERT until the following fall of QFF and will be available in 1-bit digital form at the Q output of the U20-B flip-flop as DIG VID from 40 ns. after the second rise of QHH/ after START CONVERT until the first rise of QHH/ thereafter.

VI-4. A/D (SH.'S 4, 6, 9, 7, 8)

A/D mode stores the 4-bit digital video value generated by

the ADC-SH4B A/D converter (U21) for each photodiode in one of the eight 1822 memories (256-word by 4-bit LSI static random-access memories) occupying locations L25-L32. Since four memories are used at a time to record scan data and since memory address 0 is not used, a total of 255x4 or 1020 4-bit digital video values can be stored for one scan. There is no chance that data will be overwritten, except at the last memory address (# 255), since the memory address circuitry causes the memory address counters to stop counting when they reach 255 (the four memories used together being addressed together).

The 4-bit digital video signal is available at the outputs of the 4042 latch (U3) as DI4-DI1 from 56 ns. max. after QBB rises until QFF falls and at the same time is available at the data inputs of the four 4076 4-bit D-type registers (pins 14, 13, 12, and 11 of U30, U25, U12, and U26). For A/D mode operations to function, A/D (U9-19) must be high and the other three mode selectors - PIXEL (U9-17), TRAN (U9-21), AND STR.L. (U9-23) -low. As long as A/D is high, A/Dt/ (U35-4) is low, enabling the outputs of the four 4076's by setting their Output Disable inputs (pins 1 and 2 of U30, U25, U12, and U26) low. At any given time, however, only one of the 4076's has its data inputs enabled, which 4076 being determined by the outputs of U6, a 74LS195 4-bit parallel-access shift register. That 4076 whose Data inputs are enabled has the data DI4-DI1, transferred to its outputs by the rise of QEE, the clock for the 4076's. Since the data is available at the inputs of the 4076's from 56 ns. after the rise of QBB, i.e., 270 ns. before QEE rises, the 4076 data setup time of 200 ns. is satisfied.

When A/D mode is chosen, A/D is set high during the blanking period, i.e., long before BLANK falls and BLANK/ rises,so that A/Dt (U18-6), the Data input to U1, a D-type flip-flop, will be high when BLANK/ (35-6) goes high setting the Q/ output of the flip-flop (U1-6), and consequently the Shift/Load input of the 74LS195 shift register (U6-9), low. Shift/Load (U6-9) goes low

145 ns. max. after BLANK falls and rises 45 ns. max. after the 195 CLOCK (U6-10) rises; 195 CLOCK (U5-4), inverted, clears the D flip-flop (U1), setting its Q/ output (U1-6) and thus Shift/Load (U6-9) high. Thus Shift/Load stays low until the first 195 CLOCK pulse (U7-6) arrives and then goes high. 195 CLEAR (U6-1), on the other hand, goes low 89 ns. after BLANK rises and stays low until 144 ns. after BLANK falls. Thus 195 CLEAR goes away about the same time that Shift/Load goes low for loading. The only other time 195 CLEAR goes low is at the end of the scan, 44 ns. max. after GATE2/, GATE3, and QBB are all high, forcing the output of the NAND gate into which they feed (U32-A) to go low; 195 CLEAR then rises 44 ns. max. after any one of these three signals falls. 195 CLEAR goes away as Shift/Load goes low for load mode, but both occur a long time before 195 CLOCK rises to parallel load the outputs and then to set Shift/Load high for shift mode. 195 CLEAR is asynchronous and direct, but shifting and loading are synchronous and follow the positive transition of 195 CLOCK (U6-10).

Shortly after BLANK goes low, Shift/Load goes low and stays low until PREGATE goes high generating a positive 195 CLOCK transition that causes the data at the Parallel Data inputs - A, B, C, and D (U6-4, 5, 6, and 7) - to be loaded into their corresponding outputs - QA, QB, QC, and QD - (U6-15, 14, 13, and 12). QA (U6-15), which is loaded low, is inverted by U5-6 to form the G2 Data Disable input for 4076-A (U30-10). Since A/Dt/, which feeds the G1 Data Disable inputs of all four 4076's (pin 9 of U30, U25, U12, and U26), was set low before the scan began, both Data Disable inputs to 4076-A are low, enabling the data at its inputs to be clocked into the 4076 output register when QEE, the 4076 Clock input, rises. There may be a rise of QEE between the rise of PREGATE and the rise of GATE1, but the data gated through 4076-A will simply be replaced by that gated through by the QEE that rises between the rise of GATE1 and the rise of GATE2. 4076-A has its inputs enabled the entire time from the rise of

PREGATE until the rise of QBB following the rise of GATE2. As a result the last data clocked into 4076-A before its G2 input goes high disabling the inputs corresponds to the data from the first photodiode after the Start Gate.

The QB, QC, and QD outputs of the 74LS195, (U6-14, 13, and 12) are loaded low, so their inverted forms, (U5-8, 10, and 12), which feed the G2 Data Disable inputs of the other three 4076's (pin 10 of U25, U12, and U26), are high. Thus data will be blocked from being clocked into 4076-A, 4076-B, and 4076-C when QEE goes high.

When GATE2 rises, Shift/Load having gone high shortly after the rise of PREGATE clocked U6, the way is clear for QBB to clock serial shifts through U6. The J and K/ inputs (U6-2 and 3) are tied together so that the first stage of the shift register acts as a D-type flip-flop. QD (U6-12) feeds the J-K/ pair so that the four inputs loaded into the outputs in parallel fashion at the beginning of the scan form a closed ring that shifts sequentially through the outputs of U6 in the direction from QA to QD. This way there is always one of the outputs (QA, QB, QC, or QD) that is high and three that are low, and, consequently, one of the 4076's G2 Data Disable inputs that is low, enabling that 4076 to clock in data, and three that are high, disabling those 4076's from clocking in data. Once QBB rises, it takes 95 ns. max. for the chosen G2 to fall and 89 ns. max. for the other three G2's to rise. This enables the chosen 4076 235 ns. min. before QEE rises to clock in the data and allows 237 ns. min. for the other three 4076's to disable their inputs before QEE rises (the minimum data input disable setup time is only 180 ns. max.).

Data is ready at the 4076 data input positions (pins 15, 14, 13, and 12), at the latest, 56 ns. after QBB rises. This is 270 ns. before QEE, the 4076 Clock, rises, so the 4076's 200 ns. minimum data setup time requirement is met. The width of the CLOCK pulse, and therefore of the QEE pulse, depends on the CLOCK rate; the narrowest pulse is 868 ns. (corresponding to a CLOCK

rate of 576 KHZ), which generously meets the 4076's 120 ns. min. clock width requirement.

The data clocked into 4076-A arrives at the outputs - Q1, Q2, Q3, and Q4 (U30-3, 4, 5, and 6) 600 ns. max. after QEE rises and stays there until another QEE clocks data into this chip (four QEE clocks later).

The first QBB to rise after GATE2 rises causes a shift in the outputs of U6. QB (U6-14) is now high, while QA, QC, and QD (U6-15, 13, and 12) are low. Thus 4076-B has its data inputs enabled and so when QEE rises next the data at its inputs is clocked through to the outputs. The other three 4076's have their data inputs disabled.

The second QBB to rise after GATE2 rises causes another shift in the U6 outputs, resulting in data being clocked into 4076-C while the other three 4076's remain unchanged, their data inputs being disabled. Similarly, the third QBB enables 4076-D to receive data. At this point each of the 4076's is holding a 4-bit digital video signal value. Each 4076 sends its outputs to the Data inputs of a different pair of 1822 memories - the outputs of 4076-A feed the Data inputs of 1822 Memories A4 and B4; 4076-B feeds A3 and B3; 4076-C A2 and B2; and 4076-D A1 and B1. Since these eight 1822 memories all have their CS2 (chip select) inputs (pin 17) tied high, i.e., chip enable mode, the responsibility for enabling the proper memories for reading and writing at the proper times is left to the other chip select input, CS1/. During the write cycle, the CS1/ inputs of four memories are enabled at the same time. Thus the four 4-bit, or A/D, values at the outputs of the four 4076's can be, and are, loaded into four memories (either A4 (L25), A3 (L27), A2 (L29), and A1 (L31) or B4 (L26), B3 (L28), B2 (L30), and B1 (L32)) simultaneously.

When the memories are loaded is controlled by L52, a 74LS191 synchronous up/down counter, and its surrounding circuitry. The START/ pulse sent out to initiate each scan feeds into this 191's Load input (L52-11) within 24 ns. max. Since Load is

asynchronous, the Q outputs of the 191 (L52-7, 6, 2, and 3) go low 74 ns. max. after START/ goes low, and PIXAD (L51-3) falls 140 ns. max. after START/ falls (unless, of course, PIXAD is already low for other reasons). PIXAD feeds the Data input of a D-type flip-flop (L35-12), so when PIXAD goes low the next rise of QBB (arriving at L35-11) causes the Q/ output of the flip-flop (L35-8) to go high within 25 ns. max. and the Load input to the 191 (L52-11) to go high within 49 ns. (assuming that START/ is high). Q/ (L35-8) is high a minimum of 835 ns. before QCC rises and thus gates QCC through to the Clock input of the 191 (L52-14) 24 ns. max. later. No counting will occur until the G (enable) input (L52-4) goes low. The Down/Up input (L52-5) is tied low, so the counter will only count up when it is enabled.

The G input (L52-4) is controlled by the Q output of a D-type flip-flop (L70-9). When a RESET/ pulse is sent out by the computer, it presets the flip-flop (via L70-10) causing the Q output (L70-9) and thus the G input (L52-4) to go high disabling counting. Q and G will go low following the first rise of QEE, which clocks the flip-flop via L70-11, after both A/Dt and GATE1 are high. A/Dt, which is just a buffered version of A/D, goes high just after A/D is set high before the scan begins, so the Data input to the flip-flop (L70-12) follows the inverse of GATE1 by 44 ns. max., or the rise of CLOCK (causing a change of state in GATE1) by 74 ns. max., plenty of time before QEE rises. The rise of QCC immediately following the rise of GATE1 does not clock the 191 counter (L52) because the counter isn't enabled until after the rise of QEE. Thus the counter, in fact, enables the QCC's that occur while GATE2 is high. Once GATE1 falls, the next QCC gets through to the 191 Clock (L52-14) and then QEE rises and disables the 191 counter (L52).

Counting, for A/D mode, is monitored by a three-input AND gate (L53-B). One input, L53-5, is held high as long as A/Dt is high. The other two inputs (L53-3 and 4) go high when QC and QB (L52-6 and 2) go high. This happens when the count of 3 is

reached. At that time the output of the AND gate (L53-6) goes high making one input of the XOR gate (L51-2) high. The other input to the XOR gate (L51-1) is held low because PIXELt (L24-6), one of the inputs to the AND gate L19-C, is low causing the output of that AND gate (L19-8) to be low causing, in turn, the output of the AND gate into which it feeds (L19-11) to be low and thus also L51-1. If, through some error, PIXELt were high, L51-1 would still be held low because QA and QD (L52-3 and 7) would be low forcing the outputs of the AND gates into which they feed, L53-12 and L19-8, to be low, thus forcing the next AND gate to have a low output, L19-11. L19-11 feeds L51-1. Thus L51-1 is low and L51-2 is high, causing PIXAD (L51-3) to go high, this happening within 101 ns. of the rise of the QCC that clocked the 191 counter, L52, to 3, i.e., just before the rise of QDD.

PIXAD feeds the Data input of D-type flip-flop L35-12 which is clocked via L35-11 by the rise of QBB. Since PIXAD, at this time, is high, the Q/ output (L35-8) goes low enabling the 191 Load input (L52-11), which causes zeros to be loaded into the 191 outputs, QA-QD (L52-3, 2, 6, and 7), resulting in PIXAD going low within 141 ns. of the rise of QBB, and blocking the passage of QCC to the 191 Clock input (L52-14). Q/ (L35-8) remains low, even though PIXAD has gone low, until the next QBB arrives at L35-11 to gate the low through to Q (L35-9) and thus a high to Q/ (L35-8). Q/ (L35-8) goes high within 25 ns. of the rise of QBB, thus opening the gate for the next QCC to pass through to the 191 Clock input (L52-14).

While PIXAD is high, which lasts, approximately, from the rise of QDD to the rise of the next QBB, the memory address counters are advanced and the four 4-bit digital video values stored in memory. TRANSAD (L51-4) will be low during any scans done in PIXEL or A/D mode, unless the STR. L. or the TRAN selector bit (U9-23 and 21) were somehow set high. If TRANSAD (L51-4) and PIXAD (L51-5) were both high, then the output of the XOR gate whose inputs they feed would go low blocking any writing into

memory. Assuming, however, that TRANSAD is low, when PIXAD goes high, L51-6 goes high enabling the MADCLKW/ and WRITE/ pulses to be generated. MADCLKW/ falls 20 ns. max. after QEE rises and rises 40 ns. max. after QFF rises. MADCLKW/ is delayed 18 ns. on its way to the Count Up input of the appropriate memory address counter, let's say L65-5. The outputs of the cascaded 74LS193 4-bit synchronous counters (pins 7, 6, 2, and 3 of L49 and L65) are valid 73 ns. max. after the Count Up input (L65-5) rises. (The Count Down inputs (L65-4 and L49-4) are tied high because in order for one Count input to count the other must be high.)

The eight outputs of the "A" memory address counters - AA7-AA0 (pins 7, 6, 2, and 3 of L49 and L65) - feed into the eight address inputs of the four "A" memories - A7-A0 (pins 7, 6, 5, 21, 1, 2, 3, and 4 of L25, L27, L29, and L31). These address lines are stable 131 ns. after QFF rises and remain so until just after the next QFF rises.

Meanwhile, the WRITE/ pulse (L50-12) falls within 40 ns. of the fall of QCC and rises within 20 ns. of the fall of QFF. The 74LS257 quad 2-line-to-1-line data selector, L43, delays WRITE/ by 18 ns. and sends it as R/WA to the R/W inputs of the "A" memories (pin 20 of L25, L27, L29, and L31) forcing these R/W inputs to go low 58 ns. max. after QCC falls and high 38 ns. max. after QFF falls (when PIXAD is high). Thus, these R/W's fall at least 450 ns. after the memory address lines are stable, amply satisfying the 200 ns. min. address setup time; stay low for at least 305 ns., satisfying the 250 ns. min. write pulse width; and rise at least 800 ns. before the address lines become unstable, most generously satisfying the 50 ns. min write recovery time - all these being requirements of the 1822 memories.

Thus the overall function of the 73LS191 counter, L52, and its circuitry, for A/D mode operation, is to count "0, 1, 2, 3, 0, 1, 2, 3,..." and load data into memory on the count of 3 , which occurs every fourth count. The outputs of 4076-D, the fourth latch to be loaded, are valid 58 ns. max. after QBB rises,

which leaves 51 ns. min. before QCC rises and thus 51 to 109 ns. before R/W falls. The outputs of 4076-A, 4076-B, and 4076-C become valid three, two, and one CLOCK periods, respectively, before those of the 4076-D. Thus, by the time that R/WA falls, valid data will have been at the Data inputs of all four "A" memories (pins 15, 13, 11, and 9 of L25, L27, L29, and L31) at least 51 ns. and will remain there until about 720 ns. after R/WA rises. Since R/WA is at least 305 ns. wide, the data is at the inputs for at least 356 ns. before R/WA rises, more than satisfying the 250 ns. min. data-in-width-effective of the 1822 memories. R/WA rises about 720 ns. before the data goes unstable at the Data inputs of the 1822's, thus satisfying the 50 ns. min. data-in-hold time required by the 1822's.

Looking at the timing diagram, one can see that the outputs of 4076-A become valid during the latter half of the period during which the count at the outputs of the 191 (L52) is 0, outputs of 4076-B during count 1, and the outputs of 4076-C and 4076-D during count 2 and count 3, respectively. It is during the latter part of the count 3 period that the four 4076's have their data recorded in memory.

VI-5. PIXEL (SH.'S 4, 6, 7)

From the discussion of PREGATE and DIG VID generation, we know that the analog video signal present at the Analog In input of the ADC-SH4B 4-bit A/D converter (U21-31) when the START CONVERT pulse arrives at the Start Convert input (U21-6) is available as DIG VID (U20-9) following the second rise of QHH/ after that same START CONVERT pulse. DIG VID is fed into the Data input (U11-2) of one of two cascaded 4094 8-stage shift-and-store bus registers (U11 and U10). These registers operate when PIXEL (U9-17), the selector bit for pixel mode, is high. The Strobe and Output Enable inputs of the two 4094's (pins 1 and 15 of U10 and

U11) are tied to PIXEL. Each of the eight stages of a 4094 serial shift register has a storage latch associated with it. When the Strobe input of a 4094 is high, as in pixel mode, data in each shift register stage is transferred to its associated storage register location. When the Output Enable input of a 4094 is high, data in the storage register appears at the outputs of the 4094. When both the Strobe and the Output Enable inputs are high, the outputs of the 4094 follow the shift register data, after a delay.

Shifting takes place in the two 4094's (U10 and U11) only when GATE2, one of the inputs to NAND gate (U7-A), is high, allowing the rise of the other input to the NAND gate, QBB, (which is inverted by the NAND gate and then reinverted by an inverter (U52-F)), to reach the Clock inputs of the 4094's (pin 3 of U10 and U11) within a maximum delay of 40 ns. Once the 4094 Clock, QBB delayed, rises, the shifted data appears at the Q outputs of the 4094's (pins 4, 5, 6, 7, 14, 13, 12, and 11 of U10 and U11) within 840 ns., i.e., by 880 ns. max. after QBB rises or, at the latest, 12 ns. after the first subsequent fall of QBB.

The Serial output of the lower order shift register (U11-9) feeds the Data input of the upper order shift register (U10-2), thus cascading the two registers to make, in effect, one 16-bit shift register. After sixteen shifts of these two registers, the sixteen data bits at their outputs, i.e., the 1-bit digital video values of sixteen consecutive photodiodes, are loaded into memory. The 74LS191 synchronous counter (L52) and its support circuitry govern the loading of the 1822 memories for pixel mode in much the same way as they do for A/D mode, as described earlier, but with two major differences. First, the G enable input (L52-4) goes low 40 ns. max. after QEE rises following the rise of GATE2 (PIXEL having been set high between scans) and rises 25 ns. max. after QEE rises following the fall of GATE2. Thus the QCC pulses that in fact clock the 191 counter (L52) are those appearing while GATE3 is high. Second, PIXAD (L51-3) goes high when the count of

15 is reached by the 191 counter, instead of the count of 3. When the count of 15 is reached, QD, QC, and QB (L52-7, 6, and 2) are high setting the inputs of the three-input AND gate (L53-1, 2, and 13) and thus also the output of that AND gate (L53-12) high. QA (L52-3) and PIXELt (L24-6) are also high setting the inputs to the two-input AND gate (L19-9 and 10) high and, subsequently, also the output (L19-8). At this point the inputs to the next stage two-input AND gate (L19-12 and 13) are high causing the output (L19-11) to go high and thus also one input to the XOR gate (L51-1). The other input to the XOR gate (L51-2) is low because the AND gate feeding into it, L53-B, is held low by one of its inputs, A/Dt, which must be low while PIXEL is high, in order for the system to function properly in pixel mode.

As can be seen on the timing diagram, PIXAD goes high shortly after the count of 15 is clocked into the outputs of the 191 counter L52, just as it went high after the count of 3 was reached in A/D mode. As seen before in the A/D mode discussion, the next rise of QBB transfers the high on PIXAD from the Data input (L35-12) to the Q output (L35-9) of a D-type flip-flop. Thus the Q/ output (L35-8) goes low causing the Load input to the counter (L52-11) to go low, forcing the loading of zeros into the Q outputs of the counter (L52-7, 6, 2, and 3) and the blocking of the next QCC pulse from reaching the counter's Clock input (L52-14). The load operation causes PIXAD to go low so that at the next rise of QBB, Q/ (L35-8) will go high removing the load enable and reopening the gate through which QCC must pass to reach the counter Clock input (L52-14). As a result of all this, the counter (L52) counts "0, 1, ... , 15, 0, 1,..., 15,..." for as long as it is enabled.

The clocking of the memory address counters and the generation of the R/W pulses to cause data to be written into the 1822 memories is the same as for A/D mode, i.e., happening only when PIXAD is high. The L52 circuitry starts and ends operation one clock period later for pixel mode than it does for A/D mode

because DIG VID is ready approximately one clock period later than the corresponding 4-bit digital video signal data coming out of the 4042 (U3).

Data is ready at the outputs of the 4094's, (pins 4, 5, 6, 7, 14, 13, 12, and 11 of U11 and U10), and thus at the Data inputs of the 1822 memories, 12 ns. after the fall of QBB, at the latest. R/W falls 58 ns. max. after QCC falls and rises 38 ns. max. after QFF falls. The data-in-width-effective extends, at the least, from 12 ns. after QBB falls until QFF falls, which is about 314 ns., and meets the minimum of 250 ns. required by the 1822's. The data becomes unstable after QBB rises, meaning it is stable around 400 ns. after the R/W pulse goes away and therefore satisfies the 1822's 50 ns. min. data-in-hold time.

VI-6. AND VI-7. STRING LENGTH AND TRANSITION MODES

(SH.'S 4, 10, 5, 7, 9)

In order for string length data to be recorded, Status Control Register U9 must be loaded with STR.L. (U9-23) high and PIXEL, A/D, and TRAN (U9-17, 19, and 21) low. When the START/ pulse (L38-8) is generated, it enters one input of a two-input AND gate (U47-12) causing the output, TRCLEAR (U47-11), and thus the Clear input to a D-type flip-flop (U34-13) to go low. As a result, the Q output of this flip-flop, TRANSITION (U34-9), goes low within 64 ns. after START/ goes low; TRANSAD (U72-6), the output of an AND gate fed by TRANSITION, follows TRANSITION low by 24 ns., feeds into an AND gate (U72-A) causing its output (U72-12) to go low within 24 ns. and within another 110 ns. the delayed, buffered version, STROBE (U68-4), which feeds the Strobe inputs of two 4508 latches (pins 2 and 14 of U40 and U41), to go low. The low on TRANSAD feeds into another AND gate (U70-B) causing its output (U70-6) to go low and SLOAD1, the output of the following NAND gate (U71-6) to go high. The low on TRANSAD feeds into another NAND gate (U71-A) setting its output (U71-3) high within

20 ns. and within another 140 ns. setting its delayed, buffered version, OD (U68-2), which feeds the Output Disable inputs of the two 4508's (pins 3 and 15 of U40 and U41), high. The START/ pulse passes through another AND gate (U72-C) setting its output, 191 LOAD (U72-8), low and thus also the Load inputs of three 74LS191 synchronous counters (pin 11 of U46, U69, and U57). As a result, the Q outputs of these counters (pins 3, 2, 6, and 7 of U46, U69, and U57) are all low within 74 ns. of the fall of START/.

DIG VID (U20-9) is the signal used to generate string length data. When DIG VID changes state, it does so between the rise of QHH/ and 40 ns. thereafter. It feeds into (U34-2), the Data input of a D-type flip-flop, and is settled at least 157 ns. before QBB (U34-3) rises to clock it through to the Q output (U34-5) as STORE VID/. DIG VID and STORE VID/ are the two inputs to an XOR gate (U56-1 and 2). As long as they are in the same state, the output of the XOR gate, TRCLK (U56-3), is low. However, when DIG VID changes state, making it and STORE VID/ of opposite states, TRCLK, which feeds the Clock input of a D-type flip-flop (U34-11), goes high clocking the high at the flip-flop's Data input (U34-12) through to its output, TRANSITION (U34-9), within 102 ns. of that fall of QHH that clocked the change of state into DIG VID. TRCLK remains high, for sure, from 17 ns. max. after DIG VID changes state, (or 77 ns. max. after QHH falls) until STORE VID/ changes state to agree with DIG VID, 40 ns. max. after QBB rises. Therefore TRCLK is a minimum of 130 ns. wide, which is greater than the 25 ns. min. Clock pulse width required by the 74LS74 flip-flop (U34).

TRANSITION is cleared by a low on TRCLEAR, which feeds the Clear input of the flip-flop (U34-13). TRCLEAR goes low 24 ns. max. after START/ falls. It also goes low 64 ns. max. after QFF falls and high again 44 ns. max. after QGG falls. Thus TRANSITION falls 64 ns. max. after START/ falls and 104 ns. max. after QFF falls.

TRANSITION rises 102 ns. max. after QHH falls, which could be

before or after CLOCK (U18-2) rises. GATE3 rises 30 ns. max. after CLOCK rises. TRANSITION and GATE3 rise at about the same time and feed into two inputs (U72-3 and 4) of a three-input AND gate (U72-B). The third input (U72-5) is fed by the output of an XOR gate (U56-6) which is high if either STR.L. (U9-23) or TRAN (U9-21), but not both of them, is high. Assuming U56-6 is high (having been set so before the scan began), TRANSAD (U72-6), the output of the three-input AND gate, goes high within 24 ns. after both TRANSITION and GATE3 have gone high, which will be, at the latest, by 54 ns. after QAA rises.

TRANSAD, in its high state, gates through the signals causing the 1822 memories to be written into. First of all, as mentioned before, TRANSAD is inverted by a NAND gate (U71-A) and delayed by a 4050 buffer/converter (U68-A) to form OD, which feeds the Output Disable inputs of two 4508's (pins 3 and 15 of U40 and U41). As a result, OD goes low within 160 ns. of the rise of TRANSAD and high within 160 ns. of the fall of TRANSAD. Data is available at the outputs of these 4508's from 180 ns. max. after OD falls until 180 ns. max. after OD rises, or from 340 ns. max. after TRANSAD rises until 340 ns. max. after TRANSAD falls. Thus the outputs of the 4508's are enabled from 466 ns. max. after QHH falls until 468 ns. max. after QFF falls.

Secondly, when TRANSAD is high it enables the AND gate (U72-A) to go high from 24 ns. max. after QCC rises until 44 ns. max. after QEE rises. The output of U72-A, as pointed out earlier, passes through a 4050 buffer/converter (U68-B) to form STROBE, which feeds the Strobe inputs of the two 4508's (pins 2 and 14 of U40 and U41). STROBE goes high 164 ns. max. after QCC rises and falls 184 ns. max. after QEE rises. Thus STROBE is approximately 237 ns. wide, satisfying the 140 ns. minimum Strobe pulse width required by the 4508's. The delay time from Strobe to the outputs of the 4508's is 260 ns. max. Therefore, strobed data is at the outputs of the 4508's by 424 ns. after QCC rises, i.e., by 10 ns. before QGG rises.

The data feeding the Data inputs of the 4508's (pins 4, 6, 8, 10, 16, 18, 20, and 22 of U40 and U41) are available from the outputs of the 74LS191 counters (pins 7, 6, 2, and 3 of U46, U69, and U57) within 36 ns. of the rise of CLOCK, which causes these counters to count, as long as 191 LOAD (U72-8) is high and the G input(s) (pin 4 of U46, U69, and U57) low. The Down/Up inputs (pin 5 of U46, U69, and U57) are tied low so that the counters only count up.

Thirdly, a high on TRANSAD enables a NAND gate (U71-B) that controls the loading of the counters (U46, U69, and U57). When TRANSAD and STR. L. are both high, SLOAD1, the output of NAND gate (U71-B) goes low 88 ns. max. after QAA falls and stays low until 68 ns. max. after QDD falls. SLOAD2, the output of NAND gate U71-C, goes low within 20 ns. max. of the rise of GATE2/ and stays low until 20 ns. max. after GATE2/ falls (assuming STR.L. is high). SLOAD2 is low mostly during non-scan time and overlaps SLOAD1 only when SLOAD1 occurs between the fall of GATE2 and the fall of GATE3. The START/ pulse occurs before the scan begins, so when SLOAD1 goes low, the other two inputs to the AND gate (U72-C), with the one exception just mentioned, are high. Thus, while GATE2 is high, loading of the counters (U46, U69, and U57) is controlled by SLOAD1. It takes a maximum of 50 ns. from the time that 191 LOAD (U72-8), which feeds the Load inputs of the counters (pin 11 of U46, U69, and U57), goes low until the Q outputs (pins 3, 2, 6, and 7 of U46, U69, and U57) are valid. The Q outputs are in flux from some time after the fall of QAA until 162 ns. max. after QAA falls. 191 LOAD stays low until after QDD falls, so since no CLOCK's arrive while 191 LOAD is low (and GATE2 high), the Q outputs of the three 191 counters (and thus the Data inputs of the 4508's) are stable from 162 ns. max. after QAA falls until the next CLOCK rises.

During a CLOCK period in which TRANSITION goes high, the data to be written into the 1822 memories is valid at the Q outputs of U46, U69, and U57 and thus at the Data inputs of the latches (U40

and U41) from 36 ns. max. after CLOCK rises until shortly after QAA falls. The STROBE pulse arrives 164 ns. max. after QCC rises and falls 184 ns. max. after QEE rises. Thus the data to be strobed into the 4508's is at their Data inputs over 380 ns. before STROBE arrives (the required data setup time for the 4508's is only 50 ns.) and stays until about 250 ns. after STROBE goes low (no hold time is required by the 4508's). Thus, correct data is strobed into the U40 and U41, and that data remains stable until the next STROBE pulse arrives. (See Fig. VI-7.)

Fourthly, when TRANSAD goes high, it sets the output of the XOR gate, L51-B, high, (assuming that PIXAD is low, as it should be during string length mode operations), enabling the generation of MADCLKW/ (L71-8) and of WRITE/ (L50-12). L51-6 goes high 17 ns. max. after TRANSAD goes high, or, at the latest, by 71 ns. after QAA rises, and stays high until 17 ns. after TRANSAD goes low, or, at the latest, by 37 ns. after QGG falls. Thus L51-6 is high, approximately, from the rise of QBB to the fall of QGG and thus is high when needed to gate through the signals that generate MADCLKW/ (from the rise of QEE to the rise of QFF) and the signals that generate WRITE/ (from the fall of QCC to the fall of QFF). In the discussion of A/D mode, it is shown that, when L51-6 is high, the address lines of the appropriate 1822 memories are stable from 131 ns. max. after QFF rises until the next rise of QFF, and the R/W pulse goes low from 58 ns. after QCC falls until 38 ns. max. after QFF falls. Valid data is at the 1822 Data inputs from the 4508 latches (U40 and U41), at the latest, by 10 ns. before QGG rises. The 4508 outputs are enabled from 466 ns. after QHH falls until 468 ns. after QFF falls, i.e., from 32 ns. after QDD rises, at the latest, until 34 ns. after QBB rises, at the latest. Thus the data at the 1822 Data inputs is valid from the rise of QGG until the next rise of QBB, so it is valid at least 760 ns. before R/W falls (thus meeting the 250 ns. minimum data-in-width-effective time required by the 1822's) and remains valid about 400 ns. after R/W rises (thus meeting the 1822's 50

ns. minimum data-in-hold time requirement).

So, in string length data mode, the synchronous counters - U46, U69, and U57 - are loaded with 0's at the start of a scan. After GATE2 goes high the counters start counting, using the same CLOCK as the photodiode address counters (U58, U61, and U62). U46, U69 and U57 are delayed in starting to count so that the DIG VID signal being acted upon corresponds to the same photodiode as does the count in these three counters. When DIG VID changes state, it sets in motion the machinery to record the 12-bit count in the counters (U46, U69, and U57), along with a 2-bit camera number, STORE VID (1 bit indicating the state of the data of the string), and MEMA (1 bit indicating which memory bank - "A" or "B" - is being written into). STORE VID is used because by the time the information is strobed into the latches, U40 and U41, the new value of DIG VID is already transferred to STORE VID/, making STORE VID match the state of the string length data being recorded. The counters (U46, U69, and U57) are loaded with 0's so that the first CLOCK (once the counters are enabled) counts 1; this way, if a transition occurs during the first CLOCK period following a load, the string length recorded is 1, as it should be. This makes possible a resolution of 1 photodiode, which would be needed if DIG VID were to change state each CLOCK period, in which case a whole series of 1's would be recorded for the string lengths. The other three bits of information stored for string length data mode - the camera number, a 2 bit number specifying which camera is being used (U40-4 and 6 coming from U28-3 and 4, respectively) and MEMA (U40-10 from L20-8 via J2-5) - are set before the scan and don't change during the scan.

TRAN mode (transition mode) functions the same way that STR.L mode (string length mode) does, with the exception that the counters (U46, U69, and U57) are not reloaded with zeroes every time a transition occurs. Instead, they are loaded with zeroes only at the start of a scan and then start counting as soon as BLANK2X falls. This way they contain the photodiode address for

the current DIG VID signal so that when a transition occurs the address stored is that of the first photodiode in the new group, i.e., the address of the first photodiode after the transition itself. The other four data bits, indicating the camera selection and the states of STORE VID and of MEMA, are the same as for string length data mode.

VI-8. "A" MEMORY ADDRESS CIRCUITRY (SH.'S 11, 7, 8, 2, 3, 10, 9)

The timing diagram shows three scan/process periods, i.e., the time between two successive PROC.COMP. signals sent out by the computer, and part of a fourth period, taken from the midst of many scans. The rising edge of PROC.COMP. feeds L20-11, the Clock input to a D flip-flop, clocking MEMA (L20-8), which is also the Data input (L20-12), into MEMB (L20-9), thus causing MEMA and MEMB to switch states. The first PROC.COMP. on the timing diagram sets MEMA high and MEMB low, in which case the "A" memories will be written into during the first period shown.

When PROC.COMP. rises, it also causes the "A" memory address counters - L49 and L65 (two 74LS193 synchronous 4-bit up/down counters) - to be cleared via pin 14 of these counters. The Q outputs of these counters (pins 3,2,6, and 7 of L49 and L65) are all low within 35 ns. of the rise of PROC.COMP. Meanwhile PROC.COMP./ falls enabling the Preset input of the L44-B flip-flop to set its output (L44-9) high, thus removing the low from the Load inputs of the "A" memory address counters (pin 11 of L49 and L65).

Next, the computer sends out an OUTRAN pulse (L54-12), which feeds into a NAND gate, L67-B. The other input to this NAND gate, MEMB (L20-9), is low at this time, so the output L67-6, and consequently the Output Disable inputs to the 4508 dual 4-bit latch (L47-3 and 15) remain high disabling the outputs of the L47 latch.

The START pulse, sent to the Reticon some time after the PROC.COMP. signal has set things up for a new scan, is not shown on the timing diagram, but its existence is implied by the lows on the BLANK signal. Once BLANK goes low, the positive portion of ØB (U48-3) occurring soonest after the first CLOCK rises is gated through a 4073 three-input AND gate, U51-A, to generate the SS pulse, U51-9. Because ØB rises 220 ns. before CLOCK falls and falls 250 ns. before CLOCK rises and because U51-A can have a maximum delay of 250 ns. SS coincides, approximately, with the negative portion of CLOCK. SS and MEMA (L20-8) are the inputs to a 4081 two-input AND gate, L68-B, whose output, L68-4, feeds the Reset inputs of a 4508 latch (L47-pins 1 and 13). Since MEMA is already high, L68-4 and the Reset inputs follow SS. The outputs of the latch (L47-5, 7, 9, 11, 17, 19, 21, and 23) are low within 430 ns. of the rise of SS (or of the fall of CLOCK).

Now that the outputs of the "A" memory address counters (pins 3,2,6, and 7 of L49 and L65) and the outputs of the dual 4-bit latch (pins 5, 7, 9, 11, 17, 19, 21, and 23 of L47) are all low, all is ready for scanning. COUNT A (L43-4) causes the lower order counter (L65) to count up via L65-5, the Count Up input. The Count Down inputs (pin 4 of L49 and L65) are tied high because the Count Up pulses can cause the counters to count only if the Count Down inputs are high. The Carry output, pin 12, of counter L65 feeds the Count Up input, pin 5, of counter L49, thus cascading L49 into L65. (The Carry output produces a pulse equal in width to the Count Up input of its own counter when an overflow condition exists.) With MEMB low, the Select input to a 74LS257 quad 2-line-to-1-line data selector (L43-1) is low causing the A inputs to be passed through to the outputs. Thus COUNT A (L43-4) follows MADCLKW/ (L71-8), rising 38 ns. max. after QFF rises and falls 38 ns. max. after QEE falls. The counter outputs (pins 3,2,6, and 7 of L49 and L65) are stable within 73 ns. of the rise of COUNT A, which feeds L65-5, and thus within 111 ns. of the rise of QFF , and stay stable until just after the next QFF rises.

On the timing diagram COUNT A (L65-5) receives only one pulse, but it could receive as many as occur while the gate for the particular mode in use is high. Within 30 ns. of the third rise of CLOCK after PREGATE (U47-8) falls, GATE3 (U43-10) falls. EOS/ (U17-2) falls 44 ns. max. after GATE3 falls and rises one period later, i.e., 44 ns. max. after GATE4 (U43-15) falls. When MEMA (U16-4) is high, STROBE8 (U16-6) goes high as EOS/ (U17-2) goes low. STROBE8 feeds the Strobe inputs of the dual 4-bit latch (pins 2 and 14 of L47). Data is at the outputs of the latch (L47-5, 7, 9, 11, 17, 19, 21, and 23) within 260 ns. of the rise of STROBE8. The data latched in is the last "A" memory address into which data was written during that particular scan.

Nothing else happens until the computer sends out another PROC.COMP. signal. As before, the outputs of the "A" memory address counters (pins 3,2,6, and 7 of L49 and L65) are low within 35 ns. of the rise of PROC.COMP. (L54-6 and pin 14 of L49 and L65) and the memories switched within 40 ns. Now MEMA (L68-5) is low, so the SS signal generated at the beginning of the scan is blocked from passing through the AND gate (L68-B) to reset the dual 4-bit latch (L47). (Instead SS is passed through L68-A to reset the latch connected to the "B" memory address counters - L48.) MEMB (L67-4) is high, though, so when OUTRAN (L67-5) is sent out from the computer, the NAND gate, L67-B, will go low enabling the outputs of the L47 latch via the Output Disable inputs (pins 3 and 15 of L47). The latch outputs are still holding the last memory address written into during the previous scan, so this is the data that appears at the outputs of the latch (L47-5, 7, 9, 11, 17, 19, 21, and 23) within 200 ns. of the rise of OUTRAN (L54-12) and on the data lines of the multibus (P1-68, 67, 70, 69, 72, 71, 74, and 73) within 395 ns. of the rise of OUTRAN. OUTRAN (L54-12) goes high approximately 120 ns. after the multibus address lines (P1-57, 58, 55, 56, 53, 54, 51, and 52) are stable (the same timing as described for MACR generation - Section VI-10). Thus the data (the last memory address written into) is valid on the

multibus data lines from 515 ns. max. after the multibus address lines are stable (with, of course, the proper address to generate OUTRAN) until just after IORC/ (P1-21 and L37-1) rises, i.e., when READ (L37-12) falls blocking the passage of data through the 74LS242 bus transceivers (L62 and L63) onto the data bus lines.

In order to move the data stored in the "A" memories (L25, L27, L29, and L31) during the last scan to the SBC 80/20 memory, the computer must send two MACR read signals (L54-8) for every memory address filled, i.e., twice as many MACR signals as the number of memory locations filled, this number having been read when the OUTRAN pulse was sent out. No adjustment of this number is necessary because the first address used was 1, not 0, in which case the address of the last location filled equals the total number of memory locations filled.

Within 21 ns. of the rise of MEMB (L43-1), COUNT A (L43-4) starts following 43SEL (L43-3 from L20-5) and thus goes low. Because only address 01 of the "A" memories was written into during the last scan, OUTRAN read 01 and thus the computer will send two MACR pulses to read the data stored in location 01 of the A4, A3, A2, and A1 memories (L25, L27, L29, and L31). As described in MACR generation, the first MACR pulse (L20-3 from L54-8) sets 43SEL (L20-5 and L43-3) high and thus pulses the lower order address counter (L65) setting the "A" memory address counters to 01. Since 43SEL is high, the data in location 01 of the A4 and A3 memories (L25 and L27) is read. The second MACR pulse sets 43SEL low and 21SEL (L70-5) high. Because 43SEL undergoes a negative transition, instead of the positive transition needed to advance the counters, the second MACR pulse doesn't advance the counters, L49 and L65; what it does is cause the data in location 01 of the other two "A" memories, A2 and A1 (L29 and L31), to be read and put out onto the data bus.

The next PROC.COMP. sent out again switches the memories so that MEMA (L20-8) is high and MEMB (L20-9) low and clears the outputs of the memory address counters (pins 3,2,6,and 7 of L49

and L65). MEMB (L67-4) is low,so OUTRAN (L67-5) doesn't affect the "A" memory address circuitry; MEMA, on the other hand, is high, so SS (L68-6) is passed through L68-B to reset the latch outputs (L47-5, 7, 9, 11, 17, 19, 21, and 23) low. This scan/process period, the third one shown on the timing diagram, is like the first, except that it shows what happens when the counters (L49 and L65) reach their maximum count of 255 (FF in hexadecimal).

When all of the Q outputs of the counters (pins 3, 2, 6, and 7 of L49 and L65) are high, meaning the count of 255 (FF in hex) has been reached, the Carry output (L49-12) sends out a pulse equal in width to the Count Up input of that same counter, (L49-5), (which is also equal in width to the Count Up input (L65-5) of the lower order counter). This Carry output (L49-12) feeds the Clock input of a D flip-flop (L44-11); its rising edge causes the Q output (L44-9) to go low within 40 ns. and likewise the Load inputs to the two counters (pin 11 of L49 and L65). These Load inputs remain low from 40 ns. max. after Carry (L49-12) rises until the next PROC.COMP. signal is sent out by the computer. Within 40 ns. of when these Load inputs go low, the Q outputs (pins 3, 2, 6, and 7 of L49 and L65) are loaded with ones. Load , for the 74LS193's, is independent of the count pulses, so any count pulses arriving between the fall of Load and the fall of PROC.COMP./ (L44-10), which removes the low from the Load inputs (pin 11 of L49 and L65) by presetting the Q output of the D flip-flop (L44-9) high, are blocked from counting. Thus, once the counters reach a count of 255 (FF hex), they are held at that number until a PROC.COMP. signal arrives. In the meantime the STROBE8 pulse (U16-6 and L47-2 and 14) is generated to strobe the number 255 (FF hex) into the dual 4-bit latch, L47.

The next PROC.COMP. pulse arrives, switches the memories by setting MEMA low and MEMB high, and sets the Q outputs of the "A" memory address counters to zero. The OUTRAN pulse, sent soon therafter, enables the outputs of the latch (L47-5, 7, 9, 11, 17,

19, 21, and 23), as described earlier for the second scan/process period, so the number 255 (FF hex) is put out on the data bus and taken in by the computer.

This covers the basic functioning of the "A" memory address counter circuitry. It alternates between generating memory addresses to be written into during one scan/process period and memory addresses to be read from during the next scan/process period. The "B" memory address counter circuitry functions in the same way as the "A" memory address counter circuitry, but at opposite times. That is, when the "A" memory address counter circuitry is generating addresses to be written into, the "B" memory address counter circuitry is generating addresses to be read from, and vice versa. The two circuitries operate essentially independently of each other, under the direction of the 74LS257 data selector, L43.

VI-9. READ (SH.'S 11, 7, 8, 3, 9)

During initialization procedures, a RESET/ pulse (L69-12) is sent out by the computer. Within 40 ns. after RESET/ goes low, MEMB (L20-9) is high and MEMA (L20-8) is low. Within 64 ns. 43SEL (L20-5) and 21SEL (L70-5) are both low. When the computer is finished with whatever processing it needs to do, it sends out a PROC.COMP. signal (L54-6) to set things in motion to start another scan. Within 40 ns. after PROC.COMP. (L20-11) rises, MEMB is low and MEMA high. Sometime therafter a START pulse will be generated to start the scanning routine. MEMA is high, so the "A" memories (L25, L27, L29, and L31) will have data written into them during the coming scan/process period (a scan/process period being the time between two successive PROC.COMP. signals), while the "B" memories (L26, L28, L30, and L32) will be read from. If this were any scan other than the first, what would be read out of the "B" memories would be the information written into them during the

previous scan/process period. However, since this is the first scan, the "B" memories have garbage in them, so that is what will be read.

When the computer has finished reading from the "B" memories, it will send out a READ COMP/ signal (L69-4) which, via AND gate L33B-A, will clear 43SEL and 21SEL to 0. Then after the computer has finished whatever processing it has to do, it will send out another PROC.COMP. signal, which, among other things, will clock the L20-B flip-flop, causing MEMB and MEMA to switch states, making MEMB high and MEMA low. Now the "B" memories will be written into and the "A" memories read from. The way the memories are written into is covered in the A/D mode description. Of interest now is how the memories are read.

The PROC.COMP./ pulse presets the Q outputs of two D-type flip-flops (L44-A and B), thus disabling the Load inputs of the memory address counters (pin 11 of L49, L65, L64, and L66), and PROC.COMP. clears these same counters to 0 via their Clear inputs (pin 14). At the end of the previous scan cycle, when the "A" memories were having data written into them and when MEMA was high, STROBE8 (U16-6) was generated causing the memory address of the last location written into in the "A" memories to be latched into 4508 latch L47. Since that data was latched, a PROC.COMP. switched the memories, making MEMB high. Now the computer sends out an OUTRAN signal (L54-12) to read the memory address strobed into L47 at the end of the previous scan. Since MEMB is already high, the positive OUTRAN pulse will force the output of the NAND gate into which MEMB and OUTRAN feed - L67-B - low, and, consequently, the Output Disable inputs of the 4508 latch (pins 3 and 15 of L47) low, enabling the Q outputs (L47-5, 7, 9, 11, 17, 19, 21, and 23) 180 ns. max. later. These outputs are put on the multibus data lines and sent to the computer, so the computer now knows how many memory addresses it has to read.

For every memory address to be read, the computer must do two reads because at each memory address there are sixteen bits of

data (four data bits in each of the four "A" memories) to be read, whereas the multibus has only eight data lines via which it can receive data. Each time the computer wants to read from the memories it sends out a MACR pulse (L54-8). 43SEL/ (L20-6), which was set high when READ COMP/ (L69-4) cleared 43SEL to 0 before PROC.COMP. was sent, feeds the Data input of flip-flop L20-A. 43SEL feeds the Data input of flip-flop L70-A. Thus when MACR goes high clocking these flip-flops via their Clock inputs (L20-3 and L70-3), 43SEL goes high within 25 ns. and 21SEL stays low. The next MACR pulse sets 43SEL low and 21SEL high. Each MACR pulse after that changes the state of 43SEL and of 21SEL. Thus 43SEL and 21SEL are in opposite states throughout the reading period, i.e., until READ COMP/ is sent (at the end of the reading) to set them both low.

GG (L33A-6), the output of a NAND gate, is a signal that is high from 20 ns. max. after one of its inputs, GATE1/ (L33A-4), falls until 20 ns. max. after its other input, GATE2/ (L33A-5), rises. With MEMB high, GGB (L34-8) goes low setting B43/ and B21/ low from 64 ns. max. after GATE1 rises until 64 ns. max. after GATE2 falls, thus enabling the four "B" memories (L26, L28, L30, and L32) for this period of time. MEMA, on the other hand, is low, forcing the output of the NAND gate into which it feeds, GGA (L34-11), high. Since GGA is one of the inputs to both L60-A and L60-C, two two-input AND gates, A43/ (L60-3) will follow L50-6 and A21/ (L60-8) will follow L71-12. L50-6 goes low 20 ns. max. after 43SEL (L20-5), MEMB (L20-9), and MACRd (L24-15) are all high and goes high 20 ns. max. after the first of these 3 signals falls. MEMB is high from the start of the scan. 43SEL rises within 25 ns. of the rise of MACR and falls within 40 ns. of the next rise of MACR. MACRd rises within 140 ns. of the rise of MACR and falls within 110 ns. of the fall of MACR. Thus MACRd is the last of the three inputs to L50-B to rise and the first to fall. Thus A43/ falls 184 ns. max. after MACR rises and rises 154 ns. max. after MACR falls.

A21/ (L60-8) follows L71-12, which goes low 20 ns. max. after 21SEL (L70-5), MEMB (L20-9), and MACRd (L24-15) are all high. If 21SEL were high at this time, A21/ would fall 184 ns. max. after the rise of MACR and would rise 154 ns. max. after the fall of MACR. At this point, however, 21SEL is low, so A21/ is high. Thus the A4 and A3 memories (L25 and L27) are enabled and the A2 and A1 memories (L29 and L31) disabled.

OD43A (L22-3) goes low 250 ns. max, after MACR and L58-2 are both high and rises 240 ns. max. after the first of these two inputs to to NAND gate L22-A falls. L58-2 rises 60 ns. max. after L50-6 falls, which is 220 ns. max. after MACR rises, and falls 60 ns. max. after L50-6 rises, which is 190 ns. max. after MACR falls. L58-2 rises after MACR rises, whereas MACR falls before L58-2. Thus OD43A falls 470 ns. max. after MACR rises and rises 250 ns. max. after MACR falls.

OD21A (L22-11) goes low 250 ns. max. after L58-6 and MACR are both high. L58-6 can go high only when 21SEL and MEMB are high, in which case OD21A would fall 470 ns. max. after the rise of MACR and would rise 250 ns. max. after the fall of MACR. Since, at this point, 21SEL is low, OD21A remains high.

OD43B (L22-4) and OD21B (L22-10) remain high. L50-8 is high because one of its inputs, MEMA (L50-9), is low. As a result, L58-4 is low forcing OD43B (L22-4) high. L71-6 is high because one of its inputs, MEMA, (L71-3), is low. Consequently, L58-8 is low forcing OD21B (L22-10) high.

At any one time only one of the three-input NAND gates - L50-B, L50-C, L71-A, and L71-B - is low. Therefore only one of the Output Disables - OD43A, OD21A, OD43B, and OD21B - is low, and that is the one generated by the one low NAND gate among the four just listed.

MEMB (L43-1) is high, so the B inputs of the 74LS257 quad 2-line-to-1-line data selector (L43-3, 6, 10, and 13) are passed through to the outputs (L43-4, 7, 9, and 12). The G enable input (L43-15) is tied low enabling the outputs at all times. Thus

43SEL is passed through to COUNT A (L43-4), which clocks the "A" memory address counter, L65, at pin 5. Recall that the PROC.COMP. signal sent out by the computer set all four memory address counters (L49, L65, L64, and L66) to 0 before the beginning of the scan. The first MACR pulse causes a low-to-high transition in 43SEL (L20-5), which in turn causes the lower "A" memory address counter, L65, to count up to 1. It takes 38 ns. max. for the L65 outputs to be stable. Once the count is above 15 both counters (L49 and L65) are involved, in which case the longest delay until the outputs are settled is 73 ns. Thus, for the worst case, the Q outputs of the "A" memory address counters (pins 3, 2, 6, and 7 of L49 and L65) are stable, and likewise the address inputs to the 1822 "A" memories (pins 7, 6, 5, 21, 1, 2, 3, and 4 of L25, L27, L29, and L31), 116 ns. max. after MACR rises and remain so until 43SEL rises again.

Again, since MEMB (L43-1) is high R/W (L43-7) follows the 2B input and thus remains high (read mode). A43/ falls 184 ns. max. after MACR rises and rises 154 ns. max. after MACR falls. OD43A falls 470 ns. max. after MACR rises and rises 250 ns. max. after MACR falls. From the fall of OD43A a maximum of 200 ns. may elapse before the A4 and A3 memory outputs are valid, i.e., 670 ns. max. after MACR rises. The access time from when the A4 and A3 memory address lines are stable is 450 ns., or 566 ns. after MACR rises. From the fall of A43/ to the time the A4 and A3 memory outputs are valid is 450 ns. max. or 634 ns. max. after MACR rises. Since all three of these conditions for valid outputs must be met before the outputs are valid, the A4 and A3 memory outputs (pins 10, 12, 14, and 16 of L25 and L27) are valid, at the latest, 670 ns. after MACR rises. The outputs remain valid until 20 ns. min. after OD43A rises, which is 270 ns. max. after MACR falls, until 20 ns. min. after A43/ rises, which is 174 ns. max. after MACR falls, or until the memory address changes, which isn't until after 43SEL rises again. The earliest of these is 174 ns. max. after MACR falls. So the outputs of the A4 and A3 memories

are valid from 670 ns. max. after MACR rises until about 174 ns. max. after MACR falls, or, to be sure, until MACR falls. From the discussion of MACR generation (the next section), one can see that the multibus timing requirements are satisfied.

One read being finished, the next MACR pulse is sent out by the computer. Within 40 ns. of the rise of MACR, 43SEL is low and 21SEL high. The "A" memory address counters don't change, so the same addresses are on the "A" memory address lines as before. This time the data in the A2 and A1 memories will be put out on the data bus lines, the other six memories having their outputs disabled. A43/ and OD43A will remain high and A21/ and OD21A will have the same timing with respect to the present MACR pulse as A43/ and OD43A, respectively, did with respect to the last MACR pulse. Meanwhile, as long as GATE1 or GATE2 is high, B43/ and B21/, which feed the CS1/ inputs of the "B" memories (pin 19 of L26, L28, L30, and L32), will remain low keeping those memories enabled, while OD43B and OD21B, the Output Disable inputs to the "B" memories (pin 18 of L26, L28, L30, and L32), will remain high disabling the outputs of these memories.

When the "A" memories have been read, a READ COMP/ pulse is sent to reset 43SEL and 21SEL low. Then, as soon as the scan circuitry has finished writing into the "B" memories and the computer has finished processing data from the "A" memories (data from the previous scan), a PROC.COMP. pulse is sent to switch the memories in preparation for a new scan. During this scan the "A" memories will be written into and the "B" memories read from. Thus A43/, OD43A, A21/, and OD21A will trade roles with B43/, OD43B, B21/, and OD21B, respectively. These alternating roles can be seen on the Read timing diagram.

VI-10. MACR (SH.'S 11, 7, 9, 10)

MACR (L54-8) is generated when the computer executes a

command to read port 86H. 86H is a hexadecimal number, whose binary form is HLLLLHHL. However, addresses are put out on the multibus address lines in negative true form. Thus ADR7/-ADR0/ (P1-52, 51, 54, 53, 56, 55, 58, and 57) receive LHHHHLLH, respectively, which are sent on to the inputs of a 74LS241 octal 3-state buffer (L40 -11, 13, 15, 17, 8, 6, 4, and 2). The OEa/ input to the buffer (L40-1) is tied low and the OEb input (L40-19) high so that all eight outputs (L40-9, 7, 5, 3, 12, 14, 16, and 18) are always enabled.

Once the negative true binary form of the hexadecimal number 86 is on the address lines, the 8, which is the base address, is decoded by a 4-input NAND gate (L38-A) whose output, BASE ADR/ (L38-6), goes low within 58 ns. of when the valid address is stable on the bus. When BASE ADR/ goes low, it sets the G1 and G2 chip enables of the 74154 4-line-to-16-line decoder/demultiplexer (pins 18 and 19 of L41) low enabling the chip. The digit 6 of the number 86 is decoded by L41 causing PMACR/ (L41-7) to go low within 71 ns. after the address, 86, is stable on the bus. (All other L41 outputs remain high.) PMACR/ may not go low until 85 ns. after the address is stable on the bus, however, because it may take that long for the output to be enabled via the strobes G1 and G2 (L41-18 and 19). PMACR/ stays low until 71 ns. max. after the address (86H) on the bus goes away.

The multibus manual points out that IORC/ (P1-21) goes low a minimum of 50 ns. after the address is valid on the bus and goes high a minimum of 50 ns. before the address on the bus goes away. Within 20 ns. after IORC/ goes low, the output of the NAND gate into which it feeds (L33A-C) goes high removing the Clear from the 74LS164 8-bit parallel-out serial shift register, L57. Both Data inputs of this shift register, Dsa and Dsb (L57-1 and 2), are tied high so that when the Clear input (L57-9) is high the positive transiton of the Clock input, which is the 9.216MHZ clock, will cause a high to be shifted into QA (L57-3) and all other Q outputs to shift one position in the direction from QA toward QH.

Following this procedure, QH will go high anywhere from about 760 ns. to 895 ns. after Clear (L57-9) goes high. XACK/ (L59-5) follows QH (L57-13) by 16 ns. max. , as long as BOARD ENABLE/ (L33A-11), which feeds the enable input of the 74LS368 3-state inverter (L59-1), is low. BOARD ENABLE/ goes low 40 ns. after BASE ADR/ and IORC/ are both low. IORC/ goes low a minimum of 50 ns. after the address is on the multibus, whereas BASE ADR/ goes low a maximum of 58 ns. after the address is on the multibus. Either way, BOARD ENABLE/ (L33A-11) is low long before QH (L57-13) goes high, which happens between 780 and 915 ns. after IORC/ goes low. XACK/ (L59-5) goes low within 16 ns. of when QH goes high.

40 ns. after either BASE ADR/ (L38-6) or IORC/ (P1-21) goes high BOARD ENABLE/ (L33A-11) goes high, and 23 ns. later XACK/ (L59-5) goes to high impedance. According to multibus specifications, the address remains valid on the bus 50 ns. min. after the command, in this case IORC/, goes away. Thus XACK/ goes low from between 796 and 931 ns. after IORC/ goes low (thus adhering to the 0 ns. - 10 ms. acknowledge delay time allowed by the multibus) and rises 63 ns. after IORC/ rises (thus staying within the multibus' 0 ns. - 100 ns. allowed acknowledge hold time).

READ (L37-12) goes high 20 ns. max. after IORC/ (L37-1) and BASE ADR/ (L37-2 and 13) are both low and falls 20 ns. max. after either one of these signals rises. READ/ (L39-10) is the inverted form of READ (L37-12), delayed by 20 ns. max. Thus READ/ goes low 40 ns. max. after IORC/ (P1-21) and BASE ADR/ (L38-6) are both low and high 40 ns. max. after one of these signals goes high.

MACR (L54-8) goes high 20 ns. max. after both PMACR/ and READ/ are low. PMACR/ goes low as long as 85 ns. after the bus address lines are stable and READ/ within 40 ns. of when IORC/ and BASE ADR/ are both low. IORC/ goes low 50 ns. min. and BASE ADR/ 58 ns. max. after the bus address lines are stable, so the rise of MACR will be, perhaps, around 118 ns. after the bus address lines are stable, unless IORC/ goes low later than BASE ADR/, in which

case MACR will rise 60 ns. max. after IORC/ falls. MACR will fall within 60 ns. after the rise of IORC/, the first of the three signals to go away.

43SEL (L20-5) rises 25 ns. after MACR rises and falls 40 ns. max. after the next MACR rises and repeats this rise and fall routine for the duration of the reading cycle. 21SEL (L70-5) follows the same timing as 43SEL, but one MACR pulse later. 43SEL and 21SEL are always in opposite states while reading is going on. Between reading cycles 43SEL and 21SEL are both low.

When MEMB (L20-9) and 43SEL are both high, A43/ (L60-3) will fall 154 ns. after MACR rises and rise 184 ns. after MACR falls. When MEMB and 21SEL are both high, A21/ (L60-8) will fall instead of A43/, but with the same timing as just mentioned for A43/. Otherwise A43/ and A21/ remain high. (If MEMB is low, B43/ (L60-6) and B21/ (L60-11) follow the timing just mentioned for A43/ AND A21/.)

Shortly after L50-6 goes low L22-2, the inverted form of L50-6, goes high gating through part of the MACR pulse (L22-1) causing OD43A (L22-3) to go low. OD43A falls 670 ns. max. after MACR rises and rises 250 ns. max. after MACR falls, but only in the read cycle in which L50-6 goes low. Similarly, when it's L71-12's turn to go low, OD21A (L22-11) will fall and rise with the timing just described for OD43A. Thus only one Output Disable, ODxxx, will go low during a MACR read. During one reading period, either OD43A and OD21A or OD43B and OD21B will alternate going low as the computer alternates between reading memories x4 and x3 and memories x2 and x1 (x being A or B, whichever memory bank is being read.)

The outputs of A4 and A3 (pins 10, 12, 14, and 16 of L25 and L27) are valid within 450 ns. max. of the fall of A43/, or 604 ns. after MACR rises; within 200 ns. of the fall of OD43A, or 870 ns. max. after the rise of MACR; and 450 ns. max. from when the 1822 address lines are stable, or 541 ns. max. after the multibus address lines are stable. Thus the A4 and A3 outputs are valid by

870 ns. after MACR rises, or about 930 ns. after IORC/ falls. It takes a maximum of 195 ns. for the data to get from the A4 and A3 memory outputs to the multibus data lines, which thus have valid data (in negative true form, due to passage through the 74LS242's (L62 and L63), quad inverting bus transceivers) on them by 1125 ns. max. after IORC/ falls.

Valid data remains at the outputs of the A4 and A3 memories until 20 ns. min. after OD43A rises, or 270 ns. after MACR falls; or until 20 ns. min. after A43/ rises, or 204 ns. after MACR falls. However, data is allowed through the 74LS242 quad bus transceivers (L62 and L63) to the bus only when READ (pins 1 and 13 of L62 and L63) is high and is invalid from 25 ns. max. after READ falls. Thus the valid data is on the multibus data lines from 1125 ns. after IORC/ falls, essentially until READ falls, which is shortly after IORC/ rises, so correct data is read into the computer.

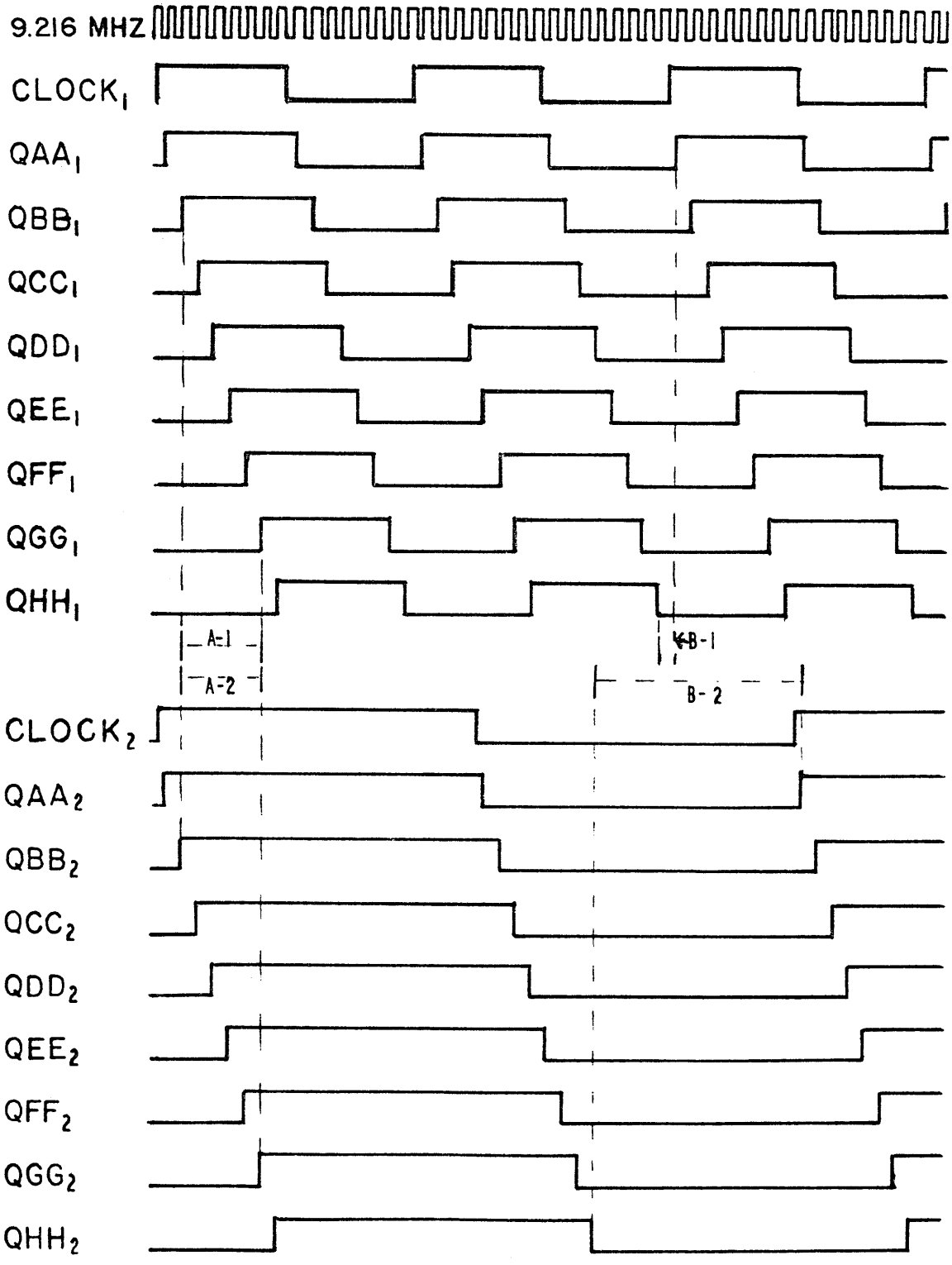


Fig. VI-O QAA - QHH

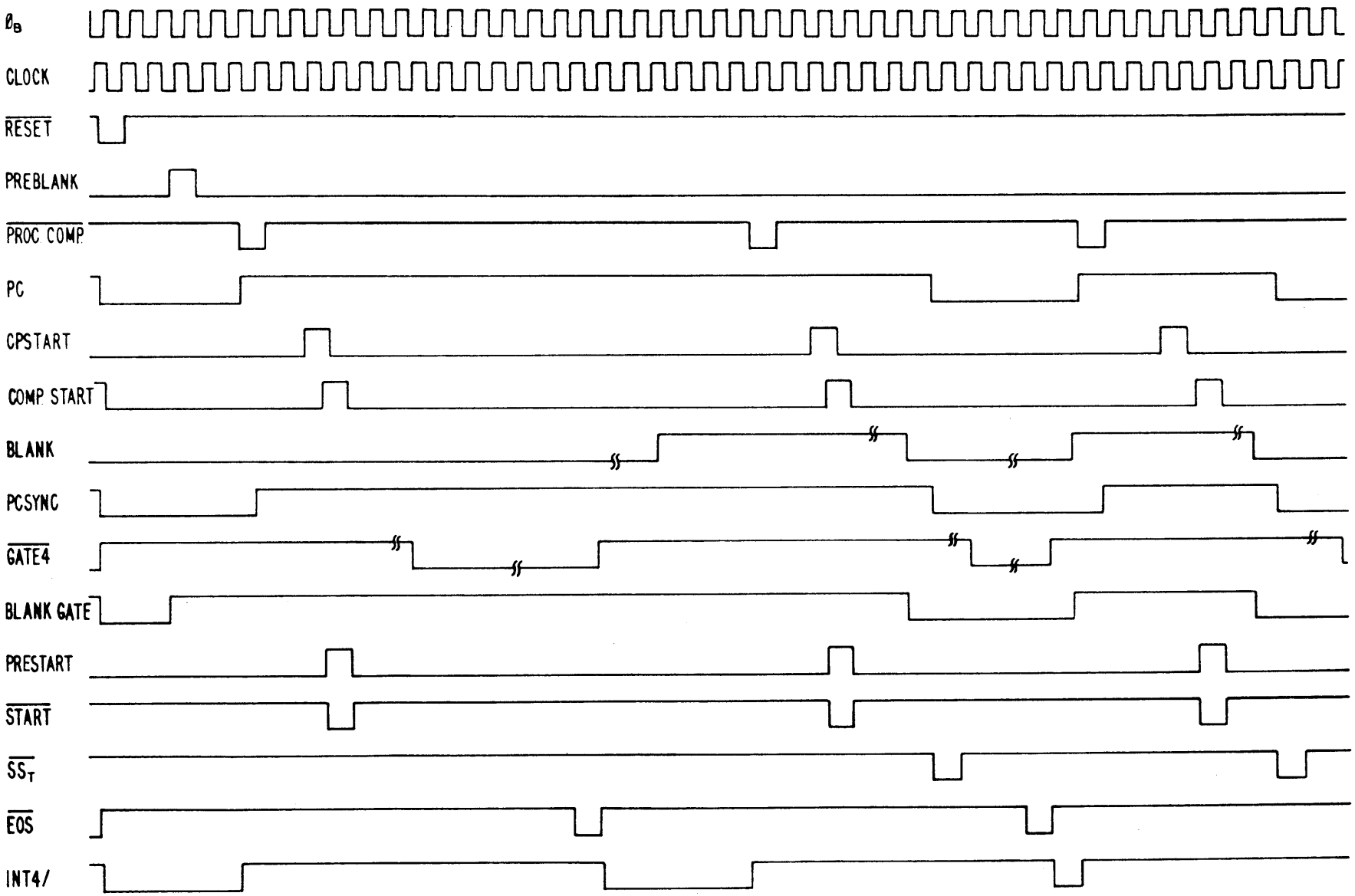


Fig. VI-1 CLOCK, START, CONTROL

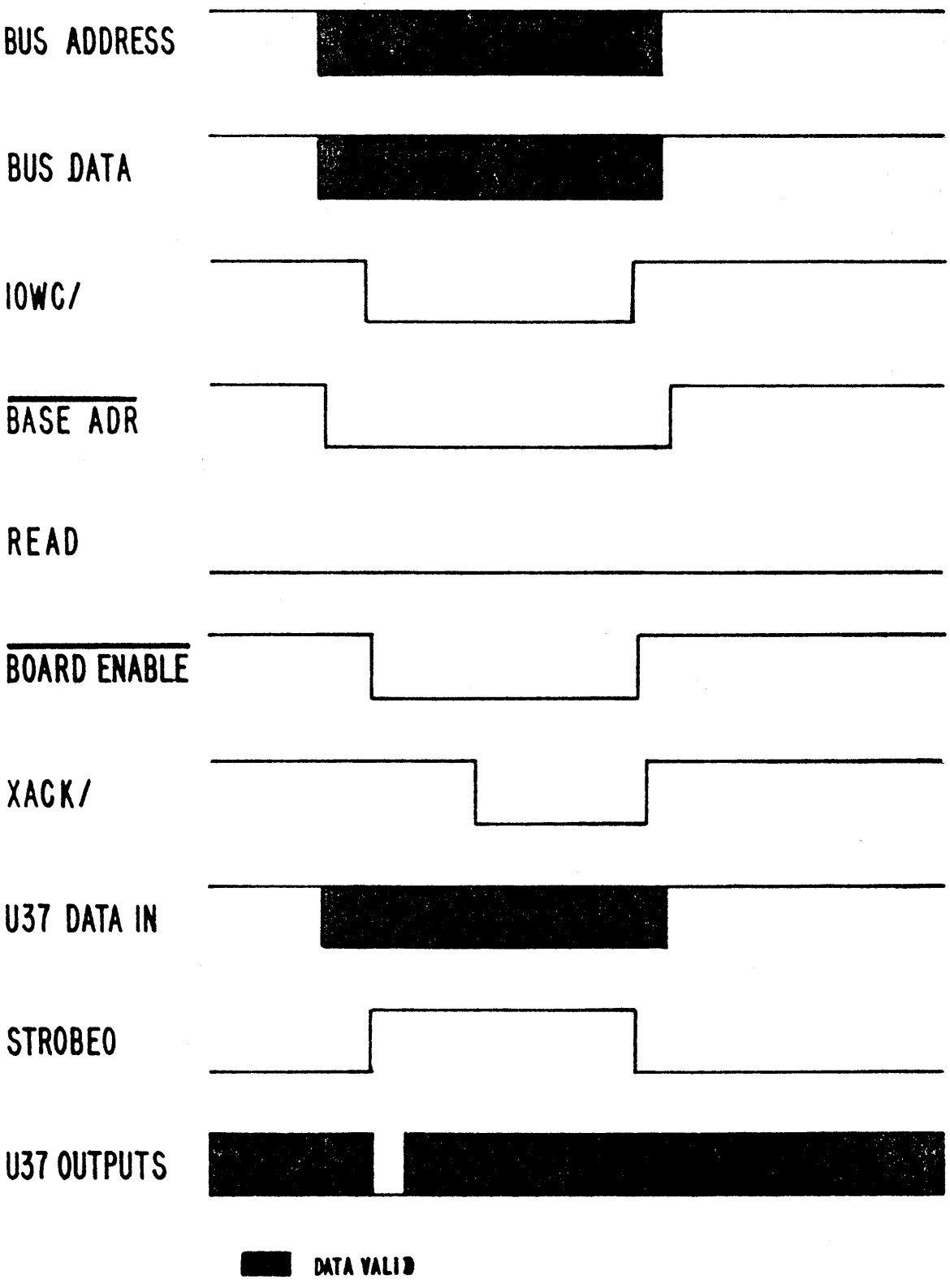


Fig. VI-2 STROBEO

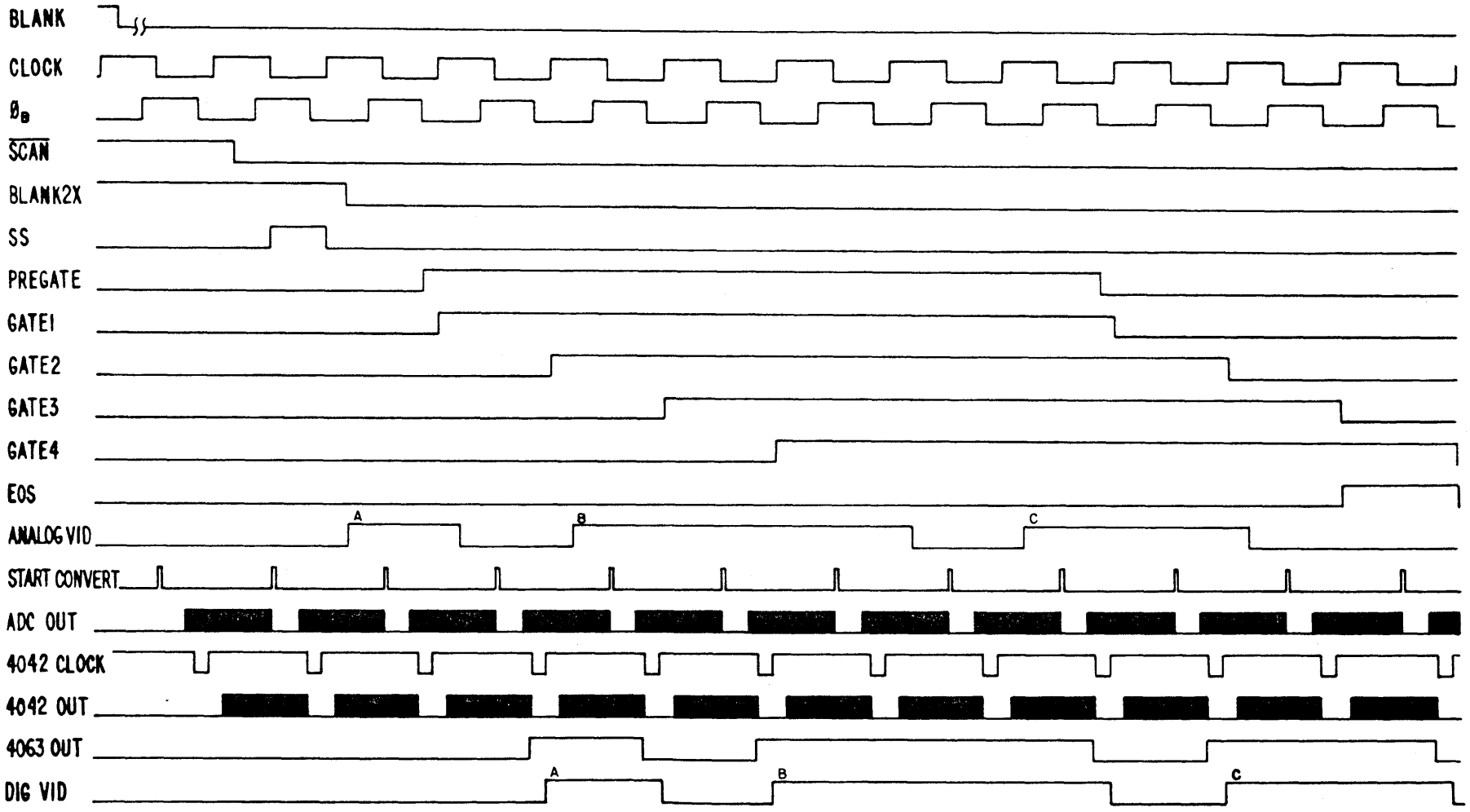


Fig. VI-3 PREGATE / DIG VID

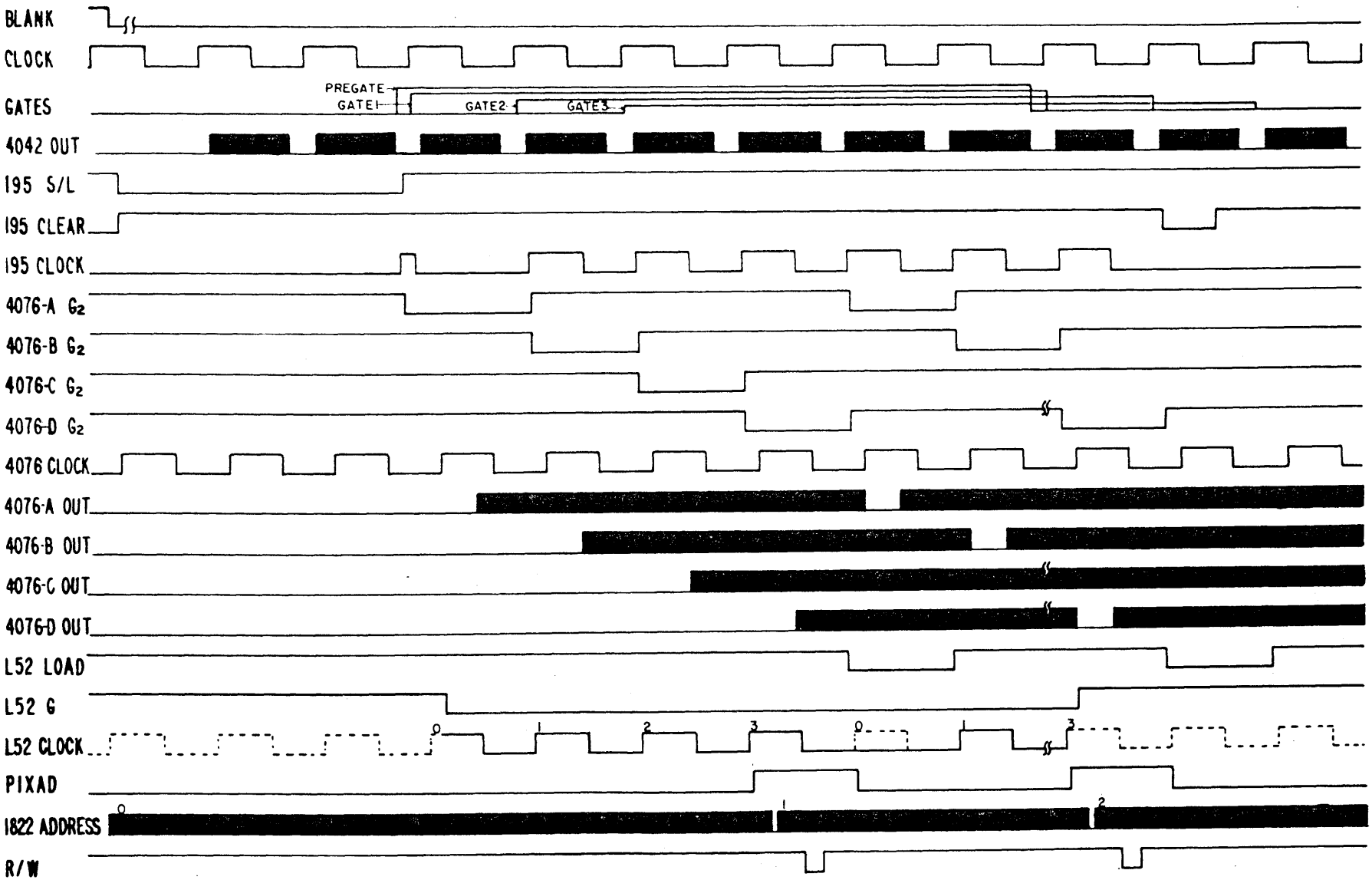


Fig. VI-4 A/D MODE

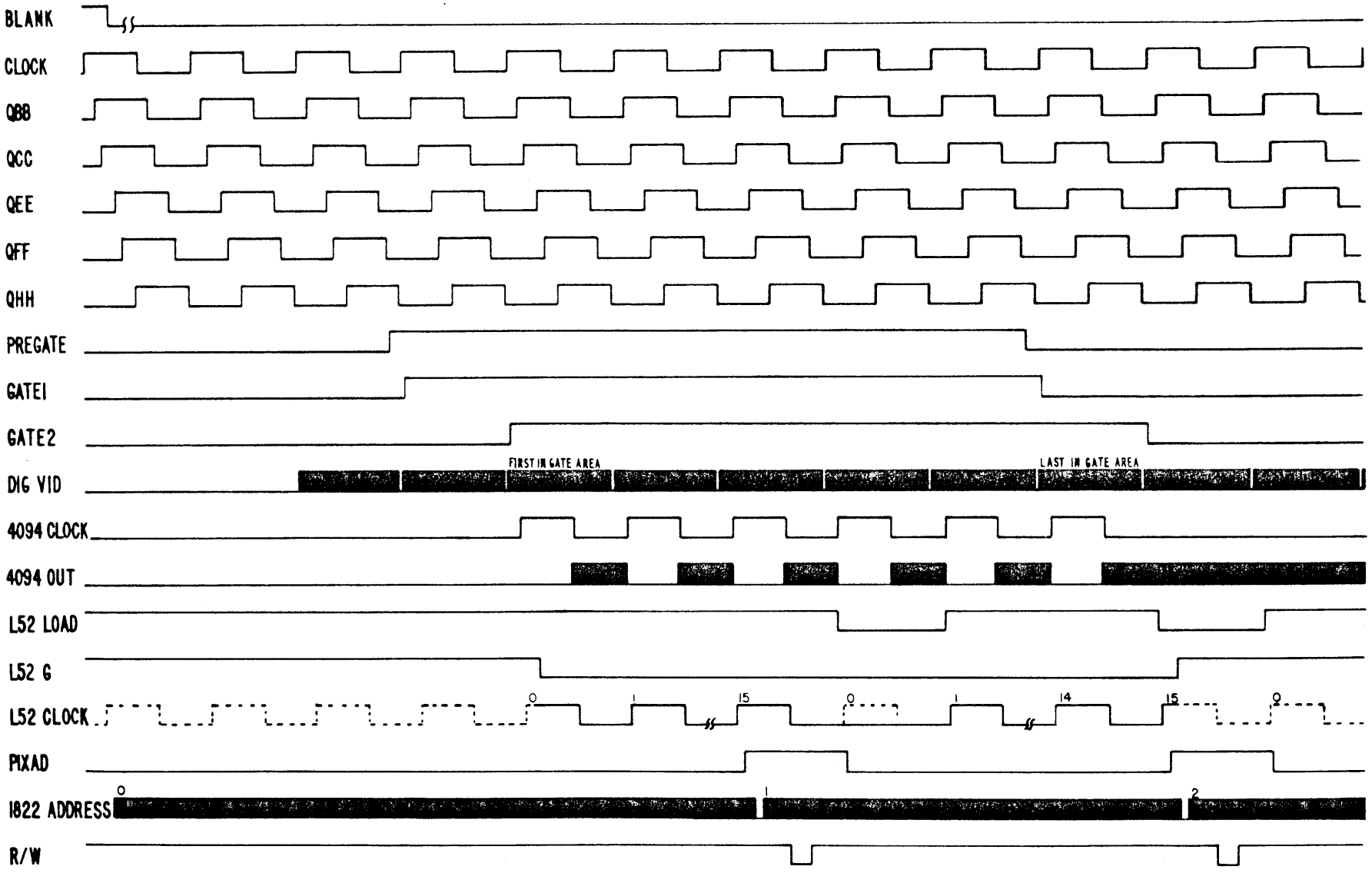
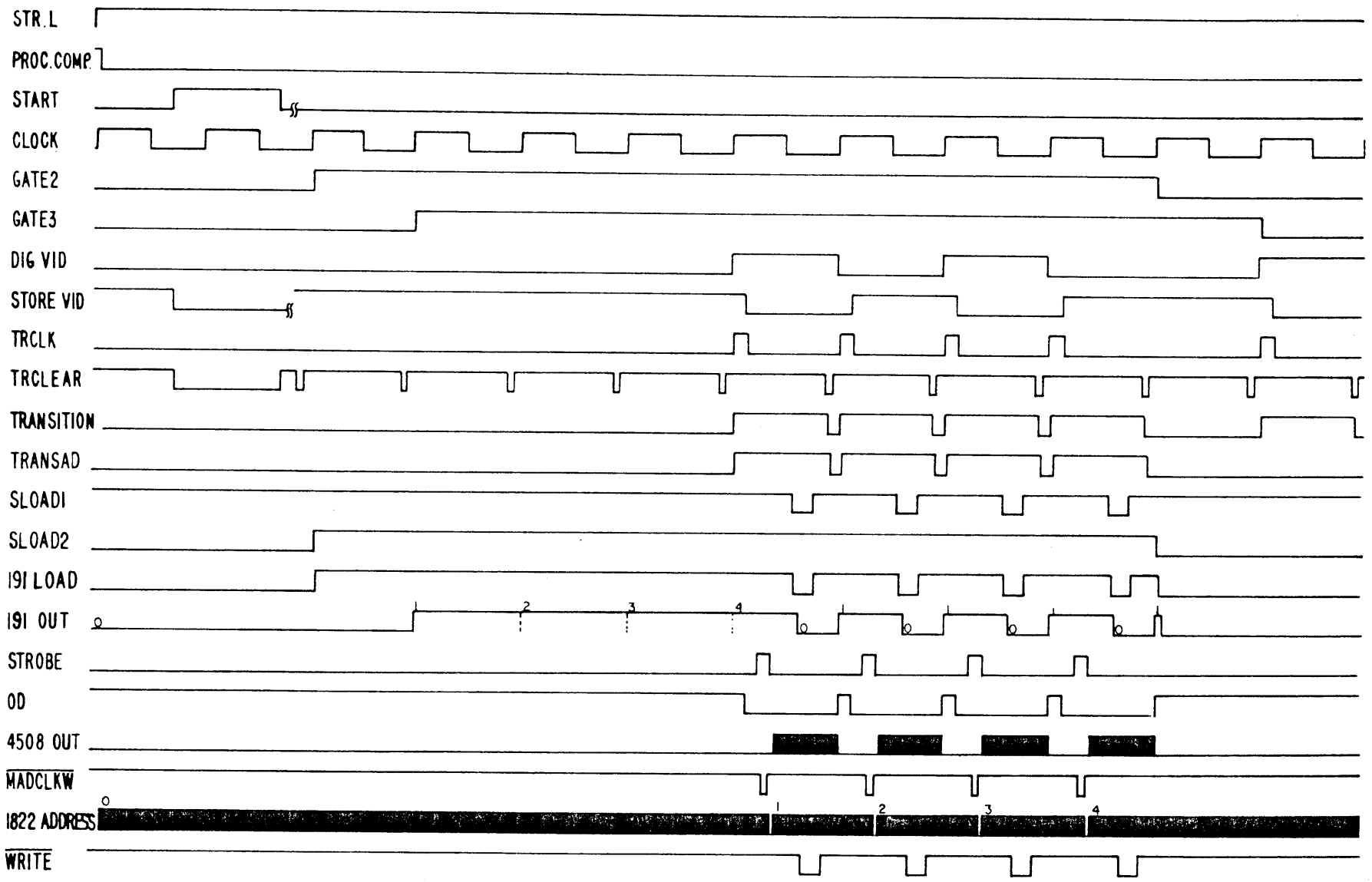


Fig. VI-5 PIXEL MODE



DATA VALID

Fig. VI-6 STR.L MODE

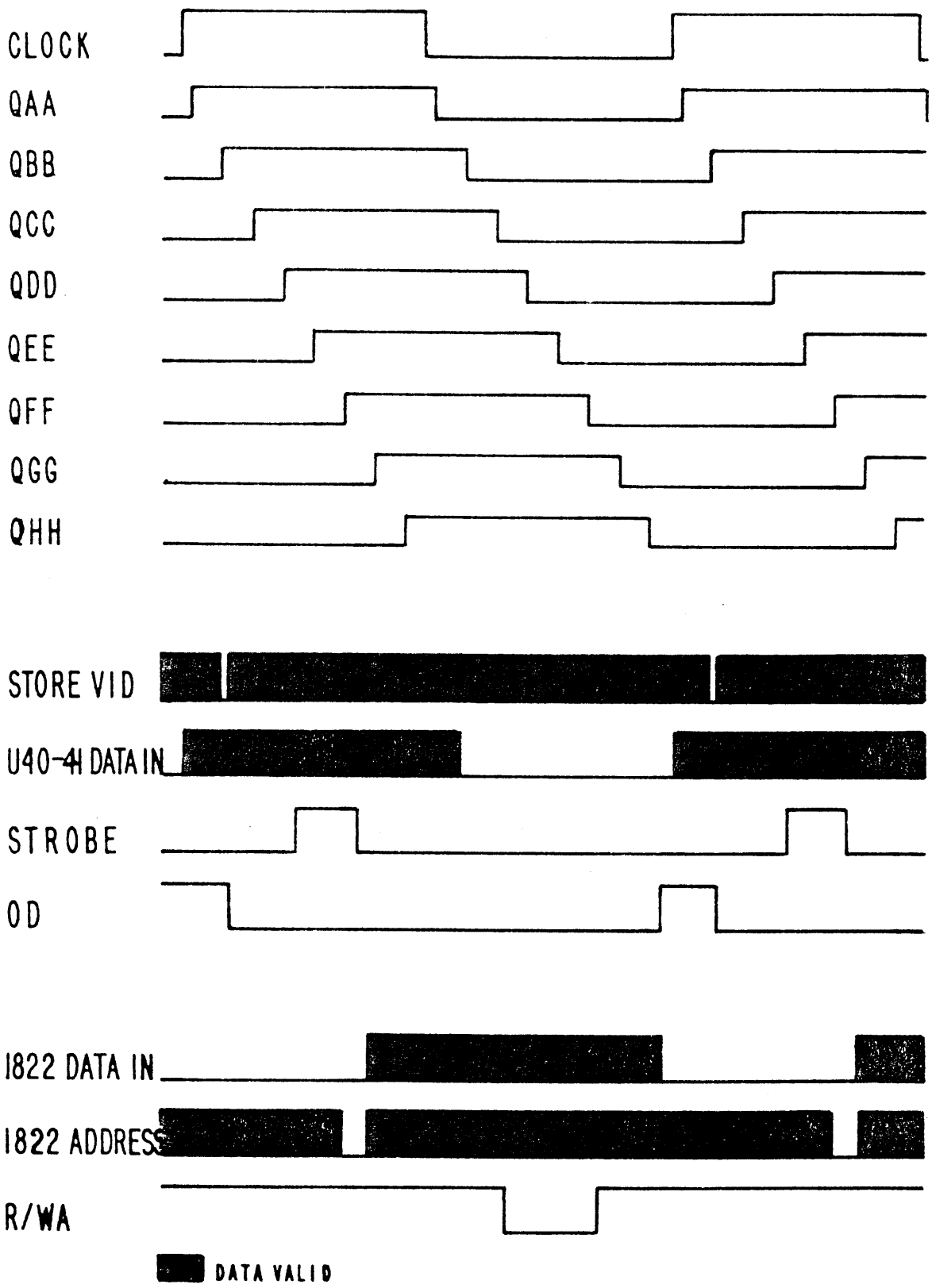


Fig. VI-7 STR.L. or TRAN. MODE

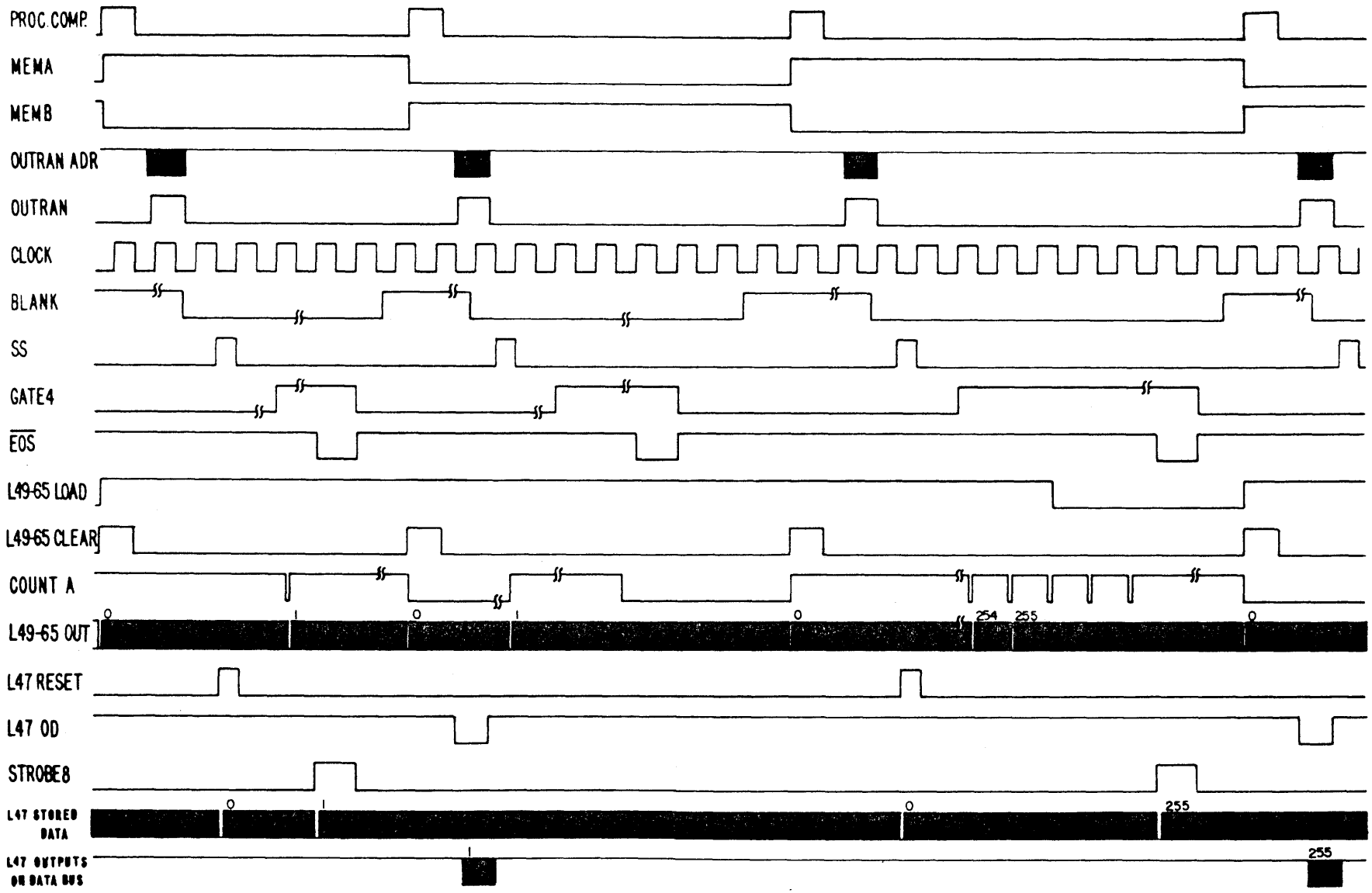


Fig. VI-8 "A" MEMORY ADDRESS CIRCUITRY

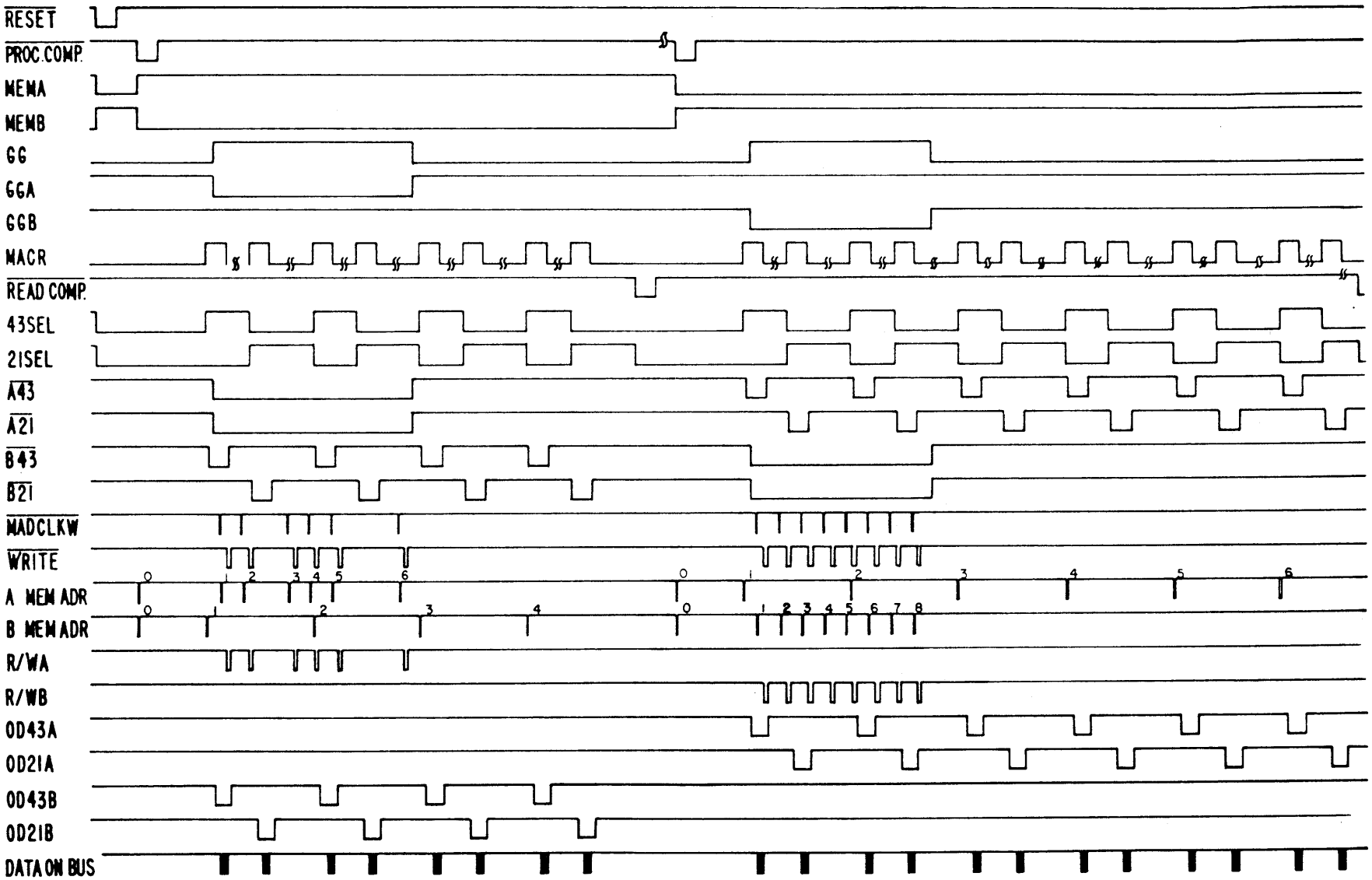

RESET
PROC.COMP.
MEMA
MEMB
GG
GGA
GGB
MACR
READ COMP.
43SEL
21SEL
A43
A21
B43
B21
MADCLKW
WRITE
A MEM ADR
B MEM ADR
R/WA
R/WB
OD43A
OD21A
OD43B
OD21B
DATA ON BUS
DATA VALID

Fig. VI-9 READ

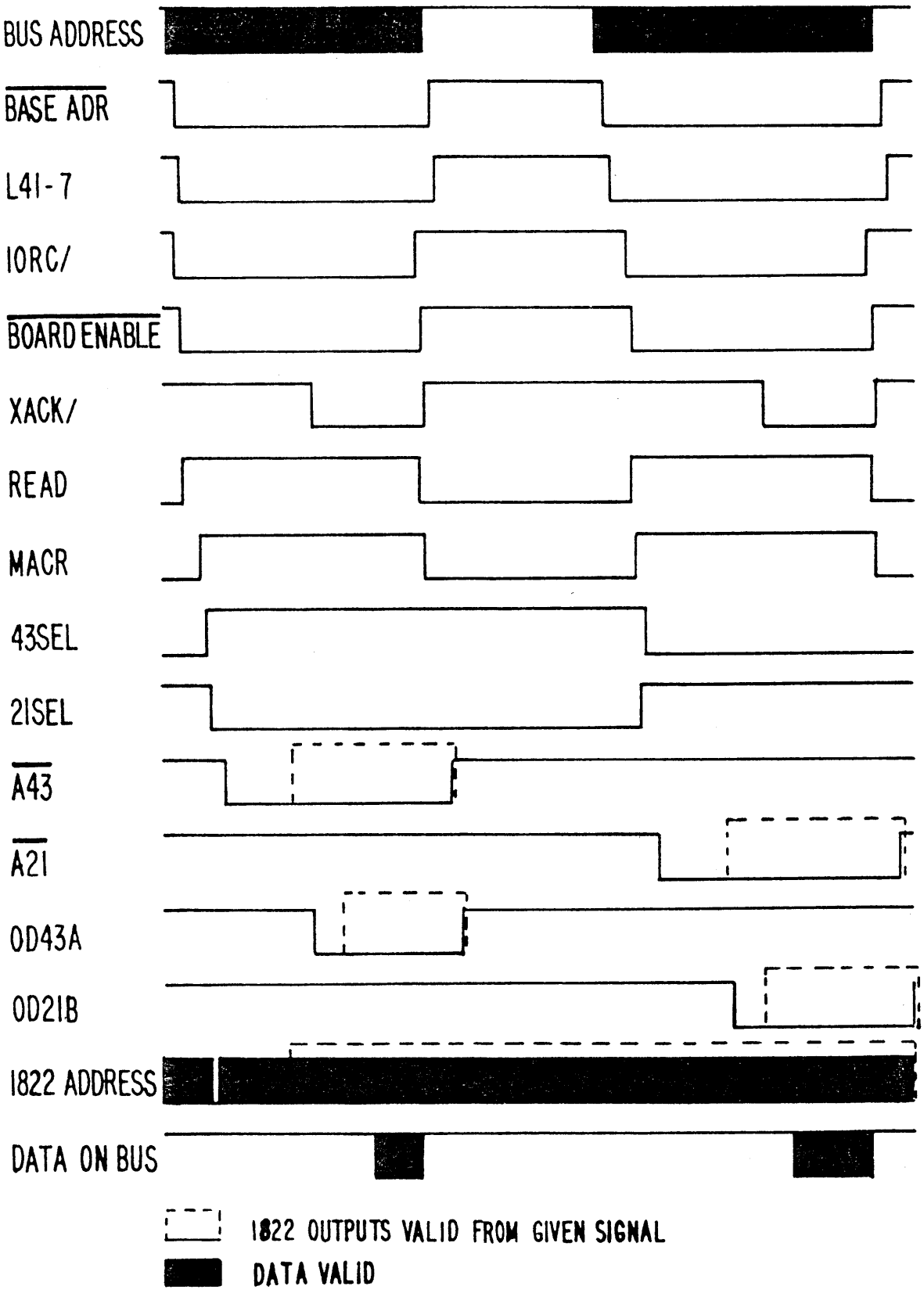


Fig. VI-10 MACR and READ

VII. CONCLUSIONS

The Camera-Microcomputer Interface works very well and does, as has been pointed out in this paper, provide the user with a great deal of flexibility, as well as control. The major shortcoming of the interface, at least as far as future users are concerned, is its occupation of a rather large amount of real estate -- two boards. Thus designs are already in progress to reduce it to a one-board version. This is not as difficult as it may appear, since there are many superfluous elements on the boards, partly due to the constraint of having to design with a limited variety of chips available (as, for example, having to use three-input NOR gates when only two-input ones were needed), and partly due to simplification of the design without a corresponding reduction in chips used (leaving, for example, Status Control Register 5 on board, when its functions could be taken over by the two unused positions in Status Control Register 0). One new feature will be provided, however, that will greatly enhance the new version - the use on board of a microprocessor with DMA (Direct Memory Access) capability to do some of the processing done by hardware on the present interface. Meanwhile, as the new version is being designed, work is being done on the development of applications programs.

VIII. REFERENCES

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Wickes, William E. Logic Design with Integrated Circuits. John Wiley and Sons, New York, 1968

Manuals published by Intel Corporation, Santa Clara California:

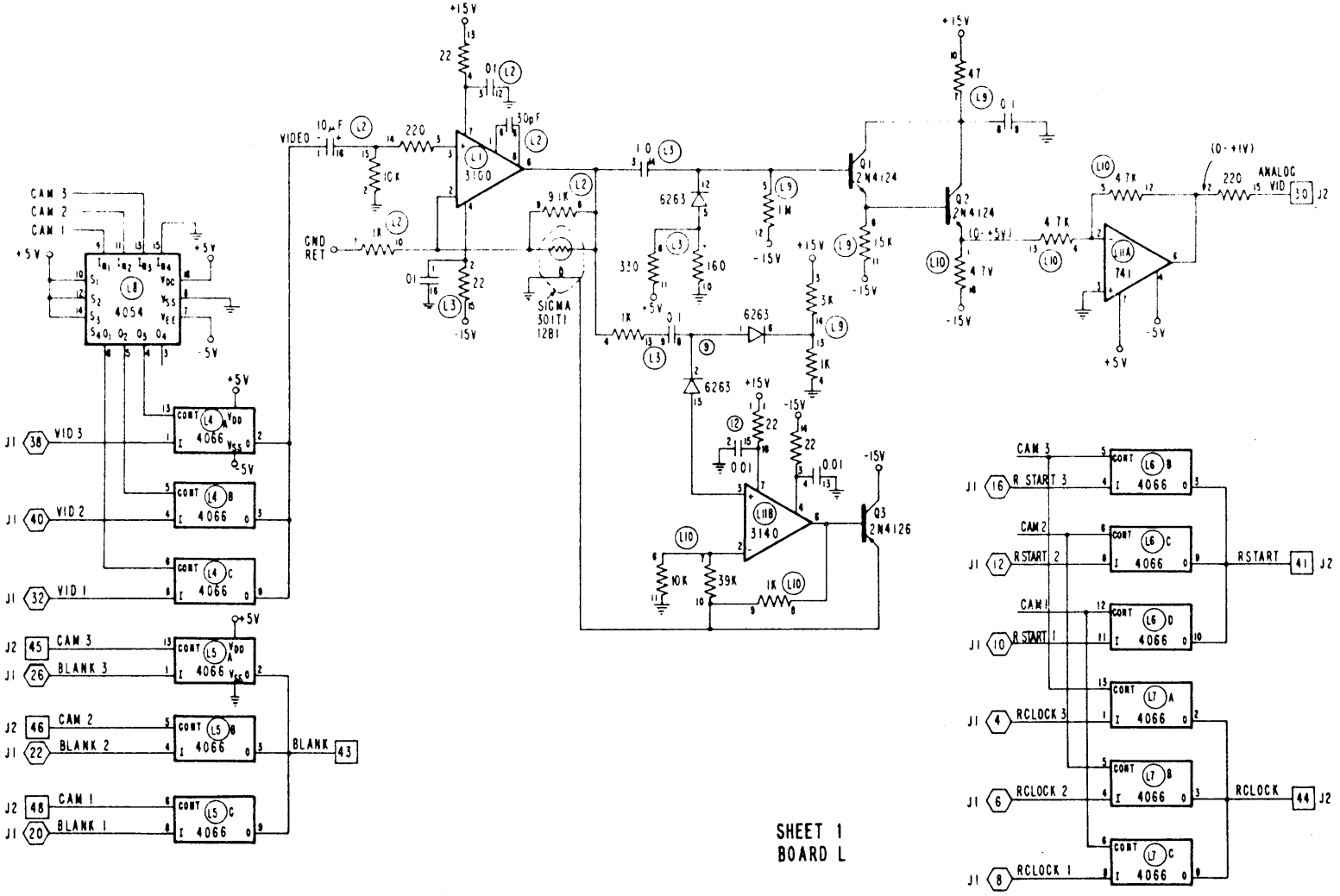
MCS-80 User's Manual

8080/8085 Assembly Language Programming Manual

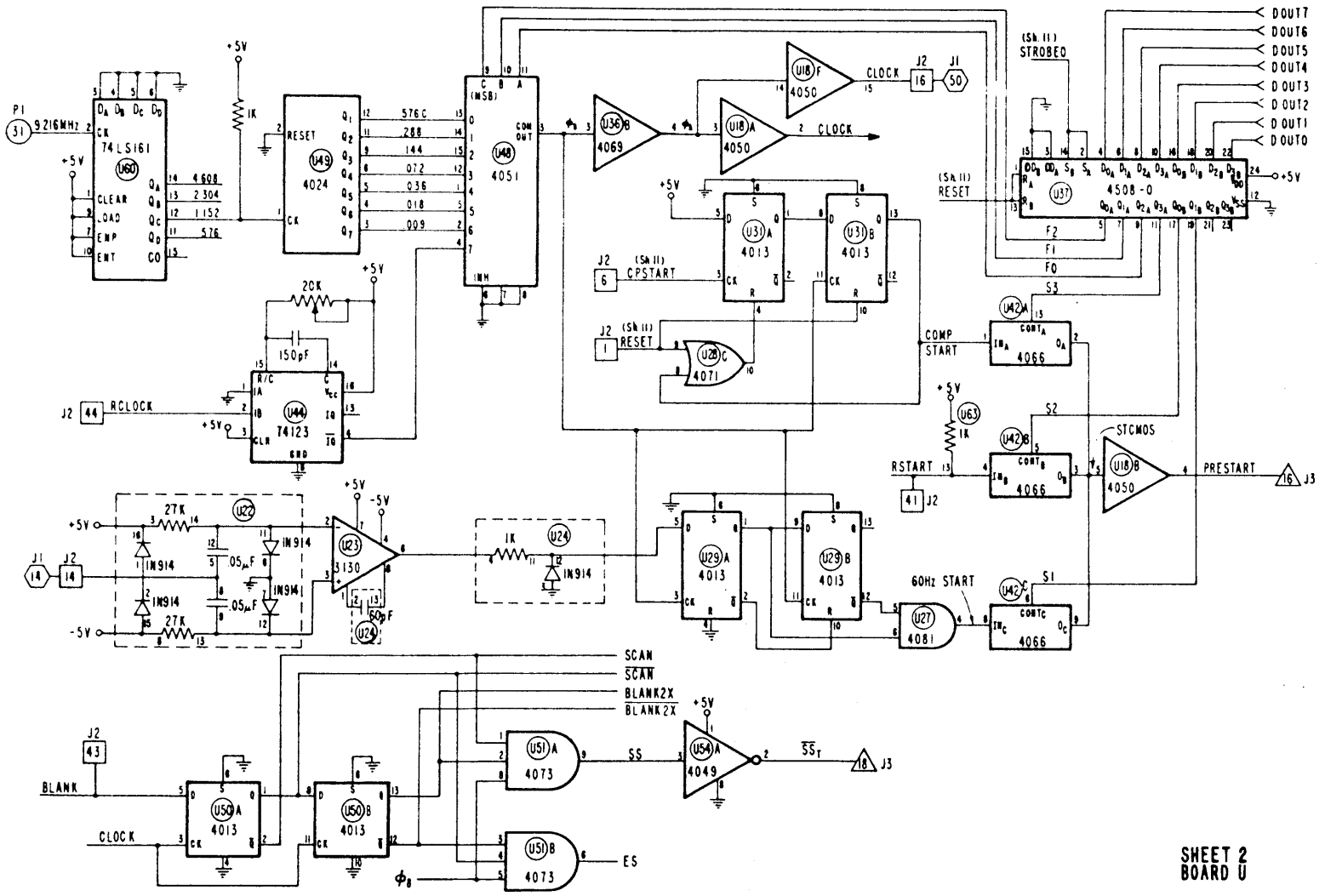
System 80/20-4 Microcomputer Hardware Reference Manual

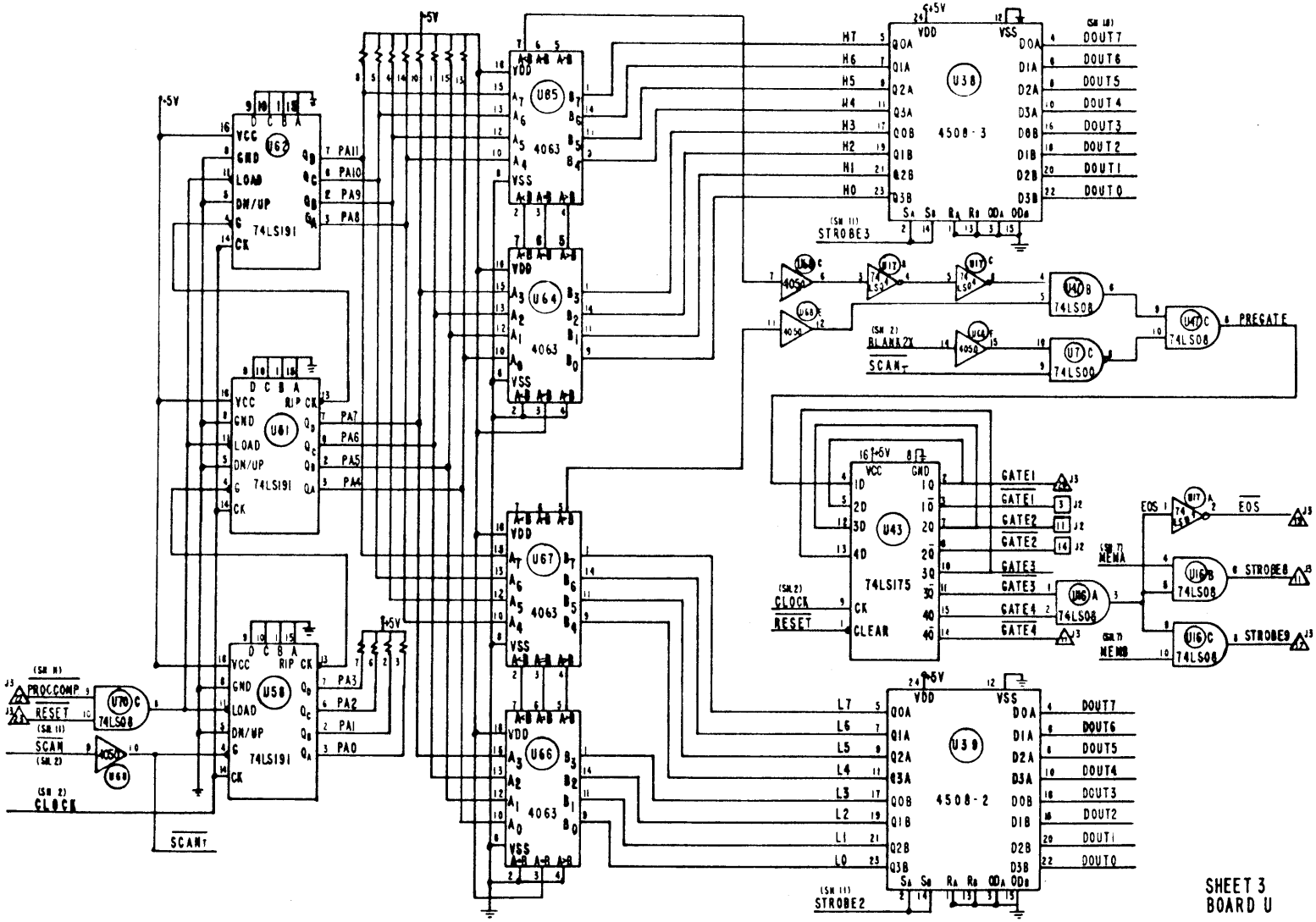
8080 Microcomputer System User's Manual

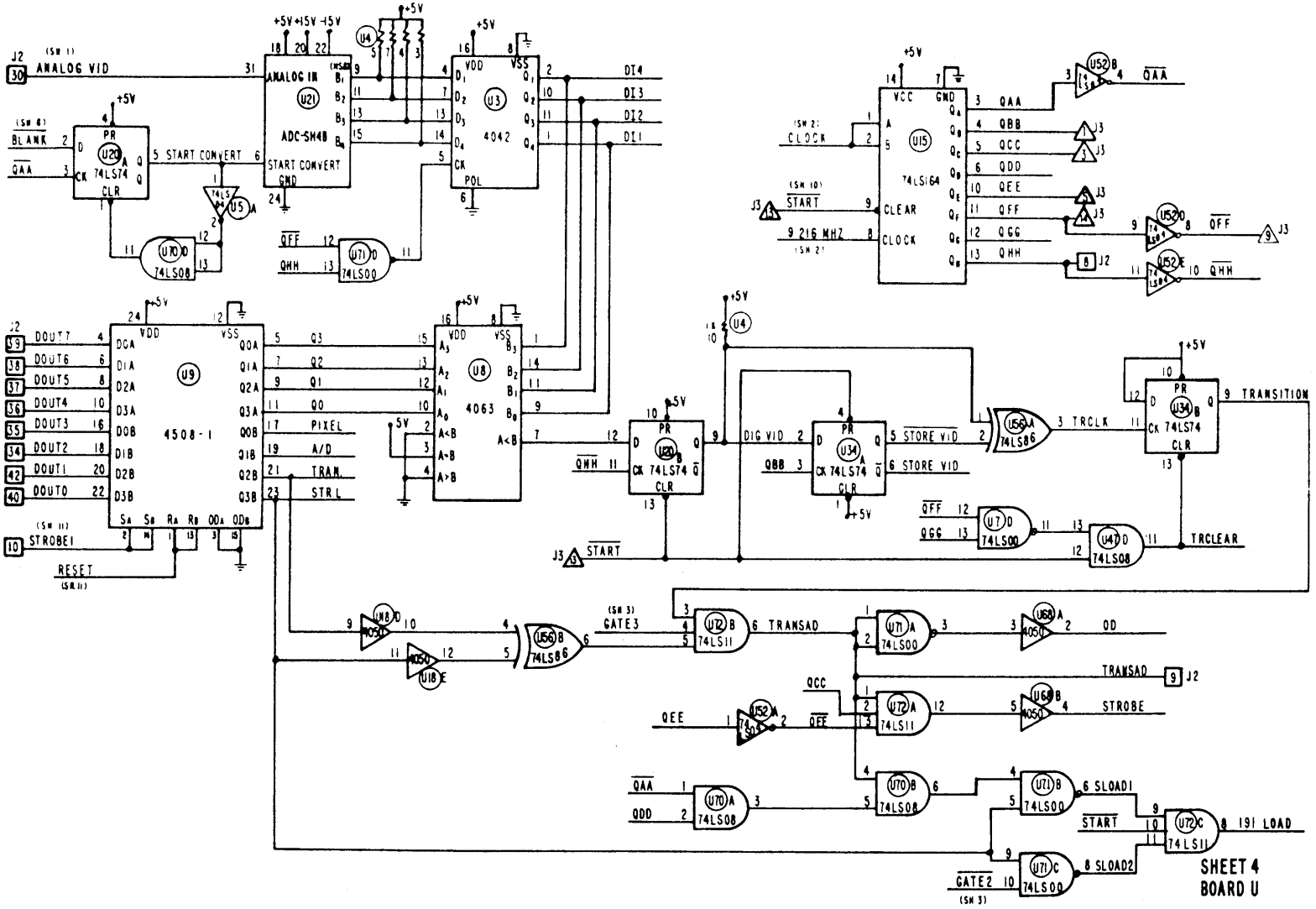
Intel Multibus Interfacing by Thomas Rolander

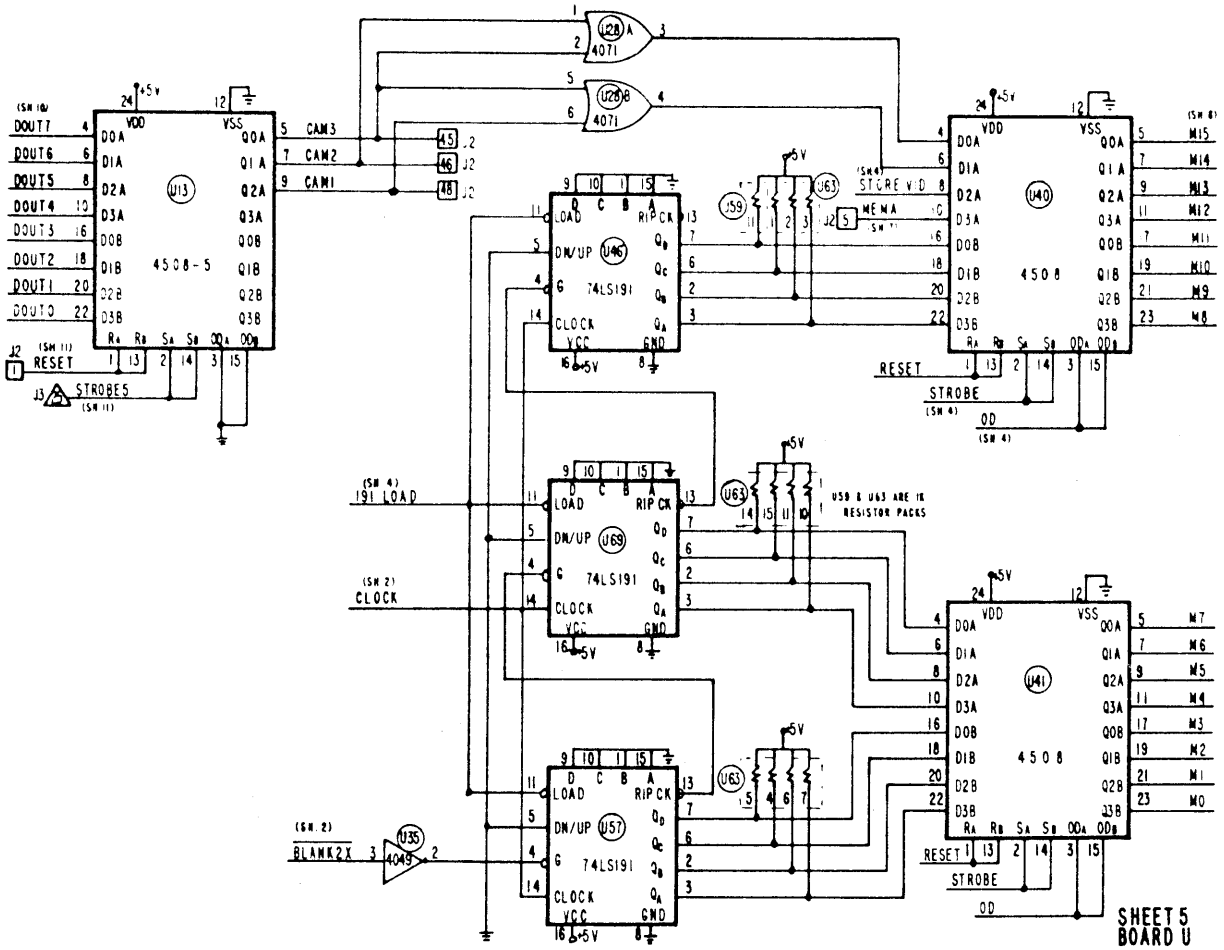


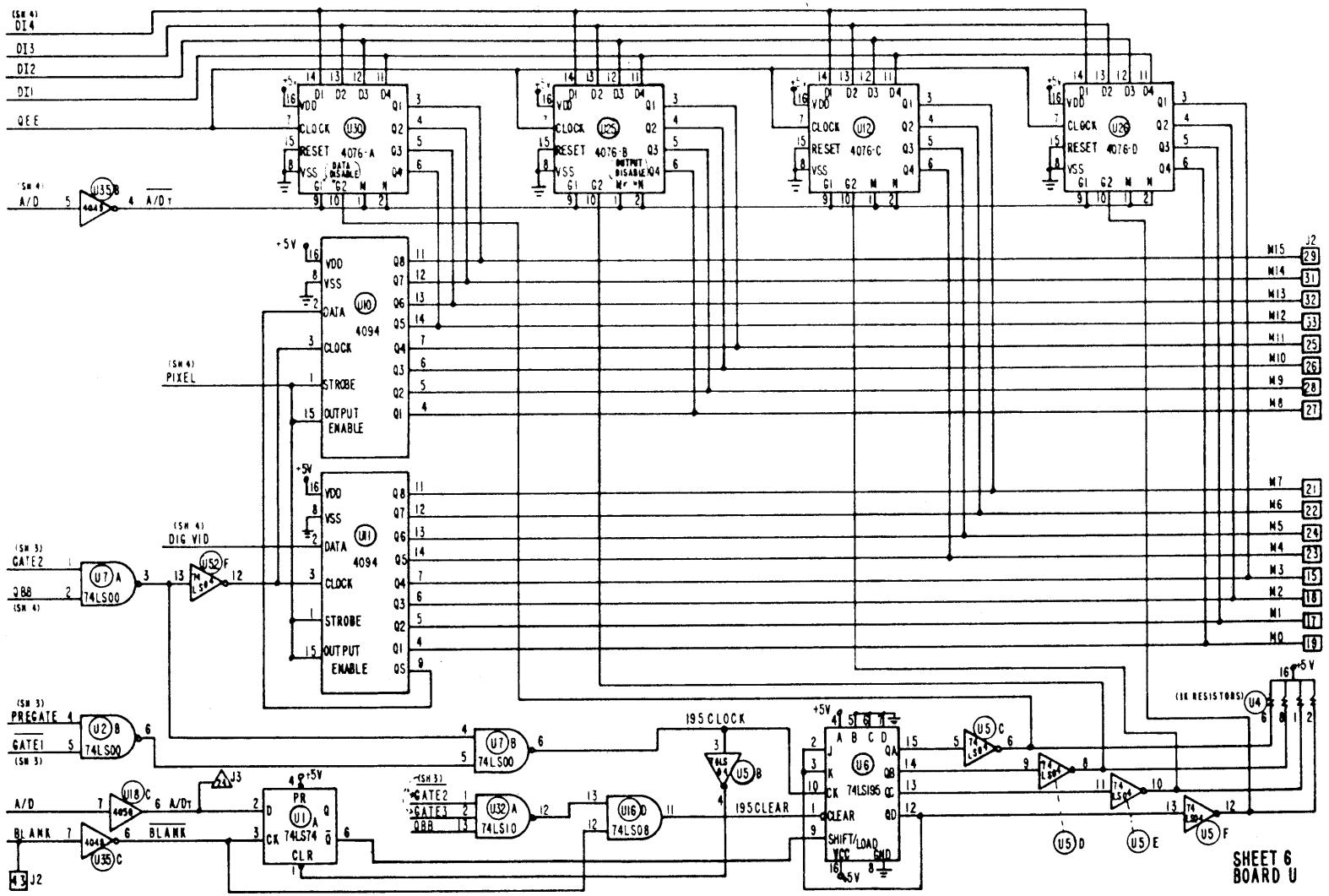
SHEET 1
BOARD L

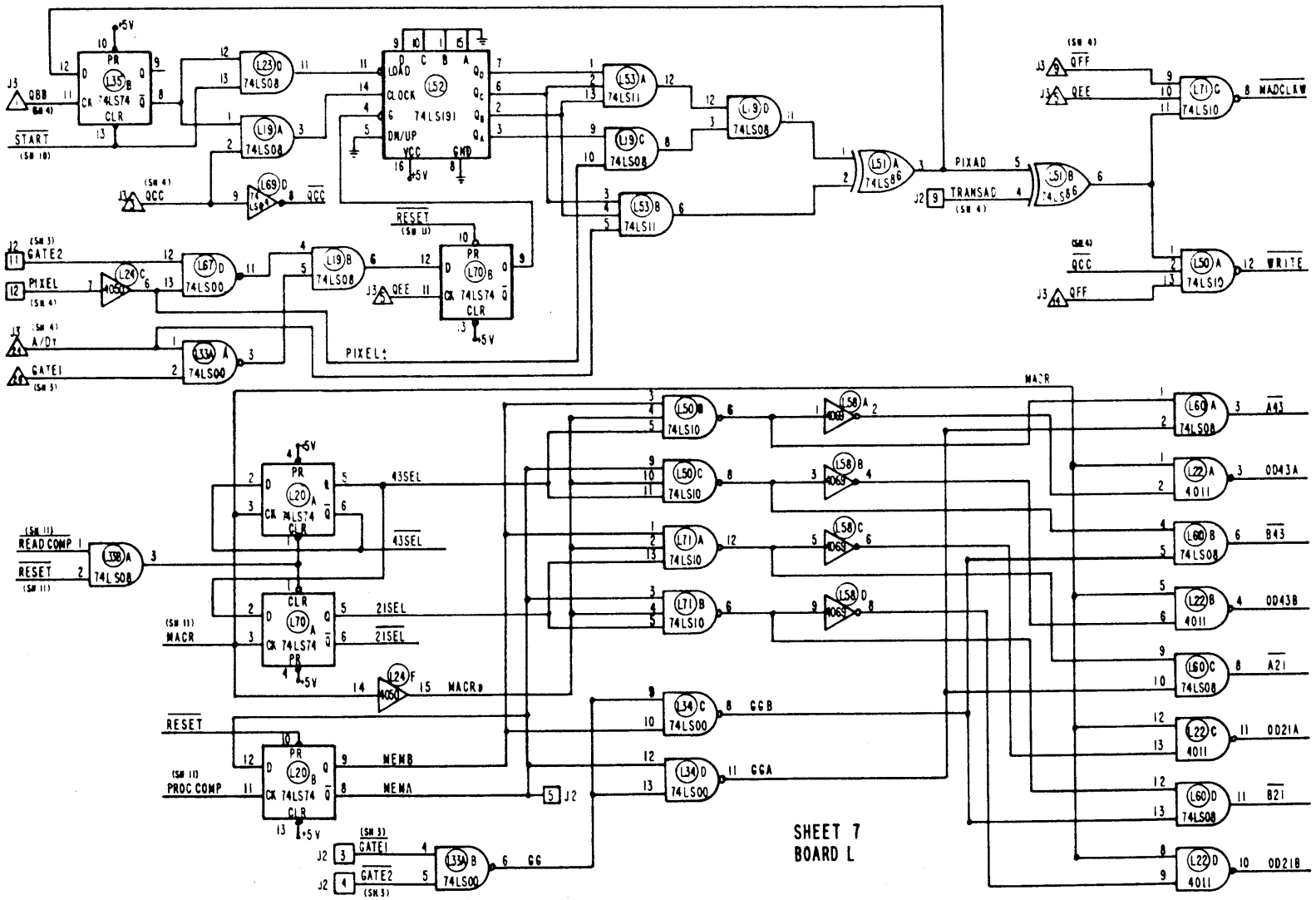

P1
9.216MHz
74LS161
U60
4608
2304
1152
576
CLEAR
LOAD
ENP
ENT
CK
CO
+5V
1K
RESET
U49
4024
576 C
288
144
072
036
018
009
(MSB)
U48
4051
INH
COM OUT
U36 B
4069
U18 F
4050
U18 A
CLOCK
J2
16
J1
50
(Sh 11)
STROBE0
DOUT7
DOUT6
DOUT5
DOUT4
DOUT3
DOUT2
DOUT1
DOUT0
4508 - 0
U37
F2
F1
F0
(Sh 11)
RESET
U31 A
4013
U31 B
J2
6
(Sh 11)
CPSTART
U28 C
4071
J2
1
(Sh 11)
RESET
20K
150pF
R/C
74123
U44
J2
44
RCLOCK
COMP
START
S3
U42 A
4066
S2
U42 B
RSTART
41
J2
U63
1K
STCMOS
U18 B
4050
PRESTART
16
J3
S1
U42 C
60Hz START
U27
4081
U29 A
4013
U29 B
4013
27K
IN914
.05μF
U22
U23
3130
60pF
U24
1K
U24
IN914
J1
18
J2
14
SCAN
SCAN
BLANK2X
BLANK2X
J2
43
BLANK
CLOCK
U50 A
4013
U50 B
4013
U51 A
4073
U51 B
4073
SS
ES
U54 A
4049
SS T
J3
18
SHEET 2
BOARD U

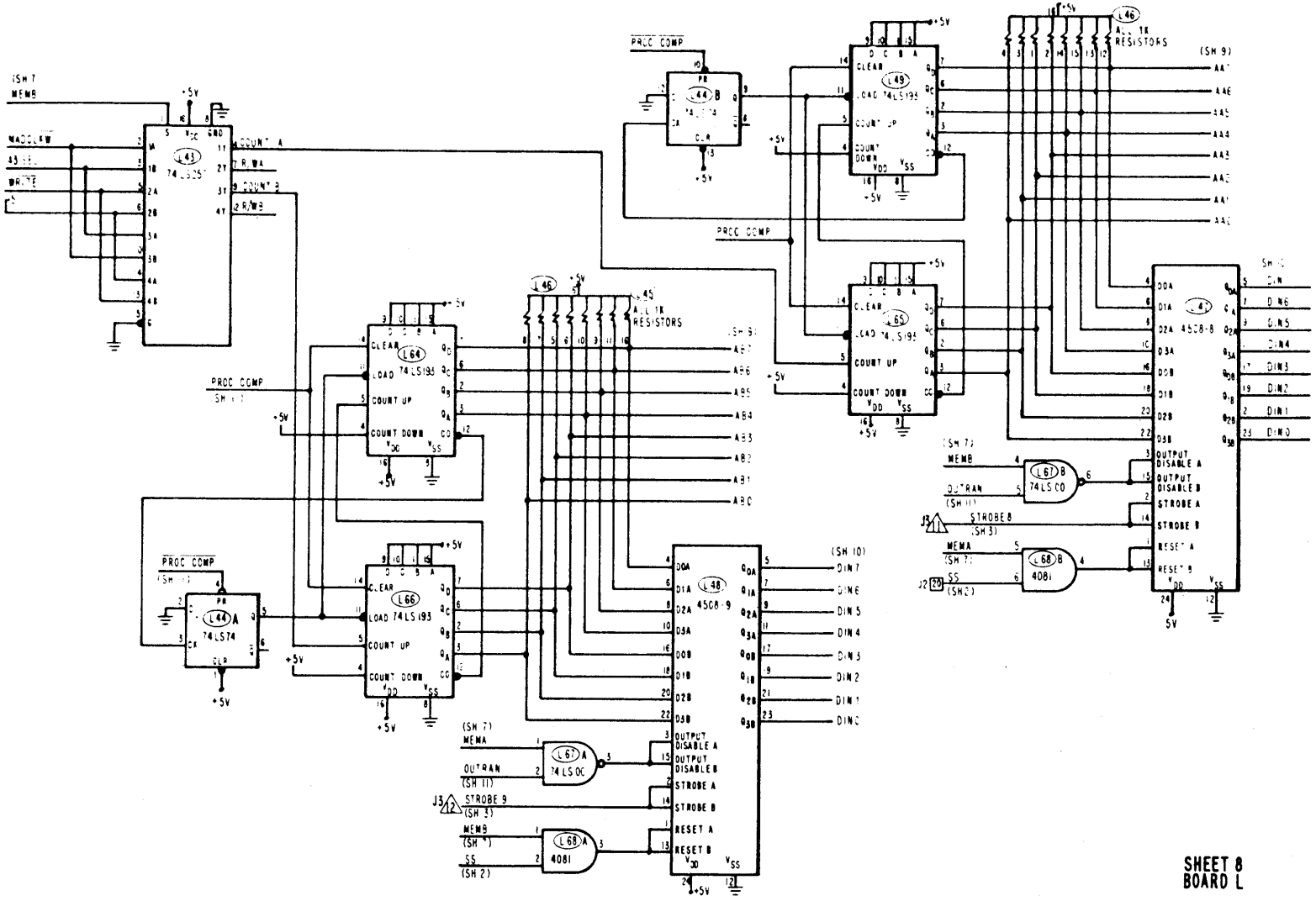

SHEET 3
BOARD U


ANALOG VID
BLANK
QAA
START CONVERT
ADC-SH4B
4042
DI4
DI3
DI2
DI1
QFF
QHH
74LS74
74LS08
74LS00
CLOCK
74LS164
START
9.216 MHZ
QAA
QBB
QCC
QDD
QEE
QFF
QGG
QHH
DOUT7
DOUT6
DOUT5
DOUT4
DOUT3
DOUT2
DOUT1
DOUT0
4508-1
4063
PIXEL
A/D
TRAN.
STRL
STROBE1
RESET
DIG VID
QBB
STORE VID
TRCLK
TRANSITION
TRCLEAR
GATE3
TRANSAD
QCC
QEE
STROBE
QAA
QDD
191 LOAD
START
GATE2
SLOAD1
SLOAD2
SHEET 4
BOARD U

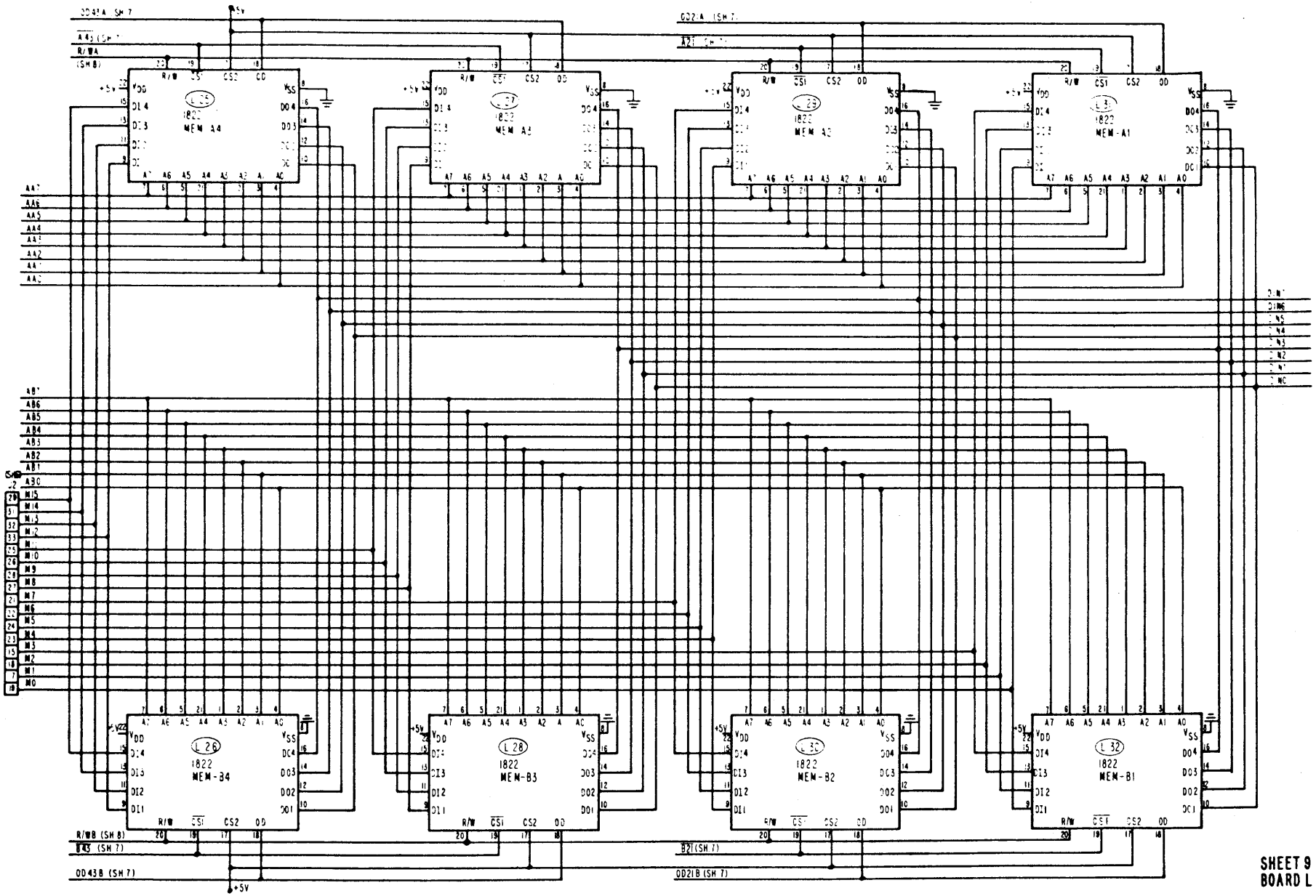

U28A
4071
U28B
4071
U13
4508-5
DOUT7
DOUT6
DOUT5
DOUT4
DOUT3
DOUT2
DOUT1
DOUT0
CAM3
CAM2
CAM1
J5
J6
J8
J2
RESET
STROBES
U46
74LS191
U59
U63
STORE VID
MEMA
U40
4508
M15
M14
M13
M12
M11
M10
M9
M8
STROBE
OD
191 LOAD
CLOCK
U69
U63
U8 & U63 ARE 1K
RESISTOR PACKS
U41
4508
M7
M6
M5
M4
M3
M2
M1
M0
BLANK2X
U35
4049
U57
74LS191
SHEET 5
BOARD U


DI4
DI3
DI2
DI1
QEE
A/D
A/D↑
PIXEL
DIG VID
GATE2
QBB
PREGATE
GATE1
BLANK
BLANK
195CLOCK
195CLEAR
M15
M14
M13
M12
M11
M10
M9
M8
M7
M6
M5
M4
M3
M2
M1
M0
(1K RESISTORS)
SHEET 6
BOARD U

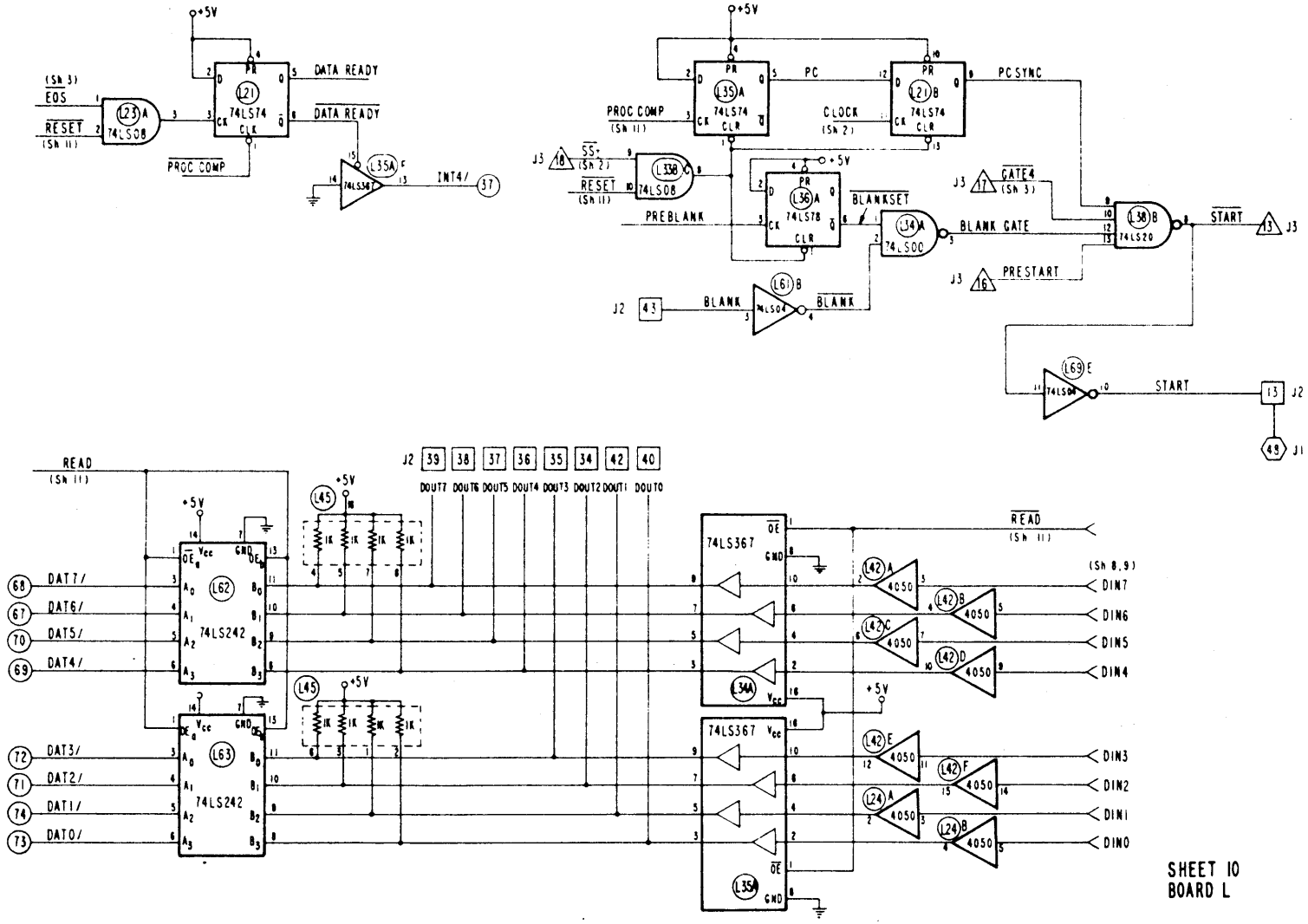

+5V
QBB
START
QCC
GATE2
PIXEL
A/D1
GATE1
RESET
PIXEL1
PIXAD
TRANSAD
QFF
QEE
MADCLKW
WRITE
MACR
43SEL
21SEL
READ COMP
MACRD
MEMB
MEMA
PROC COMP
GG
GGB
GGA
A43
0D43A
B43
0D43B
A21
0D21A
B21
0D21B
74LS74
74LS08
74LS11
74LS191
74LS86
74LS10
74LS00
4011
4069
4050
SHEET 7
BOARD L



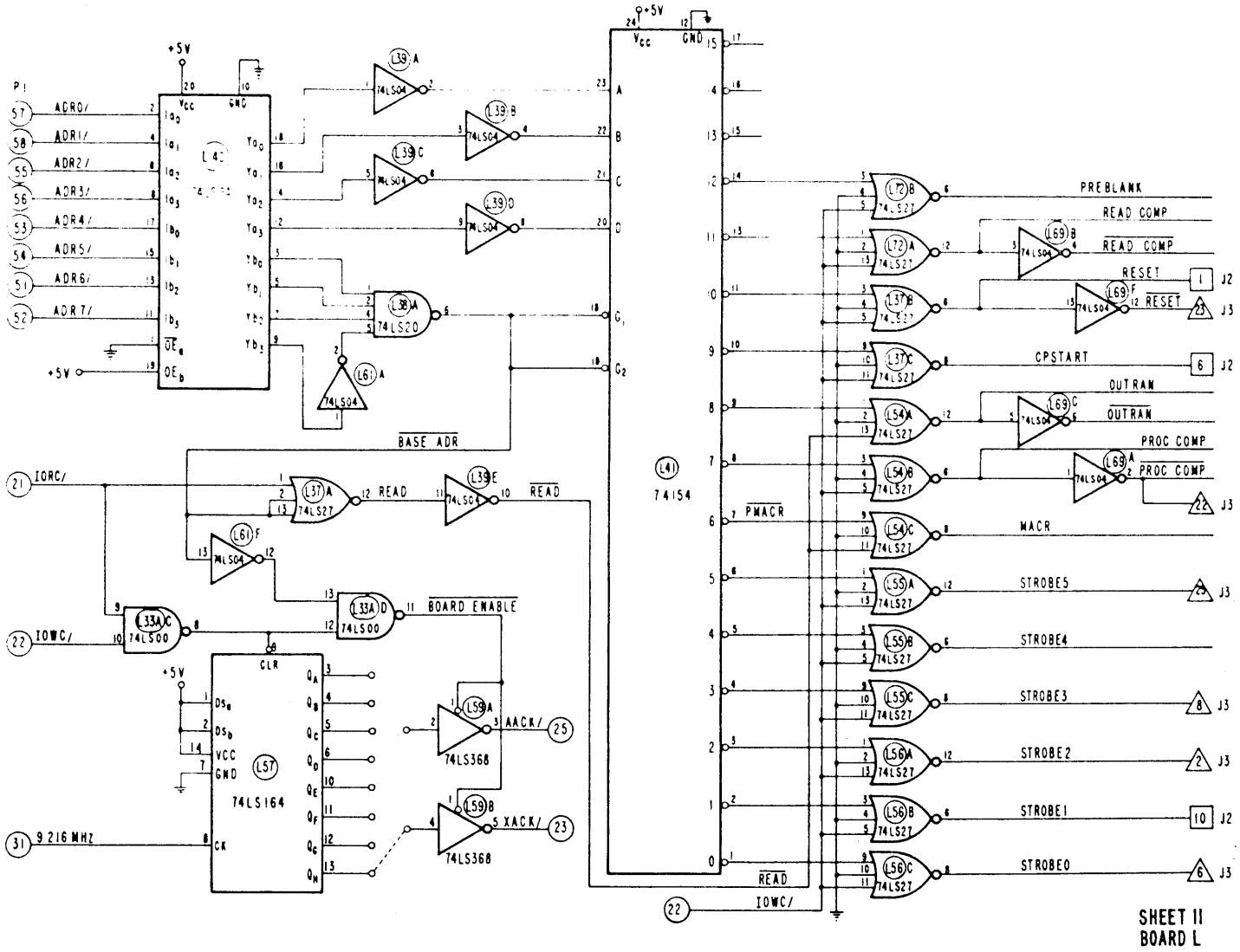
SHEET 8
BOARD L

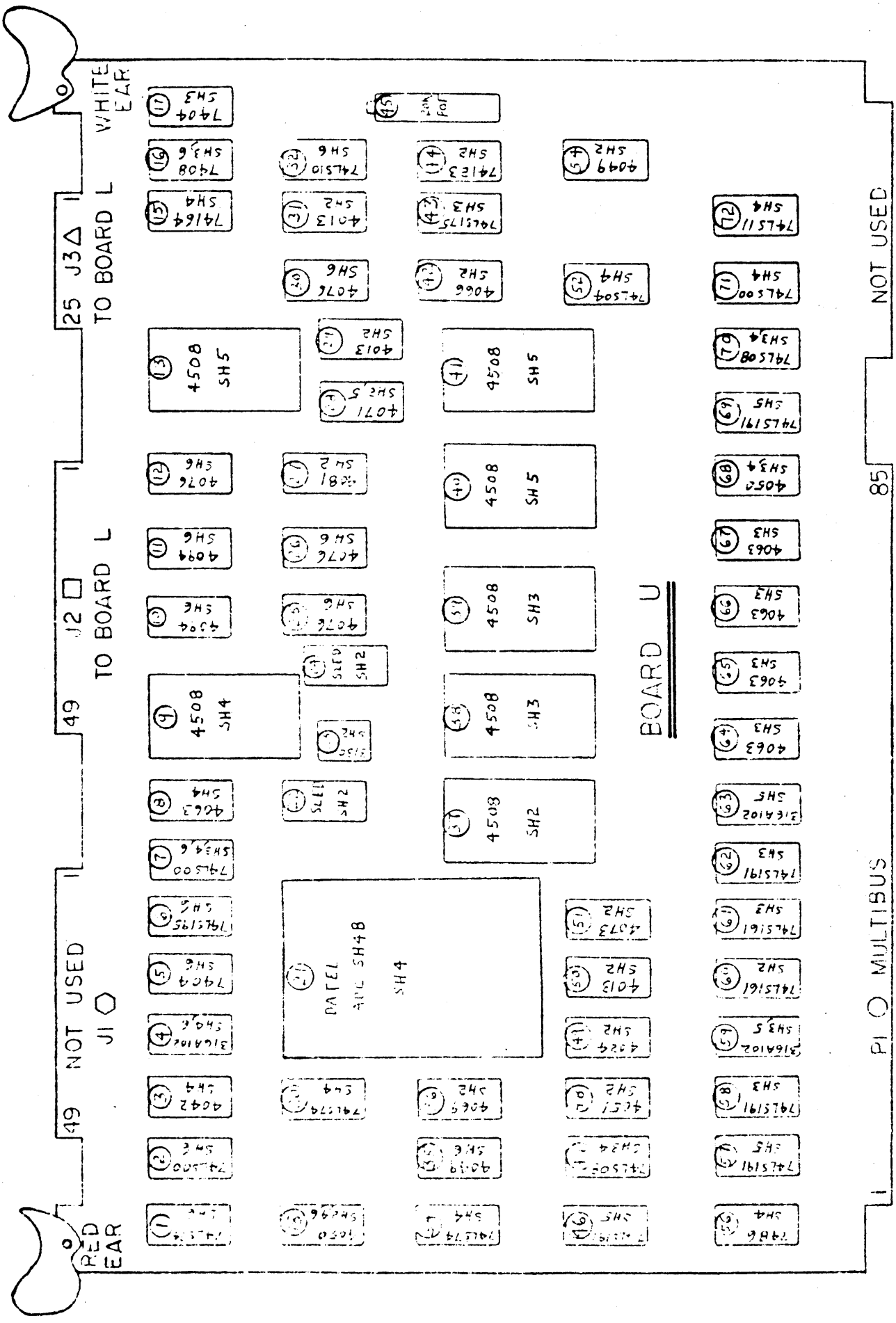


SHEET 9
BOARD L



SHEET 10
BOARD L


P1
ADR0/
ADR1/
ADR2/
ADR3/
ADR4/
ADR5/
ADR6/
ADR7/
+5V
L40
74LS688
L39 A
L39 B
L39 C
L39 D
74LS04
L38 A
74LS20
L61 A
BASE ADR
L41
74154
IORC/
IOWC/
L37 A
74LS27
READ
L39 E
L61 F
L33A C
L33A D
74LS00
BOARD ENABLE
9.216 MHZ
L57
74LS164
CLR
L59 A
74LS368
AACK/
L59 B
XACK/
PMACR
L72 B
L72 A
L37 B
L37 C
L54 A
L54 B
L54 C
L55 A
L55 B
L55 C
L56 A
L56 B
L56 C
PREBLANK
READ COMP
RESET
CPSTART
OUTRAN
PROC COMP
MACR
STROBE5
STROBE4
STROBE3
STROBE2
STROBE1
STROBE0
L69 A
L69 B
L69 C
L69 F
J2
J3
SHEET II
BOARD L


WHITE EAR
RED EAR
25 J3Δ
TO BOARD L
49 J2 □
TO BOARD L
49 NOT USED
J1 ○
NOT USED
85
P1 ○ MULTIBUS
BOARD U
4508 SH5
4508 SH4
4508 SH3
4508 SH2
PATEL SHAB SH4
74LS00
74LS04
74LS08
74LS11
74LS74
74LS175
74LS191
74LS195
4013
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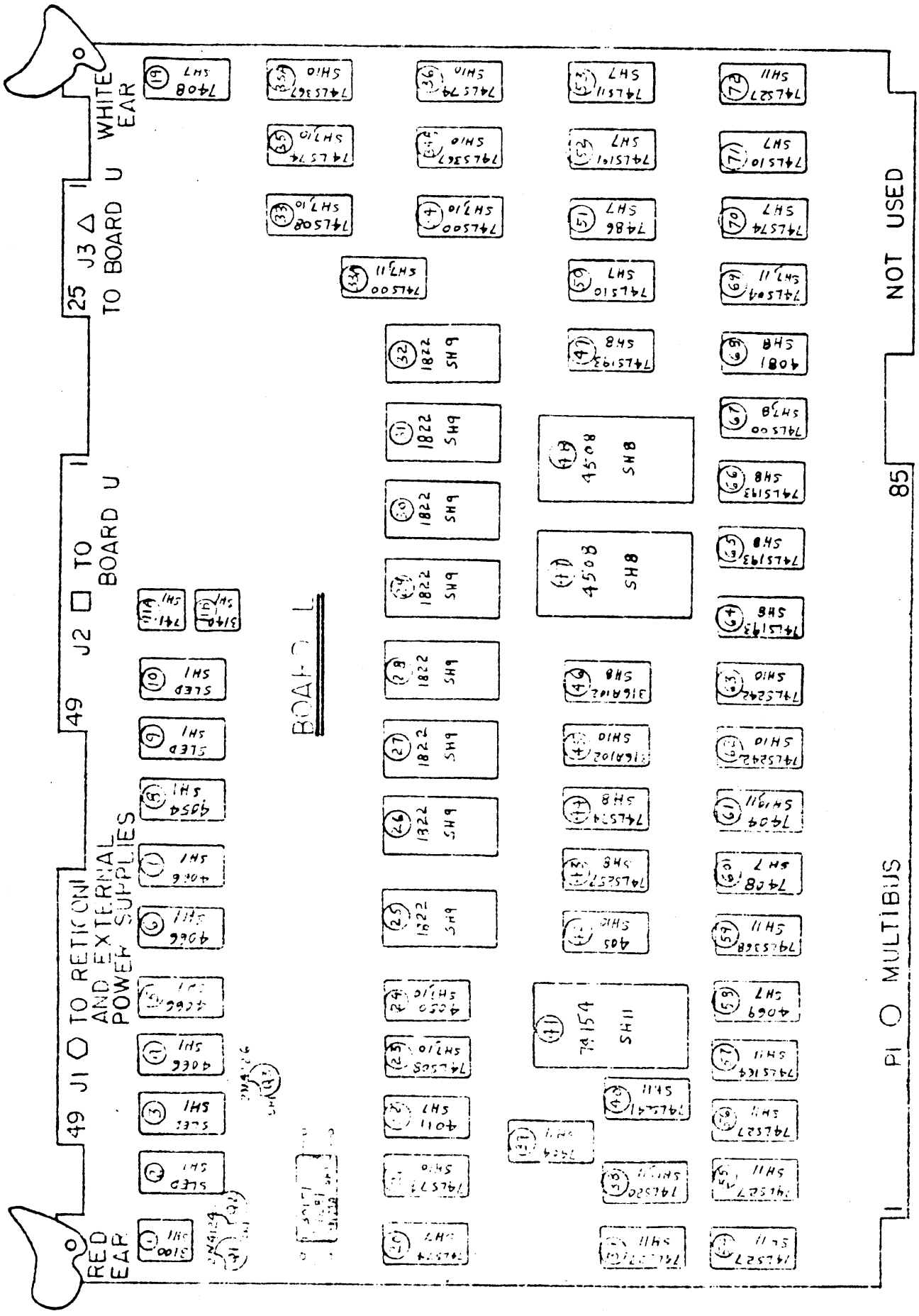
25 J3 △ 1 TO BOARD U WHITE EAR
49 J2 □ 1 TO BOARD U
49 J1 ○ TO RETICON AND EXTERNAL POWER SUPPLIES
RED EAR
BOARD L
1 P1 ○ MULTIBUS 85
NOT USED

J1 (BD.2 - EXT.*)		J2 (BD.2 - BD.1)		J3 (BD.2 - BD.1)	
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	+15 V	1	RESET	1	ØBB
2	-15 V	2	576 KHZ	2	
3	GND	3	GATE1/	3	ØCC
4	RCLOCK3	4	GATE2/	4	MEMB
5	RCLOCK1	5	MEMA	5	ØEE
6	RCLOCK2	6	CPSTART	6	STROBE0
7	60 HZ	7		7	STROBE2
8		8	ØHH	8	STROBE3
9		9	TRANSAD	9	ØFF/
10	RSTART1	10	STROBE1	10	
11		11	GATE2	11	STROBE8
12	RSTART2	12	PIXEL	12	STROBE9
13		13	START	13	START/
14		14	60 HZ	14	ØFF
15		15	M3	15	EOS/
16	RSTART3	16	CLOCK	16	PRESTART
17		17	M1	17	GATE4/
18		18	M2	18	SSt/
19		19	M0	19	
20	BLANK1	20	SS	20	
21		21	M7	21	
22		22	M6	22	PROC.COMP./
23		23	M4	23	RESET/
24		24	M5	24	A/Dt
25		25	M11	25	STROBE5
26	BLANK3	26	M10	26	GATE1
27		27	M8		
28	BLANK2	28	M9		
29		29	M15		
30		30	ANALOG VID		
31		31	M14		
32	VID1	32	M13		
33		33	M12		
34		34	DOUT2		
35		35	DOUT3		
36		36	DOUT4		
37		37	DOUT5		
38	VID3	38	DOUT6		
39		39	DOUT7		
40	VID2	40	DOUT0		
41		41	RSTART		
42		42	DOUT1		
43		43	BLANK		
44		44	RCLOCK		
45		45	CAM3		
46		46	CAM2		
47		47	GND		
48	START	48	CAM1		
49		49	+15 V		
50	CLOCK	50	-15 V		

*RETICON UNIT, POWER SUPPLIES, and 60 HZ LINE

SIGNAL NAME	J1	CABLE	RETICON*
BLANK from RETICON	20	19	P2-D
START from RETICON	10	9	P2-B
CLOCK from RETICON	8	7	P2-C
VIDEO from RETICON	32	31	P2-N
GND	3	4	P2 1-22
+5	18	17	P2-E
START to RETICON	48	47	P2-A
CLOCK to RETICON	50	49	P2-Z
60 HZ	14	13	**

*RC-100A EDGE CONNECTOR PINS
**LINE VOLTAGE DOESN'T GO TO RETICON

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Sig GND
	3	+5V	+5VDC	4	+5V	+5VDC
	5	+5V	+5VDC	6	+5V	+5VDC
	7	+12V	+12VDC	8	+12V	+12VDC
	9	-5V	-5VDC	10	-5V	-5VDC
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknow	24	INH1/	Inhibit 1 disable RAM
	25	AACK/	Advance Acknow	26	INH2/	Inhibit 2 disable PROM or ROM
	27			28		
	29			30		
	31	CCLK/	Constant Clk	32		
	33	INTA/	Intr Acknow	34		
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77			78		
	79	-12V	-12VDC	80	-12V	-12VDC
	81	+5V	+5VDC	82	+5V	+5VDC
	83	+5V	+5VDC	84	+5V	+5VDC
	85	GND	Signal GND	86	GND	Signal GND

GLOSSARY

In the following definitions, a "/" is used in place of the overbar that appears in the schematics. In cases where a signal is used in both negative true and positive true forms, only one form, usually the positive true form, is defined. Imbedded blanks in signal names are not significant - CAM1 and CAM 1 refer to the same signal. Finally, the information appearing in parentheses immediately following the signal name indicates, in most cases, the point of origin of that signal.

AACK/ (L59-3) - Advanced acknowledge signal, sent on bus to CPU in response to memory read or memory write command.

AA7-AA0 (pins 7,6,2,3 of L49 and L65) - "A" memory address

AB7-AB0 (pins 7,6,2,3 of L64 and L66) - "B" memory address

ADR7/-ADR0/ (P1-52,51,54,53,56,55,58,57) - 8 bus address lines, with ADR7/ being the most significant bit (MSB)

ANALOG VID (L10-15) - 0-+1 volt boxcar video signal

A/D (U9-19) - Selector bit for A/D (or 4-bit data) mode

A/Dt/ (U35-4) - TTL version of A/D/

A21/ (L60-8) - Chip Enable for memories A2 and A1 (L29 and L31)

A43/ (L60-3) - Chip Enable for memories A4 and A3 (L25 and L27)

BASE ADR/ (L38-6) - Low when upper digit on address bus (base address) is 8

BCLK/ (P1-13) - Bus clock, asynchronous to CPU clock

BLANK (J2-43) - Reticon signal that is low from just before the 1st piece of VIDEO data is sent out until just after the last is sent out and is high during the blanking period

BLANK GATE (L34-3) - high when all is ready for a START pulse to be generated

BLANKSET/ (L36-6) - set low by PREBLANK to assure that BLANK GATE is high when needed to generate a START pulse

BLANKx (J1-26,22,20) - BLANK signal coming from camera x

BLANK2X (U50-13) - Follows BLANK, 2 CLOCK periods later

BOARD ENABLE/ (L33A-11) - Allows AACK/ or XACK/ onto the multibus

B21/ (L60-11) - Chip Enable for memories B2 and B1 (L30 and L32)

B43/ (L60-6) - Chip Enable for memories B4 and B3 (L26 and L28)

CAMX (U13-5,7,9) - Selector bit for camera x

CCLK/ (P1-31) - Constant Clock, 9.216 MHZ signal sent out on multibus by SBC 80/20 board

Clock - Any clock input or clock generated

CLOCK (U18-2,5) - Basic clock for the photodiode array and for the interface

COMP.START (U31-13) - Computer-generated Start signal

COUNT A (L43-4) - Clock for the "A" memory address counters

COUNT B (L43-9) - Clock for the "B" memory address counters

CPSTART (L37-8) - Computer signal used to generate COMP.START

CPU - Central processor unit

DATA READY/ (L21-6) - Enables INT4/ to be sent as soon as data in the GATE area has been stored in interface memory

DIG VID (U20-9) - 1-bit digital video data signal

DIN7-DIN0 (L42-3,5,7,9,11,14 and L24-3,5) - Data being sent to the data bus (and thus to the CPU) from the interface

DI4-DI1 (U3-2,10,11,1) - 4-bit, or A/D, data

DOUT7-DOUT0 (J2-39,38,37,36,35,34,42,40) - Data being sent to the interface from the CPU via the data bus

END GATE - L7-L0 - Upper eight bits of the photodiode address marking the end of the GATE area

EOS (U16-3) - Positive pulse generated when the GATE area has been passed, should really be EOG (for End of Gate)

ES (U51-6) - End-of-Scan - Positive pulse generated just after the end of the scan

GATEx (U43-2,7,10,15) - Follows PREGATE, on the xth rise of CLOCK thereafter

GATE area - That portion of the photodiode array whose output is to be processed by the interface; START GATE and END GATE delimit the GATE area

GG (L33A-6) - High as long as either GATE1 or GATE2 is high

GGA (L34-8) - Low when "A" memories being written into

GGB (L34-11) - Low when "B" memories being written into

H7-H0 (U38-5,7,9,11,17,19,21,23) - END GATE

INT4/ (L35A-13) - Set low when data in the GATE area has been stored in interface memory and is ready for transfer to SBC 80/20 memory

IORC/ (P1-21) - I/O Read Command - Bus signal that is low when the address of an input port is on the address bus

IOWC/ (P1-22) - I/O Write Command - Bus signal that is low when the address of an output port is on the address bus and corresponding data is on the data bus

L7-L0 (U39-5,7,9,11,17,19,21,23) - START GATE

MACR (L54-8) - Signal sent out by the computer when it wants to read interface memory - serves as the Clock for the Memory Address Counters during the Read cycle

MACRd (L24-15) - Delayed version of MACR

MADCLKW/ (L71-8) - Memory Address Counter Clock for the Write cyle

MEMA (L20-8) - High when "A" memories being written into

MEMB (L20-9) - High when "B" memories being written into

MUX (L43) - Quad 2-line-to-1-line multiplexer

M15-M0 (J2-29,31,32,33,25,26,28,27,21,22,24,23,15,18,17,19) - 16 data inputs to the interface memories

OD (U68-2) - Output Disable input for U40 and U41 latches

OUTRAN (L54-12) - Signal sent out by the computer to read the number of interface memory addresses filled during the

last scan

OD21A (L22-11) - Output Disable input for memories A2 and A1 (L29 and L31)

OD21B (L22-10) - Output Disable input for memories B2 and B1 (L30 and L32)

OD43A (L22-3) - Output Disable input for memories A4 and A3 (L25 and L27)

OD43B (L22-4) - Output Disable input for memories B4 and B3 (L26 and L28)

PA11-PA0 (pins 7,6,2,3 of U62, U61, U58) - Photodiode Address, used to generate PREGATE

PC (L35-5) - Process Complete flip-flop - Set high when PROC.COMP is sent out by the computer

PCSYNC (L21-9) - PC synchronized to CLOCK

PIXAD (L51-3) - High when PIXEL or A/D data ready to be, or in process of being, written into interface memory

PIXEL (U9-17) - Selector bit for PIXEL (or 1-bit digital data) mode

PIXELt (L24-6) - TTL level version of PIXEL

PMACR/ (L41-7) - "PREMACR" - goes low to generate MACR

PREBLANK (L72-6) - Signal sent out by the computer to set BLANK GATE high to assure, in turn, that a START signal can be generated

PREGATE (U47-8) - Signal that is high as long as the upper eight bits of the photodiode address are larger than the START GATE and smaller than the END GATE

PRESTART (U18-4) - Signal selected by user from the 3 Start signals to become START farther down the line

PROC.COMP (L54-6) - Process Complete signal sent out by the computer, when both processing and scanning have been completed, to prepare the interface for a new scan

QAA-QHH (U15-3,4,5,6,10,11,12,13) - Signals that follow the CLOCK signal 1 to 8 9.216 MHZ Clocks later, respectively

Q3-Q0 (U9-5,7,9,11) - 4-bit quantizing level, chosen by the user

and used to convert A/D data to 1-bit PIXEL data

READ (L37-12) - Signal that is high when the computer is reading (receiving data) from the interface

RESET (L37-6) - Signal sent out by the computer to initialize the interface boards

RCLOCKx (J1-4,6,8) - Internal Clock signal coming from camera x

RSTARTx (J1-16,12,10) - Internal Start signal coming from camera x

R/WA (L43-7) - Read/Write signal that is low when the "A" memories are being written into

R/WB (L43-12) - Read/Write signal that is low when the "B" memories are being written into

SCAN/ (U50-1) - Follows BLANK on next CLOCK

SCANt/ (U68-10) - TTL version of SCAN/

SCR - Status Control Register

SLOAD1 and SLOAD2 (U71-6,8) - Signals that control the loading of the string length counters (U46, U69, U57) with zeros between scans and at the end of each string

SS (U51-9) - Positive pulse generated just after the start of a scan

SSt/ (U54-2) - TTL version of SS/

Start - Any start signal other than the one sent to the cameras (START)

START (L69-10) - Positive Start signal sent out to the cameras

START CONVERT (U20-5) - Narrow positive pulse sent to the A/D converter to start the conversion of the video coming from the Reticon camera (in the form of ANALOG VID) from a boxcar signal to 4-bit, or A/D, data

START GATE - H7-H0 - upper eight bits of the first photodiode address in the GATE area

STCMOS (U18-5) - CMOS version of PRESTART

STORE VID (U34-6) - holds the state of the data of the string at the time that STR.L or TRAN mode data is written into

interface memory

STR.L (U9-23) - Selector bit for STR.L (string length data) mode

STROBE (U68-4) - Signal to strobe TRAN or STR.L data into latches U40 and U41

STROBEx (L56-8,6,12; L55-8,12;) - Computer-generated signal to load data into SCRx, where x is 0, 1, 2, 3, or 5; and (U16-6,8) - interface-generated signal to load last memory address written into, into latch L47 or L48, where x is 8 or 9, respectively

TRAN (U9-21) - Selector bit for TRAN (transition data) mode

TRANSAD (U72-6) - Signal that goes high to generate signals to store STR.L or TRAN data in interface memory

TRANSITION (U34-9) - Signal that goes high when a transition occurs

TRCLEAR (U34-13) - Signal that resets TRANSITION to zero

TRCLK (U56-3) - Signal that sets TRANSITION high when a transition occurs

uF - Microfarad

um - Micron

us - Microsecond

VIDEO (L4-2,3,9) - Boxcar video signal (from the designated camera) to be processed by the interface

VIDEO-CP (page 7) - Charge-pulse video output of the photodiode array

VIDx (J1-38,40,32) - Boxcar video signal coming from camera x

WRITE/ (L50-12) - Signal used to generate R/WA or R/WB to allow data to be written into interface memory "A" or interface memory "B," respectively

XACK/ (L59-5) - Transfer acknowledge signal sent to the CPU on the multibus to indicate the completion of an I/O Read or Write operation

ØA (U36-4) - Delayed, inverted version of ØB

ØB (U48-3) - Selected CMOS Clock, used to generate the TTL CLOCK

191 LOAD (U72-8) - Signal that controls the loading of the STR.L or TRAN counters (U46, U69, and U57)

195 CLEAR (U16-11) - Signal used to clear U6, thus disabling data from being loaded into latches U30, U25, U12, and U26

195 CLOCK (U7-6) - Clock for U6

21SEL (L70-5) - Signal that goes high when either memories A2 and A1 or memories B2 and B1 are being read from

43SEL (L20-5) - Signal that goes high when either memories A4 and A3 or memories B4 and B3 are being read from

60 HZ START (U27-4) - Start signal generated from the line voltage

9.216 MHZ (P1-31) - CLock sent out by the SBC 80/20 on the multibus as CCLK/