Substrate Engineering for Monolithic Integration of III-V Semiconductors with Si CMOS Technology

by

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Bachelor of Science with Honors in Materials Science and Engineering
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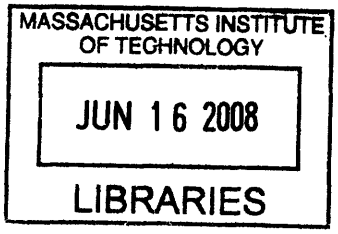

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ABSTRACT

Ge virtual substrates, fabricated using $Si_{1-x}Ge_x$ compositionally graded buffers, enable the epitaxial growth of device-quality GaAs on Si substrates, but monolithic integration of III-V semiconductors with Si CMOS using this platform is hampered by the large thickness of the $Si_{1-x}Ge_x$ graded region. To address this issue, the Silicon on Lattice-Engineered Silicon (SOLES) was developed, consisting of a silicon-on-insulator (SOI) structure fabricated on a Ge virtual substrate. Placement of the Si device layer at the surface makes it possible to process this platform similarly to typical SOI wafers, with the added functionality of a buried III-V template which can be used for GaAs device fabrication. This platform was fabricated using a scalable layer transfer technique. AlInGaP LEDs were also demonstrated on a SOLES substrate.

In addition, an alternative growth process was investigated for $Si_{1-x}Ge_x$ virtual substrates with lower threading dislocation density (TDD) and thickness. This process, the thermally relaxed ultra-thin (TRUT) buffer process, consists of coherent growth of lattice-mismatched $Si_{1-x}Ge_x$ layers, followed by post-growth annealing. Growth of TRUT buffers over the $Si_{0.5}Ge_{0.5}$ to $Si_{0.3}Ge_{0.7}$ alloy range with high strain levels resulted in the nucleation of surface defects which appear to limit the maximum strain rate of compositionally graded buffers. However, application of the TRUT process in the $Si_{0.1}Ge_{0.9}$ to Ge alloy range resulted in relaxed Ge virtual substrates with a 59% reduction in TDD compared to conventional processes.

Lastly, growth of high-quality lattice-matched $GaAs_yP_{1-y}$ on $Si_{0.5}Ge_{0.5}$, $Si_{0.3}Ge_{0.7}$, and $Si_{0.2}Ge_{0.8}$ virtual substrates was investigated. Adaptation of standard GaAs on Ge processes to this heteroepitaxial system resulted in mostly non-planar growth (similar to typical GaP growth on Si) with only limited regions of planar $GaAs_yP_{1-y}$ layers on $Si_{0.2}Ge_{0.8}$ virtual substrates. Planar growth of $GaAs_yP_{1-y}$ on $Si_{0.3}Ge_{0.7}$ virtual substrates was enabled by minimizing the atmospheric exposure of the $Si_{0.3}Ge_{0.7}$ as it is transferred between growth reactors, establishing that the $GaAs_yP_{1-y}$ growth process on $Si_{1-x}Ge_x$ is strongly affected by atmospheric contaminants. Further minimization of air exposure, through use of $Si_{1-x}Ge_x$ homoepitaxial buffers and growth of $Si_{1-x}Ge_x$ and $GaAs_yP_{1-y}$ in a

single reactor, is expected to further improve epitaxial quality across the entire lattice-matched $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ range, including GaP on Si.

Thesis Supervisor: Eugene A. Fitzgerald
Title: Merton C. Flemings-SMA Professor of Materials Science and Engineering

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Acknowledgements

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Chapter 1: Motivation for CMOS/III-V Monolithic Integration

1.1 Introduction

Since its invention in 1959, the integrated circuit has demonstrated remarkable robustness and capacity for ever-improved performance. For over four decades, a concerted effort by the microelectronics industry has produced an exponential increase in device density of integrated circuits, which has been the benchmark of progress in the semiconductor industry for most of its existence. This rate of increase, first observed by Gordon Moore and commonly referred to as "Moore's Law," has held remarkably steady throughout this time and continues to this day, as shown in the plot of microprocessor transistor count versus time in Figure 1.1.

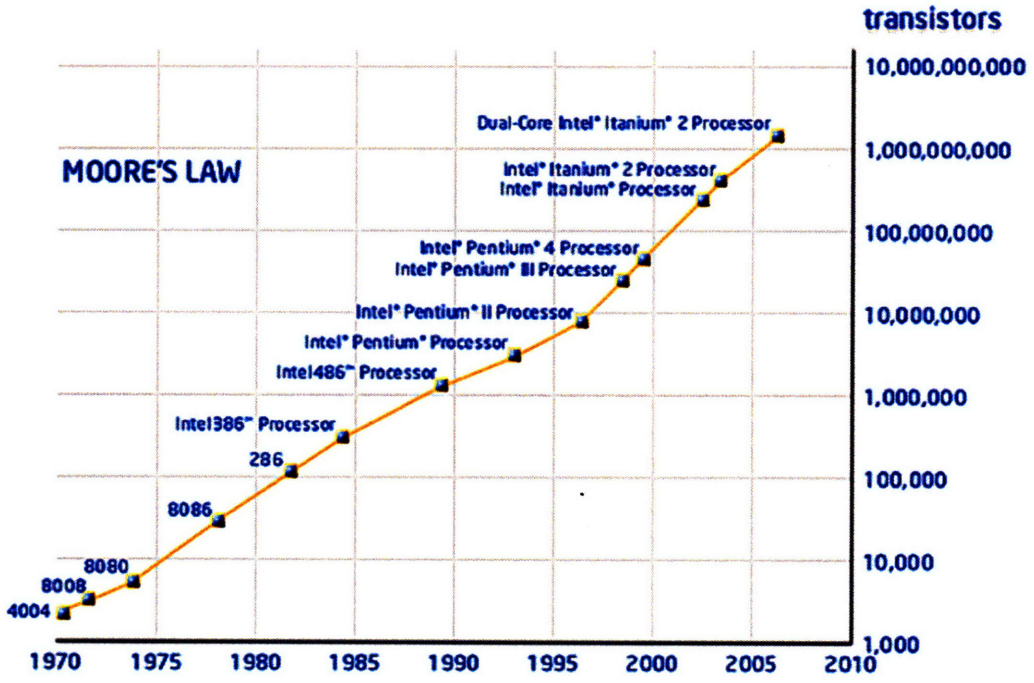


Figure 1.1 – Plot of Intel microprocessor transistor count versus year, illustrating the exponential growth rate known as "Moore's Law." Figure adapted from Intel corporation web site [1].

This remarkable rate of progress has been made possible by the scaling of microelectronic devices to ever smaller dimensions. It is a fortuitous fact that almost every metric for device performance: device speed, power consumption, cost per device;

improves with decreased device size. Device scaling has proven to be an extremely effective way to greatly improve the performance and cost of integrated circuits, thus enabling the pervasiveness of electronics in modern society.

While the use of scaling has provided enormous benefit over the years, there are clear signs that this strategy is reaching fundamental limitations that cannot be overcome by scaling alone. The end of scaling has been erroneously predicted repeatedly over the years, but problems related to the ever-shrinking device size are already plaguing the industry. The gate length of CMOS transistors has been progressively pushing the diffraction limit of photolithography techniques used to define device features. While photolithography technology has managed to keep pace with performance demands, it does so at an ever increasing cost which at some point will no longer be cost-effective. In addition, the thickness of the gate oxide in modern transistors has now reached atomic dimensions, which clearly cannot be much further reduced. In addition, the dramatic reduction of device size and increase in devices per integrated circuit has required both an increased length and reduced linewidth of metal interconnects, which has reduced their performance and made them increasingly a "bottleneck" for IC performance. Scaling has continued to advance despite these obstacles, but these advances require larger and larger investments in capital equipment with each new technology "node," and the cost-benefit breakdown for scaling is becoming less and less favorable as scaling continues. Thus, scaling alone cannot provide the performance improvements required if Moore's Law is to hold.

In order to mitigate the problems of continued scaling, the semiconductor industry is increasingly introducing new materials to complement its efforts in scaling. In the

early years of the scaling paradigm, CMOS ICs were composed almost entirely of just three materials: silicon (along with trace dopants), silicon dioxide, and aluminum. New materials were gradually added to the CMOS process for certain very specific applications (such as tungsten vias for connection between interconnect layers), but most of the components of the chip were fabricated using the traditional material set. However, as scaling becomes increasingly difficult, semiconductor manufacturers are increasingly finding the introduction of new materials to provide a very valuable strategy for continued improvement.

Numerous examples of these new materials can already be seen. The industry is now using $Si_{1-x}Ge_x$ sources and drains in its MOSFETs for introduction of strained Si channels, improving carrier mobility of this region and thus enhancing device performance. For gate dielectrics, SiO_2 is being replaced by higher-dielectric constant materials such as HfO_2 in order to provide further boosts in MOS capacitance without decreasing the gate dielectric thickness. Metal interconnects in ICs, traditionally made from aluminum, are now fabricated using copper thanks to its lower resistivity and better electromigration characteristics. In addition, SiO_2, the traditional material for inter-layer dielectrics between layers of metal interconnects, is now being replaced by lower dielectric constant materials to reduce RC time constant delays for metal interconnects. These are just a few examples of the increasing shift in the semiconductor industry away from scaling and towards use of new materials for IC performance improvement.

1.2 Optical interconnects for Si CMOS

As mentioned previously, the perpetual shrinking of integrated circuits has put an increasing burden on metal interconnects, whose performance unfortunately does not

improve with increased scaling. In the past, the speed of an integrated circuit was largely defined by the gate delay of the transistors, which defined how quickly they could be turned on and off. Delays due to interconnect data speeds were largely negligible. However, scaling has simultaneously decreased gate delays and increased interconnect delays, with the result that interconnect delays are now the dominant performance-limiting factor for integrated circuits. This is depicted in Figure 1.2. The introduction of copper interconnects and inter-layer dielectrics with a low dielectric constant made a significant improvement in the interconnect delay time, thus providing partial relief of the interconnect bottleneck. However, this improvement can only provide a one-time boost in interconnect performance because of the lack of CMOS-compatible metals with better resistivity than copper and the fact that the cost-benefit comparison of developing new inter-layer dielectrics is continuously decreasing. Thus, the 2007 Interational Technology Roadmap for Semiconductors has projected that "the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs"[2].

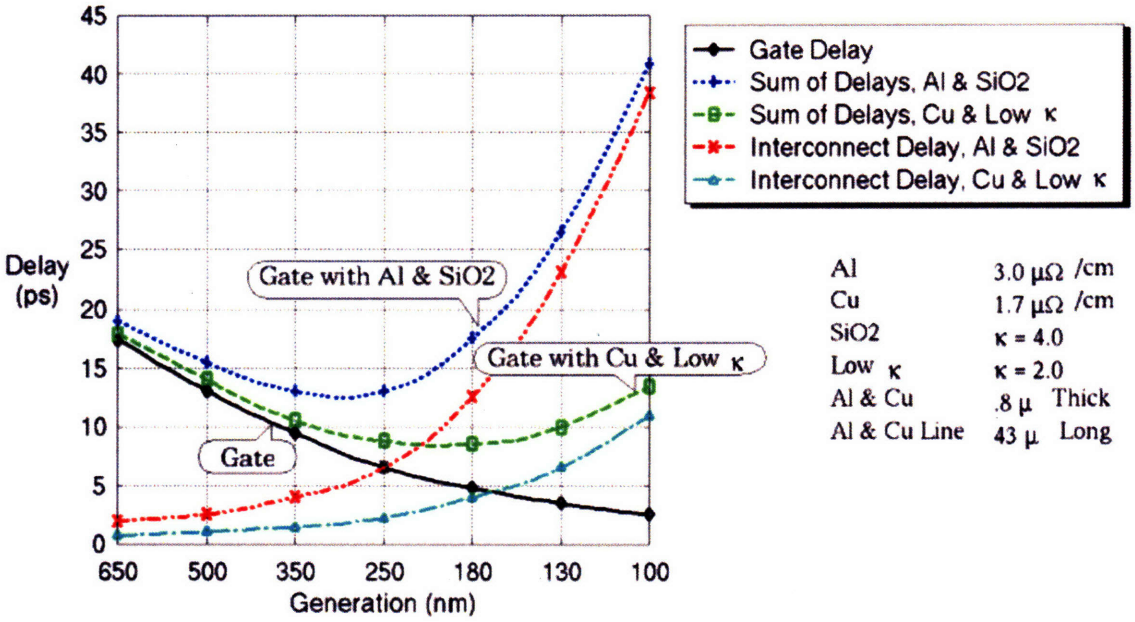


Figure 1.2 – Plot of delay time versus technology generation for CMOS circuits. As device sizes shrink, gate delay (which is essentially the speed limitation of the transistors) continues to decrease, while interconnect delay increases, thus creating an "interconnect bottleneck" for integrated circuit performance. Image adapted from the International Technology Roadmap for Semiconductors (ITRS) [2].

Because of this obstacle, the semiconductor industry is exploring more fundamental changes to how information is transmitted in an integrated circuit. One potential solution that has garnered considerable excitement and interest over the years is the use of on-chip optical interconnect schemes. An optical interconnect system would use light signals to transmit information between different parts of the chip, in the same way that fiber optics are used to transmit information over macroscopic distances. A plot of information transmission capacity versus year of introduction for various communication systems is shown in Figure 1.3. Fiber optics takes advantage of the tremendous bandwidth of near-infrared light (as compared to radio and microwave frequencies) to give a very large increase in data transmission rates.

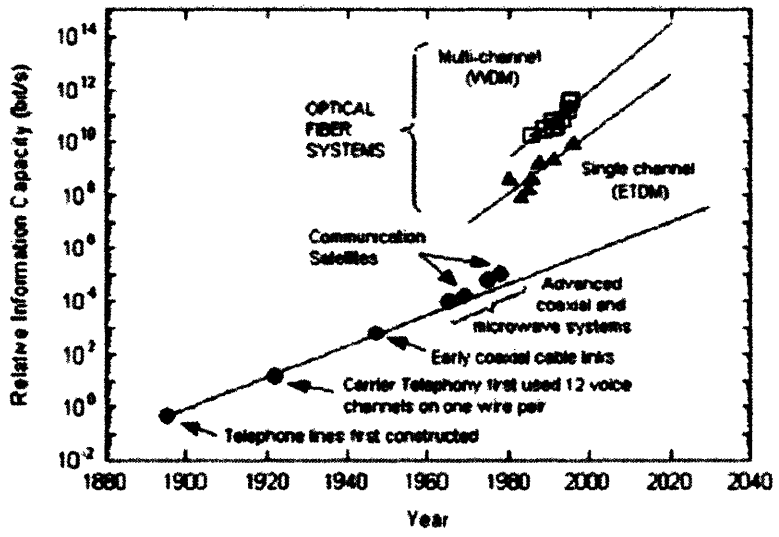


Figure 1.3 – Plot of information transmission capacity versus year of introduction for various telecommunication technologies, illustrating the impressive gains produced by fiber optics [3].

An on-chip optical interconnect system would provide the same increase in bandwidth observed for fiber optics, thus ensuring that interconnects do not serve as a bottleneck to IC speed. Additionally, optical interconnects would not be affected by RC time constant delays and do not suffer crosstalk effects between interconnects. However, the introduction of optical interconnects would require the addition of a vast array of active and passive photonic and optoelectronic components to the traditional CMOS process. This need has created a field known as silicon photonics, and much progress has been made in developing the required components [3-5].

Much of this work has focused on use of Si and $Si_{1-x}Ge_x$ for as many of the components as possible because of its proven CMOS compatibility. However, because of their indirect band gap, Si and $Si_{1-x}Ge_x$ are generally very inefficient as light-emitting materials, despite intense research efforts to overcome this barrier. In contrast, many of the III-V semiconductors, notably those based on GaAs and InP, have a direct band gap and have been used to produce the optoelectronic components that have helped power the

fiber optic revolution. Integration of III-V semiconductors on Si CMOS circuits would enable use of highly mature III-V optoelectronic devices to power an optical interconnect system instead of Si and $Si_{1-x}Ge_x$ devices which have yet to be fully developed.

Methods for integration of III-V semiconductors with Si CMOS can be roughly grouped into two categories: monolithic and hybrid integration, which are depicted in Figure 1.4. Most schemes for hybrid integration involve the separate fabrication of III-V and Si components followed by placement of individual III-V die of III-V onto the Si CMOS IC. This technique offers the advantage that III-V and CMOS devices can be fabricated separately using existing well-established techniques for each material system, only being combined towards the end of the manufacturing process. However, hybrid integration requires very precise alignment of III-V die onto the Si chip. This alignment process is time-consuming and costly, and if the III-V/CMOS process requires a large number of separately bonded die (as an optical interconnect system most likely would), then this would make this process a major obstacle to the cost-effective application of hybrid integration.

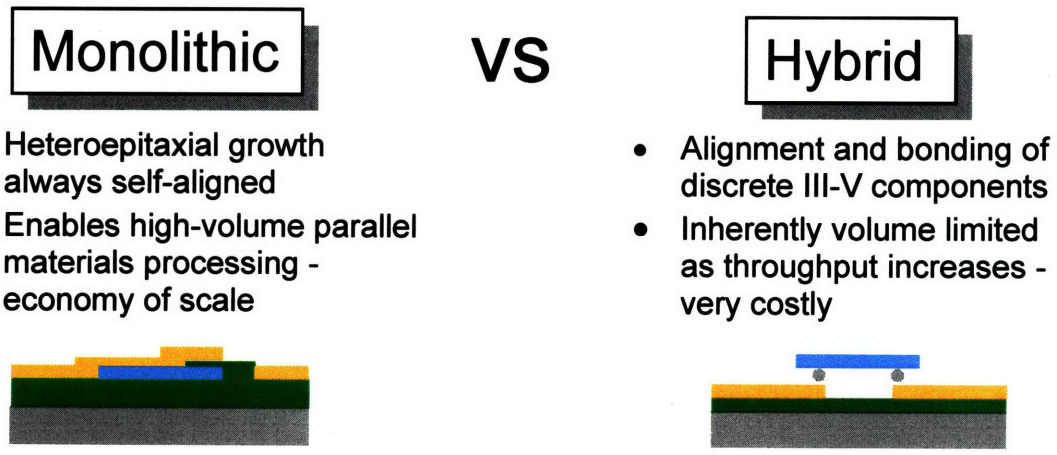


Figure 1.4 – Comparison of monolithic and hybrid integration techniques. Image adapted from Yang [6]

In contrast, monolithic integration entails the processing of III-V of Si CMOS components side-by-side on a single Si substrate. This method eliminates the separate die aligning step and, in principle, it should allow parallel processing of CMOS and III-V devices, thus producing economies of scale and reduced costs. However, the integration of III-V semiconductors with Si CMOS has numerous technological challenges that have prevented it from being implemented to date on a large scale

This thesis will address some of the challenges involved in III-V CMOS optoelectronic integration and present experimental progress in solving these challenges.

Chapter 2: Methods and Challenges of Monolithic CMOS - III-V Integration

Techniques for monolithic integration of III-V semiconductors on Si substrates can be further divided into three categories: direct heteroepitaxial growth, heteroepitaxial growth using $Si_{1-x}Ge_x$ compositionally graded buffers, and wafer-bonding. This chapter will present a basic description of these categories.

2.1 Heteroepitaxial Direct Growth

Heteroepitaxial growth is a common way to integrate different semiconductors together on a single substrate. Heteroepitaxial semiconductor growth has wide application for devices such as lasers, heterojunction bipolar transistors (HBTs), and photodetectors [7]. In the case of III-V/CMOS integration, this strategy requires the use of lattice-mismatched epitaxy. The fundamentals of this process are discussed below.

2.1.1 Fundamentals of Lattice-Mismatched Epitaxy

Lattice mismatch refers to the difference in lattice parameter between the epitaxial film and the substrate. For planar film growth, this lattice mismatch is accommodated by a combination of elastic and plastic strain in the film. This is defined mathematically as follows:

$$f = \frac{a_{sub} - a_{film}}{a_{film}} = \varepsilon + \delta \qquad [2.1]$$

where a_{film} and a_{sub} are the lattice parameters of the epitaxial layer and substrate, respectively; ε is the elastic strain in the film; and δ is the plastic strain. When an epitaxial layer is grown on a substrate, the in-plane lattice parameter of the epitaxial layer initially conforms to the substrate lattice parameter, as shown in Figure 2.1a. In the compressively strained example in this figure, the in-plane lattice parameter of the film (a_{ip}) is compressed to match the substrate lattice parameter (a_{sub}). This compressive strain in the in-plane direction produces a tensile out-of-plane strain in the film via the Poisson

effect, thus lengthening the film out-of-plane lattice parameter (a_{oop}). This distortion of the film lattice is referred to as tetragonal distortion, and the film is said to be under biaxial strain. However, as the thickness of the film increases, the strain energy in the film increases, and above a certain "critical thickness", there will be a thermodynamic driving force for the film to relax this strain by forming misfit dislocations at the interface, as shown in Figure 2.1b.

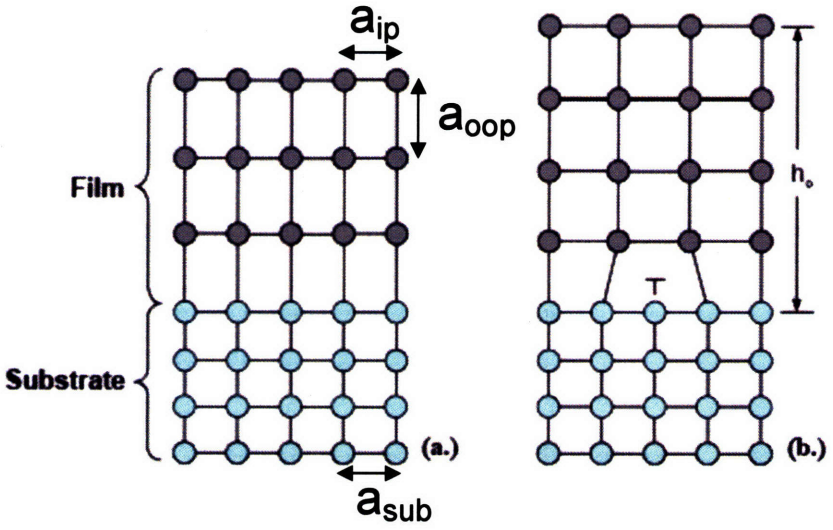


Figure 2.1- Schematic of (a) a coherent compressively strained layer (note the tetragonal distortion in the film lattice) and (b) a compressive partially relaxed layer with a misfit dislocation at the interface. a_{ip} denotes the in-plane lattice parameter of the film, while a_{oop} denotes the out-of-plane lattice parameter of the film. Image adapted from Pitera [8].

The critical thickness mentioned above corresponds to the film thickness at which the equilibrium strain value of the film (determined by minimization of the total energy of the system) equals the misfit between the film and substrate. This critical thickness was first derived by Matthews and Blakeslee [9] and was expressed by Fitzgerald [10]as follows:

$$h_c = \frac{D(1-\nu\cos^2\alpha)(b/b_{eff})[\ln(h_c/b)+1]}{2Yf} \qquad \textbf{[2.2]}$$

where h_c is the critical thickness, D is the average shear modulus, ν is the Poisson ratio of the film, α is the angle between the dislocation line direction and Burger's vector, b and b_{eff} are the magnitude of the full and effective Burger's vectors, Y is the biaxial elastic modulus, and f is the lattice misfit between film and substrate.

Thus, a film grown above its critical thickness will contain a misfit dislocation array at the interface at equilibrium. In addition, to misfit dislocations, a typical partially relaxed layer will also have threading dislocation segments which extend from the interface to the surface of the film. A schematic image of such a film is shown in Figure 2.2. For semiconductor device applications, a misfit dislocation array can be very detrimental to devices that utilize the interface. However, for many device applications, the devices can be fabricated sufficiently close to the film surface to avoid the effect of the misfit dislocation array, and thus only the threading dislocations affect device performance. Thus, in working with relaxed lattice-mismatched films, growing the lattice-mismatched layer with a minimum of threading dislocations is a key concern.

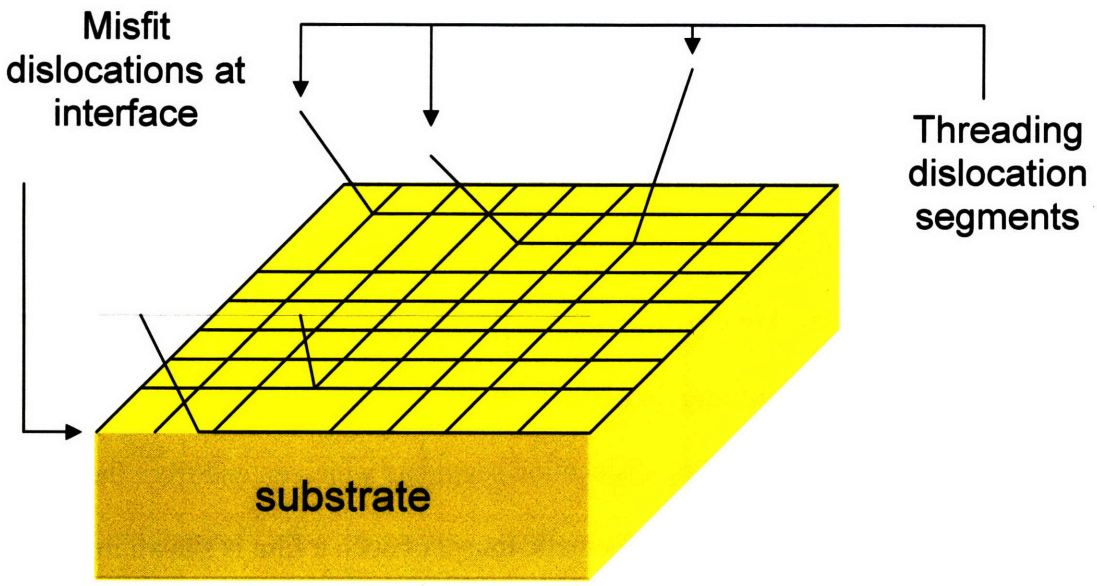


Figure 2.2 – Schematic of a representative partially relaxed lattice-mismatched film, showing a misfit dislocation network at the interface as well as threading dislocation segments that intersect the film surface. The epitaxial layer is represented by the transparent box on top of the substrate.

In the typical relaxation process for low-misfit systems ($f < \sim 2\%$), a misfit dislocation will form by dislocation glide of a threading dislocation segment. This process is illustrated in Figure 2.3. All semiconductors considered in this work possess a diamond cubic or zincblende crystal structure. In these crystal structures, dislocations can glide along {111} planes in <110> directions, thus creating twelve possible slip systems. During film relaxation, threading dislocation segments will glide along these systems, leaving misfit dislocation segments in their wake along the <110> glide directions. Because of the slip system requirements, the misfit dislocations formed by this process are neither pure edge nor pure screw dislocations but rather have an angle of 60° between the dislocation line and the Burger's vector. It should be noted that only the edge component of the misfit dislocation provides strain relief to the film. Thus, edge dislocations would relieve strain more efficiently than 60° dislocations, but pure edge dislocations at the interface would be sessile and could not form by this mechanism. In

general, the relaxation of low-mismatch films proceeds by the mechanism described above, while for high-mismatch systems (f > ~2%), strain is relieved by a combination of 60o and edge dislocations, which form by a different mechanism [10].

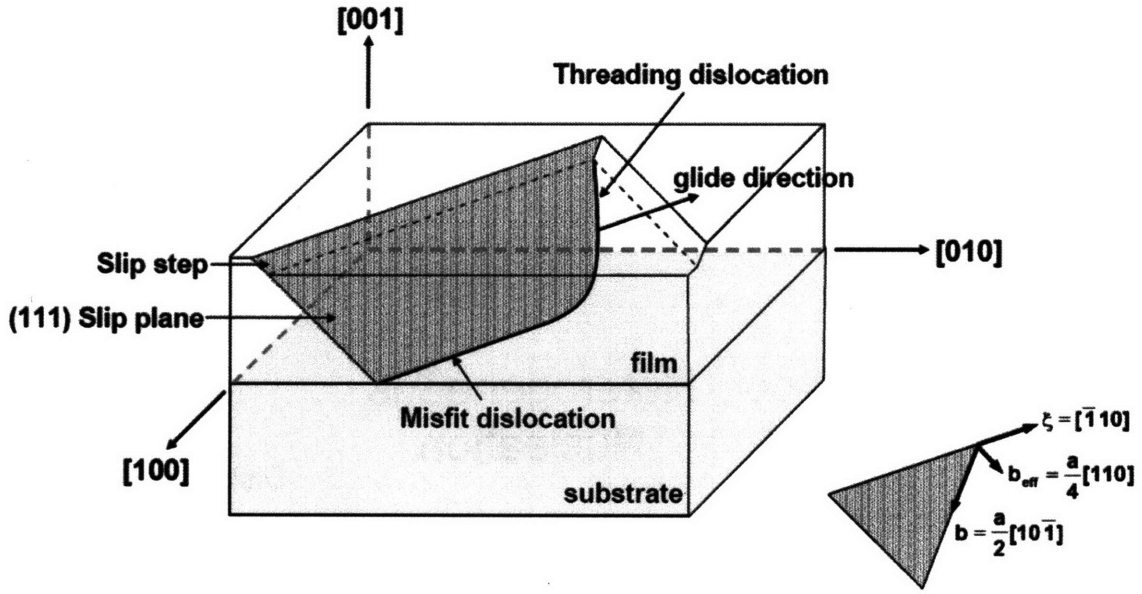


Figure 2.3 – Illustration of process of strain relaxation in an epitaxial layer by dislocation glide. As relaxation progresses, the threading dislocation segment moves in the glide direction, thus extending the misfit dislocation segment. Image adapted from Pitera [8].

In addition to threading dislocation glide by the process described above, threading dislocation nucleation also occurs in lattice-mismatched films. This is shown in Figure 2.4. Nucleation proceeds by the spontaneous formation of an unstable dislocation half-loop at the surface, as shown in part (a). If the half-loop is sufficiently large, it will reach the interface, where it will form a stable configuration consisting of a misfit segment and two threading segments as shown in part (b), which can then cause strain relaxation in the film using the previously described mechanism. However, more frequently, an imperfection at the surface can serve as a site for heterogeneous nucleation (Figure 2.4c,d). Heterogeneous nucleation sites can also sometimes cause pinning of threading dislocations, preventing them from gliding. Both processes are thermally activated, and

heterogeneous nucleation will generally have a lower activation energy than the homogeneous process. Thus, nucleation produces the threading dislocations needed for the film relaxation mechanism.

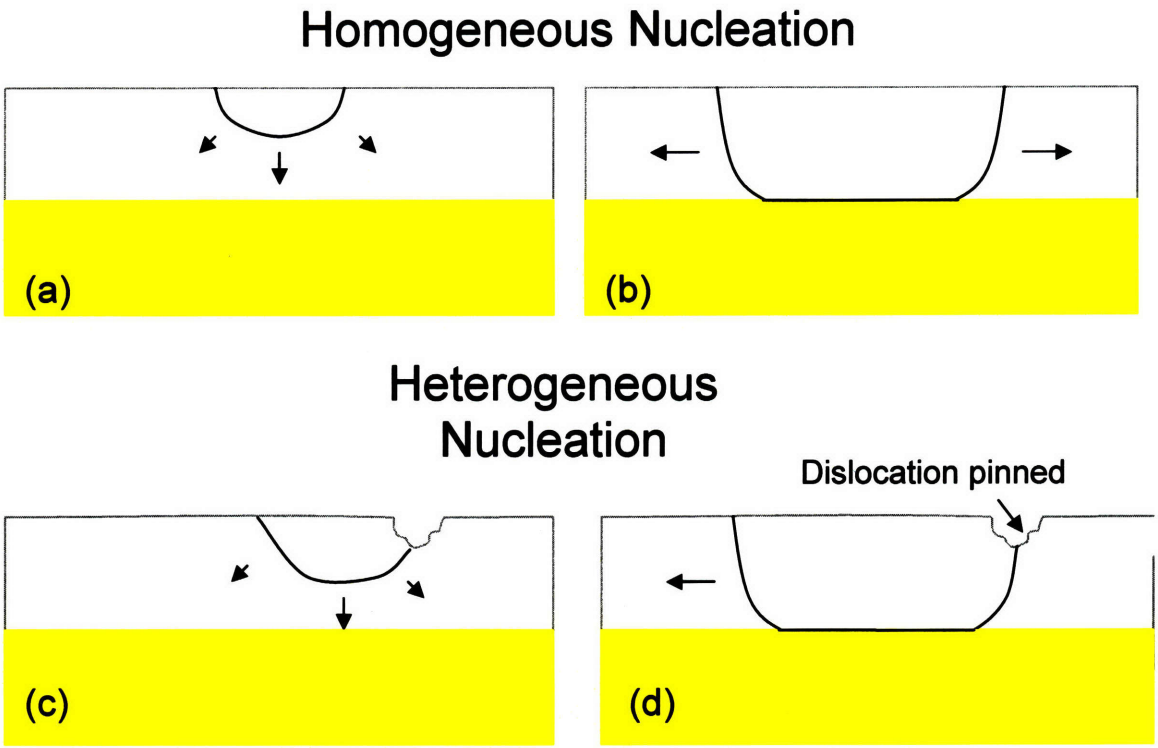


Figure 2.4 – Schematic of dislocation nucleation mechanisms for low misfit epitaxial films. (a) Initial homogeneous nucleation of an unstable dislocation half-loop at the surface of the film, (b) When the half-loop reaches the interface, it forms a misfit segment with two threading segments. (c) and (d) show analogous process for heterogeneous nucleation.

2.1.2 Direct Growth of Lattice-Mismatched Semiconductors

For the integration of III-V semiconductors on Si, the lattice mismatch issue poses a serious problem. Figure 2.5 shows a plot of band gap energy versus lattice constant for several III-V and Group IV semiconductors. The case of epitaxial growth of GaAs on Si and InP on Si are of particular interest because of the large number of existing semiconductor devices fabricated on GaAs and InP substrates. As this figure shows, for the case of GaAs growth on Si, there is a 4.1% lattice mismatch while InP on Si is even worse. This presents a serious impediment to growth of GaAs on Si with a low threading

dislocation density (TDD). During the 1980s, numerous studies attempted to achieve direct growth of this semiconductor on Si substrates, but despite a great deal of effort, the best results in which TDD was measured still routinely gave TDD values of $\sim 10^8$ cm^{-2} [11]. By contrast, GaAs substrates typically have TDD of 10^3 cm^{-2} [7].

Another growth system which has received wide attention is the direct growth of Ge on Si. Ge on Si has nearly the same lattice mismatch as GaAs on Si, but this growth system has received more attention recently due to greater acceptance by the semiconductor industry of Ge as a material that is compatible with typical CMOS processing. Luan [12] has demonstrated a process for direct growth of Ge on Si with TDD of 2×10^7 cm^{-2}. While this TDD is sufficient for some device applications, such as Ge photodetectors on Si, it still results in a limitation of device performance.

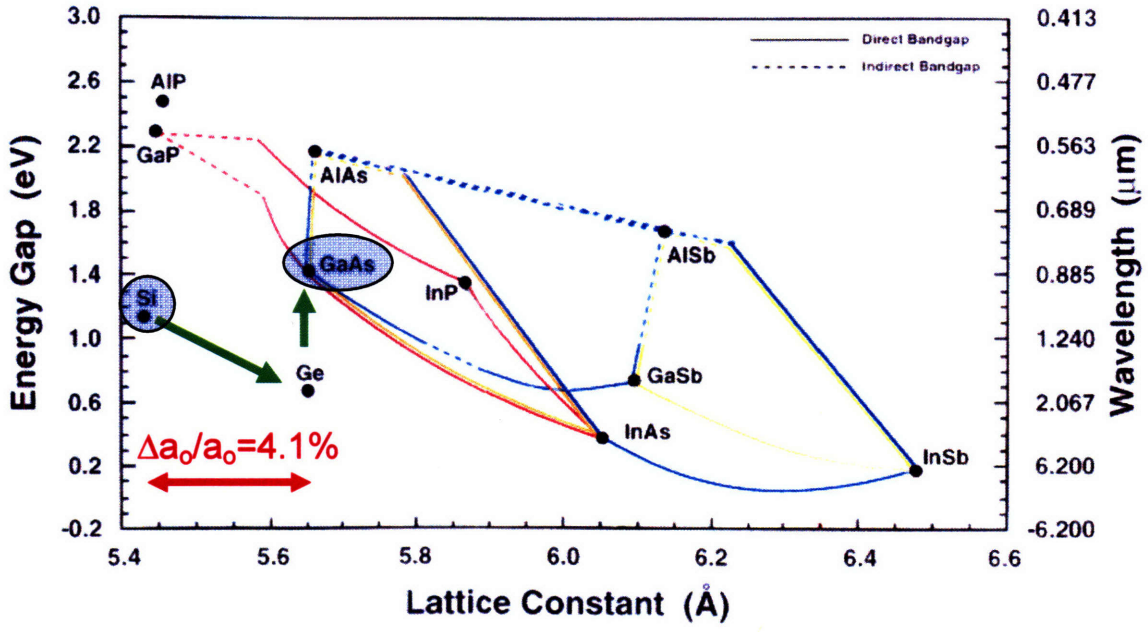


Figure 2.5 – Plot of band gap energy versus lattice constant for several III-V and Group IV semiconductors. In the case of GaAs on Si, there is a 4.1% lattice mismatch, which results in a high TDD for direct epitaxial growth. TDD of this process can be greatly improved by use of $Si_{1-x}Ge_x$ compositionally graded buffers graded to pure Ge, which is closely lattice-matched to GaAs.

2.2 $Si_{1-x}Ge_x$ Compositionally graded buffers

2.2.1 General Description

The growth of high-quality GaAs on Si underwent a major breakthrough with the development by Fitzgerald [13] of $Si_{1-x}Ge_x$ compositionally graded buffers. In the $Si_{1-x}Ge_x$ compositionally graded buffer process, films $Si_{1-x}Ge_x$ with incrementally increasing Ge content are deposited on a Si substrate, as shown in Figure 2.6. A typical $Si_{1-x}Ge_x$ graded buffer uses a Ge increment of ~2%, thus ensuring that each heteroepitaxial interface in the graded buffer is very low mismatch ($f \sim 0.08\%$). The $Si_{1-x}Ge_x$ alloy system is fully miscible, thus allowing $Si_{1-x}Ge_x$ alloys of any Ge fraction to be deposited without phase separation issues. In the $Si_{1-x}Ge_x$ graded buffer, each layer is grown above the critical thickness at high temperature in an effort to relax each layer as fully as possible so as to minimize the buildup of strain in the structure.

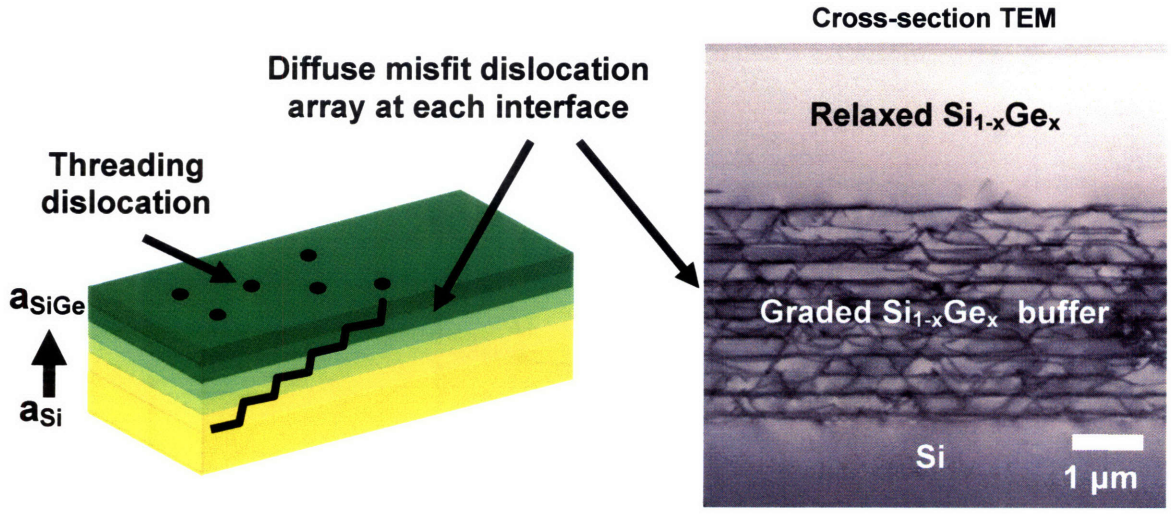


Figure 2.6 – Schematic and cross-sectional TEM of a $Si_{1-x}Ge_x$ compositionally graded buffer. Image adapted from Gupta [14].

2.2.2 $Si_{1-x}Ge_x$ Compositionally Graded Buffer Growth

The typical process for graded buffer growth involves continuous layer deposition in which the $Si_{1-x}Ge_x$ layers relax as they are grown. In this procedure, Fitzgerald

proposed [15] and Leitz showed experimentally [16] that $Si_{1-x}Ge_x$ graded buffers should be grown at high temperature to maximize dislocation velocity and to ensure that there is minimal strain buildup in the graded buffer as it is grown. As described by Pitera [17], the maximum growth temperature in UHVCVD is limited by gas-phase nucleation of SiH_4 and GeH_4 precursor molecules, which can result in roughening of the graded buffer. With this effect taken into account, the standard growth temperatures established by Pitera with this technique are shown in Figure 2.7.

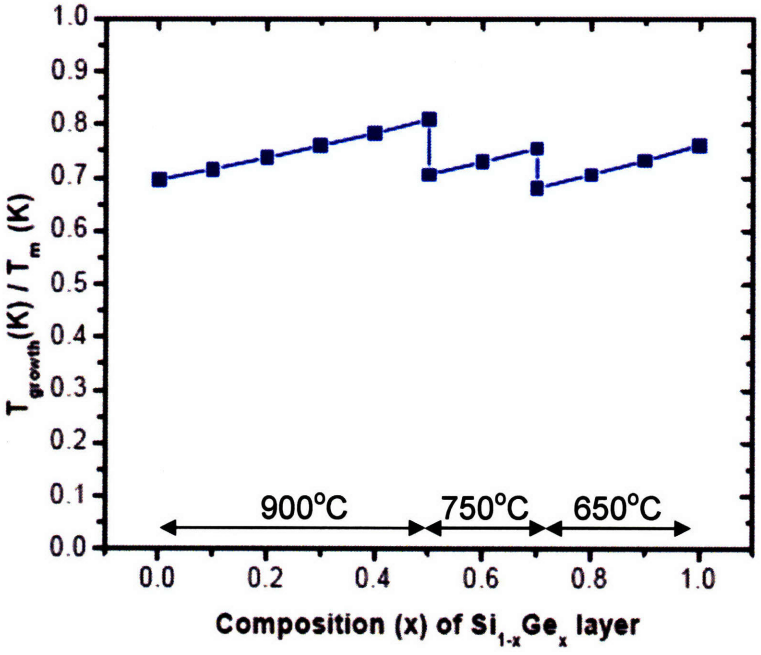


Figure 2.7 – Plot of homologous temperature (T/T_{melt}) versus Ge content used in the "conventional" process for $Si_{1-x}Ge_x$ compositionally graded buffers. The temperatures employed are 900°C for x_{Ge} = 0-50%, 750°C for x_{Ge} =50-70%, and 650°C for x_{Ge} = 70-100%. Figure adapted from Pitera [8].

The basic theory of compositionally graded buffer growth was described in full by Fitzgerald [15]. At high temperatures, it is assumed that the layer has sufficient thermal energy to stay in Matthews-Blakeslee equilibrium throughout growth.

After an initial density of threads is nucleated in the first few layers of buffer growth, the TDD should be relatively constant under certain conditions. Fitzgerald also

formulated a simplified quantitative relation for threading dislocation density as a function of growth rate, grading rate, and temperature. This is given below:

$$TDD = \frac{2R_g R_{gr} e^{E_{glide}/kT}}{bBY^m \varepsilon_{eff}^m} \quad [2.3]$$

where R_g is the growth rate of the $Si_{1-x}Ge_x$ layers, R_{gr} is the grading rate (defined as the mismatch per unit thickness), T is the temperature, E_{glide} is the activation energy for dislocation glide, b is the Burger's vector magnitude, B is a constant, Y is the elastic modulus, and m is an exponent with value generally between 1 and 2. From this expression one sees that the TDD increases with increases in both growth rate and grading rate. Thus, for lowest TDD, it would seem logical to reduce both these values, but there are practical limitations on both these factors. The growth rate cannot be altered appreciably with making the growth time impractically long, while Currie [18] has shown that very slow grading rates (5%Ge/μm) lead to cracking in the graded buffer as the sample cools from the growth temperature to room temperature due to the large thickness of thermal-expansion mismatched material. Currie showed that a 10%Ge/μm grading rate avoided this issue, thus putting a limit on this variable.

Experiments with $Si_{1-x}Ge_x$ graded buffers have validated the general trend of the relaxed graded buffer equation. Leitz measured the field TDD of the $Si_{1-x}Ge_x$ graded buffer as a function of Ge content of the cap layer using this procedure; this is shown in Figure 2.8 [16]. The figure shows that the field TDD in the graded buffer initially increases sharply from the substrate TDD level (which is less than 1 cm^{-2}) and then remains relatively stable, although a (near) monotonic increase in TDD is still observed as the Ge content of the buffer increases. One contributor to this gradual monotonic

increase observed is the effect of misfit dislocation strain fields on the semiconductor epitaxy process [19]. These low-level strain fields produce crosshatch and impede the motion of dislocations, thus necessitating nucleation of new threading dislocations to further relax the material. The formation of crosshatch is cumulative as the graded buffer grows, thus making the problem more severe as the Ge content of the buffer is increased.

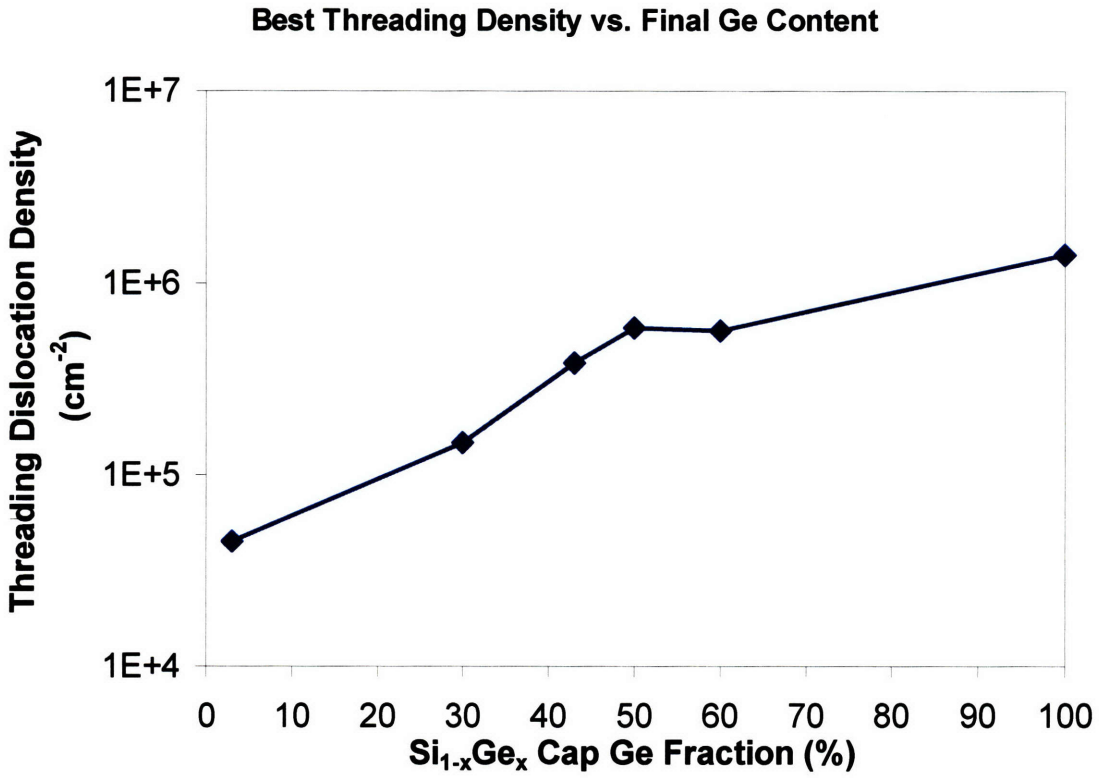


Figure 2.8: Plot of best attained threading dislocation density (TDD) versus Ge content of $Si_{1-x}Ge_x$ cap for "conventional" $Si_{1-x}Ge_x$ compositionally graded buffers. The conventional buffers were graded at a rate of 10%Ge/μm. Figure adapted from Leitz [16].

The role of crosshatch in the TDD evolution of compositionally graded buffers was further established by the work of Currie [18], which showed that the TDD of buffers graded from pure Si to pure Ge can be greatly improved through the use of chemo-mechanical planarization to remove crosshatch at the $Si_{0.5}Ge_{0.5}$ layer before growing the graded buffer from $Si_{0.5}Ge_{0.5}$ to pure Ge. In this study, the combination of high-

temperature growth (using temperatures of Figure 2.7), grading rate of 10%Ge/μm, and use of CMP at the $Si_{0.5}Ge_{0.5}$ layer to remove surface roughness will be referred to as the "conventional" process for the $Si_{1-x}Ge_x$ compositionally graded buffer growth.

2.2.3 Application of $Si_{1-x}Ge_x$ compositionally graded buffers

Compositionally graded buffers are very useful as "virtual substrates" for other epitaxial structures. Because Ge is closely lattice-matched to GaAs, a Ge virtual substrate can be used for the growth of GaAs on Si with low TDD. Figure 2.9 shows a plot of the minority carrier lifetime of GaAs grown on Ge virtual substrates as compared to direct growth of GaAs on Si and GaAs on Ge substrates. As the figure indicates, GaAs on Ge virtual substrates has much longer minority carrier lifetimes than direct GaAs on Ge with much higher TDD. In addition, the minority carrier lifetime of GaAs on Ge virtual substrates has nearly reached the saturation point at which minority carrier lifetime does not change with further decreases in TDD.

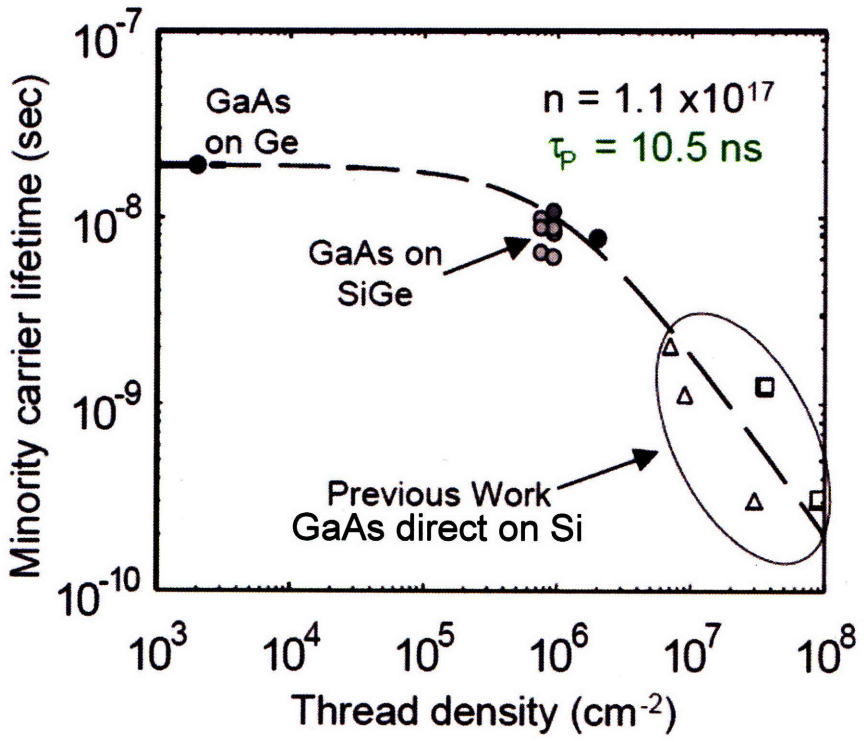


Figure 2.9 – Minority carrier lifetime versus threading dislocation density for n-type heteroepitaxial GaAs layers. The previous work was direct growth of GaAs on Si by Yamaguchi [20]. **Image adapted from** [21].

In addition to minority carrier lifetimes that approach saturation values, Ge virtual substrates have been used for fabrication of numerous GaAs-based devices whose performance compares favorably to control samples fabricated on GaAs wafers. A wide array of GaAs-based devices have been fabricated, including GaAs [22] and InGaP [23] solar cells; AlGaAs heterojunction bipolar transistors [24]; GaAs [25], strained InGaAs [26], and AlInGaP [27] lasers; and an integrated AlGaAs LED-waveguide-photodetector optical link [28].

As an example of GaAs device performance on Ge virtual substrates, consider the AlGaAs/GaAs laser on Ge virtual substrate studied by Groenert [25]. A plot of optical output power versus current (L-I curve) for lasers fabricated on Ge virtual substrates and GaAs substrates is shown in Figure 2.10. This figure shows that the L-I curve for lasers

on Ge virtual substrates was comparable to that of nominally identical lasers fabricated on GaAs substrate after the laser process was optimized to address issues particular to laser fabrication on the Ge virtual substrate, including surface roughness, Ge autodoping of the laser structure, and cleaving of the laser facets. However, as shown in Table 2.1, while many of the important metrics of laser performance compare favorably to the GaAs substrate control sample, the device lifetime was still severely limited for lasers on Ge virtual substrates, which Groenert concluded was caused by a degradation mechanism which is accelerated at higher TDD.

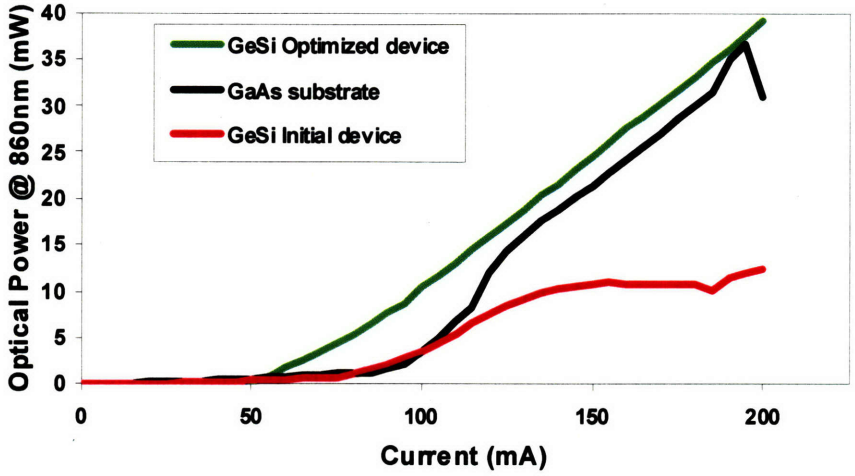


Figure 2.10 – Plot of optical output power versus input current for AlGaAs/GaAs lasers fabricated on Ge virtual substrates and a GaAs substrate. After optimization of the laser process, the laser on Ge virtual substrate gives comparable performance to an identical laser fabricated on a GaAs substrate. Image adapted from Groenert [25].

	Optimized Ge virtual substrate	Initial Ge virtual substrate	GaAs substrate (control)
Threshold current density	*269 A/cm2*	577 A/cm2	529 A/cm2
Differential quantum efficiency	*0.20*	0.13	0.19
Characteristic temperature	*129 K*	61 K	128 K
Device Lifetime	*~4hrs*	~15min	1000s of hrs

Table 2.1 – Device performance data for lasers fabricated on Ge virtual substrate and GaAs substrate. Table adapted from Groenert [25].

In addition to some limitations due to TDD, the utility of Ge virtual substrates for III-V device integration on Si is also limited by the thickness of the $Si_{1-x}Ge_x$ graded buffer. Growth of thick III-V layers on Ge virtual substrates can lead to cracking of the III-V layers. In a study of this phenomenon, Yang [29] concluded that this effect was caused by residual strain in the $Si_{1-x}Ge_x$ graded buffer, which in turn is due to mismatch in the thermal expansion coefficient between Si and Ge. The large thickness of the $Si_{1-x}Ge_x$ graded buffer (~10μm) exacerbates this problem, and Yang showed that the thickness of III-V material that can be grown on Ge virtual substrates without cracking is limited to about 3μm.

The large thickness also poses a challenge for monolithic integration of Si devices and III-V devices together on a single chip. As shown in Figure 2.11, the graded buffer thickness creates a large vertical separation between the III-V device layer and the Si device layer. This would complicate the processing and interconnection of both materials together in an electronic-photonic integrated circuit. This is an issue that must be addressed for practical use of Ge virtual substrates for monolithic III-V/CMOS integration.

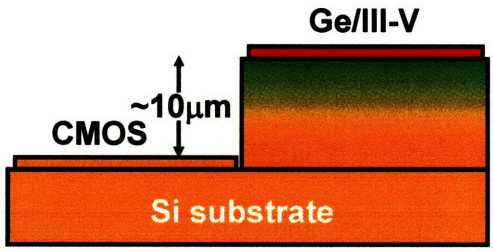


Figure 2.11 – Schematic of monolithic integration of CMOS and III-V devices on a Si substrate, showing the large vertical distance between the Si and III-V device layers. Image adapted from Pitera [8].

As a final concern, the surface roughness of the Ge cap of the Ge virtual substrate affects the performance of lasers and waveguides, which are sensitive to interfacial light

scattering [26]. While this surface roughness has been manageable for previous demonstrations of III-V devices, this roughness cannot be effectively removed by chemo-mechanical planarization (as will be explained in Chapter 4), and it would be desirable to reduce the roughness in the as-grown Ge virtual substrate. Also, because the surface roughness of the $Si_{1-x}Ge_x$ graded buffer also negatively affects the mobility of threading dislocations as the layer grows, an improvement in surface roughness may also result in an improvement in TDD. Thus, TDD, graded layer thickness, and surface roughness are the three metrics (in order of importance) which are of primary concern for application of the Ge virtual substrate for monolithic integration.

2.3 Wafer-Bonding Methods

In addition to Ge virtual substrates, wafer bonding is also being considered for application to monolithic III-V/CMOS integration. Wafer bonding is a conceptually simple technique that takes advantage of the very high level of perfection of modern semiconductor wafers. It is based on the fact that two very flat, smooth surfaces will spontaneously adhere to each other when brought into contact, even without any adhesive. The driving force for wafer bonding is provided by van der Waals forces between the two surfaces, which generally are significant only at very short range; this is why demanding flatness and smoothness are essential for effective wafer bonding [30].

Semiconductor wafers are typically manufactured with very demanding specifications for wafer smoothness and flatness, as this is generally required for many aspects of semiconductor processing. This flatness and smoothness means that semiconductor wafers can be bonded together typically with minimal additional polishing or other processing. If the wafers have undergone any pre-bonding processing (etching,

oxidation, film deposition, etc.), the wafers will typically be planarized using chemo-mechanical planarization (CMP) to achieve the best possible smoothness.

Wafer bonding can be used to transfer semiconductor layers from one wafer to another, thus allowing two different semiconductors to be combined together on a single wafer. Because the bonding takes places at low temperatures (often at room temperature), lattice-mismatched semiconductors can be bonded together – either directly or with a dielectric layer such as SiO_2 in between – with only a network of misfit dislocations at the interface; because the process occurs at low temperature, there is no formation of threading dislocations or other crystalline defects in the transferred layer.

A typical wafer bonding process proceeds as follows: first, if there was any pre-bonding processing that may have roughened the surface, the wafers are planarized using CMP. Then, the wafers are treated with a pre-bond cleaning step, typically using a wet chemical treatment or possibly plasma or other surface activating treatments. In addition to removing particulates that could adversely affect the bond strength, this step alters the surface chemistry of the wafers so as to maximize their adhesion. Next, the wafers are bonded by bringing them into physical contact, usually under a vacuum and combined with pressure. After bonding, the bonded pair is typically annealed to strengthen the bond.

For layer transfer processes, the wafer that is donating a layer (the "donor wafer") to the other wafer must be removed from the wafer that is receiving the layer (the "handle wafer"). There are typically two methods for removing the donor wafer while leaving the transferred film on the handle wafer. The first method is referred to as "bond and etch-back." As the name implies, the donor wafer is removed by etching, typically using wet

etchants. In order to ensure that the etch only removed the donor wafer and not the transferred layer, the donor wafer is typically processed with an "etch-stop" layer that is not attacked by the etchant used for etch-back. Thus, by epitaxially growing an etch-stop layer followed by the transfer layer, one can ensure that the donor wafer is etched away while the transfer layer is left behind. If required, the etch-stop layer can usually also be removed using a different etchant that preferentially attacks the etch-stop layer but not the transfer layer.

While this method can be effective for layer transfer, it is not very efficient or elegant in that the donor wafer is completely destroyed in the process. Also, precise control of thickness uniformity can be a problem, especially if there is not a suitable combination of etchants and etch-stop layers that can be used in the process. As an alternative, a novel approach to layer transfer, first reported by Bruel [31], has been developed. This approach, which was first applied to fabrication of Si-on-insulator (SOI) wafer, is outlined in Figure 2.12.

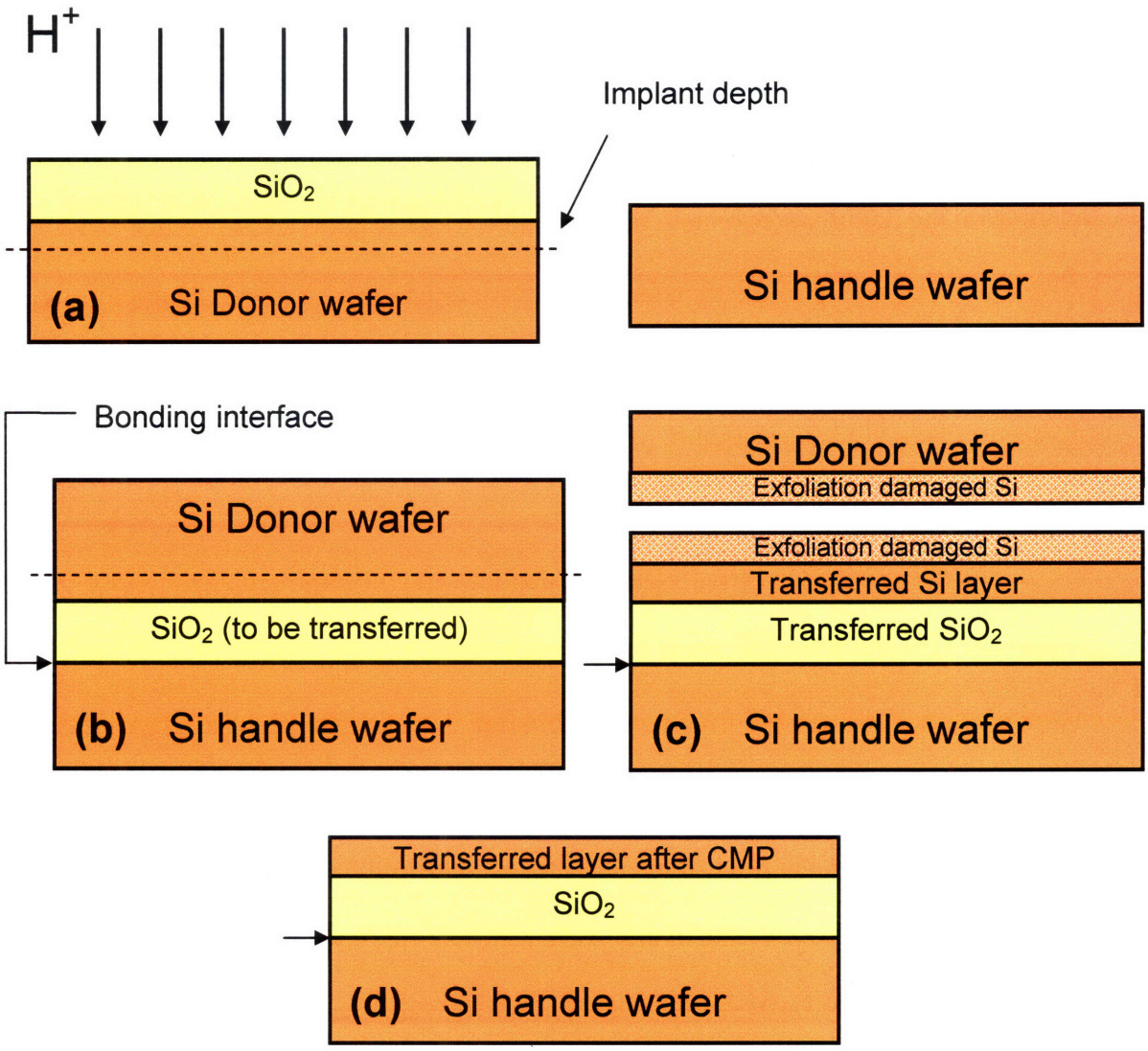


Figure 2.12 – Overview of "Smartcut" process for fabrication of Si-on-insulator (SOI) wafers. This procedure was first reported by Bruel [31]. **Note that the donor wafer in part (a) is then inverted when bonded to the handle wafer – the donor wafer orientation in parts (b,c) is inverted from orientation in part (a).**

The procedure described by Bruel is essentially as follows: an oxidized Si donor wafer is implanted with a hydrogen dose of $2x10^{16}$ - 10^{17} cm^{-2} (Figure 2.12a) to an average implant depth where one desires to separate the donor from the transfer layer. The donor wafer is then bonded to an unprocessed Si handle wafer (Figure 2.12b). The bonded pair is then subjected to an annealing sequence. During annealing, the implanted hydrogen leads to creation of a network of hydrogen platelets in the Si centered on the

average depth of the hydrogen implant. These platelets mechanically weaken the Si and cause it to fracture along a plane located at the implant depth, a process referred to as exfoliation. Thus, the donor wafer is removed from the bonded pair, while SiO_2 and Si layers from the donor wafer remain on the handle wafer (Figure 2.12c). After exfoliation, the surface of the transferred Si layer contains exfoliation damage from the region of platelet formation that remained behind. This damaged Si can be removed with chemo-mechanical planarization (CMP), leaving an undamaged Si-on-insulator (SOI) wafer (Figure 2.12d).

This technique has seen widespread application and commercialization for the production of SOI wafers. Because the technique does not destroy the Si donor wafer, it can be reclaimed using CMP to remove exfoliation damage and then reused as a donor wafer for another SOI wafer, although that practice has not yet been commercialized. There is also considerable interest in studying the application of this technique for transfer of other semiconductors to a Si wafer, such as Ge or GaAs for the creation of Ge-on-insulator (GeOI) or GaAs-on-insulator (GaAsOI) wafers.

However, while this technique has been very successful for the creation of SOI wafers, it is not as well-suited when used for bonding of wafers with dissimilar coefficients of thermal expansion (CTE). Thermal annealing of the bonded pairs, which is required to strengthen the relatively weak bond at room temperature, will cause bowing which can result in delamination at the bond interface. Using a bending mechanics approach, Pitera has calculated the bond strength required for a representative case of bonding of GaAs and Si wafers. For a wafer thickness of 525μm and annealing temperature of 700°C (typical values for a potential bonding process), Pitera reports a

bond strength of 320 J/m^2 is required to maintain adhesion, while the maximum possible bond energy for this system is 2.25 J/m^2 [8].

It may be possible to mitigate this problem through the use of thinner wafers to decrease the strain energy. However, another complication for widespread application of this technique is the size availability of semiconductor wafers. The Si CMOS industry has largely adopted the use of 300mm wafers for its production. The wafer size has been steadily increased over the years because larger wafer size allows more devices to be produced per wafer, lowering costs. However, wafers of other materials are generally not widely available in such sizes. For instance, 150mm GaAs substrates are the most common size used for device production, and while Ge wafers were recently announced to be available in 300mm size [32], the cost of these wafers is still expected to far exceed that of 300mm Si wafers. In order to be applied to a Si CMOS production environment, a layer transfer process would require 300mm wafers of the material to be transferred, which is not economically practical any semiconductors other than Si.

2.4 Summary

In this chapter, we have reviewed approaches for monolithic integration of III-V semiconductors with Si CMOS. Heteroepitaxial growth of III-V materials on Si is an appealing technique for this goal, but it is complicated by the lattice mismatch between Si and GaAs and InP, the technologically most important III-V semiconductors. For GaAs growth on Si, this issue can be dealt with effectively by use of $Si_{1-x}Ge_x$ compositionally graded buffers to fabricate device-quality GaAs on Si, which has been proven through fabrication of a number of GaAs-based devices. However, the TDD and the large thickness of the $Si_{1-x}Ge_x$ graded buffer are two factors that limit the utility of the $Si_{1-x}Ge_x$

graded buffer for III-V/CMOS monolithic integration. Alternatively, wafer bonding can be used for layer transfer, but this is limited by the CTE mismatch between Si and other semiconductors, as well as the availability of 300mm wafers for materials other than Si. A comparison of the two approaches is shown in Figure 2.13.

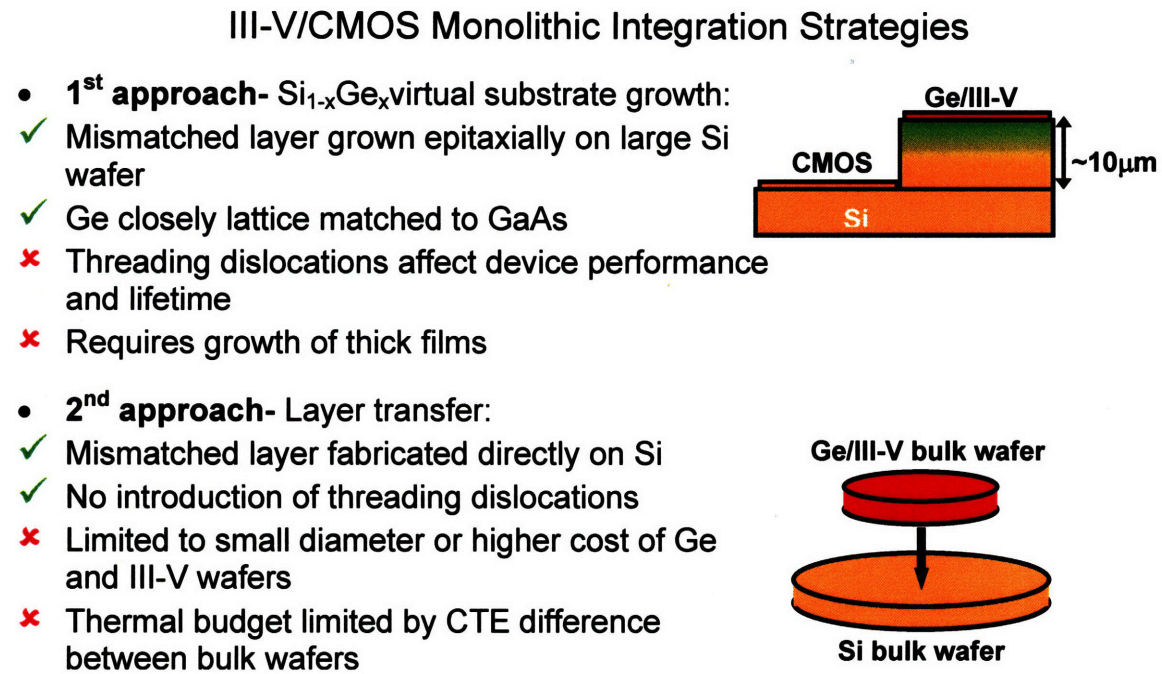


Figure 2.13 – Comparison of III-V/CMOS monolithic integration strategies. Adapted from Pitera [8].

Chapter 3: Experimental Methods

The work presented in this thesis is intended to overcome some of the limitations on III-V/CMOS integration discussed in the previous chapter. This work involves the use of several semiconductor growth and characterization techniques. This chapter gives an overview of the growth and characterization techniques employed in the work presented in this thesis.

3.1 Semiconductor Growth

3.1.1 Ultra-high vacuum chemical vapor deposition (UHVCVD)

UHVCVD was used for growth of all $Si_{1-x}Ge_x$ structures (including compositionally graded buffers) fabricated for this work. This reactor, which is depicted in Figure 3.1, is a custom-built vertical system designed to provide advanced $Si_{1-x}Ge_x$ growth capabilities. The growth chamber consists of a quartz tube pumped with a high-displacement turbo pump. An inlet for process gases is located at the top of the tube; the connection between the quartz and process gas piping is made with a brazed molybdenum quartz-to-metal seal to minimize the leak rate through this seal. The base of the tube is sealed to a metal flange using two concentric o-rings in which the interstitial space between the o-rings is evacuated by a separate pumping system. The size of the quartz tube and the wafer boats is sufficient to allow growth on up to ten 150mm wafers in a single batch. The quartz tube is surrounded by a furnace which is capable of operating at a temperature of up to 900°C. The system is equipped with a loadlock to maintain low base pressure in the growth chamber. The chamber has a base pressure of less than 10^{-9} torr at a standby temperature of 800°C.

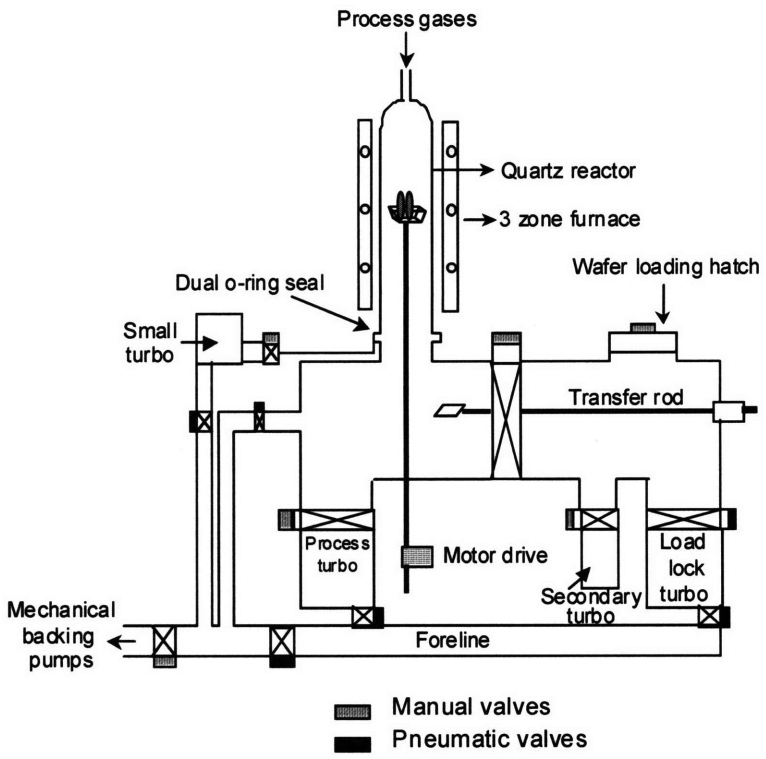


Figure 3.1 – Schematic of UHVCVD reactor used for $Si_{1-x}Ge_x$ epitaxial growth. Image adapted from Giovane [33].

The flow of process gases to the reactor is regulated by a computer-controlled gas manifold consisting of 79 valves and 40 mass flow controllers. The precursor gases which are plumbed into the manifold are SiH_4 (primary Si precursor), GeH_4 (Ge precursor), Si_2H_6 (low-temperature Si precursor), B_2H_6 (p-type dopant source), PH_3 (n-type dopant source), and Ar (dilutant). The growth pressure of the reactor during growth is typically controlled by partially closing a manual gate valve over the process turbo-pump, essentially using the gate valve as a throttle valve. Growth pressures typically range from 1-30 millitorr.

In a typical growth process, wafers are subject to a pre-epitaxial clean in a clean room environment to remove surface contamination and native oxide immediately prior to growth. For Si wafers and $Si_{1-x}Ge_x$ virtual substrates with $x_{Ge} = 0.5$ or less, the clean

consists of a 10min rinse in a piranha acid bath (3:1 H_2SO_4:H_2O_2) to remove organic contaminants, followed by a 1min rinse in a diluted HF bath (10:1 H_2O:HF) to etch the native oxide and leave a hydrogen-terminated surface on the wafer to protect the wafer from oxidation. After this step, the wafer is removed from the HF bath without rinsing and placed directly into the wafer box. The lack of a rinse procedure is made possible by the fact that the hydrogen-terminated surface of the Si wafer is extremely hydrophobic, thus making it possible to withdraw the Si wafer from the HF bath without any droplets of HF remaining on the surface – thus drying is also not required. Rinsing is avoided because it will replace the hydrogen passivation of the surface with a surface terminated by hydroxyl species, which leaves the surface susceptible to formation of a native oxide. Meyerson has shown that the HF treatment described above will protect the Si surface from native oxide formation for a period of minutes after the treatment [34]. Thus, the wafers are transferred as quickly as possible (within approximately 15min) to the UHVCVD loadlock to begin pumping down. After insertion into the loadlock, the loadlock is pumped down to a pressure of less than 10^{-6} torr before transferring the wafers to the main chamber. The wafers are then heated to 200-250°C for 30min to desorb water vapor and other contaminant species from the surface before heating to 900°C for 10min for a final desorb of any remaining surface species on the wafers before initiating epitaxial growth.

3.1.2 Organo-metallic Chemical Vapor Deposition Reactor

Organo-metallic chemical vapor deposition (OMCVD) was used for epitaxial growth of $GaAs_yP_{1-y}$ layers on $Si_{1-x}Ge_x$ virtual substrates as described in Chapter 6 of this thesis. The OMCVD reactor used in this work is a Thomas Swan close-coupled

showerhead OMCVD reactor. A schematic of this reactor is shown in Figure 3.2. In the close-coupled showerhead design, process gases are flowed onto a rotating susceptor at normal incidence with a small distance between the showerhead and susceptor (on the order of 1cm). Precursor gases for Group III species and Group V species are not mixed until they reach the showerhead to minimize any possible reactions between the gases before they reach the wafer surface. The susceptor has six pockets for 50mm wafers as shown in the figure. The growth pressure is controlled by a mechanical roughing pump with a throttle valve, which can maintain a constant pressure throughout semiconductor growth. The growths in this work were performed at 100 torr. The susceptor is heated radiatively by a lamp and is capable of temperatures of over 850°C. The precursor gases for the work in this thesis were trimethylgallium (TMG) for gallium, arsine (AsH_3) for arsenic, and phosphine (PH_3) for phosphorus. The reactor main chamber is enclosed in an N_2-purged glove box to prevent the reactor from being exposed to ambient air when loading and unloading wafers from the system, thus reducing exposure to contaminants which can be problematic for III-V semiconductor epitaxial growth. A loadlock is used to transfer wafers into and out of the reactor glove box.

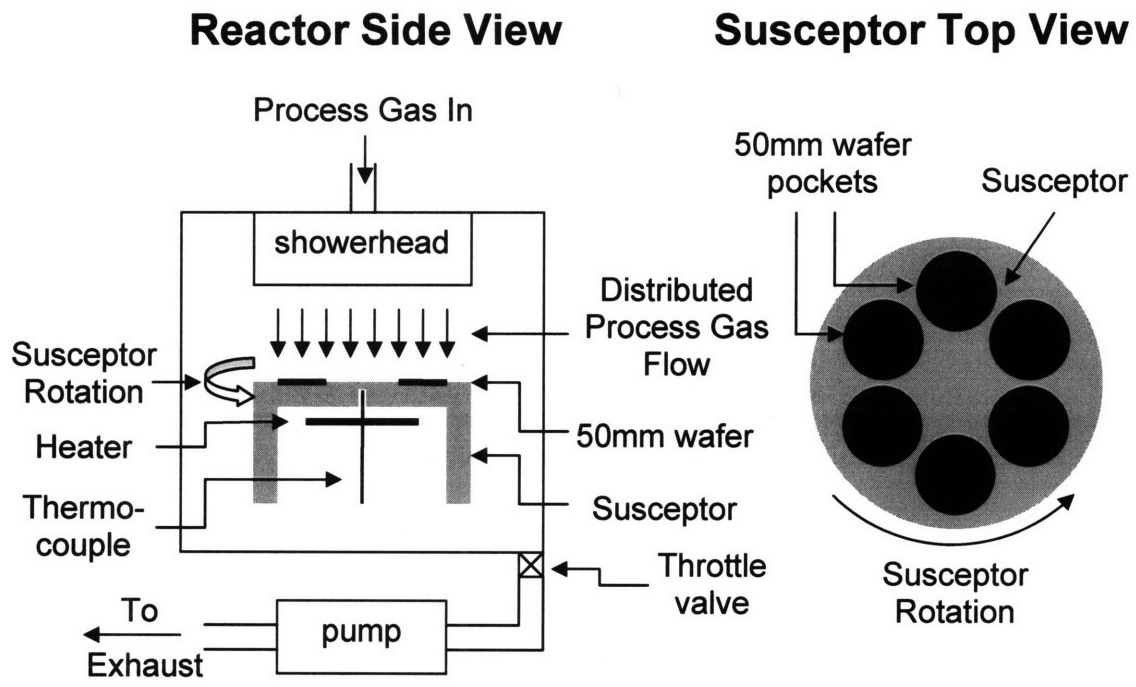


Figure 3.2 – Schematic of Thomas Swan close-coupled showerhead OMCVD reactor used in this work.

3.2 Material Characterization

Several material characterization techniques were heavily utilized in the work described in this thesis. This section gives a description of these techniques and how they were implemented in this work.

3.2.1 Differential Interference Contrast (Nomarski) Microscopy

Optical microscopy can provide valuable information about surface morphology in semiconductor processing. However, epitaxially grown semiconductor structures or other very flat surfaces generally result in very low contrast of surface features as observed in standard reflective optical microscopy. However, this contrast can be greatly enhanced through the use of differential interference contrast microscopy (also known as

Nomarski microscopy). In this technique, the polarized optical light source is divided into two beams which are incident on the sample and then recombined in the microscope. Small variations of sample height produce a different optical path length for the two beams, which results in interference when the beams are recombined. This enables the microscope to detect variations in surface height down to the nanometer size scale. A representative Nomarski image of a Ge virtual substrate is shown in Figure 3.3, showing the presence of "crosshatch" surface roughness.

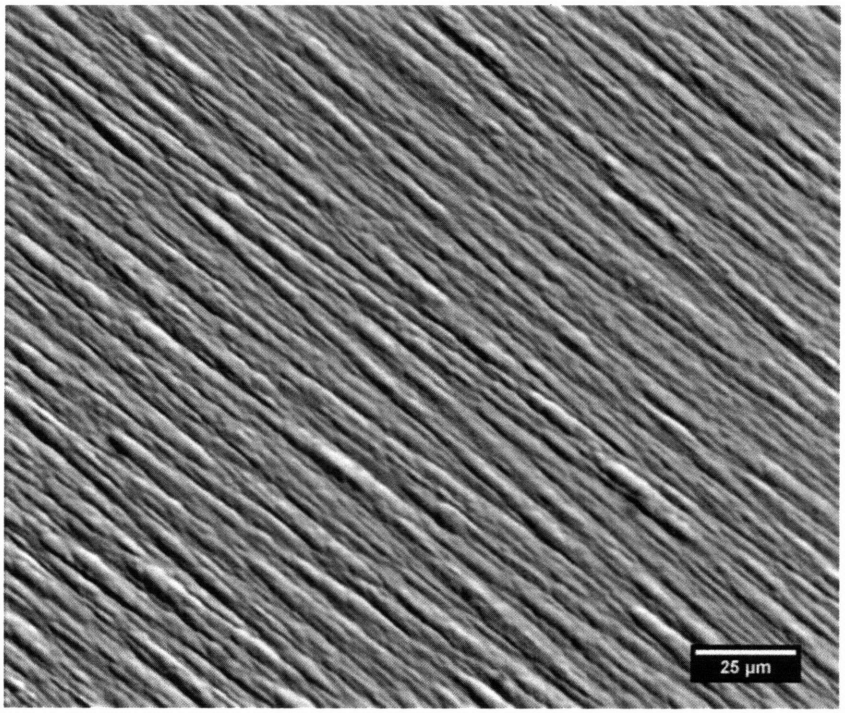


Figure 3.3 – Representative Nomarski image of a Ge virtual substrate, showing the appearance of surface roughness ("crosshatch"). The surface shown in this image corresponds to an RMS surface roughness of 10-15nm over a 25x25µm area, as measured by AFM.

3.2.2 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a technique of measuring nanometer-scale height variations over a microscopic region of a sample surface. The data produced are analogous to a topographic map and can be processed into color-coded two-dimensional images or three-dimensional views of the surface. The AFM obtains these measurements

by rastering a vibrating Si cantilever over the surface of interest. The Si cantilever vibrations are very sensitive to the proximity of the Si surface. The height of the cantilever is adjusted to provide a constant feedback from the surface as it is rastered, thus allowing the surface height to be determined as a function of the position on the surface. This technique can be used for areas ranging from 1x1μm to 50x50μm areas and can provide a height resolution on the order of 1nm. The AFM used in this work is a Digital Instruments Dimension 3000 Nanoscope IIIa operating in tapping mode. A representative image is shown in Figure 3.4.

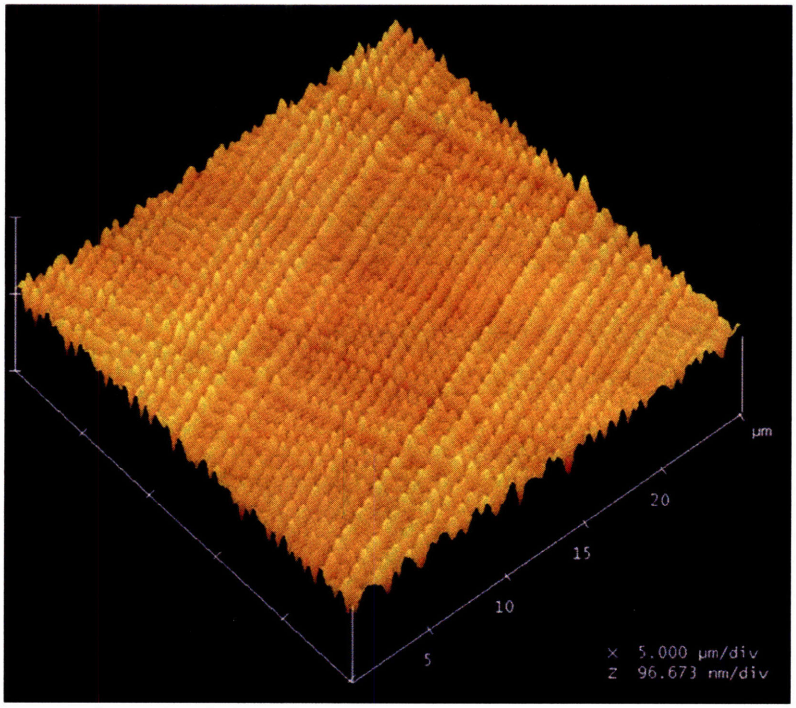


Figure 3.4 – Representative AFM image of $Si_{1-x}Ge_x$ heterostructure surface, rendered as a three-dimensional view.

3.2.3 X-Ray Diffraction (XRD)

XRD is an invaluable tool in materials science. In the study of epitaxial layers, XRD can be used to measure both the in-plane and out-of-plane lattice parameter of a semiconductor layer, thus allowing the determination of strain state. In the case of

semiconductor alloys such as $Si_{1-x}Ge_x$, the in-plane and out-of-plane lattice parameters can be used to determine the composition x_{Ge} according to Vegard's Law, which essentially states that the lattice parameter of the alloy is a linear interpolation of the lattice parameter of the pure substances. Vegard's Law is also employed for determination of $GaAs_yP_{1-y}$ alloy compositions in this work by interpolation between GaP and GaAs.

All XRD measurements used in this work utilize measurement of the 004 and 224 diffraction peaks of each epitaxial layer of interest and comparing their locations to the 004 and 224 peaks of the substrate to determine in-plane and out-of-plane lattice parameter. This technique was first described by Matney and Goorsky [35].

For each measurement, both 004 and 224 diffraction peaks from each layer of interest as well as the substrate were measured. The approximate angle of incidence and exit of the x-ray beam for these diffraction peaks relative to an exactly oriented (001) semiconductor wafer is shown in Figure 3.5. The 004 peak is termed symmetric because the angle of incidence equals the angle of exit for this peak, while the 224 peak is asymmetric.

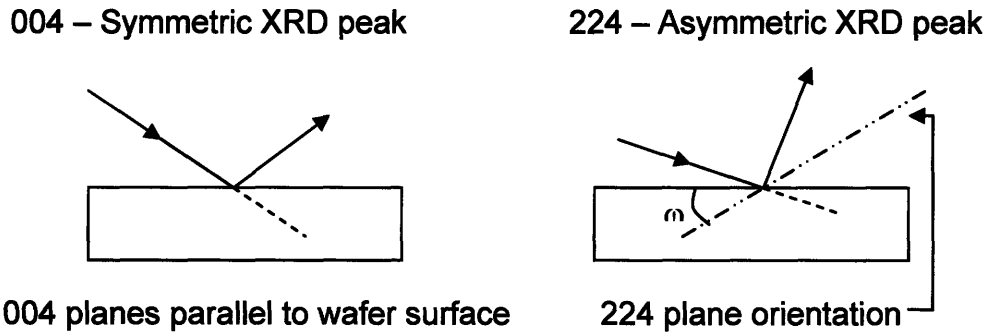


Figure 3.5 – Illustration of approximate angle of incidence and exit of the x-ray beam relative to the wafer surface for both 004 and 224 reflections. The 224 illustration shows the glancing-incidence geometry, which was used in this work.

A schematic of the experimental setup used for measurements in this study is shown in Figure 3.6. For each sample, the values of 2θ and ω (the angle between the sample stage and the diffracting plane) for the 004 and 224 diffraction peaks of the substrate and each layer of interest were measured. The difference in peak positions between the layer diffraction peaks and the substrate diffraction peaks is then calculated and used to calculate the composition and strain state.

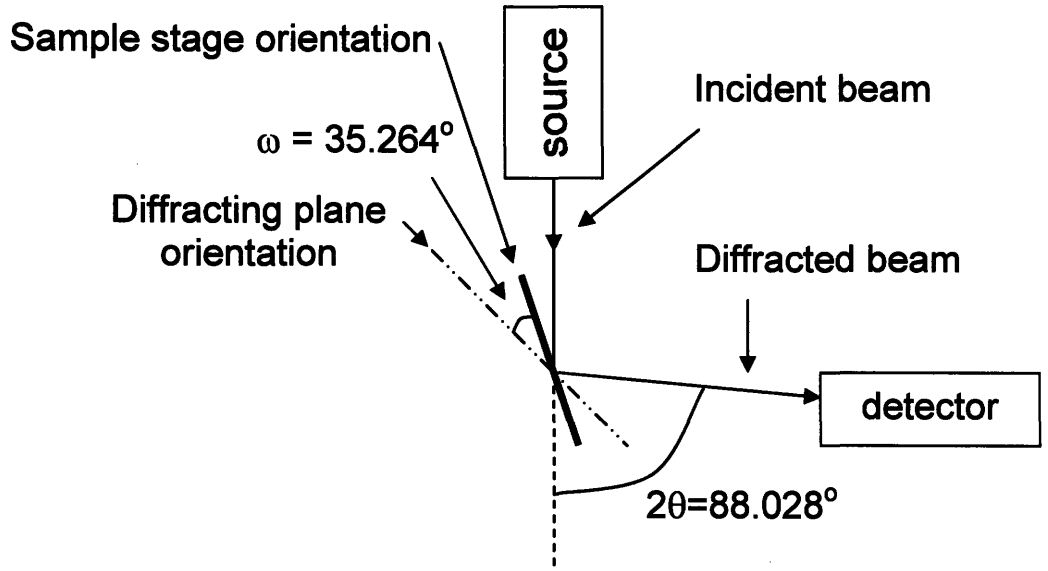


Figure 3.6 – Schematic of experimental setup for XRD measurement of the 2θ and ω values of a diffraction peak. The values of 2θ and ω in this diagram correspond to the positions for the 224 diffraction peak of a Si substrate.

As described by Leitz [36], the in-plane (k_{ip}) and out-of-plane (k_{oop}) reciprocal lattice wavevectors from a glancing-incidence 224 measurement can be calculated as follows:

$$k_{ip} = \frac{2}{\lambda}\sin(\theta_{224} + \Delta\theta_{224})\sin(\phi - \Delta\omega_{224} + \Delta\omega_{004}) \quad [3.1]$$

$$k_{oop} = \frac{2}{\lambda}\sin(\theta_{224} + \Delta\theta_{224})\cos(\phi - \Delta\omega_{224} + \Delta\omega_{004}) \quad [3.2]$$

where θ_{224} is the substrate Bragg angle, $\Delta\theta_{224}$ is the angular separation between the film and substrate 224 peaks, ϕ is the angle between (004) and (224) planes (35.264°), and

$\Delta\omega_{224}$ and $\Delta\omega_{004}$ are the separation in ω between the film peak and substrate peak for the 224 and 004 peaks, respectively.

The wavevectors above can then be used to determine the in-plane and out-of-plane lattice parameters as follows:

$$a_{ip} = 2\sqrt{2}/k_{ip} \quad [3.3]$$

$$a_{oop} = 4/k_{oop} \quad [3.4]$$

$$a_r = \frac{a_{oop} + \nu \cdot a_{ip}}{1+\nu} \quad [3.5]$$

where a_{ip}, a_{oop}, and a_r are the in-plane, out-of-plane, and relaxed lattice parameters of the layer, respectively; and ν is the Poisson ratio. Composition and strain can then be determined from these values.

The XRD tool used in this work is a Philips PANalytical Xpert Pro XRD system using Cu Kα radiation. Unfortunately, this tool is not ideal for epitaxial film analysis because this system does not filter out Kα2 radiation from the x-ray beam. The result of this is that two peaks appear for each epitaxial layer under study, one from Kα1 and one from Kα2 radiation. This can require careful interpretation to determine which layer and wavelength each peak corresponds to. Thus, it can be helpful to measure an intensity contour plot of 2θ versus ω (also referred to as a reciprocal space map) to show all the peaks for each layer and wavelength centered on either the 004 or 224 reflection. An example is shown in Figure 3.7. For most samples reported in this study, values of 2θ and ω were determined using one-dimensional θ-2θ and ω scans (these correspond to horizontal and vertical line scans in the reciprocal space map shown). More details on the XRD procedure used in this work are given by Bowen and Tanner [37].

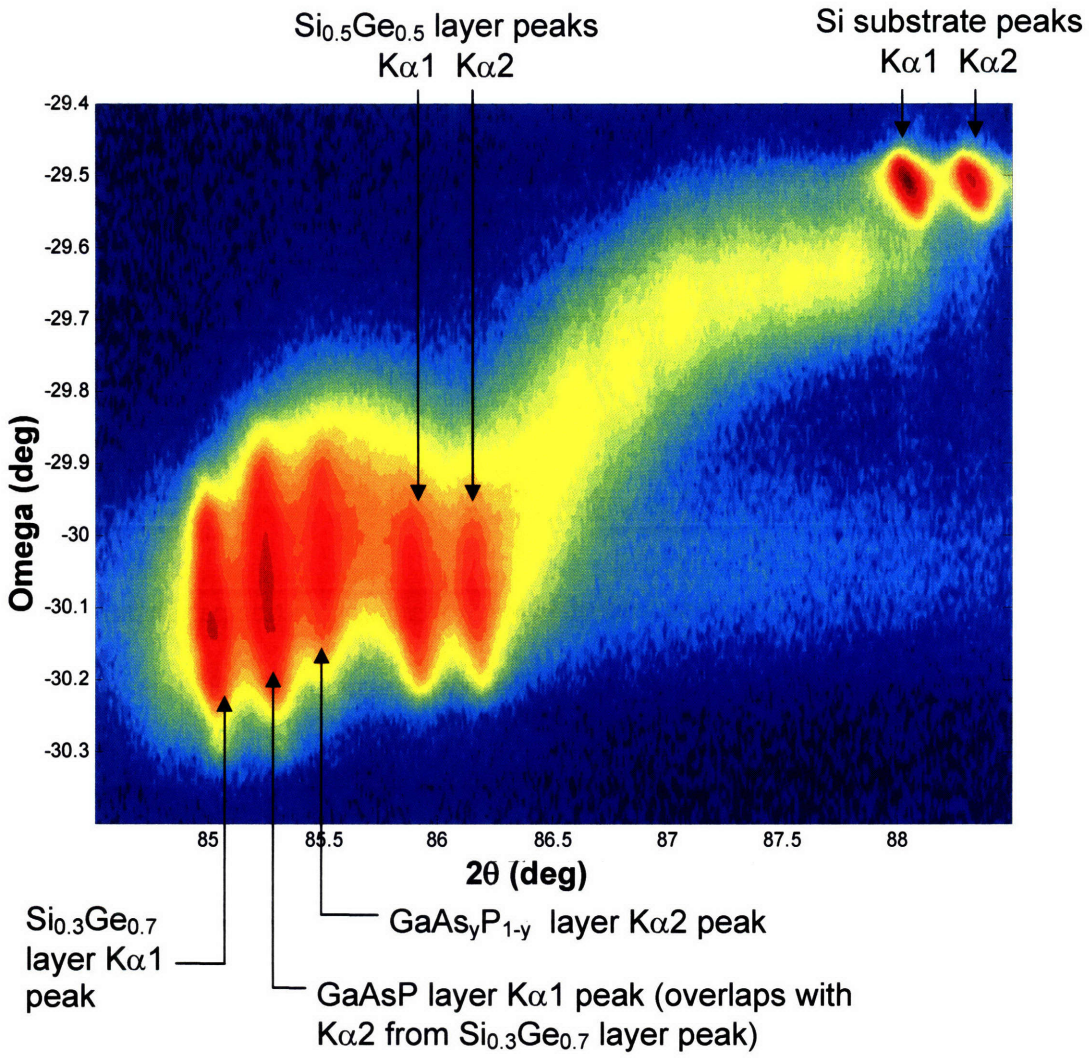


Figure 3.7 – Reciprocal space map of the 224 diffraction plane of a $GaAs_yP_{1-y}$ layer grown on a $Si_{1-x}Ge_x$ virtual substrate deposited on a Si wafer. For this sample, careful interpretation was required to correctly match each peak with a layer and wavelength.

3.2.4 Transmission Electron Microscopy

Transmission electron microscopy was extensively utilized in this work. A transmission electron microscope (TEM) consists of a high-energy (~200keV) electron source and a series electromagnetic lenses for focusing the electrons into a beam incident on the sample and for image formation. The arrangement of components in a TEM is actually quite analogous to the arrangement of components in a transmission optical microscope, with an electron source and electromagnetic lenses substituted for a light

source and optical lenses. Thus, the operation of the TEM can be understood at a rudimentary level using the same sorts of optical ray diagrams that are commonly employed for basic descriptions of light microscopy. One key breakdown in the TEM/optical microscope analogy is that, unlike optical lenses, the characteristics of electromagnetic lenses (magnification, aberrations, etc.) can be adjusted during microscope operation by varying current flows to the lens components, whereas the characteristics of optical lenses is determined during the lens manufacturing process and cannot be adjusted during operation. Thus, correction of lens imperfections (astigmatism in particular) can be achieved by adjusting current flows in the instrument to obtain a higher-resolution image.

Just as transmission optical microscopy requires optically transparent samples, TEM requires an electron-transparent specimen in order for it to be imaged. However, while many materials are optically transparent at macroscopic thicknesses, the semiconductors studied in this work are only electron-transparent at very thin thicknesses, generally less than one micron. Thus, unless the specimen of interest is already electron-transparent (certain nanostructures), TEM requires that the samples be thinned to electron transparency before imaging. This thinning requirement can be very difficult to fulfill for some materials, and the quality of TEM sample preparation often limits the amount of information which can be obtained from the specimen. Thus, successful TEM sample preparation requires a preparation technique that is well-suited to the material under study.

TEM samples used in this study were prepared using a combination of mechanical grinding and ion milling. In this work, two different specimen orientations were

employed: cross-section and plan-view. Cross-sectional TEM (xTEM) specimens were prepared using the standard "sandwich" method. Two pieces of the sample were sectioned and glued face-to-face using epoxy. They were mechanically polished down to a thickness of approximately 10μm, finishing with a 0.3μm SiO_2 slurry grit on both sides. The sample was then ion milled using a Gatan Precision Ion Polishing System (PIPS) from both sides of the specimen at an angle of 5° with beam energy of 5kV until the specimen was perforated in the center. The specimen area in the vicinity of the perforation was then thin enough for electron-transparency. Preparation of plan-view (pvTEM) samples was similar, except that specimens were thinned from the back side only (in both mechanical grinding and ion milling), and a Fischione ion milling system operating at 4kV was primarily used for these samples.

One of the uses of TEM in this work was to observe crystallographic defects. Defect imaging in this work was achieved through the use of two-beam diffraction conditions, which is discussed in detail by [38]. In this work, 220 two-beam diffraction conditions were employed for imaging of crystallographic defects, including dislocations, stacking faults, and anti-phase boundaries. For cross-sectional TEM, samples for defect imaging were tilted to create a 220 two-beam condition in the vicinity of the <011> pole. This is found to provide good defect contrast for dislocations and stacking faults [38] as well as anti-phase boundaries [39]. Figure 3.8a shows defects identified by Ting as APBs in a GaAs layer grown on Ge. Figure 3.8b shows an image take by the author of defects in the GaAs buffer layer in a III-V device structure grown on Ge virtual substrate. These were identified as APBs by the author based on their similar appearance to APBs in GaAs on Ge reported by Ting. Similarly, dislocations and stacking faults were identified

based on their resemblance to images of dislocations and stacking faults reported in the literature, taken under similar diffraction conditions.

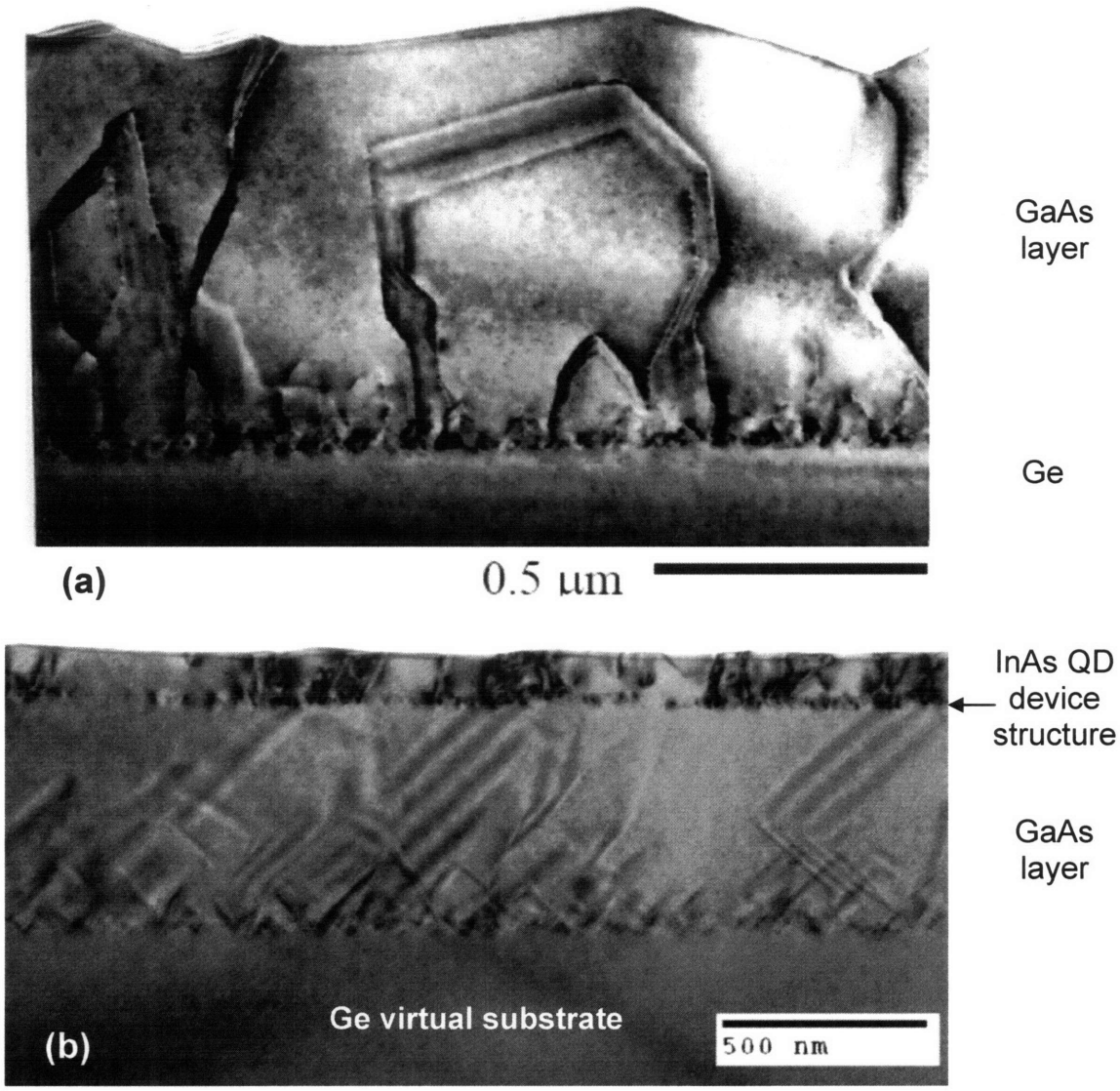


Figure 3.8 – Images of anti-phase boundaries (APBs) in GaAs grown on Ge samples taken using cross-sectional TEM with a 220 two-beam condition near the <011> pole. (a) Image of defects in GaAs on Ge film identified by Ting as anti-phase boundaries (APBs) . The image was taken using a 220 two-beam condition close to the <011> pole. Image adapted from Ting [40]**. (b) InAs quantum dot (QD) device structure grown on Ge virtual substrate, imaged by author. The defects visible in the GaAs buffer layer were identified as anti-phase boundaries based on similarity in appearance to APBs identified by Ting. Additional defects are present in the InAs QD device region. Image taken using 220 two-beam condition near <011> pole, in similar manner to Ting.**

Other diffraction conditions employed in this work were 004 two-beam conditions (for strain layer contrast enhancement) and directly along the <011> pole (for high-resolution TEM) [38].

In addition to observing material defects, TEM can also sometimes be used to determine defect density. However, this can be limited by the small sample area of TEM. For instance, in cross-sectional TEM, a threading dislocation density of at least 10^8 cm^{-2} is typically required in order to reliably observe threading dislocations [41]. Thus, the lack of threading dislocations in a cross-sectional TEM sample only indicates that the TDD is less than ~10^8 cm^{-2} and cannot provide more information than that. Plan-view TEM can be used to measure lower TDD values because it probes a larger area of the sample. In the TEM used in this thesis, an image taken at 5000x (one of the lowest magnification settings for this instrument) covers a sample area of 2.2 x10^{-7} cm^2. Thus, a TDD of 4.5 x10^6 cm^{-2} corresponds to an average of one thread per image at this magnification. It is not clear the number of threads that must be counted in order to obtain a reliable average TDD, but it seems clear that TDD values below this level will become increasingly error-prone.

3.2.5 Etch-Pit Density (EPD)

The TDD values of $Si_{1-x}Ge_x$ virtual substrates are typically near or below the minimum TDD measurement limit for plan-view TEM; thus, another technique for TDD measurement is desired to complement pvTEM (or substitute for it for $Si_{1-x}Ge_x$ compositionally graded buffers with TDD < 10^6 cm^{-2}). This can be done by using a defect etch to create etch pits on the surface at the site of each threading dislocation, which can then be observed using Nomarski microscopy.

Schimmel has developed a reliable etch-pit density (EPD) etchant for Si consisting of a mixture of CrO_3, HF, and H_2O [42]. The work of Lai further established that a modified version of this etch (8g CrO_3, 200mL HF, 250mL H_2O) can create etch pits on $Si_{1-x}Ge_x$ virtual substrates with x_{Ge} up to 70% [43]. This etchant, which is referred to as the Schimmel etch in this thesis, was used to determine TDD of all $Si_{1-x}Ge_x$ virtual substrates with x_{Ge} = 70% or less in this work. The etching time and depth required to form etch pits was dependent on Ge content, and it was found that an etch time of 3min was adequate to form etch pits for x_{Ge} = 50-63%, while an etch time of 4min was required to form etch pits for x_{Ge} = 70%. The issue of etch depth for this etch is discussed in more detail in Chapter 5.

The effect of this etching treatment on a $Si_{0.5}Ge_{0.5}$ virtual substrate is shown in Figure 3.9. For this demonstration, the surface roughness was removed prior to etching so that the effect of the EPD etch would not be mistaken for existing crosshatch. Figure 3.9a shows the sample after 10min, producing a nearly feature-less surface as seen under Nomarski. Figure 3.9b shows the effect of adding the EPD etch to this procedure. Etch pits are clearly seen, and EPD etch also produces a roughness pattern similar to the crosshatch pattern of $Si_{1-x}Ge_x$ virtual substrates. This indicates that the EPD etch probably has some selectivity to strain fields of underlying misfit dislocations, the cause of surface crosshatch [19].

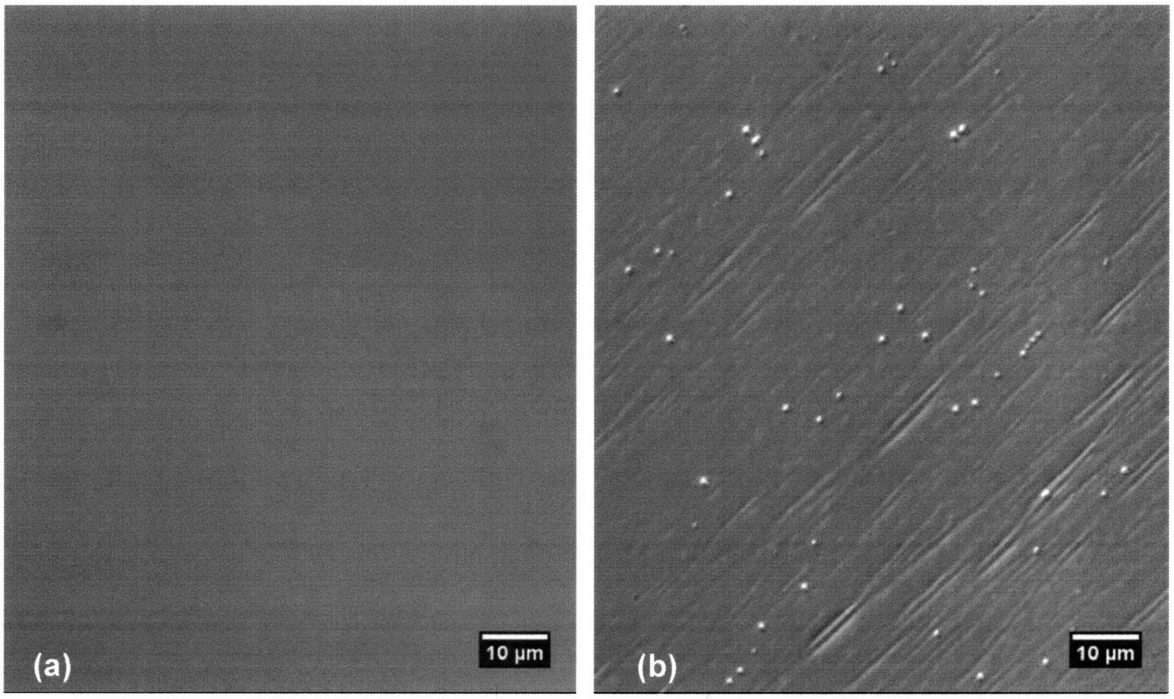


Figure 3.9 – Nomarski images of CMPed $Si_{0.5}Ge_{0.5}$ virtual substrate before and after EPD treatment. (a) $Si_{0.5}Ge_{0.5}$ virtual substrate after 10min CMP. The sample appears essentially feature-less when viewed with Nomarski with a 50x objective. (b) $Si_{0.5}Ge_{0.5}$ virtual substrate after 10min CMP and 3min EPD etch. The etching treatment produces etch pits as well as additional roughening of the surface.

For EPD measurements of Ge, Baribeau reported that an etchant consisting of 300mg of iodine dissolved in a 5:10:11 solution of hydrofluoric acid (HF), nitric acid (HNO_3), and acetic acid (CH_3COOH) was effective at producing producing etch pits in Ge [44]. It should be noted that the etch rate of this etchant is ~300nm/sec. Because a typical Ge virtual substrate is grown with a Ge cap thickness of ~1μm, this means that an etch time of >3.3 sec will result in the Ge cap being fully etched away from the Ge virtual substrate. The presence of misfit dislocations below the Ge cap would be expected to greatly complicate the pit counting process, and Ge virtual substrates are generally etched

with a "quick dip" of 1-2 sec in the EPD etchant before rinsing with water to halt the etching process before the Ge cap is fully removed. This has proven effective for TDD determination of Ge virtual substrates, and Luan later correlated the data from this EPD procedure for Ge with pvTEM results and showed that they were in agreement to within a factor of two [12].

Given this discrepancy between EPD and pvTEM reported by Luan, it should be mentioned that there are several potential sources of error in EPD measurements. Etch pits typically have a size of 1-2μm, and if dislocations are spaced more closely than this, the etch pits will merge, as shown in Figure 3.10. This will tend to cause undercounting of etch pits. In addition, many EPD samples have ambiguous features which could either be etch pits or other surface roughness generated by crosshatch. This is also shown in Figure 3.10. Samples with etch pits which are not well-defined would be expected to suffer from undercounting, while samples with a high surface roughness (due to crosshatch for instance) would be expected to suffer from overcounting. In making EPD measurements of different samples, it is important to try to maintain a consistent standard of what constitutes a pit in order to make EPD comparisons between different samples meaningful. In addition, because there is some subjectivity involved in deciding what constitutes a pit, comparing EPD measurements made by different individuals would be expected to have more error than comparisons of EPD measurements made by the same individual.

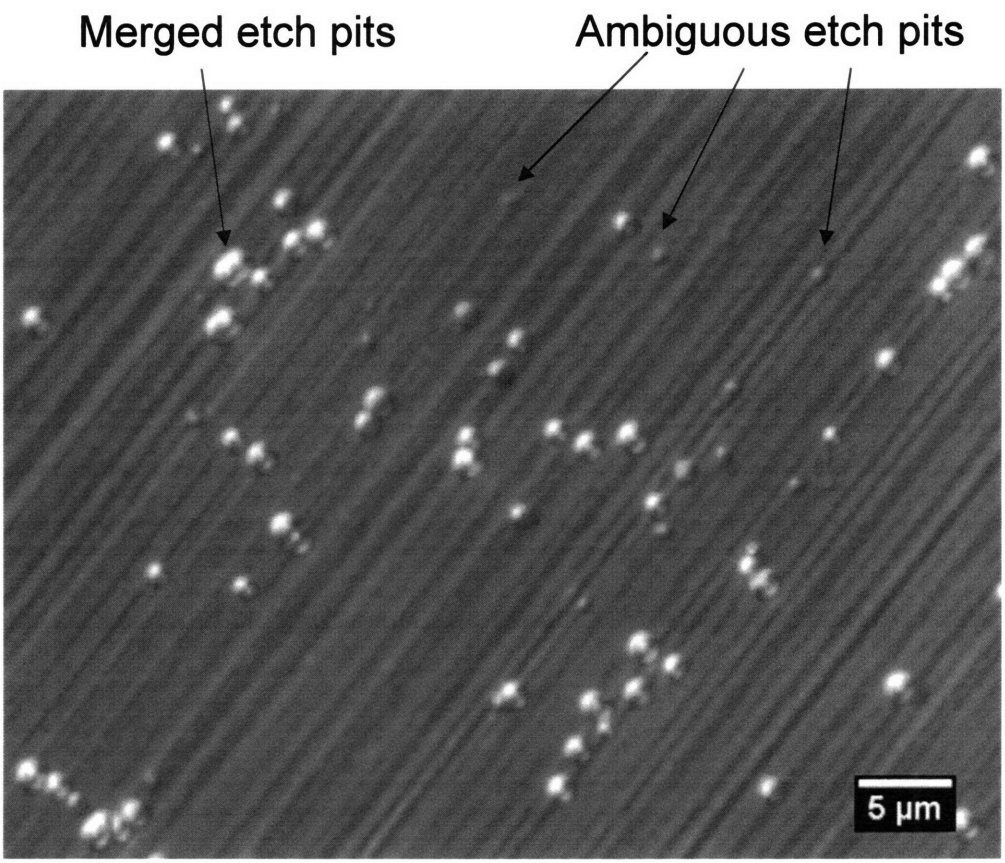


Figure 3.10 - Nomarski image of EPD-etched $Si_{0.3}Ge_{0.7}$ surface illustrating both merged etch pits and ambiguous etch pits as shown in figure.

When comparing EPD and pvTEM TDD results, it should be noted that EPD techniques generally probe a much larger sample area than pvTEM. The standard area of Nomarski images taken for EPD in this study was 3.6×10^{-4} cm^2, over 1000 times larger than the standard image size for pvTEM. Thus, a typical EPD measurement will provide an average over a much larger area than pvTEM, making it much less susceptible to local fluctuations in TDD on the surface. EPD measurements in this study were taken using at least three images. Error bars and margins of error reported in this thesis correspond to the 95% confidence interval, which is determined as follows:

$$error = \frac{ts}{\sqrt{n}} \qquad [3.6]$$

where s is the standard deviation, n is the number of measurements (typically three), and t is Student's t, which was found in a statistical table and depends on the size of the confidence interval and degrees of freedom (for a 95% confidence interval with two degrees of freedom, t = 4.303) [45]. Based on the sample area imaged and typical TDD values of samples in this work, the typical number of pits counted for each reported measurement is on the order of 600.

3.2.6 Cathodoluminescence

Room temperature cathodoluminescence was used to investigate the optoelectronic properties of $GaAs_yP_{1-y}$ films grown on $Si_{1-x}Ge_x$ virtual substrates as discussed in Chapter 6. In this technique, the sample area of interest is imaged in a scanning electron microscope (SEM). The electron beam from the SEM creates electron-hole pairs in the sample, which then recombine, and a fraction of these recombinations emit light. The emitted light is collected and analyzed using a diffraction grating and photo-multiplier tube to determine the intensity versus wavelength. For thick films (i.e. not quantum wells or other nanostructures), the peak wavelength of emission generally corresponds to the band gap wavelength of the material, which then provides information on the composition of semiconductor alloys. In addition, the peak width and intensity can provide some qualitative information on material quality, mainly when compared to cathodoluminescence data from samples with known material quality.

3.2.7 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) was used in this study to measure chemical concentration as a function of depth in epitaxial films. SIMS can provide

invaluable information on the presence of a wide variety of impurities as well as alloy composition as a function of depth. In SIMS, a sputtering technique is used to etch into the film. The material removed by sputtering is then analyzed using mass spectroscopy to determine concentrations of the chemical species of interest. This is achieved by ionizing the material from the sample and then accelerating it through a magnetic field. The trajectory of the ions through the magnetic field is determined by their mass, allowing them to be separated so that their concentration can be measured independently [46]. By continually measuring chemical concentration as the etch proceeds deeper into the structure, a plot of concentration versus depth in the structure can be determined.

SIMS analysis in this work was completed using the services of Evans Analytical Group, Sunnyvale, CA.

3.3 Conclusion

This chapter reviewed the semiconductor epitaxial growth and characterization techniques employed in this work. This chapter, along with Chapters 1 and 2, provide the background required for understanding the studies of methods for III-V/CMOS monolithic integration presented in Chapters 4, 5, and 6.

Chapter 4: Silicon on Lattice-Engineered Silicon (SOLES)

4.1 Introduction

As discussed in Chapter 2, Ge virtual substrates and layer transfer by wafer bonding both have drawbacks that make them less than ideal for monolithic integration of III-V semiconductors on the Si CMOS platform. For Ge virtual substrates, one of these drawbacks is the large thickness (~10μm) of the $Si_{1-x}Ge_x$ graded buffer, which complicates interconnection between the Si device layer and III-V device layer. For layer transfer methods, the problem of CTE mismatch between Si and III-V wafers as well as the availability of 300mm III-V and Ge substrates must be overcome in order to apply this technique on a large scale for monolithic integration.

In this chapter, we discuss ways in which both of these techniques can be combined to take advantage of the strengths of both methods while avoiding each technique's drawbacks. We then present demonstration of a new commercially-viable platform for III-V/CMOS integration, which we refer to as Silicon on Lattice-Engineered Silicon (SOLES).

4.2 Layer transfer with $Si_{1-x}Ge_x$ virtual substrates

The combination of layer transfer with $Si_{1-x}Ge_x$ virtual substrates has attracted considerable interest for its potential to create a variety of different on-insulator platforms for high-performance CMOS devices. In addition to III-V/CMOS integration, $Si_{1-x}Ge_x$ graded buffers have also seen wide application to the creation of low-TDD strain-engineered $Si_{1-x}Ge_x$ heterostructures in order to create high-mobility channels for high-performance MOSFETs [47]. Numerous high-mobility MOSFETs have been fabricated using this technique, but the thickness of the compositionally graded buffer is a concern for commercial application of this process for many of the same reasons that it creates

challenges for III-V/CMOS integration. In addition, separation of the device layer from the bulk substrate using SOI and other on-insulator platforms eases the isolation of devices from each other and improves MOSFET performance due to a reduction of the body effect, thus increasing MOSFET speed [48].

Thus, a number of different on-insulator platforms using $Si_{1-x}Ge_x$ compositionally graded buffers have been developed. Unlike bonding of CTE-mismatched wafers, bonding of $Si_{1-x}Ge_x$ virtual substrates to other Si wafers is unaffected by CTE-related issues because the $Si_{1-x}Ge_x$ virtual substrate is deposited on a Si wafer; thus, the bulk wafers in this case are both Si, meaning they are perfectly CTE-matched. Cheng demonstrated the fabrication of a $Si_{1-x}Ge_x$-on-insulator (SGOI) substrate by transferring a relaxed $Si_{1-x}Ge_x$ layer (x_{Ge} = 20-25%) to an oxidized Si handle wafer using both hydrogen-induced exfoliation [49] and bond and etch-back [50] methods. Additionally, Taraschi has fabricated strained-Si-on-insulator (SSOI) wafers by transferring a strained Si layer grown on a $Si_{1-x}Ge_x$ virtual substrate to an oxidized Si handle wafer using bond and etch-back [51]. Åberg has used a similar process to fabricate multi-layer strained $Si_{1-x}Ge_x$ heterostructures for high-mobility MOSFET channels on insulator [52]. Isaacson has also used virtual substrate layer transfer to create transferred structures without an intermediate oxide layer, including a strained Si layer on a relaxed Si substrate and a strained Si layer on a relaxed $Si_{1-x}Ge_x$ layer on a Si substrate [53].

These results demonstrate the feasibility of layer transfer processes using $Si_{1-x}Ge_x$ compositionally graded buffers with both bond and etch-back and hydrogen-induced exfoliation layer transfer methods. However, these results have all been achieved using $Si_{1-x}Ge_x$ virtual substrates with $Si_{1-x}Ge_x$ alloys close to that of Si ($x_{Ge} < 0.3$). For

applications involving GaAs integration with Si CMOS, $Si_{1-x}Ge_x$ virtual substrates with x_{Ge} = 100% are required. The work of Pitera [54] showed that this introduces several additional challenges for successful layer transfer. $Si_{1-x}Ge_x$ virtual substrates with x_{Ge} < 0.5 can be chemo-mechanically planarized (CMPed) using standard Si CMP technology to produce a very smooth surface with less than 0.5nm RMS roughness over a 25x25μm area while removing less than 0.5μm of layer thickness. This greatly facilitates virtual substrate wafer bonding since very smooth surface are required for high bond strength. However, $Si_{1-x}Ge_x$ virtual substrates capped with x_{Ge} > 0.5 cannot be planarized to nearly the same surface roughness. In particular, Pitera showed that CMP of a Ge virtual substrate using a standard Si CMP process (KOH-based slurry for 30min) results in the formation of "etch pits" at the site of threading dislocations in the Ge layer. This is shown in Figure 4.1. These etch pits prevent the surface roughness from being reduced to the requisite 0.5nm that Pitera determined was required for bonding.

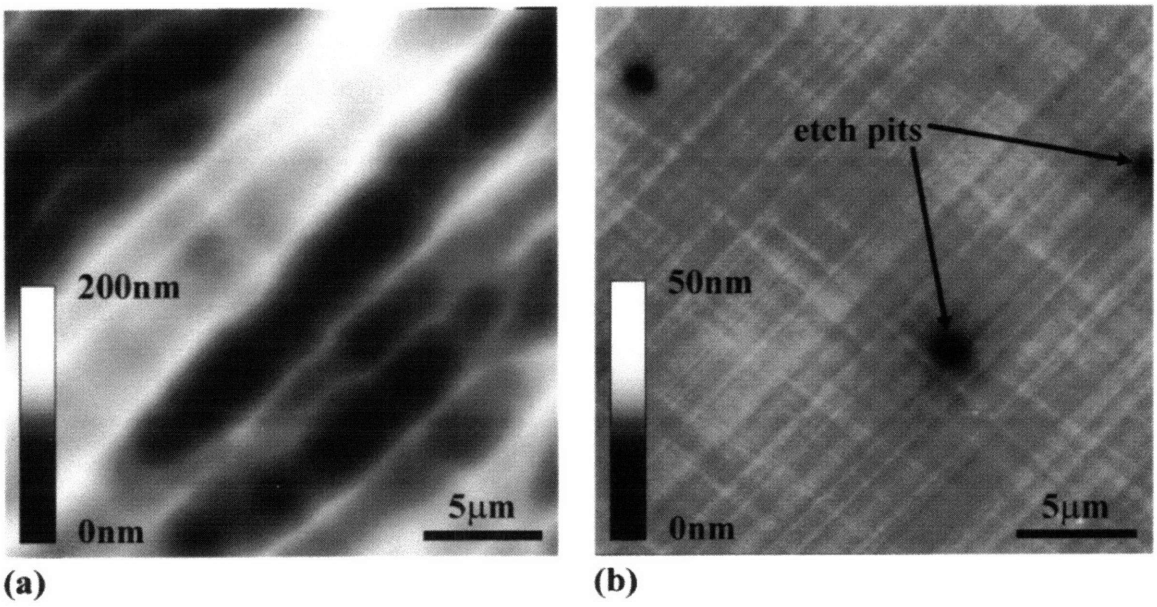


Figure 4.1 – AFM images of a Ge virtual substrate (a) before and (b) after CMP using a standard Si CMP process. CMP reduces RMS surface roughness of a 25x25μm area from 12nm to <5nm but at the expense of creating etch pits on the surface, thus preventing further surface roughness improvement. Image adapted from Pitera [54].

Planarization processes for bulk Ge wafers typically remove a large thickness from the wafer, which is not feasible for Ge virtual substrates, in which the thickness of the Ge cap is limited to about 2μm due to the same CTE mismatch concerns mentioned in Chapter 2 in regards to cracking of III-V layers on Ge virtual substrates. However, Pitera showed that this issue can be overcome through the deposition of an SiO_2 layer on the Ge virtual substrate, which can then be planarized by CMP to a roughness of <0.5nm for a 1x1μm area. By utilizing an SiO_2 "CMP layer" on the Ge virtual substrate and hydrogen-induced layer exfoliation, Pitera was able to transfer a Ge layer from a Ge virtual substrate to a Si handle wafer to fabricate a Ge-on-insulator (GeOI) substrate.

4.3 Description of SOLES

The GeOI process described above is a practical technique for transfer of a Ge layer from a Ge virtual substrate to a Si handle wafer which can easily be scaled up to 300mm wafers. However, it is worth considering whether there may be a better platform than GeOI for III-V monolithic integration with Si CMOS. The goal of monolithic integration techniques is to provide a process that is as compatible as possible with existing Si CMOS processing technology. A GeOI wafer has a surface that is substantially different from a Si wafer. The presence of the Ge layer limits the thermal budget of GeOI wafers - the melting point of Ge is 940°C. In addition, Groenert experienced autodoping of GaAs layers grown on Ge virtual substrates via a gas phase transport mechanism at temperatures as low as 700°C [25], and similar effects could be experienced in CMOS processing at that temperature. Typical CMOS processing regularly employs temperatures of well over 1000°C for post-implantation anneals and regularly exceeds 700°C for oxidation and other processing [7]; thus, CMOS processing on GeOI substrates

would require substantial temperature modification from the standard CMOS process. In addition, the Si device layer can only be accessed after removing the Ge and SiO_2 layers from specific regions of the GeOI. Adjustments to the Si CMOS process would be required in order to accommodate etching down to the Si and processing only the exposed regions of the Si device layer, and it would be preferred if these adjustments could be avoided.

Many of the issues discussed above can be avoided or mitigated by placing the Si device layer on the surface of the substrate platform. If the Si device layer is at the surface and the III-V/Ge device layer is buried, then the wafer appears very much like an SOI wafer and can be processed in much the same way. Burial of the Ge layer would prevent any possible gas-phase transport autodoping (of the type observed by Groenert for GaAs on Ge growth), thus increasing the thermal budget of this platform relative to GeOI. An implementation of this using a Ge virtual substrate is shown Figure 4.2. This substrate platform is referred to as Silicon on Lattice-Engineered Silicon (SOLES) [55].

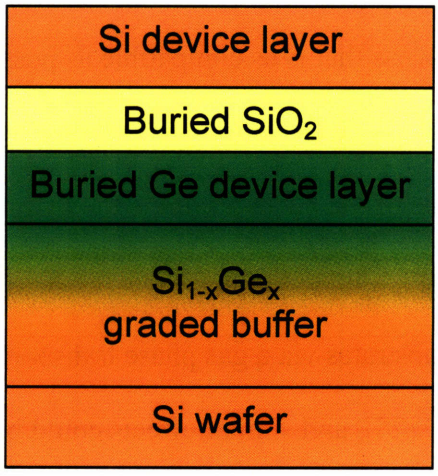


Figure 4.2 – Schematic of Silicon on Lattice-Engineered Silicon (SOLES) platform

Placement of the Si device layer at the surface gives SOLES numerous advantages over GeOI for monolithic integration. It is essentially an SOI wafer with the added functionality of a buried epitaxial template for Ge or III-V devices. Because the Si device layer can be made very thin (hundreds of nanometers or thinner), SOLES provides the same convenience of coplanar integration that is achieved with GeOI, thus alleviating the need to interconnect devices across the 10μm thickness of the $Si_{1-x}Ge_x$ graded buffer. The envisioned process flow for utilizing SOLES in a monolithic integration process is shown in Figure 4.3. Step 1 in the figure shows fabrication and isolation of Si MOSFETs just as it would proceed for typical SOI processing. During this processing, the Ge is buried and has minimal effect on the CMOS process. After CMOS front-end processing is complete, mesas can be opened in the SiO_2 layer to expose the Ge surface for processing. III-V device layers can then be grown using selective area epitaxy on the Ge surface (step 2 in figure). The selective growth of GaAs on Ge by MOCVD has been demonstrated by Brammertz [56] and can be applied to this process. The III-V layers can then be processed into devices (step 3) and interconnected (step 4) using standard, well-established processes for both steps.

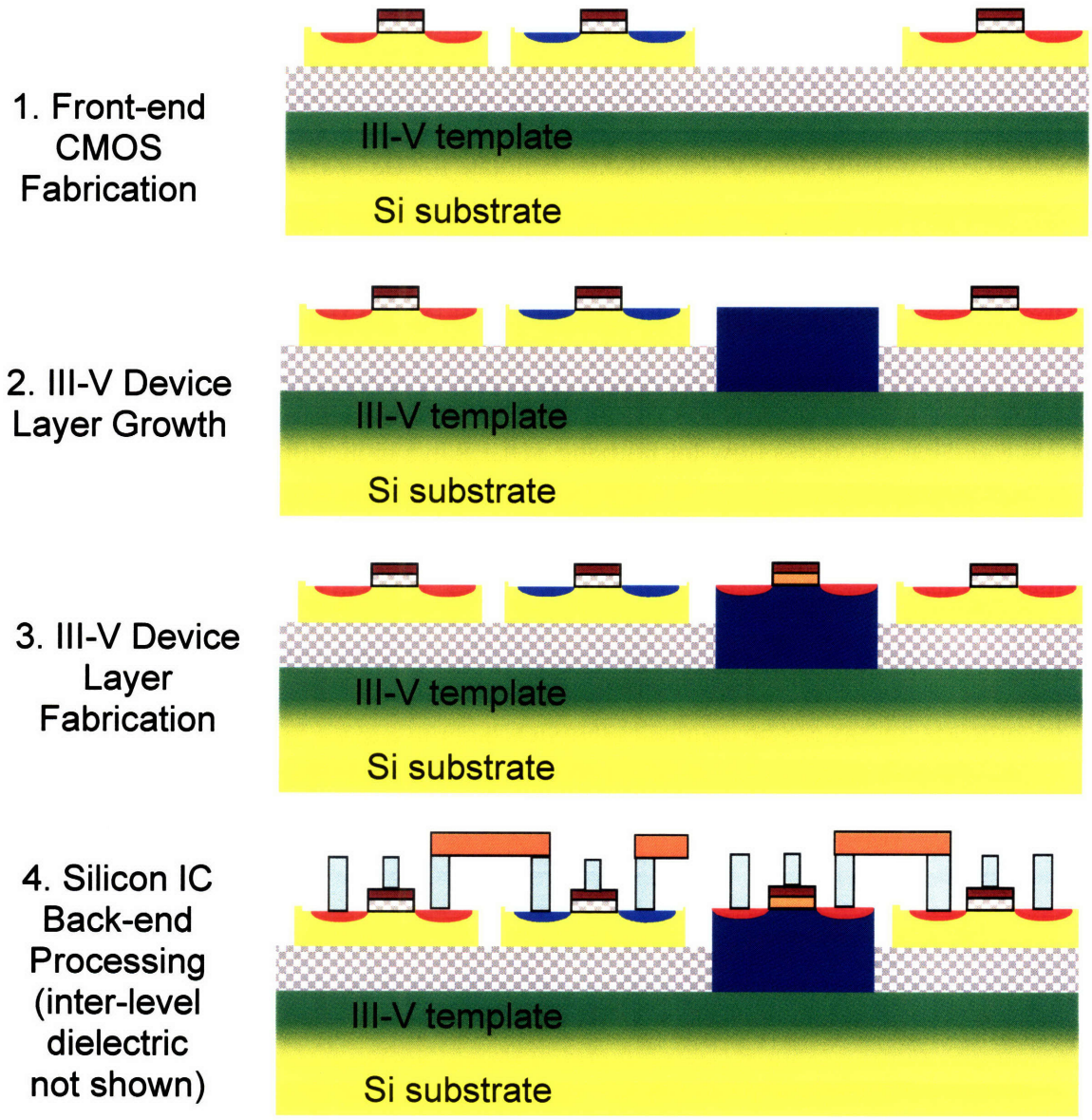


Figure 4.3 – Illustration of monolithic III-V/CMOS integration process utilizing SOLES wafer.

4.4 Fabrication of SOLES

In this study, a process was developed for fabrication of the SOLES platform. The design of the fabrication process was based on the results and techniques of previous virtual substrate bonding studies. Ge virtual substrates were prepared using the "conventional" $Si_{1-x}Ge_x$ graded buffer process described in Chapter 2. The wafer size

used throughout this work is 150mm. The work of Pitera [54] showed that use of an LPCVD-deposited SiO_2 CMP layer on a Ge virtual substrate provided a much smoother surface for bonding than direct CMP of the Ge surface; thus, the same technique was adopted for the SOLES process. As shown in Figure 4.4a, a 1μm SiO_2 CMP layer was deposited on the Ge virtual substrate. The CMP layer was then thinned to ~250nm by planarizing the wafer using CMP (Figure 4.4b). This is expected to reduce the surface roughness to <0.5nm over a 1x1μm area as reported by Pitera. This process prepared the Ge virtual substrate (which is the handle wafer in this process) for bonding.

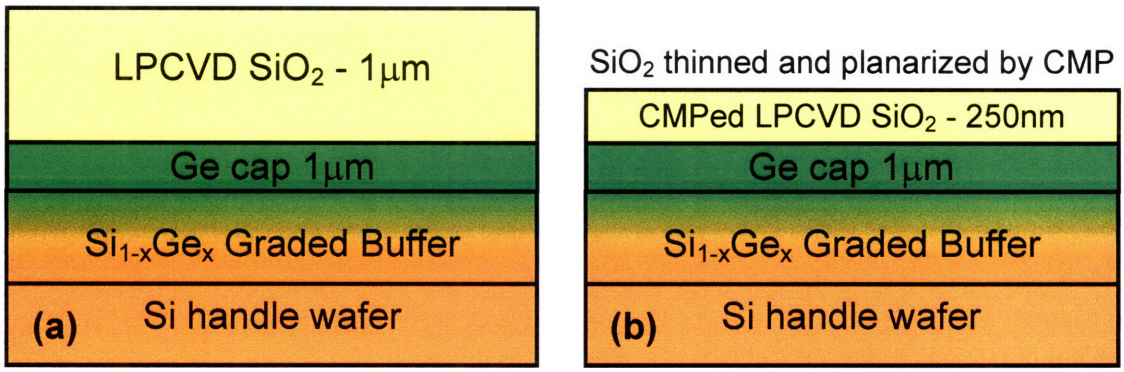


Figure 4.4 – Preparation of SOLES handle wafer for bonding (a) deposition of SiO_2 CMP layer on Ge virtual substrate, (b) thinning and planarizing of CMP layer to reduce roughness for bonding.

To prepare the donor wafer, first a 200Å thermal SiO_2 layer was grown on the Si donor wafers (Figure 4.5a). The purpose of this SiO_2 layer is to ensure that the bonding interface is fully encapsulated by SiO_2 on both sides. It is also possible to bond the handle wafer directly to a Si wafer with no oxide; in fact, the procedure of hydrophilic Si/SiO_2 bonding is generally found to provide a slightly higher bonding energy at room temperatures (~60mJ/m^2) than hydrophilic SiO_2/SiO_2 bonding (~50mJ/m^2) [30]. However, for monolithic integration, it is undesirable to have the bonding interface in contact with the Si device layer because contaminants at the bonding interface could

affect device performance if they are in direct contact with the Si device layer. A better alternative is to use SiO_2/SiO_2 bonding to move the bonding interface slightly away from the Si device layer. Thus, a 200Å thermal oxide was grown on the Si donor wafer for this purpose. The thickness of 200Å was chosen because it was desired to keep the buried SiO_2 layer as thin as possible to reduce the distance between the Si device layer and Ge/III-V device layer.

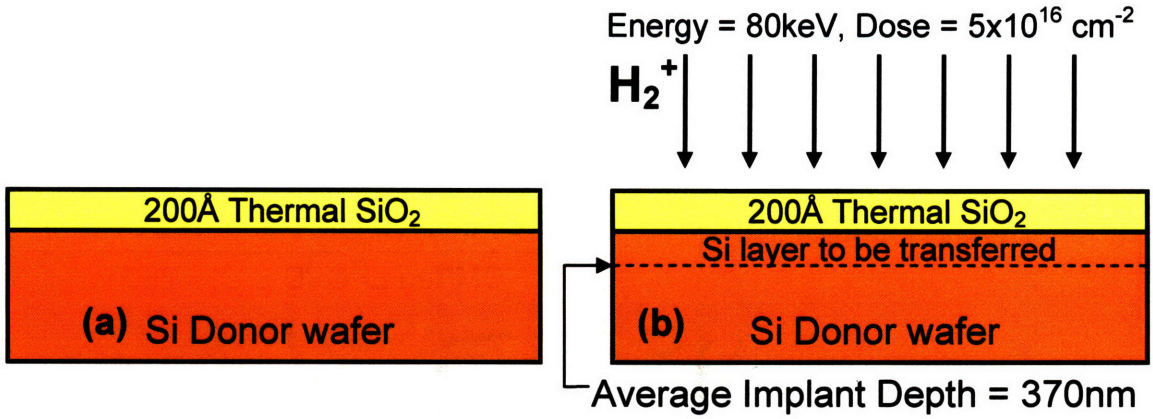


Figure 4.5 – Preparation of the Si donor wafer for bonding. (a) Growth of 200Å thermal oxide, (b) Implant of H_2^+ ions with energy of 80keV and dose of $5x10^{16}$ cm^{-2}

The SOLES substrate can be fabricated using either a bond and etch-back procedure or hydrogen-induced exfoliation for removal of the donor wafer from the bonded pair. For this study, hydrogen-induced exfoliation was chosen because of its better layer thickness uniformity as well as its simpler process requirements (bond and etch-back would require an etch-stop layer, which would require an epitaxial growth; hydrogen-induced exfoliation does not require this). Thus, the donor wafer must be implanted with hydrogen before bonding. The primary process variables which must be chosen for the hydrogen implant are the implant energy and dose. The implant energy determines the average depth of implant. The physics of ion implantation in solids is well understood and can be simulated with reasonable accuracy using the Stopping and

Range of Ions in Matter (SRIM) computer program by Ziegler [57]. The thickness of transferred Si desired for this process was 250-500nm, and SRIM was used to determine an appropriate implant energy that would provide an average implant depth in this range. Figure 4.6 shows the results of simulation of implant of H_2^+ at 80keV into the thermally-oxidized donor wafers used in this study. This provided an average ion range within the desired Si transfer thickness, so these conditions were chosen. The dose of $5x10^{16}$ cm^{-2} corresponds to the dose used by Bruel for SOI fabrication by the hydrogen-induced exfoliation process [31].

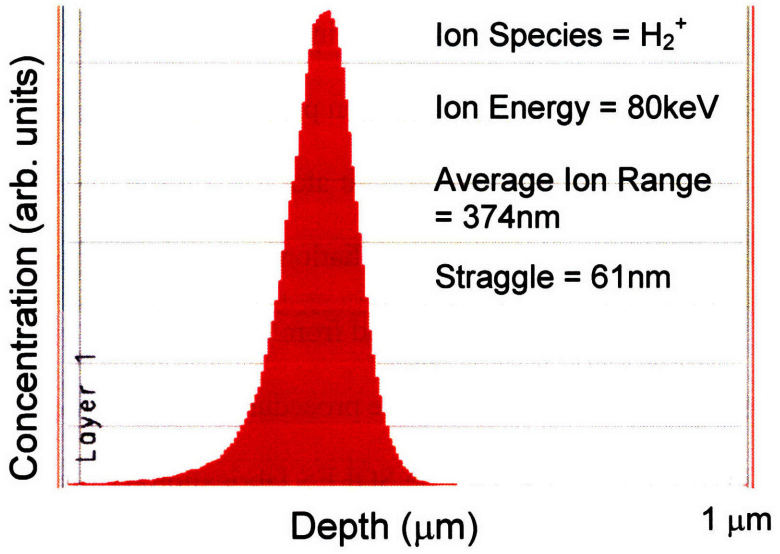


Figure 4.6 – Plot of hydrogen concentration versus depth for results of SRIM simulation of H_2^+ implant into Si donor wafer with 200Å thermal oxide.

After implantation of the donor wafer, the wafer pair is ready to be bonded. Use of proper surface cleaning and activation immediately before bonding is a crucial step to ensure high bonding strength. In the case of SiO_2/SiO_2 bonding, these steps can be accomplished simultaneously using the standard RCA-1 clean for Si wafers (1:1:5 $NH_4OH:H_2O_2:H_2O$). The RCA-1 solution is very effective at removing particulates from Si and SiO_2 surfaces, most likely through reducing the strength of capillary forces and

surface charges on the particles and the wafer [30]. Additionally, the RCA-1 clean activates Si and SiO_2 surfaces by creating a high density of Si-OH (silanol) groups on the surface [30]. These OH groups enable hydrogen bonding between the surfaces of the bonded wafers, which greatly increases the bond strength.

After a pre-bonding clean with RCA-1 solution, the wafers are bonded together under vacuum (Figure 4.7a). The bonded pair is then subjected to a two-step annealing sequence. The bonded pair is first annealed at 250°C for 1-2hr to strengthen the bond; this process is expected to increase the SiO_2/SiO_2 bond strength from 52 to over 1000 mJ/m^2 [30] with minimal effect on the hydrogen implant. The bonded pair is then annealed to 450°C for 0.5-1hr to induce hydrogen platelet nucleation at the implant depth, exfoliating the donor wafer from the bonded pair along this plane (Figure 4.7b) and leaving the transferred Si layer along with exfoliation damage. After exfoliation of the donor wafer, the exfoliation damage is removed from the transferred layer using a "touch" CMP step (Figure 4.7c), following the procedure of Bruel for exfoliation damage removal from SOI [31]. This completes the SOLES fabrication process.

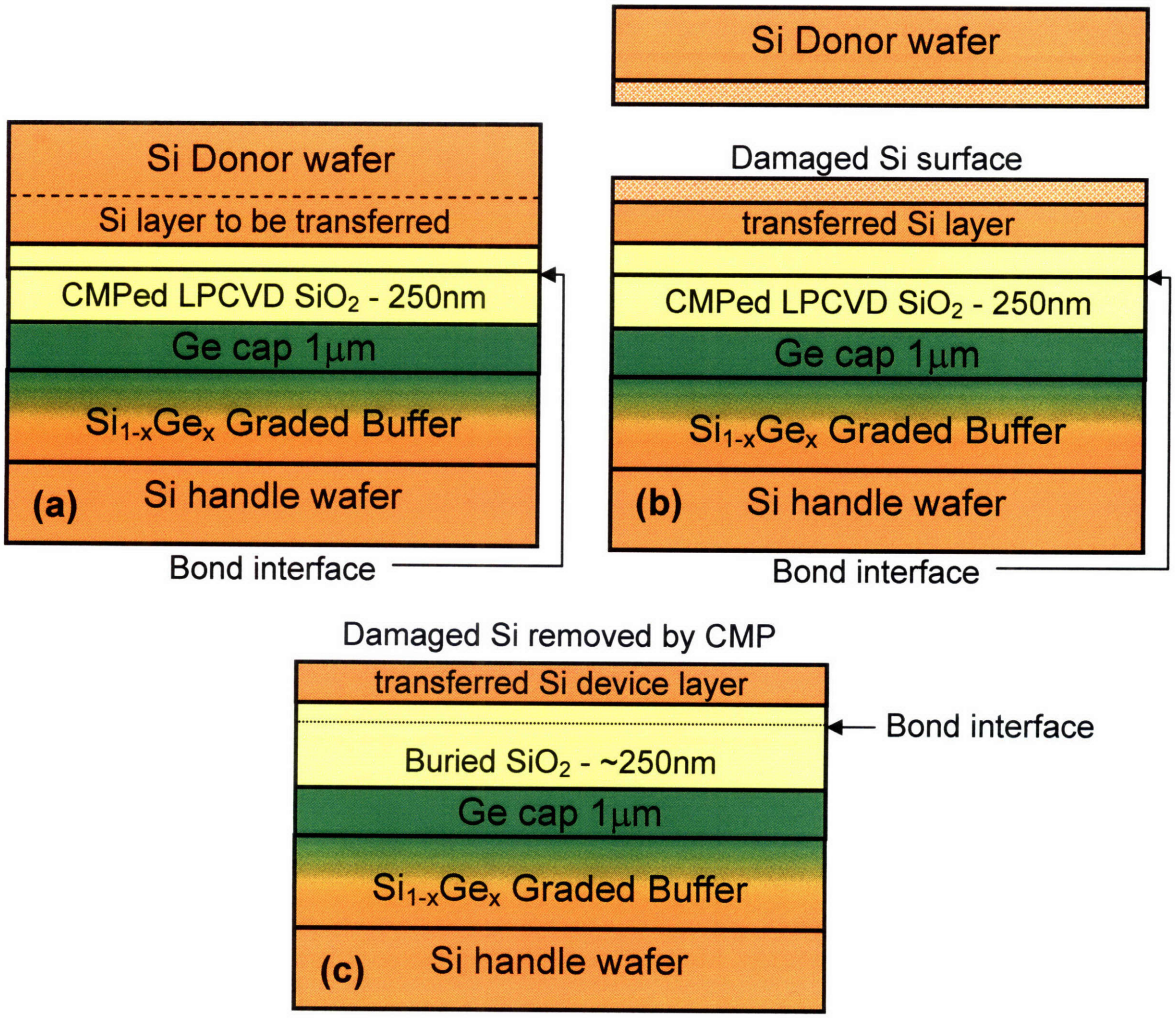


Figure 4.7 - Schematic of bonded pair process steps in SOLES process. (a) bonding of donor and handle wafers together, (b) exfoliation of donor wafer from bonded pair by annealing, leaving Si transfer layer and exfoliation damage, (c) removal of damaged Si from transfer layer surface using CMP, resulting in completed SOLES wafer.

4.5 Results of SOLES Fabrication Process

After designing the SOLES process, the process was used to fabricate SOLES wafers using facilities at the MIT Microsystems Technologies Lab (MTL). Initial efforts to fabricate SOLES wafers used $Si_{0.04}Ge_{0.96}$ virtual substrates, which are expected to behave very similarly to Ge virtual substrates. Figure 4.8 shows cross-sectional TEM of a SOLES wafer fabricated following the above process up to the layer exfoliation step (i.e. exfoliation damage was not removed from this sample). The inset clearly shows the

layer structure of the SOLES platform. The layer thicknesses measured in xTEM closely match the target layer thicknesses from the SOLES process design, further validating the success of the process design effort.

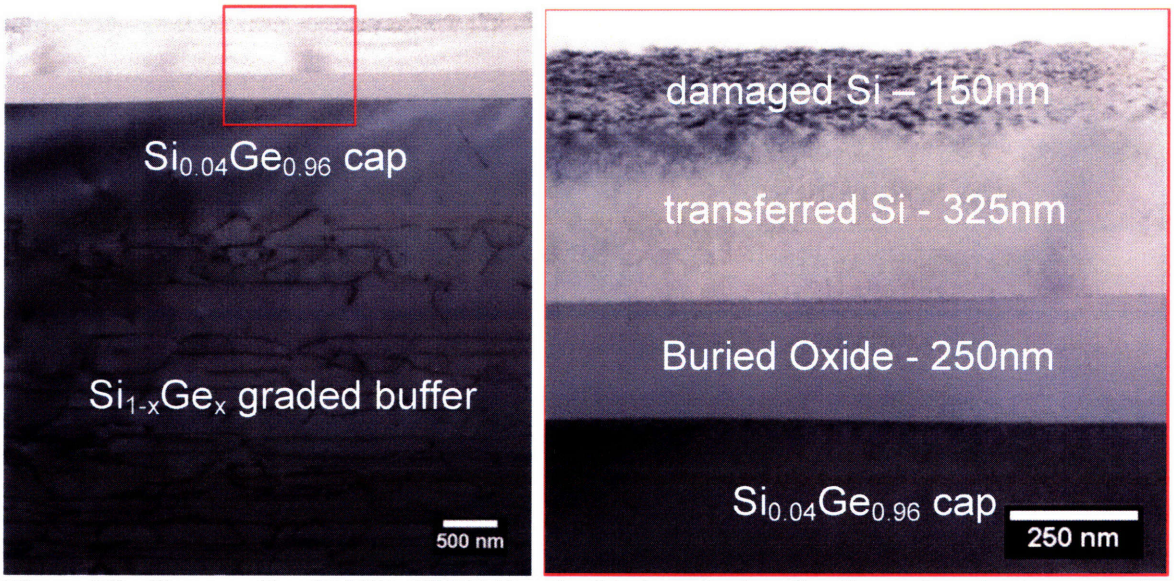


Figure 4.8 – Cross-sectional TEM of SOLES wafer fabricated using $Si_{0.04}Ge_{0.96}$ virtual substrate and without removal of the exfoliation damage from the surface. The right image shows the inset of the left image.

The next step in demonstration of the SOLES process is removal of the exfoliation damage shown in Figure 4.8. This was not attempted in initial trials because it was feared that the friction applied to the film by the CMP might overcome the bond strength, causing delamination of the transferred Si layer. The work of Bruel [31] only mentions that a "touch CMP" step is required to remove exfoliation damage, and no specific descriptions of this step appear in the literature. Thus, the next SOLES was CMPed for 10sec increments, in between which it was viewed under Nomarski to observe the change in exfoliation damage with added CMP time. The results from this experiment are shown in Figure 4.9. High surface roughness due to exfoliation damage is clearly visible in the first image, and this roughness steadily declines as CMP time

increases, until there is only a very small amount of damage visible at 30sec. This shows that only very short CMP times are required to remove the exfoliation damage.

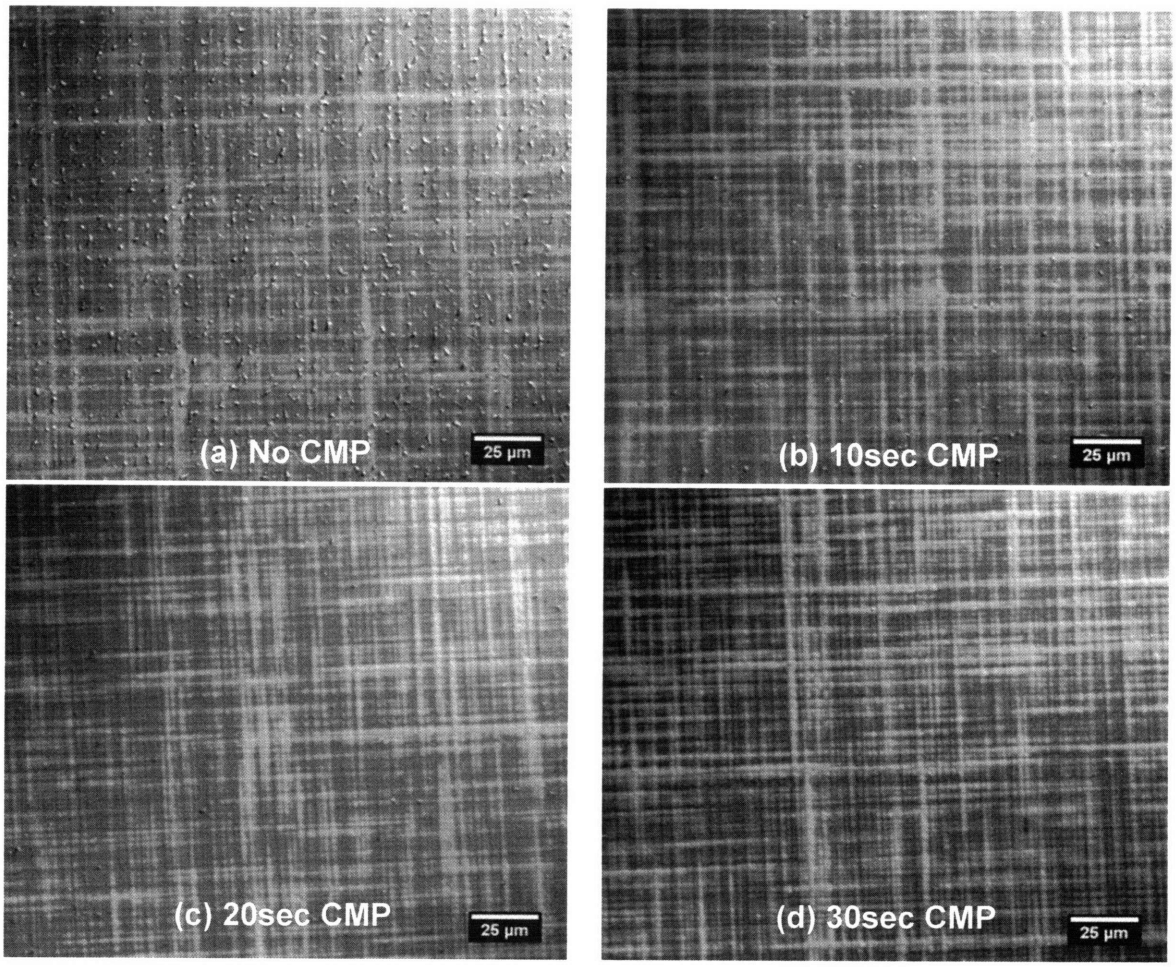


Figure 4.9 – Nomarski images of exfoliation damage removal from SOLES sample by CMP. Images a-d correspond to CMP times of 0, 10, 20, and 30sec, respectively.

After 30sec total CMP time, CMP of this sample was halted for more detailed characterization. A photograph of this sample is shown in Figure 4.10. The areas without layer transfer are noted in the figure; all other regions of the wafer had successful layer transfer. Based on this image, the fraction of wafer area with successful layer transfer is estimated to be 88%. This is notable because many studies involving layer transfer often achieve successful transfer over only very small portions of the sample, but the areal fraction with successful transfer is generally not reported. The process

developed in this study is capable of achieving transfer across the vast majority of the wafer surface, and the bonding interface is strong enough to withstand the friction of CMP without delamination. The only areas of the film removed by CMP are near the corners of the flat, but these were removed by polishing all the way through the transferred Si layer, not by delamination of the film (the material removal rate in these areas is faster due to pressure concentration from the CMP apparatus).

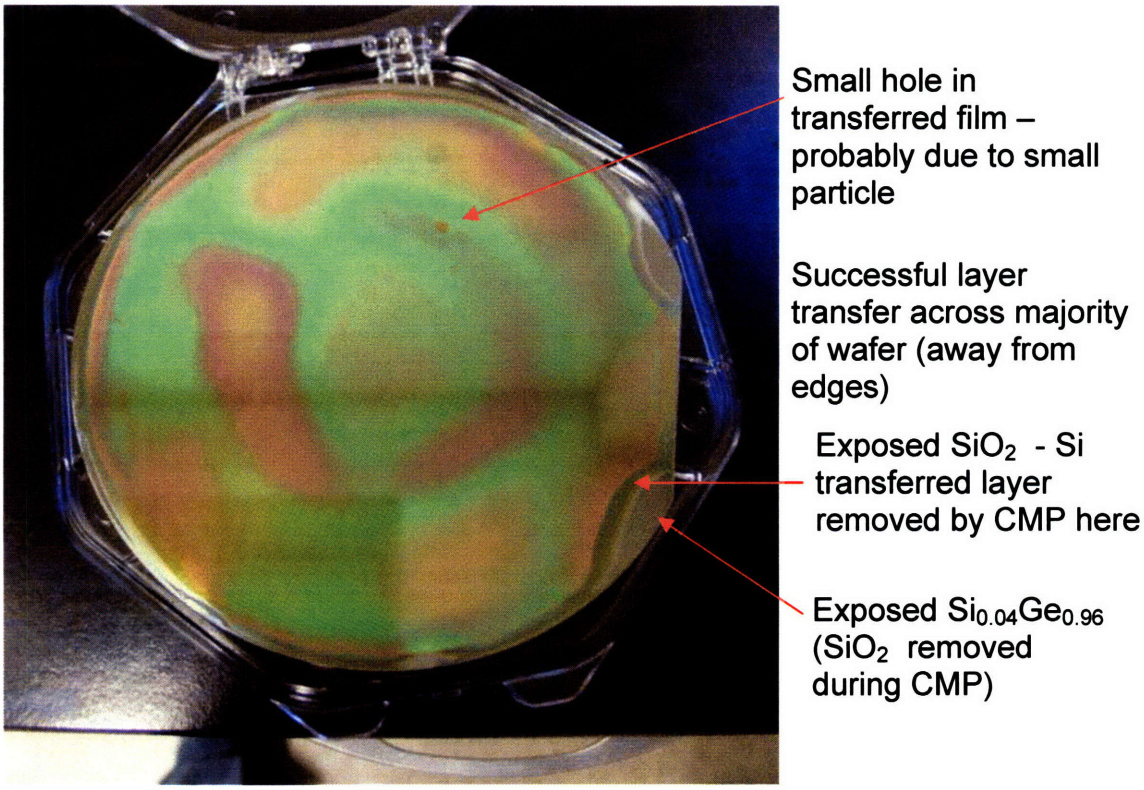


Figure 4.10 – Photograph of 150mm SOLES wafer after 30sec CMP to remove exfoliation damage. Layer transfer was successful across most of the wafer area, with minor exceptions as noted in the figure. The color variation across the center of sample area is due to global non-uniformity in SiO_2 CMP layer after CMP.

The color variation seen in the central portion of the image is due to thickness variation in the SiO_2 CMP layer. This is suspected to be caused by unbalanced pressure distribution on the wafer by the CMP tool during planarizing. The CMP tool available for this study is not state-of-the-art, and it is expected that a more modern CMP tool

would produce a more uniform SiO_2 layer. It should be noted that this global non-uniformity in SiO_2 thickness did not affect the amount of layer transfer achieved with this sample. Bonding strength is primarily determined by surface roughness with a lateral size scale of microns or smaller. Submicron variations in surface height across macroscopic size scales are gradual enough to not disrupt the bonding strength [30].

After CMP, this sample was sectioned for cross-sectional TEM. The results of this are shown in Figure 4.11. This figure shows that most of the hydrogen exfoliation damage has been removed by the CMP treatment, but the inset reveals that there is still a small thickness of damaged area that was not removed. Thus, some exfoliation damage remained in this sample despite the disappearance of roughness in Nomarski. However, this can be easily corrected in future SOLES process by using a slightly longer CMP time for exfoliation damage removal.

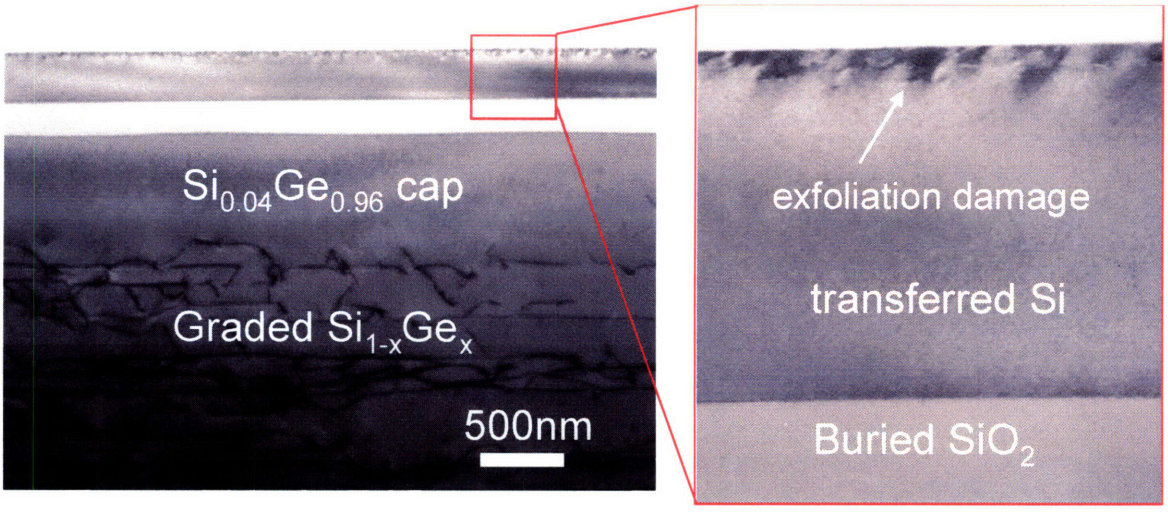


Figure 4.11 – Cross-sectional TEM of SOLES wafer after 30sec CMP to remove exfoliation damage. This image shows that not all exfoliation damage was removed with this treatment.

4.6 Demonstration of AlInGaP LEDs on SOLES Platform

After the successful fabrication of the SOLES platform in this study, it was desired to demonstrate an optoelectronic device on the SOLES platform to further build the case for SOLES as a platform for III-V/CMOS monolithic integration. For this phase of the SOLES project, which was led by Chilukuri [58], the device chosen for a demonstration was an AlInGaP LED. The composition of the device layers in the AlInGaP structure was chosen to be lattice-matched to GaAs (which in turn is closely lattice-matched to Ge) to ensure that dislocations are not generated in the device layer. An illustration of the process used in this project is shown in Figure 4.12.

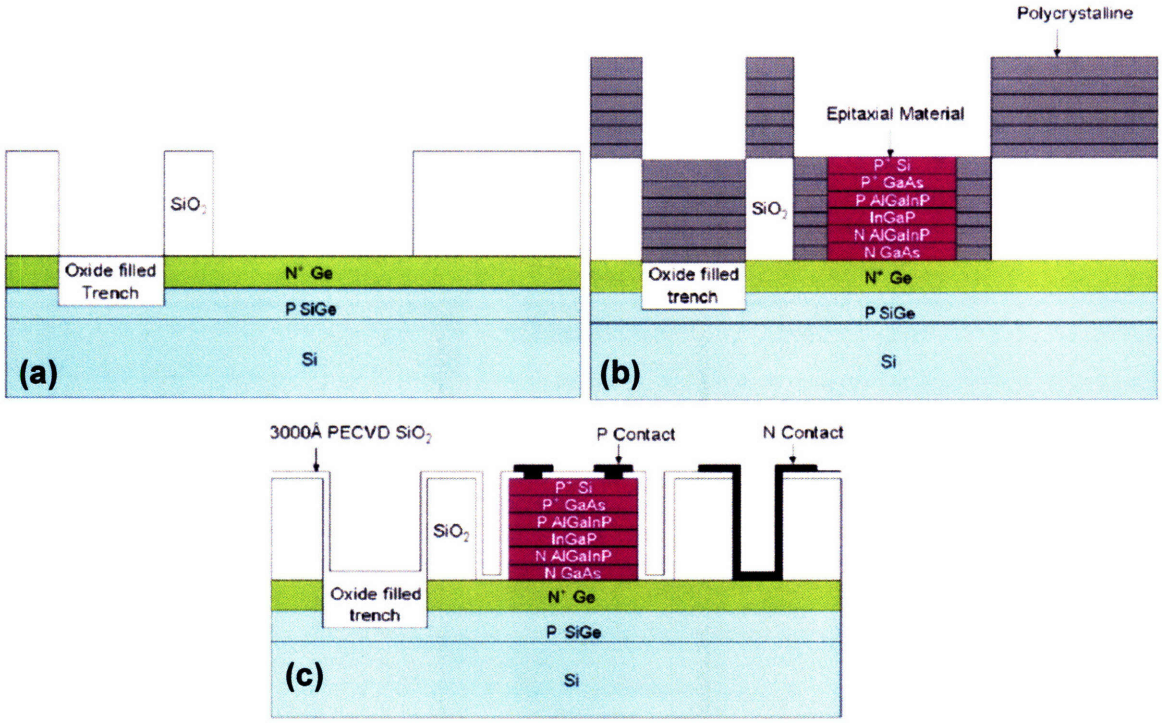


Figure 4.12 – Process illustration for AlInGaP LED fabrication on SOLES (a) Device isolation and mesa etch to expose Ge device layer for III-V growth, (b) Epitaxial growth of AlInGaP LED structure on the Ge epitaxial template with polycrystalline AlInGaP deposits across the rest of the sample area, (c) AlInGaP LED passivating oxide deposition and metallization, showing final LED structure. Image adapted from Chilukuri [59].

Mesa etches are first made through the Si and SiO_2 layers to expose the Ge epitaxial template (Figure 4.12a). An epitaxial AlInGaP LED structure is then grown on the Ge

template using MOCVD, while polycrystalline AlInGaP is deposited by the MOCVD process on the rest of the area of the wafer (Figure 4.12b). Then, a passivating oxide is deposited and metallization is used for the final component of LED fabrication (Figure 4.12c).

Cross-sectional TEM of the AlInGaP LED structure grown in this project is shown in Figure 4.13. This figure shows an absence of both threading and misfit dislocations in the AlInGaP layers, which is indicative of close lattice-matching. The texture of the AlInGaP layers is unusual, which may indicate that the growth was not entirely defect-free.

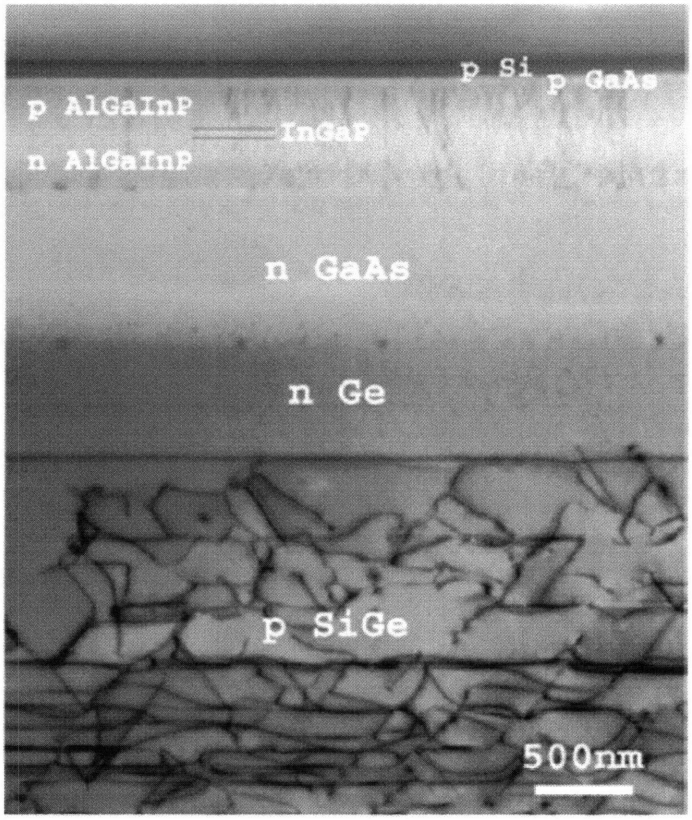


Figure 4.13 – Cross-sectional TEM of AlInGaP LED epitaxial structure on SOLES platform. Image adapted from Chilukuri [59].

The device process of Chilukuri resulted in successful fabrication of AlInGaP LEDs operating in the visible spectrum. Images of these LEDs under test are shown in

Figure 4.14. In these images, the illumination produced by the LED can be clearly seen, indicating successful operation. The LEDs operated with a peak wavelength of 671nm. The successful demonstration of AlInGaP LEDs on SOLES further validates the feasibility of SOLES as a platform for monolithic III-V/CMOS integration.

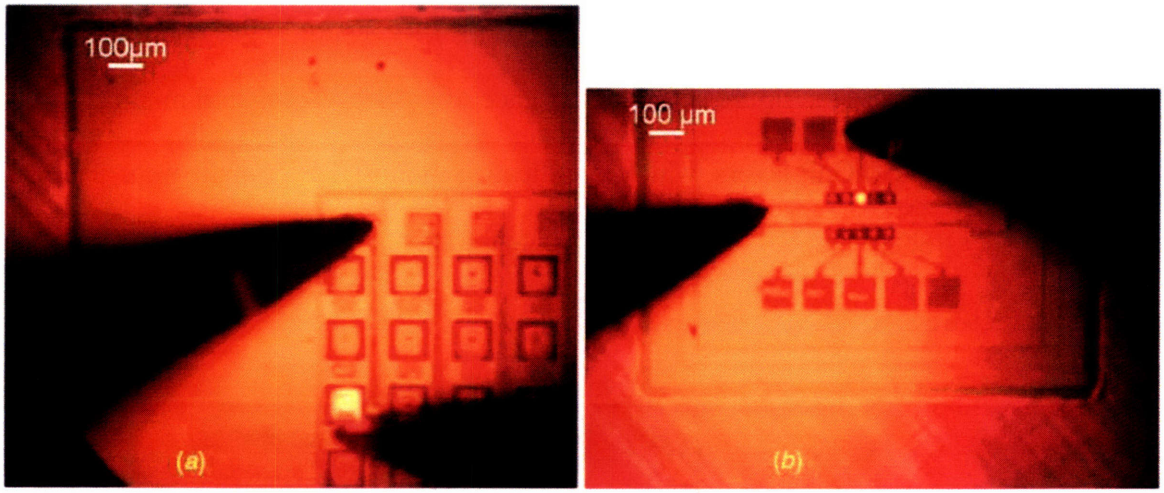


Figure 4.14 – Images of AlInGaP LEDs on SOLES substrate under test. (a) LED with 100x100µm pixel emitting area, and (b) LED with 20x20mm pixel emitting area. Image adapted from Chilukuri [59].

4.7 Summary

The SOLES substrate platform is a way to enhance the utility of the Ge virtual substrate for III-V/CMOS monolithic integration. The addition of an SOI structure on top of the Ge virtual substrate allows the wafer to be processed much like a traditional SOI wafer for CMOS fabrication, after which the buried Ge layer can be accessed by etching through the SOI and GaAs-based device structures can be grown by selective area epitaxy on the Ge surface. The SOLES platform can be fabricated in a variety of ways, and in this study the SOLES platform was fabricated with a CMP layer on the Ge virtual substrate to reduce surface roughness and hydrogen-induced layer exfoliation to achieve layer transfer. Demonstration of this process resulted in successful layer transfer across 88% of the handle wafer, which is expected to be improved with the use of more

advanced processing equipment. The bond strength of the transferred layer was sufficient to withstand the frictional force of CMP without delaminating. An appropriate CMP process was developed for removing exfoliation damage from the surface. The feasibility of III-V device growth and fabrication on the SOLES platform was established by successful fabrication and testing of AlInGaP LEDs on a SOLES wafer.

Chapter 5: Thermally-Relaxed Ultra Thin (TRUT) $Si_{1-x}Ge_x$ Compositionally Graded Buffers

5.1 Introduction

In the previous chapter, we described how the SOLES platform can greatly enhance the utility of the Ge virtual substrate for monolithic integration. One benefit provided by the SOLES platform is that it allows for coplanar integration of the III-V and Si device layers despite the presence of the thick (~10μm) $Si_{1-x}Ge_x$ graded buffer. However, SOLES does not alleviate all the challenges created by the thickness of the $Si_{1-x}Ge_x$ graded layer. Namely, the problems of thick III-V layer cracking and the low thermal conductivity of the $Si_{1-x}Ge_x$ graded buffer will still afflict OEICs fabricated on the SOLES platform. In addition, the TDD level and surface roughness of the Ge virtual substrate in a SOLES wafer are expected to have the same negative effects on GaAs-based device performance and reliability that they have on GaAs-based devices fabricated on stand-alone Ge virtual substrates. Thus, there is still significant motivation to reduce the key metrics of TDD, graded layer thickness, and surface roughness of the $Si_{1-x}Ge_x$ graded buffer.

In this study, we investigate an alternative growth process, first proposed by Gupta [14], for improving the aforementioned metrics. This process involves low-temperature coherent growth of lattice-mismatched layers followed by post-growth annealing to achieve relaxation of the layer. In order to understand the potential benefits of this process, the next section reviews the work of Gupta, which will be used as a starting point for the work presented in this chapter.

5.2 Review of Previous $Si_{1-x}Ge_x$ TRUT Buffer Work

While the $Si_{1-x}Ge_x$ compositionally graded buffer work reviewed in Chapter 2 focused on continuous growth at high temperature, results by Gupta [14] have recently

shown benefits from an alternative growth process. This process featured a multi-stage cycle consisting of three parts: low-temperature coherent growth of a mismatched buffer layer (up to 0.42% mismatch) above the Matthews-Blakeslee critical thickness, post-growth annealing of the layer to achieve partial relaxation, and growth of a strain-relieving layer at high temperature to drive the coherently-grown layer to full relaxation. This process, which Gupta [14] refers to as the thermally relaxed ultra-thin (TRUT) buffer process, can then be repeated at higher Ge content to further extend the graded buffer in Ge content. Because of the larger grading increment used with this method, it is possible to achieve more rapid grading rates while maintaining a TDD value at or below the level expected for a traditional graded buffer process.

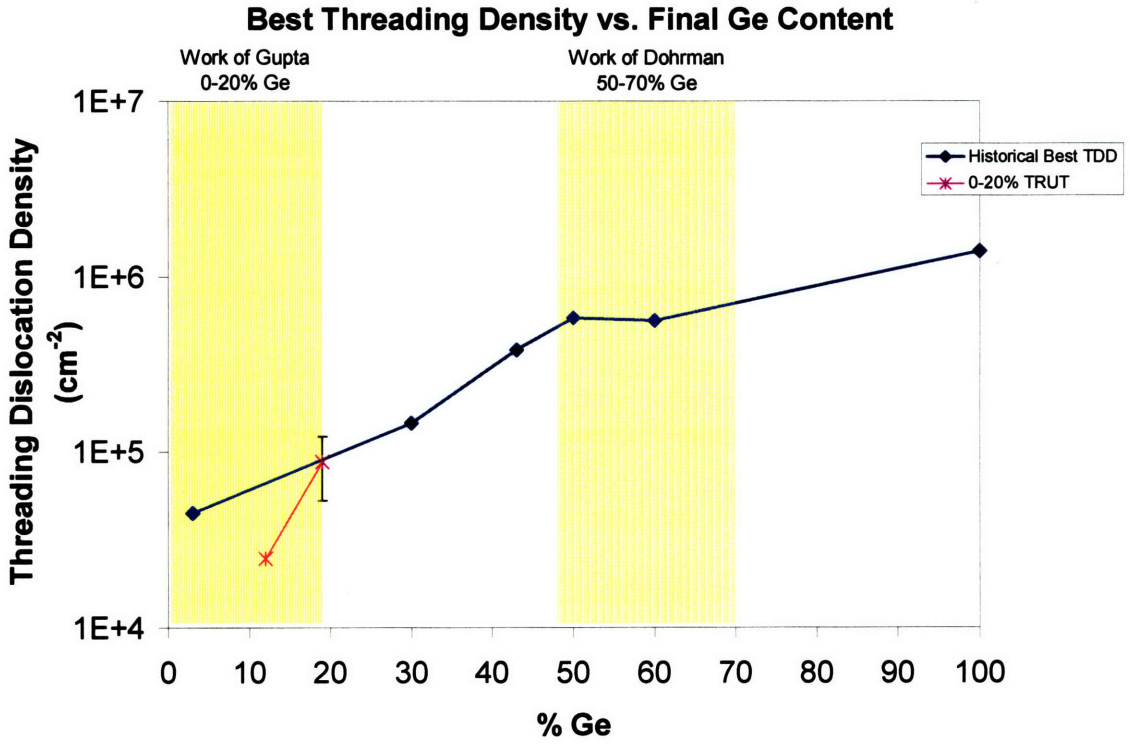


Figure 5.1: Plot of best attained threading dislocation density (TDD) versus Ge content of $Si_{1-x}Ge_x$ cap for "conventional" compositionally graded $Si_{1-x}Ge_x$ graded buffers and the TRUT process by Gupta [14]. **The conventional buffers were graded at a rate of 10%Ge/μm, while the TRUT buffer shown was graded at 21%Ge/μm. Figure adapted from Leitz** [16] **with additional data from Gupta** [14].

Gupta [14] reported fabricating a totally relaxed $Si_{1-x}Ge_x$ buffer graded from Si to $Si_{0.81}Ge_{0.19}$ using two stages of the process described above. This buffer possessed a TDD of $8.8x10^4$ cm^{-2} with a grading rate of 21%Ge/μm. For comparison, Figure 5.1 shows a plot of TDD versus Ge content of graded buffer cap comparing Gupta's results using the TRUT process to the conventional graded buffer grown at high temperature with a slower grading rate of 10%Ge/μm. The TRUT results have TDD levels that are comparable to the conventional $Si_{1-x}Ge_x$ graded buffer method but can achieve this using a much smaller thickness of the $Si_{1-x}Ge_x$ graded layer.

These results are encouraging, but they were limited to a $Si_{1-x}Ge_x$ composition range of $0 < x_{Ge} < 0.19$. In this study, we investigate the potential of extending the TRUT process to higher $Si_{1-x}Ge_x$ compositions.

5.3 Study of Relaxation of Single-Layer SiGe x_{Ge} =58% on x_{Ge}=46% Virtual Substrate

For this study, we chose to examine the properties of TRUT buffers over the composition range $0.5 < x_{Ge} < 0.7$ to see the effect of higher Ge content on the process. In order to provide a relaxed, low TDD platform for studying the $0.5 < x_{Ge} < 0.7$ alloy range, $Si_{0.54}Ge_{0.46}$ virtual substrates were grown using the conventional graded buffer process (900°C with 10%Ge/μm grading rate). This growth procedure produced a virtual substrate with a TDD of $2\text{-}5x10^5$ cm^{-2}, consistent with (or slightly better than) that reported by Leitz [16] for optimal TDD produced by the conventional graded buffer process. In addition, we then used chemo-mechanical planarization (CMP) to remove the crosshatch from the $Si_{0.54}Ge_{0.46}$ virtual substrates to give a highly planar starting surface for investigating the TRUT process.

For initial experiments, we started with growth of a single layer of various thicknesses with composition $Si_{0.42}Ge_{0.58}$ coherently on the $Si_{0.54}Ge_{0.46}$ virtual substrate. We used a growth temperature of 500 to 550°C for the coherent $Si_{0.42}Ge_{0.58}$ layer and then subjected them to a ramped anneal to 750°C to achieve relaxation. The growth and anneal temperatures were chosen so that the homologous temperature for the $Si_{0.42}Ge_{0.58}$ films (defined as T / T_{melt}) would match the homologous temperature used by Gupta for his work with $Si_{0.9}Ge_{0.1}$ films (Gupta used growth and maximum annealing temperature of 650°C and 900°C, respectively). The annealing sequence used for this study is shown in Figure 5.2. All samples were annealed using a ramp anneal at 125°C/hr to the desired maximum annealing temperature and then held there for 30min. In some of the early samples, this annealing sequence was approximated using the step anneal profile shown in the figure.

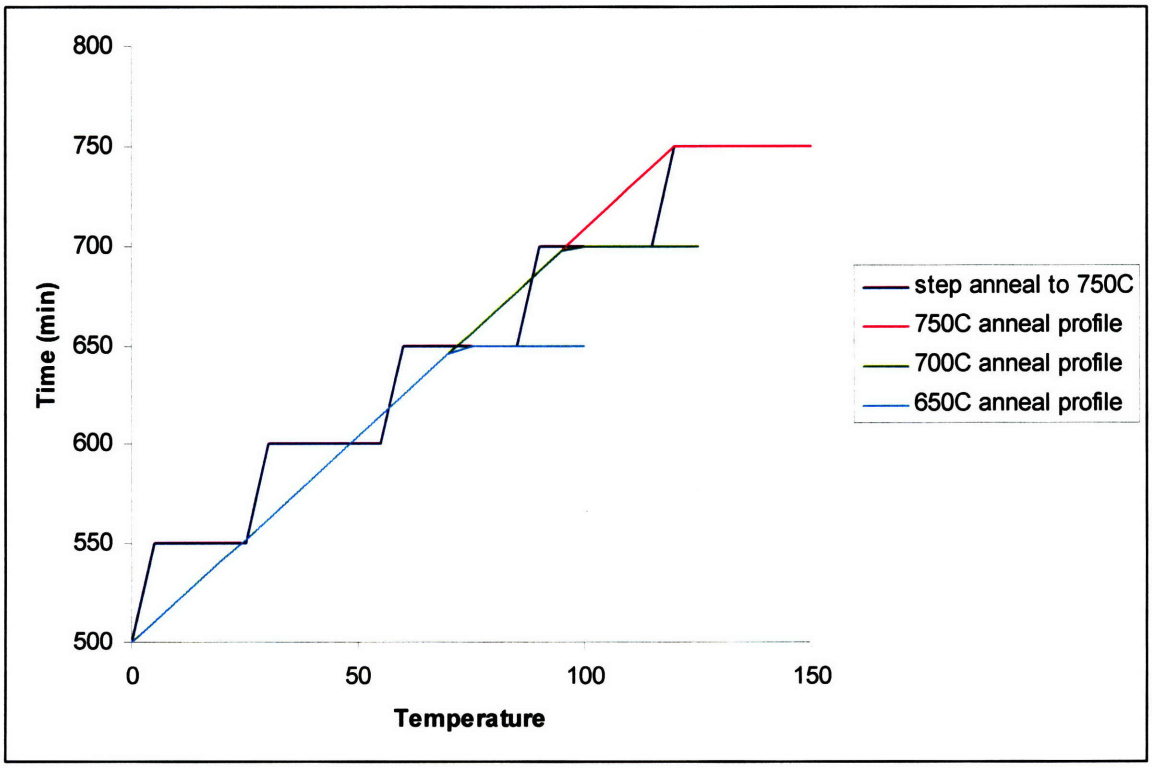


Figure 5.2 – Annealing profiles used for post-growth relaxation of TRUT layers in this study.

The relaxation of each layer was measured using x-ray diffraction (XRD) and is plotted in Figure 5.3. This figure compares the measured relaxation values of the $Si_{0.42}Ge_{0.58}$ films to the equilibrium relaxation value calculated from Matthews-Blakeslee strained layer theory. The figure indicates that all the films remained well below their equilibrium relaxation values after the thermal annealing treatment. This is consistent with the results of Gupta for $Si_{0.9}Ge_{0.1}$ layers, which led him to the use of strain-relieving layers to achieve further relaxation. However, Figure 5.3 also indicates that the thicker layers showed higher surface roughness. Because surface roughness is expected to be deleterious to further graded buffer growth, the 100nm layer was chosen for experiments with strain-relieving layers to achieve more complete relaxation while maintaining low surface roughness.

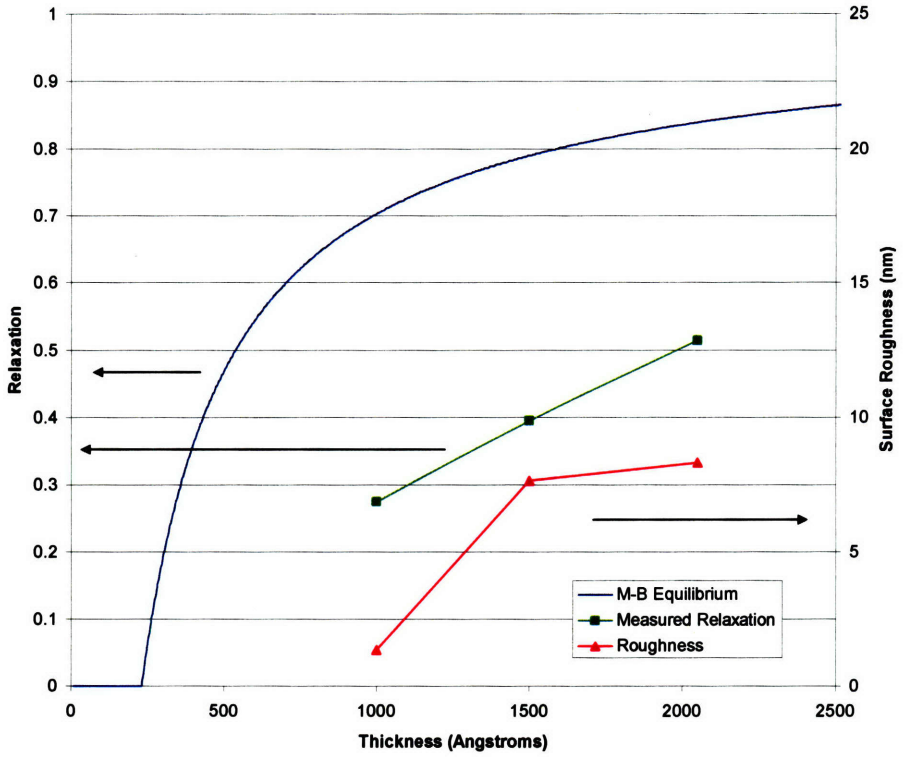


Figure 5.3: Plot of measured values of relaxation (left y-axis) and surface roughness (right y-axis) versus thickness of x_{Ge} =58% films on x_{Ge} = 46% virtual substrates after a ramped annealing sequence up to 750°C. Also plotted is the Matthews-Blakeslee (M-B) equilibrium value of relaxation versus thickness for the films. The samples in this experiment remained well below the equilibrium values, while surface roughness increased with increasing film thickness.

5.4 Study of strain-relief layer for x_{Ge} = 58% layer on x_{Ge} = 46% virtual substrate

In the strain-relieving layer experiment, both low and high temperature strain-relief layers were employed. Following the procedure for single-layer study, $Si_{1-x}Ge_x$ films with x_{Ge} = 58% were first grown to 100nm and step-annealed to 750°C. In the high-temperature experiment, a 210nm x_{Ge} = 60% film was grown at 750°C, which was again chosen so that the homologous temperature of this film matched the homologous temperature of the corresponding layer in the work of Gupta. As shown in Figure 5.4, xTEM of this sample revealed that the strain-relief layer experienced substantial roughening which makes it likely that it will not be suitable for continued compositional

grading. This differed substantially from the expected result, as Gupta reported that a high-temperature x_{Ge} = 12% layer on an x_{Ge} =10% strained layer experienced no such roughening. Because the increase in Ge content of the strain-relief layer is so small compared to the x_{Ge} = 58% layer, there is little margin with which to further decrease the Ge content of this layer. Thus, it seemed that lowering the growth temperature would be necessary to prevent roughening of the surface.

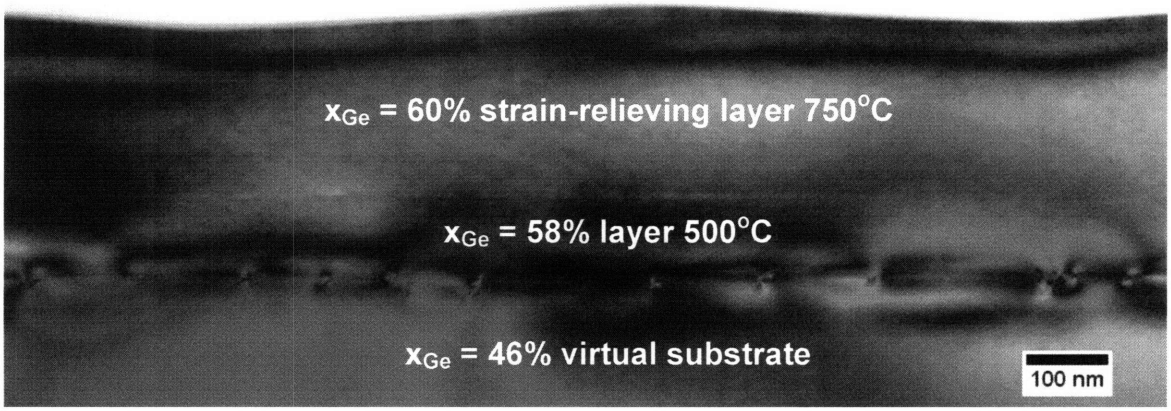


Figure 5.4: cross-sectional TEM image of a TRUT sample consisting of a single low-temperature layer with a high-temperature strain-relieving layer grown to induce relaxation. There is obvious undulation visible on the strain-relieving layer surface, indicating poor surface roughness.

For the low temperature experiments, the initial growth step at 500°C consisted of 100nm of x_{Ge} = 58% with 20nm of x_{Ge} = 68% $Si_{1-x}Ge_x$ as the strain-relief layer. The strain-relief layer was kept below its critical thickness on the x_{Ge} = 46% lattice in order to ensure that it did not relax. In one sample, the strain-relief layer was grown on the surface of the sample, while in another sample it was grown in the middle of the x_{Ge} = 58% layer. These samples were then subjected to the same 750°C annealing sequence as used previously.

xTEM images from these samples are shown in Figure 5.5. Figure 5.5a and b show the sample with the strain-relief layer on top before and after annealing, respectively. Figure 5.5a reveals that the sample grew in a planar fashion with minimal

surface roughness, while Figure 5.5b shows the extreme islanding effect of the anneal. Evidently, the surface diffusivity of the strain-relief layer during the anneal was sufficient to drive this layer from a highly planar film to a series of islands on the surface. Figure 5.5c shows xTEM of the sample with the strain-relief layer in the middle after the annealing treatment. In this case, the strain-relief layer was buried within the x_{Ge} = 58% material, thus blocking surface diffusion as a mechanism for roughening. Because the x_{Ge} =58% Ge layer is under 45% less strain than the x_{Ge} =68% layer, there is considerably less driving force to induce islanding, and thus it is able to withstand the annealing treatment.

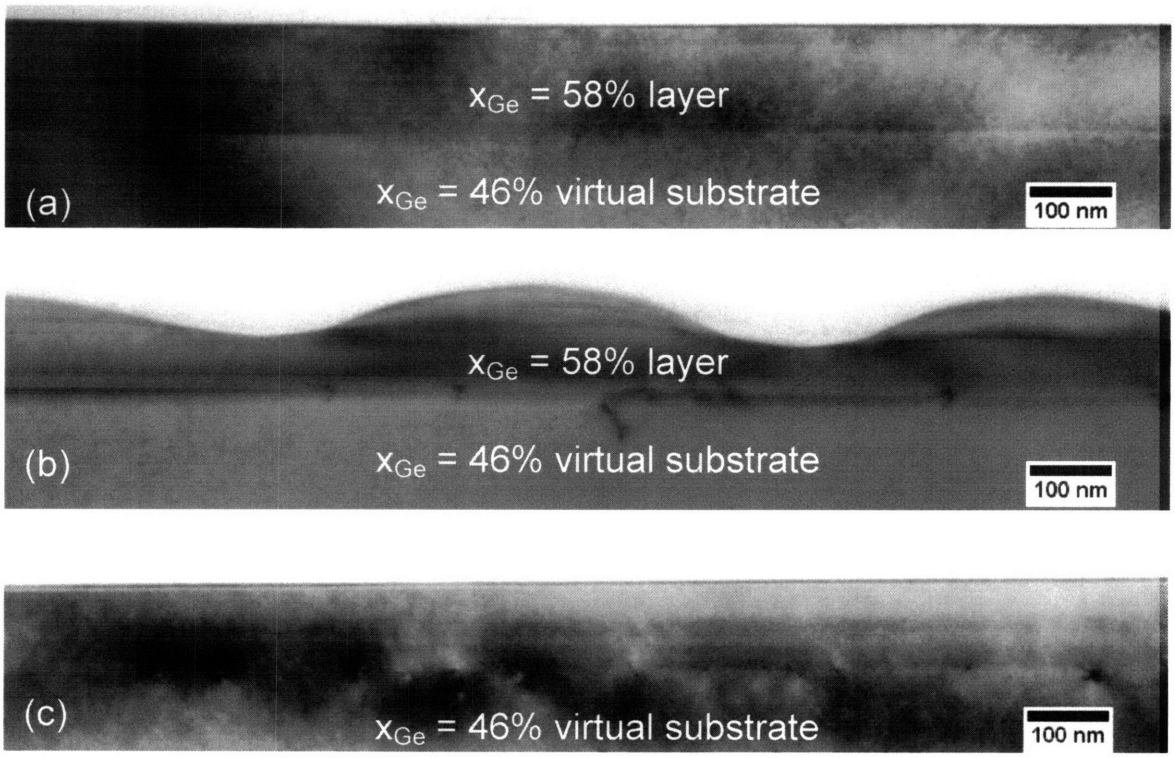


Figure 5.5 – xTEM images of TRUT samples with low-temperature strain-relieving layers. (a) - single-layer TRUT with low-temperature x_{Ge} = 68% strain-relieving layer on surface before annealing. (b) – sample from image (a) after annealing. (c) TRUT layer with x_{Ge} = 68% strain-relieving layer inserted in center of x_{Ge} = 58% layer. Note that image (c) is after annealing to 750°C.

Figure 5.5c clearly shows an array of misfit dislocations at the interface between the x_{Ge} = 58% layer and the x_{Ge} = 46% virtual substrate. XRD and pvTEM of this specimen revealed a relaxation of 56% within this sample, which is higher than is achieved with a single x_{Ge} =58% layer at twice the thickness. Figure 5.6 is a representative pvTEM image of this specimen, revealing an orderly misfit dislocation network. Also, AFM measurements indicated a RMS surface roughness of 1.1nm, nearly equal to that of the 100nm single-layer sample. This is shown compared to other TRUT samples in Figure 5.7.

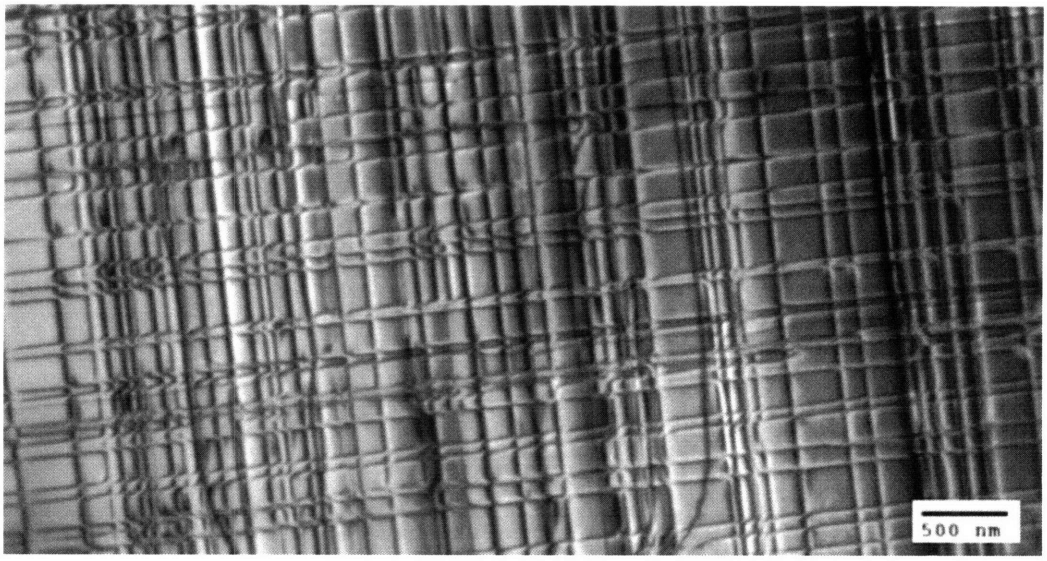


Figure 5.6 – Representative plan-view TEM image after annealing of x_{Ge} = 58% TRUT layer with strain-relieving layer inserted into middle of x_{Ge} = 58% layer.

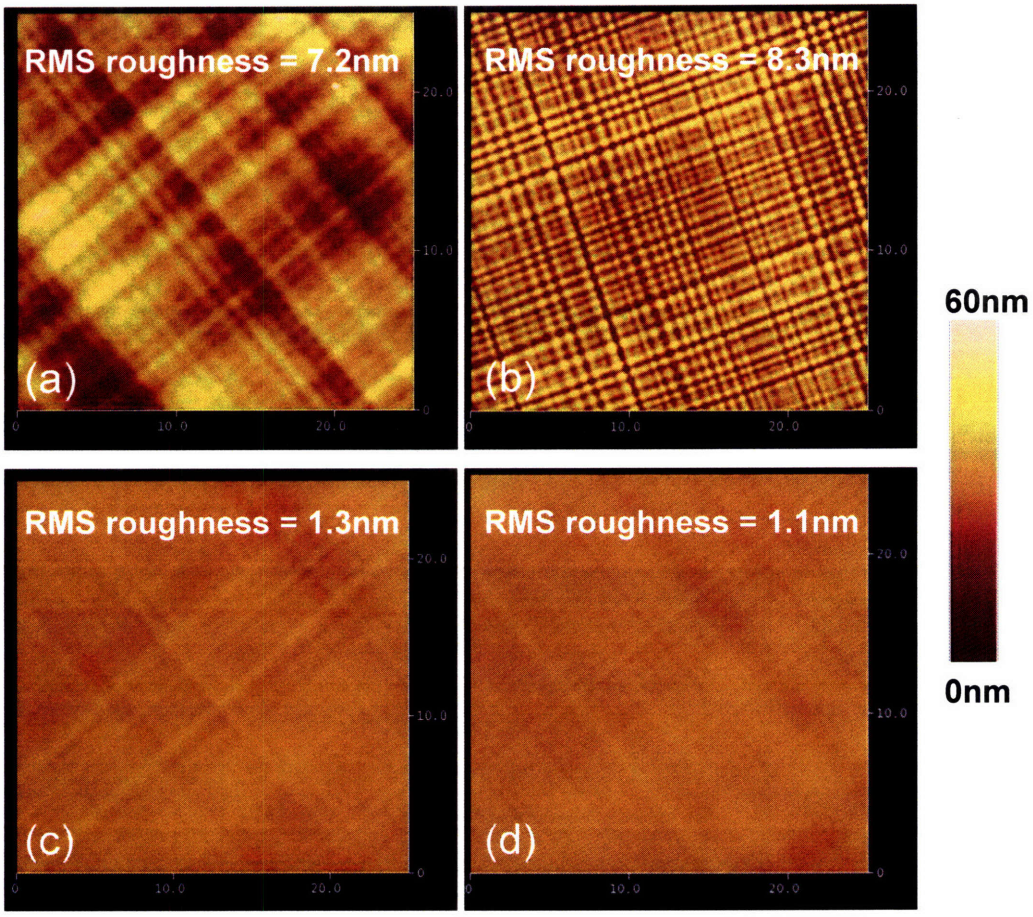


Figure 5.7 – AFM images of TRUT samples and control after annealing. (a) – Conventional graded buffer capped with x_{Ge} = 58%. (b) – Single-layer 200nm TRUT structure, (c) – Single-layer 100nm TRUT structure, (d) – Single layer 100nm TRUT with strain-relieving layer inserted.

5.5 TRUT layers with small Ge increments

The procedure involved so far in this work has employed growing layer with a compositional change of x_{Ge} = 12% from the underlying virtual substrate. This process led to a dilemma: growth of thick layers leads to high surface roughness, while growth of thin layers produces difficulty in achieving a high degree of relaxation. One potential reason for the lack of complete relaxation of the TRUT structures is the density of misfit dislocations. As a mismatched layer relaxes, misfit dislocations must cross over or bend around misfits orthogonal to them in order to continue extending. This is clearly visible in Figure 5.6. Fitzgerald [41] showed that misfit dislocations can impede dislocation

motion, leading to incomplete relaxation or nucleation of additional threading dislocations to complete the relaxation. This is one reason that the conventional graded buffer process uses small (~2%Ge) composition increments. If the single-layer 12%Ge composition jump is replaced with a series of smaller composition jumps, the high misfit density at the x_{Ge} = 58% - x_{Ge} = 46% interface will be replaced with several interfaces with much lower misfit density, easing the propagation of dislocations through the structure. Thus, we investigated altering the TRUT process to replace the single high-mismatch layer with several low mismatch layers. An outline of the revised process is shown in Figure 5.8.

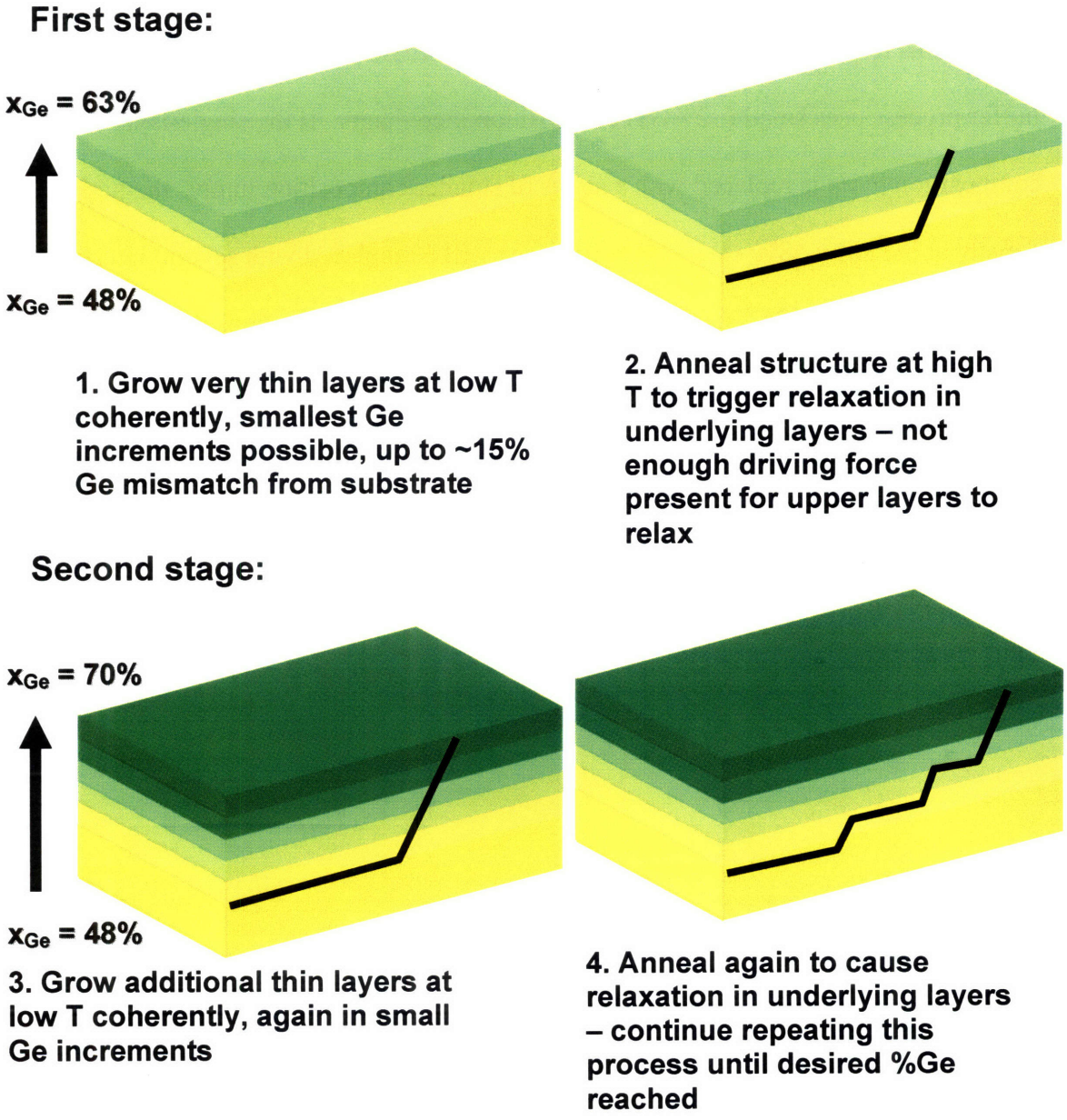


Figure 5.8 – Outline of process for graded TRUT experiments

For the next experiment, it was desired to measure the TDD of the samples since this is one of the primary metrics of graded buffers. For TDD values in this range (~10^5 cm^{-2}), etch-pit density is the usual technique employed. The work of [43] found that the etch-pit density etchant proposed by [42] for (100) Si can be used to observe threading dislocations in $Si_{1-x}Ge_x$ alloys up to x_{Ge} = 70%. However, etch-pit density measurements

necessarily etch the surface, and the measurement will be made very hard to interpret if the layer of interest is completely removed during the etching process. The $Si_{1-x}Ge_x$ layers in the present study are as thin as 100nm, substantially thinner than those used by [43] in her study (~1μm), so a test was done on a thick (~1μm) x_{Ge} = 58% layer to determine the minimum etch depth required to form observable etch pits on the surface of the layer.

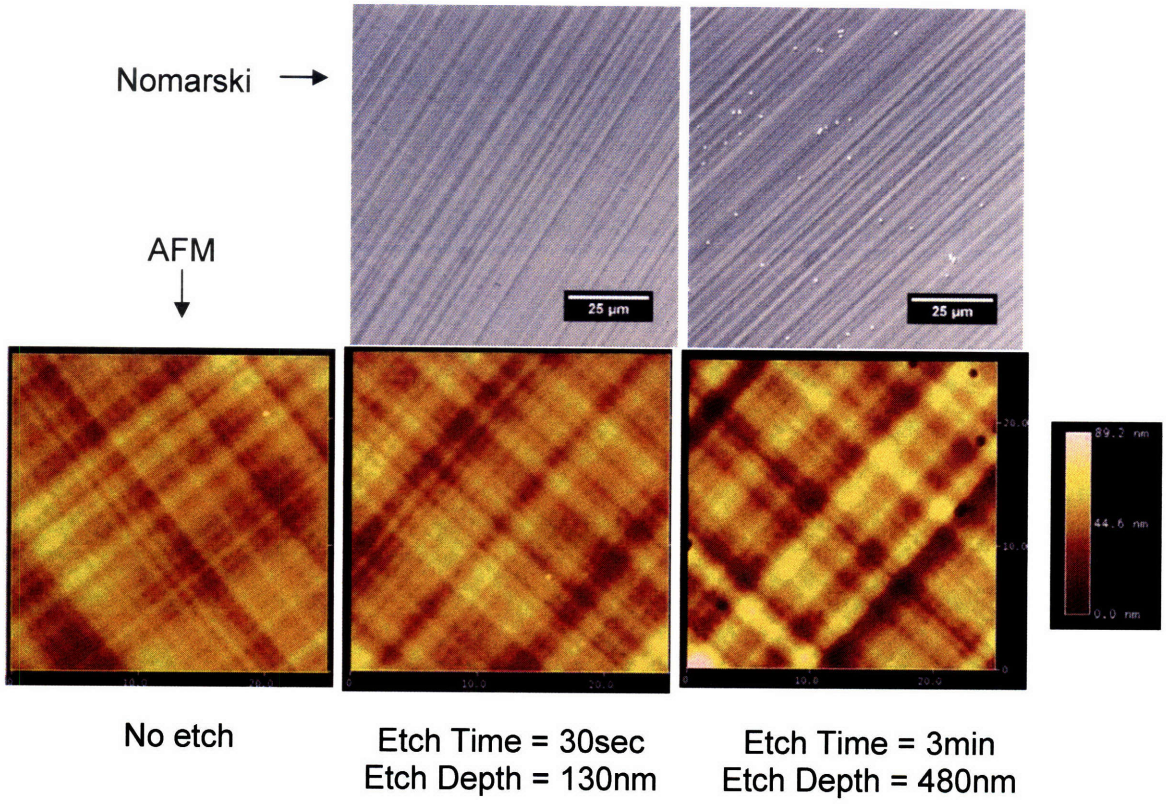


Figure 5.9 – AFM and Nomarski microscopy images showing the effect of etch time on etch pit formation using etchant employed in this study. Results show that an etch depth of 480nm is required to reveal etch pits in this Ge composition range, thus necessitating the EPD cap employed in this study.

This test revealed that an etch depth of 480nm was required to reveal etch pits using this etchant, far greater than the 100nm thickness of the thinnest layers found in this study. At an etch depth of 130nm, no pits can be observed using either Nomarski optical microscopy or AFM, making EPD measurement impossible. This is shown in Figure 5.9.

Thus, in order to measure the TDD of the layers in this study, the following procedure was used. First, the sample of interest was grown and characterized by XRD to determine its strain state. Next, an identical sample was grown and annealed, but a thick 1μm cap layer (which we refer to as the "EPD cap") was added on top. The composition of the EPD cap was chosen to be lattice-matched to the underlying TRUT structure based on the strain measurement for the first sample. In this way, we were able to accurately make TDD measurements of each sample.

In the first experiment using both small grading increments and EPD caps, three samples with different grading rates were grown from x_{Ge} = 48% to 63% and then annealed using a ramped annealing process for a single iteration of the TRUT process (this corresponds to steps 1 and 2 in the process in Figure 5.8). Grading rates of 100%, 50%, and 25%Ge/μm were used, and a conventional graded buffer grown to x_{Ge} = 58% at 10%Ge/um was also prepared as a control sample. The process described above was used to obtain relaxation and TDD data for each sample.

The results of this experiment are shown in Figure 5.10. The relaxation data (plotted on the right side of the figure) show that more relaxation is achieved by using a slower grading rate, leading to a relaxation of 74%Ge.

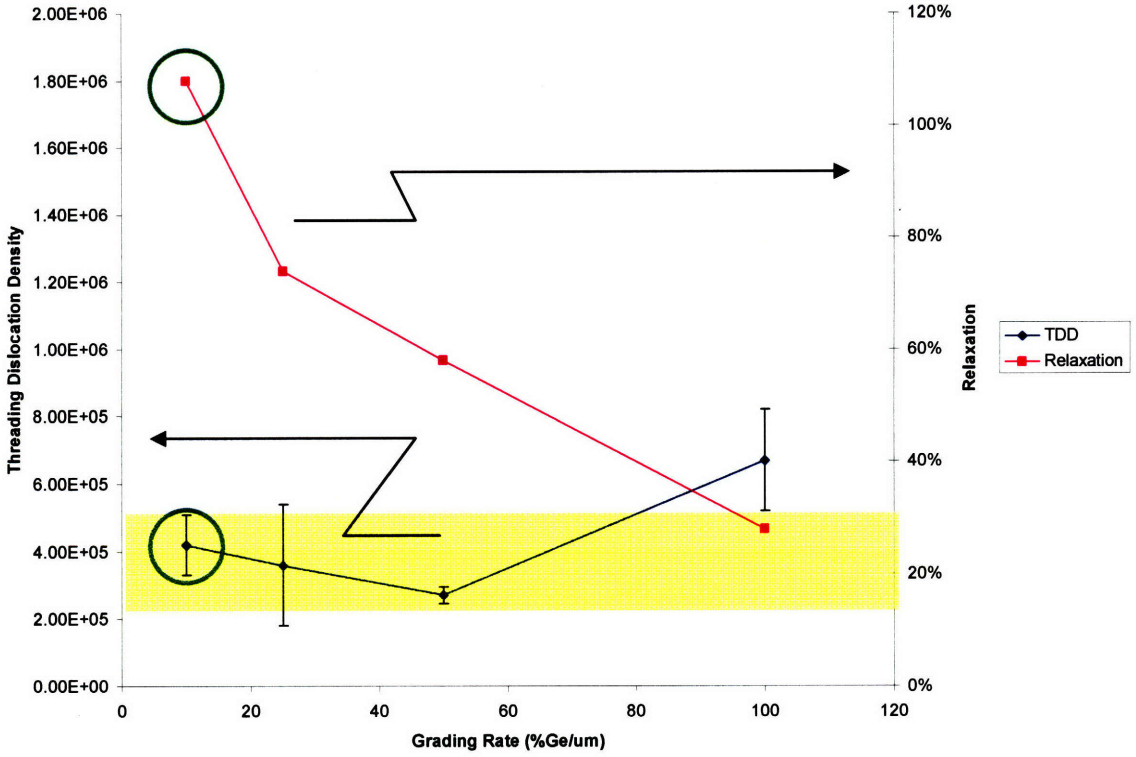


Figure 5.10 – Plot of TDD (left-hand side) and Relaxation (right-hand side) versus grading rate for single-stage graded TRUT samples. The circled data points correspond to the control sample fabricated using the conventional graded buffer process. The shaded region denotes the TDD range that is observed with x_{Ge} = 48% virtual substrates.

In comparing the TDD values for the respective samples, it should be noted that there is variation in the TDD of the x_{Ge} = 48% virtual substrate starting material. Throughout this project, the TDD of x_{Ge} = 46-48% virtual substrates was measured from a few wafers from each batch to ensure uniformity in the starting material for TRUT experiments (the virtual substrates were prepared in batches of ten wafers each). This practice found some batch-to-batch variation as well as variation within each batch. The distribution of different batches spans a range from 2.0 - 5.4 $x10^5$ cm^{-2} and is shown in Figure 5.11. The etch-pit density process is destructive, and thus it is not possible to measure the TDD of a virtual substrate and then grow a TRUT structure on it. So, this

work relied on random sampling of virtual substrates to ensure that the batch fell within the range shown in the graph below.

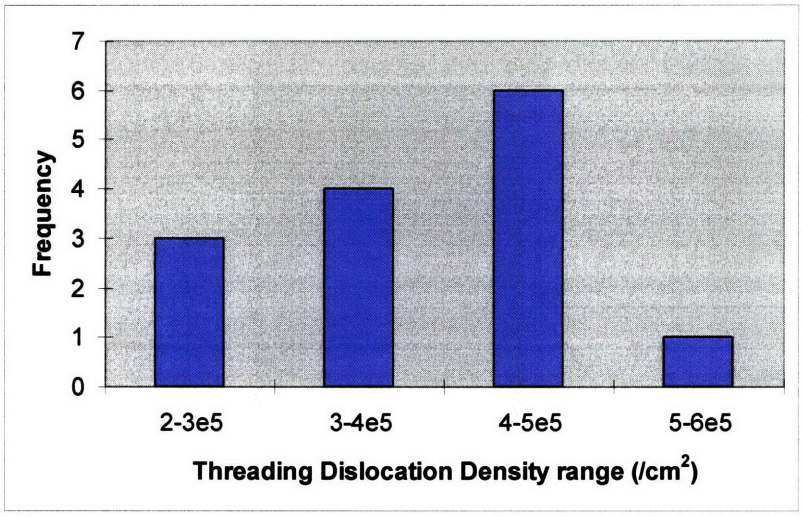


Figure 5.11 – Histogram of threading dislocation density values of x_{Ge} = 46-48% virtual substrates used in this study. This variance must be taken into account when comparing TDD values of TRUT samples since the samples do not all start with the same TDD.

In light of this, we can now interpret the TDD data of Figure 5.10. The shaded band in the figure indicates the range of TDD levels spanned by the virtual substrate starting material. Thus, any measured TDD values that fall within this range could represent no change from the virtual substrate starting material. The TDD data for the 25%Ge/μm, 50%Ge/μm, and control sample all fall within this range, and thus they most likely represent a negligible change from the virtual substrate. The TDD for the 100%Ge/μm sample is slightly above this range, so it most likely experienced some increase from the virtual substrate.

Results from xTEM also indicated the worse quality of the 100%Ge/μm sample. This is shown in Figure 5.12. Pit-like defects were seen in the 100%Ge/μm sample running throughout the thickness of the TRUT layers. Although they could not be identified, it seems highly likely that they would be disruptive to graded buffer growth

and material quality, and avoidance of them seems wise. No such defects were observed in the 25%Ge/μm and 50%Ge/μm; these samples appeared planar with no observable defects.

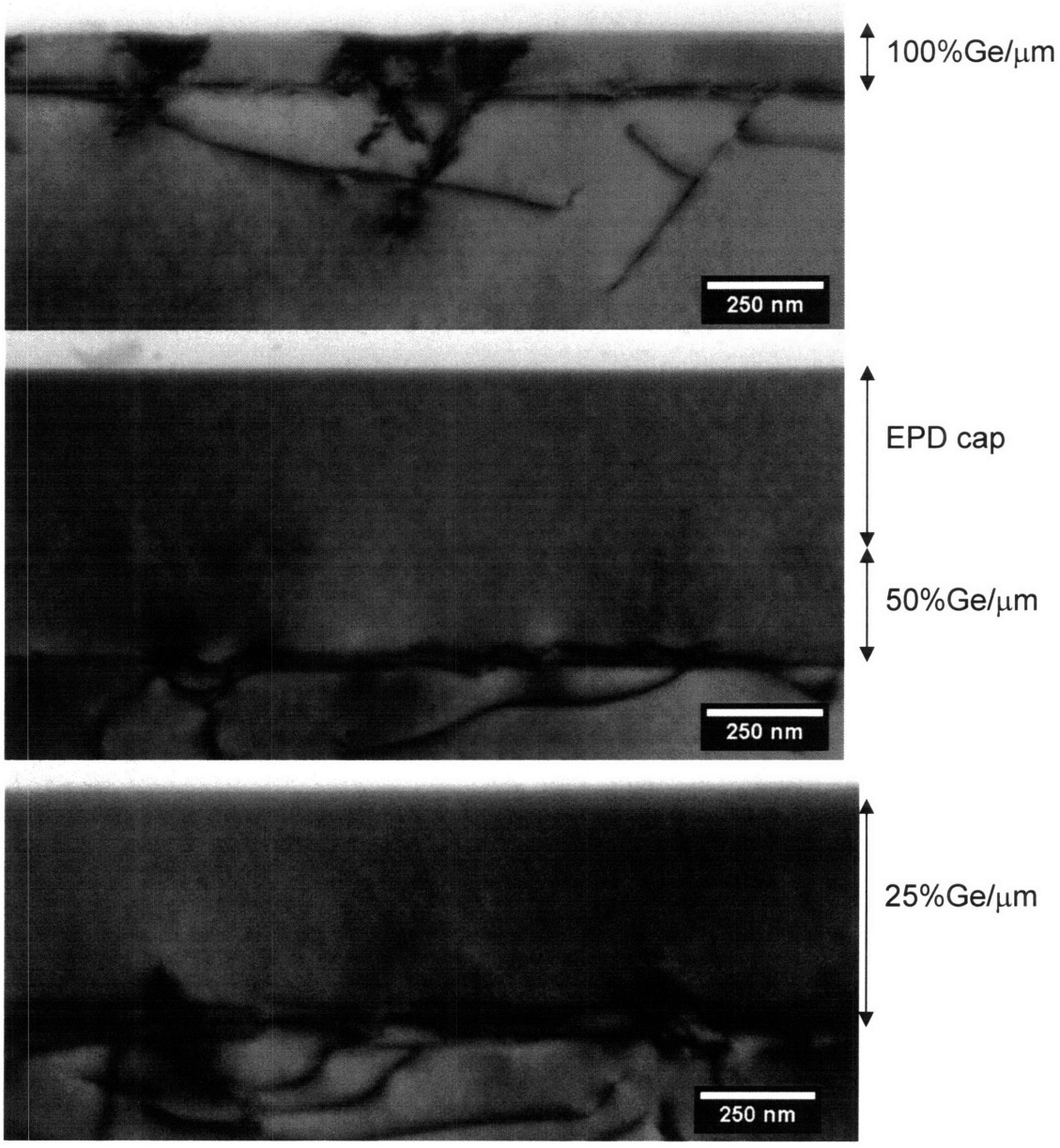


Figure 5.12 – xTEM of single-stage x_{Ge} = 48-63% graded TRUT structures after annealing. (a) – 100%Ge/μm, (b) 50%Ge/μm with EPD cap, (c) 25%Ge/μm

5.6 Two-stage TRUT Experiments

Based on these results, it appears that both the 25%Ge/μm and 50%Ge/μm could be viable grading rates for a multi-stage TRUT buffer process. For the next experiment,

a two stage TRUT growth (steps 1-4 of procedure in Fig. 2.8) was tested. The grading range for each stage was the same for each sample: stage 1 was graded from x_{Ge} = 48% to 63% and stage 2 was graded from x_{Ge} = 63% to 70%. The grading range for stage 2 was approximately half that of stage 1 because the 50%Ge/μm single-stage sample only achieved 58% relaxation; thus, the in-plane lattice parameter of this layer is approximately the equivalent of a relaxed x_{Ge} = 56% relaxed layer. Thus, growth of strained x_{Ge} = 70% material on this epitaxial template will be under roughly the same strain as the growth of x_{Ge} = 63% layer was on the x_{Ge} = 48% virtual substrate.

This experiment consisted of three samples with grading rates for stage 1 and 2 specified in Table 2.1 below:

Table 5.1 – Description of two-stage graded TRUT structures fabricated for this study

Sample	Stage 1 Grading Rate (grading from x_{Ge} = 48 – 63%)	Stage 2 Grading Rate (grading from x_{Ge} = 63 – 70%)
1	50%Ge/μm	20%Ge/μm
2	50%Ge/μm	40%Ge/μm
3	25%Ge/μm	25%Ge/μm
control	10%Ge/μm (conventional)	10%Ge/μm (conventional)

After growth and annealing, these samples were characterized by EPD and XRD. By combining the TDD data of these samples with the data for single-stage TRUT, we can create a picture of how the TDD changes from the first stage to the second stage. This is depicted in Figure 5.13, which shows the TDD plotted as a function of Ge content in the cap layer. The data for x_{Ge} = 48% comes from the virtual substrate, the data for x_{Ge} = 63% comes from the single-stage TRUT samples, and the data from x_{Ge} = 70% comes from the two-stage samples. In the first stage, the TDD of all the samples is roughly indistinguishable from that of the control sample as well as the range of TDD observed in x_{Ge} = 48% virtual substrates (this range is again denoted by the shaded region).

However, this graph indicates that there is a definite increase in TDD introduced by the second stage, as all the two-stage samples clearly increase in TDD while the control sample is still indistinguishable from the initial virtual substrate.

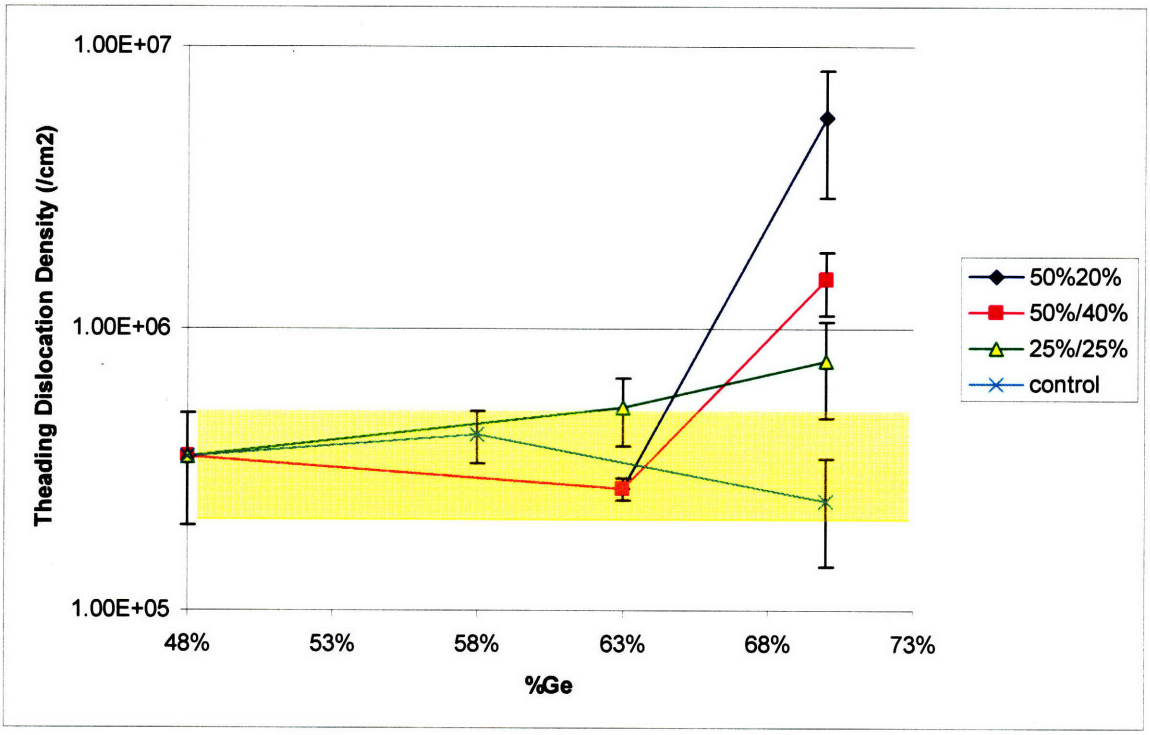


Figure 5.13 – plot of TDD versus Ge content for TRUT samples and control after annealing. Data for x_{Ge} = 48, 63, and 70% corresponds to the virtual substrate, single-stage TRUT, and two-stage TRUT samples, respectively.

Figure 5.14 shows the change in strain state (expressed as the relaxed x_{Ge} equivalent of the measured in-plane lattice parameter) plotted against the Ge content of the cap layer. After the first stage, there is residual strain left in the TRUT layers due to incomplete relaxation. During the second stage anneal, there is generally a greater change in lattice parameter because the partially strained layers from first stage are relaxing in addition to the layers from the second stage. This added relaxation seems to create more need for dislocation nucleation, thus explaining the increase in TDD observed during this stage. Thus, one can conclude that the more rapid grading rate of

the TRUT process does not lead to an increase in TDD in the first stage, in part due to incomplete relaxation at that stage, but that the addition of the second stage increases the total strain energy in the film, leading to increased threading dislocation nucleation. It should be noted that Gupta also observed a large TDD increase between the first and second stages (from x_{Ge} = 12% to x_{Ge} = 19%), as shown in Figure 2.8, thus suggesting that this effect is observed across a wide $Si_{1-x}Ge_x$ composition range.

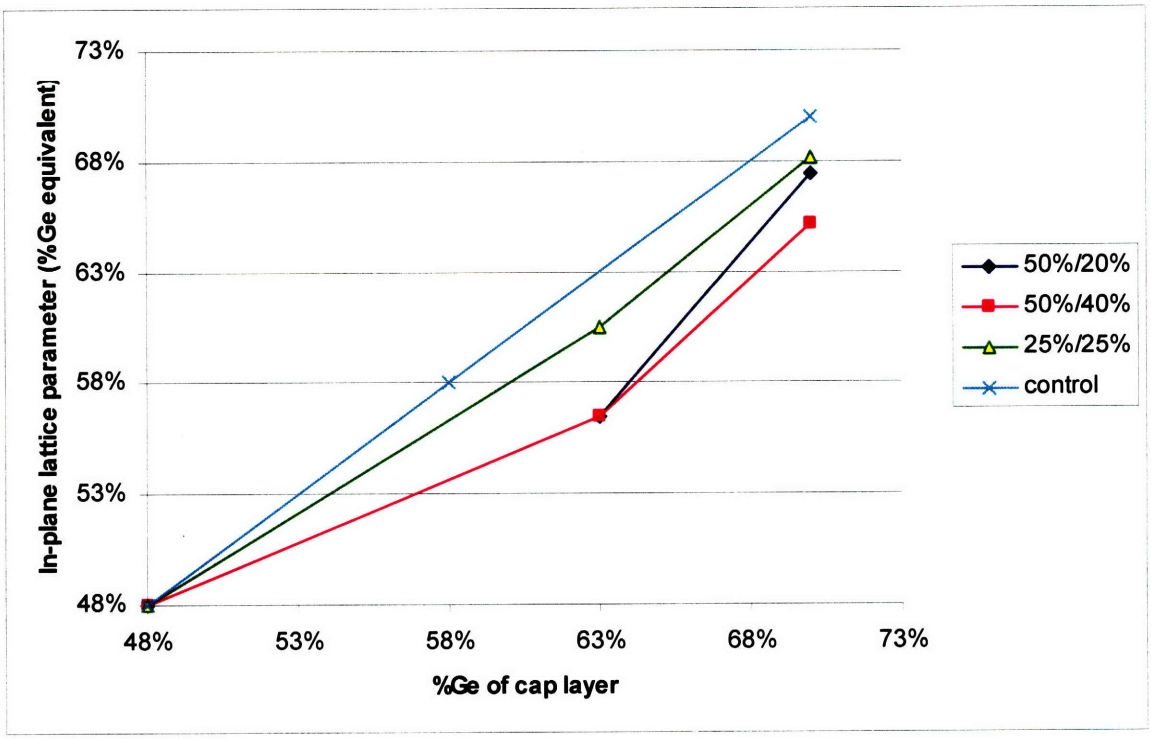


Figure 5.14 – Plot of in-plane lattice parameter (given in terms of its x_{Ge} equivalent) versus actual x_{Ge} of cap layer for TRUT samples. Again, data for x_{Ge} = 48, 63, and 70% corresponds to the virtual substrate, single-stage TRUT, and two-stage TRUT samples, respectively.

These samples were also characterized using cross-sectional TEM. TEM results of all three samples are shown in Figure 5.15. In cross-section, most of the image appeared defect free, as shown in the left-hand side images in Figure 5.15. However, as shown in the right-hand side images, xTEM also revealed surface defects in each sample

similar to the ones observed in the single-stage TRUT sample graded to 100%Ge/μm (Figure 5.12a).

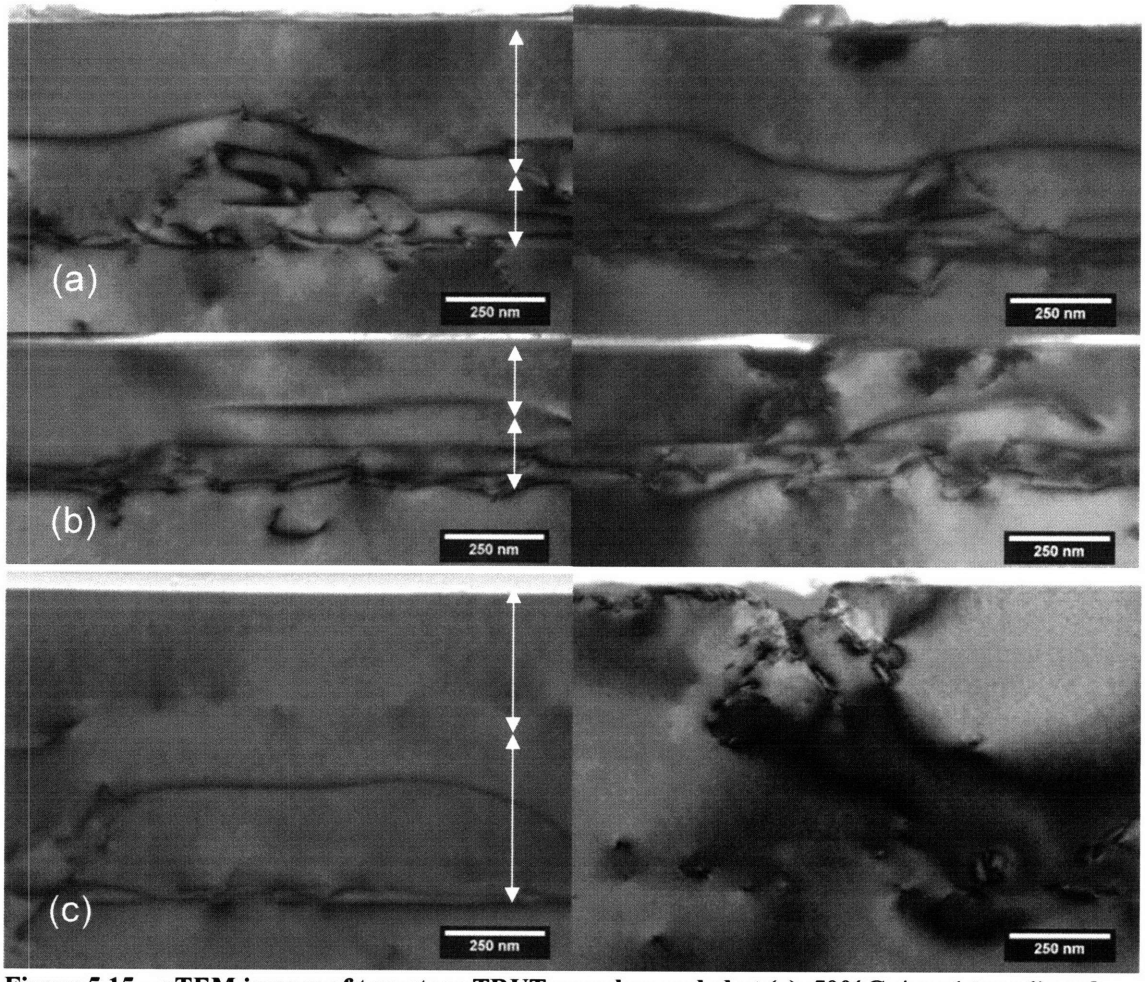


Figure 5.15 – xTEM images of two-stage TRUT samples graded at (a) 50%Ge/μm (stage 1) and 20%Ge/μm (stage 2), (b) 50%Ge/μm (stage 1) and 40%Ge/μm (stage 2), and (c) 25%Ge/μm (stage 1) and 25%Ge/μm (stage 2). The images on the left side correspond to good regions of the sample, while images on the right side show the surface defects observed in each sample. The arrows in the left side images indicate the approximate locations of the first and second stages in each sample.

The identity of these defects could not be firmly established. They are clearly three-dimensional as compared to one-dimensional (e.g. dislocations) or two-dimensional (e.g. stacking faults) defects. In several of the images, these defects have what appear to be threading dislocations originating from them, which suggests they could be acting as sites for heterogeneous nucleation of dislocations. The origin of these defects is also unclear. They were only observed in the two-stage TRUT samples and the 100%Ge/μm

single-stage TRUT sample. The problem occurs predominantly on the second stage of the TRUT process, so the cause could be related to the low-temperature growth of strained layers on an already-strained epitaxial template. It could also be related to the higher Ge content used in the second stage. The single-stage TRUT sample that exhibited these defects was also the one grown at the highest grading rate and thus had the highest strain level after post-growth annealing. This suggests that a high strain level at high temperatures is the cause of these surface defects. This could be caused by a strain-driven catastrophic surface nucleation event that nucleates these surface defects and their associated threading dislocations.

Regardless of their cause, these defects would no doubt be very detrimental to any further compositional grading or to any electronic devices processed with this material. The size of the defects is approximately 100-200nm, too small to be observed in the optical microscopy images used to collect etch-pit density data. Observation of these defects in xTEM indicates that they are probably at a high density due to the small sampling area used in this technique. In the case of threading dislocations, Fitzgerald [41] estimates that their observation in xTEM corresponds to an areal density of at least 10^8 cm^{-2}. If we assume that the same estimate holds for these defects, then they would be at a density at least 100 times higher than the typical TDD in conventional compositionally graded $Si_{1-x}Ge_x$ buffers would undoubtedly cause widespread problems at that density. Thus, the critical strain-driven nucleation process observed in this work limits the strain level which is tolerable for the TRUT process. Because the use of a second TRUT stage seems to increase this strain level above the critical value regardless

of grading rate, this phenomenon represents a major obstacle to the further development of the TRUT process in this composition range.

5.7 Application of TRUT to x_{Ge} = 90-100% Range

Facing this obstacle, alternative strategies were considered for continued progress. Figure 5.16 is a modified version of Figure 2.8 adding the TDD data from the best two-stage TRUT growth (25%Ge/μm for both stages) and from the control samples. It is noteworthy to point out that the control samples produced for this study showed superior TDD values than the best TDD values reported by Leitz for the conventional compositionally graded buffer process. Additionally, the expected trend for compositionally graded buffers is shown as they are graded from 70%-100%Ge.

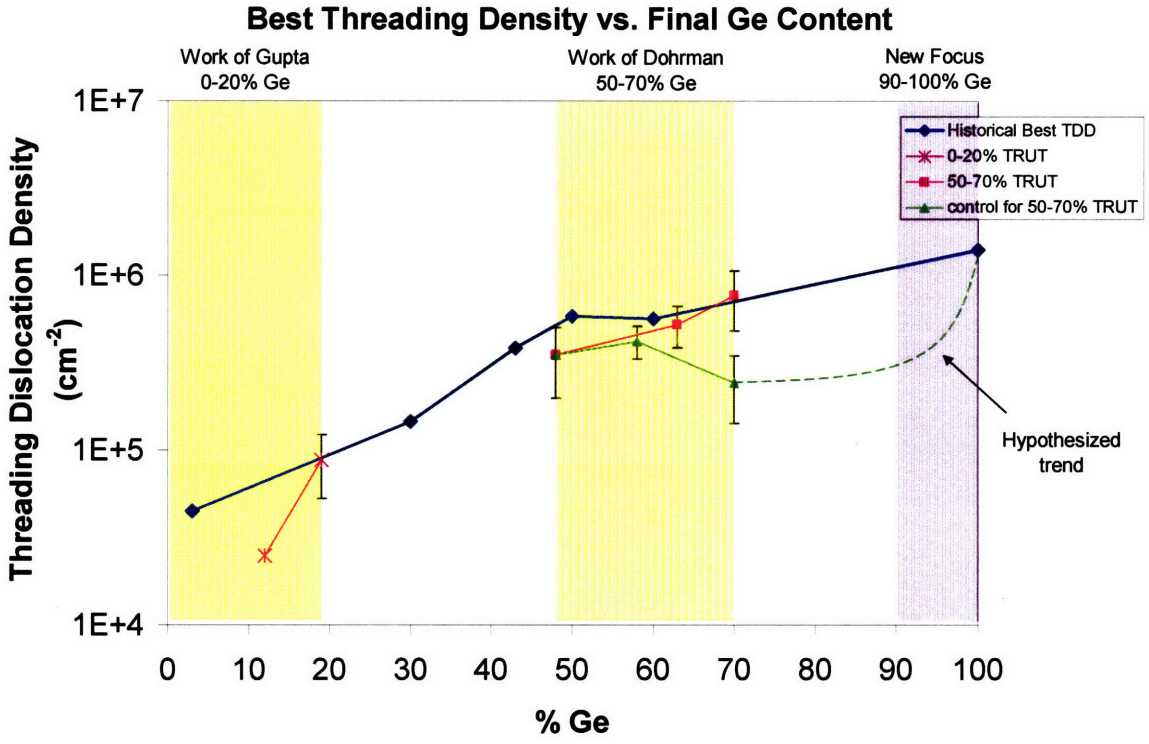


Figure 5.16 – Plot of TDD versus Ge composition of $Si_{1-x}Ge_x$ compositionally graded buffers, including results from conventional graded buffers, TRUT buffers of Gupta, TRUT buffers from this work, and control samples from this work. Also shown is the hypothesized trend for TDD for x_{Ge} = 70-100%.

As shown in Figure 5.17, Yonenaga [60] revealed that the yield strength of SiGe alloys drops dramatically as the Ge content goes from x_{Ge} = 90% to 100%, and the size of this effect increased as the temperature in increased. Isaacson [61] hypothesized that this would lead to a deviation from the graded buffer model of Fitzgerald [15] and cause an increase in TDD over this range. Thus, this composition range appears that it would be especially well-suited to benefit from the low-temperature TRUT process. In addition, because the composition range from x_{Ge} =90-100% can be spanned with a single TRUT stage, it would relieve the burden of having to use multiple TRUT stages and bypass the particulate defects that were observed in xTEM predominantly with two-stage TRUT growths. Thus, it is of interest to see if the TRUT process can improve upon the TDD of pure Ge conventional graded buffers, which have a TDD of 2 x10^6 cm^{-2}.

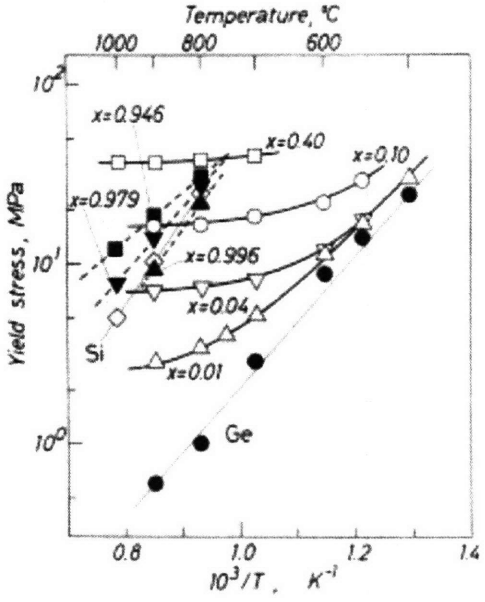


Figure 5.17 – Results from Yonenaga [60] **showing an Arrhenius plot of yield stress versus 1/T for bulk Si_xGe_{1-x} alloys. Note that in this figure x represents the Si content of the SiGe alloy (unlike the rest of this work which uses x to denote Ge fraction). The plot clearly illustrates a dramatic loss in yield strength from x_{Si} = 0.1 to x_{Si} = 0 (pure Ge). This effect is more severe at higher temperatures. Figure adapted from Yonenaga** [60].

In this experiment, x_{Ge} = 0 - 90% SiGe virtual substrates were prepared using the conventional graded buffer process. After growth of the x_{Ge} = 90% cap layer, the growth temperature was dropped to T = 450°C and two different growths were performed: a single layer of pure Ge and a graded region from x_{Ge} = 90-100% graded at 10%Ge/μm. Note that the second sample described is essentially identical to the conventional graded buffer process but with the temperature for the x_{Ge} = 90-100% portion dropped from 650 to 450°C. The growth temperature of 450°C was chosen because it is the lowest practical growth temperature for Ge in the UHVCVD reactor employed for this work; the growth rate drops exponentially with temperature in this range, and lower temperatures produce an impractically slow growth rate. The samples were then ramp-annealed to maximum temperatures of 550, 600, and 650°C, where 650°C corresponds to the temperature used for Ge growth in the conventional graded buffer technique. Etch-pit density and XRD were then used to determine the TDD and strain state of the sample, respectively.

A plot of TDD versus maximum annealing temperature for these samples is shown in Figure 5.18. The line across the sample indicates the typical TDD value for conventional graded buffers graded to pure Ge. As is clear from the graph, the single-layer Ge sample produced a TDD nearly equal to the conventional process, while the graded x_{Ge} = 90-100% process produced a TDD that is less than half that of the conventional process. Both samples produced slightly lower TDD values in the annealed versus un-annealed samples, although it is unclear from this graph whether this difference in TDD is statistically significant. Thermally-activated dislocation annihilation reactions, as described by Leitz [16], are a possible explanation for this trend. This effect can typically only make a slight impact on TDD for values in this range, which is consistent

with what is observed in this experiment. This annealing effect is more perplexing when one considers that the purpose of the anneal was to induce relaxation of the low-temperature-grown layers, which would be expected to either increase or hold constant the TDD level in these samples. However, XRD revealed that the pure Ge layers in both samples were fully relaxed even before annealing. Thus, there was no driving force for further nucleation of dislocation half-loops, and dislocation annihilation reactions are the only plausible mechanisms for change in TDD in these specimens, thus explaining the drop in TDD.

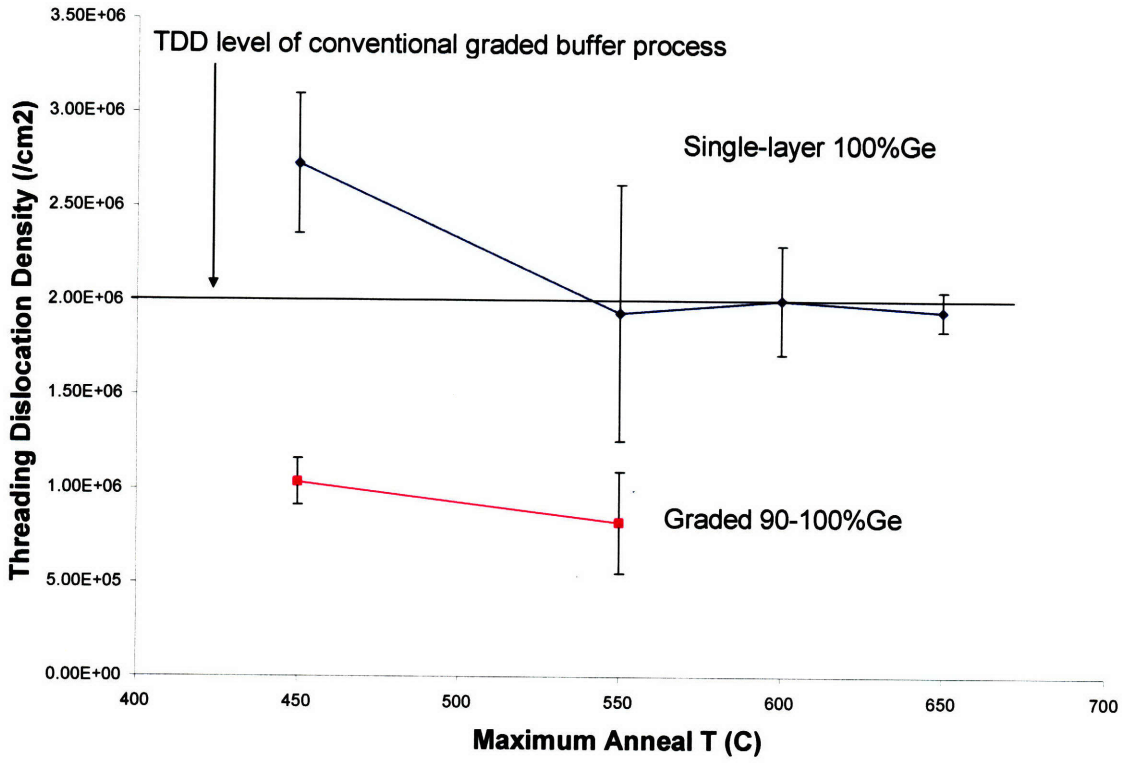


Figure 5.18 – Plot of TDD versus maximum annealing temperature for x_{Ge} = 90-100% TRUT samples. The graded 90-100% sample showed significant improvement over the single-layer sample and over the conventional graded buffer.

These results indicate that the use of smaller grading increments results in a lower TDD when other variables are held constant. Again, this is most likely attributable to the increased amount of interaction among misfit dislocations required for relaxation at

interfaces with higher mismatch. This experiment also shows that the use of lower growth temperatures in the 90-100%Ge region produces graded buffers with a lower final TDD value. Again, as suggested by Isaacson [61], this is most likely due to the loss of solid-solution strengthening as the $Si_{1-x}Ge_x$ alloy composition approaches pure Ge. By combining the samples from this experiment with samples reported by Isaacson as well as conventional graded buffer samples, one can make a plot of TDD versus growth temperature used for the final Ge layer, as shown in Figure 5.19. This figure shows a clear monotonic decrease in TDD as the growth temperature of the x_{Ge} = 90-100% layers is decreased. This trend suggests that solid solution hardening changes the balance between threading dislocation glide and nucleation, driving the steady-state threading dislocation density higher. Because the solid solution strengthening is more pronounced at higher temperatures, the steady-state TDD increases as the growth temperature increases.

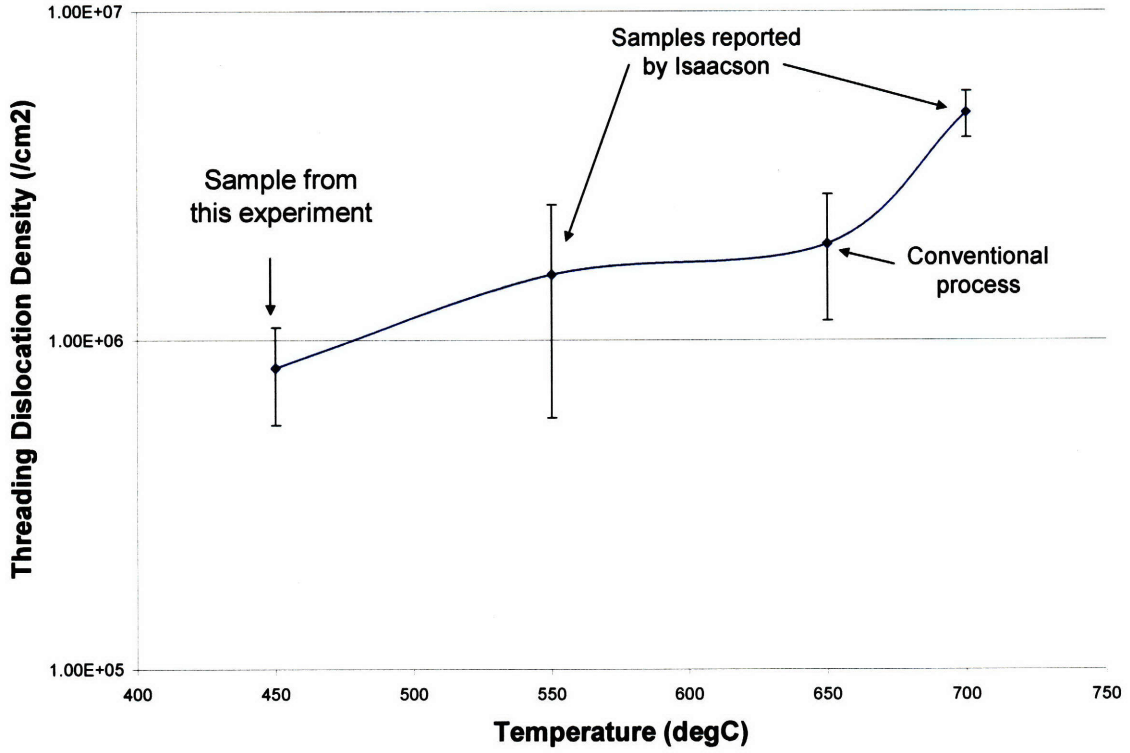


Figure 5.19 – Plot of TDD versus growth temperature for $Si_{1-x}Ge_x$ compositionally graded buffers capped with pure Ge. The 550 and 700°C samples were prepared by Isaacson [61], while the 650°C sample corresponds to a conventional graded buffer. The 450°C sample corresponds to the x_{Ge} = 90-100% graded TRUT sample of this work.

Thus, one can now plot this result in comparison to the plot of TDD versus x_{Ge} shown in Figure 5.16. The revised version of this plot is shown in Figure 5.20. While the result in the previous experiment is a 59% decrease in TDD over the conventional graded buffer process, it is still slightly higher than the TDD values measured at x_{Ge} = 70% , suggesting that there is still room for improvement. However, the growth temperature of 450°C used in this experiment is the lowest practical temperature available using UHVCVD, and thus other techniques (such as molecular beam epitaxy) would be required to grow x_{Ge} = 90 – 100% layers at a lower growth temperature.

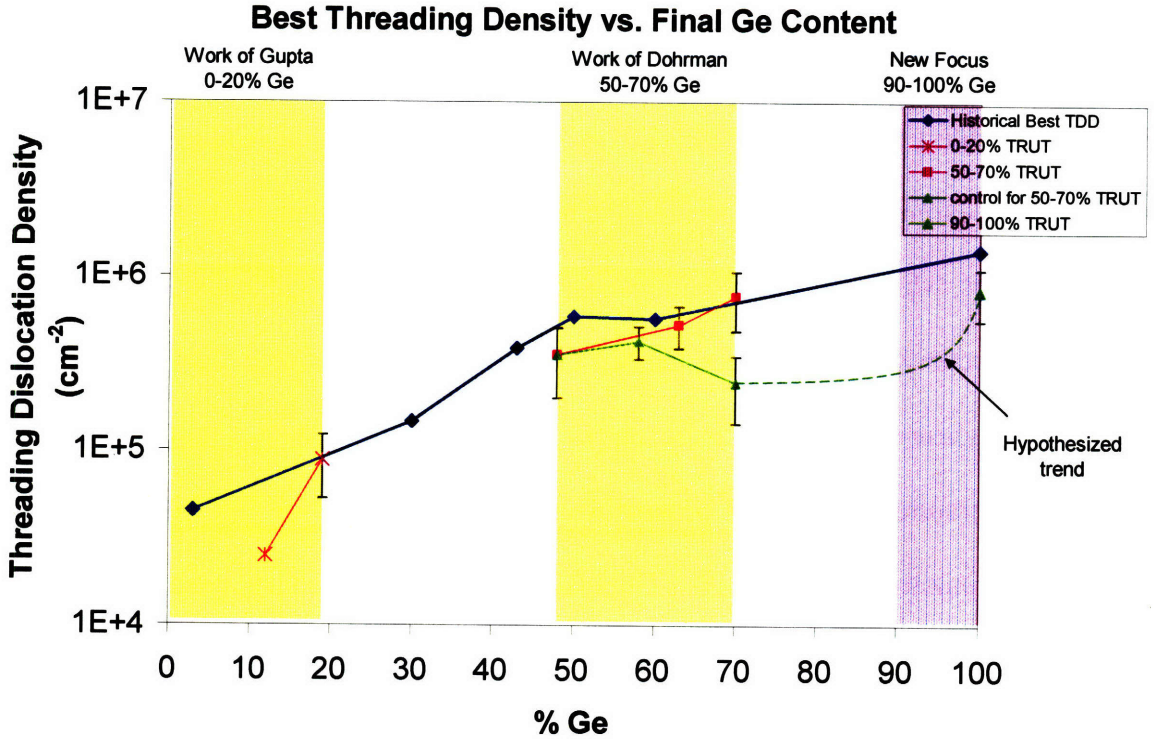


Figure 5.20 – Plot of TDD versus Ge fraction of various $Si_{1-x}Ge_x$ compositionally graded buffers. This is the same plot as Figure 5.16 but updated to show the graded x_{Ge} = 90-100% TRUT sample at x_{Ge} = 100%.

5.8 Summary

In this work, we have extended the work of Gupta [14] to investigate whether the use of low temperature growth and post-growth annealing in a repeated process (known as the TRUT process) can reduce the threading dislocation density, thickness, and surface roughness of compositionally graded buffers. For single-layer TRUT structures of x_{Ge} = 58% on x_{Ge} = 46% virtual substrates, it was found that post-growth annealing could not fully relax the layers, and the addition of strain-relieving layers (both low and high temperature) either roughened the surface severely or left built-in strain in the structure which could lead to cracking if used in multiple stages of a TRUT process. TRUT structures with compositional grading achieved more complete relaxation with no increase in TDD and without surface roughening; however, the growth of two-stage

TRUT structures based on this procedure resulted in an increase in TDD as well as the appearance of surface defects in the epitaxial layers as viewed in xTEM. These surface defects, which are suspected to be caused by a catastrophic strain-driven surface nucleation phenomenon, appear to limit the maximum strain rate possible for $Si_{1-x}Ge_x$ graded buffers, which is especially problematic for two-stage TRUT structures.

To circumvent these issues, the $Si_{1-x}Ge_x$ alloy range of interest was changed to x_{Ge} = 90-100%, where the results of Isaacson [61] and Yonenaga [60]suggested that the low growth temperature of the TRUT process would be beneficial. This was validated through the demonstration of a 100% Ge relaxed layer on a x_{Ge} = 90% virtual substrate with a TDD of 8.22±2.7 x10^5 cm^{-2}, a 59% decrease over the accepted values for conventional $Si_{1-x}Ge_x$ compositionally graded buffers. This work suggests that careful optimization of graded layer-like processes can minimize layer thicknesses and achieve threading dislocation densities in the 10^5 cm^{-2} range for any $Si_{1-x}Ge_x$ alloy composition on Si substrates.

Chapter 6: High-Quality Epitaxial Growth of $GaAs_yP_{1-y}$ Alloys on $Si_{1-x}Ge_x$ Virtual Substrates

6.1 Introduction

The work of Chapter 5 demonstrated a significant improvement in TDD over the previously accepted minimum for Ge virtual substrates. However, as discussed in that chapter, there is still a substantial increase in TDD as the Ge content of the $Si_{1-x}Ge_x$ graded buffer increases from x_{Ge} = 70% to x_{Ge} = 100%. The reduction in temperature for the x_{Ge} = 90-100% growth cannot be reduced any further using the epitaxial growth equipment available, but it is still desired to find improved processes to eliminate the TDD increase observed over this composition range.

Figure 6.1 is a modified version of the plot of TDD versus Ge content used in Chapter 5. This figure shows a plot of threading dislocation density versus lattice parameter for compositionally graded buffers on three different semiconductor alloy/substrate combinations. The TDD values for $Si_{1-x}Ge_x$ graded buffers in this figure reflect the new best minimum for x_{Ge} = 100% established in work described in this thesis. However, there are other compositionally graded buffer material systems that overlap the $Si_{1-x}Ge_x$ materials system over this range of lattice parameter. Mori [62] has demonstrated remarkably low TDD levels ($<10^4$ cm^{-2}) for tensile-graded $GaAs_yP_{1-y}$ buffers on GaAs substrates over the same lattice parameter range in which TDD is shown to escalate in $Si_{1-x}Ge_x$ graded buffers. Mori has also reported TDD values for compressively-graded $GaAs_yP_{1-y}$ buffers that are superior to the TDD of $Si_{1-x}Ge_x$ graded buffers with corresponding lattice parameter. These data are also shown in Figure 6.1.

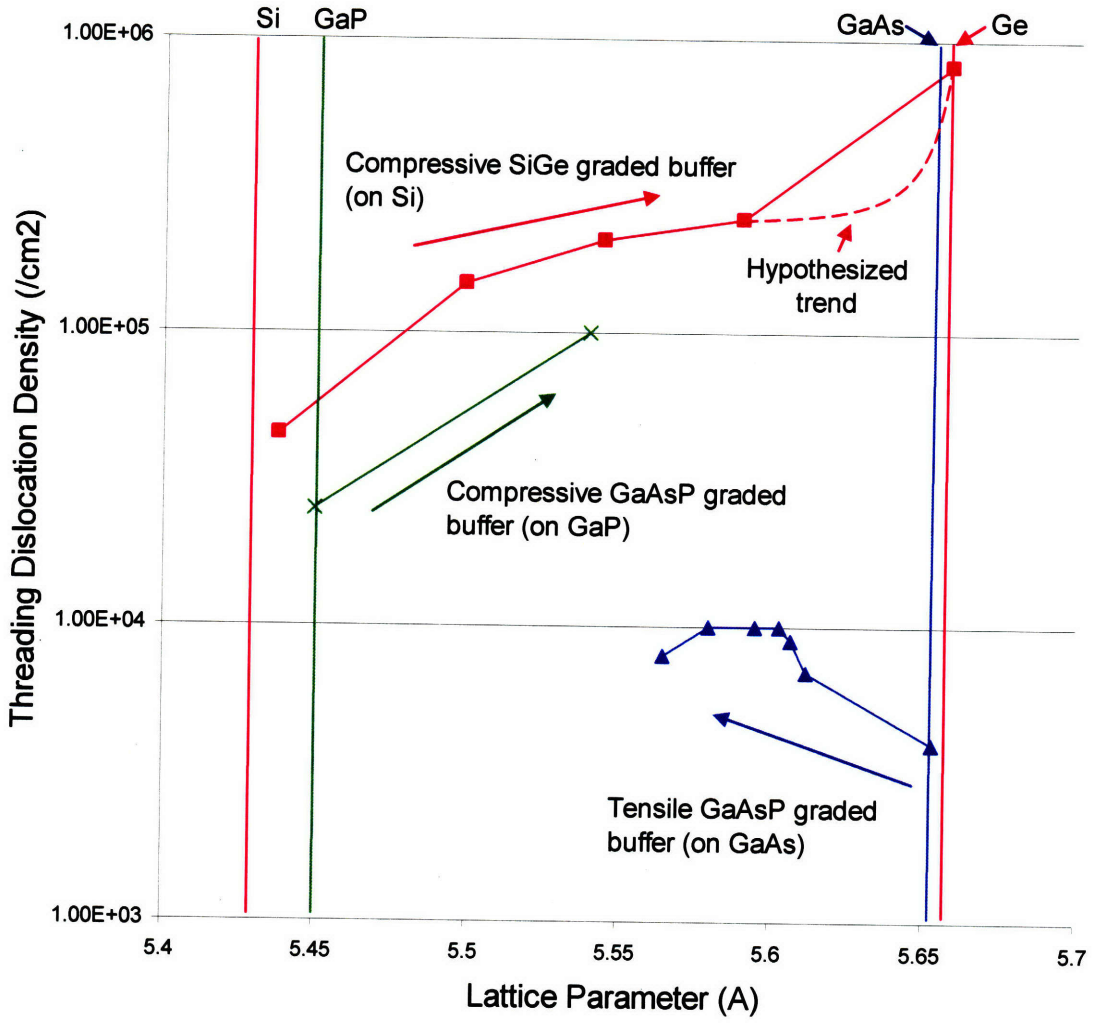


Figure 6.1 – Plot of threading dislocation density versus lattice parameter for compositionally graded buffers using three different semiconductor alloy/substrate combinations: $Si_{1-x}Ge_x$ on Si (compressive grading), $GaAs_yP_{1-y}$ on GaAs (tensile grading), and $GaAs_yP_{1-y}$ on GaP (compressive grading). Both types of $GaAs_yP_{1-y}$ buffers show superior TDD values as compared to $Si_{1-x}Ge_x$ buffers at corresponding lattice parameter, thus suggesting that they may be beneficial for growth of GaAs on Si.

Given the superior TDD results for $GaAs_yP_{1-y}$ graded buffers, one is inclined to consider whether $GaAs_yP_{1-y}$ graded buffers could be substituted for portions of the $Si_{1-x}Ge_x$ graded buffer to produce GaAs on Si with lower TDD. One can envision a process in which a $Si_{1-x}Ge_x$ graded buffer is grown on a Si wafer to extend the lattice parameter part of the way to GaAs, at which point a lattice-matched $GaAs_yP_{1-y}$ is grown on the $Si_{1-x}Ge_x$ surface, followed by compressive grading of the $GaAs_yP_{1-y}$ until GaAs is reached.

This would be particularly useful to bypass the large jump in TDD experienced in $Si_{1-x}Ge_x$ graded buffers from x_{Ge} = 70% to pure Ge that is caused by loss of solid-solution strengthening. In order to accomplish this, a process for heteroepitaxial growth of lattice-matched $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ graded buffers must be developed. That is the aim of the present study.

In addition to the goal of an improved GaAs on Si process, a process for lattice-matched $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$ would also be very useful as a means for growing device-quality $GaAs_yP_{1-y}$ on Si substrates. This could serve as platform for fabrication of InGaAsP LEDs with novel emitting wavelengths, as discussed by Mori [62].

In this work, the issues and challenges of epitaxial growth of lattice-matched $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ are investigated, and a process for high-quality $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ is developed. In order to understand the challenges involved in this study, we review the growth behavior of two heteroepitaxial "end-point" materials systems: GaAs on Ge and GaP on Si.

6.2 Epitaxial Growth of GaP on Si and GaAs on Ge

The heteroepitaxial growth systems of GaAs on Ge substrates and GaP on Si substrates have several obvious similarities. Both can be categorized as the growth of a polar III-V semiconductor on a nonpolar Group IV substrate, and as can be seen in Figure 6.1, GaP and GaAs are closely lattice-matched to Si and Ge, respectively.

A major complication for both growth systems is the growth of a polar epitaxial layer on a nonpolar substrate. The zincblende crystal structure of the polar epitaxial layer possesses less symmetry than the diamond cubic substrate [63]. This reduced symmetry results in two different orientations in which the epitaxial layer can nucleate on the

substrate, and the presence of both orientations in an epitaxial layer results in the formation of anti-phase boundaries (APBs) where regions with different orientations intersect. These anti-phase boundaries consist of a high concentration of anti-bonding defects (i.e. in the case of GaAs, it results in the presence of Ga-Ga and As-As bonds) and are detrimental to material quality. The problem of APB formation is expected to be exacerbated by the presence of atomic steps on the Group IV surface. This problem was also faced in the direct growth (i.e. without a graded buffer) of GaAs on Si, which received much attention during the 1980s. As reviewed by Kroemer [64], APBs are prevalent in GaAs grown on nominally (100)-oriented Si substrates, but it was found that APBs could be effectively suppressed by using (100) wafers with intentional mis-orientation towards the nearest {111} plane. After a pre-growth anneal, Si surfaces with this orientation show a preference for formation of double steps instead of single steps, which do not result in the formation of an APB.

In the case of GaAs on Ge, Ting [39] showed that the use of offcut (100) substrates combined with the proper temperature sequence could produce high-quality GaAs on Ge virtual substrates using OMCVD. As mentioned in the introduction, numerous GaAs-based devices demonstrated on Ge virtual substrates, building on the work of Ting to initiate high-quality GaAs growth on the Ge virtual substrate.

However, while the problem of GaAs growth on Ge has been effectively solved, experiments in heteroepitaxial growth of GaP on Si have yielded very different results. Experimental studies of GaP on Si growth have reported that, unlike GaAs on Ge, this system tends to grow with a three-dimensional island morphology with a high density of microstructural defects, including threading dislocations and twins [65]. Various studies

[65-68] have reported progress in reducing the defect density; however, all studies that include cross-sectional TEM data still show the presence of defects penetrating through the GaP layer. Because of the small sample volume that is probed with cross-sectional TEM, the observation of defects with this technique is indicative of a very high defect density, thus making it unlikely that high-performance semiconductor devices could be fabricated with this material. Narayanan [65] has attributed the problem of three-dimensional growth to the fact that the GaP-Si interface is not charge neutral, causing a change in interfacial energy that favors three-dimensional growth. However, this fails to explain why the same phenomenon does not affect GaAs growth on Ge, which should also suffer from a surface that is not charge neutral. Thus, the difference in behavior between GaP growth on Si and GaAs on Ge is not fully understood.

In addition to studies of growth of GaAs on Ge and GaP on Si, McGill [69] has studied the growth of lattice-matched InGaP alloys on $Si_{1-x}Ge_x$ virtual substrates with x_{Ge} = 50% and 70% using OMVPE. McGill observed severe three-dimensional growth for this system under a variety of growth temperatures and surface cleaning techniques. In investigating this phenomenon, McGill observed roughening of the $Si_{1-x}Ge_x$ surface during exposure to the PH_3/H_2 growth environment used for growth of the InGaP layer and speculated that this was somehow the cause of or related to the three-dimensional growth morphology. If this is the case, then one would expect this effect to be less severe in $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ because of the lower phosphorus content of $GaAs_yP_{1-y}$ as compared to InGaP (and hence lower concentration of PH_3 required for growth).

Regardless of the causes for three dimensional growth, one must consider the behavior of all three growth systems above when trying to predict the growth behavior of

$GaAs_yP_{1-y}$ alloys on $Si_{1-x}Ge_x$. It stands to reason that the growth behavior of lattice-matched $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ will be some combination of the behavior of the GaAs-on-Ge and GaP-on-Si systems and will depend on the alloy composition chosen (i.e. a composition closer to GaAs on Ge should behave more like that system, and likewise for GaP on Si). One aim of this study is to investigate different alloy combinations to better understand the transition from GaAs-on-Ge behavior to GaP-on-Si behavior.

6.3 Experimental Procedures

Growth of the $Si_{1-x}Ge_x$ compositionally graded buffers was completed by UHVCVD using the procedure of Leitz [16]. For APB suppression, the Si substrates used were (001) oriented with 6° offcut towards the nearest {111} plane. Wafers were then transferred to a Thomas Swan close-coupled showerhead OMVPE reactor for growth of the lattice-matched $GaAs_yP_{1-y}$ layer. The procedure for $GaAs_yP_{1-y}$ growth is based on that of Mori for growth of $GaAs_yP_{1-y}$ compositionally graded buffers [62] and on the procedure of Ting [39] for GaAs on Ge growth . All growths in this study were completed at 100Torr using N_2 as a carrier gas with AsH_3, PH_3, and tri-methyl gallium (TMG) as the As, P, and Ga precursor gases, respectively.

Various pre-epitaxial surface treatments were employed, as discussed in later sections. After pre-epitaxial surface treatment, the samples were annealed in the reactor chamber at 850°C for 10min under an N_2 ambient before cooling to the growth temperature. After temperature stabilization, growth was initiated by switching on flow of Group V precursors (AsH_3 and PH_3) for 5sec, then adding flow of TMG to initiate layer growth. In each growth, a relatively high V/III ratio was used to grow a thin (<100nm) nucleation layer, after which the V/III ratio was reduced by approximately a

factor of two for the remainder of the layer growth so that a higher growth rate could be achieved. The V/III ratio used for $GaAs_yP_{1-y}$ initiation in this work ranged from 188 to 400, and variation of the V/III ratio within this range had no effect on the morphology of the resulting $GaAs_yP_{1-y}$ layer. Thicknesses of the $GaAs_yP_{1-y}$ layers ranged from 250nm to 1μm. After growth, the $GaAs_yP_{1-y}$ layer was capped with a very thin (30-60Å) strained GaAs layer so as to prevent post-growth surface roughening due to uncontrolled non-stoichiometric depletion of As and P species from the surface as the sample cools from the growth temperature to room temperature. Mori identified this roughening phenomenon and showed that the strained GaAs cap was an effective remedy [62]; thus, this practice was adopted in this study.

6.4 Direct $GaAs_yP_{1-y}$ Growth with wet pre-epitaxial clean

In this experiment set, lattice-matched $GaAs_yP_{1-y}$ layers were grown directly on $Si_{0.5}Ge_{0.5}$, $Si_{0.3}Ge_{0.7}$, and $Si_{0.2}Ge_{0.8}$ virtual substrate compositions; the corresponding lattice-matched $GaAs_yP_{1-y}$ compositions are y_{As} = 46%, 69%, and 80%, respectively. We chose $Si_{1-x}Ge_x$ compositions with Ge fraction greater than 0.5 because these were seen as more likely to exhibit GaAs-on-Ge growth behavior. The work of Ting [39], Groenert [70], and others have concluded that the high-quality growth of GaAs on Ge by OMCVD can only be achieved within certain growth temperature "windows", and thus growth temperature was also explored in this experiment series. Our adaptation of the GaAs on Ge procedure of Ting uses a growth temperature of 650°C and produces good results, so $GaAs_yP_{1-y}$ growth temperatures of 675, 725, and 775°C for this series. The temperatures were increased over the optimal GaAs on Ge temperature based on the hypothesis that the temperature window will move to higher temperatures due to the increased melting point

of the $GaAs_yP_{1-y}$ layers and $Si_{1-x}Ge_x$ virtual substrates as compared to GaAs and Ge, respectively.

All samples in this series were given a wet chemical pre-epitaxial clean immediately prior to growth of the $GaAs_yP_{1-y}$ layer. The $Si_{1-x}Ge_x$ graded buffers were cleaned using either a 10min piranha clean (3:1 H_2SO_4:H_2O_2) or a 30sec 3:1 H_2O_2:H_2O mixture to remove surface contaminants. After contaminant removal, all samples in this series were then cleaned in 10:1 H_2O:HF to remove native oxide and leave a hydrogen-passivated surface (we refer to this procedure as an "HF-last" clean). This cleaning procedure is based on pre-epitaxial substrate cleans successfully employed for Si and Ge substrates.

6.4.1 Analysis of non-planar regions of $GaAs_yP_{1-y}$ layers

The $GaAs_yP_{1-y}$ films grown on $Si_{0.5}Ge_{0.5}$ and $Si_{0.3}Ge_{0.7}$ virtual substrates in this experiment set exhibited a non-planar surface morphology over the entire sample area, while films grown on $Si_{0.2}Ge_{0.8}$ virtual substrates exhibited similar morphology over large portions of the sample surface. Table 6.1 shows the samples produced in this experiment set and lists the amount of planar area of each sample as determined by optical microscopy.

	Growth Temperatures		
	675°C	725°C	775°C
$Si_{0.5}Ge_{0.5}$	-	No planar area	-
$Si_{0.3}Ge_{0.7}$	No planar area	No planar area	No planar area
$Si_{0.2}Ge_{0.8}$	Area = 55%	-	Area = 3.7%

Table 6.1 – Listing of samples from direct $GaAs_yP_{1-y}$ growth experiment set. The column of each entry specifies the growth temperature of the sample, and the row of each entry specifies the Ge content of the $Si_{1-x}Ge_x$ virtual substrate of the sample. Each entry in the table gives the fraction of planar area of the sample.

Cross-sectional TEM of the non-planar regions clearly reveals a rough surface morphology and a high density of threading dislocations, stacking faults, and other

crystalline defects. Representative cross-sectional TEM images of the non-planar areas observed in this experiment set are shown in Figure 6.2. The $GaAs_yP_{1-y}$ layers shown in this figure were grown lattice-matched to $Si_{0.5}Ge_{0.5}$ and $Si_{0.3}Ge_{0.7}$ virtual substrates at the same growth temperature (725°C).

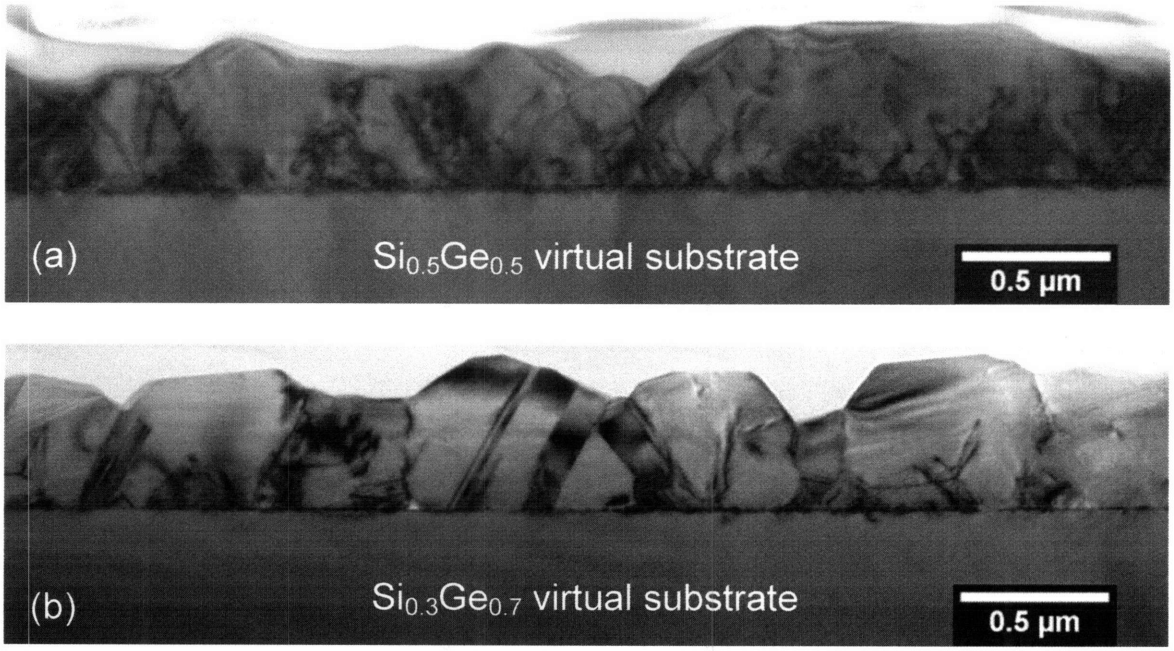


Figure 6.2 – Cross-sectional TEM of lattice-matched $GaAs_yP_{1-y}$ layers grown at 725°C on (a) $Si_{0.5}Ge_{0.5}$ virtual substrate and (b) $Si_{0.3}Ge_{0.7}$ virtual substrate. These images show the non-planar defect morphology and high concentration of stacking faults, threading dislocations, and other crystalline defects.

These images show a high density of threading dislocations, stacking faults, and other crystalline defects. High-resolution TEM images of the $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ interface in these samples are shown in Figure 6.3. These figures show twin boundaries originating at the interface as well as a white interface contrast in regions of the interface. These images and other HRTEM images from this series showed a loss of lattice resolution in the vicinity of the white interface contrast, suggesting that it may be amorphous; however, this interface contrast could not be further identified directly.

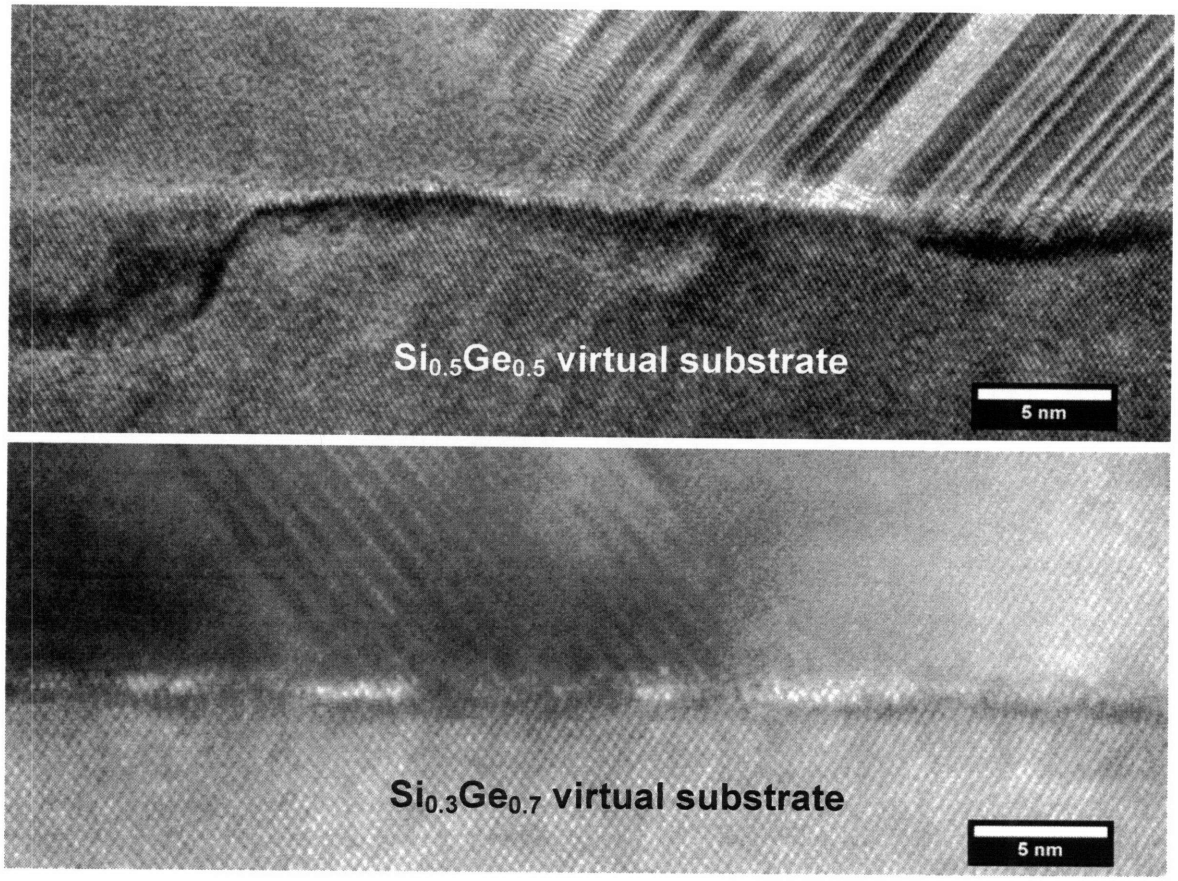


Figure 6.3 – High-resolution TEM images of $GaAs_yP_{1-y}$ /$Si_{1-x}Ge_x$ interface of samples shown in Figure 6.2: lattice-matched $GaAs_yP_{1-y}$ layers grown at 725°C on (a) $Si_{0.5}Ge_{0.5}$ virtual substrate and (b) $Si_{0.3}Ge_{0.7}$ virtual substrate. These images show stacking faults originating at the $GaAs_yP_{1-y}$/$Si_{1-x}Ge_x$ interface. Also shown is interfacial roughness, particularly for (a), and "white contrast" at the interface.

In addition to crystalline defects, the images in Figure 6.2 reveal a non-planar surface morphology with surface height variations that are a large fraction of film thickness. The morphologies of the two samples have some qualitative differences; Figure 6.2a has a relatively smooth morphology, while Figure 6.2b has a faceted morphology. The morphology is further revealed in the AFM images of Figure 6.4, showing the same two samples as Figure 6.2 and Figure 6.3. These xTEM and AFM results indicate that the lattice-matched $GaAs_yP_{1-y}$ on $Si_{0.5}Ge_{0.5}$ grows with a slightly different morphology than $GaAs_yP_{1-y}$ on $Si_{0.3}Ge_{0.7}$, with increased roughness and faceting.

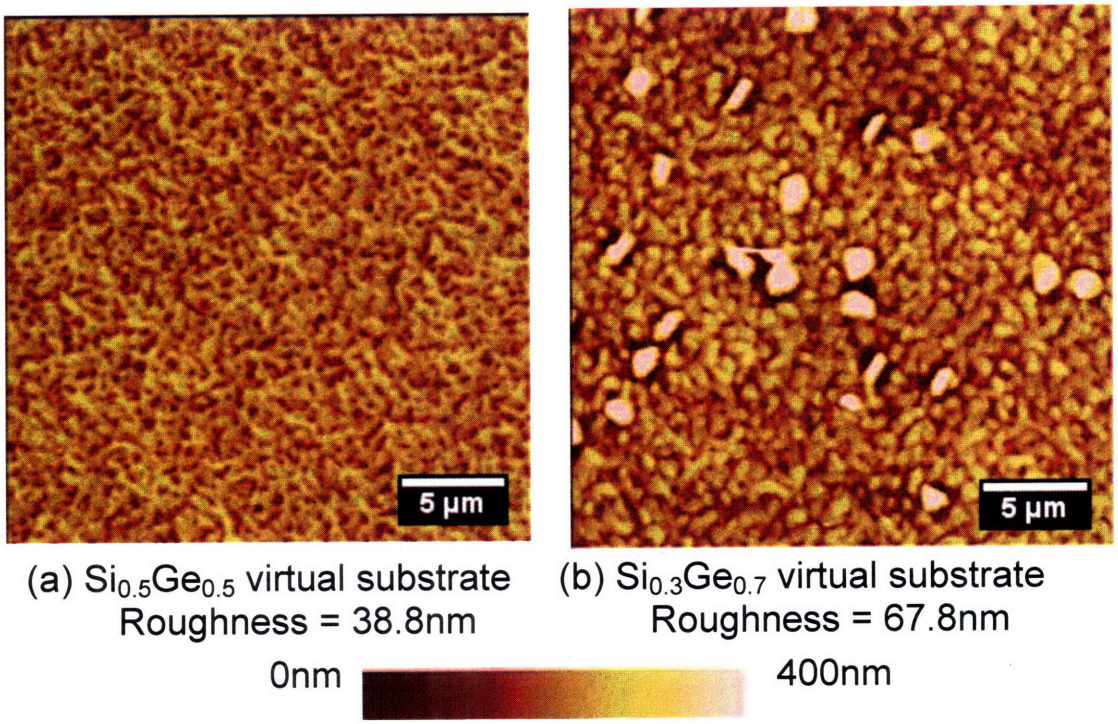
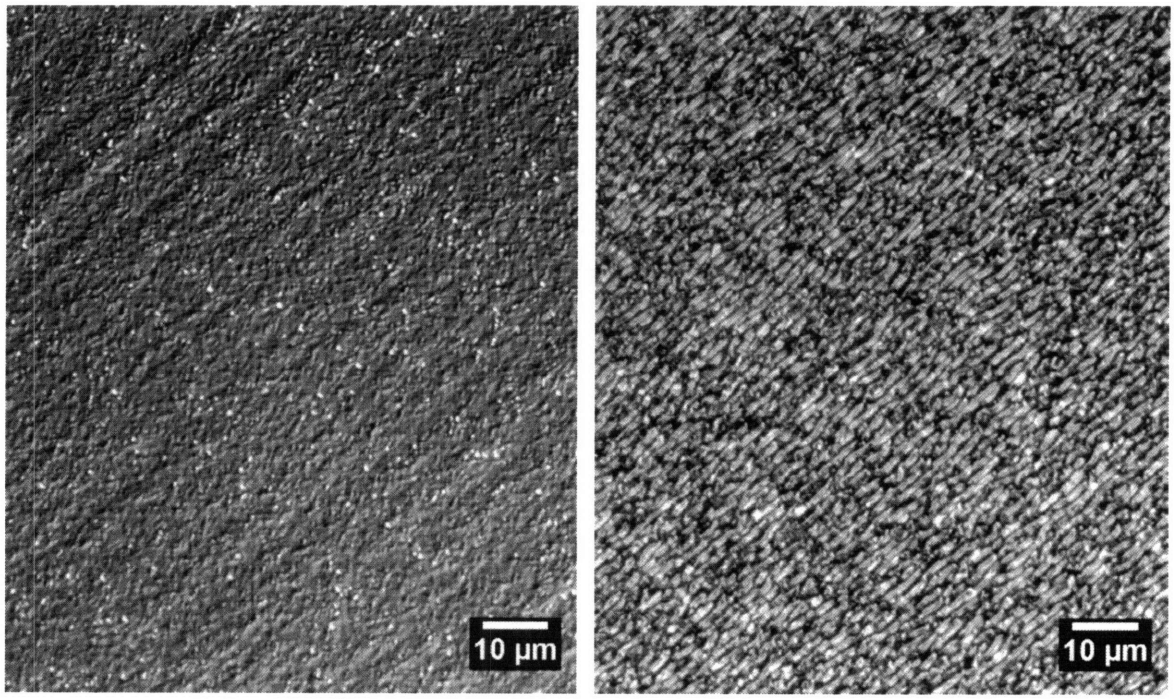


Figure 6.4 – AFM images of the samples from Figure 6.2, lattice-matched $GaAs_yP_{1-y}$ layers grown at 725°C on (a) $Si_{0.5}Ge_{0.5}$ virtual substrate and (b) $Si_{0.3}Ge_{0.7}$ virtual substrate, showing planar views of the surface morphology shown in Figure 6.2. Roughness values were calculated over the 25x25µm areas shown in the figure.

In addition to the effect of $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ composition, the non-planar surface morphology has some dependence on growth temperature. Figure 6.5 shows representative Nomarski images of the surface morphology observed in $GaAs_yP_{1-y}$ films grown on $Si_{0.3}Ge_{0.7}$ virtual substrates at 675 and 775°C. The morphology of Figure 6.5b (775°C) consists of an interconnected network of ridges and valleys, while the morphology of Figure 6.5a appears more granular and jagged.



(a) - 675°C
$GaAs_yP_{1-y}$ on $Si_{0.3}Ge_{0.7}$

(b) - 775°C
$GaAs_yP_{1-y}$ on $Si_{0.3}Ge_{0.7}$

Figure 6.5 – Nomarski microscopy images of non-planar surface of $GaAs_yP_{1-y}$ layers grown on $Si_{0.3}Ge_{0.7}$ virtual substrates at (a) 675°C and (b) 775°C.

The samples in this series were also characterized by x-ray diffraction (XRD) to measure the degree of lattice-matching of the $GaAs_yP_{1-y}$ layer to the $Si_{1-x}Ge_x$ virtual substrate. The range of temperatures and $GaAs_yP_{1-y}$ compositions used in this series exceeded the $GaAs_yP_{1-y}$ calibration data available for our OMCVD system, and thus lattice mismatch of up to 1% was produced in the samples in this series. The lattice mismatch of all samples in this series is shown in Table 6.2. While this adds another variable to the experiment, no correlation between surface morphology and lattice-mismatch was observed in this series. One typically expects that lattice mismatch could have a negative effect on layer morphology due to the presence of strain, which can also nucleate dislocations. In this series, the sample with the largest planar area ($GaAs_yP_{1-y}$ growth on $Si_{0.2}Ge_{0.8}$ at 675°C) also has one of the largest mismatches of the samples in

this series (f = 0.69%). The work of Mori has indicated that $GaAs_yP_{1-y}$ can grow in a planar fashion at lattice-mismatch values of this magnitude [62], and so we expect that the lattice mismatch in this series had a negligible impact on surface morphology.

	675°C	725°C	775°C
$Si_{0.5}Ge_{0.5}$	-	No specular area f = -1.0%	-
$Si_{0.3}Ge_{0.7}$	No specular area f = 0.24%	No specular area f = -0.49%	No specular area f = -0.72%
$Si_{0.2}Ge_{0.8}$	Area = 55% f = 0.69%	-	Area = 3.7% f = -0.23%

Table 6.2 – Experimental data from direct $GaAs_yP_{1-y}$ growth experiment set. The column of each entry specifies the growth temperature of the sample, and the row of each entry specifies the Ge content of the $Si_{1-x}Ge_x$ virtual substrate of the sample. For each entry in the table, the top line gives the amount of specular area of the sample, and the bottom line gives the lattice-mismatch between the $GaAs_yP_{1-y}$ layer and the $Si_{1-x}Ge_x$ virtual substrate.

The variation in surface morphology over the sample area was generally arranged as a pattern of bands on the sample surface. Similar patterns of bands across the sample surface were reported by Ting in his study of GaAs growth on Ge virtual substrates [39]. Ting attributed this banded pattern to a temperature dependence of nucleation of the two different GaAs sublattice orientations on Ge. Ting found that a transition between the two orientations occurred in the 500-600°C temperature range; GaAs grown on Ge virtual substrates above or below this temperature range exhibited single-domain structure, while GaAs grown within this temperature range produced regions of both sublattice orientations arranged in bands on the sample. Ting showed that the each band had a different sublattice orientation and that boundary of each banded region experienced a high degree of anti-phase disorder. Ting attributed the shape of the banded pattern to a surface transition as the sample was cooled from its pre-growth anneal temperature to its growth temperature. Areas near the periphery of the sample cooled more quickly than regions in the interior, and Ting concludes that a kinetically-limited surface transition

occurred in which quickly-cooled areas were quenched into the surface state favoring one GaAs sublattice orientation, while the more slowly-cooled areas were able to transition to the surface state favoring the other sublattice orientation.

While the shape of the banded patterns in this series were similar to the band patterns reported by Ting, there are notable differences between the two. The bands in Ting's study were relatively small areas of non-planar area separating planar areas of the sample; the $GaAs_yP_{1-y}$ bands in this study separate non-planar regions from other non-planar regions (or non-planar regions from planar regions in the case of $GaAs_yP_{1-y}$ layers on $Si_{0.2}Ge_{0.8}$ virtual substrates). One can speculate that the non-planar regions of the $GaAs_yP_{1-y}$ growths could essentially be very wide regions of anti-phase disorder separating very narrow single-domain regions, essentially the inverse of the pattern observed by Ting. Indeed, closer inspection of the boundary regions between non-planar areas in the $GaAs_yP_{1-y}$ samples of this series revealed an improvement in surface roughness within a very narrow region, although these improved regions still were clearly non-planar as observed in Nomarski microscopy. In addition, the material defects that dominate the $GaAs_yP_{1-y}$ film morphology in this series are stacking faults and twins, not the anti-phase boundaries in the case of GaAs on Ge as reported by Ting. Thus, while the shape of the banded patterns of $GaAs_yP_{1-y}$ films in this series suggests that they may be caused by a similar phenomenon to that observed in GaAs on Ge, the very limited regions of planar areas and the different material defects observed in the $GaAs_yP_{1-y}$ samples of this series tend to suggest that the non-planar growth encountered in this series is due to another phenomenon.

While we have observed some trends for the surface morphology of the non-planar regions of samples from this experiment set, these trends are broad generalizations due to the variety of surface morphologies observed in the samples in this experiment set. Some samples exhibited one morphology in one region and a different morphology in another. The most dramatic example of this is the fact that the samples grown on $Si_{0.2}Ge_{0.8}$ virtual substrates had planar regions in addition to the non-planar regions discussed in this section. However, in all cases, the areas which were described as "non-planar" in this section are characterized by surface feature heights that are a large fraction (>10%) of the total $GaAs_yP_{1-y}$ film thickness and large densities of threading dislocations, stacking faults, and other crystalline defects, as well as white interface contrast, observable in xTEM.

The variety of morphologies and high defect density of the non-planar regions of these $GaAs_yP_{1-y}$ layers is generally similar to the various morphologies and high defect density for GaP growth on Si reported in the literature. These GaP on Si morphologies were observed in all lattice-matched $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ compositions fabricated in this series, with planar $GaAs_yP_{1-y}$ areas only occurring on samples using $Si_{1-x}Ge_x$ virtual substrates with the highest Ge content used in this series (x_{Ge} = 80%). In contrast, the GaAs on Ge control sample produced for this study exhibited a planar GaAs morphology across the entire substrate area. This result confirms the logical hypothesis that $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$ surfaces with higher Ge content yields behavior that more closely resembles GaAs growth on Ge. This suggests that the wet clean direct growth procedure used in this study quickly becomes ineffective for planar $GaAs_yP_{1-y}$ growth as the Ge

content of the $Si_{1-x}Ge_x$ surface decreases below 100%, instead switching to a non-planar growth mode resembling GaP growth on Si.

6.4.2 Analysis of planar regions of $GaAs_yP_{1-y}$ layers on $Si_{0.2}Ge_{0.8}$

The planar regions of the two samples grown on $Si_{0.2}Ge_{0.8}$ virtual substrates were also characterized. Nomarski and AFM images of planar regions from these two samples and a GaAs on Ge virtual substrate control sample are shown in Figure 6.6. The Nomarski image of the 775°C sample closely resembles that of the GaAs on Ge control sample, while the 675°C sample is noticeably much rougher. AFM images show that both $GaAs_yP_{1-y}$ samples have a higher RMS surface roughness than the GaAs on Ge control sample. The $GaAs_yP_{1-y}$ sample grown at 675°C contains pits with a diameter ranging from 200-500nm and depth of up to 50nm. While the $GaAs_yP_{1-y}$ growth at 775°C is still rougher than the GaAs on Ge control sample, the wavy morphology seen in the AFM image of the 775°C $GaAs_yP_{1-y}$ layer was reported by Mori as being characteristic of $GaAs_yP_{1-y}$ layers grown compressively on GaP substrates [62]. As shown in Table 6.2, the $GaAs_yP_{1-y}$ layer grown at 775°C was grown compressively with a mismatch of -0.23%. Thus, the morphology of the planar region of this sample is the same as would be expected for growth on a III-V substrate with similar lattice parameter to the $Si_{0.2}Ge_{0.8}$ virtual substrate.

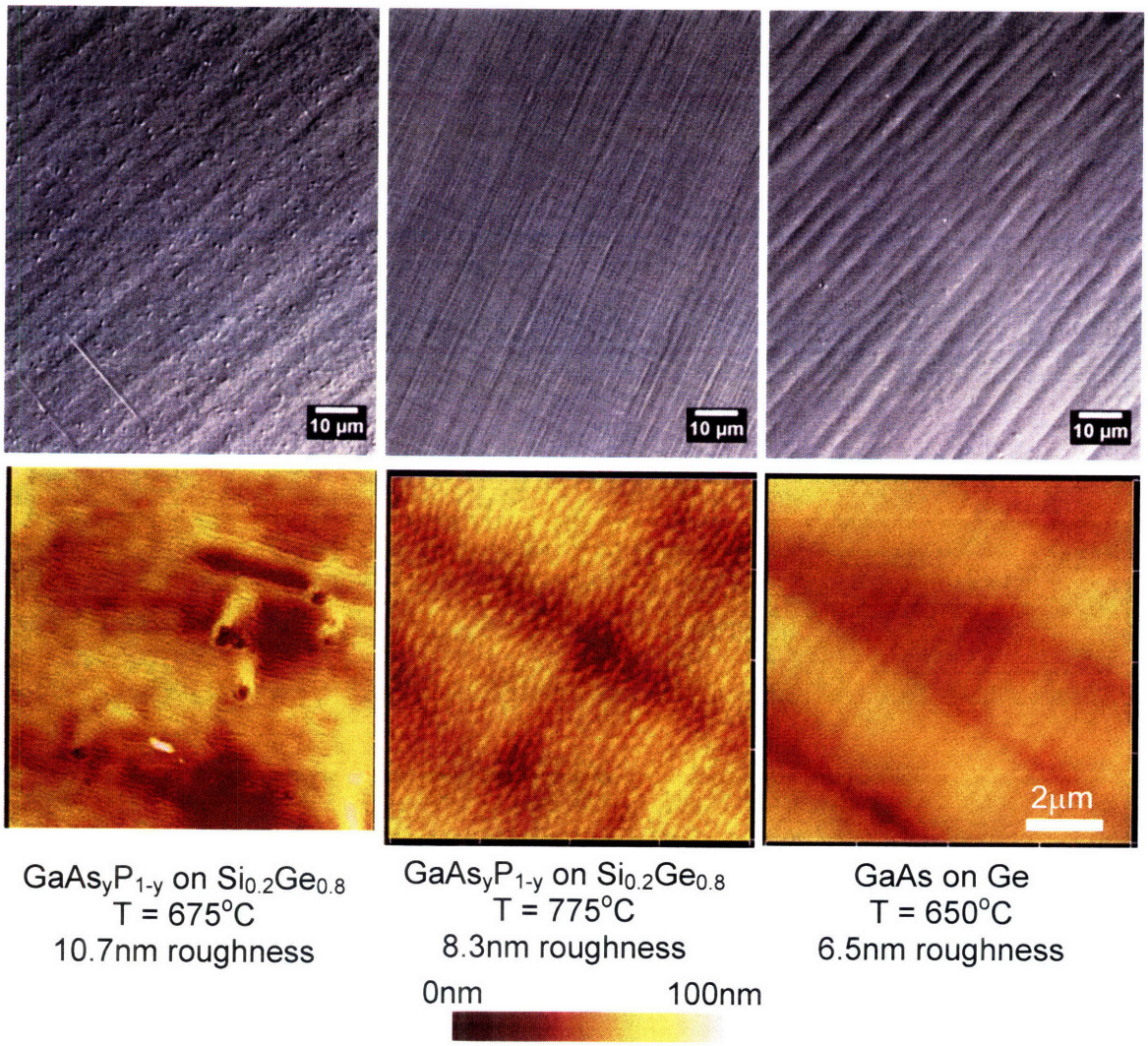


Figure 6.6 – Nomarski and 10x10µm AFM images of planar $GaAs_yP_{1-y}$ layers on $Si_{0.2}Ge_{0.8}$ virtual substrates grown at 675 and 775°C as well as GaAs on Ge control sample. The 775°C sample closely resembles the GaAs on Ge control sample, while the 675°C sample has additional surface features.

Surface morphology of the $GaAs_yP_{1-y}$ layer grown on $Si_{0.2}Ge_{0.8}$ at 675°C was also inspected using cross-sectional TEM as shown in a representative image in Figure 6.7. This image shows that the 675°C is very flat at the submicron size scale. However, this figure also shows the presence of stacking faults and threading dislocations, although at much lower densities than those in non-planar regions of the $GaAs_yP_{1-y}$ samples.

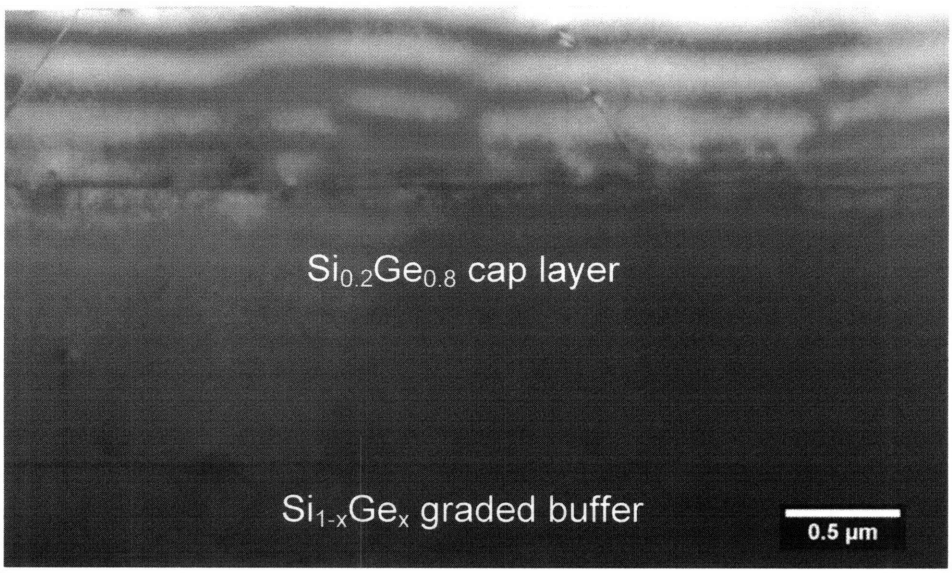


Figure 6.7 – Cross-sectional TEM of planar 1µm $GaAs_yP_{1-y}$ layer grown on $Si_{0.2}Ge_{0.8}$ virtual substrate at 675°C. Image shows a very flat film morphology. Defects similar to those seen in non-planar films can be seen, although at a much lower density.

Plan-view TEM was used to image the misfit dislocation network at the $GaAs_yP_{1-y}/Si_{0.2}Ge_{0.8}$ interface of the two planar $GaAs_yP_{1-y}$ on $Si_{0.2}Ge_{0.8}$ samples. Images of the misfit dislocation network of these samples are shown in Figure 6.8. The misfit network of the 675°C sample is denser than that of the 775°C sample owing to the higher $GaAs_yP_{1-y}/Si_{0.2}Ge_{0.8}$ lattice mismatch of the 675°C sample as compared to the 775°C sample. In addition to misfit dislocations, pvTEM revealed planar stacking faults throughout the 675°C sample at an areal density of approximately 8.3×10^6 cm^{-2}. No stacking faults were observed in the $GaAs_yP_{1-y}$ film grown at 775°C, which suggests a stacking fault density of less than 10^5 cm^{-2} based on the amount of sample area imaged. The smoother morphology and lower stacking fault density of the $GaAs_yP_{1-y}$ layer grown at 775°C makes it much more suitable for device applications than the material grown at 675°C.

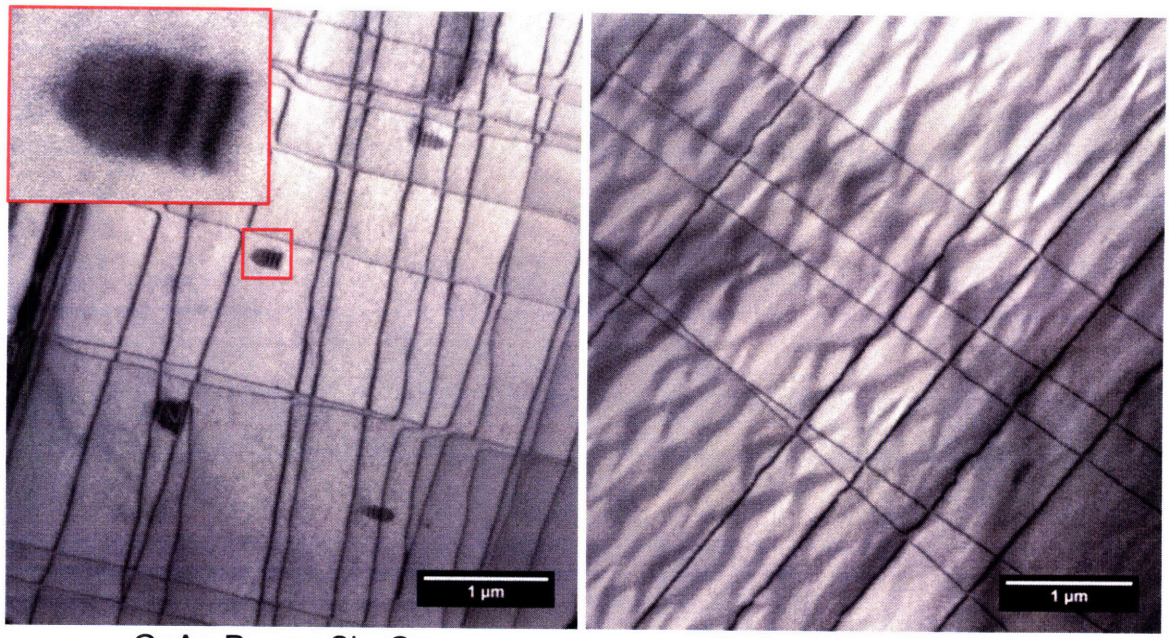


Figure 6.8 – Representative plan-view TEM images of planar regions of $GaAs_yP_{1-y}$ layers grown on $Si_{0.2}Ge_{0.8}$ virtual substrates.

The trends of smoother surface morphology and lower stacking fault density at increased growth temperature seen with $GaAs_yP_{1-y}$ films grown at 675 and 775°C mirror the findings of Groenert for GaAs growth on Ge virtual substrates [70]. Groenert showed that growth of GaAs on Ge at temperatures 50°C below the optimal temperature window produced GaAs layers with higher roughness and stacking fault density on the order of 10^7 cm^{-2}, while GaAs on Ge growth within the optimal temperature window produced smoother films with no observable stacking faults in pvTEM. The results of this study suggest that the lower bound of the optimal temperature window for $GaAs_yP_{1-y}$ growth on $Si_{0.2}Ge_{0.8}$ virtual substrates lies between 675 and 775°C, which is above the 650°C optimal temperature used for the GaAs on Ge control sample. This finding is consistent with our hypothesis that the optimal temperature window for $GaAs_yP_{1-y}$ growth on Si_{1-}

$_xGe_x$ is at higher temperature than that of GaAs growth on Ge due to the higher melting point of the $GaAs_yP_{1-y}$ and $Si_{1-x}Ge_x$ as compared to GaAs and Ge, respectively.

6.5 *Initiation Layer Series for $GaAs_yP_{1-y}$ growth on $Si_{0.3}Ge_{0.7}$ Virtual Substrate*

Results from the previous section indicate that initiation of a $GaAs_yP_{1-y}$ layer directly on a $Si_{1-x}Ge_x$ virtual substrate leads to formation of a non-planar surface morphology and a high density of crystalline defects over much or all of the sample area. $GaAs_yP_{1-y}$ layers grown in this manner would be unsuitable for device applications, and thus we consider alternative ways to improve $GaAs_yP_{1-y}$ quality on $Si_{1-x}Ge_x$ virtual substrates.

One potential solution is to replace the $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ growth interface with a series of growth interfaces which can be reliably controlled using established techniques to produce a high-quality $GaAs_yP_{1-y}$ nucleation layer. Insertion of thin Ge and GaAs layers at the growth interface would produce a structure in which each growth interface ($Si_{1-x}Ge_x$/Ge, Ge/GaAs, and GaAs/$GaAs_yP_{1-y}$) can be grown with high quality using established heteroepitaxial processes. However, because of the lattice mismatch of Ge and GaAs to the $Si_{1-x}Ge_x$ virtual substrate, these layers must be kept thin in order to avoid roughening or dislocation nucleation at the Ge and GaAs layers.

In this experiment series, $GaAs_yP_{1-y}$ layers are grown on $Si_{0.3}Ge_{0.7}$ virtual substrates using GaAs and Ge initiation layers in an effort to improve the nucleation of $GaAs_yP_{1-y}$ on the $Si_{0.3}Ge_{0.7}$ virtual substrate. The initiation layers in this series were kept below 60Å, which is below the critical thickness for Ge and GaAs on the $Si_{0.3}Ge_{0.7}$ virtual substrate. GaAs initiation layers were grown with the same V/III ratio used for initiation of high-quality GaAs growth on Ge in the control sample (V/III = 188), while the V/III

ratio used for $GaAs_yP_{1-y}$ growth was reduced to 100 for higher growth rate after growth of a nucleation layer. All $GaAs_yP_{1-y}$ layers in this series were grown at 725°C, while initiation layers were grown at various temperatures described below. $Si_{0.3}Ge_{0.7}$ virtual substrates were cleaned before $GaAs_yP_{1-y}$ growth using either an HF-based clean or a UHV anneal at 750°C for 30min. Descriptions of the samples in this growth series are given in Table 6.3.

Initiation Layer Samples	Pre-epitaxial Clean(s) of $Si_{0.3}Ge_{0.7}$ surface	Lattice Mismatch
30Å GaAs initiation layer 725 °C, $GaAs_yP_{1-y}$ 725 °C	UHV desorb, no clean	-0.58%
60Å GaAs initiation layer 725 °C, $GaAs_yP_{1-y}$ 725 °C	UHV desorb	~0%
60Å GaAs initiation layer 650°C, $GaAs_yP_{1-y}$ 725 °C	UHV desorb	-0.43%
30Å Ge initiation layer 350 °C, 60Å GaAs 650 °C, $GaAs_yP_{1-y}$ 725 °C	HF-based wet clean, w/ and w/o UHV desorb	-0.24%

Table 6.3 – Summary of experimental conditions of samples in initiation layer series. All samples in this series were grown at 725°C. UHV desorb indicates annealing at 750°C for 30min in a UHV environment immediately before $GaAs_yP_{1-y}$ growth. The far right column lists lattice mismatch of $GaAs_yP_{1-y}$ layer to underlying $Si_{0.3}Ge_{0.7}$ virtual substrate as measured by XRD.

All growths in this series resulted in non-planar $GaAs_yP_{1-y}$ layers across the entire sample area. All samples had essentially the same morphology and defect density when viewed in xTEM as non-planar $GaAs_yP_{1-y}$ layers from the direct $GaAs_yP_{1-y}$ growth series. A representative cross-sectional TEM image from this series is shown in Figure 6.9. The sample that included thin Ge and GaAs initiation layers had no apparent differences in morphology or defect density when compared to the samples containing only a GaAs initiation layer or to samples from the direct growth series.

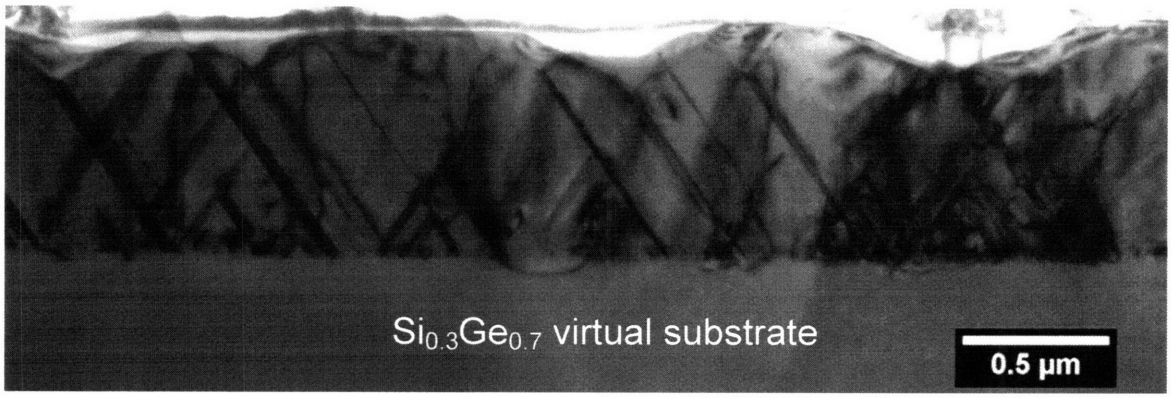


Figure 6.9 – Representative cross-sectional TEM image of sample from initiation layer series. This image was taken from sample consisting of 30Å Ge initiation layer at 350 °C, 60Å GaAs at 650 °C, $GaAs_yP_{1-y}$ at 725 °C.

High-resolution cross-sectional TEM was used to image the initiation layers of these samples; however, the initiation layers could not be located in any of the samples. The target thicknesses for initiation layers used in this series should have been sufficient to be viewed in HRTEM; however, they may have been obscured by the high defect density at the $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ interface. One possible explanation is that the actual layer thicknesses may have differed substantially from the target layer thicknesses. In working with strained $Si_{1-x}Ge_x$ heterostructures, Lee observed that the average growth rate of thin (< 100Å) strained $Si_{1-x}Ge_x$ layers differed substantially from the average growth rate of thick layers with all other system variables constant [71]. It is possible that a similar effect caused the strained Ge and GaAs initiation layers to be much thinner than their target thickness. A high density of white interface contrast was seen in these samples similar to the non-planar directly-grown $GaAs_yP_{1-y}$ layers; this white interface contrast again appeared to correlate with the initiation of twin boundaries at the interface. A representative HRTEM image of the $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ interface is shown in Figure 6.10.

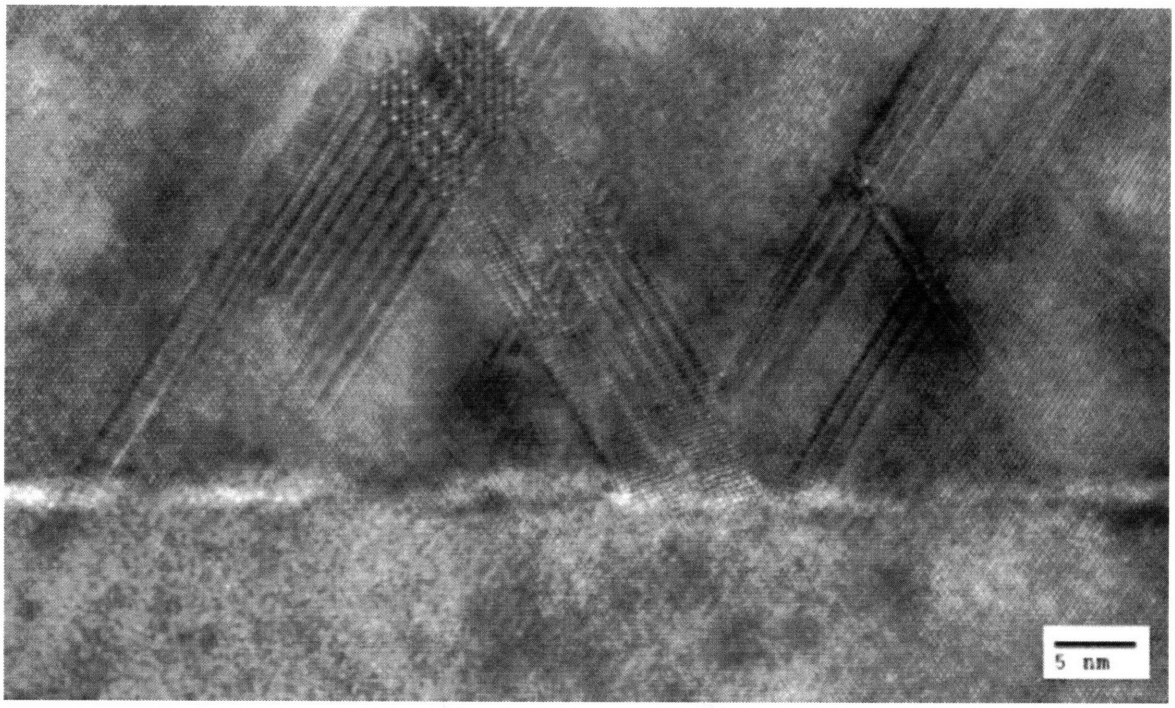


Figure 6.10 – Representative high-resolution cross-sectional TEM image of the interface between the $GaAs_yP_{1-y}$ layer and the $Si_{0.3}Ge_{0.7}$ virtual substrates for initiation layer samples. Initiation layers were not found in xTEM, but all samples contained white interface contrast similar to directly grown $GaAs_yP_{1-y}$ series.

The results from this series suggest that thin strained GaAs and Ge initiation layers used in this series have a negligible effect on surface morphology. If the initiation layers were somehow not deposited on the $Si_{0.3}Ge_{0.7}$ virtual substrate (perhaps due to growth rate reduction for thin strained layers), then the samples from this series would be expected to behave exactly like the directly-grown $GaAs_yP_{1-y}$ series. This is consistent with the results observed with this series. Compensating for this sort of growth rate reduction would require careful calibration of the strained layer growth rate as a function of thickness.

6.6 $GaAs_yP_{1-y}$ Growth on $Si_{0.3}Ge_{0.7}$ with Minimal Ambient Air Exposure

In this experiment series, the wet clean and UHV desorb surface treatments are replaced with direct transfer of the $Si_{1-x}Ge_x$ virtual substrate from the UHVCVD reactor

in which it is grown to the OMCVD reactor used for $GaAs_yP_{1-y}$ growth. The goal in this series was to investigate whether minimizing air exposure of the $Si_{0.3}Ge_{0.7}$ virtual substrate can improve the surface morphology and material quality of $GaAs_yP_{1-y}$ growth on $Si_{0.3}Ge_{0.7}$ virtual substrates. This experiment consisted of three samples. In the first sample (referred to as sample A), a $Si_{0.3}Ge_{0.7}$ virtual substrate is removed from the UHV environment of the UHVCVD, transferred in ambient air to the OMCVD, and then immediately loaded into the OMCVD for $GaAs_yP_{1-y}$ growth. This procedure exposed the $Si_{0.3}Ge_{0.7}$ virtual substrate to ambient air for approximately 5min.

For the second sample (referred to as sample B), we constructed an N_2-purged enclosure around the UHVCVD loadlock so that $Si_{0.3}Ge_{0.7}$ virtual substrates could be removed from this reactor with minimal air exposure. This enclosure only provides a modest degree of atmosphere control; however, the enclosure reduced the relative humidity in its interior from 50% (ambient laboratory air at time of experiment) to 25%. The $Si_{0.3}Ge_{0.7}$ virtual substrate was removed from the UHVCVD inside the enclosure and then placed inside a vacuum dessicator. The vacuum dessicator was evacuated using a mechanical pump, and samples were then immediately transferred to the OMCVD glovebox loading area to begin $GaAs_yP_{1-y}$ growth. The OMCVD glovebox is an N_2 environment with dew point of -60°C, so this procedure ensured that the $Si_{0.3}Ge_{0.7}$ virtual substrate was never exposed to ambient air during the transfer. However, it was exposed to some atmospheric contaminants inside the UHVCVD enclosure.

The UHVCVD/OMCVD transfer procedure for the third sample (referred to as sample C) was identical to that of sample B, but this sample was then stored inside the OMCVD glovebox for approximately 18 hours before growth of the $GaAs_yP_{1-y}$ layer.

The $GaAs_yP_{1-y}$ growth of sample B in this series resulted in a planar $GaAs_yP_{1-y}$ layer across 18% of the sample surface, while the $GaAs_yP_{1-y}$ layers of samples A and C were non-planar across the entire sample area. Representative Nomarski images of the samples are shown in Figure 6.11, with the image from sample B corresponding to the planar area. The non-planar regions of these samples appear generally similar in these images to the non-planar regions of the wet-cleaned direct $GaAs_yP_{1-y}$ growth series. However, sample B shows a clearly planar surface.

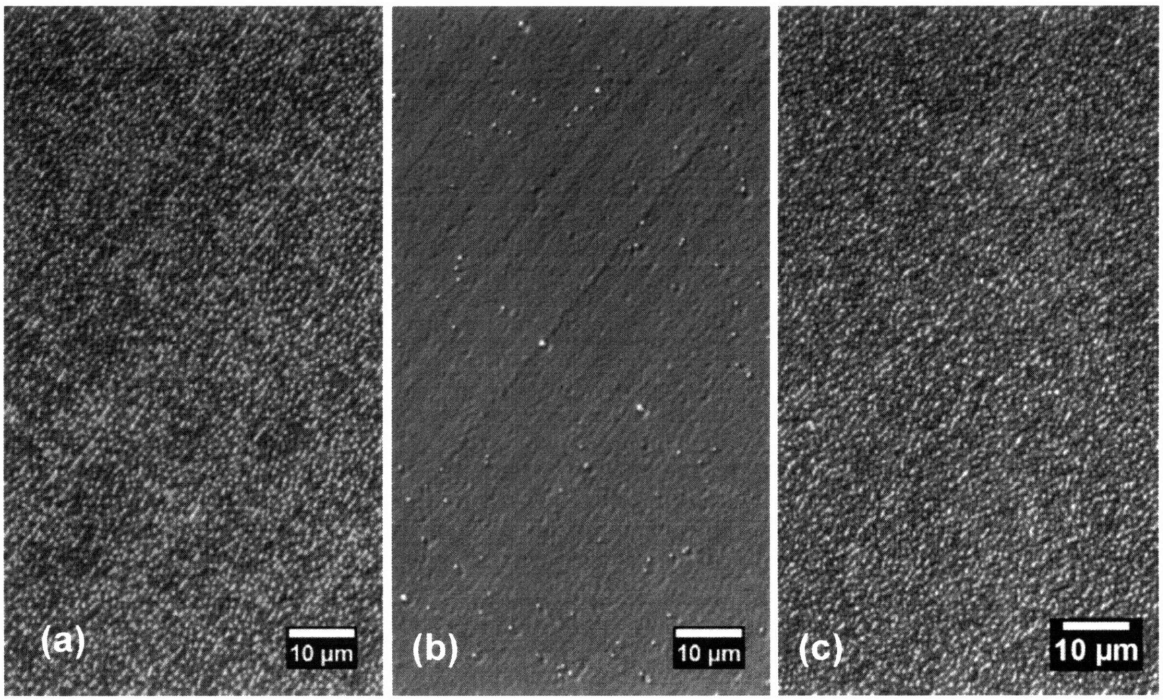


Figure 6.11 – Representative Nomarski images from samples A, B, and C from this series. The image of sample B was taken of the planar area of this sample.

Cross-sectional TEM images of the samples from this series are shown in Figure 6.12. This figure shows that the different samples each resulted in distinctly different morphologies. While Nomarski images of sample A show that it is clearly non-planar, the sample appears very different from the other non-planar samples in this study when viewed in cross-sectional TEM. The density of material defects in this sample is

dramatically reduced compared to other non-planar samples, with only isolated threading dislocations visible. The xTEM image of Sample B, taken from planar region of sample, shows very uniform 1μm $GaAs_yP_{1-y}$ layer with no threading dislocations, or stacking faults visible in this image. The morphology of sample C has the same characteristics of previous non-planar samples with large roughness and high defect density.

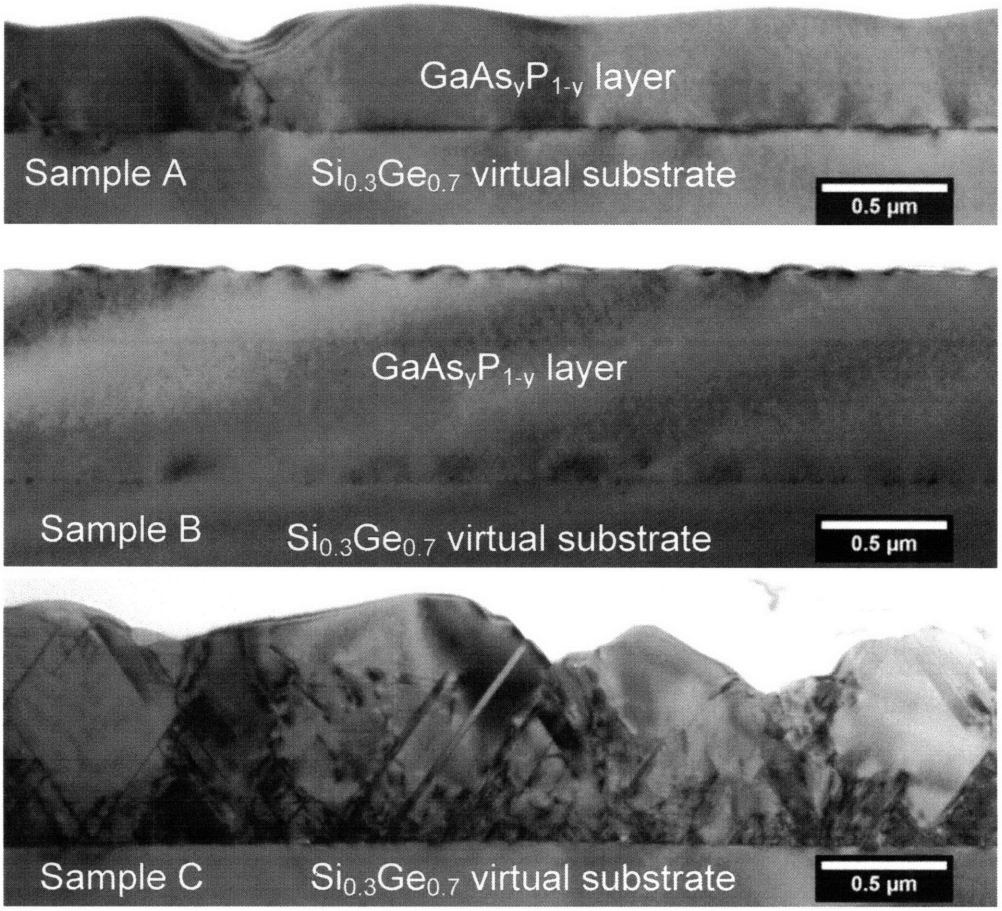


Figure 6.12 – Cross-sectional TEM images of samples from minimal air exposure series.

Greater detail of sample B is shown in Figure 6.13. The surface roughness shown in the top inset of this figure is characteristic of post-growth $GaAs_yP_{1-y}$ surface roughening as described in the Experimental Procedures section. The GaAs cap layer of this sample was too thin (~30Å) to prevent formation of this roughness. However, Mori has shown that this can be remedied through use of a thicker GaAs layer [62]. The

bottom inset of this figure shows that the $GaAs_yP_{1-y}/Si_{0.3}Ge_{0.7}$ interface of sample B shows no white interface contrast in high-resolution TEM.

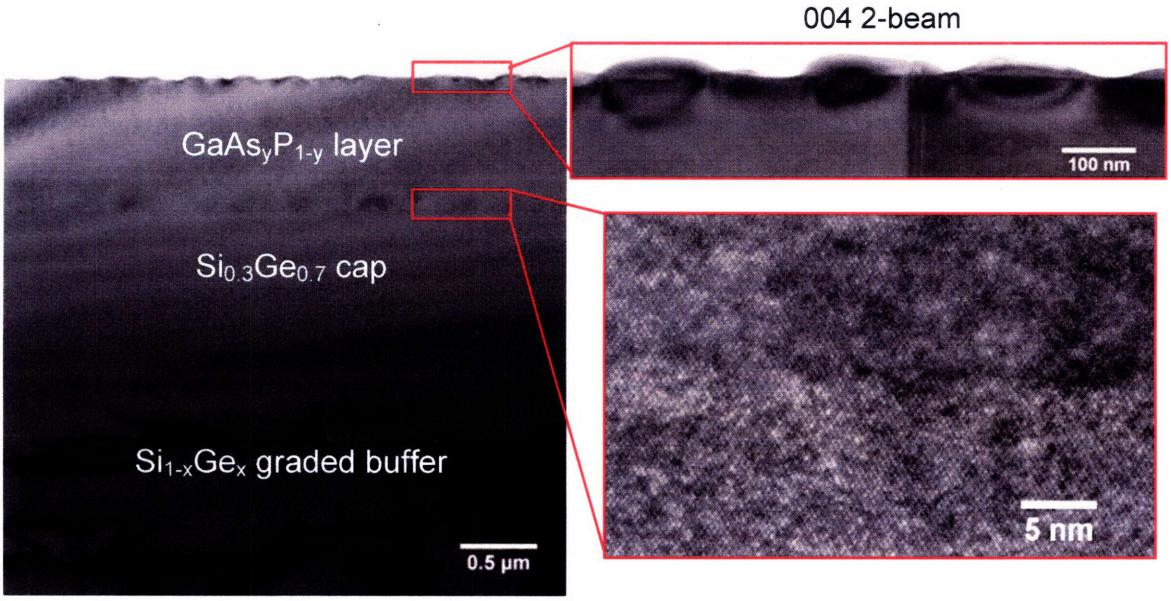


Figure 6.13 – xTEM of $GaAs_yP_{1-y}$ growth with minimal air exposure. Bottom inset shows a high-quality $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ interface with no white interface contrast. Top inset shows post-growth $GaAs_yP_{1-y}$ surface roughening.

In addition to the features shown in these images, xTEM of sample B also revealed the presence of submicron-sized cracks running through the $GaAs_yP_{1-y}$ layer. These cracks were observed with an average spacing of 6.5µm in these samples. Mori has reported cracks in $GaAs_yP_{1-y}$ tensile graded buffers with grading rates above a certain critical value, and he has attributed this to the buildup of tensile strain in the graded buffer[62]. These cracks could have been introduced by the TEM sample preparation process or during subsequent handling of the TEM specimen, as the thin TEM specimen can nucleate cracks more easily than films on bulk wafers. Regardless, XRD results revealed that the $GaAs_yP_{1-y}$ layer has a tensile misfit of 0.18% to the virtual substrate and that most of this misfit was not relaxed, leaving the film under tensile strain and

susceptible to crack formation. Better lattice-matching of the $GaAs_yP_{1-y}$ to the $Si_{0.3}Ge_{0.7}$ virtual substrate could be expected to prevent crack formation in the $GaAs_yP_{1-y}$ layers.

The results from this series show that exposure of the $Si_{0.3}Ge_{0.7}$ virtual substrate to atmospheric contaminants has a profound effect on the growth of lattice-matched $GaAs_yP_{1-y}$ layers. The sample with the least atmospheric exposure (sample B) clearly produced the best morphology, while limiting the ambient air exposure to 5min (sample A) still produced an improved morphology over samples grown on $Si_{0.3}Ge_{0.7}$ virtual substrates from the wet clean direct growth series and the initiation layer series. A typical non-planar morphology was seen in sample C, even though it only differed from sample B by an additional 18hr storage period of the $Si_{0.3}Ge_{0.7}$ under N_2 before $GaAs_yP_{1-y}$ growth. This indicates that the storage period had a considerable impact on the morphology of this sample.

6.7 Discussion

These results from the minimal air exposure series strongly suggest that atmospheric contaminants at the $Si_{1-x}Ge_x$ surface have a strong effect on the surface morphology of $GaAs_yP_{1-y}$ layers grown on $Si_{1-x}Ge_x$ virtual substrates. Further support of this argument is provided by profiles of impurity concentration versus depth obtained using secondary ion mass spectroscopy (SIMS) for $GaAs_yP_{1-y}$ layers grown on $Si_{0.3}Ge_{0.7}$ virtual substrates at 725°C using different pre-epitaxial surface treatments: a wet clean, a UHV desorb, and the procedure of sample A in this series. Carbon and oxygen profiles showing the effect of three different surface treatments are shown in Figure 6.14. Unfortunately, the high surface roughness of the films in this study had an extreme broadening effect on the SIMS profiles; however, despite this, the profiles of sample A

show a clearly lower oxygen content than the other samples by at least an order of magnitude and generally lower carbon content than these techniques (depending on interpretation of the artifact peak at the surface of the samples). In particular, the concentration of oxygen and carbon in sample A is lower at the $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ interface than the other two samples (the $GaAs_yP_{1-y}/Si_{1-x}Ge_x$ interface is interpreted to be the peak in impurity values near the end of the scan range). These results conclusively show the presence of lower atmospheric contaminant levels in sample A than in samples prepared using either a wet clean or UHV desorb.

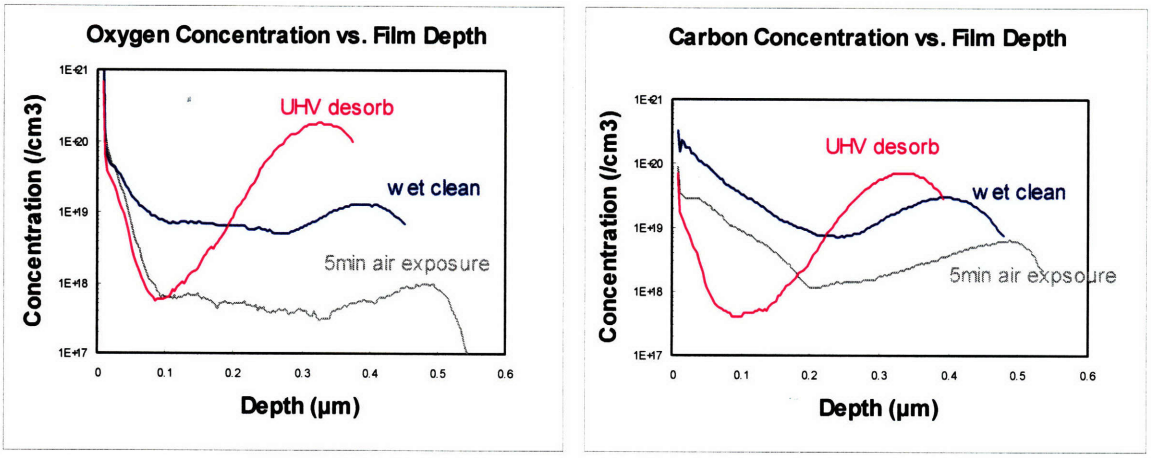


Figure 6.14 - Depth profiles of oxygen and carbon concentration in $GaAs_yP_{1-y}$ films on grown on $Si_{0.3}Ge_{0.7}$ at 725°C obtained using SIMS. The $GaAs_yP_{1-y}$ films were growth using three different pre-epitaxial surface treatments, as labeled in the figure.

A comparison of the results from the wet clean series and sample B from the minimal air exposure series is shown in Figure 6.15. This figure shows a plot of the fraction of planar $GaAs_yP_{1-y}$ area of each sample versus the Ge content of the $Si_{1-x}Ge_x$ virtual substrate used for the sample. In the wet clean series, planar areas were only achieved for growths using $Si_{1-x}Ge_x$ virtual substrates with $x_{Ge} = 0.8$. As stated previously, growths on $Si_{1-x}Ge_x$ virtual substrates with higher Ge content are expected to have better morphology due to their closer resemblance to growth of GaAs on Ge.

However, sample B of the minimal air exposure series produced planar area on a $Si_{0.3}Ge_{0.7}$ surface, which was not achieved using the wet clean procedure. Given that sample B showed a superior fraction of planar area to samples from the wet clean series, we expect that the procedure of sample B would produce greater planar area for $GaAs_yP_{1-y}$ grown on any $Si_{1-x}Ge_x$ composition employed in this study.

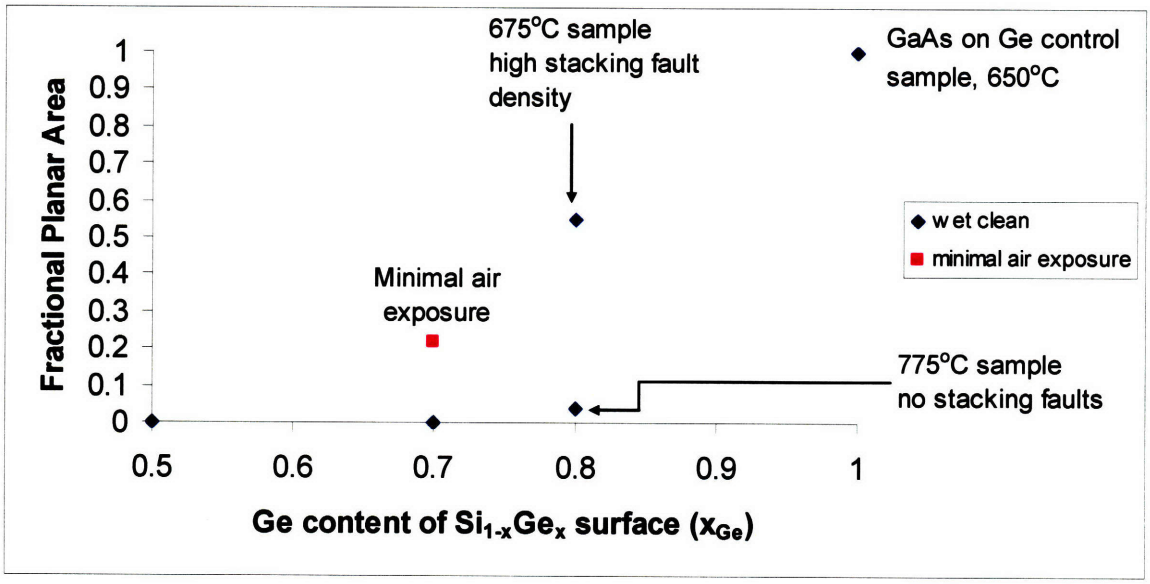


Figure 6.15 – Plot of fractional planar area versus Ge content of $Si_{1-x}Ge_x$ virtual substrate for $GaAs_yP_{1-y}$ layers produced in the wet clean series and minimal air exposure series.

Considering the clear role of surface contamination on the growth morphology of $GaAs_yP_{1-y}$ layers on $Si_{1-x}Ge_x$ surfaces, further improvement in surface morphology and fraction of planar area is expected from more rigorous reduction of contamination at the $Si_{1-x}Ge_x$ surface prior to $GaAs_yP_{1-y}$ growth. This can be achieved through growth of a homoepitaxial $Si_{1-x}Ge_x$ buffer layer on the $Si_{1-x}Ge_x$ virtual substrate in the OMCVD reactor in order to bury contamination introduced by transfer of the $Si_{1-x}Ge_x$ virtual substrates from the UHVCVD to the OMCVD. Surface contamination is expected to have a much lesser impact on a $Si_{1-x}Ge_x$ homoepitaxial interface than at a $Si_{1-x}Ge_x/GaAs_yP_{1-y}$ interface. Additionally, the problem of impurities can be completely

avoided through the growth of the $Si_{1-x}Ge_x$ virtual substrate and the $GaAs_yP_{1-y}$ layers all in a single epitaxial growth process in a single reactor, thus eliminating the need for transfer of the sample between systems. Work is currently underway to demonstrate both of these concepts.

The link between surface contamination and growth morphology of $GaAs_yP_{1-y}$ layers on $Si_{1-x}Ge_x$ established in this study also suggests that surface contamination may play a role in the epitaxial growth of lattice-matched $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$ alloys at other compositions, including GaP on Si. The typical morphology of GaP on Si is very similar to the non-planar $GaAs_yP_{1-y}$ layers in this study, which were improved through reduction of atmospheric contamination. Previous studies of GaP growth on Si have generally relied on a wet clean procedure such as an RCA clean to prepare the Si surface for GaP growth. However, this study showed that minimization of air exposure resulted in lower levels of surface contaminants, so a similar procedure may prove beneficial for GaP growth on Si. This could be achieved through growth of a Si buffer layer on the Si substrate to bury surface contamination before initiating GaP growth.

6.8 Summary

We have investigated methods for growth of device-quality lattice-matched $GaAs_yP_{1-y}$ on $Si_{0.5}Ge_{0.5}$, $Si_{0.3}Ge_{0.7}$, and $Si_{0.2}Ge_{0.8}$ virtual substrates. Direct growth of $GaAs_yP_{1-y}$ layers on $Si_{1-x}Ge_x$ virtual substrates cleaned with an HF-last cleaning procedure resulted in non-planar, high defect density material on all three $Si_{1-x}Ge_x$ compositions used in this study, with limited regions of planar growth only on $Si_{0.2}Ge_{0.8}$ virtual substrates. The morphology of these non-planar $GaAs_yP_{1-y}$ layers is characteristic of GaP growth on Si as reported in the literature. Inspection of the planar regions of

$GaAs_yP_{1-y}$ layers on $Si_{0.2}Ge_{0.8}$ virtual substrates showed that increasing the growth temperature from 675°C to 775°C improved surface roughness and decreased the occurrence of stacking faults. These findings mirror results for GaAs growth on Ge reported in the literature. In addition, we found that the minimum temperature for optimized growth of $GaAs_yP_{1-y}$ on $Si_{0.2}Ge_{0.8}$ is higher than that of GaAs growth on Ge, which is expected due to the higher melting points of $GaAs_yP_{1-y}$ and $Si_{1-x}Ge_x$.

Initiation layers and control of $Si_{1-x}Ge_x$ ambient air exposure were used in an effort to improve the non-planar morphology of growth on $Si_{0.3}Ge_{0.7}$ virtual substrates. The use of very thin strained Ge and GaAs initiation layers did not improve planar morphology of $GaAs_yP_{1-y}$ layers grown in this study. However, reduction of ambient air exposure of the $Si_{1-x}Ge_x$ virtual substrate prior to $GaAs_yP_{1-y}$ growth was seen to have a dramatic effect on layer morphology, enabling planar growth on $Si_{0.3}Ge_{0.7}$ virtual substrates. Results from SIMS confirmed a significant reduction of oxygen and carbon in samples $Si_{0.3}Ge_{0.7}$ virtual substrates grown using minimized air exposure compared to those grown using other pre-epitaxial surface treatments. We expect that the fraction of planar area on $Si_{0.3}Ge_{0.7}$ virtual substrates can be further improved through better reduction of atmospheric contaminant exposure, including the use of homoepitaxial buffer layers as well as growth of $Si_{1-x}Ge_x$ and $GaAs_yP_{1-y}$ in a single growth process using a single reactor. Additionally, we expect that these results for lattice-matched growth $GaAs_yP_{1-y}$ growth on $Si_{0.3}Ge_{0.7}$ virtual substrates can be applied to other compositions of $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$, including the growth of GaP on Si.

Chapter 7: Conclusion

7.1 Summary of Experimental Results

This thesis has explored three different ways to enhance the feasibility of monolithic III-V/CMOS integration. This work has made several advancements in this area that bring the goal of monolithic integration at a commercial level many steps closer to realization. A new substrate platform, the SOLES platform, was designed specifically for monolithic integration and fabricated using standard CMOS processing equipment. The feasibility of III-V device growth with SOLES was proven by demonstration of an AlInGaP LED on this platform.

The SOLES platform simplifies the processing of CMOS devices for monolithic integration and enables coplanar integration of III-V and CMOS devices but does not address the problems of TDD and graded layer thickness of the virtual substrate. To address this, a new $Si_{1-x}Ge_x$ graded buffer growth technique, the TRUT process, was tested as a way to improve the key metrics for $Si_{1-x}Ge_x$ virtual substrates. Use of more than one stage of the TRUT process resulted in an increase in TDD and the strain-driven nucleation of surface defects at a high density which makes multi-stage versions of the TRUT process unsuitable for device quality growth. However, this difficulty was alleviated by applying the TRUT process to the x_{Ge} = 90 - 100% composition range of the $Si_{1-x}Ge_x$ alloy system, where only one stage is required to reach x_{Ge} = 100% and where previous work had shown that the $Si_{1-x}Ge_x$ alloy experiences a loss of solid solution strengthening. Application of the TRUT process to this alloy range resulted in a 59% reduction in TDD for a fully relaxed Ge virtual substrate as compared to the accepted best reported TDD value for Ge virtual substrates.

While this improvement in TDD was significant, further improvement in TDD was desired. The TRUT process could not be further optimized in the x_{Ge} = 90-100% range, so alternative methods for TDD reduction were considered. Results from compositionally graded buffers using the $GaAs_yP_{1-y}$ alloy system on GaAs and GaP substrates had shown that it was capable of achieving much lower TDD values than those seen in the $Si_{1-x}Ge_x$ alloy system at the same values of lattice parameter. Thus, it was suggested that a combination of $Si_{1-x}Ge_x$ and $GaAs_yP_{1-y}$ compositionally graded buffers be used to create a platform for GaAs on Si. In order to achieve this goal, it was required to develop a process for lattice-matched growth of $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ virtual substrates. Various processes for lattice-matched $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$ virtual substrates were explored, using the process for high-quality GaAs growth on Ge as a starting point. These results showed that the growth process was highly dependent on Ge content of the $Si_{1-x}Ge_x$ virtual substrate, growth temperature, and surface treatment of the $Si_{1-x}Ge_x$ virtual substrate immediately before growth. $GaAs_yP_{1-y}$ material quality was generally found to be improved with increasing Ge content of the $Si_{1-x}Ge_x$ virtual substrate, increased growth temperature, and minimization of the air exposure of the $Si_{1-x}Ge_x$ virtual substrate prior to growth of the $GaAs_yP_{1-y}$ layer. Using these optimizations, specular $GaAs_yP_{1-y}$ layers with low surface roughness, no observed twin boundaries or stacking faults, and device-quality TDD levels were grown on both $Si_{0.2}Ge_{0.8}$ and $Si_{0.3}Ge_{0.7}$ virtual substrates, although the fraction of high-quality sample area remains as a challenge.

7.2 Suggestions for Future Work

Based on the results reported in this thesis, many suggestions for future work can be made. The successful fabrication of the SOLES platform makes possible many potential demonstrations of monolithic integration. The fabrication of AlInGaP LEDs on the SOLES platform established the feasibility of III-V device fabrication – a logical next step would be to fabricate CMOS devices in the Si layer as well. Once that is established, creation of a simple monolithic OEIC on the SOLES platform with interconnections between the Si and III-V device layers would be an exciting next step. A good potential choice for this would be an AlInGaP LED interconnected to a Si MOSFET which could be configured to control the LED. After demonstration of this, one can envision a number of increasingly complex OEICs that could be demonstrated on SOLES until the demonstration complexity reached the level of a modern CMOS IC.

Another idea for future work with SOLES is fabrication of SOLES by transferring a Si layer that has already undergone some amount of CMOS processing. This may bypass some of the thermal budget limitations of the SOLES platform by allowing high-temperature steps to be completed on the Si wafer before layer transfer. This could be considered to be a type of quasi-hybrid integration as described by Barkley [72]. Processing of the Si donor wafer may be limited by the fact that the donor wafer must maintain a high degree of flatness for wafer bonding; however, it may be possible to use a CMP layer on this wafer just as was done with the Ge virtual substrate to overcome this problem.

The work with $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$ suggests a wide variety of possible avenues for future work. One area of interest for future work would be to gain a better understanding of the effects of different pre-epitaxial surface treatments on the $Si_{1-x}Ge_x$

virtual substrate. A study of hydrogen passivation state of the $Si_{1-x}Ge_x$ surface as a function of time after various surface treatments, similar to the work of Rivillon for the Ge surface [73], could prove beneficial to developing an optimal cleaning procedure for $GaAs_yP_{1-y}$ growth on $Si_{1-x}Ge_x$. This may also help elucidate the origin of the large variation between specular and non-specular regions of $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ and, more importantly, suggest a way to eliminate it so that the entire area of the $GaAs_yP_{1-y}$ layer is uniformly specular.

Another way to deal with possible surface contamination would be to grow a homoepitaxial $Si_{1-x}Ge_x$ buffer layer on the $Si_{1-x}Ge_x$ virtual substrate before initiating $GaAs_yP_{1-y}$ growth. This homoepitaxial process would be expected to be much less sensitive to surface contamination and is a standard practice in the field of epitaxial growth. This was actually used for all $Si_{1-x}Ge_x$ samples produced for this work, but it is slightly more difficult because the Thomas Swan close-coupled showerhead reactor used for $GaAs_yP_{1-y}$ growth was designed for growth of III-V semiconductors in a Group III mass-transport limited growth regime, whereas growth of $Si_{1-x}Ge_x$ layers (which would grow in a different growth regime) is not proven. However, this issue is expected to be easily overcome through what would essentially be calibration growths of $Si_{1-x}Ge_x$ layers in this system.

If it proves possible to grow a $Si_{1-x}Ge_x$ buffer layer in the Thomas Swan reactor, then it may also be possible to grow the complete $Si_{1-x}Ge_x$ virtual substrate in this reactor, thus completely eliminating the need to transfer samples from one reactor to another in this process. This would completely eliminate concerns about native oxide and surface

cleanliness since the sample would remain inside the growth chamber until the structure is complete.

Since this work established that high-quality $GaAs_yP_{1-y}$ can be grown on $Si_{1-x}Ge_x$ virtual substrates, one obvious area for future work would be growth of a compressive $GaAs_yP_{1-y}$ graded buffer on a $Si_{1-x}Ge_x$ virtual substrate to achieve GaAs on Si. This was the original motivation for this project, and the demonstration of high-quality lattice-matched $GaAs_yP_{1-y}$ on $Si_{1-x}Ge_x$ virtual substrates opens the door for this process. It would be very interesting to compare the TDD of GaAs on Si grown using this process to GaAs on Si grown using $Si_{1-x}Ge_x$ virtual substrates graded to $x_{Ge} = 100\%$. Once GaAs on Si is established using a combined $Si_{1-x}Ge_x/GaAs_yP_{1-y}$ graded buffer, the next logical step would be demonstration of GaAs-based devices on this platform.

If $Si_{1-x}Ge_x/GaAs_yP_{1-y}$ graded buffers are demonstrated with lower TDD than GaAs on Ge virtual substrates, another interesting improvement that could be made with this system would be to use a $Si_{1-x}Ge_x/GaAs_yP_{1-y}$ graded buffer instead of a Ge virtual substrate for fabrication of SOLES wafers. This would make the growth of III-V materials on the SOLES platform easier by allowing the growth of a GaAs buffer layer on a GaAs surface, instead of requiring initiation of GaAs growth on a Ge surface. This could eliminate problems that might arise with anti-phase boundaries due to requirement of using a selective area epitaxy process for the GaAs growth [56]. This would also increase the thermal budget of the SOLES wafer since the melting point of GaAs and As-rich $GaAs_yP_{1-y}$ alloys is significantly higher than the melting point of Ge and Ge-rich $Si_{1-x}Ge_x$ alloys.

Another interesting application of the $GaAs_yP_{1-y}$ work in this thesis is the possibility of growing $GaAs_yP_{1-y}$ or $In_xGa_{1-x}P$ LEDs lattice-matched to the $Si_{1-x}Ge_x$ virtual substrate. $GaAs_yP_{1-y}$ or $In_xGa_{1-x}P$ LEDs with a composition range lattice-matched to the $Si_{1-x}Ge_x$ virtual substrates used in this work would have band gap wavelengths in the visible spectrum, including green light. There is currently not an available semiconductor substrate with lattice parameter in this range, which has prevented the development of semiconductor devices at this lattice parameter. The achievement of an LED that directly emits green light would be a significant accomplishment, since existing green LEDs produce green light via various indirect means. A direct-emission green LED could have major commercial implications, as the "green gap" is a major problem in the design of LED displays and projectors and white LED light sources for solid-state lighting. The fact that this process would produce these LEDs on an inexpensive Si wafer would only further improve the commercial significance of this technology. Thus, the growth of $GaAs_yP_{1-y}$ LEDs on Si could have even greater impact than the development of a $Si_{1-x}Ge_x/GaAs_yP_{1-y}$ graded buffer for GaAs on Si.

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