# Strained Ge channel *p*-type metal-oxide-semiconductor field-effect transistors grown on $Si_{1-x}Ge_x$/Si virtual substrates

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**Abstract**

We have fabricated strained Ge channel *p*-type metal-oxide-semiconductor field-effect transistors (*p*-MOSFETs) on $Si_{0.3}Ge_{0.7}$ virtual substrates. The poor interface between silicon dioxide ($SiO_2$) and the Ge channel was eliminated by capping the strained Ge layer with a relaxed, epitaxial silicon surface layer grown at 400ºC. Ge *p*-MOSFETs fabricated from this structure show a hole mobility enhancement of nearly 8 times that of co-processed bulk Si devices, and the Ge MOSFETs have a peak effective mobility of 1160 $cm^2$/V-s. These MOSFETs demonstrate the possibility of creating a surface channel enhancement mode MOSFET with buried channel-like transport characteristics.

***Keywords*** **–** strained-Ge, SiGe, germanium, MOSFET, mobility, strained-Si, pMOSFET

## I. Introduction

As device scaling reaches its outermost limits, control over carrier mobility by channel engineering has emerged as the final variable for dramatic improvements in the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs). Low defect density relaxed silicon germanium ($Si_{1-x}Ge_x$) alloys on silicon[1] have created a new platform for high mobility electronic devices as well as integration of optoelectronics on Si.[2,3] For example, strained silicon *n*-type MOSFETs (*n*-MOS) on relaxed $Si_{1-x}Ge_x$/Si virtual substrates exhibit electron mobility enhancements of 1.25 to 2 times that of bulk devices.[4] While strained Si hole channel devices also demonstrate mobility enhancements of 1.4 to 1.8,[5,6] just as in bulk Si, the *p*-type MOSFET's (*p*-MOS) mobility still lags the *n*-MOS considerably. Compressively strained $Si_{1-y}Ge_y$ channels on $Si_{1-x}Ge_x$ (y>x) have thus been used to attain even higher hole mobilities. Höck et al. recently reported a peak effective mobility of 760 $cm^2$/V-s for a *p*-MOS device using a strained $Si_{0.17}Ge_{0.83}$ channel on a $Si_{0.52}Ge_{0.48}$ buffer.[7] Numerous reports in the literature also describe the use of relaxed pure germanium as a MOSFET channel material. Effective mobilities as high as 1000 $cm^2$/V-s have been reported for *n* and *p*-type FETs fabricated on bulk Ge and utilizing germanium oxynitride as the gate material.[8] Another group attained a hole effective mobility of 430 $cm^2$/V-s for relaxed Ge deposited directly onto a Si substrate with no buffer layers and utilizing a silicon dioxide ($SiO_2$) gate.[9]

Although bulk Ge MOSFETs show the potential of Ge-based MOS technology, the most manufacturable and economical means of implementing a high mobility Ge channel would be to fabricate MOSFETs on a Ge-rich layer on top of a Si substrate. In addition, a slightly lower virtual substrate composition than pure Ge is desired, since the highest hole mobility can be realized with a compressively strained, pure germanium channel due to the lack of alloy scattering and reduction of intervalley scattering.[10] Room temperature Hall mobilities as high as 1300-1870 $cm^2$/V-s have been reported in strained Ge layers on $Si_{1-x}Ge_x$/Si, and extremely high mobility Schottky gate MODFETs have been fabricated on such heterostructures.[11-13] To date, no strained Ge channel devices with $SiO_2$ gates on silicon substrates have been reported. We report the first results on strained-Ge channel

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*p*-MOSFETs fabricated on a $Si_{0.3}Ge_{0.7}$/Si virtual substrate utilizing $SiO_2$ as the gate material.

## II. STRAINED LAYER GROWTH

Relaxed graded $Si_{1-x}Ge_x$ buffers (x= 0 to 0.6, 10%/μm) grown by ultrahigh vacuum chemical vapor deposition (UHV-CVD) serve as the starting material for these devices. After growth, relaxed graded buffers are chemical-mechanically polished (CMP) to remove the "cross-hatch" surface roughness associated with the relaxation of mismatched heteroepitaxial layers.[14] Chemical-mechanical polishing also serves to reduce the defect density in the top layers by freeing dislocations caught in pile-ups and minimizing subsequent dislocation nucleation.[14] The wafers are then re-inserted into the UHV-CVD where compositional grading continues to a value of x=0.7 at 750°C. At elevated temperatures, compressively strained Ge layers grown on $Si_{1-x}Ge_x$ have been shown to undulate at a wavelength of approximately 100nm. These ripples strongly scatter holes and can greatly reduce their mobility.[15] The temperature is thus reduced to 400°C to ensure planar growth and 60Å of Ge is deposited. Since the Ge film height does not exceed the equilibrium critical thickness, the strain of the channel is thermodynamically stable and will not relax during subsequent device processing.[16] A thin Si cap is then grown to serve as the interface with the gate in order to avoid the high interface state density that results from depositing $SiO_2$ directly onto the Ge channel.[17] Since Si is mismatched to the $Si_{0.3}Ge_{0.7}$ buffer by approximately 3%, again a low growth temperature must be used to prevent islanding.[18] However, $SiH_4$ decomposes extremely slowly at 400°C (growth rate = $1\times10^{-5}$Å /s), and even growing a 20Å layer takes an impractically long time. Therefore growth is initiated at 400°C and the temperature is increased to 450°C where it is held for some time. $SiH_4$ decomposition on a germanium-rich surface exhibits a slightly elevated rate compared to decomposition over a silicon-rich surface due to differences in surface energy[19], allowing a 10Å layer of Si to completely cover the Ge in a reasonable amount of time. However, once the surface regains its silicon-like character, the growth rate decays back to $1\times10^{-5}$Å/s. In order for Si growth to proceed, the temperature is raised to 550°C, and the Si cap layer is grown to a total thickness of approximately 50-60Å. As can be seen in figure 1, this growth process yields an exceptionally flat Ge channel and Si cap. Note that, in contrast to the compressive Ge channel, the Si cap layer is substantially relaxed (dislocated), since it is grown beyond its critical layer thickness.

## III. MOSFET FABRICATION

Large geometry ($L_{gate}$ = 200μm) ring transistors were fabricated using a self-aligned, one-mask level short flow process, the details of which are reported elsewhere.[20] The gate stack consists of 3000Å of low temperature oxide (LTO) followed by 500Å of poly-silicon, and a schematic of the device wafer including epitaxial growth and CMP steps is shown in figure 2. Before boron implantation and metallization, the gate is slightly undercut to form a T-shape, allowing for a natural lift-off process when the metal is evaporated onto the wafers at normal incidence. These transistors measure true mobility in MOSFETs when extracted properly, and the thick gate oxide allows the transport in the channel to be investigated at a wide range of vertical electrical fields, including the large fields used in scaled MOSFET devices.[20]

## IV. HOLE MOBILITY ENHANCEMENT

Figure 3(a) shows the effective mobility extracted from two device wafers (here labelled UHV_338 and UHV_328) and a bulk silicon control at 300K. To the author's knowledge, the peak mobility of 1160 $cm^2$/V-s represents the highest effective mobility ever measured in a *p*-type MOSFET at room temperature. As can be seen in figure 3(b), the strained germanium channel devices maintain a mobility enhancement of approximately 8 times that of the control over a wide range of vertical fields. UHV_328 and UHV_338 are identical in structure, except that UHV_328's as-grown Si cap thickness is 60Å while UHV_338's as-grown Si cap thickness is 50Å. Native oxide formation and cleaning steps reduce the top Si thickness to 35Å for UHV_328 and 25Å for UHV_338. At high vertical field, figure 3(b) shows that UHV_328 has a degraded mobility enhancement compared to UHV_338, strongly suggesting that part of the hole wave

function can be pulled into the lower mobility Si cap layer. Despite this, UHV_328's mobility enhancement at high fields is still quite significant, indicating that the hole wave function is largely confined in the compressive Ge even in the presence of a parallel conduction path above the channel. The consistency of UHV_338's mobility enhancement over a wide range of vertical electrical fields shows that maintaining a sufficiently low Si cap thickness allows the high field mobility enhancement to be completely preserved.

## V. CONCLUSION

A strained Ge channel with a thin Si cap exhibiting planar morphology was grown on a $Si_{0.3}Ge_{0.7}$/Si CMP'd virtual substrate. *p*-type MOSFETs were fabricated using LTO as the gate material, and a record mobility of 1160 $cm^2$/V-s was extracted. A mobility enhancement of approximately 8 times could be maintained over a wide range of vertical electrical field by minimizing the Si cap thickness. These devices possess immense potential for use in analog applications, as well as potentially serving as a symmetric mobility complement to high-mobility strained-Si *n*-type MOSFETs.

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## REFERENCES

[1]E.A. Fitzgerald, Y.-H. Xie, M.L. Green *et al.*, "Totally relaxed GexSi1-x layers with low threading dislocation densities grown on Si substrates," Appl. Phys. Lett. **59** (7), 811-813 (1991).

[2]E.A. Fitzgerald, Y.-H. Xie, D. Monroe *et al.*, "Relaxed GexSi1-x structures for III-V integration with Si and high mobility two-dimenstional electron gases in Si," J. Vac. Sci. Technol. B **10** (4), 1807-1819 (1992).

[3]J.A. Carlin, S.A. Ringel, E.A. Fitzgerald *et al.*, "Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates," Applied Physics Letters **76** (14), 1884-1886 (2000).

[4]J. Welser, J.L. Hoyt, and J.F. Gibbons, "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," IEEE Electron Device Letters **15** (3), 100-102 (1994).

[5]K. Rim, J. Welser, J.L. Hoyt *et al.*, "Enhanced Hole Mobilites in Surface-channel Strained-Si p-MOSFETs," IEEE IEDM Tech. Dig. , 517-519 (1995).

[6]D.K. Nayak, K. Goto, A. Yutani *et al.*, "High Mobility Strained-Si PMOSFETSs," IEEE Transactions on Electron Devices **43** (10), 1709-1716 (1996).

[7]G. Hock, E. Kohn, C. Rosenblad *et al.*, "High hole mobility in Si0.17Ge0.83 channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhance chemical vapor deposition," Applied Physics Letters **76** (26), 3920-3922 (2000).

[8]C.M. Ransom, T.N. Jackson, and J.F. DeGelormo, "Gate-Self-Aligned n-channel and p-channel Germanium MOSFETs," IEEE Transactions on Electron Devices **38** (12), 2695 (1991).

[9]D. Reinking, M. Kammler, N. Hoffman *et al.*, "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," Electronics Letters **35** (6), 503-504 (1999).

[10]M.V. Fischetti and S.E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," J. Appl. Phys. **80** (4), 2234-2252 (1996).

[11]S.J. Koester, R. Hammond, and J.O. Chu, "Extremely High Transconducatnce Ge/Si0.4Ge0.6 p-MODFET's Grown by UHV-CVD," IEEE Electron Device Letters **21** (3), 110-112 (2000).

[12]U. Konig and F. Schaffler, "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters **14** (4), 205-207 (1993).

[13]G. Hock, T. Hackbarth, U. Erben *et al.*, "High performance 0.25um p-type Ge/SiGe MODFETs," Electronics Letters **34** (19), 1888-1889 (1998).

[14]M.T. Currie, S.B. Samavdeam, T.A. Langdo *et al.*, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-

mechanical polishing," Applied Physics Letters **72** (14), 1718-1720 (1998).

[15]Y.H. Xie, D. Monroe, E.A. Fitzgerald *et al.*, "Very high mobility two-dimensional hole gas in Si/GexSi1-x/Ge structures grown by molecular beam epitaxy," Appl. Phys. Lett. **63** (16), 2263-2264 (1993).

[16]E.A. Fitzgerald, "Dislocations in strained-layer epitaxy:theory, experiment, and applications," Materials Science Reports **7**, 87-142 (1991).

[17]F.K. Legoues, R. Rosenberg, T. Nguyen *et al.*, "Oxidation studies of SiGe," J. Appl. Phys. **65** (4), 1724-1728 (1989).

[18]Y.H. Xie, G.H. Gilmer, C. Roland *et al.*, "Semiconductor Surface Roughness: Dependence on Sign and Magnitude of Bulk Strain," Physical Review Letters **73** (22), 3006-3009 (1994).

[19]D.J. Tweet, T. Tatsumi, H. Hirayama *et al.*, "Factors determining the composition of strained GeSi layers grown with disilane and germane," Appl. Phys. Lett. **65** (20), 2579-2581 (1994).

[20]M. Armstrong, Ph.D. Thesis Massachusetts Institute of Technology (1999).


Figure 1- Cross-sectional TEM of the Ge MOSFET structure as grown, showing the relaxed $Si_{0.3}Ge_{0.7}$ buffer layer, Ge channel, and Si cap

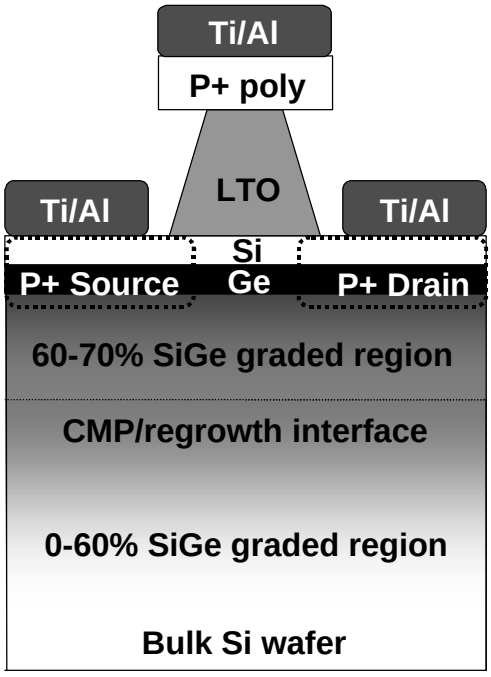
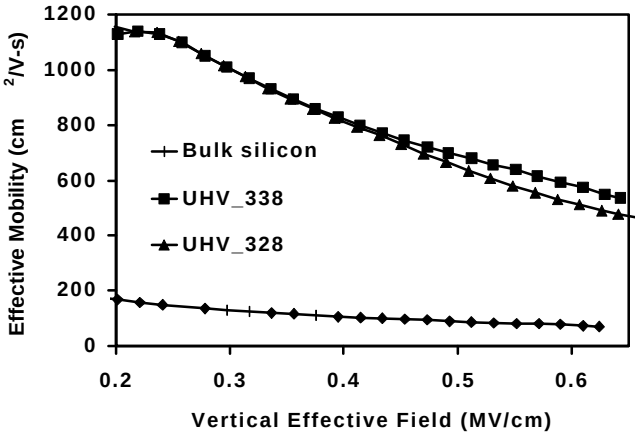
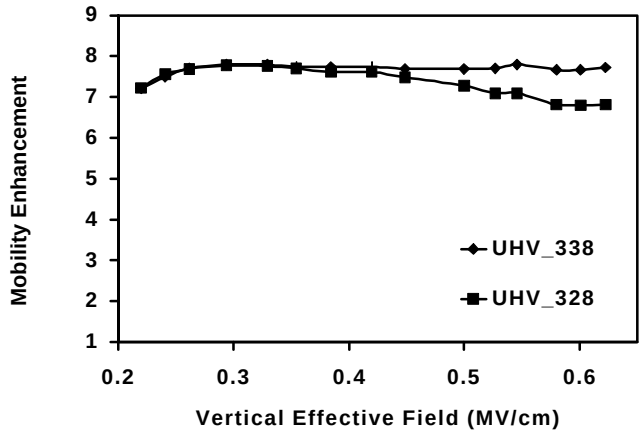



Figure 2-Schematic of short flow Ge MOSFET




(a)




(b)

Figure 3- (a) Effective hole mobility of strained Ge p-MOSFETs compared with the co-processed bulk Si p-MOSFET
(b) Mobility enhancement of the strained Ge p-MOSFET showing slight degradation at high field for UHV_328