Substrate Noise Analysis and Techniques for Mitigation in Mixed-Signal RF Systems

by

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S.B., Massachusetts Institute of Technology (2001)
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Abstract

Mixed-signal circuit design has historically been a challenge for several reasons. Parasitic interactions between analog and digital systems on a single die are one such challenge. Switching transients induced by digital circuits inject noise into the common substrate creating substrate noise. Analog circuits lack the large noise margins of digital circuits, thus making them susceptible to substrate voltage variations. This problem is exacerbated at higher frequencies as the effectiveness of standard isolation technique diminishes considerably. Historically, substrate noise was not a problem because each system was fabricated in its own package shielding it from such interactions.

The work in this thesis spans all areas of substrate noise: generation, propagation, and reception. A set of guidelines in designing isolation structures was developed to assist designers in optimizing these structures for a particular application. Furthermore, the effect of substrate noise on two key components of the RF front end, the voltage controlled oscillator (VCO) and the low noise amplifier (LNA), was analyzed.

Finally, a CAD tool (SNAT) was developed to efficiently simulate large digital designs to determine substrate noise performance. Existing techniques have prohibitively long simulation times and are only suitable for final verification. Determination of substrate noise coupling during the design phase would be extremely beneficial to circuit designers who can incorporate the effect of the noise and re-design accordingly before fabrication. This would reduce the turn around time for circuits and prevent costly redesign. SNAT can be used at any stage of the design cycle to accurately predict (less than 12% error when compared to measurements) the substrate noise performance of any digital circuit with a large degree of computational efficiency.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

1.1 Motivation

The first electrical circuits consisted of discrete components such as resistors, inductors, capacitors, and vacuum tubes. With the invention of the transistor and the integrated circuit (IC) in 1947 and 1959 respectively, a new era of high density, low cost, complex circuits began. The IC allowed for millions for transistors to be integrated on a small piece of silicon measuring as little as a few millimeters squared. Advances in manufacturing have allowed for more transistors to be packed into a smaller area with higher yield allowing more complex designs to be realized.

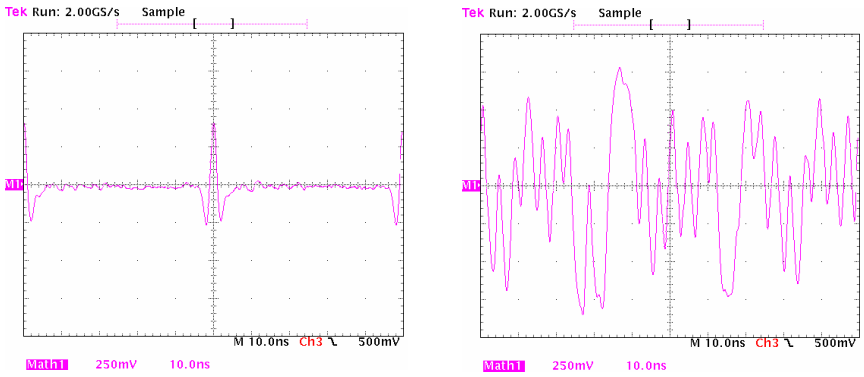
The ever decreasing transistor features sizes have naturally led to increased levels of integration. This integration results in not only higher density circuits but also increased performance by eliminating off-chip connections. Thus, today's state of the art solutions exploit high levels of integration. In particular, products in the wireless telecommunications industry have fueled increased demands for portability while achieving enhanced functionality and low power consumption. As a result of these demands, digital and analog circuits that were previously fabricated on separate chips are being placed on the same die to achieve increased performance.

However, many challenges have arisen that oppose this single chip integration. Parasitic interactions between analog and digital systems fabricated on a single die are one such challenge. Switching transients induced by digital circuits inject noise into

the common substrate. Analog circuits lack the large noise margins of digital circuits, thus making them susceptible to substrate voltage variations resulting in corrupted performance. Historically, these problems did not exist because each system was fabricated in its own package shielding it from such interactions.

With increasing circuit speeds and levels of integration, the detrimental effect of substrate noise is becoming more and more severe. Designers are only now starting to realize how serious the substrate noise problem is. Previous attempts to minimize substrate noise were largely ad hoc. A particular guard ring geometry that worked in one design would be used repeatedly even though the substrate noise requirements probably differed. Such ad hoc techniques are no longer able to solve the substrate noise problem in large designs. In fact, for current and future designs, substrate noise is considered to be a major "showstopper" to large levels of integration.

Figure 1.1 details how severe the substrate noise problem is. Figure 1.1 shows the output of a low noise amplifier that is part of an ultra wideband (UWB) transceiver. The system was fabricated in TSMC's 0.18 μm mixed-mode process. Figure 1-1(a) shows the output of the LNA when the digital system is turned off. The received signal is clearly defined. Figure 1-1(b) shows the output when the digital system is powered on. Substrate noise completely swamps out the received signal.



(a) Digital off. (b) Digital on.

Figure 1-1: LNA output of a UWB transceiver with the digital system powered off and on. Figures courtesy of F. Lee.

Designing for substrate noise remains somewhat of a "black art". Tricks are

employed without an understanding for why it works, or how it can be optimized. Analog designers typically design the system assuming a particular substrate noise value that is a result of intuition. The accuracy of this estimate is typically not verified. As a result, systems could be severely over-designed or, even worse, under-designed for substrate noise robustness.

Moreover, there is currently no systematic methodology on how to design isolation structures. Parameters that greatly affect isolation are the geometry and the connections to the power supply. For example, a 100 μm wide guard ring will yield better isolation than a 5 μm guard ring. Most designs for guard rings have arbitrarily chosen widths. In addition, the connections to the guard ring have a profound effect on the isolation that it is able to provide. Improper connections can actually result in increasing the noise instead of mitigating it.

The substrate noise problem is extremely complex. In order to minimize the effects of substrate noise, a combination of techniques needs to be employed. For example, TI demonstrated a single-chip GPS solution using many different isolation techniques [52]. Because of the stringent requirements of the GPS receiver, a large amount of isolation was required. No single technology provides an adequate amount of isolation. TI was able to integrate the digital and RF front end together by employing careful frequency planning, careful layout, dedicated hardware to reduce the effects of switching currents, differential circuits, careful pin assignment, guard rings, and optimized placement of digital blocks to achieve the isolation required to implement the single chip solution.

The goal of this thesis is to shed some light into this "black art" by providing a methodology and set of guidelines to design to.

1.2 Contributions of this Dissertation

The work described in this dissertation spans all three categories of substrate noise work. An overview of existing work in the area of substrate noise is presented in Chapter 2. To completely understand the complex problem of substrate noise, the

various mechanisms behind it were examined. This is presented in Chapter 3.

The effect of substrate noise on two key components of the RF front end was analyzed. Through simulation, the amount of isolation required to integrate RF front ends implementing different wireless standards with a Pentium® 4 microprocessor was derived in Chapter 4. Moreover, a test chip was designed to study the effect of substrate noise on the phase noise of a voltage controlled oscillator (VCO). In addition, the effect of different VCO parameters on the noise performance was also examined. This work is discussed in Chapter 5.

A CAD tool (SNAT) was developed to efficiently simulate large digital designs to determine substrate noise performance. Other tools exist that perform this same function; however, they are only amenable for use as a final verification tool.

SNAT can work at any stage in the design cycle. The real power of the tool is its ability to determine an estimate of the substrate noise early in the design cycle when measures can be taken to mitigate the noise. If an estimate is determined only after the design and layout are complete, any re-design would be extremely cumbersome. The SNAT methodology is described in detail in Chapter 6.

To verify the results of SNAT, comparisons to both a full transistor level simulation using SPICE and measured data on fabricated test circuits were performed. These results are discussed in Chapter 7. The most accurate SNAT simulation yields less than 12% error when compared to substrate noise measurements on a digital PLL designed in TI's 90 nm technology.

To demystify the design of isolation structures, different structures were examined to determine the effect of different parameters on the isolation characteristic. As a result, a set of guidelines in designing these structures was developed to assist designers in optimizing isolation structures for a particular application. These guidelines are presented in Chapter 8.

Finally, future work in the area of substrate noise is proposed.

Chapter 2

Overview of Substrate Noise Work

With the increasing levels of integration in ICs today and ever-increasing digital circuit speeds, the problem of substrate noise is becoming more and more pronounced. The performance of sensitive analog circuits can be severely degraded. The effect of substrate noise on the circuits within an IC is typically observed during the testing phase only after the chip has been fabricated. Determination of substrate noise coupling during the design phase would be extremely beneficial to circuit designers who can incorporate the effect of the noise and re-design accordingly before fabrication. This would reduce the turn around time for circuits and prevent costly redesign. It is becoming more and more apparent that substrate noise is a topic that merits further and more detailed investigation.

Work in the area of substrate noise falls into one of three categories. The first is the simulation of digital circuits to determine the substrate noise generated. To be able to manage the substrate noise problem, the need for simulation to predict substrate noise performance is becoming more evident.

Standard techniques to simulate for substrate noise tend to be either accurate, but extremely inefficient or fast, but rather inaccurate. Noise macromodelling approaches fall in between these two ends of the spectrum. The inefficient techniques are accurate because all noise sources, coupling, and propagation mechanisms are well modeled; however, this leads to a large number of nodes which account for the inefficiency. These techniques involve simulating a large number of nonlinear devices in order to

accurately model the noise current profiles. The fast techniques rely on the random nature of the noise generated. They assume that if the number of gates is large enough and if the global switching activity is uniformly distributed over a large portion of the spectrum, the noise can be modeled as a single Gaussian white or pink noise source [38]. Approximating the noise as a Gaussian source captures only a small portion of the entire energy spectrum. Thus, detrimental noise components are often omitted or grossly underestimated.

A survey of these techniques is presented in Section 2.1. Understanding these approaches permits a greater understanding of the substrate noise analysis methodology that is presented in Chapter 6.

The second category of work concerns modeling the substrate itself. Most work on substrate noise falls into this category. Different approaches to accurately model the substrate typically result in an extremely large mesh of passives. Much work has focused on techniques to reduce the substrate netlist to a more manageable form while maintaining accuracy [53] [33] [32]. Accurate substrate modeling is a very complex problem that is outside the scope of this work. However, more rudimentary substrate models were developed to permit extremely fast substrate simulations at the expense of some accuracy.

The final category of work and also the least developed is in the area of examining the effect of substrate noise on analog circuits. Most work has focused on low frequency circuits such as A/D converters [17]. Most work on radio frequency (RF) circuits has been limited to the low noise amplifier [60].

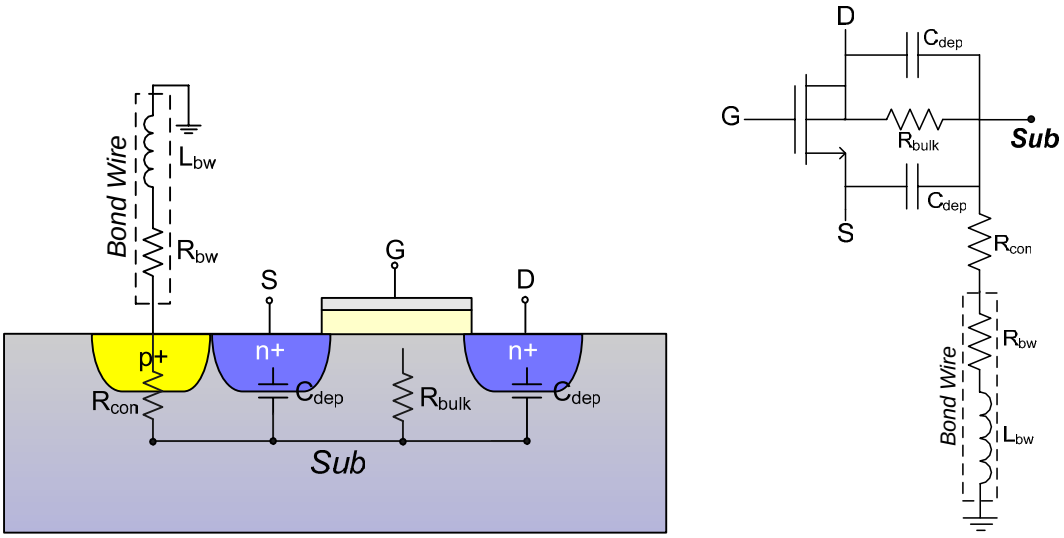
2.1 Substrate Noise Simulation Strategies

Existing approaches to substrate noise simulation are presented in this section. Section 2.1.1 describes a full transistor level methodology to simulate for substrate noise. Section 2.1.2 discusses three methodologies that speed up the simulation with the use of noise macromodels.

2.1.1 Full Transistor-Level Simulation Using SPICE

The most straightforward technique to simulate for substrate noise involves modifying the circuit netlist to account for noise injection into the substrate as well as propagation in the substrate itself [55].

Figure 2-1(a) shows the cross-section of an NMOS device and the elements that are added to model injection into the substrate. Figure 2-1(b) shows these elements in a circuit.



(a) Cross-section. (b) Equivalent circuit.

Figure 2-1: Elements added to an NMOS device to model injection into the substrate.

The source and drain regions are capacitively coupled to the substrate through the depletion capacitances. These nonlinear capacitances depend on the source and drain voltages as given by [46]:

$$C_J = \frac{AC_{JA}}{(1-\frac{V}{\phi_B})^{m_A}} + \frac{PC_{JSW}}{(1-\frac{V}{\phi_B})^{m_{SW}}} \tag{2.1}$$

Because of this dependence, these capacitances will vary over time if the outputs are switching.

The bulk node of the device is resistively connected to the local substrate node through a resistance given by Equation 2.2 [55]. ρ is the resistivity of the channel

region. For an epi substrate, T is the thickness of the epi layer. For a non-epi substrate, T is roughly the junction depth.

$$R_{bulk} = \frac{\rho T}{LW} \tag{2.2}$$

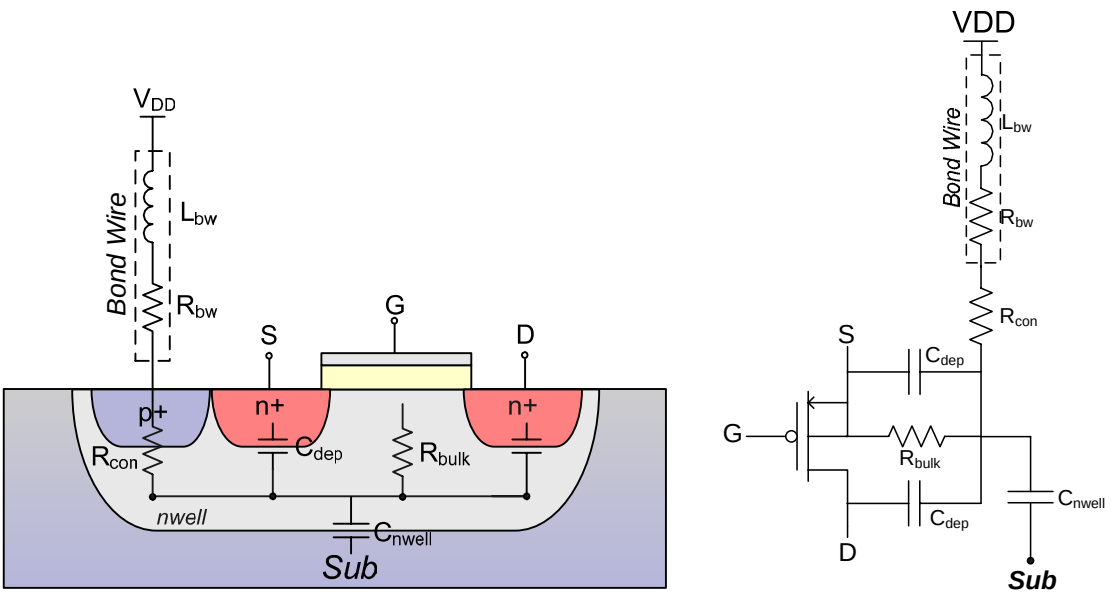
The final element that is added to account for coupling into the substrate is the resistance of the substrate contact, which is connected to ground through a bond wire. A series resistance and inductance is used to model the bond wire impedance. The amount of noise that couples through the substrate contact can be quite significant. Typically the source is shorted to the substrate contact to prevent any threshold voltage fluctuation. In doing so, switching currents work in tandem with the impedance associated with the ground line to create ground bounce. This node is resistively connected to the substrate resulting in most of the ground bounce appearing on the substrate itself.

To model injection into the substrate, these four elements have to be added per NMOS device. However, in most circuits, the source is connected to the same ground as the substrate contact thus shorting out the source depletion capacitance. In this case, only three additional elements need to be added.

The elements that must be added to a PMOS device are similar to that of the NMOS except an additional term to model the n-well must be incorporated. The additional elements are shown in Figure 2-2(a) and 2-2(b).

The expression for the depletion capacitance is roughly the same, except signs are changed to compensate for the PMOS nature. The expression for R_{bulk} as given in Equation 2.2 is the same for the PMOS device except the resistivity is now the resistivity of the n-well. The substrate contact for the PMOS is connected to V_{DD} through bondwires. The local substrate node, however, is shielded from the substrate by the n-well. This is modeled with a resistance through the n-well and a capacitance representing the n-well junction capacitance.

For each PMOS device, six additional elements are required to model injection into the substrate. For most circuits, the source is connected to the same power



(a) Cross-section. (b) Equivalent circuit.

Figure 2-2: Elements added to a PMOS device to model injection into the substrate.

supply as the substrate contact shorting out the depletion capacitance. This results in only five additional elements to model the injection.

Example: CMOS Inverter

To predict the noise injected by a single CMOS inverter, the elements described above need to be added to the inverter circuit to account for injection into the substrate. The circuit in the dashed blue box of Figure 2-3 represents the inverter with the additional elements to model injection into the substrate. The circuit elements in the dashed green box represent the model for the substrate at low frequencies. The circuit in the dashed red box is the model for a substrate contact used to probe the substrate noise.

For such a simple circuit, an additional eight nodes have to be simulated with a combination of nonlinear and linear devices to determine the noise injected into the substrate. Additional nodes have to be simulated in order to model propagation in the substrate. From this simple example, it is apparent that the additional elements that have to be added to model for substrate noise increase rapidly with the size of

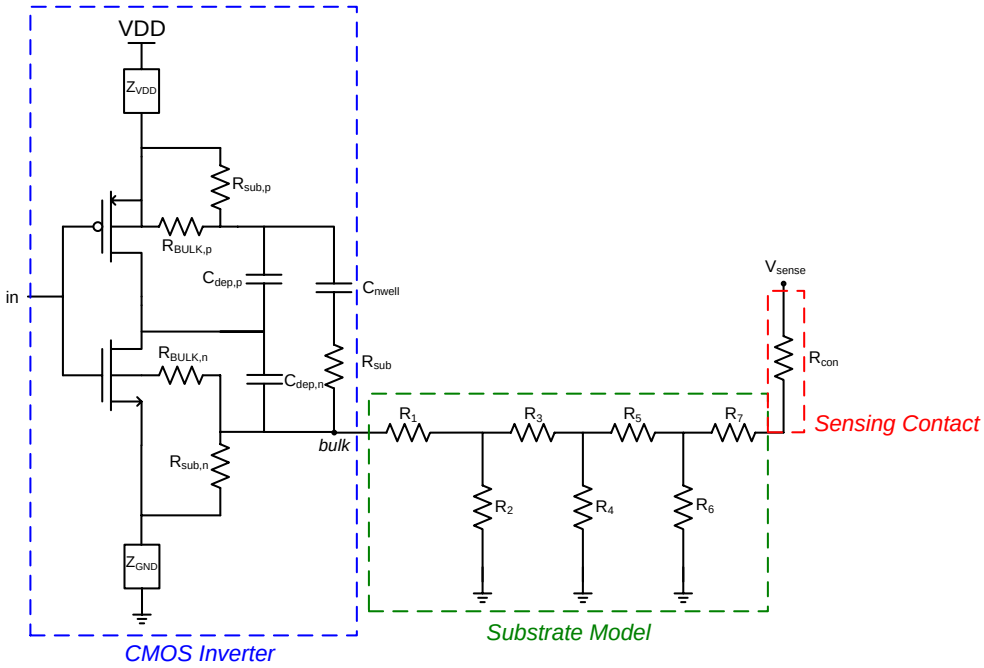


Figure 2-3: CMOS inverter with noise injection and substrate models.

the circuit.

Consider a medium-scale circuit with approximately one million devices. To model injection into the substrate, an additional four million passive elements must be added to the circuit. Thus, in order to predict the noise injected, a simulation of one million nonlinear devices and four million passive elements has to be performed. To model propagation within the substrate itself, more elements have to be added. Because the complexity of the circuit scales rapidly with circuit size, the simulation time will be excessively long and in most cases will not converge.

2.1.2 Noise Macromodels

Transistor level simulation techniques result in prohibitively long simulation times as described in Section 2.1.1. If the noise behavior could be abstracted to a higher level while still preserving the relationship to the substrate, simulation times could be reduced. One way of accomplishing this is to extract the switching behavior of the digital circuit and to use mathematical models to calculate the substrate noise. In [41], a behavioral model based on AnalogHDL is used. Switching transitions from

AnalogHDL together with mathematical expressions for the substrate noise are used to predict the substrate noise profile. Because mathematical expressions instead of real waveforms are used to generate the noise profiles, this methodology can never yield an accurate prediction of the substrate noise. Furthermore, with technology scaling, mathematical models used to model transistor behavior are becoming more complex. Because this technique relies on the ability of the mathematical expressions to model the substrate noise behavior, its accuracy will further diminish for future technology nodes. The methodology was only verified for a 0.6 μm process.

Another technique that abstracts the noise behavior is macromodelling. In order for the macromodels to still yield accurate results, the noise behavior of the circuit has to be completely encapsulated. This involves not only accurately modeling injection into the substrate but also accurately modeling the switching noise.

Noise macromodelling approaches fall into two categories. The first three methodologies presented are input dependent and all follow a similar flow. These approaches are based on the superposition of patterns and current profiles to generate the noise signature. Noise waveforms at critical nodes are determined based on user-supplied I/O vectors. Switching elements are typically simplified with linear macromodels that mimic the switching behavior of the original circuit. The strategies in [22], [38], and [14] are examples of techniques that use input dependent macromodels. All these techniques generate an equivalent circuit similar to that shown in Figure 2-4. Each, however, uses a different macromodel.

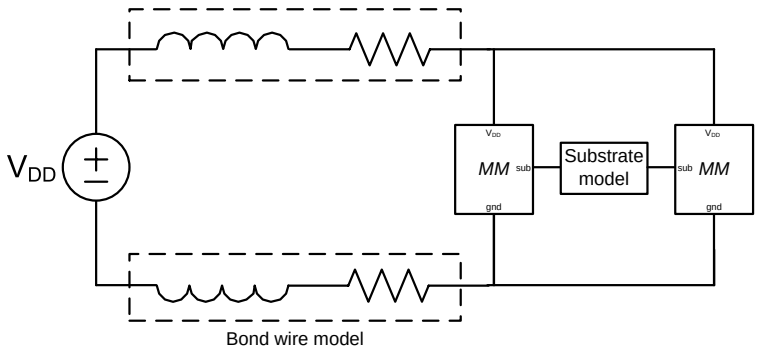


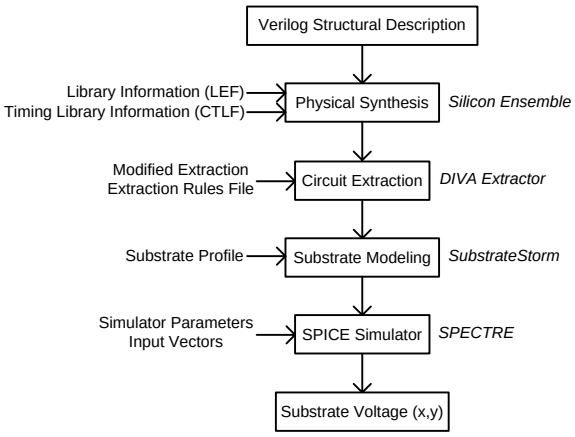
Figure 2-4: Equivalent circuit generated by macromodelling approaches.

These approaches yield the best accuracy with reasonable simulation times. The main limitation of the macromodelling technique is that determining the worst case noise behavior of the circuit can be a formidable task. Multiple simulations over different input conditions would have to be performed. The main input dependent macromodelling methodologies are described in this section. Each of these methodologies vary in the implementation of the algorithm and in the macromodel used.

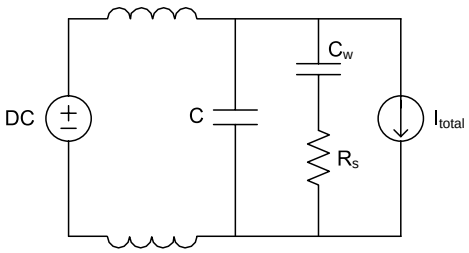
The second type of methodology is input independent and is discussed later in this section.

Universitat Politècnica de Catalunya Methodology

In this methodology [22], a gate level macromodel is constructed to model the substrate noise behavior of a particular gate. These gate macromodels are then combined to form the complete circuit macromodel. Together with event information from logic simulation, SPICE is used to simulate the entire equivalent circuit. Figure 2-5(a) shows the simulation flow. Figure 2-5(b) shows the macromodel used.



(a) Simulation methodology.



(b) Noise macromodel.

Figure 2-5: Universitat Politècnica de Catalunya's simulation methodology [42].

Their macromodel consists of a package model that typically can be reduced to a lumped inductance associated with the V_{DD} and ground pins. The model only has one noise source that is represented by a current source. This is based on the observation that most of the noise is a result of switching currents in the power supply

network. Finally, passive elements that model the parasitics between V_{DD} and ground are included.

The model of a full digital circuit is generated through the superposition of the macromodels of the building blocks of the circuit. A library for a set of standard cells that contains the noise macromodels for each cell is constructed. The macromodels are then connected using a substrate model generated from SubstrateStorm [8]. Because SubstrateStorm requires a full layout, this methodology is only amenable for use as a final verification tool.

Their methodology was validated against SPICE for a 0.35 μm technology and yielded excellent correlation. The limitation of this tool is that the effect of switching inputs and outputs is neglected. The contribution due to this source is not negligible resulting in significant errors for interconnect dominated applications.

SubWave Methodology

SubWave is a methodology developed at Berkeley that is also based on macromodels [38]. SubWave's main limitation is that coupling from the supply is ignored. Only injection from impact ionization currents and source/drain depletion capacitances is considered. The omission of the power supply coupling greatly reduces the accuracy of this methodology as it has been well established that power supply coupling is a major source of substrate noise [15].

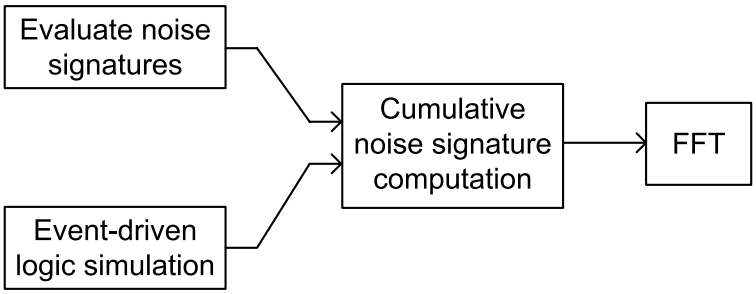


Figure 2-6: Flow diagram of SubWave [38].

SubWave also includes a library characterization step where the substrate current for each standard cell is extracted for each input switching pattern. For a given

input pattern, an event driven simulation records every transition. An impulse train of events generated from the event information is convolved with the precomputed noise signatures to yield the resulting substrate noise profile. Figure 2-6 shows the methodology. Their methodology is based on the assumption that all noise sources are spatially independent. This assumption is not valid for non-epi substrates.

Susbstrate Waveform Analysis (SWAN) Methodology

The methodology of the tool (SNAT) developed in this thesis is based on the SWAN methodology developed at IMEC [26]. This methodology is described in this section so that the architectural changes implemented in SNAT become apparent when discussed in Chapter 6.

The main contribution of this thesis is that all possible noise sources are considered. Switching inputs and outputs were not included in the methodology developed at the Universitat Politècnica de Catalunya [22]. Thus, the tool will yield inaccurate results for interconnect dominated applications, which are becoming more and more pervasive. The SubWave [38] tool ignored power supply coupling, which is a significant source of noise. The SWAN methodology uses a macromodel that is more complete than the other methodologies surveyed in this chapter. Figure 2-7 shows the SWAN macromodel.

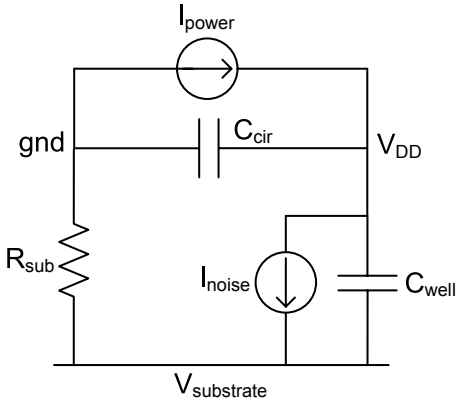


Figure 2-7: SWAN macromodel [26].

The two current sources in the macromodel represent the two noise sources consid-

ered: power supply coupling and coupling from the MOSFET itself. I_{power} represents the current through the power supply. I_{noise} models the substrate current injection through switching nodes. R_{sub} represents the resistance between the on-chip ground and the substrate. It is typically quite small as it consists of the parallel combination of the resistances of the substrate contacts. C_{well} is the capacitance between V_{DD} and the substrate and is essentially the n-well capacitance. C_{cir} is the circuit capacitance between V_{DD} and ground.

The SWAN methodology is very similar to that used by the Universitat Politècnica de Catalunya and is shown in Figure 2-8.

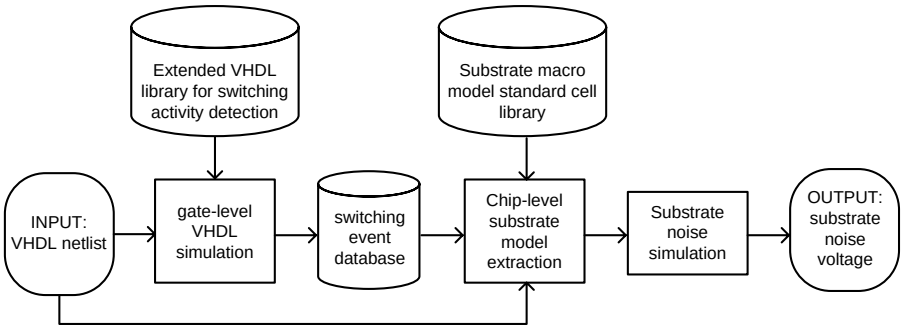


Figure 2-8: SWAN methodology [13].

First, each standard cell is characterized to extract the element values of the macromodel. The dependencies of I_{power} and I_{noise} are extracted for all possible input combinations during this one time characterization step. This library characterization need only be performed once per technology node and takes roughly 39 hours for a library containing 96 cells [26].

The second step in the methodology involves the substrate noise simulation itself. First, the characteristics of the switching events have to be extracted. This is accomplished by adding switching event detection processes to VHDL. In this process, all input transitions are recorded. Next, the macromodels of the individual gates are combined together. For epi substrates, the substrate is one electrical node allowing all the macromodels to connect in parallel. Thus, all macromodel elements add in parallel. The waveforms of the noise currents are calculated by convolving the current patterns with the switching events. Finally, a package model is added, and the

resulting equivalent circuit is solved to obtain the substrate voltage. SWAN shows good correlation to SPICE simulations with approximately 6.3% error in the RMS voltage but with a speedup of 213 times for an 8-bit multiplier [12]. Experimental verification on a 220K gate WLAN chip implemented in a 0.35 μm CMOS process on an epi substrate has been presented [11]. For this system, SWAN was accurate to within 20% of the measured RMS voltage.

They also demonstrated experimental verification on a 40K gate telecom circuit in a 0.18 μm CMOS technology on a non-epi substrate. For this test circuit, SWAN was accurate to within 20% of measurements. SubstrateStorm [8] was used to generate the substrate model from layout.

Input independent macromodels

The work in [39] is an example of an input independent simulator. It relies on power dissipation data from a system-level power estimator to predict the substrate noise profile. In that work, substrate coupling from interconnect and source/drain diffusion regions is assumed to be negligible compared to V_{DD} and ground noise. More and more digital systems are interconnect dominated, and in such circuits, the noise contribution from interconnect can be significant [37]. However, their assumption is valid for small scale circuits where the role of the interconnect is not important. Because only power supply noise is considered, examining the power dissipation permits the prediction of current transients that dissipated the power. The root mean square (RMS) value of the current transients can be calculated using the following equation.

$$I_{Vdd} = P_{Vdd}/V_{DD} \tag{2.3}$$

Once the current is computed, the entire system is replaced with an equivalent linear macromodel shown in Figure 2-9. The macromodel is then simulated to generate the substrate noise profile.

This methodology determines RMS contours of the substrate noise that represent the average amount of noise at any point on the substrate. This technique cannot be

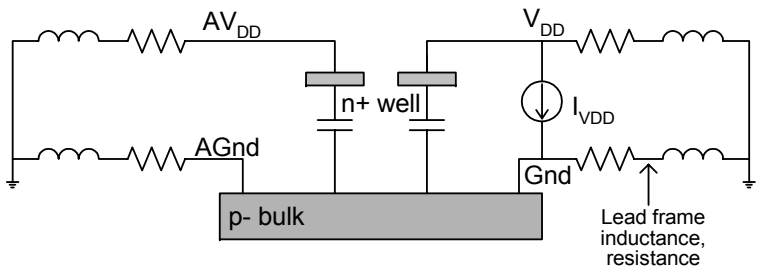


Figure 2-9: Input independent macromodel used in [39].

used to examine the time varying nature of the substrate noise or to get a sense for the frequency content of the noise. Knowing only an estimate of the peak substrate noise value without knowing its frequency content is not entirely useful. The purpose of determining the noise profile is to be able to design appropriate isolation structures and to determine the effect of that noise on any analog circuits that are integrated with the digital system. If a narrowband RF circuit is to be integrated with a particular digital system, only the noise in band is of interest. Without knowing the frequency content, the severity of the substrate noise problem cannot be assessed. Furthermore, the amount of attenuation afforded by isolation structures is frequency dependent. Without knowing what frequencies should be targeted, the isolation structure design will not be optimized.

This technique can only used to generate a rough estimate of the noise and thus is only useful for floorplanning [39].

2.2 Summary

Existing methodologies to simulate for substrate noise were presented in this chapter. A full SPICE transistor-level simulation yields the most accurate results; however, run times are excessively long. Several approaches exist that use noise macromodels to speed up the run time. Each has its own shortcomings, which the CAD tool developed in this thesis attempts to address in Chapter 6.

Chapter 3

Substrate Noise Mechanisms

3.1 Overview

The ability to implement mixed-signal systems by integrating analog and digital subsystems on a single die has led to dramatic improvements in performance and enabled a host of new applications. However, this integration has given rise to several new problems created by parasitic interactions between the two subsystems. Historically, these problems were not an issue as the two subsystems were isolated in their own packages.

Even though these two systems are often physically separated by large distances, they are still connected through the common substrate as shown in Figure 3-1. The switching of digital circuits injects noise into the substrate. The substrate is a conductive medium thereby allowing noise to easily propagate from the digital subsystem to the analog subsystem. Because analog circuits lack the noise immunity of digital circuits, the coupled noise detrimentally affects the analog performance.

The three mechanisms governing substrate noise (injection, propagation, and reception) are discussed in this chapter in Sections 3.2-3.4. A survey of the different types of isolation schemes is presented in Section 3.5.

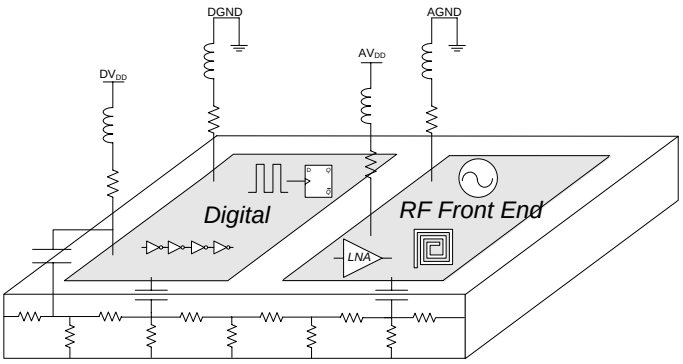


Figure 3-1: RF and digital systems on the same chip.

3.2 Injection

Figure 3-2 depicts the various noise mechanisms in a mixed-signal circuit. The cross-section of an inverter is shown on the left and is used to represent the digital system. The circuit on the right is a simple NMOS transistor used to represent the analog system.

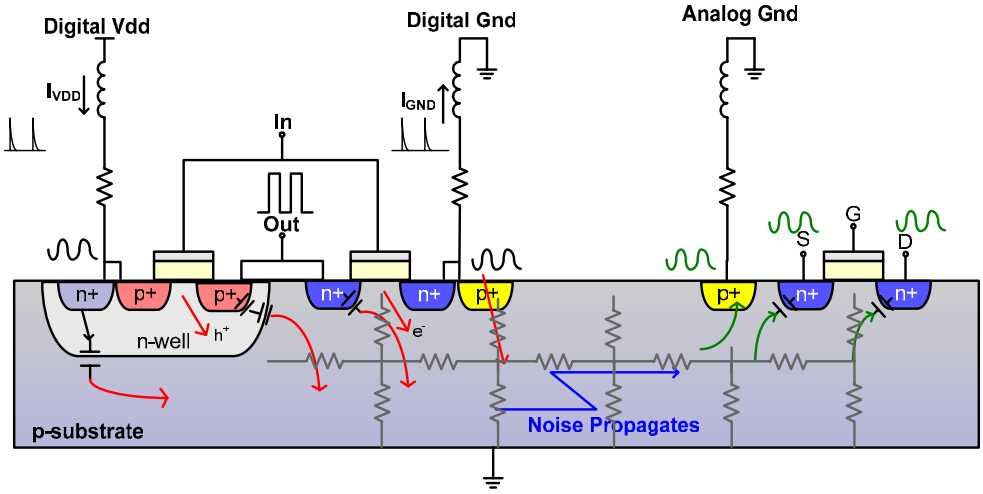


Figure 3-2: Noise mechanisms in a mixed-signal system.

Noise is injected into the substrate through three paths. The first is *coupling through capacitances*. Every source and drain is coupled to the substrate through a depletion capacitance. Furthermore, interconnect lines also have a capacitance to substrate. At switching instances, noise will capacitively couple from these nodes into the substrate. The voltage levels on these lines tend to be rail to rail. If the capaci-

tance is sufficiently large, the coupled noise from these sources can be significant. In particular, long lines carrying high-speed signals can inject noise that is comparable to hundreds of switching transistors [37].

Injection from interconnect is more complicated than simple capacitive coupling. Global wires in higher level metal layers typically have other metal layers underneath, which can shield coupling to the substrate. Nevertheless, long, wide, global wires still exist, for example, in routing I/O lines often times with little interconnect underneath. Moreover, noise injection through bond pads can also be significant. The capacitance to substrate from the pad stack can be on the order of picofarads. If high-speed signals are routed on and off-chip, the injected noise from the pads can be significant. In fact, neglecting the injection from bond pads can lead to significant errors in estimating substrate noise levels. This is discussed further in Section 7.3.4 of Chapter 7.

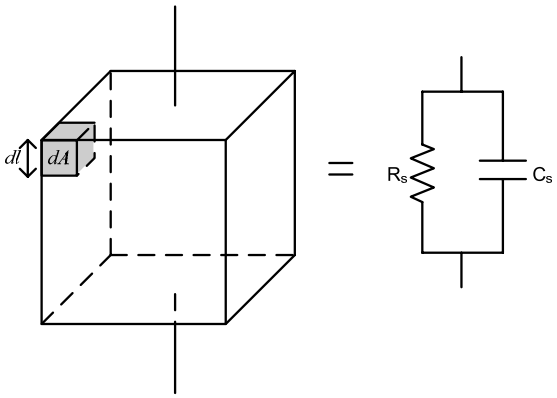
The second injection mechanism is through *substrate contacts*. Substrate contacts consisting of p+ and n+ diffusion regions from NMOS and PMOS devices respectively are used to set the bulk terminal of the device to either ground or V_{DD} depending on the device type. Furthermore, the source and bulk terminals are typically shorted together to prevent threshold voltage fluctuations due to the backgate effect [46]. For an NMOS device, the source and bulk are connected to ground; whereas, for a PMOS, the source and bulk are connected to V_{DD}. The power and ground lines are connected to the outside world through bond pads and pins of the package. A series inductance and resistance is associated with the bondwires.

When a digital transition occurs, a spike of current from the power supply is used to charge an output load. A significant portion of this current is discharged to ground which the substrate ultimately connects to. These currents work in tandem with the parasitics of the power and ground lines to cause ringing in the supplies. This is known as V_{DD} and ground bounce. This ringing is typically on the order of tens of millivolts. Compared to the full swing signals that induce noise through capacitive coupling, this noise would appear to be negligible. However, since the substrate is connected to power and ground through low resistance substrate contacts, any noise that appears on these lines directly appears on the substrate.

The last source of noise injection is from *impact ionization currents*. High electric fields in the depleted drain end of the device result in the creation of electron-hole pairs. For an NMOS device, the holes created by impact ionization flow into the substrate creating a current flowing between the drain and the substrate [56]. As this current flows into the resistive substrate, it induces fluctuations in the bulk potential.

3.3 Propagation

The second mechanism that governs substrate noise is propagation through the common substrate. Silicon, as a semiconducting material, exhibits both conductive and dielectric behavior. However, at low frequencies, the conductive nature of silicon dominates over the dielectric behavior. This crossover frequency depends on the doping and is given by Equation 3.1 for a p-type substrate. This frequency essentially corresponds to the dielectric relaxation time constant of silicon. At operating frequencies below the crossover, any charge storage effects can be neglected; thus, the substrate can be modeled as purely resistive. At frequencies above the crossover, the dielectric behavior of the silicon can no longer be neglected; thus, the substrate must be modeled as a resistive and capacitive mesh. A plot of the crossover frequency versus substrate doping is shown in Figure 3-4.



$$
\begin{aligned}
J &= \sigma E = q(n\mu_n + p\mu_p)E \\
Y_s &= \frac{1 + sR_sC_s}{R_s} = \frac{1 + j\omega T_s}{R_s} \\
T_s = R_sC_s &= \frac{\rho_s dl}{dA}\frac{\epsilon_s dA}{dl} = \frac{\epsilon_s}{q(n\mu_n + p\mu_p)} \\
f_0 &= \frac{1}{2\pi T_s} = \frac{q(n\mu_n + p\mu_p)}{2\pi\epsilon_s} \\
f_{0,min} &= \frac{q\mu_p p}{2\pi\epsilon_s}
\end{aligned}
\tag{3.1}
$$

Figure 3-3: Model for a piece of homogeneous substrate [45].

There is an inverse relationship between the crossover frequency and substrate re-

sistivity. The resistivity of typical mixed-mode (high resistivity) non-epitaxial wafers is typically around 10-15 Ω·cm. A resistivity of 13 Ω·cm corresponds to a crossover frequency of 11.6 GHz. Typical operating frequencies in silicon are below 10 GHz; thus, a resistive approximation for the substrate is valid.

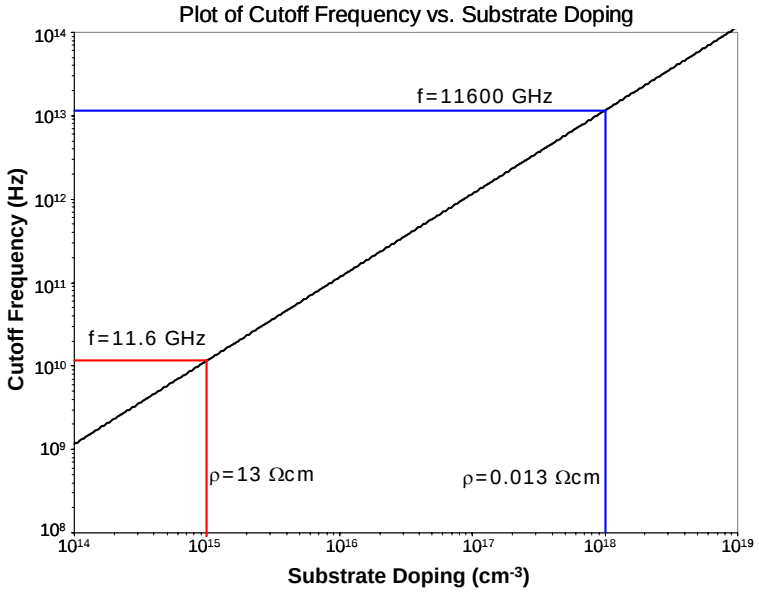


Figure 3-4: Crossover frequency versus substrate doping for silicon.

The model for the substrate depends on the type of substrate used. CMOS IC's are fabricated on one of three types of substrates: epitaxial, non-epitaxial, and silicon-on-insulator.

3.3.1 Epitaxial Wafers

Epitaxial (epi) wafers consist of a lightly-doped (high resistivity) thin layer atop a heavily-doped (low resistivity) bulk. A cross-section is shown in Figure 3-5. Epi wafers are typically used in digital CMOS processes. The low resistivity bulk is required to prevent latch-up [31].

Su et al. [55] have shown that for distances greater than four times the effective thickness of the epi layer, the substrate can be modeled as a single node. Thus, any noise that is injected at one part of the substrate appears at every other node in the circuit. The model for an epi substrate is shown in Figure 3-6. Because of the low

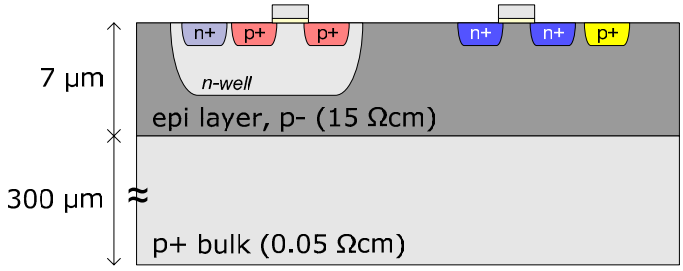


Figure 3-5: Cross-section of an epi wafer.

resistivity bulk, most of the substrate noise propagates in the low resistivity region. For this reason, epi wafers are unacceptable for mixed-signal circuits.

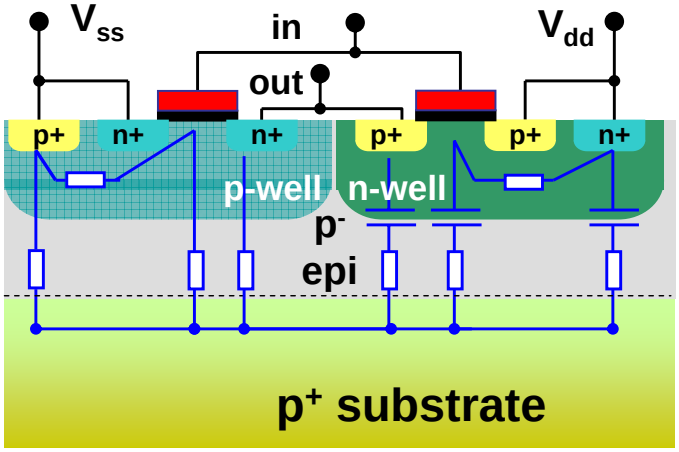


Figure 3-6: Model for an epi wafer [20]. Figure courtesy of G. Van der Plas.

3.3.2 Non-Epitaxial Wafers

Mixed-signal systems are typically fabricated on non-epitaxial (non-epi) wafers. The cross-section is shown in Figure 3-7.

Non-epi wafers are becoming more prevalent as latch-up is no longer of much concern as power supply voltages scale down with each technology generation. Because there is no low resistivity bulk, current flow is more uniform through the substrate; thus, increasing separation distance does increase the amount of isolation between two nodes. Figure 3-9 shows the current flows in both epi and non-epi substrates. For epi substrates, current flow is confined to the low resistivity bulk; whereas, in non-epi

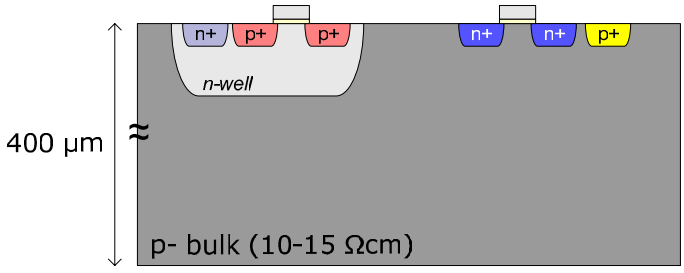


Figure 3-7: Cross-section of a non-epi wafer.

substrates, the current is more uniform throughout the bulk. Figure 3-8 shows the model for a non-epi substrate. Because the substrate does not act as a single node, increasing the separation distance does improve the isolation.

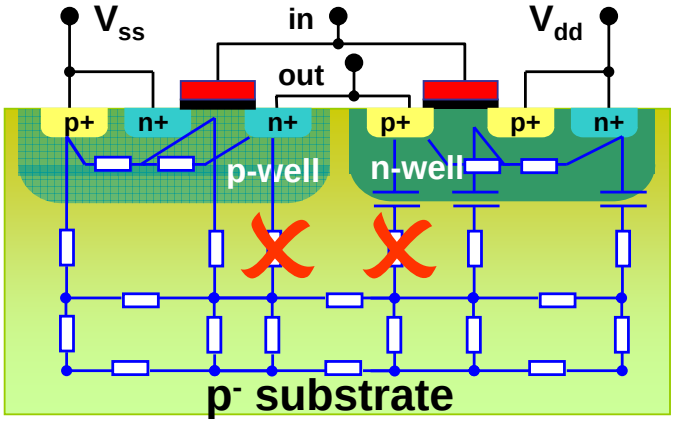
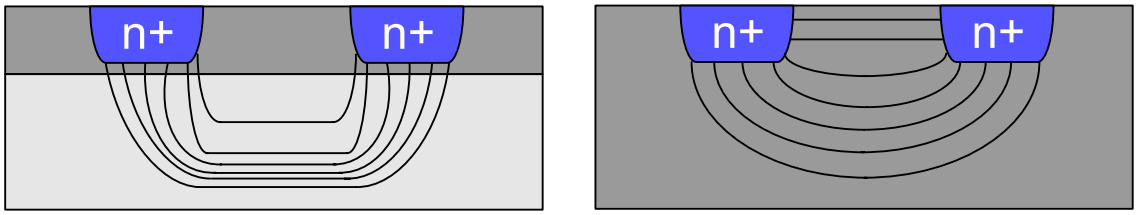


Figure 3-8: Model for a non-epi wafer [20]. Figure courtesy of G. Van der Plas.

Test structures were designed to determine the effect of distance on the attenuation. A top view of the test structure is shown in Figure 3-10. To get a sense for the degree of isolation, the amount of power received at one port when power is injected at another port needs to be measured. This corresponds to the s-parameter measurement S21. S21 is the forward transmission coefficient and essentially represents the power received at port 2 for an incident wave at port 1 and is commonly used in literature as a figure of merit for isolation [25]. Measurements on non-epi wafers show that as the separation increases from 50 μm to 200 μm, the amount of isolation improves by 8 dB as shown in Figure 3-11.

The transmission crosstalk versus frequency was measured between the diodes as a

means of determining the degree of isolation afforded by the various isolation schemes investigated.



(a) Current flow in an epi substrate. (b) Current flow in a non-epi substrate.

Figure 3-9: Current flows in epi and non-epi substrates.

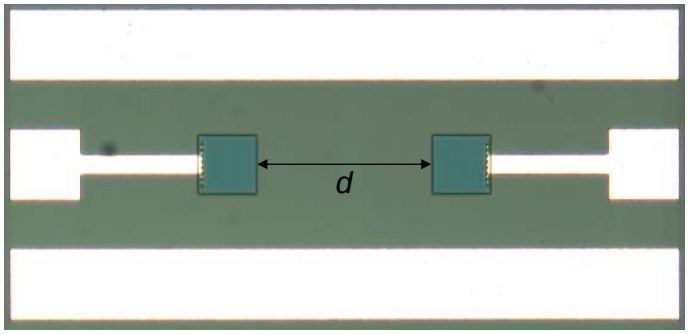


Figure 3-10: Die photo of test structure (top view).

Increasing the substrate resistivity beyond 20 Ω·cm also increases the amount of isolation; however, at higher resistivities, latch-up becomes more of a concern. Furthermore, a 20 Ω·cm substrate is very lowly doped. At the low impurity concentrations required to obtain such low doping levels, even small levels of impurities can alter the resistivity substantially.

3.3.3 Silicon-on-Insulator (SOI) Wafers

Silicon-on-insulator (SOI) substrates are becoming more widely used for their speed improvements through reduced parasitic capacitances. SOI has also demonstrated much potential in reducing substrate crosstalk. Devices are built in thin silicon islands separated from the substrate by a buried oxide layer [47]. Therefore, there is no dc path between silicon islands. A cross-section is shown in Figure 3-12.

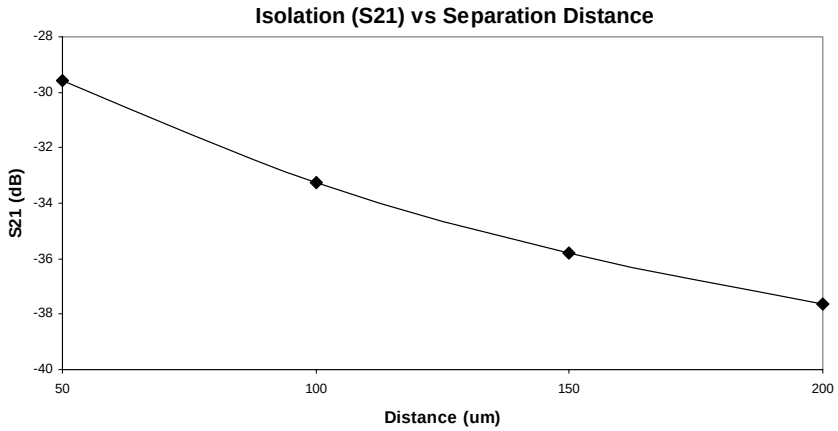


Figure 3-11: Isolation versus separation distance (f=5 GHz).

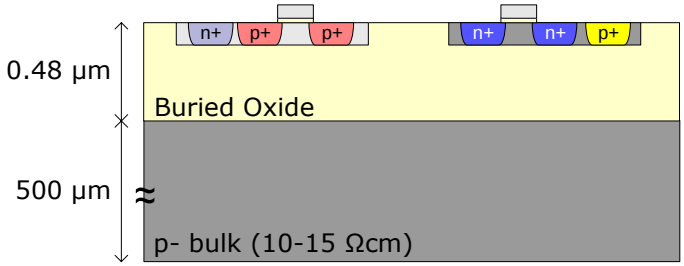


Figure 3-12: Cross-section of an SOI wafer.

At low frequencies, there is very little crosstalk between diffusion regions. However, at higher frequencies, the impedance associated with the buried oxide capacitance reduces thereby limiting its shielding effect. In fact, depending on the geometry of the SOI wafer, SOI yields no advantage in isolation over a non-epi wafer above approximately 27 GHz as shown in Figure 3-13.

An advantage of SOI is that the substrate resistivity can be increased with no latch-up consequences. [47] showed that a 5000 Ω·cm SOI wafer provides almost 20 dB of additional isolation at 1 GHz over a 20 Ω·cm SOI wafer.

3.4 Reception

The last mechanism of substrate noise is the reception mechanism. The paths for reception are analogous to that of injection: *transistor capacitive coupling* and *noise picked up from substrate contacts*. Any noise present on the substrate will capacitively

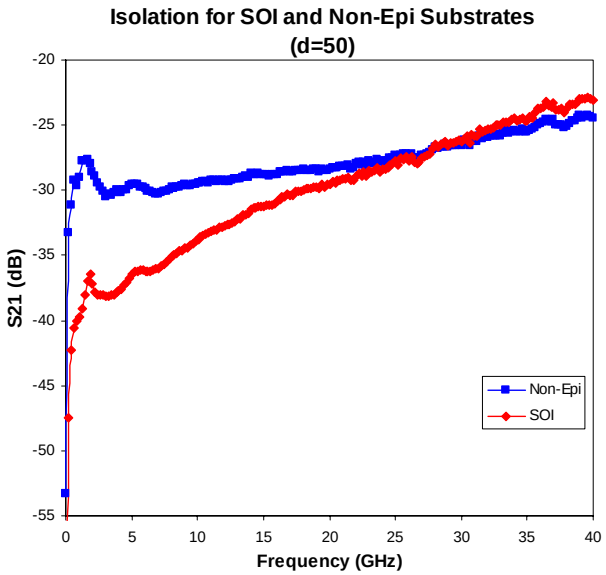


Figure 3-13: Isolation comparison for SOI and non-epi substrates.

couple to the gate, source, and drain nodes. For example, in a low noise amplifier, this noise would directly appear at the output corrupting the desired signal. Any high capacitance nodes will couple noise more easily. An inductor has a large capacitance to substrate and thus can quite easily couple noise from the substrate. This is discussed further in Chapter 5.

Analog circuits usually operate from dedicated supplies as digital supplies tend to be noisy. Analog circuits also bias the bulk terminals of the transistor to power or ground depending on the type of transistor. This again is achieved through low resistance substrate contacts. Any noise that appears on the substrate appears on the analog supply lines because of these contacts. The noise on the supply lines can cause variation in the operating point of the circuit affecting performance parameters such as gain and bandwidth.

Another mechanism for reception is the *backgate effect*. If a voltage between the source and bulk terminals of a transistor is present, then the threshold voltage is changed from its nominal value. The following equation describes this phenomenon [27].

$$V_T = V_{T0} + \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}} \left(\sqrt{|2\phi_f| + V_{SB}} - \sqrt{|2\phi_f|} \right) \tag{3.2}$$

Because the bulk terminal in mixed-signal ICs is fluctuating, the source-bulk voltage fluctuates, in turn causing the threshold voltage to fluctuate. Threshold voltage variations adversely affect not only analog circuits but also digital circuits. Threshold voltage variations in digital clock circuits can result in timing jitter and skew and can change the operating point of analog circuits.

Moreover, through the backgate effect, a gain stage exists between the substrate and the drain of a MOS device. The backgate transconductance and the forward transconductance can be related by the following equation [27].

$$\frac{g_{mb}}{g_m} = \frac{\sqrt{2q\epsilon_s N_A}}{2C_{ox}\sqrt{2\phi_f + V_{SB}}} < 1 \tag{3.3}$$

Noise coupling from the backgate effect is troublesome at all frequencies; whereas, noise from capacitive coupling only becomes significant at higher frequencies.

3.5 Isolation Structures

Isolation structures fabricated in the substrate itself reduce substrate noise by altering the propagation mechanism. Different guard ring configurations implemented in both non-epi and SOI substrates are discussed in this section. Results of test structures fabricated by Chuan Seng Tan in the Microsystems Technology Laboratories' 0.5 μm CMOS process on both non-epi and SOI substrates are presented. Both substrates had a bulk resistivity of 10-15 Ω·cm. Moreover, 3-D integration is explored for its potential to minimize substrate noise.

3.5.1 Non-Epi Substrates vs. SOI

The buried oxide of SOI substrates provides additional shielding between noise injection points and the underlying substrate. In order for noise to propagate from one location to another, noise must capacitively couple through the buried oxide to the

underlying silicon where it can then propagate to another location. The noise then capacitively couples into sensitive nodes.

At low frequencies, the capacitive effect from the buried oxide results in approximately 12 dB of additional isolation. Figures 3-14(a)-3-14(d) compare the isolation afforded by SOI and non-epi over four different separation distances.

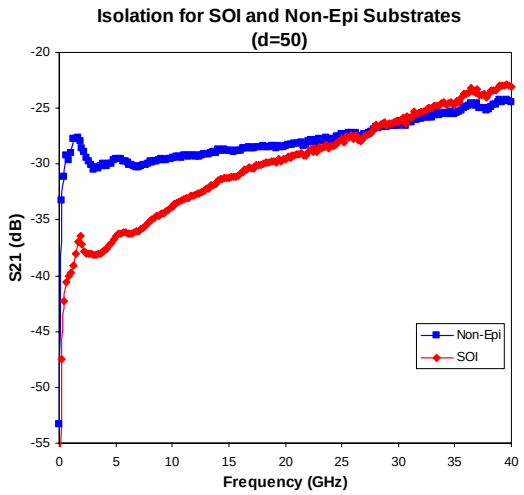
At higher frequencies, the SOI isolation curves coincide with the non-epi because the impedance of the buried oxide shorts out. The frequency at which the SOI and non-epi isolation curves merge is determined by the substrate doping and the thickness of the buried oxide. Above this crossover frequency, SOI has no advantage over bulk silicon.

3.5.2 Single Guard Ring

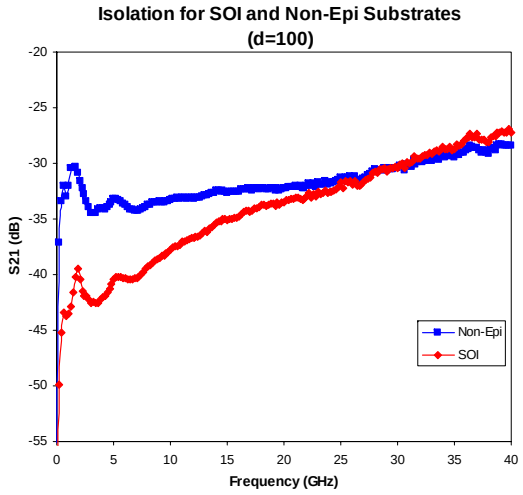
Guard rings can attenuate substrate noise by sinking the noise current to a low impedance ground. The cross-section of the single guard ring test structure used is shown in Figure 3-15. The die photo showing the top view of the test structure is shown in Figure 3-16.

The amount of isolation afforded by guard rings for both non-epi and SOI substrates is shown in Figures 3-17(a)-3-17(d). This data was extracted from a structure with a 10 μm wide p+ guard ring. Over a wide frequency range, these guard rings provide approximately 5 dB of additional attenuation over a structure with no guard ring.

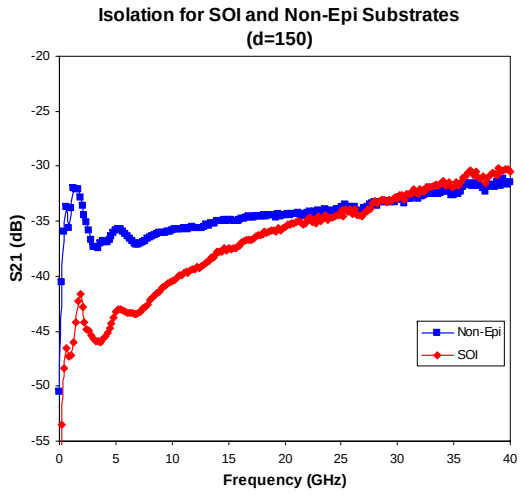
Even in SOI, guard rings provide approximately 5 dB of additional isolation independent of frequency. In SOI, the implanted region of the guard ring is present only in the thin silicon layer above the buried oxide as depicted in Figure 3-15(b). Because guard rings have an effect in SOI, this indicates that a significant portion of the noise current flows in through the device layer.



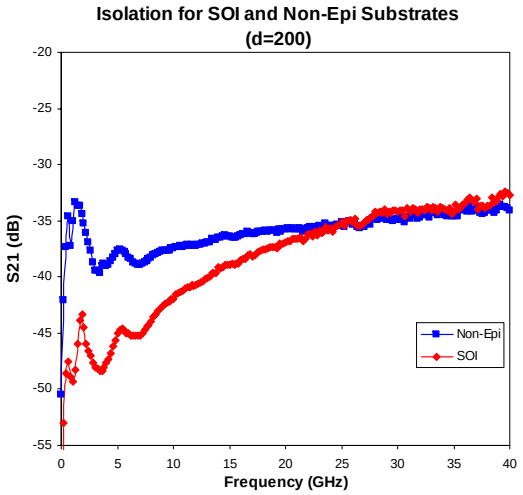
(a) d=50 μm.



(b) d=100 μm.

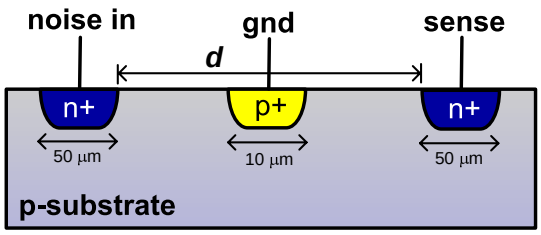


(c) d=150 μm.

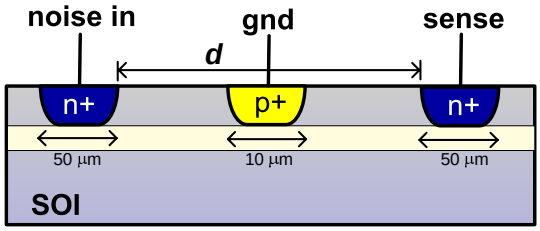


(d) d=200 μm.

Figure 3-14: Isolation comparison for SOI and non-epi substrates. Separation distance between two n+ contacts is varied.



(a) Non-epi.



(b) SOI.

Figure 3-15: Cross-sections of single guard ring test structures.

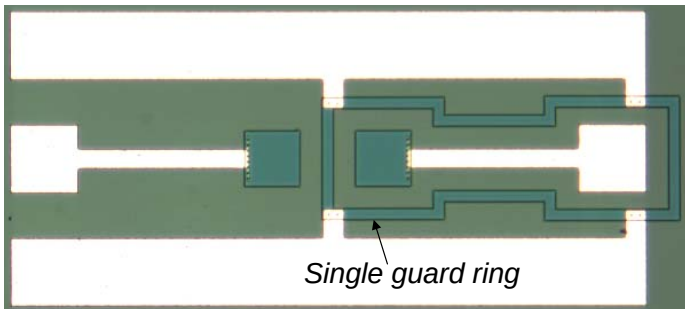


Figure 3-16: Die photo of single guard ring test structure (top view).

3.5.3 Double Guard Rings

Double guard rings consist of two guard rings: one surrounding the noisy portion of the circuit and another surrounding the sensitive portion of the circuit. Figure 3-18 shows the cross-section of the double guard ring test structure. Figure 3-19 shows the die photo of the double guard ring test structure.

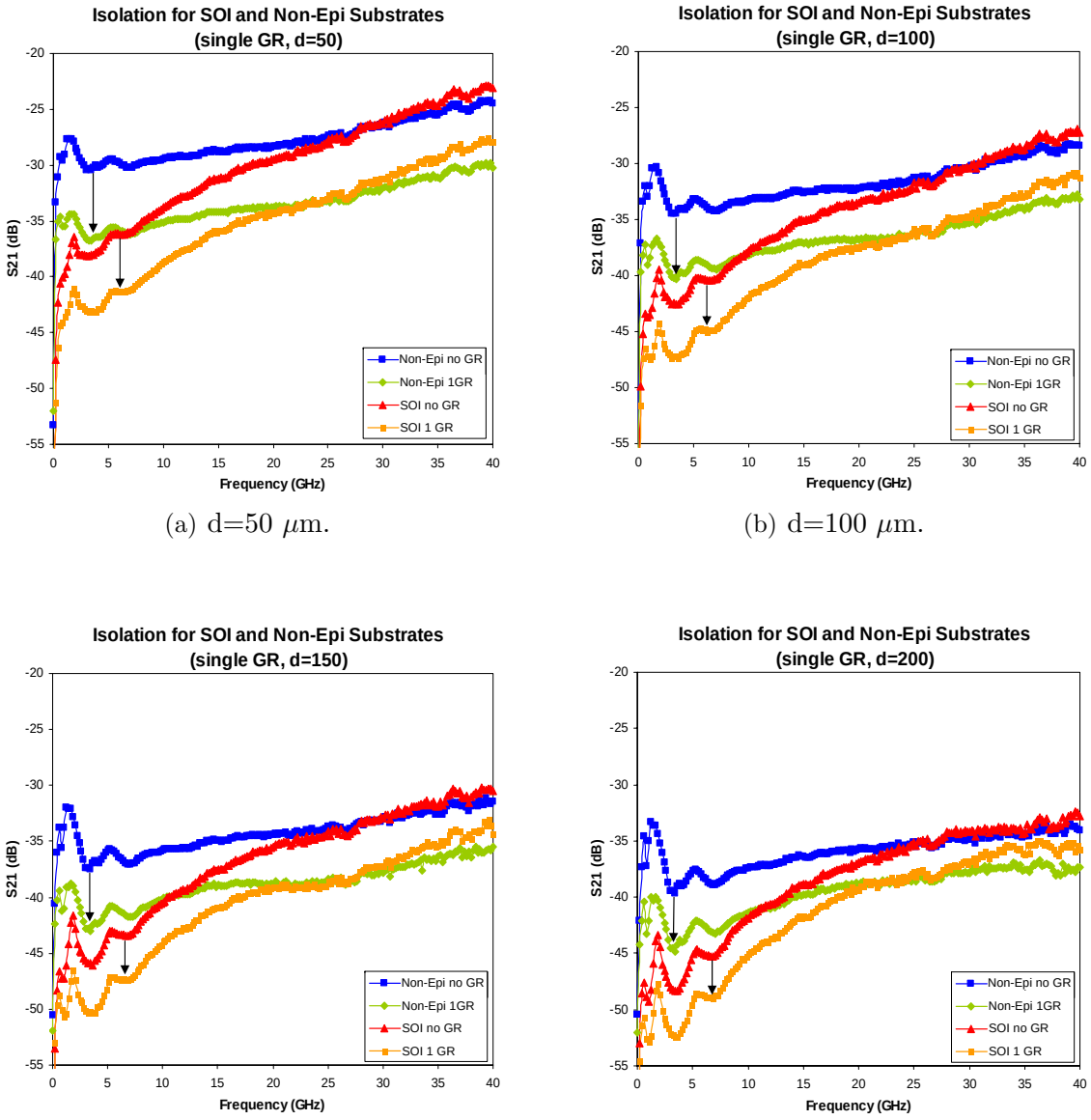
The amount of isolation afforded by double guard rings for both non-epi and SOI substrates is shown in Figures 3-20(a)-3-20(d). The addition of the second guard ring provides another 5 dB of attenuation independent of frequency.

3.5.4 Three-Dimensional Integration

Three-dimensional integrated circuits (3-D ICs) consist of multiple active silicon layers connected through front and backside contacts. A cross-section of a typical 3-D IC is shown in Figure 3-21.

Various approaches exist to fabricate 3-D ICs; the most prevalent are recrystallization and wafer bonding using oxide or copper as the bonding material. The technology being explored at MIT is copper wafer bonding and is discussed here [23].

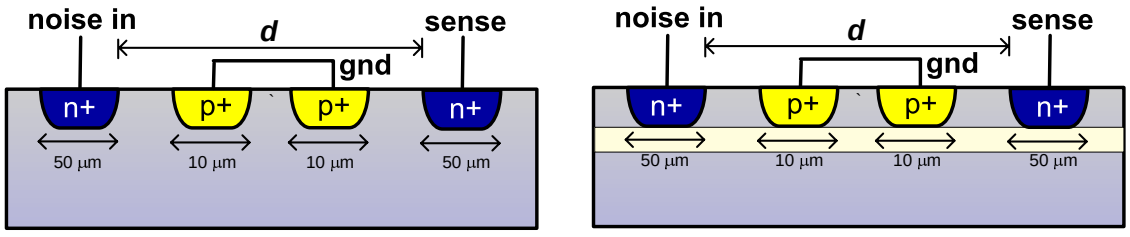
Each wafer is independently fabricated using conventional processing steps. For a silicon process, the starting layer is bulk silicon. Each subsequent layer is fabricated using SOI wafers. The underlying silicon of the SOI wafers is thinned back to the buried oxide. The resulting wafer is only 0.7 μm thick compared to 600 μm for the bulk silicon layer. Thinned wafers are used to ease the aspect ratio requirement for



(a) d=50 μm. (b) d=100 μm.

(c) d=150 μm. (d) d=200 μm.

Figure 3-17: Isolation comparison for SOI and non-epi substrates with a single guard ring. Separation distance between two n+ contacts is varied.



(a) Non-epi. (b) SOI.

Figure 3-18: Cross-sections of the double guard ring test structure.

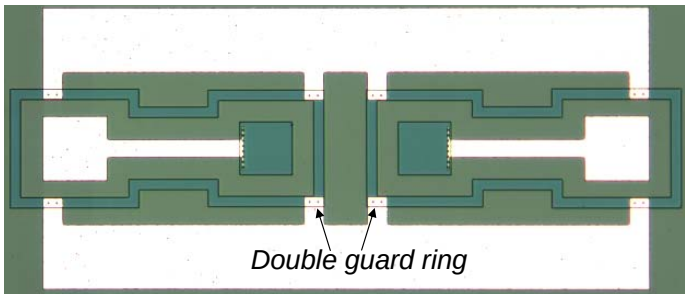
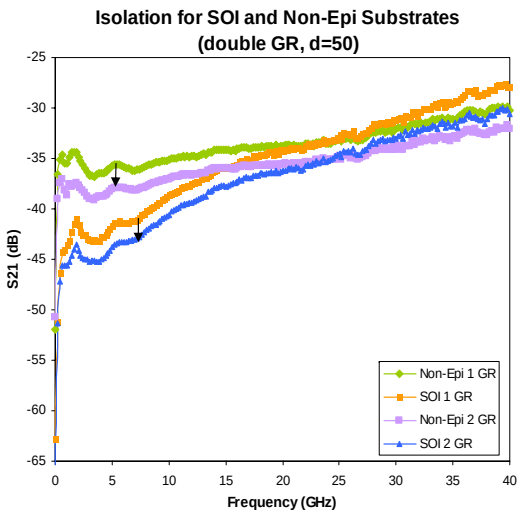


Figure 3-19: Die photo of double guard ring test structure (top view).

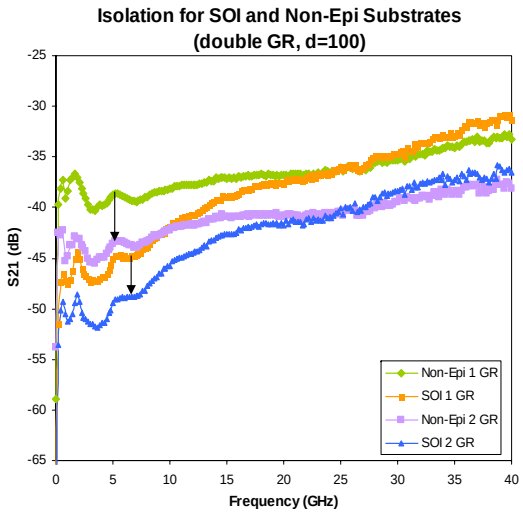
interlayer vias. After each wafer is processed, vias are patterned, and the two wafers are bonded using copper.

3-D integration exhibits much potential for mixed-signal systems. First, analog and digital systems could be designed on separate substrates. The resistive connection through the substrate would be broken altering the noise propagation mechanism. Any noise injection would occur through the bonding interface. For example, interconnect associated with the bottom device layer could couple noise into the substrate above. Simulations using HFSS [3], a 3-D field solver, were performed to determine the amount of isolation achievable with 3-D integration. The structures used in the simulation are shown in Figure 3-22. A Faraday cage [59] test structure was included to compare the results of the simulations to measured data.

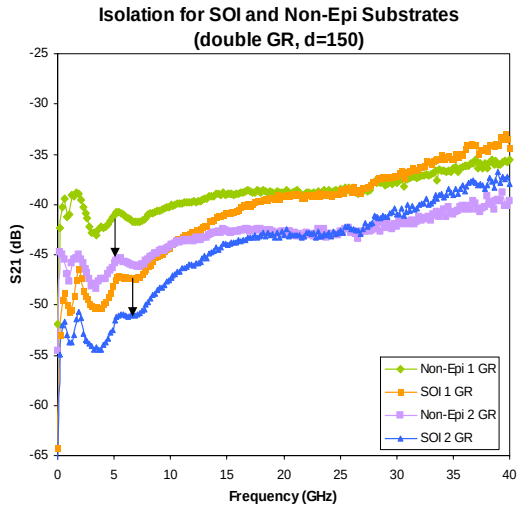
Two different types of simulations were performed to determine the effect of the bonding material on the isolation. One set of simulations assumed a floating copper bonding interface while the other assumed oxide as the bonding material. The family of curves generated for each set of simulations correspond to a change in the geometry of the test structure as shown in Figures 3-22(b) and 3-22(c). The use of a copper bond provides between 10 and 20 dB of isolation (depending on the geometry) over an oxide bond. Figure 3-23 shows the results of the simulations. The improved isolation from the copper bond is due to the role of fringing fields. Field lines originating on the metal line of the bottom device layer terminate on the copper bond rather than on the substrate. This reduces the coupling between the metal line and the top substrate. The oxide bond cannot provide this termination. For the wider bonding



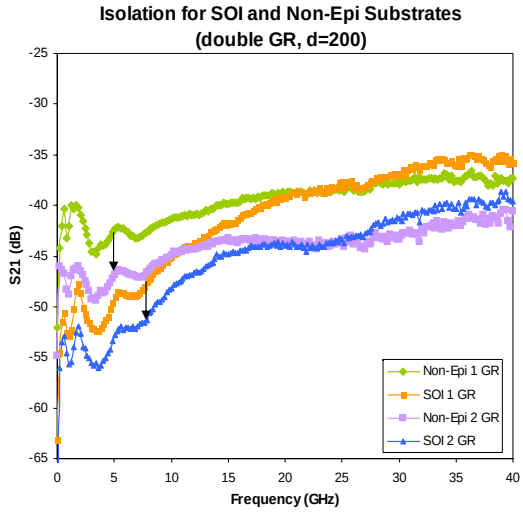
(a) d=50 μm.



(b) d=100 μm.



(c) d=150 μm.



(d) d=200 μm.

Figure 3-20: Isolation comparison for SOI and non-epi substrates for a double guard ring. Separation distance between two n+ contacts is varied.

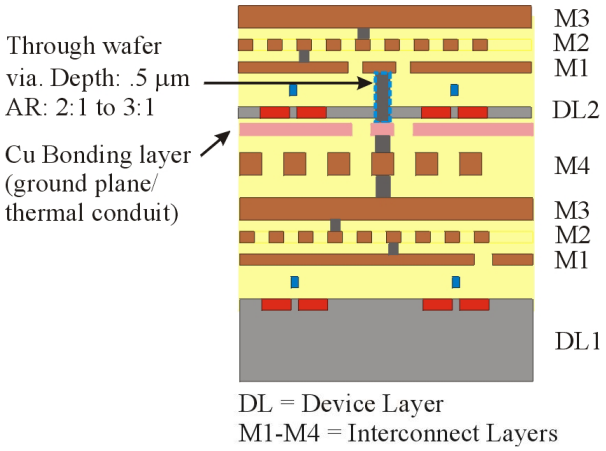
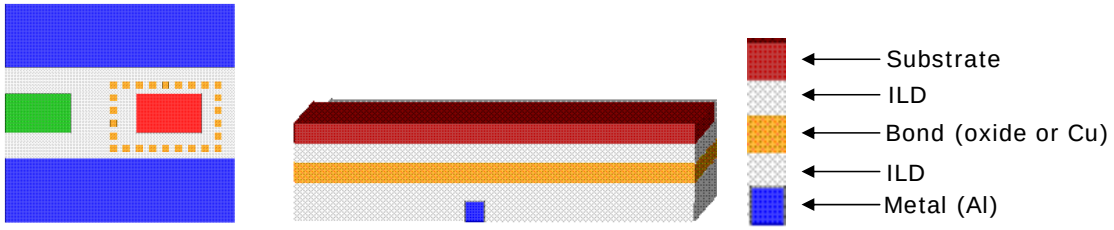


Figure 3-21: Cross-section of a 3-D IC using wafer bonding. Figure courtesy of A. Fan [23].



(a) Faraday cage test structure.

(b) One type of 3-D structure.

(c) Another 3-D structure.

Figure 3-22: Test structures used in the HFSS simulations.

interface geometries, more fringing fields terminate on the bond resulting in improved isolation.

As much as 85 dB of isolation can be achieved by exploiting the conductive nature of the copper bond by grounding it. This results in near perfect isolation between two layers.

Data from measured structures fabricated in Lincoln Lab's 0.18 μm FDSOI process was used to verify the simulation results. The cross-sections of the measured test structures are shown in Figure 3-24.

Figure 3-24(a) represents the test structure used to measure the isolation achievable with an oxide bonding process. Figure 3-24(b) represents the test structure for a copper bonding process. In this test structure, the bond pad is the same size as

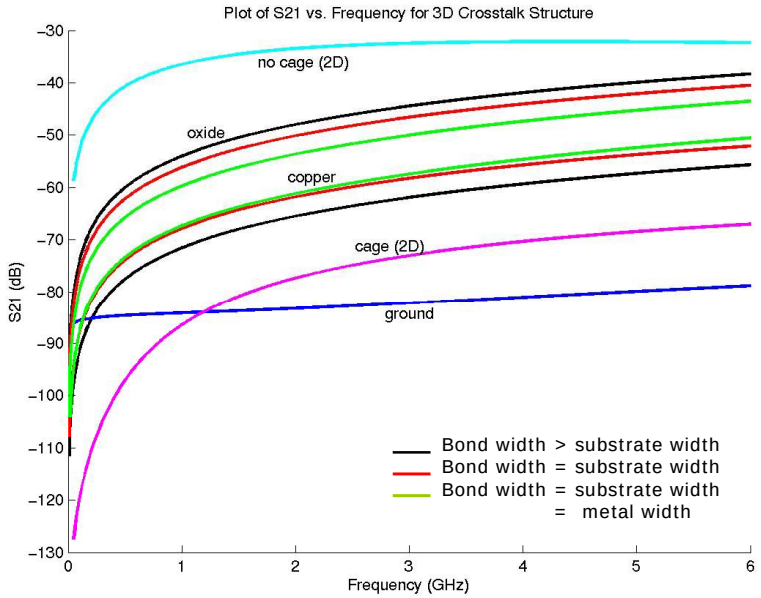
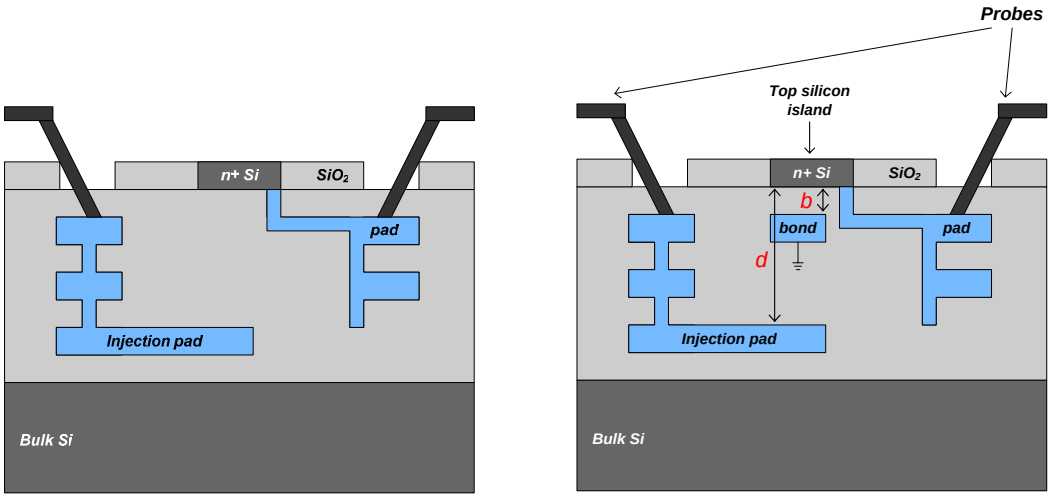


Figure 3-23: Isolation of various test structures. The top curve represents the S21 for a structure with no isolation. The curve labeled Faraday cage was generated for the structure in Figure 3-22(a). The remaining curves represent the S21 for the 3-D test structures shown in Figures 3-22(b) and 3-22(c).

both the injection pad and the top silicon island. Furthermore, two variables could be varied. The first is the distance between the injection pad and the top substrate, d. The second is the distance between the bond and the top substrate, b. Figure 3-25 shows the measured isolation for both structures.

Below 5 GHz, the copper bonding approach provides almost 20 dB of additional isolation over the oxide bonding structure verifying the results of the HFSS simulations. When the parameter d is increased, the amount of isolation improves as the noise source is farther away from the sensing location. When the parameter b is increased, there is a negligible effect on the amount of isolation. This indicates that the distance between the bond and the top substrate has no effect on isolation. To achieve greater levels of isolation with 3-D integration, the bonding interface should be made as wide as possible. The results of the HFSS simulations indicate that near perfect isolation is achievable for a copper bonding layer that is the width of the entire die.



(a) Oxide bonding structure (Reference).

(b) Copper bonding structure.

Figure 3-24: 3-D measurement test structures.

3.6 Summary

The three mechanisms governing substrate noise in mixed-signal systems were discussed. Noise is injected into the substrate through power and ground noise, switching inputs and outputs, and through impact ionization currents. Silicon is a semiconducting material that allows noise to easily propagate from one location to another. Analog circuits pick up substrate noise through mechanisms analogous to injection. The isolation afforded by different guard ring geometries was also discussed. 3-D integration was shown to exhibit much potential for use in mixed-signal systems. It is even possible to achieve near perfect isolation.

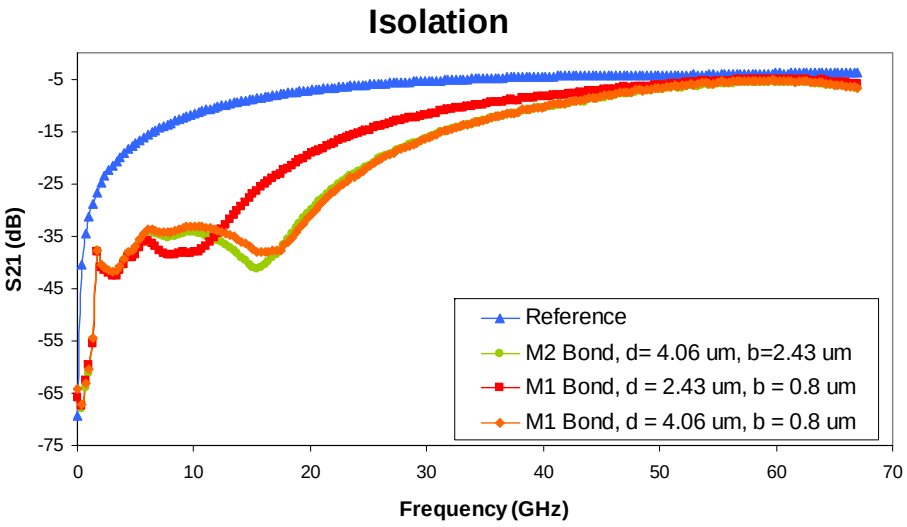


Figure 3-25: Measured isolation of test structures in Figure 3-24.

Chapter 4

Isolation Requirement for the Integration of a Microprocessor with a Low Noise Amplifier

4.1 Overview

In wireless mixed-signal systems, the problem of substrate noise is especially severe as the effectiveness of traditional isolation techniques tends to fail at RF frequencies. Figure 4-1 shows the block diagram of a direct conversion receiver. The digital system implementing the baseband processing generates the most noise that is often on the order of tens of millivolts. Typically a digital signal processor (DSP) or microprocessor implements this function. The most sensitive components of the RF front end are the low noise amplifier (LNA) and the voltage controlled oscillator (VCO).

The amount of isolation required to integrate a microprocessor with an LNA is discussed in this chapter. In Section 4.2, background on the LNA is presented. Section 4.3 discusses challenges in integrating the LNA with a microprocessor. Section 4.4 discusses noise coupling paths into the LNA. Section 4.5 derives the amount of isolation required to integrate three different wireless standards with a Pentium® 4 microprocessor.

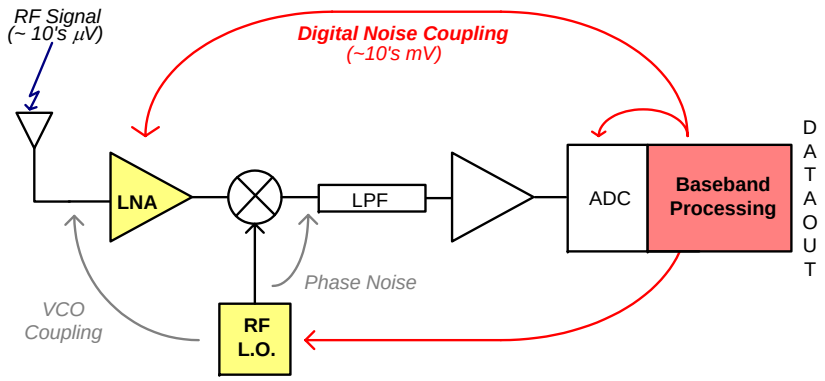


Figure 4-1: Block diagram of a direct conversion receiver.

4.2 Low Noise Amplifier

The LNA is a narrowband circuit that applies gain to the input signal over a narrow frequency range. A typical single-ended LNA is shown in Figure 4-2.

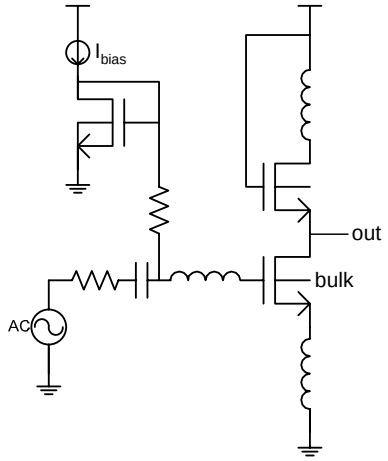


Figure 4-2: Single-ended LNA schematic [34].

Depending on the wireless standard being implemented, the LNA has to be able to amplify input signals that are on the order of microvolts. Table 4.1 shows the receiver requirements for three different wireless standards. The receiver sensitivity corresponds to the minimum signal that the receiver must be able to detect.

Substrate noise generated by digital circuits can be on the order of millivolts; thus, the LNA has to be able to amplify the received signal in the presence of noise several orders of magnitude larger.

Table 4.1: Receiver sensitivities for different wireless standards.

	Bluetooth [6]	802.11b [4]	Cellular/PCS [58]
Sensitivity	-70 dBm	-76 dBm	-120 dBm
Sensitivity	70.7 μV	35.4 μV	0.22 μV
Frequency Range	2.402 GHz - 2.48 GHz	2.4 GHz - 2.483 GHz	824 MHz - 894 MHz 1.85 GHz - 1.99 GHz

4.3 Integration with a Microprocessor

In this chapter, the integration of LNAs implementing three different wireless standards with a Pentium® 4 microprocessor is considered. The substrate noise performance of the Pentium® 4 was published in [24].

The Pentium® 4 operates from a 1.5 V power supply resulting in a maximum power dissipation of 55 W. It consists of 104 million transistors switching at a 1 GHz clock frequency. At maximum power dissipation, the noise on the substrate is 190 mV_{rms}. Under typical operating conditions, the power dissipation is 15 W resulting in 100 mV_{rms} of substrate noise. This noise is spread over the entire frequency band; however, most power is concentrated at the 1 GHz clock frequency and its harmonics as shown in Figure 4-3.

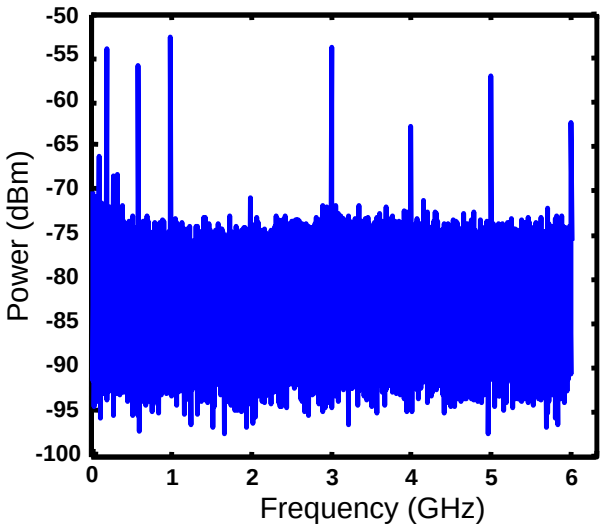


Figure 4-3: Substrate noise spectrum of the Pentium® 4 microprocessor operating with a 1 GHz clock. From [24].

The noise spectrum consists of power from the clock generation and distribution

network and power from random switching events that set the noise floor. Because most of the noise power is concentrated at the clock and its harmonics, frequency planning is essential to lessen the problem of substrate noise. Figure 4-4 shows the consequence of poor frequency planning. Shown in red, the received RF signals lies in the same band as one of the clock harmonics. As the RF frequency is predetermined and set, the clock frequency must be chosen such that the fundamental and its harmonics lie outside of the frequency range of interest. This is shown in green in Figure 4-4. With good frequency planning, the minimum noise possible couples into the LNA.

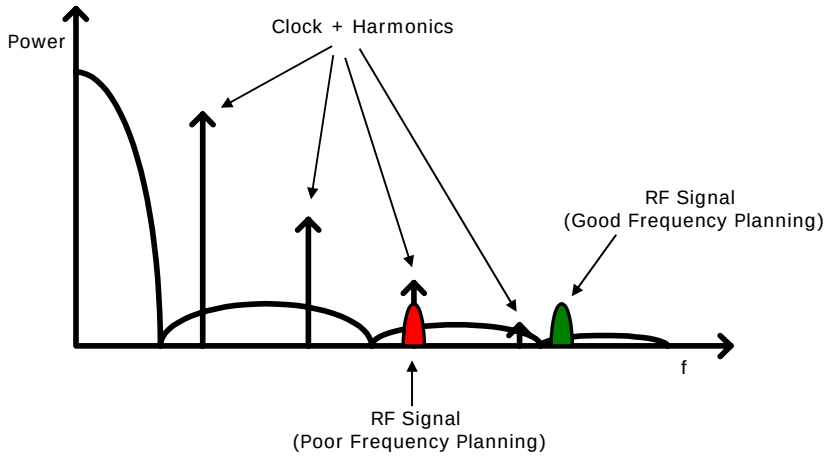


Figure 4-4: Frequency Planning. An example of poor frequency planning is shown in red. Good frequency planning is shown in green.

For the analysis in this chapter, good frequency planning is assumed; thus, the noise coupled is determined by random switching events.

4.4 Noise Coupling Paths

Noise can couple into analog circuits through several paths, which were described in detail in Chapter 3. If separate ground connections are assumed, the most significant noise coupling path for the LNA is through the backgate effect [60]. Through the backgate effect, any noise appearing at the bulk node of a device will experience a gain proportional to the backgate transconductance, g_{mb}. g_{mb} in turn is proportional

to the forward transconductance, g_m, and thus also the overall gain of the circuit. The signal gain of the LNA depends on g_m while the gain experienced by the noise depends on g_{mb}. Thus, the ratio g_m/g_{mb}, which depends on the bias point of the circuit, sets the signal to noise ratio.

4.5 Isolation Requirement

The 190 mV_{rms} substrate noise signal is spread over the entire frequency band. The only noise that will corrupt LNA performance is the noise that appears in-band. Thus, the noise in the frequency band of interest need only be considered. Because the substrate noise is several orders of magnitude larger than that of the received signal, isolation is required. In order to yield a bit error rate (BER) less than 10^{-9}, a signal to substrate noise ratio (SsNR) of at least 20 dB is necessary [24]. The amount of isolation required to meet this BER specification is derived for three different wireless standards: Bluetooth, 802.11b, and cellular/PCS.

4.5.1 Isolation Requirement for Bluetooth

Bluetooth was chosen for this analysis to represent a low performance wireless system. It can operate at either 2.4 GHz or 5.2 GHz. Both bands are considered here. When integrating the LNA of a Bluetooth receiver with the Pentium® 4, only the noise in the 50 MHz band around 2.4 GHz and 5.2 GHz needs to be considered.

Integrating the substrate noise over the 50 MHz bandwidth around 2.4 GHz yields an in-band substrate noise of 7.76 mV_{rms} [35]. In order to meet the BER specification, the SsNR must be at least 20 dB. Before any LNA amplification or isolation, the SsNR is -40.8 dB at 2.4 GHz. Through a combination of LNA gain and isolation, the SsNR of -40.8 dB must be transformed to 20 dB.

The SsNR can be improved by increasing the signal amplitude and reducing the substrate noise. By increasing the LNA gain, the signal amplitude increases; however, the noise gain also increases. The input signal sees the full amplification of the LNA gain. However, the substrate noise experiences only a fraction of the LNA gain.

This fraction depends on the g_m/g_{mb} ratio and thus on the bias point. For example, through simulation, it is observed that when the LNA gain is 10 dB, the gain through the bulk terminal is only 1 dB. When the LNA gain is 20 dB, the gain through the bulk terminal increases to 2 dB.

With an LNA gain of 20 dB, the SsNR becomes -22.8 dB. To further increase the SsNR, the only other option is to reduce the substrate noise by incorporating isolation. To meet the BER specification, approximately -42.8 dB of isolation is required assuming an LNA gain of 20 dB. The use of differential circuits provides approximately 20 dB of isolation [24] resulting in -22.8 dB of isolation that must come from technology. These results are summarized in Table 4.2. The amount of isolation required at 5.2 GHz is also derived and summarized in Table 4.2.

Table 4.2: Isolation required to integrate a Bluetooth receiver with the Pentium® 4.

	LNA Gain	SsNR after LNA	Isolation Required	Isolation from Technology
f=2.4 GHz	10 dB	-31.8 dB	-51.8 dB	-31.8 dB
	20 dB	-22.8 dB	-42.8 dB	-22.8 dB
f=5.2 GHz	10 dB	-29.3 dB	-49.3 dB	-29.3 dB
	20 dB	-20.3 dB	-40.3 dB	-20.3 dB

The various types of isolation techniques were discussed in Chapter 3. The isolation afforded by several standard isolation techniques is summarized in Table 4.3.

Table 4.3: Isolation at 2.4 GHz for different isolation techniques [16][24][59].

Technique	Isolation
Guard ring (w = 100 μm)	-28 dB
Guard ring (w = 300 μm)	-25 dB
Triple well	-25 dB
Deep n-well	-50 dB
Faraday cage	-75 dB
3-D Integration	-85 dB

In order to integrate a Bluetooth receiver operating at 2.4 GHz with the Pentium® 4, approximately -42.8 dB of isolation is required. The use of differential circuits

relaxes that requirement to -22.8 dB. Referring to Table 4.3, all standard techniques provide enough isolation to permit this integration. In fact, Ericsson demonstrated a 0.18 μm single-chip Bluetooth receiver with integrated digital baseband processing with the use of a 300 μm wide guard ring surrounding the RF front end [57]. Figure 4-5 shows the die photo with the guard ring marked.

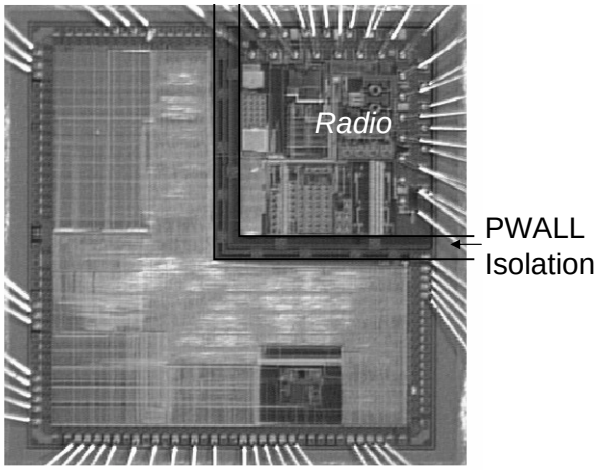


Figure 4-5: Die photo of Ericsson's single-chip Bluetooth solution. The PWALL isolation is simply a 300 μm wide guard ring [57].

4.5.2 Isolation Requirement for 802.11b

Using the analysis presented in Section 4.5.1, an isolation requirement to integrate an 802.11b receiver with the Pentium® 4 can be derived. Table 4.4 summarizes these results.

Table 4.4: Isolation required to integrate an 802.11b receiver with the Pentium® 4.

	LNA Gain	SsNR after LNA	Isolation Required	Isolation from Technology
f=2.4 GHz	10 dB	-37.8 dB	-57.8 dB	-37.8 dB
	20 dB	-28.8 dB	-48.8 dB	-28.8 dB
f=5.2 GHz	10 dB	-35.3 dB	-55.3 dB	-35.3 dB
	20 dB	-26.3 dB	-46.3 dB	-26.3 dB

The isolation required for an 802.11b system is larger than that for Bluetooth because of the more stringent sensitivity requirement. Through careful design of the

guard ring geometry, guard rings could provide sufficient isolation for an 802.11b system.

4.5.3 Isolation Requirement for Cellular/PCS

The results of applying the same analysis to a cellular/PCS system is presented in this section. The cellular/PCS standard was chosen as it represents a very high performance wireless system. While the sensitivities of Bluetooth and 802.11b are similar, the cellular/PCS receiver has a much more stringent sensitivity. This leads to a dramatic increase in the amount of isolation required. Through a combination of LNA gain and isolation, a SsNR of -92 dB must be transformed to at least 20 dB to meet the BER specification. Table 4.5 summarizes the results for a cellular/PCS system.

Table 4.5: Isolation required to integrate a cellular/PCS system with the Pentium® 4.

	LNA Gain	SsNR after LNA	Isolation Required	Isolation from Technology
f=900 MHz	10 dB	-84 dB	-104 dB	-84 dB
	20 dB	-75 dB	-95 dB	-75 dB
f=1.9 GHz	10 dB	-83 dB	-103 dB	-83 dB
	20 dB	-74 dB	-94 dB	-74 dB

The isolation required to integrate a cellular/PCS receiver with the Pentium® 4 is considerably larger than for both Bluetooth and 802.11b. Table 4.6 summarizes the amount of isolation for various isolation techniques at 900 MHz. Even though the amount of isolation improves with reducing frequency, the isolation afforded by standard isolation techniques is still not sufficient for such a high performance application. Deep n-well is considered to be the most state of the art isolation technique available today. However, it still does not provide enough isolation for a cellular/PCS system. More advanced techniques such as the Faraday cage [59] and 3-D integration [23] will have to be explored as a possible solution.

Table 4.6: Isolation at 900 MHz for different isolation techniques [16][24][59].

Technique	Isolation
Guard ring (w = 100 μm)	-30.5 dB
Guard ring (w = 300 μm)	-31.3 dB
Triple well	-30 dB
Deep n-well	-50 dB
Faraday cage	-88 dB
3-D Integration	-85 dB

4.6 Summary

In this chapter, the amount of isolation required in order to integrate three receivers implementing different wireless standards with an Intel Pentium® 4 microprocessor is derived. Frequency planning is essential to minimizing the in-band noise that couples from the microprocessor to the LNA. For low performance wireless systems such as Bluetooth, approximately -22.8 dB of isolation is required from technology. Guard rings provide enough isolation to implement a single-chip solution. However, the stringent sensitivity requirement of high performance systems such as cellular/PCS require the use of more advanced isolation technologies in order to provide the -75 dB of isolation that is required to implement a single-chip solution. Standard techniques such as guard rings and triple wells do not provide enough isolation. Even the most advanced isolation structure in production today, the deep n-well, is not sufficient. More advanced techniques such as the use of an on-chip Faraday cage and 3-D integration will need to be explored as possible solutions.

Chapter 5

The Effect of Substrate Noise on the Voltage Controlled Oscillator

5.1 Overview

The second component of the RF front end that is particularly sensitive to substrate noise is the voltage controlled oscillator (VCO). An ideal oscillator output consists of a single tone with power only at the carrier frequency as shown in Figure 5-1. However, due to noise in the devices themselves, power around the carrier frequency is present. This is known as phase noise.

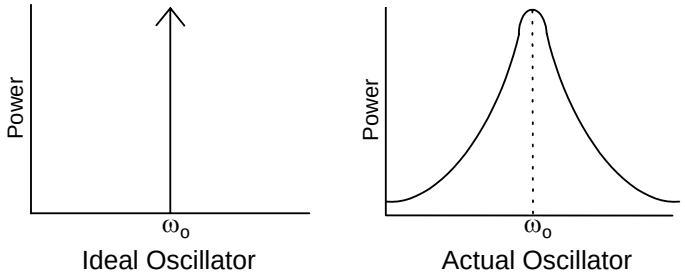


Figure 5-1: Spectrums of an ideal and real VCO.

Cross-coupled transistors loaded with an LC tank form the core of most RF VCOs. This topology offers better phase noise performance over ring oscillator based configurations. For this reason, LC tank VCOs are considered in this work.

The effect of substrate noise on the phase noise of a VCO is studied experimentally in this chapter [19]. Section 5.2 discusses how noise couples into the VCO. Section 5.3 shows that through the substrate, multiple VCOs on a single chip an interfere with each other. Section 5.4 describes the test chip that was designed for this investigation. Section 5.5 introduces the experimental setup. Section 5.6 discusses the effect of VCO bias current and guard rings on the substrate noise performance of the VCO. Section 5.7 discusses how, in the extreme, substrate noise can induce injection locking. Finally, Section 5.8 discusses the effect of low frequency noise (10 MHz) on the VCO output spectrum.

5.2 Noise Coupling Paths

The phase noise of a VCO is largely determined by device-level noise such as thermal noise and 1/f noise. The output spectrum of a VCO in the presence of only device level noise is shown in Figure 5-2.

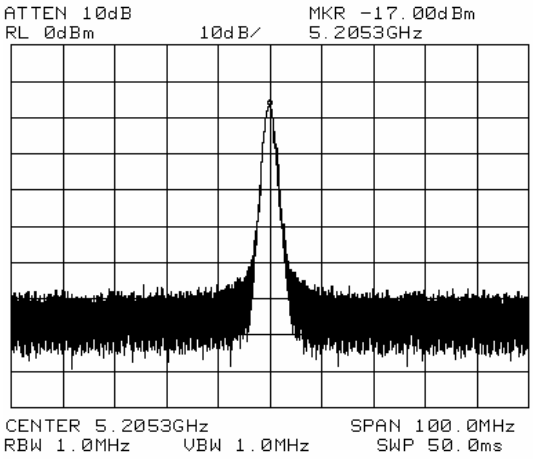


Figure 5-2: Output spectrum of a VCO with only device level noise.

Substrate noise, however, can also contribute to the phase noise of a VCO. There are several coupling paths through which substrate noise can couple into a VCO. Any noise in the power and ground lines of the VCO will directly affect the phase noise. By using separate analog and digital supplies, the amount of noise in the VCO supply lines can be minimized. However, even with the use of dedicated supplies, digital

supply noise can still couple to VCOs through the substrate. Digital power supply noise appears on the substrate through substrate contacts in the digital system. This noise then propagates through the shared substrate to the sensitive VCOs. Depending on the technology, the noise can then couple resistively to the NMOS backgate or capacitively through the n-well to the PMOS backgate. In addition, noise can couple capacitively through the inductors and varactor bulk node [54]. Substrate noise that enters into the VCO and results in a voltage fluctuation on the varactor terminals will result in modulation of the carrier frequency. Any noise in the VCO bias current and control voltage will also result in phase noise. Figure 5-3 highlights all the possible substrate noise coupling paths into a VCO.

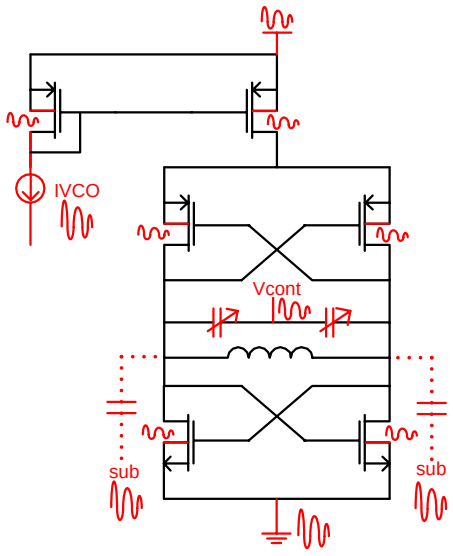


Figure 5-3: All possible substrate noise coupling paths into a VCO.

For the study presented in this chapter, the technology used included triple wells. A cross-section of NMOS and PMOS devices in a triple well technology is shown in Figure 5-4.

Triple wells mitigate coupling to the NMOS and PMOS backgates through the additional capacitances presented by the wells thereby eliminating several coupling paths. Care was taken to minimize noise on the bias current lines and on the control voltages. The triple well eliminates the coupling path through the backgate effect. The coupling paths into a VCO using triple wells is shown in Figure 5-5.

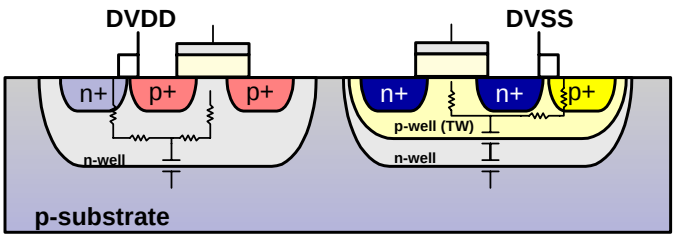


Figure 5-4: Cross-section of NMOS and PMOS devices in a triple well technology.

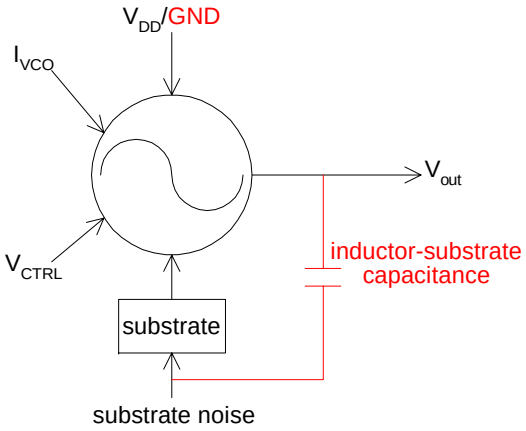


Figure 5-5: Coupling paths into a VCO using triple wells. The most significant coupling paths are highlighted in red.

From the work described in this chapter, it was determined that the most significant coupling paths are through ground noise pickup and the inductor to substrate capacitance which are highlighted in red in Figure 5-5.

5.3 VCO to VCO Interference

Through the same noise coupling paths, noise can be injected into the substrate as a result of VCO operation. The noise injected appears at the VCO carrier frequency as shown in Figure 5-6. If multiple VCOs are integrated on a single chip, interference between VCOs can result.

For multi-standard radios [61] and wireless gigabit LAN systems [29], multiple receivers and thus multiple VCOs are integrated on the same chip. For wireless gigabit LAN, multiple receive paths are used to implement the function. Each path

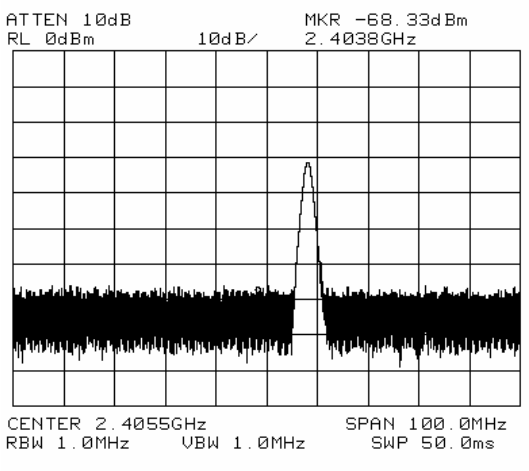


Figure 5-6: Noise coupled into the substrate from a VCO with $f_{carrier}$=2.413 GHz.

could select a different channel resulting in slightly offset VCO carrier frequencies. For example, consider a VCO operating at 2.413 GHz (VCO1) to select a particular 802.11b channel. Figure 5-7(a) shows the output spectrum. The noise that appears at the output of VCO2 when powered off as a result of coupling from VCO1 is shown in Figure 5-7(b). VCO2 in another receive path operates at 2.4038 GHz to select another channel 9.2 MHz away. Its output spectrum is shown in Figure 5-7(c). If both VCO1 and VCO2 are operating, interference between the two corrupts both output spectrums. The output of VCO2 as a result of this interference is shown in Figure 5-7(d).

For multi-standard radios such as those shown in Figure 5-8, similar interference occurs as a result of intermodulation. The direct noise component will not appear in band; however, intermodulation products can appear in band.

For example, consider the integration of a GPS receiver operating at 1.5 GHz, a cellular receiver operating at 900 MHz, and an 802.11b receiver which operates at 2.4 GHz. When the GPS receiver is operating, the VCO carrier will inject noise at 1.5 GHz. This noise will couple into both the cellular VCO and the 802.11b VCO. For both the cellular and 802.11b receivers, the nonlinearity of the VCO will result in several intermodulation products. Of particular interest are the tones at $f_{cellular} + f_{GPS}$, $f_{802.11b} - f_{GPS}$, and $f_{802.11b} - f_{cellular}$. Both of these tones tones also

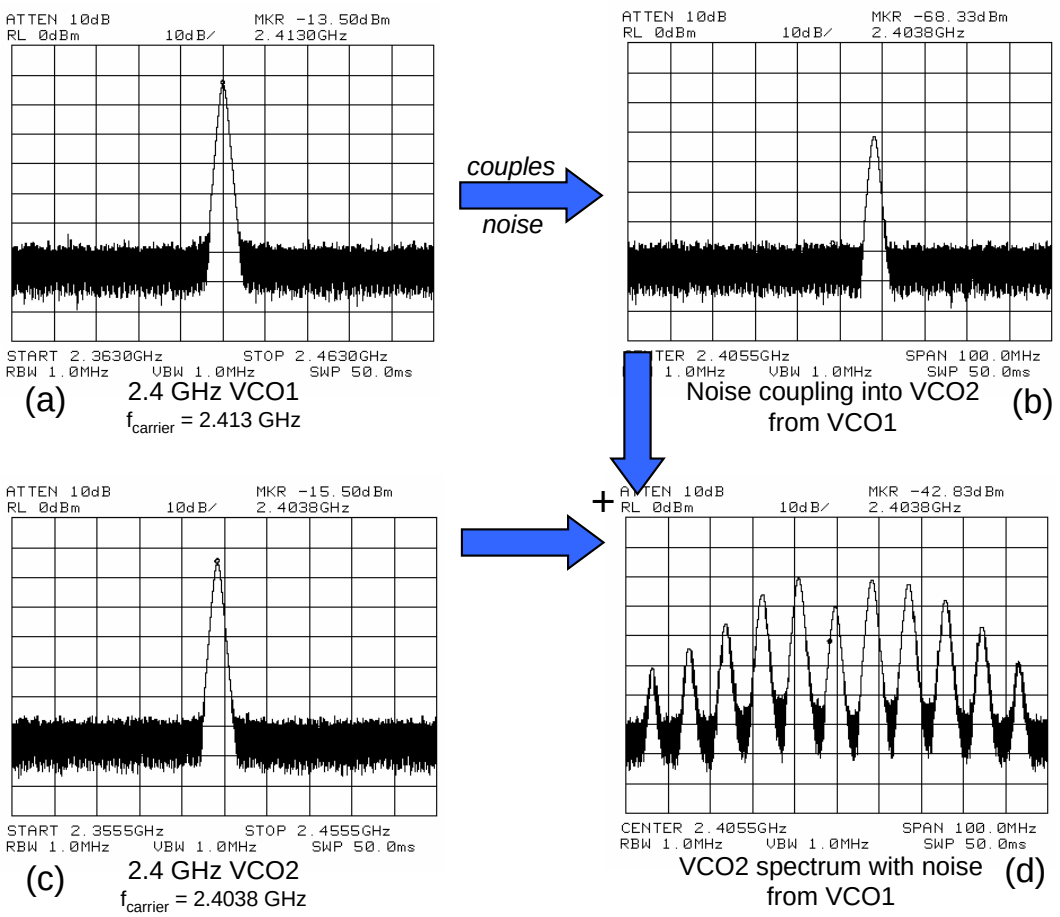


Figure 5-7: VCO-VCO Interference.

appear on the substrate where it can then couple into all the VCOs. The tone at $f_{cellular} + f_{GPS}$ appears at 2.4 GHz which is directly in the 802.11b band. Similarly, $f_{802.11b} - f_{GPS}$ appears at 900 MHz which is in the cellular band. Mixing between the 802.11b and the cellular VCOs will result in noise that appears in the GPS band. Thus, the operation of the other receiver chains can result in corruption of the VCO spectrum. One simple solution is to employ careful frequency planning such that no intermodulation products appear in the band of any of the standards being implemented.

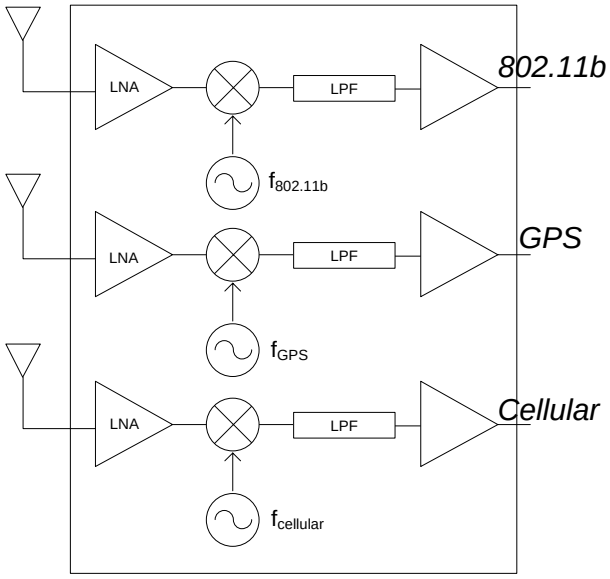


Figure 5-8: Block diagram of a multistandard radio.

5.4 Test Chip

A test chip was designed in collaboration with David D. Wentzloff to characterize the effect of substrate noise on a VCO. The test chip was fabricated in TSMC's 0.18 μm mixed-signal CMOS process. The technology included six layers of metal with a thicker top level metal for RF inductors. The substrate used was a high resistivity (10-15 Ω·cm) non-epi substrate. Thus, the substrate cannot be treated as a single node. As a result, the substrate can provide a measure of attenuation. All devices were fabricated using triple wells, which provide roughly 25 dB of isolation at 2.4 GHz [16]. The individual devices were not characterized without triple wells so the isolation effect of the triple well could not be determined. Figure 5-9 shows the die photo.

The chip consists of seven different VCOs of varying center frequency and noise isolation schemes. 900 MHz, 2.4 GHz, and 5.2 GHz were chosen as the VCO center frequencies as they represent the typical operating frequencies for wireless systems such as cellular and wireless LAN. Several parameters could be varied. First, by examining VCOs with varying center frequency, the effect of center frequency on the noise rejection properties could be determined. Second, the effect of VCO bias

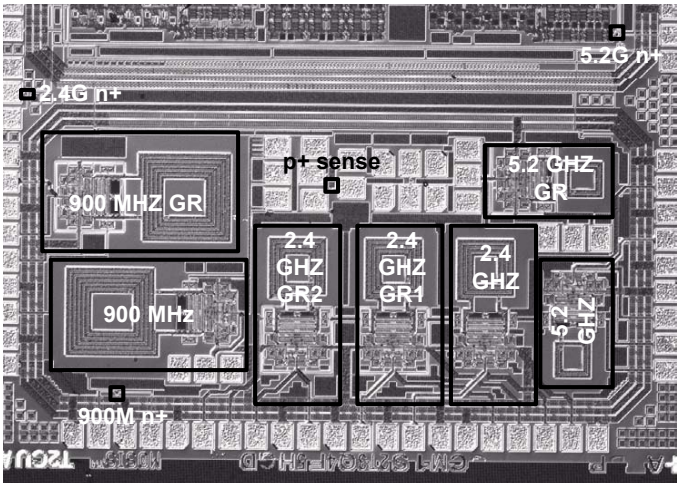


Figure 5-9: Die microphotograph of test chip.

current on the VCOs ability to reject any substrate noise was examined. Finally, the effectiveness of guard rings was analyzed. For each center frequency, a VCO with and without guard ring isolation was designed. The VCOs are identical with the exception of the added guard rings surrounding the devices of the VCO. Moreover, the test chip included several noise injection points and noise sensor locations spread over the entire die.

5.5 Experimental Setup

The test chip was mounted onto a metal plate using conductive silver epoxy. The chip was then wafer-probed using a Cascade Microtech Summit 900 probe station. Figure 5-10 depicts the experimental setup.

An HP83732B RF signal generator is used to generate the noise signal. RF ground-signal-ground (GSG) probes are used for all RF measurements. The RF signal is injected into a 240 μm^2 n+ diffusion region simulating the drain of a transistor. Several n+ regions are interspersed through the chip so that the injection location can be varied. The locations of these regions are marked in Figure 5-9.

Several p+ diffusion regions are located throughout the chip so that the substrate noise at various points across the die can be probed. A spectrum analyzer is used to

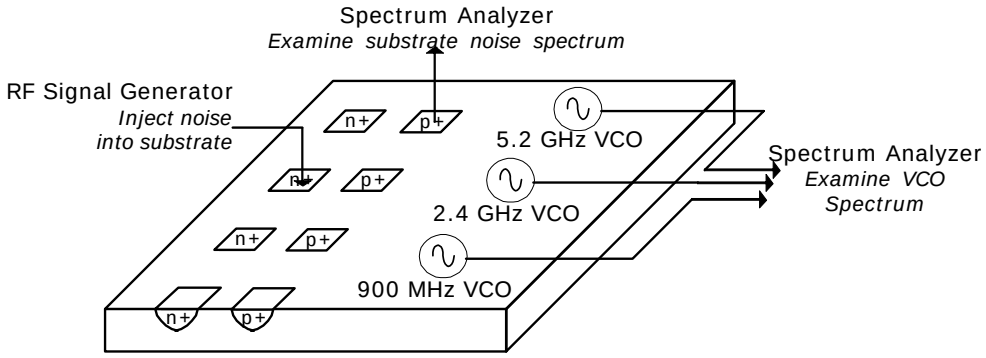


Figure 5-10: Experimental setup.

examine both the substrate noise spectrum and VCO output.

A resistive divider is present between the substrate and the spectrum analyzer due to the contact resistance of the p+ diffusion region and the 50 Ω termination in the spectrum analyzer. This is detailed in Figure 5-11. To back extrapolate the noise on the substrate, V_{sub}, from V_{out}, the following equation is used.

$$V_{sub} = \frac{50 + R_{con}}{50} V_{out} \tag{5.1}$$

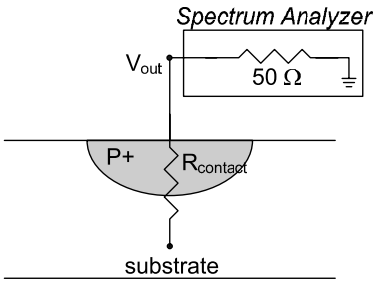


Figure 5-11: Resistive divider between the substrate and the output.

The resistance due to the p+ diffusion region and contact was calculated to be approximately 1.64 mΩ. Since R_{con} is much less than 50 Ω, V_{sub} is approximately V_{out}.

5.6 Substrate Noise and VCO Performance

The schematic for all the VCOs is shown in Figure 5-12. The same core is used for all VCOs with varying inductance and varactor capacitances to implement the correct center frequency. The VCO operates from a 1.8 V power supply and requires bias currents for the VCO core and output buffers that are provided off-chip.

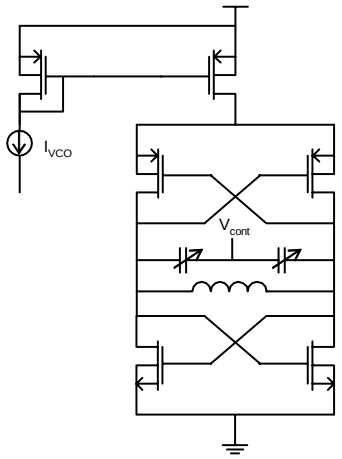


Figure 5-12: VCO schematic.

To determine how much noise appears on the substrate when a noise signal of certain power is injected, a test using the injection and probing locations is performed. In the test, a noise signal of power -15 dBm is injected at the point labeled 900M n+, and the substrate noise is probed at the located labeled p+ sense in Figure 5-9. The gain of the probed noise over the sensed noise is shown in Figure 5-13.

Over the frequency range from 500 MHz to 5.5 GHz, the measured gain is approximately constant at -50 dB. This indicates that the substrate acts as a resistive mesh over the frequency range of interest in this study. For an input signal of power -15 dBm, this corresponds to a noise level of -65 dBm on the substrate. This power level was chosen to emulate the noise power levels of a large digital system. The noise due to the fundamental of the 1 GHz clock of the Pentium® 4 has a power of roughly -52 dBm as shown in Figure 4-3 [24]. Even the higher order clock harmonics contain significant power. The fifth harmonic has a power of -62 dBm while the power level of the random digital activity is approximately -75 dBm [24]. Thus, the chosen noise

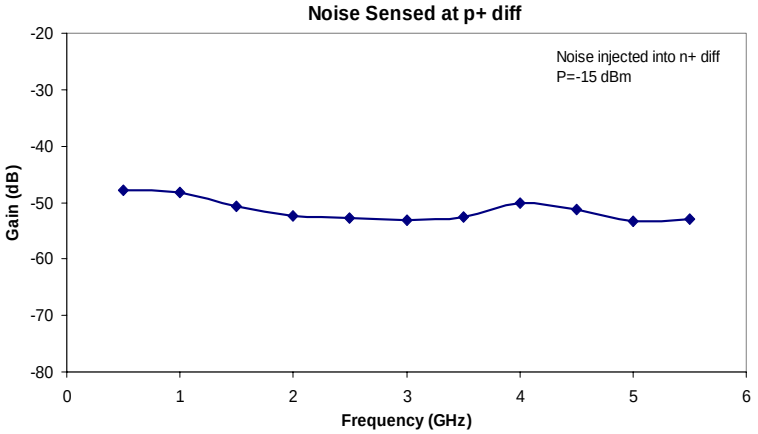


Figure 5-13: Gain from injected noise to sensed noise.

power level is on par with the noise due to the 5th harmonic of the clock.

When the VCO is powered up, and a noise signal of power -15 dBm is injected into the substrate, three tones appear at the output of the VCO as shown in Figure 5-14.

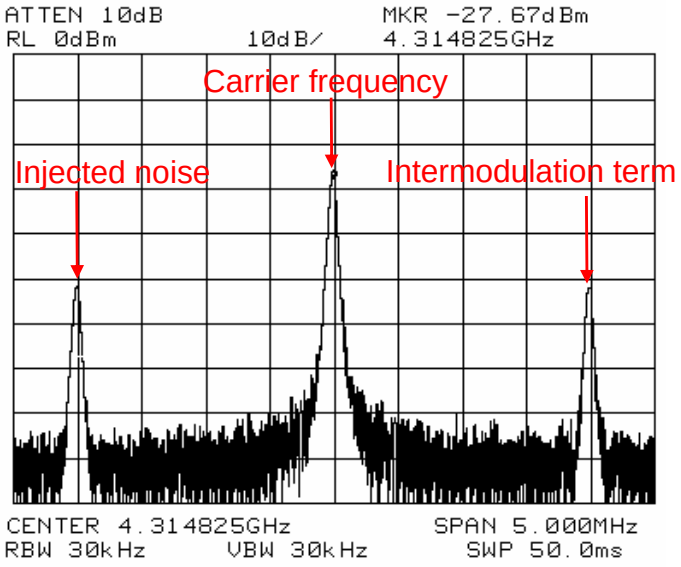


Figure 5-14: Description of tones appearing at the VCO output with f_{noise} = 4.312825 GHz.

In Figure 5-14, the largest peak corresponds to the VCO output frequency at 4.314808 GHz. Noise is injected at f=4.312825 GHz; this appears at the VCO output with gain that depends on the VCO bias current. The last tone at f=4.31679 GHz in Figure 5-14 is an intermodulation product due to the nonlinearity of the VCO [48].

The nonlinearity of the differential stages causes mixing of the noise and the carrier. Representing the input/output characteristic by Equation 5.2 for an input consisting of the carrier and a noise component in the form of $V_{in} = A_c cos(\omega_c t) + A_n cos(\omega_n t)$, results in several intermodulation products, which are listed in Table 5.1.

$$V_{out} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3 + \alpha_4 V_{in}^4 \tag{5.2}$$

For the noise depicted in Figure 5-14, the higher order intermodulation terms are below the noise floor of the system. However, as the noise frequency approaches the VCO center frequency, the main noise component as well as the intermodulation terms are amplified as a result of shaping by the LC tank. This resonant gain behavior is shown in Figure 5-25. As a result, higher order intermodulation terms appear at the VCO output as the noise frequency approaches that of the carrier. This is depicted in Figure 5-16.

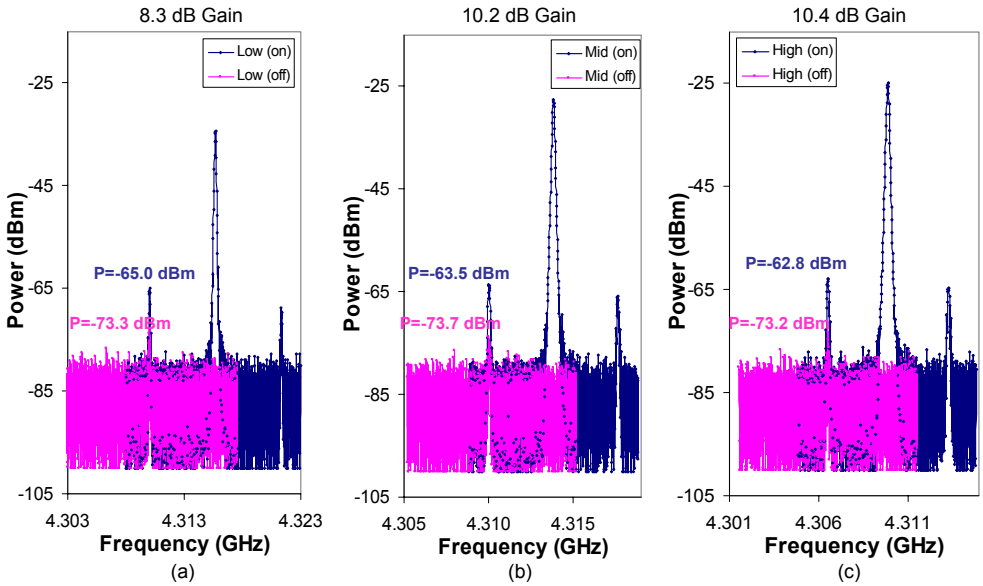


Figure 5-15: VCO output with noise on and off for varying I_{VCO}. I_{low}=1.81 mA, I_{mid}=2.71 mA, I_{high}=3.41 mA.

When the VCO is powered down, some noise still appears at the output; however, its amplitude is significantly less. This is shown in pink in Figure 5-15(a). This noise directly couples to the output and is independent of any VCO action. This indicates

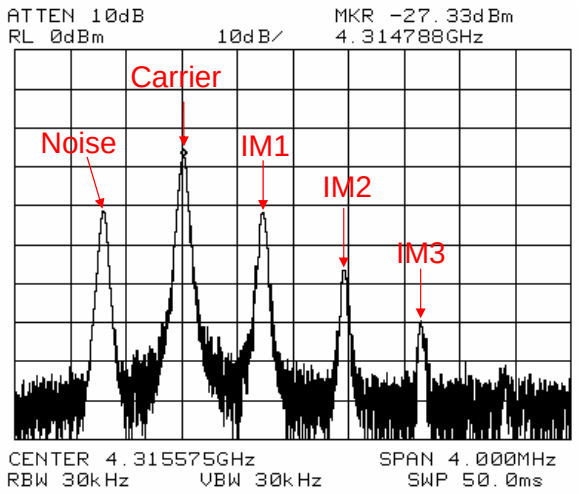


Figure 5-16: Tones at VCO output.

Tone	Frequency (GHz)
Carrier = f_c	4.314785
Noise = f_n	4.314215
IM1 = $2f_c$ - $2f_n$	4.315355
IM2 = $3f_c$ - $2f_n$	4.315925
IM3 = $4f_c$ - $3f_n$	4.316495

Table 5.1: List of tones.

that the noise couples either through the inductor to substrate capacitance or through the pad capacitance as shown in Figure 5-17.

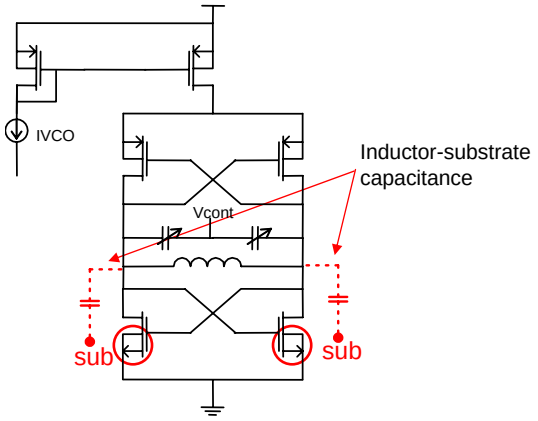
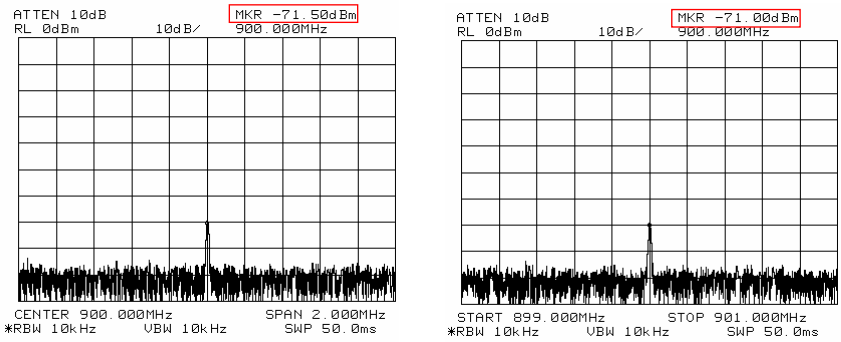


Figure 5-17: VCO schematic showing parasitic inductor to substrate capacitance.

To determine which of the two dominates, the noise is measured at an unconnected pad. The noise coupled through the pad capacitance is only 1-2 dB above the noise floor. Thus, all the noise that appears at the VCO output when powered off is a result of the inductor to substrate capacitance. This result is consistent with [45], which showed that a significant amount of noise can be injected into the substrate through the inductor to substrate capacitance.

If the noise that appears at the VCO output is indeed from the inductor to sub-

strate capacitance, the noise coupled would be independent of whether a guard ring is present. Guard rings were not placed surrounding the inductors and thus will not affect the noise coupled through the inductor. Figures 5-18(a) and 5-18(b) show that the received noise is the same irrespective of the guard ring.



(a) 2.4 GHz VCO output (GR). (b) 2.4 GHz VCO output (no GR).

Figure 5-18: Received noise at the 2.4 GHz VCO output with and without guard rings with the VCO powered off. f_{noise} = 900 MHz.

The amplitude of the noise that appears at the output is frequency dependent. As the operation frequency increases from 900 MHz to 5.2 GHz, the magnitude of the noise that couples through the inductor decreases. This is shown in Figure 5-19. The data was generated by injecting noise at 900 MHz and probing the noise coupled through both the 900 MHz VCO and the 5.2 GHz VCO. Approximately 13 dB less noise couples into the 5.2 GHz VCO than the 900 MHz VCO.

From 900 MHz to 5.2 GHz, the inductor area decreases by a factor of 6 as shown in Figure 5-20. Simulations using ASITIC [5] show that the inductor capacitance decreases from 220 fF for the 900 MHz VCO to 38 fF for the 5.2 GHz VCO. With decreasing inductor capacitance, the effective impedance increases resulting in less noise coupling to the output.

When power is applied to the VCO, the noise that appears at the output is amplified as shown in Figure 5-15. This indicates that the noise consists of two components: noise coupling through the inductor and noise from ground. Substrate taps around the periphery of the die are connected to the circuit ground; therefore,

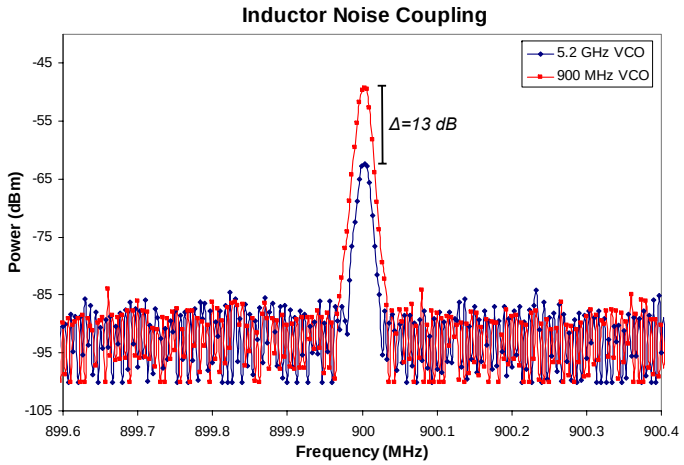


Figure 5-19: Coupled noise appearing at both the 900 MHz VCO output and the 5.2 GHz VCO output. f_{noise} = 900 MHz.

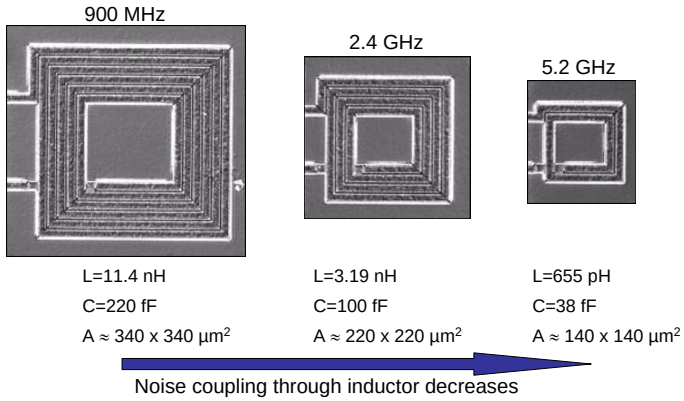


Figure 5-20: Die photos of the 900 MHz, 2.4 GHz, and 5.2 GHz inductors. The relevant parameters are listed.

any substrate noise directly appears at the VCO ground.

5.6.1 Effect of VCO Bias Current

As the VCO bias current is increased, the gain experienced by the noise increases as shown in Figure 5-15(a)-Figure 5-15(c). This is a result of the ground noise being multiplied by g_m to appear at the VCO output. For increasing bias current and operation in the current-limited regime, the VCO phase noise does not degrade despite the increased noise level as the carrier power also increases with bias current [34]. For the 5.2 GHz VCO, a bias current of 2.7 mA places the VCO at the edge of the

current-limited regime. Increasing the bias current beyond this level places the VCO in the voltage-limited regime where the carrier power is limited by the power supply and no longer scales with current. The noise level still scales with current; therefore, when operating in the voltage-limited regime, the phase noise performance actually degrades since the carrier power remains constant. This is depicted in Figure 5-21. Table 5.2 shows the ratio of carrier power to noise power for the 5.2 GHz VCO over three different bias current levels.

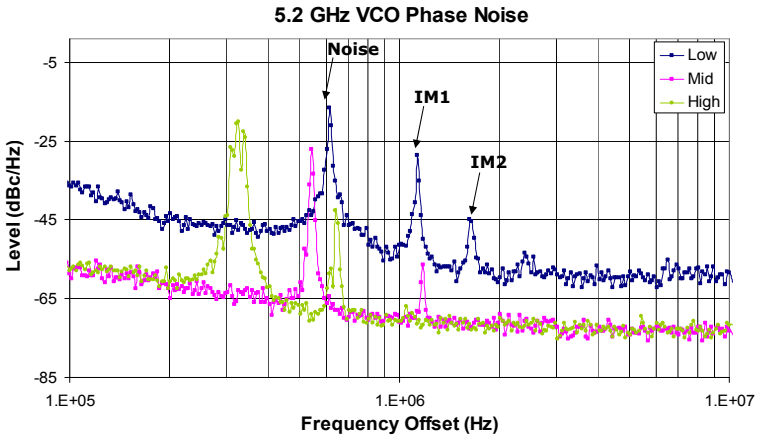


Figure 5-21: Phase noise of the 5.2 GHz VCO for varying I_{VCO}. I_{low}=1.81 mA, I_{mid}=2.71 mA, I_{high}=3.41 mA.

Table 5.2: Ratio of the carrier to noise power for the 5.2 GHz VCO.

I_{VCO}	P_c/P_n
1.81 mA	9.9 dB
2.71 mA	26.3 dB
3.41 mA	23.1 dB

5.6.2 Effect of Guard Rings

Dual guard rings consisting of p+ and n-well annular regions were placed surrounding the active devices of the VCO but not surrounding the inductor. A cross-section of the dual guard ring structure is shown in Figure 5-22. Figure 5-23 shows a top view of the VCOs with and without the guard rings. Guard rings mitigate substrate noise by sinking the surface portion of the substrate current to a lower impedance supply.

They are typically ineffective on epi substrates as the substrate current penetrates deep into the low resistivity region bypassing the guard rings where it the propagates across the die [55].

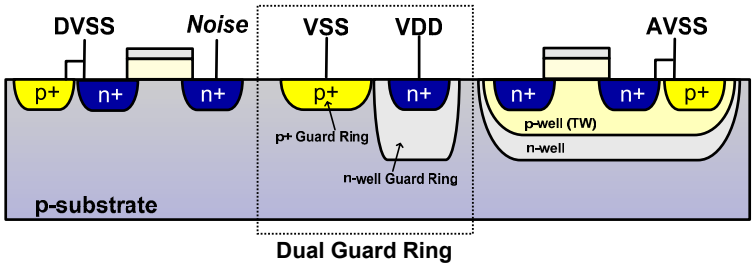


Figure 5-22: Cross-section of dual guard ring isolation.

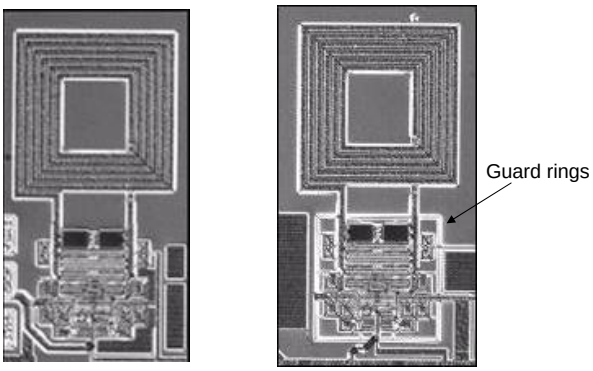
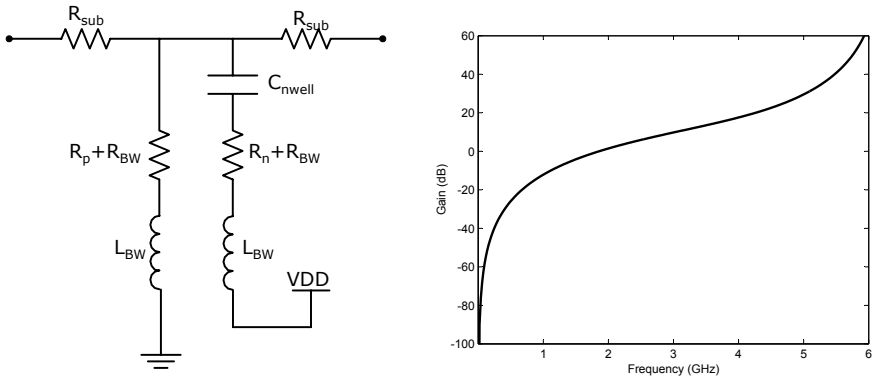


Figure 5-23: Top view of VCOs with and without guard rings.

A simple, intuitive model for the dual guard ring is shown in Figure 5-24. R_{bw} and L_{bw} represent the resistance and inductance associated with the measurement probes or for a packaged chip, the parasitics associated with the bond wires. The p+ guard ring is modeled as a resistor to circuit ground (R_p); whereas, the n-well guard ring is modeled with a series resistance (R_n) and capacitance (C_{nwell}) to V_{DD}. The effectiveness of guard rings depends on both the frequency of operation and circuit parasitics. The transfer function for the model is derived to be:

$$\frac{V_{out}}{V_{in}} = \frac{R_p + j\omega L_{bw}}{R_{sub} + R_p + j\omega L_{bw}} \frac{1 - w^2 L_{bw} C + j\omega C(R_{sub} + R_n)}{1 - w^2 L_{bw} C + j\omega C R_n} \tag{5.3}$$



(a) Schematic. (b) Transfer function.

Figure 5-24: Model for dual guard rings.

At low frequencies, the path to ground through the p+ guard ring is low impedance thereby effectively sinking a significant portion of the substrate current. At higher frequencies, the impedance of the guard ring node increases reducing the isolation effectiveness. This behavior is shown in the plot of the transfer function in Figure 5-24(b). This model provides useful intuition to aid in the design of optimized isolation structures. For example, wider guard rings would result in less impedance to ground (i.e. reduced R_p) improving the effectiveness of the guard rings; however, reducing the impedance lowers the first corner frequency resulting in less isolation at lower frequencies. The data presented in [16] supports this observation.

Moreover, the model indicates that the n-well guard ring has little impact at the frequencies of interest in this study and only contributes higher order poles and zeros where the model will fail due to omission of parasitics associated with the measurement setup. This finding is also consistent with [16]. Intuitively, this is reasonable as the n-well couples capacitively to the underlying substrate and therefore will collect significantly less substrate current than that of the p+ guard ring that is resistively coupled.

The output spectrums of the VCOs with and without guard ring isolation were examined in the presence of substrate noise. The guard rings could only attenuate the circuit component of the noise and not the inductor component as they were placed surrounding only the active devices. Figure 5-25 shows that the guard ring provides

roughly 10 dB of isolation around the carrier frequency for the 5.2 GHz VCO. The guard ring isolation degrades closer to the carrier frequency as the noise experiences a higher gain from the resonance of the LC tank.

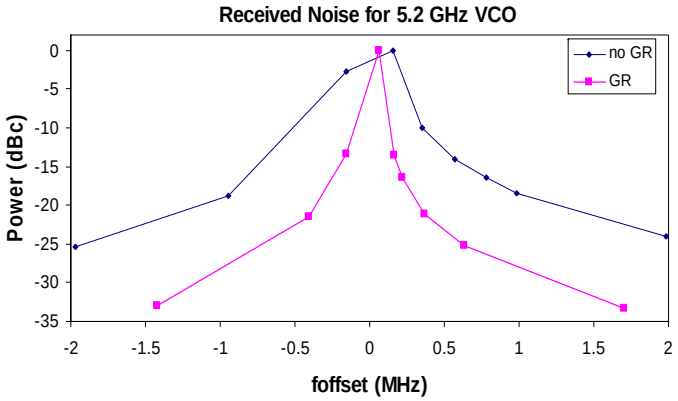


Figure 5-25: Effect of guard rings on the noise power of the 5.2 GHz VCO around $f_{carrier}$.

Figure 5-26 shows that guard rings can significantly attenuate the circuit noise component at lower operating frequencies; however, their effectiveness degrades at higher frequencies due to circuit parasitics. For example, at 900 MHz, guard rings provide approximately 15-20 dB of isolation around the carrier frequency. That isolation reduces to approximately 10 dB at 5.2 GHz.

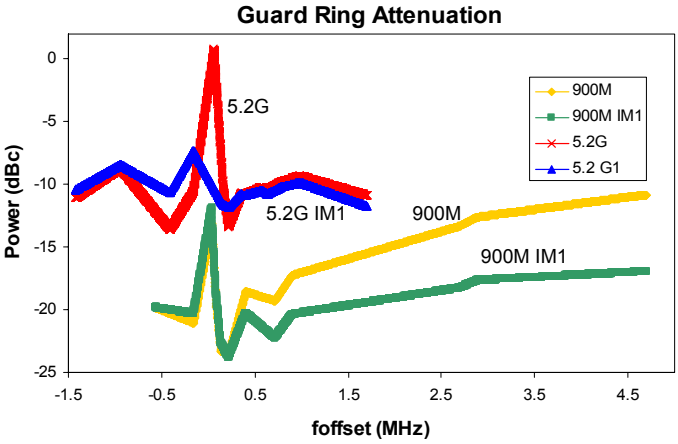
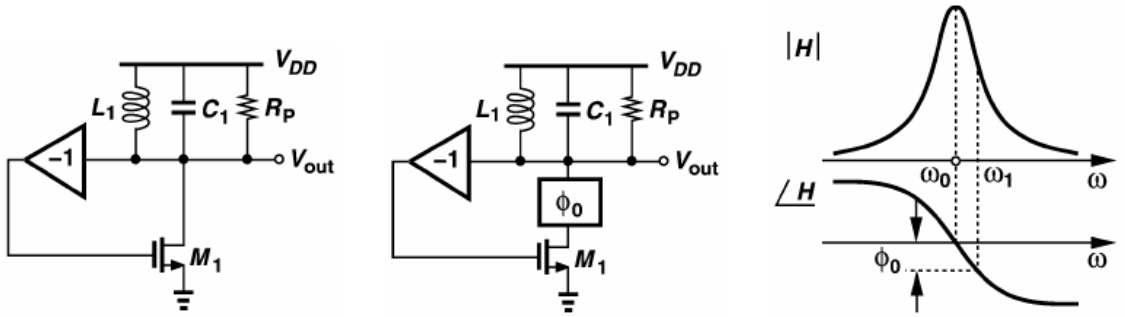


Figure 5-26: Guard ring attenuation around $f_{carrier}$ for the direct noise component and IM1.

5.7 Injection Locking

If the frequency of an interferer approaches the resonant frequency of a VCO, the oscillator can lock to the interference frequency instead of the resonant frequency of the LC tank if the power of the interferer is comparable to that of the carrier [49]. The design of injection locked frequency synthesizers relies on this phenomenon.

The oscillation frequency of a VCO is the frequency at which the total phase shift around the feedback loop is 360^o. This is shown in Figure 5-27(c). If an external signal is able to introduce an additional phase shift into the loop as shown in Figure 5-27(b), the oscillation frequency must change to offset the additional phase. The VCO now oscillates at frequency ω_1. This is what happens in injection locking. The noise on the substrate introduces a phase shift that the VCO offsets by locking to the noise instead of the resonant frequency of the tank.



(a) Conceptual VCO.

(b) VCO with additional phase shift.

(c) Open-loop characteristics.

Figure 5-27: Injection locking concept. Figures from [49].

It has been well established that injection locking is a serious impediment to the single chip integration of an RF power amplifier and a VCO as the transmitted signal is of appreciable power and acts as an interferer [48]. This study shows that without careful design, digital circuit generated substrate noise can also result in VCO injection locking.

As mentioned in Section 5.6, the substrate noise levels considered in this work are on par with that of higher order clock harmonics of a large digital system. The shaping behavior of the resonant tank causes noise around the resonant frequency to

be amplified. The shaping function can cause the noise to become significant enough to result in injection locking. Figure 5-28 shows that the 5.2 GHz VCO locks to substrate noise offset from the center frequency by 20 kHz.

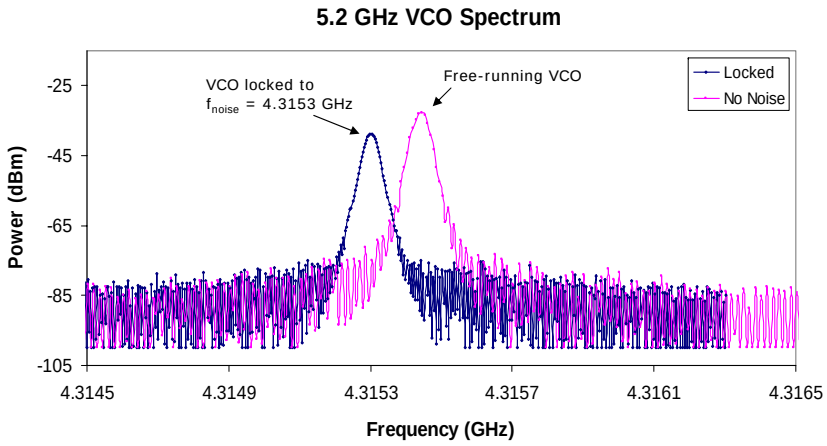


Figure 5-28: Output spectrum of the 5.2 GHz VCO. Shown in pink is the VCO output with no noise injected. Shown in blue is the VCO output locked to the noise frequency instead of the resonant frequency of the LC tank.

Injection locking relies on the relative power levels of the carrier and the noise. In fact, the range over which injection locking occurs is given by [49]:

$$f_{lock} \approx \frac{f_o}{2Q}\frac{I_{noise}}{I_{carrier}} \tag{5.4}$$

Manipulating Equation 5.4, results in the following expression relating the injection locking range to the noise power.

$$f_{lock} = \frac{f_o}{2QI_{carrier}}\sqrt{\frac{1mW}{50}}10^{P/20} \propto 10^{P/20} \tag{5.5}$$

The injection locking range depends exponentially on the noise power. For the 5.2 GHz VCO, the measurements show that the locking range does indeed follow an exponential relationship with the noise power. This is shown in Figure 5-29.

Equation 5.4 indicates that for a given noise power, reducing the carrier power increases the locking range. This relationship is validated with measurements. For increasing carrier frequency, the output power of the VCO reduces. For example, the

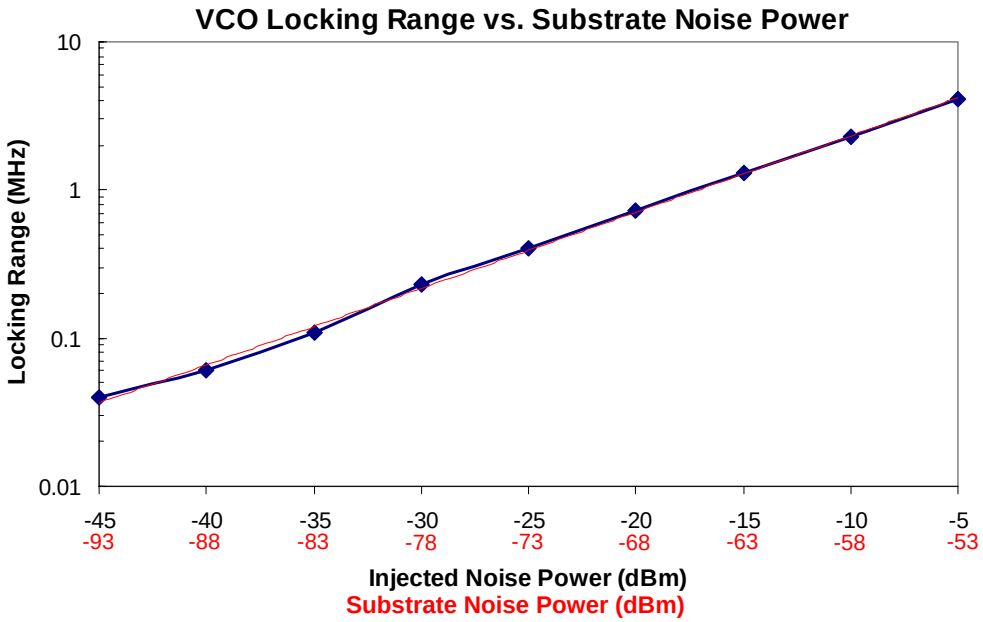


Figure 5-29: VCO locking range (log scale) vs. injected noise power into a pad. Numbers in red represent the equivalent noise on the substrate. The overlaid red curve is the data fit to an exponential.

output power of the 900 MHz VCO is greater than the output power of the 2.4 GHz VCO which is greater than the output power of the 5.2 GHz VCO. Thus, Equation 5.4 would predict a reduction in the locking range as the carrier frequency reduces. The measurements support this prediction and are summarized in Tables 5.3-5.5.

Furthermore, Equation 5.4 indicates that for a given carrier power, reducing the noise power reduces the locking range. Because guard rings can attenuate noise by as much as 25 dB for the 900 MHz VCO, guard rings also reduce the range of frequencies for injection locking. Tables 5.3-5.5 show that for each carrier frequency, the use of guard rings reduces the locking range.

Table 5.3: 5.2 GHz VCO and injection locking.

GR?	f_{center}	*Locking Frequency Range*
No GR	4.3148 GHz	500 kHz
GR	4.314 GHz	200 kHz

Table 5.4: 2.4 GHz VCO and injection locking.

GR?	f_{center}	*Locking Frequency Range*
No GR	2.027 GHz	50 kHz
GR	2.031 GHz	30 kHz

Table 5.5: 900 MHz VCO and injection locking.

GR?	f_{center}	*Locking Frequency Range*
No GR	812.89 MHz	5 kHz
GR	805.13 MHz	Doesn't Lock

5.8 Low Frequency Noise

The analysis presented thus far involved noise injected close to the VCO center frequency. This noise appears directly at the output and also creates an intermodulation product as a result of mixing with the carrier frequency.

If low frequency noise is injected, the direct noise component appears out of band with the carrier frequency; however, some intermodulation products appear in band. The products $2f_c - f_n$ and $2f_c + f_n$ are close to the carrier frequency and are observed as the two peaks around the carrier in Figure 5-30.

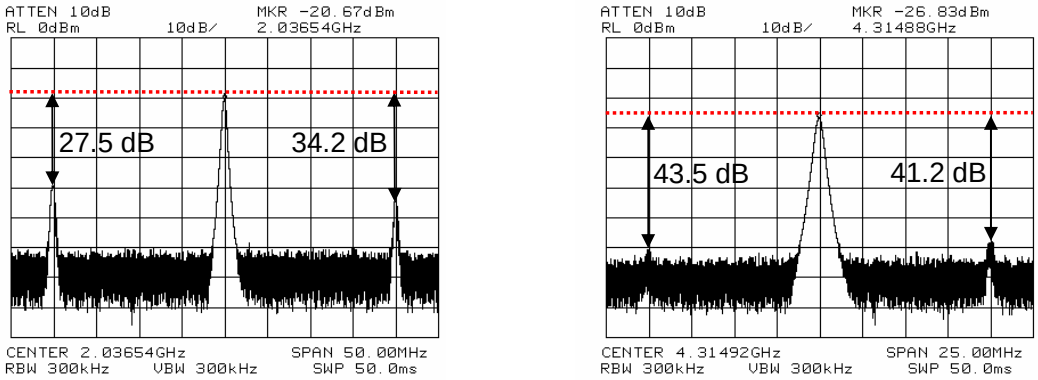


Figure 5-30: Effect of low frequency noise (f_{noise} = 10 MHz) on the 2.4 GHz and 5.2 GHz VCOs.

The coupling mechanisms for low frequency noise vary greatly from high frequency noise around the carrier. As mentioned in Section 5.6, for noise around the carrier frequency, the main coupling paths were through ground noise and coupling through

the inductor to substrate capacitance. The impedance presented by the inductor to substrate capacitance is inversely proportional to both the operating frequency and capacitance. At higher frequencies, the impedance is low resulting in more noise coupling to the output. For low frequency noise, the impedance is very large resulting in little coupling through the inductor. In general, any capacitive coupling is negligible at low noise frequencies; thus, the main coupling path is through ground noise. To validate this claim, a simple test can be performed. By powering the VCO off and probing the output, any noise that appears will be a result of coupling through the inductor. When this test is performed for an f_{noise}=10 MHz, no signal appears at the output.

A detailed analysis of the effect of low frequency noise on the phase noise of a 3.5 GHz LC tank VCO is presented in [54]. Guard rings are effective in attenuating noise at low frequencies; thus, the effect of low frequency noise can be mitigated with the use of standard isolation techniques.

5.9 Summary

Substrate noise is a serious problem that continues to plague mixed-signal designs. Components of the RF front end are particularly sensitive to substrate noise as the effectiveness of standard isolation techniques degrades at higher frequencies. This study has shown that the phase noise of a VCO is adversely affected by substrate noise. In the extreme, the VCO can lock to the substrate noise.

Bias current plays an important role in the noise performance of the VCO. Increased bias current does not always result in better phase noise. At higher bias current levels, the circuit noise component experiences higher gain. When the VCO enters the voltage-limited regime, the carrier power no longer increases; thus, the overall phase noise worsens.

Guard rings can effectively attenuate substrate noise at lower frequencies. For example, at 900 MHz, as much as 25 dB of isolation is observed. At 5.2 GHz, the isolation reduces to 10 dB. A simple model for guard rings is proposed that

explains this behavior. The simple model proposed here for guard rings provides useful intuition to aid in the design of optimized isolation structures. Furthermore, the use of guard rings can improve the response of the VCO to injection locking.

Chapter 6

Substrate Noise Analysis Tool (SNAT)

6.1 Overview

Chapter 2 presented a survey of other approaches to predict the substrate noise behavior of large digital systems. A full SPICE transistor level simulation yields the most accurate results; however, it is impractical for most circuits as the run-time increases rapidly with circuit complexity. For typical circuits, full transistor level simulations taken on the order of weeks to simulate a few clock cycles and most often do not converge.

It has been demonstrated that abstracting the noise behavior through the use of macromodels greatly improves simulation speeds without much expense in accuracy. Much work has been done in this area [22] [38] [14]. Each approach uses a different macromodel; however, the underlying methodology is the same. Each has its own shortcomings. The most common problem is that the noise macromodel does not completely encapsulate the noise behavior of the circuit. Furthermore, certain assumptions taken in SubWave [38] do not permit the tool for use with non-epi substrates. With technology scaling, latch-up is becoming less of a concern; thus, non-epi substrates are becoming more prevalent for their improved noise isolation properties over epi substrates. Both SWAN and the tool developed by the Universitat Politècnica

de Catalunya use a substrate model generated by SubstrateStorm. SubstrateStorm requires a full layout of the circuit with a substrate doping profile. Because a full layout is required, substrate noise simulation can only be performed at the end of the design cycle.

There exists several tools that can be used to predict the substrate noise profile of digital systems. However, none of these are flexible enough to work at any stage in the design cycle. These tools can only be used for final verification. Final verification of the substrate noise performance of a digital system is an important part of substrate coupling analysis. However, a tool that can yield information at earlier stages in the design cycle permits changes in both the design and the layout to try and mitigate noise coupling and, thus, performs a much more valuable function. Such a tool should be able to work at higher abstraction levels to tradeoff accuracy for simulation speed.

Section 6.2 presents a high-level description of the tool developed in this dissertation. Section 6.3 describes the inputs to SNAT. Section 6.4 describes the macromodel that forms the heart of SNAT. Section 6.5 describes the overall methodology. Finally, Section 6.6 shows how SNAT operates in the context of an example.

6.2 Description

Figure 6-1 shows a high level block diagram of SNAT. The overall methodology is based on that used by both the Universitat Politècnica de Catalunya and IMEC.

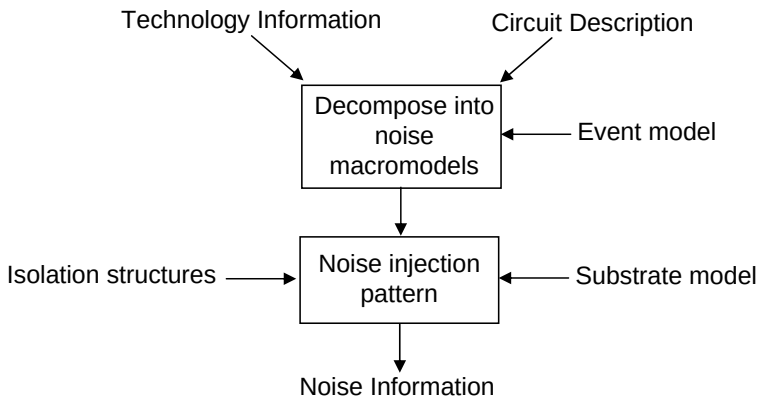


Figure 6-1: High level block diagram of SNAT.

SNAT requires two inputs: a circuit description and a technology description. SNAT decomposes the circuit into equivalent noise macromodels. The noise macromodels together with the event model for each node in the circuit are used to construct the noise signature. This noise signature is then simulated with the substrate model and power grid to compute the substrate noise profile. The outputs are a time domain representation and noise spectrum. The details of each of these steps are the subject of this chapter.

6.3 Granularity Level

SNAT works with a broad spectrum of information for both the circuit and technology descriptions. This allows SNAT to be used at any stage in the design cycle. The different input descriptions that SNAT can work with are detailed in Figure 6-2 and Figure 6-3.

6.3.1 Circuit Description

To generate the noise signature, SNAT requires information on the circuit. At a minimum, a gate-level description along with BSIM models can be used to generate the signature. At the gate level, no layout information is available; thus, the noise sources will not be accurately modeled. Because very little information is available, the simulation time will be fast; however, accuracy will be compromised.

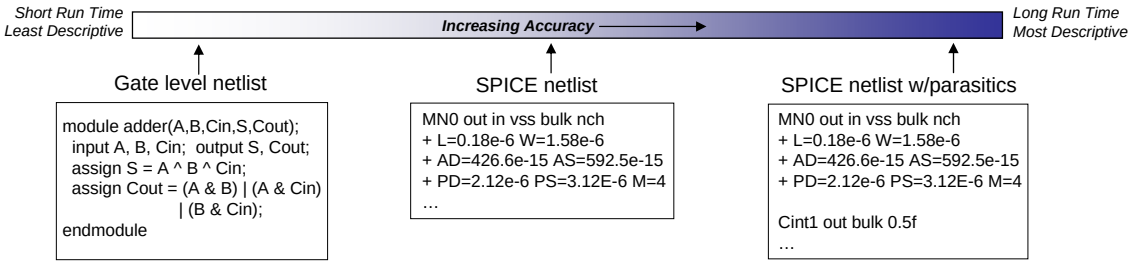


Figure 6-2: Granularity levels for the circuit description.

As the user provides more information to the tool, the noise sources will be modeled more accurately improving the overall accuracy of the simulation. However, more

nodes are now considered. As a result, the simulation time increases. For instance, providing a more detailed circuit description such as an extracted netlist from layout increases the number of elements that are simulated and thus the run time; however, the accuracy increases. The inclusion of parasitics has a significant effect on the accuracy of the generated substrate noise profile as will be shown in Chapter 7. SNAT's ability to work with a variety of input descriptions is referred to as the granularity level.

6.3.2 Technology Description

Multiple granularity levels are also present on the substrate modeling side. To properly model the high resistivity, non-epi substrate that is typically used in mixed-signal systems, a full extraction of the layout of the circuit with the substrate doping profile has to be generated. Cadence's SubstrateStorm tool is typically used for detailed extraction [8]. SubstrateStorm requires both a layout and substrate doping profile.

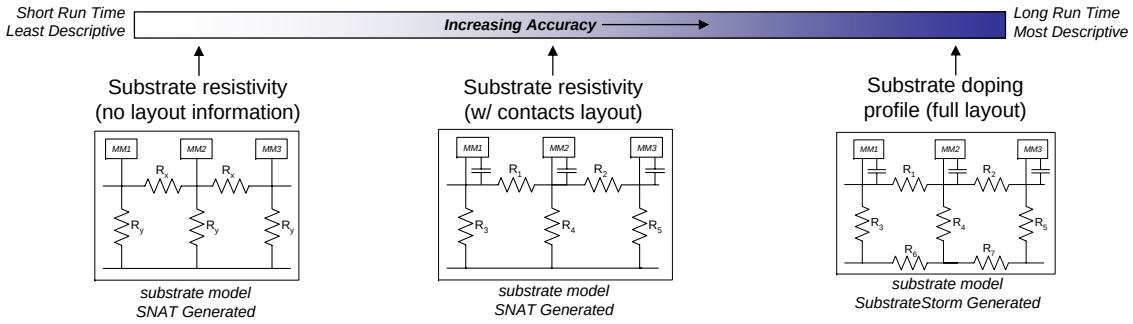


Figure 6-3: Granularity levels for the technology description.

Depending on the size of the circuit, the generated netlist can be massive since all propagation mechanisms are accounted for. It is not unusual for the resultant netlist to consist of several million elements. Using such a complete substrate model results in the most accurate estimate at the expense of a long run time. Simulation times are on the order of several days for a medium-scale circuit. Such long run times can be tolerated for final verification; however, they are prohibitively long if the simulation is performed during the design phase.

If the technology is not well characterized, substrate doping profiles might not be available. In this case, SubstrateStorm cannot be used to generate a model. SNAT can work with a substrate model generated from an outside source or can generate its own substrate model.

At the next lowest granularity level, SNAT generates a coarser substrate model knowing only the underlying substrate resistivity. It will later be shown that the capacitive effects of wells and other junctions need only be considered at lower frequencies. At higher frequencies, the resistive nature of the substrate dominates. This observation is the basis of the coarser substrate model.

Based on the layout, a purely resistive model is generated. This model is a mesh of resistances between the substrate contact locations. The number of nodes is greatly reduced speeding up run time. The user can also choose to give a less detailed layout from which a substrate model can be generated. With the reduced detail, the number of elements in the substrate model decreases speeding up run time.

SNAT also has to be able to yield a substrate model when no layout information is available. For example, if the circuit input description is a verilog netlist, no layout is available. SNAT can still yield an approximation for the substrate noise levels with no circuit layout. To generate the substrate model for such a case, an estimate of the circuit area must be provided from which a resistive substrate model is generated. In this case, an equi-resistance mesh is generated.

A comparison of simulations done on several granularity levels with that of measured data on a digital PLL is provided in Section 7.3 of Chapter 7.

6.4 Macromodel

SNAT generates equivalent macromodels for each gate. The macromodel used is a modification of that proposed in [14].

Figure 6-4 shows all the noise sources in a digital system. In order to accurately model noise injection, all noise sources must be accounted for. Each element in the macromodel is used to model a noise source. Figure 6-5 shows the SNAT macromodel.

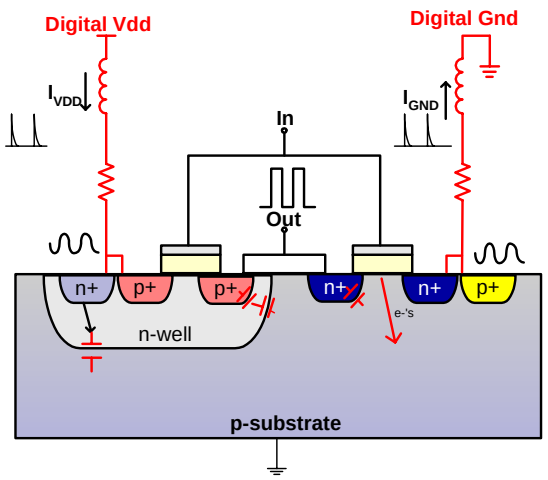


Figure 6-4: Substrate noise sources in a digital system.

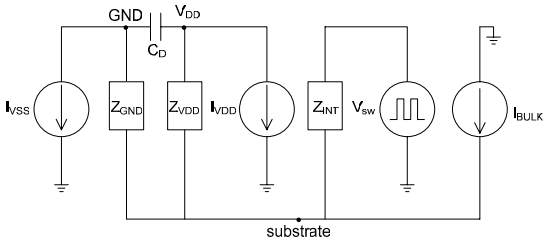


Figure 6-5: SNAT noise macromodel.

The current sources I_{VDD} and I_{VSS} represent the noise in the power and ground lines respectively. These currents working in tandem with package parasitics will create V_{DD} and ground bounce that appears on the substrate. Z_{GND} and Z_{VDD} represent the equivalent impedance from ground and V_{DD} respectively to substrate. For example, for a simple n-well process, Z_{GND} could simply be the resistance of the substrate contact, R_{sub}. Z_{VDD} would be the series combination of the n-well capacitor and the resistance through the n-well. C_D represents the impedance local to the gate between V_{DD} and ground.

Modeling the impedance from the both V_{DD} and ground to substrate as simple lumped elements is an approximation that is valid up to several GHz. IMEC compared this model to a more accurate model generated by LAYIN (now SubstrateStorm) for an inverter. The results of this comparison are shown in Figure 6-6 [26]. As shown in Figure 6-6, the lumped model in the macromodel loses its validity around 5 GHz for an inverter.

I_{bulk} represents current flowing directly into the substrate such as that from impact ionization. Voltage sources are used to represent the capacitive sources of noise such as interconnect. The addition of these elements is the main difference between the macromodel proposed here and that of other approaches. Reference [37] showed that medium-sized interconnect can couple more noise into the substrate than several

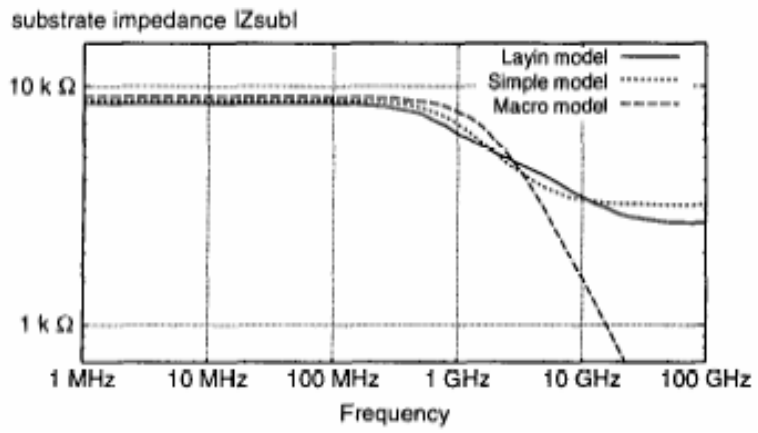


Figure 6-6: Substrate impedance of a CMOS inverter for different substrate models. From [26].

hundred switching transistors. However, the complex routing of the interconnect mesh does create a shielding effect that mitigates the amount of noise that is coupled. Nevertheless, in some situations certain interconnect can induce significant levels of substrate noise. For example, interconnect associated with clock networks is used to distribute a high-speed signal using wide metal traces that can have significant capacitance to substrate. In addition, the effect of bond pads and pad rings can be significant as will be shown in Section 7.3.4. Other approaches neglect this source of noise resulting in reduced accuracy when compared to measured data. The current noise sources in the macromodel depend on both the input rise time and output load.

6.4.1 Rise Time Dependency

Figure 6-7 shows how the current profile changes with input rise time for an inverter designed in a 0.18 μm technology. With increasing rise time, the peak reduces while the pulse width widens.

To accurately re-create the current pulses, the rise time of the inputs of each gate must be determined. This is obtained from an event-driven simulation of the digital circuit. This is discussed further in Section 6.5.

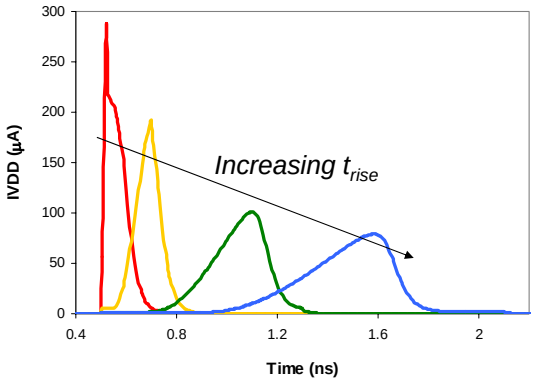


Figure 6-7: Macromodel noise current dependence on input rise time.

6.4.2 Output Load Dependency

The pulse shape of the noise current sources also depends on the output load if an output switching event occurs. For an inverter, Figure 6-8 shows that up to a particular load level, the peak increases; however, after a certain point, the peak remains constant. The fall time of the current transient increases with increasing load.

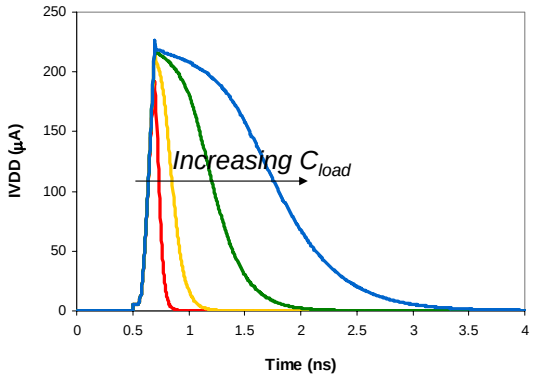


Figure 6-8: Macromodel noise current dependence on the output load.

In order to accurately re-create the current pulse, the load at each node of the circuit must be determined. This is discussed in more detail in Section 6.5.

The dependency on both the input rise time and output load is specific to each cell and is extracted during the library characterization step. This step need only be performed once per technology library and takes approximately 18 hours to characterize 471 standard cells on a dual processor 1.2 GHz SunFire 280r machine.

6.5 Methodology

Figure 6-9 outlines the methodology used by SNAT. The first step in the methodology is to characterize all the cells in the library. The dependencies on input rise time and output load are extracted and stored during this library characterization. The dependencies are unique to each cell. For example, the function describing the peak dependence of I_{VDD} on input rise time for an inverter will differ from that of a NAND gate. In addition, the impedance elements in the macromodel are extracted through an AC SPICE simulation for each gate.

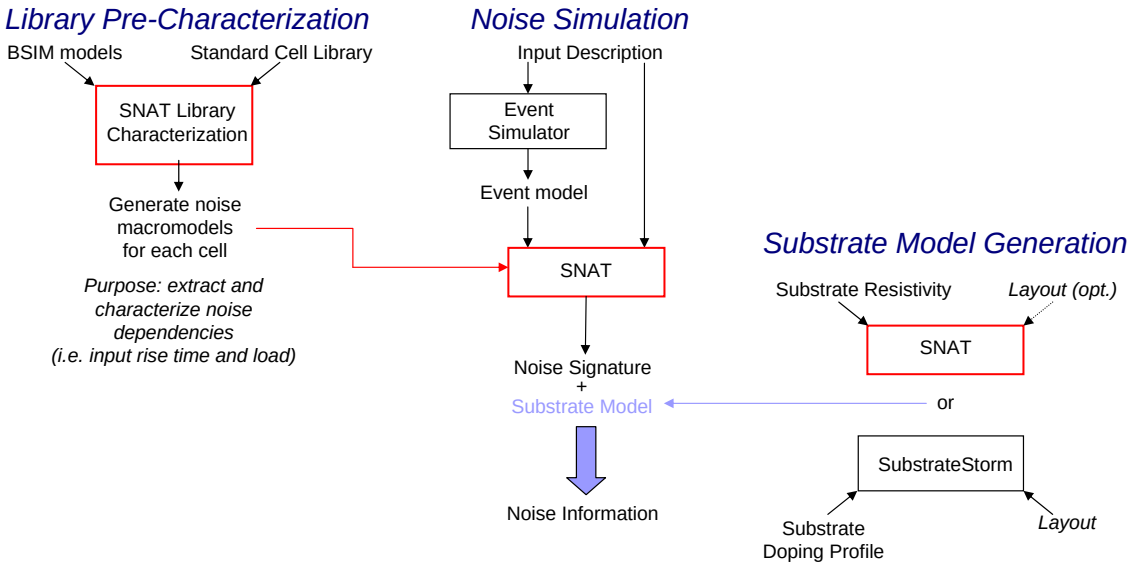


Figure 6-9: SNAT methodology.

This library characterization step takes approximately 18 hours to characterize TSMC's 0.18 μm standard cell library on a 1.2 GHz SunFire 280r machine. The characterization algorithm used is more efficient than that of SWAN. The characterization step in SWAN takes approximately 39 hours to characterize 96 standard cells on a Pentium® 2 [26]. The reason for this speed up is not clear as their algorithm has not been disclosed. The library characterization need only be performed once per technology library.

The second step in the methodology is to perform the substrate noise simulation itself. In order to accurately re-create the noise waveform, the noise sources in the

macromodel must be modeled accurately. The current pulses of a particular gate depend on the input rise and fall time and on the output load if an output switching event occurs. In order to generate the correct pulse, this information needs to be determined. An event driven simulation is performed on the full system in order to record the rise and fall times of each node and the state of all nodes at each point in time. If the input description is a gate level netlist, a gate level simulation is performed. If the input description is a SPICE netlist, Nanosim [7] is used to generate the event model.

SNAT decomposes the full circuit into equivalent macromodels. From the event model, the relevant parameters are extracted to re-create the noise current pulses for each gate. The complete macromodel for each gate of the design is then constructed.

The macromodels are then connected together with a substrate model. If a model for the power grid is supplied, the model is incorporated between the local power supply nodes.

The substrate model can be generated in one of two ways. The model could be generated from an external tool such as SubstrateStorm. This model can then be input into SNAT. If a very accurate substrate model is required, this option must be exercised as the models generated by SNAT are less accurate. Moreover, SNAT itself could be used to generate the substrate model. SNAT should be used to generate the model if a speedup in simulation is required or if the layout or technology is not well developed.

SNAT takes the constructed equivalent circuit that consists entirely of linear elements and uses SPICE as the engine to compute the substrate noise profile. SNAT determines both the time domain noise and the noise spectrum.

The effect of different isolation structures on the substrate noise profile can also be determined. The user specifies the isolation geometry and distance, and SNAT shows the resultant substrate noise profile. Currently, SNAT only works with guard ring isolation. Section 7.4 of Chapter 7 shows an example of how this noise plug-in is used.

Chapter 7 presents a comparison of the simulation results of SNAT to both full

transistor level simulations and measurements on fabricated circuits.

6.6 Example

The operation of SNAT is best understood through an example. During the library characterization, SNAT characterizes each of the standard cells and generates equivalent macromodels. In order to extract the current profiles, SPICE simulations over all possible input combinations are performed, and the resultant profiles are stored. In addition, the dependencies on rise time and load are also extracted. The final elements that must be extracted are the equivalent impedances. Z_{GND}, Z_{VDD}, and Z_{int} are calculated based on the geometry of each device and on resistance and capacitance data provided in the BSIM model file. For an NMOS device in an n-well process, Z_{GND} is typically the resistance of the p+ substrate contact. For a PMOS device, Z_{VDD} consists of the series combination of the n-well capacitance and the resistance of the n+ substrate contact. Z_{int} represents the impedance from switching interconnect to the substrate and is typically a series resistance and capacitance. For example, to incorporate the effect of a switching signal connected to an output pad, Z_{int} consists of a series capacitance representing the pad to substrate capacitance and a resistance representing a spreading resistance. C_D is extracted from an AC simulation of each cell. All this information is stored in a look-up table that is accessed during the substrate noise simulation.

Figure 6-10 shows the schematic of a one bit adder. For this example, the input to the tool is a verilog netlist that describes this adder. Figure 6-11 shows the synthesized verilog netlist.

SNAT identifies each of the standard cells in the design. For the one bit adder example, those cells are AOI22X1, XOR2X1, and INVX1. It then replaces each cell with its equivalent macromodel. A gate-level simulation is performed to extract the switching events of each node of the adder. This event information together with the look-up table generated during the library pre-characterization is used to construct the noise current waveforms for each macromodel. For example, consider constructing

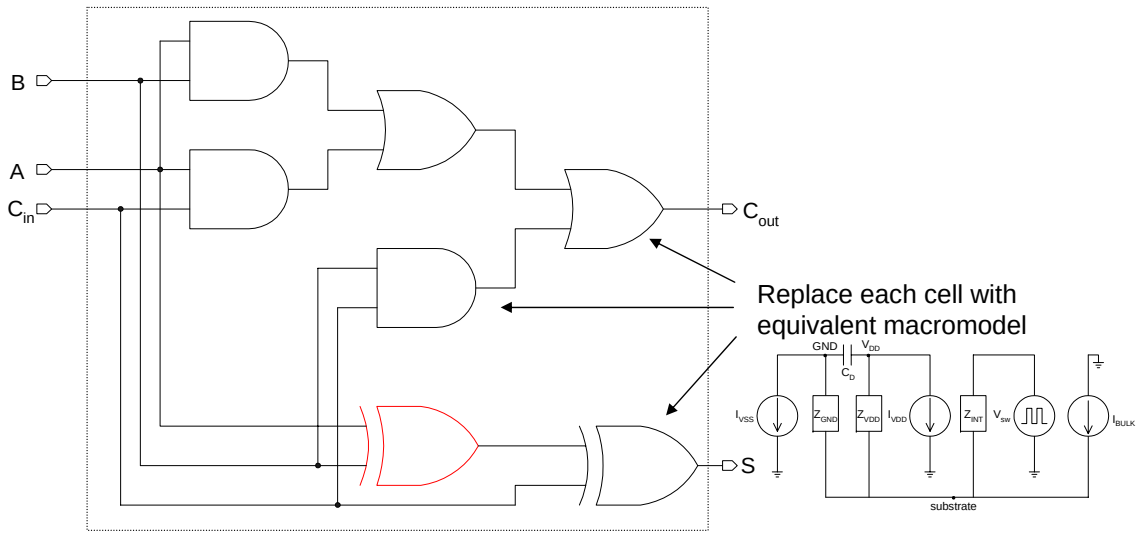


Figure 6-10: One bit adder example.

```
module adder1b ( A, B, Ci, S, Co );
input  A, B, Ci;
output S, Co;
    wire n4, n5;
    AOI22X1 U7 ( .A0(B), .A1(A), .B0(n5), .B1(Ci), .Y(n4) );
    XOR2X1 U8 ( .A(A), .B(B), .Y(n5) );
    XOR2X1 U9 ( .A(Ci), .B(n5), .Y(S) );
    INVX1 U10 ( .A(n4), .Y(Co) );
endmodule
```

Figure 6-11: Synthesized verilog netlist for the one bit adder example.

the current profiles for the XOR gate highlighted in Figure 6-10. Figure 6-12 shows the node transitions. The event information indicates that node B switches from low to high at t=0.5 ns with a rise time of 0.1 ns. Node A remains low. The output switches from low to high as a result of the transition on node A.

With the information that node B transitions from low to high with a rise time of 0.1 ns while node A remains low, SNAT reconstructs the current profile using the stored current profile from the library pre-characterization. Because an output switching event occurred, SNAT calculates the output node capacitance, and reconstructs the current profile for the load. The resultant current profiles are shown in Figure 6-13.

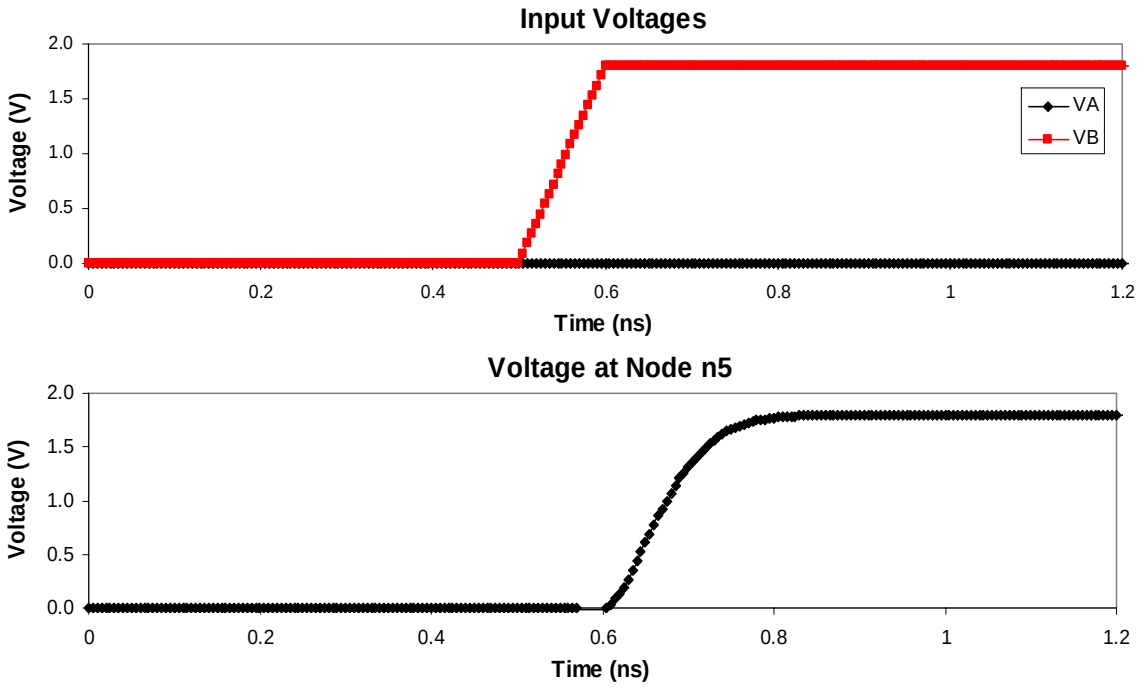


Figure 6-12: Node transitions for the XOR gate in the one bit adder example.

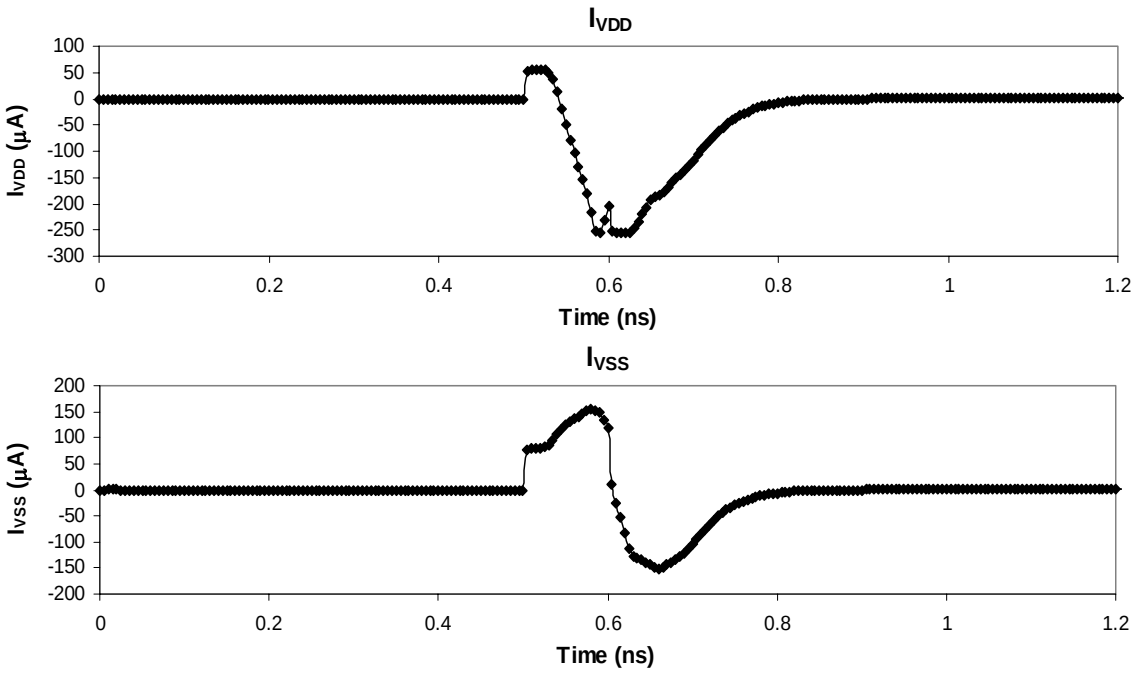


Figure 6-13: SNAT-constructed current profiles for the XOR gate in the one bit adder example.

The macromodel for the XOR gate is constructed by referring to the pre-characterization library for the other element values and combining this information with the constructed current and voltage profiles. This procedure is repeated for each of the standard cells in the design.

The resultant macromodels are combined together with a substrate model to form the final circuit. This is shown in Figure 6-14. Because of the small size of the circuit, a single substrate node was assumed. If a non-epi substrate is used, the macromodels are combined with a substrate model as shown in Figure 6-15.

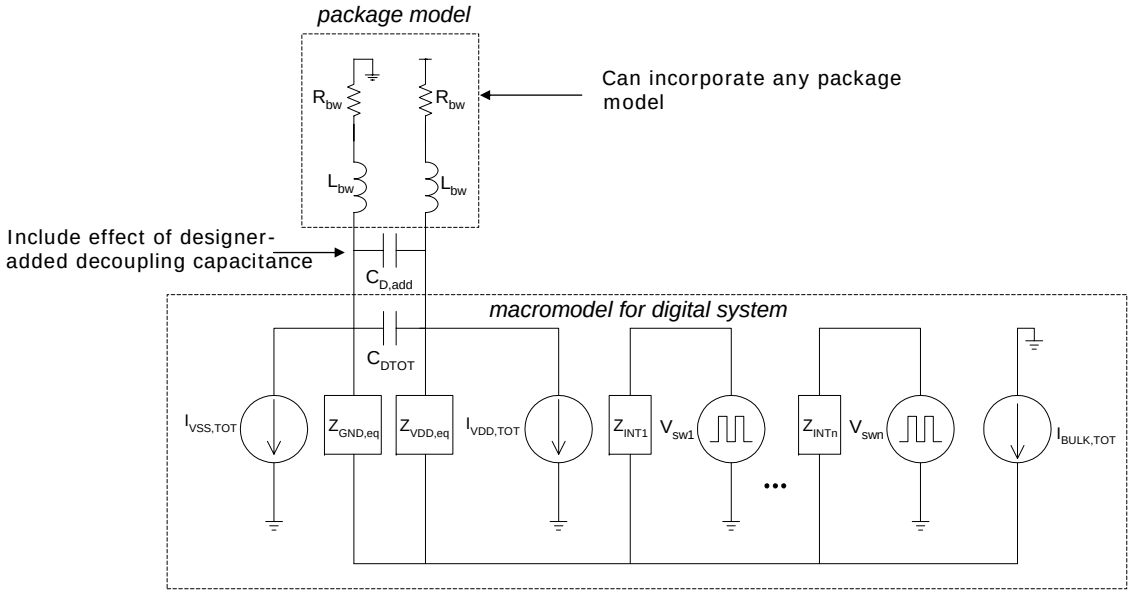


Figure 6-14: Equivalent circuit generated by SNAT for the one bit adder.

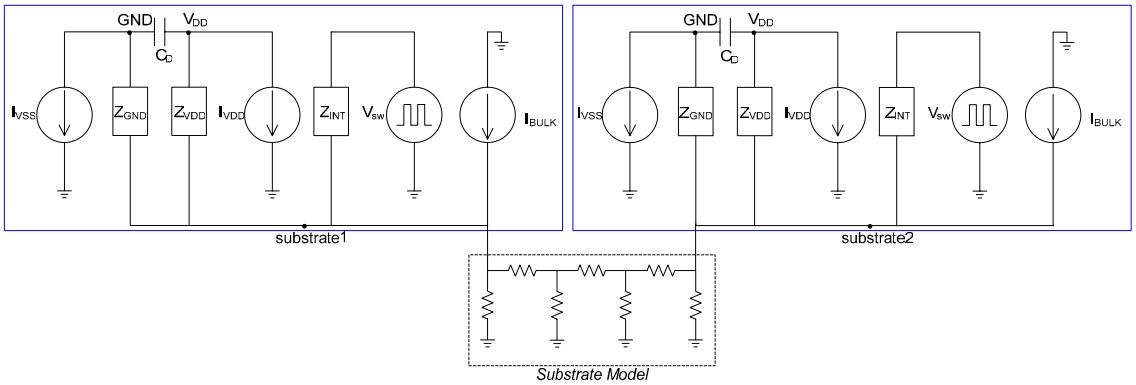


Figure 6-15: Equivalent circuit generated by SNAT for a system on a non-epi substrate.

The package plays an important role in the generated noise profile. The user must enter a package model. For this example, a simple series resistance and inductance is used to model the bondwire. The effect of user-added decoupling capacitance can also be considered. SNAT simulates this equivalent circuit to extract the substrate noise profile.

6.7 Summary

A CAD tool that can be used to predict substrate noise generation of any digital system at any point in the design cycle was presented. Simulation times are greatly reduced by using a macromodel approach. Further reduction in run time can be achieved at the expense of accuracy. The tool can be used at any stage in the design cycle from preliminarily evaluating the substrate noise performance to doing a full chip final verification.

Chapter 7

SNAT Comparison to SPICE and Measurements

7.1 Overview

Chapter 6 described the methodology behind SNAT. In this chapter, comparisons to both SPICE and measurements on fabricated circuits are presented [18]. Section 7.2 compares the results of SNAT with that of SPICE for several test circuits. Section 7.3 compares the results of SNAT with that of a fabricated circuit. The test circuit is a digital PLL (DPLL) implemented in TI's 90 nm process. Section 7.4 demonstrates how the isolation plug-in of SNAT could be used. Section 7.5 shows how each of the elements in the macromodel changes for future scaled technologies. Finally, Section 7.6 shows how SNAT performs over several technology generations.

7.2 SPICE Comparison

7.2.1 Benchmark 1: Cascaded Inverter Circuit

In this section, comparisons to a full transistor level simulation using SPICE are performed. More information on the full transistor level simulation methodology is presented in Chapter 2.

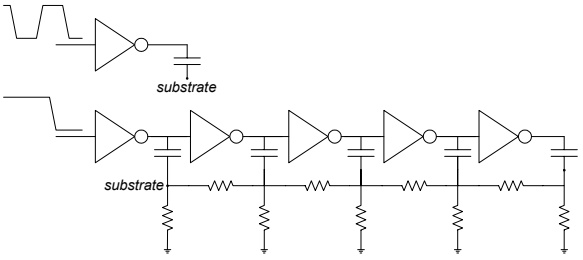


Figure 7-1: Cascaded inverter circuit.

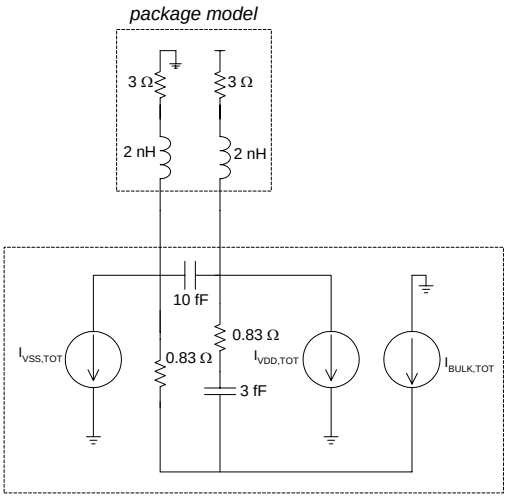


Figure 7-2: Equivalent SNAT model.

First, consider a simple test circuit consisting of cascaded inverters as shown in Figure 7-1. When the SPICE netlist describing this circuit is input into SNAT, the equivalent circuit generated is shown in Figure 7-2. For this example, because the size of the circuit is small, a single substrate node is assumed. This results in a common substrate node amongst the individual macromodels. The single substrate node allows the elements of the macromodel to be added according to network theory. Equations 7.1-7.6 show how the elements add. The voltage sources corresponding to switching nodes cannot collapse so each will appear in the equivalent circuit. SNAT simulates the equivalent circuit that represents the collapsed macromodels.

Figures 7-4(a) and 7-4(b) show the results of both the SPICE and SNAT simulation. In the time domain, the substrate noise voltage generated by SPICE looks like the SNAT profile but with an additional high frequency component. There is good correlation between the SPICE and SNAT simulations in the frequency domain up until approximately 15 GHz where the SNAT simulation starts to deviate significantly. This indicates that the high frequency component is above 15 GHz. The inability of SNAT to accurately predict the high frequency component is a result of using lumped impedances from both ground and V_{DD} to substrate in the macromodel as discussed in Chapter 6. SNAT's prediction of the RMS voltage is accurate to within 5% of the full transistor level simulation.

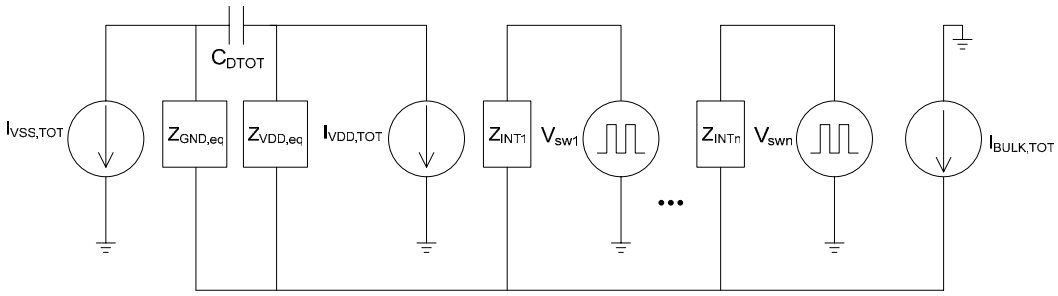


Figure 7-3: Equivalent circuit generated from collapsed macromodels. Element values are given by Equations 7.1-7.6.

$$I_{VDD,TOT} = \sum I_{VDD,i} \tag{7.1}$$

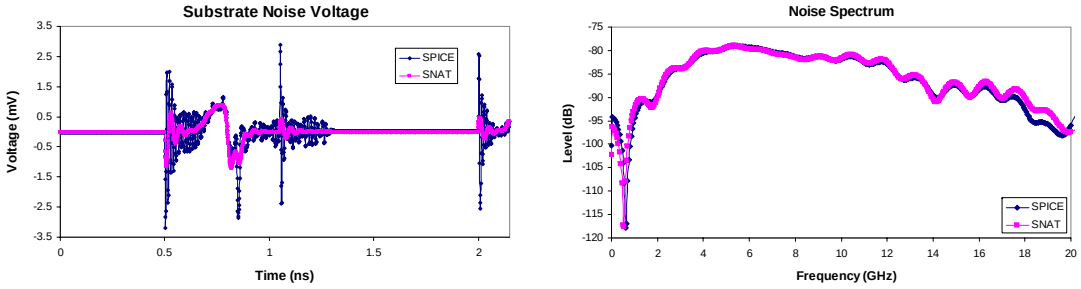
$$I_{VSS,TOT} = \sum I_{VSS,i} \tag{7.2}$$

$$I_{Bulk,TOT} = \sum I_{Bulk,i} \tag{7.3}$$

$$Z_{VDD,TOT} = \left(\sum \frac{1}{Z_{VDD,i}} \right)^{-1} \tag{7.4}$$

$$Z_{GND,TOT} = \left(\sum \frac{1}{Z_{GND,i}} \right)^{-1} \tag{7.5}$$

$$C_{D,TOT} = \sum C_{D,i} \tag{7.6}$$



(a) Time domain. (b) Noise spectrum.

Figure 7-4: Comparison between SPICE and SNAT for the cascaded inverter circuit in Figure 7-1.

7.2.2 Simulation of the Effect of Substrate Noise on an LNA

The results of the simulation can be used to simulate the effect of the noise on analog circuits. In this section, the effect of the substrate noise generated by the cascaded inverter circuit of Figure 7-1 on an LNA is simulated. Two simulations are performed. The first simulation is performed using SPICE with a 1.5 GHz input carrier signal and substrate noise generated from a full transistor level simulation of the cascaded inverter circuit. A second simulation is performed under the same test conditions; however, the substrate noise generated from SNAT is included instead. Figure 7-5 shows the LNA schematic and the two noise signatures used.

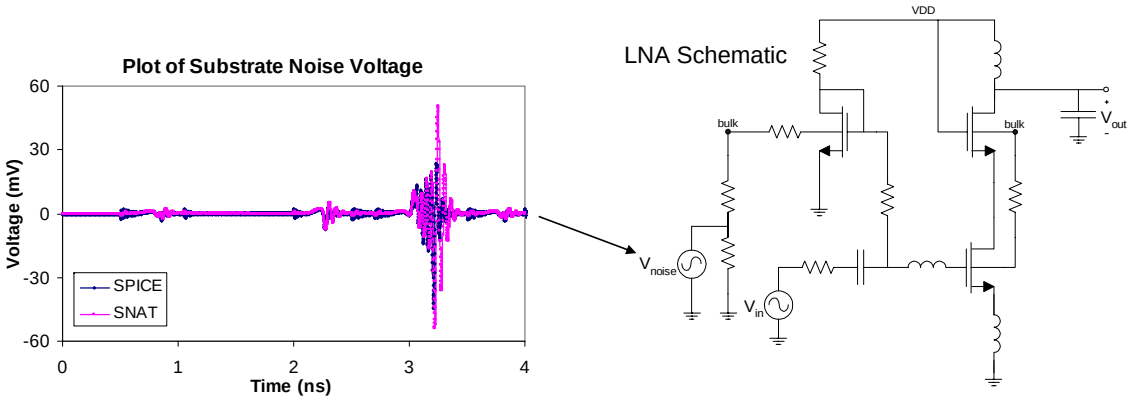
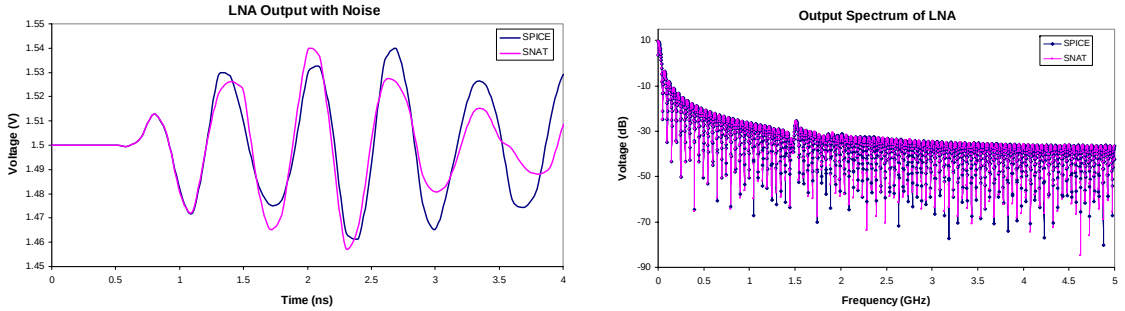


Figure 7-5: Substrate noise patterns and LNA schematic.

The results of the simulation are shown in Figures 7-6(a) and 7-6(b). There is good correlation between the SNAT simulation and the full transistor level simulation.



(a) Time domain. (b) Noise spectrum.

Figure 7-6: LNA output with a 1.5 GHz input signal and substrate noise.

7.2.3 Benchmark 2: Noise Generator

The second benchmark is a noise generator designed in TI's 90 nm technology. This configurable noise generator consists of assorted logic to drive large buffers to create significant levels of noise. The circuit consists of approximately 1200 gates (roughly 7800 transistors). A full transistor level simulation takes 43 minutes. The SNAT simulation takes approximately two minutes. Figure 7-7 shows the substrate noise voltage generated from the transistor level simulation and from SNAT. The RMS substrate noise voltage from the SNAT simulation is accurate to within 3.8% of SPICE.

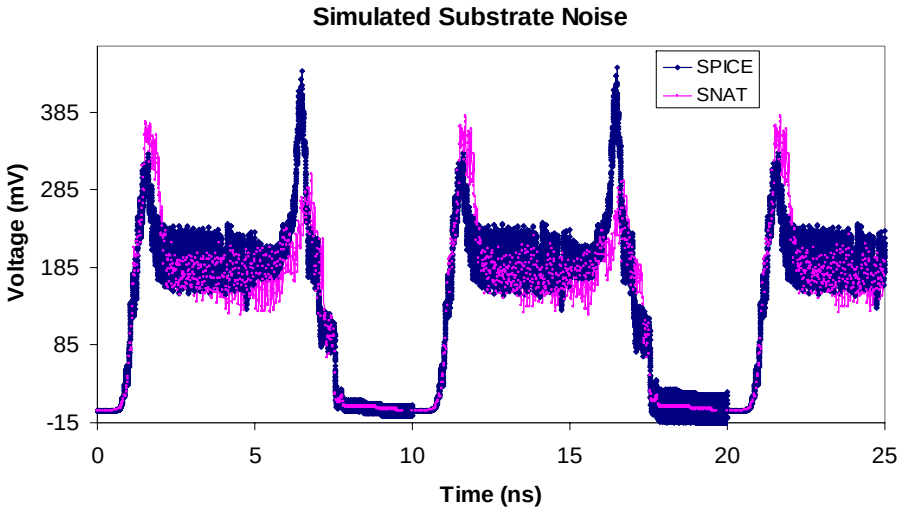


Figure 7-7: Comparison between SPICE and SNAT for a noise generator.

7.3 Measurement Comparison

To verify the results of SNAT, the simulation results were compared to measurements on a fabricated circuit. The test chip is a digital PLL fabricated in Texas Instruments' 90 nm CMOS technology. The block diagram of the DPLL is shown in Figure 7-8.

The DPLL is a medium-scale circuit with roughly 10K-20K gates. The chip was fitted with four p+ substrate contacts surrounding the system core that acted as substrate noise sensors (refer to Figure 7-9). The DPLL was configured to run with a reference clock frequency of 80 MHz and an output clock frequency of 480 MHz.

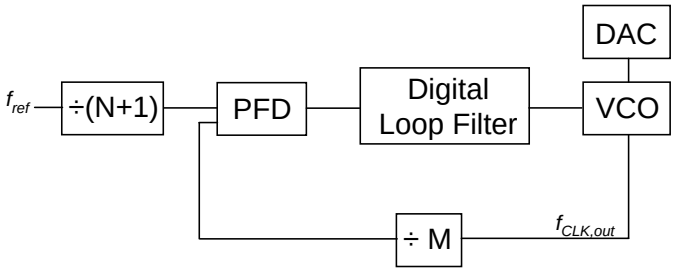


Figure 7-8: Block diagram of the DPLL.

The noise spectrum was measured using a spectrum analyzer. Due to measurement constraints, a time domain measurement could not be obtained.

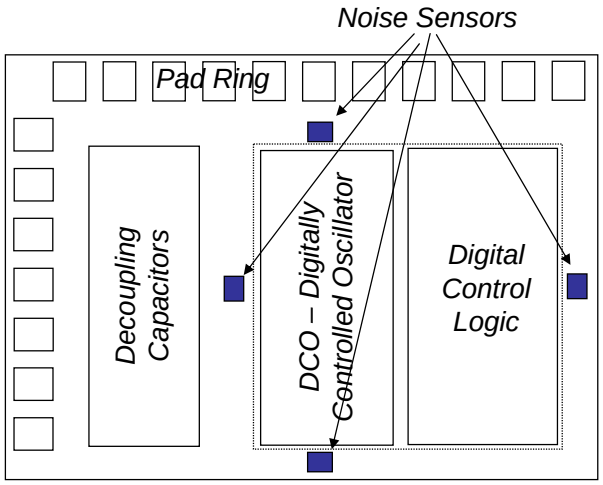


Figure 7-9: Floorplan of the DPLL.

7.3.1 Granularity Levels

SNAT was run over different granularity levels to determine the effect of each step in granularity on the overall accuracy of the simulation. Figures 7-10 and 7-11 show the granularity levels used for both the circuit and technology descriptions.

The least accurate granularity level on the circuit description side corresponds to a SPICE netlist with a less accurate event model. The main difference between a gate level netlist and a SPICE netlist with no parasitics is the event model. With a gate level netlist, the event model is generated from a gate level simulation. A SPICE

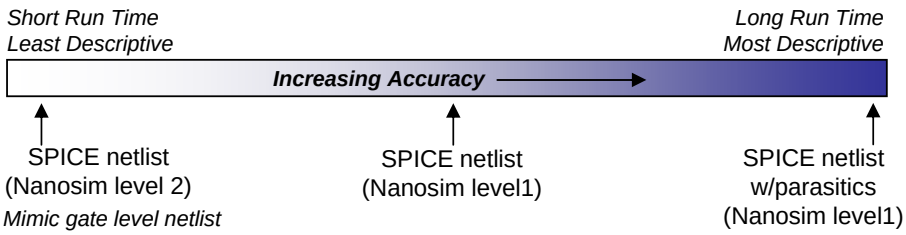


Figure 7-10: Circuit description granularity levels used in the DPLL SNAT simulation.

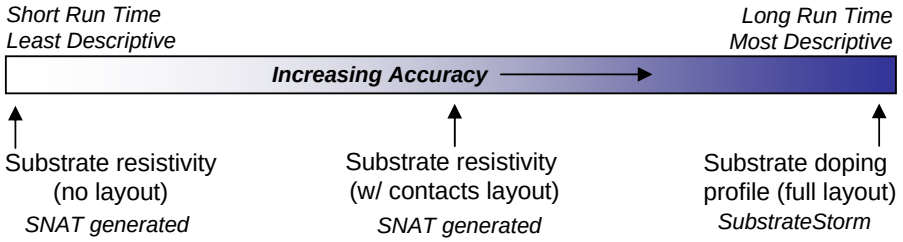


Figure 7-11: Technology description granularity levels used in the DPLL SNAT simulation.

netlist with no parasitics contains the same information as the gate level netlist; however, a more accurate event model can be generated using either SPICE or Nanosim [7]. A gate level netlist of the DPLL was not available for this study. However, the less accurate event model was mimicked by reducing an accuracy parameter in Nanosim. At this level, Nanosim uses a coarser algorithm to calculate node voltages and currents. The less accurate Nanosim simulation is referred to as Nanosim2. The Nanosim simulation generating the more accurate event model is referred to as Nanosim1.

The most descriptive granularity level for the circuit description is a SPICE netlist with extracted parasitics. Nanosim1 is used to generate the event model. It will be shown in Section 7.3.4 that parasitics play an important role in generating an accurate substrate noise profile.

On the technology description side, simulations were run over three granularity levels. The most accurate substrate model was generated using Cadence's SubstrateStorm with a modified circuit layout and substrate doping profile. The circuit layout had to be modified for substrate extraction so that the generated netlist would converge when simulated.

SubstrateStorm identifies single transistors and substrate contacts as noise injection locations. The tool uses the finite-difference method to generate the substrate model. This model is a mesh of resistances and well capacitances between all the noise injection points [42]. The resultant mesh for a large digital circuit can have millions of impedances. When SubstrateStorm is used to generate the substrate model for the DPLL from the modified layout, the generated substrate model consisted of approximately 1.7 million elements.

The modification made to the layout involved combining dense regions of diffusion into one region of equivalent area. This is referred to as de-densification and is shown in Figure 7-12. This de-densification procedure was verified on smaller test structures to have little effect on the substrate transfer function. As long as the regions of dense diffusion are not too large, the error induced through the replacement is not significant. The de-densification was written in Cadence's SKILL programming language [2].

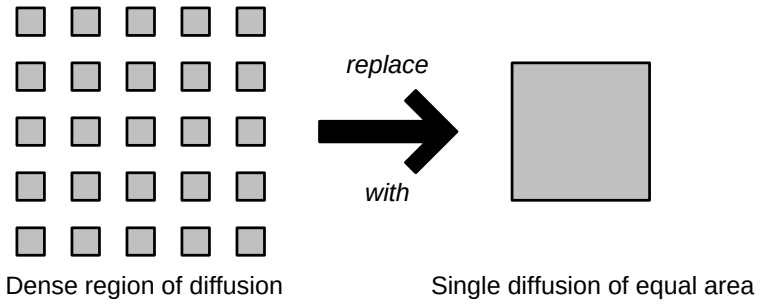


Figure 7-12: De-densification of dense regions of diffusion.

De-densification reduces the number of injection points that SubstrateStorm considers in generating the substrate model. Generating the substrate model from the modified layout took approximately 51 hours. When the original full layout was used, the SubstrateStorm substrate extraction step was terminated after one week as it was unable to provide a model within a reasonable time frame.

7.3.2 Description of Simulations

Simulations over 10 different granularity levels were performed to determine the effect of each step in granularity on accuracy. Table 7.1 describes the inputs at each granularity level. The run times for each step in the analysis are summarized in Table 7.2.

Table 7.1: Granularity level descriptions.

Level	*Event Model*	*Parasitics?*	*Substrate*
1	Nanosim2	no	SNAT+no layout
2	Nanosim2	no	SNAT+layout
3	Nanosim2	yes	SNAT+layout
4	Nanosim2	no	SubstrateStorm
5	Nanosim2	yes	SubstrateStorm
6	Nanosim1	no	SNAT+no layout
7	Nanosim1	no	SNAT+layout
8	Nanosim1	yes	SNAT+layout
9	Nanosim1	no	SubstrateStorm
10	Nanosim1	yes	SubstrateStorm

7.3.3 Event Model

The effect of the different event models on the accuracy of the simulation is discussed in this section. The Level5 simulation and the Level10 simulations are compared. Both netlists include circuit parasitics so that all noise sources are modeled as accurately as possible. In addition, the substrate model from SubstrateStorm is used as it is the most accurate so that the effect of the different event models can be extracted. The effect of the less accurate event model is that the current pulses will not be modeled as accurately. Figure 7-13 shows the time domain noise generated from both simulations.

There is a slight offset between the two profiles as a result of the less accurate event model. Figure 7-14 shows a comparison of the percent error between the two simulations and measurements. Using the Nanosim2 event model results in a doubling of the error in the RMS voltage.

Table 7.2: Run times of each step.

Step	*Run Time*
Library Characterization	18 hrs
Nanosim1	56 min
Nanosim2	7.5 min
SubstrateStorm	51 hrs
SNAT+layout	14.5 min
SNAT+no layout	5 sec

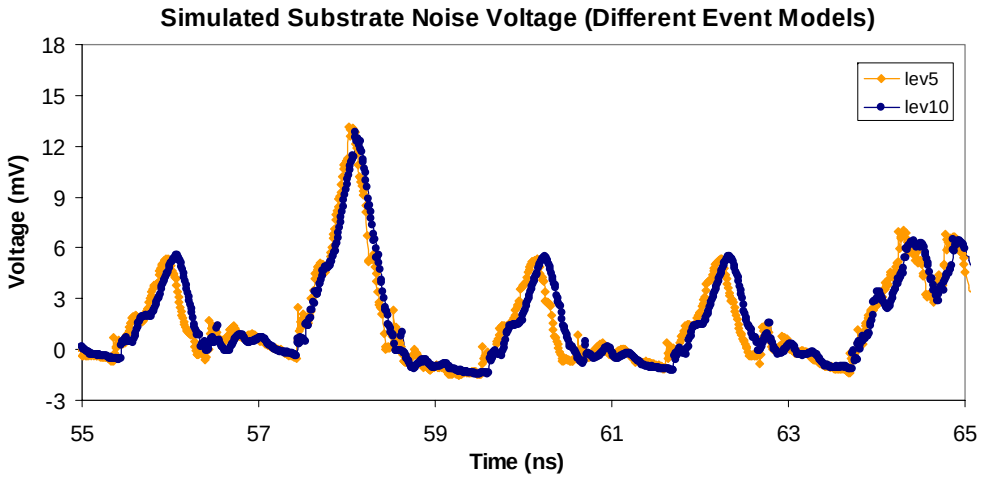


Figure 7-13: Simulated time domain noise for both event models. Level5 uses the less accurate model.

7.3.4 Effect of Parasitics

Figure 7-15 shows the noise spectrum generated for a granularity level of 9. At this granularity level, a SPICE level netlist with no parasitics and a SubstrateStorm-generated substrate model are used in the simulation. The simulated spectrum correlates very closely with that of the measured data with an error less than 15% for all tones with the exception of 80 MHz and 480 MHz, which show substantially higher error.

The increased error in the 80 MHz and 480 MHz components is a result of an incomplete parasitics model. 80 MHz and 480 MHz correspond to the input reference clock and output clock respectively. Both the reference clock and the output clock are connected externally; thus, the effect of pad parasitics need to be incorporated. The pad capacitance to substrate and capacitance from ESD structures were included

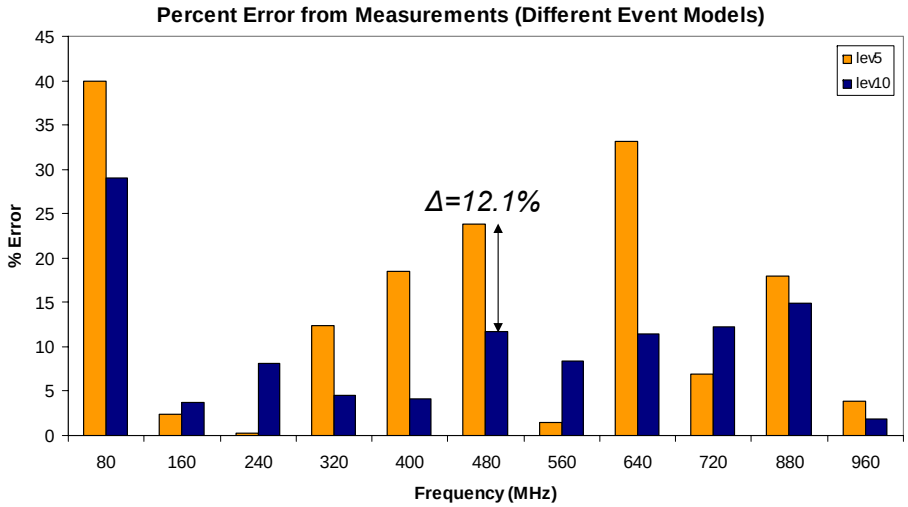


Figure 7-14: Percent error between SNAT and measurements. Level10 refers to the simulation using the more accurate event model (Nanosim1). Level5 uses the less accurate model (Nanosim2).

in the granularity level 10 netlist. The incorporation of these parasitics reduces the error of the two tones significantly resulting in only 11.7% error in the RMS voltage. Figure 7-16 shows the reduction in percent error with respect to measurements when circuit parasitics are included. A comparison between measurements and the most accurate SNAT simulation (granularity level=10) is shown in Figure 7-17

7.3.5 Substrate Model

The effect of each step in granularity on the technology description side is examined in this section. Simulation of the SubstrateStorm-generated substrate netlist together with the circuit netlist incorporating parasitics (granularity level 10) yields the least error when compared to measurements. However, the huge size of the substrate netlist (roughly 1.7 million elements) led to a very long simulation time (51 hours).

The granularity level one step below SubstrateStorm uses a substrate model generated by SNAT from the modified layout. While SubstrateStorm requires a full substrate doping profile, SNAT models the substrate as purely resistive and thus only requires the underlying substrate resistivity. Using the coarser model generated by SNAT, the simulation time of the substrate can be cut from 51 hours to less

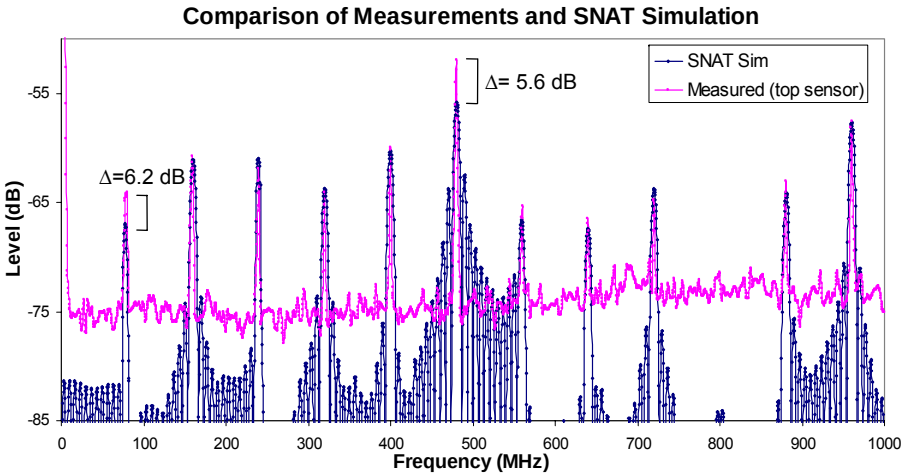


Figure 7-15: Noise spectrum at the top sensor location. Comparison between measurements (pink) and SNAT simulation (level 9 - no parasitics) (blue).

than 15 minutes. Figure 7-18 compares the substrate transfer function generated by SubstrateStorm to the transfer function of the SNAT-generated model.

Because SubstrateStorm uses a full substrate doping profile, the effects of wells and junctions are considered. These account for the frequency dependence in the transfer function. The substrate model plateaus at higher frequencies indicating that at these frequencies, the substrate can be modeled as purely resistive. SNAT models the substrate as purely resistive over the entire frequency range. This can result in reduced accuracy. For the DPLL, the error in predicting the lower frequency components increases since the attenuation provided by wells is neglected; however, the error in the RMS voltage is not significantly affected. Figure 7-19 shows the percent error in each tone using the two models.

Referring to Figure 7-18 at 480 MHz, the SNAT-generated model and the SubstrateStorm generated model converge. This implies that the substrate is primarily resistive at this frequency. This is adequately modeled using SNAT's substrate model; thus, there is very little difference in the error in the RMS voltage for the two models. However, for the rest of the tones, the error approximately doubles when using the SNAT-generated model. Figure 7-20 shows the effect of the coarser substrate model in the time domain.

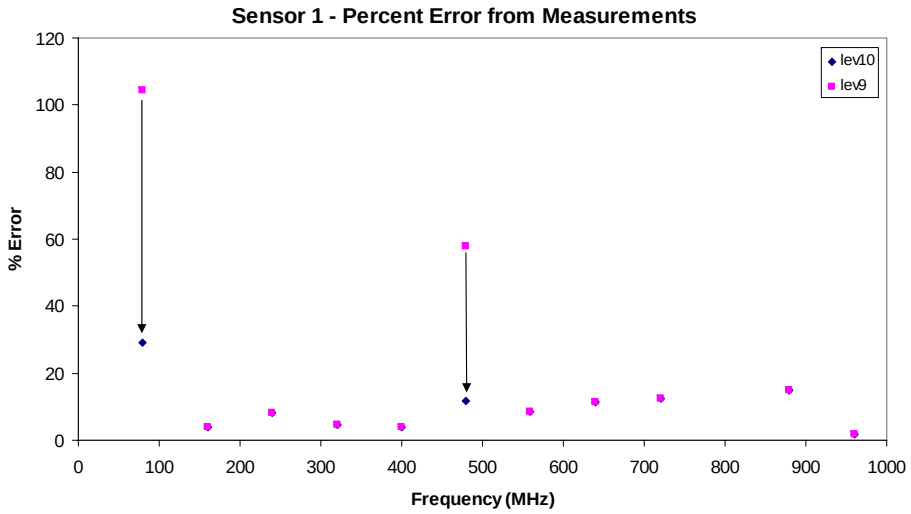


Figure 7-16: Percent error between SNAT and measurements with and without the inclusion of circuit parasitics.

With no layout information, the error in the RMS voltage increases significantly since both the capacitive attenuation of the wells is ignored, and the resistive attenuation of the substrate is modeled less accurately. Figure 7-21 shows the increase in error as the substrate model is changed. By using the SNAT-generated model with no layout, the error increases to 462%. Examining the transfer function gives insight into the large increase in error. Figure 7-22 shows the transfer functions over all three models.

It is expected that the SNAT-generated model with no layout would over-predict the substrate attenuation. If a design contains many p+ diffusion regions, a lot of coupling between nodes occurs reducing the substrate attenuation. If SNAT were used to generate the substrate model for the same design knowing only the die size, it would predict more attenuation as it has no knowledge of the large number of p+ diffusion regions that are causing the attenuation to suffer.

Even though the error is large, a simulation at this level can yield useful information as it gives an idea of the order of magnitude of the noise. For example, during floorplanning, only a rough estimate of the noise is required. The tool could be used to determine which blocks of a digital design create the most noise so that measures can be taken to mitigate the noise coupling from these blocks. These measures in-

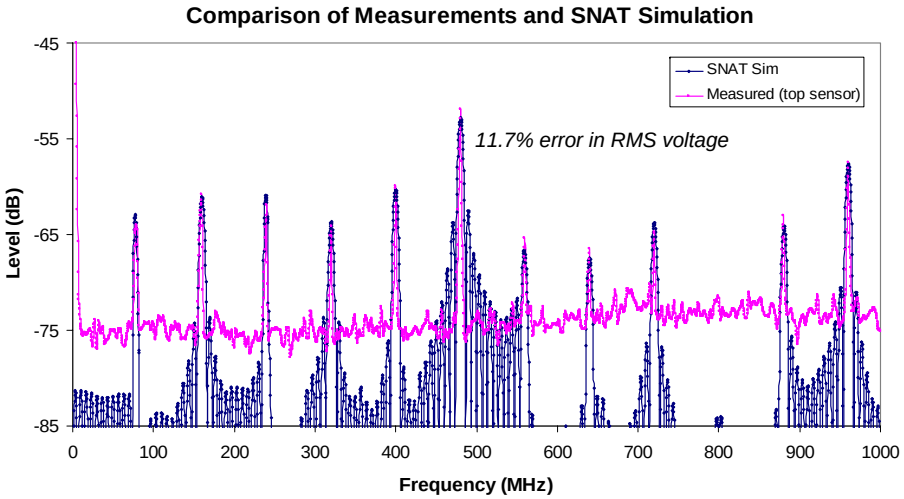


Figure 7-17: Noise spectrum at the top sensor location. Comparison between measurements (pink) and the most accurate SNAT simulation (blue).

Table 7.3: Percent error of each tone for different granularity levels.

f(MHz)	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*
80	29.1	104.5	55	28.6	184.1	39.9	121.8	51.2	22.6	208.1
160	3.8	3.8	45.3	45.3	117.9	2.4	2.4	46	46	115.1
240	8.1	8.1	39.4	39.4	141.1	0.3	0.3	34.3	34.3	161.4
320	4.5	4.5	27.2	27.2	189.8	12.4	12.4	33.2	33.2	165.9
400	4.1	4.1	12.5	12.5	248.4	18.5	18.5	0.4	0.4	296.7
480	11.7	57.8	12.1	41.2	462	23.8	55.9	10.8	39.4	455.2
560	8.4	8.4	15	15	238.3	1.4	1.4	5.9	5.9	274.7
640	11.5	11.5	5.4	5.4	319.4	33.1	33.1	36.8	36.8	151.5
720	12.3	12.3	16.8	16.8	231.2	7	7	11.7	11.7	251
880	15	15	7	7	325.8	18	18	9.8	9.8	337.2
960	1.8	1.8	7	7	270.3	3.9	3.9	12.2	12.2	249.5

clude placing the noisy blocks far from sensitive analog circuits or placing guard rings around them.

Table 7.3 summarizes the accuracy in predicting each tone of the noise spectrum for all the granularity levels.

7.3.6 Other Sensor Locations

The results shown above are for measurements from the top sensor. Referring to Figure 7-9, there are three other sensor locations surrounding the core of the DPLL. Sim-

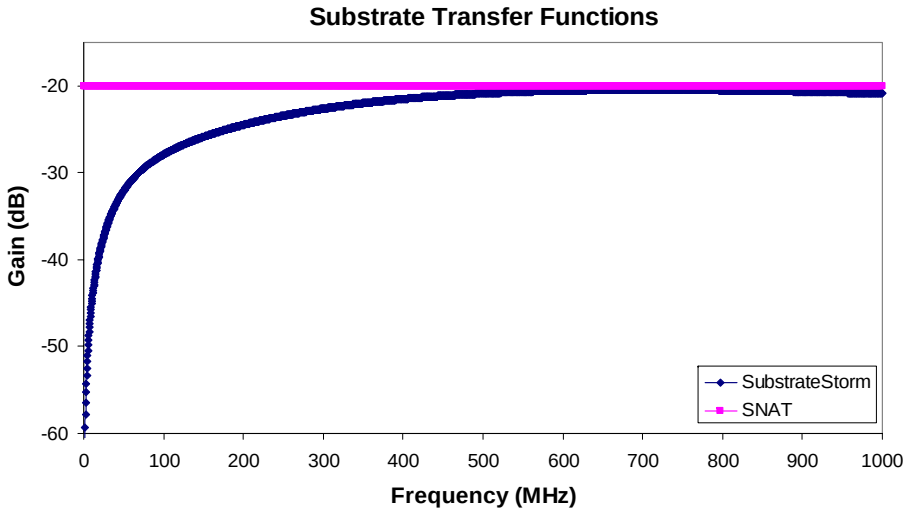


Figure 7-18: Transfer functions for the SubstrateStorm-generated model and the SNAT-generated model.

ulations and measurements were also compared for the other sensors. Figure 7-23(a) shows the noise spectrum probing the right sensor location. Figure 7-23(b) shows the noise spectrum of the top sensor location as a reference. The SNAT simulations were run for a granularity level of 10. Excellent correlation between the measurements and the simulation is achieved because the sensor location dependence is accounted for in the substrate model. SNAT even accurately predicts the attenuation of the 560 MHz tone when probing the right sensor location.

The same trends in accuracy over granularity level are also observed as shown in Figure 7-24. Both the SubstrateStorm-generated substrate model and the SNAT-generated model from layout correctly encapsulate the sensor location dependency of the received substrate noise. However, the SNAT-generated model with no layout does not incorporate the location dependence.

7.4 Isolation Plug-in

SNAT includes a plug-in that can be used to determine the effect of different isolation structures on the substrate noise profile. Figure 7-25 shows the simulated isolation if the DPLL were fabricated on an epi substrate. The amount of noise increases greatly

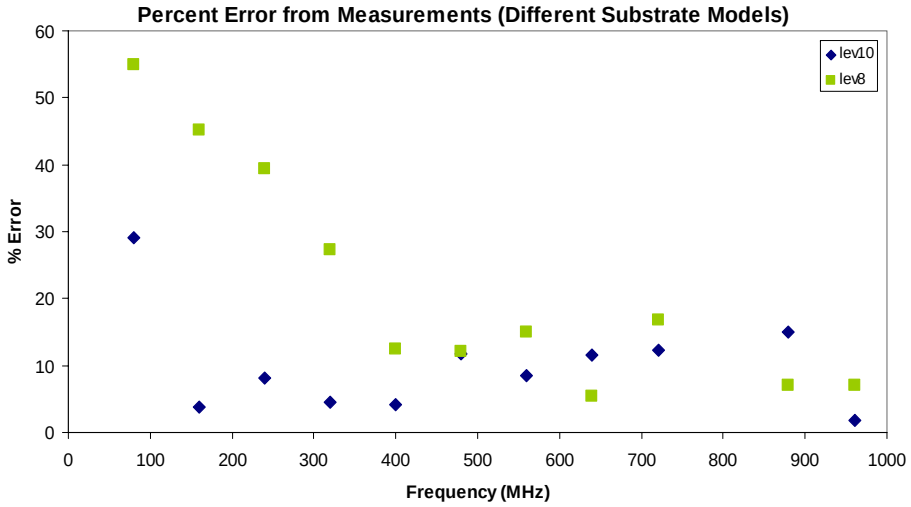


Figure 7-19: Percent error between SNAT and measurements. The green squares represent the error using the SNAT-generated substrate model from layout. The blue diamonds represent the error using the SubstrateStorm-generated model.

because the substrate now acts as a single node and yields no attenuation from one point to another. The simulated substrate noise on the non-epi substrate is shown as a reference.

In addition, the effect of a 10 μm wide guard ring surrounding the periphery of the DPLL but inside the substrate noise sensors was simulated. Because the frequency range of interest is quite low, the guard ring was very effective, attenuating the noise by 30 dB. The peak substrate noise without the guard ring was 13.3 mV. With the addition of the guard ring, the peak substrate noise reduces to 0.42 mV. The time domain noise profile is shown in Figure 7-26.

7.5 Noise Macromodel and Technology Scaling

The effect of scaled technologies on the noise sources in the macromodel are discussed here. A current source directly into the substrate is used to represent the contribution from impact ionization. Equation 7.7 shows the expression for impact ionization [38]. In Equation 7.7, k_1 and k_2 are semi-empirical constants. The impact ionization current depends exponentially on the power supply voltage. Because power supply voltages are scaling down for future technology nodes, the contribution of impact

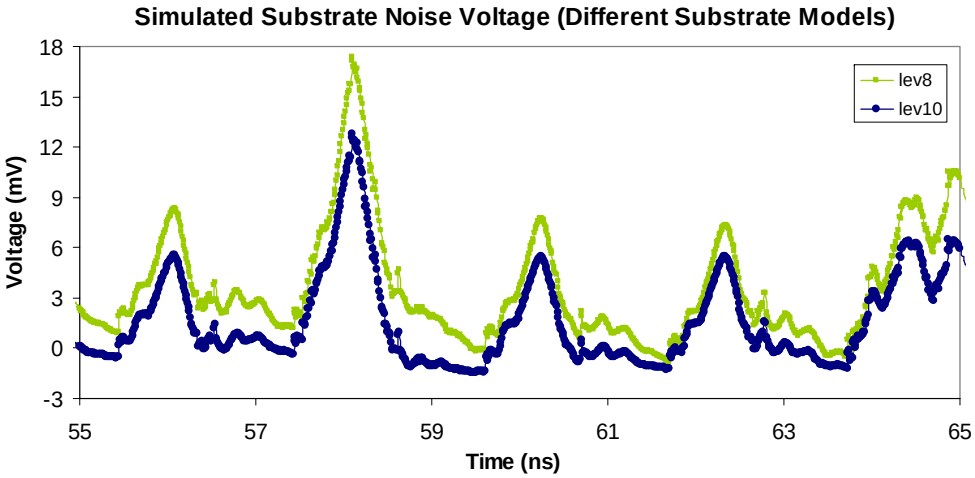


Figure 7-20: Simulated time domain noise. Level10 uses the SubstrateStorm-generated substrate model. Level8 uses the SNAT-generated substrate model.

ionization currents diminishes [15].

$$I_{sub} = k_1(V_{ds} - V_{ds,sat})I_d \; exp(\frac{-k_2}{V_{ds} - V_{ds,sat}}) \tag{7.7}$$

The contribution of switching interconnect is represented in the macromodel with a voltage source and an impedance to the substrate. Consider the noise injected from a switching drain. This is represented with a voltage source and a capacitance to substrate that is set by the drain to bulk junction capacitance. The noise current injected from this source is given by the following equation.

$$I_{sub,int} = C_j \frac{dV}{dt} \tag{7.8}$$

For scaled technologies, the drain to bulk capacitance, C_j, reduces. Both the supply voltage and the rise and fall times scale down with technology. Assuming that the downscaling of both the supply voltage and the rise times offset each other, the contribution of switching interconnect reduces with scaling.

Power supply noise is represented in the macromodel with a current source and an equivalent impedance. Both I_{VDD} and I_{VSS} scale in the same manner so for simplicity, only I_{VSS} is considered here. IMEC evaluated the contribution of power supply coupling for scaled technologies [15]. They found that the effect of scaling

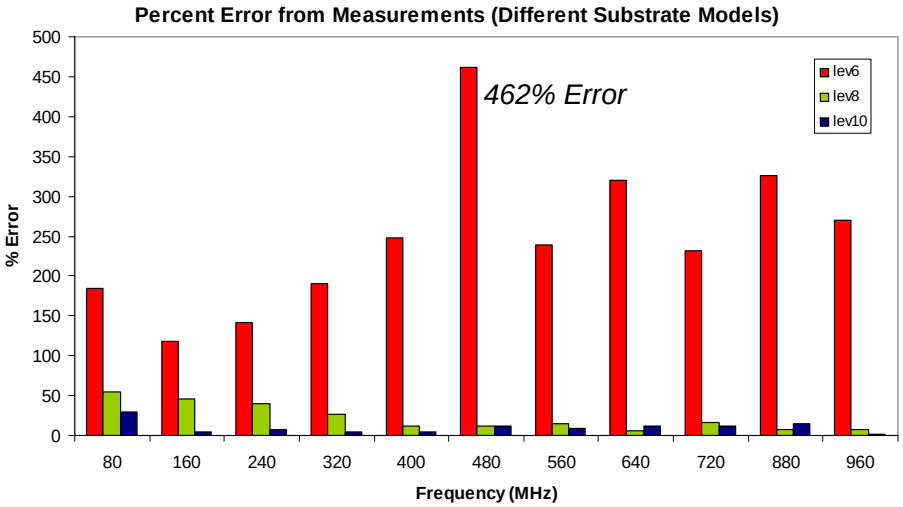


Figure 7-21: Percent error between SNAT and measurements for the different substrate models. Level6 uses the SNAT-generated substrate model with no layout. Level8 uses the SNAT-generated model with a layout. Level10 uses the SubstrateStorm-generated substrate model.

depended on the type of circuit. For small-scale circuits, the external power supply provides most of the switching current. In this case, the dependence of I_{VSS} is given by the following equation.

$$I_{VSS} = \frac{L_{bwg}}{R_{p+}} \frac{di}{dt} \tag{7.9}$$

The di/dt term scales up the fastest in Equation 7.9; thus, I_{VSS} increases with technology scaling. For large-scale circuits, the peak value of I_{VSS} is largely set by the switching activity. As a result, I_{VSS} is unaffected by technology scaling. The impedance associated with I_{VSS} is set by the underlying substrate resistivity that is independent of technology scaling. The impedance associated with I_{VDD} typically consists of a series capacitance and resistance associated with the n-well for an n-well process. The resistance is unaffected by scaling; however, the capacitance reduces.

7.6 SNAT and Technology Scaling

SNAT has been verified for designs in two technology nodes: 0.18 μm and 90 nm. Because SNAT uses models based on current profiles from SPICE, the methodology

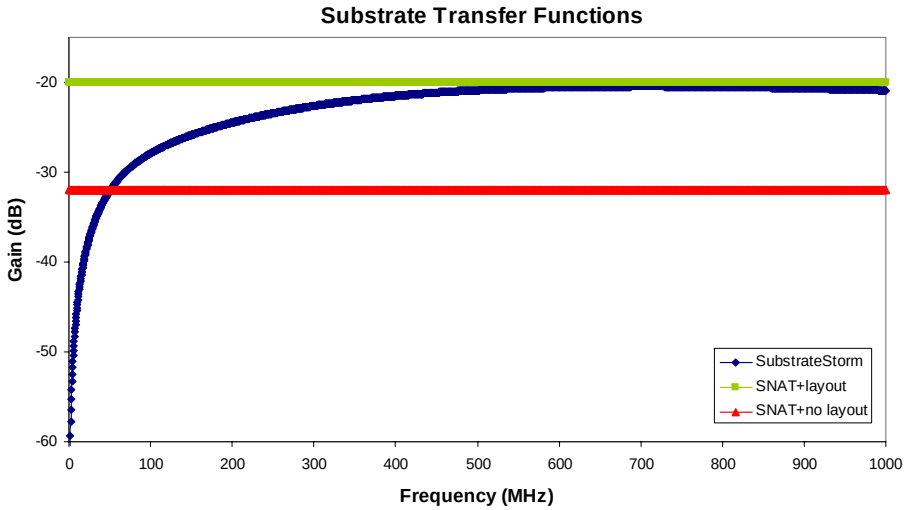


Figure 7-22: Transfer functions for the SubstrateStorm-generated model, the SNAT-generated model from layout, and the SNAT-generated model with no layout.

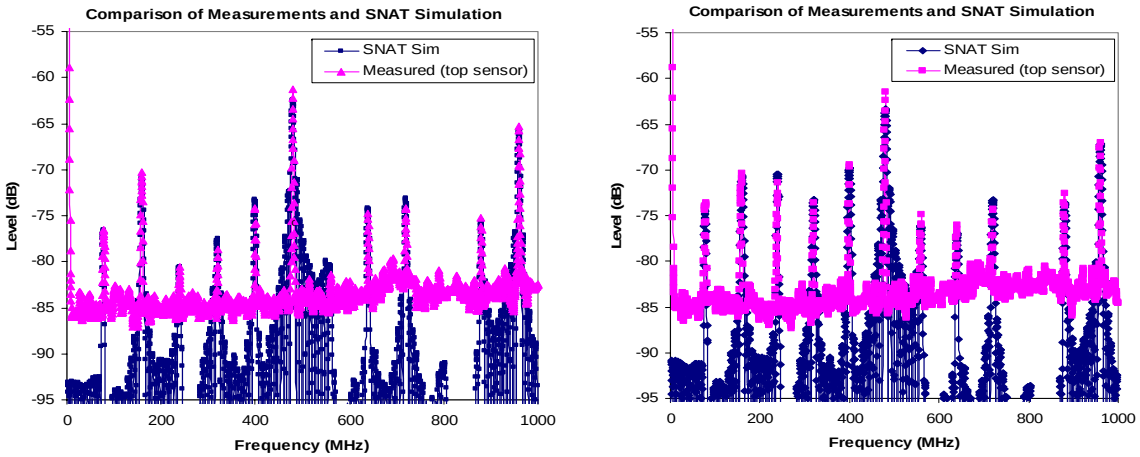
is accurate for future technology nodes. Berkeley's predictive technology models [1] for 65 nm and 45 nm were used to compare the results of a SNAT simulation to that of a full transistor level simulation using SPICE. Figure 7-27 shows the comparison for three technology nodes: 0.18 μm, 65 nm, and 45 nm. Good correlation is achieved between the SNAT and SPICE simulations. Table 7.4 shows that the percent error does increase slightly for the scaled nodes.

Table 7.4: Percent error between SNAT and SPICE for future technologies.

0.18 μm	65 nm	45 nm
9.5%	10.68%	13.6%

7.7 Summary

The results of the CAD tool developed in this thesis, SNAT, were compared to full transistor level simulations and data on a fabricated circuit in TI's 90nm technology. SNAT can be used at any stage of the design cycle to accurately predict the substrate noise performance of any digital circuit with a large degree of computational efficiency. For a medium-scale circuit, SNAT can yield an order of magnitude estimate within minutes and an extremely accurate answer in two days.



(a) Right sensor.

(b) Top sensor.

Figure 7-23: Comparison between measurements (pink) and SNAT (blue) for two sensor locations.

SNAT not only predicts the substrate noise performance with good accuracy (less than 12% error when compared to measurements) but also provides users flexibility in trading off accuracy for run time depending on the user's requirement.

Knowing the substrate noise profile of a digital system only after the design has been fully completed inhibits any re-design. If a less accurate estimate could be generated earlier in the design cycle, the full benefits of the information could be reaped. To this end, SNAT can be used at any stage in the design flow and does so in trading off accuracy for speed.

The fast simulation time of SNAT allows the designer to experiment and evaluate various circuit and layout techniques to mitigate substrate noise.

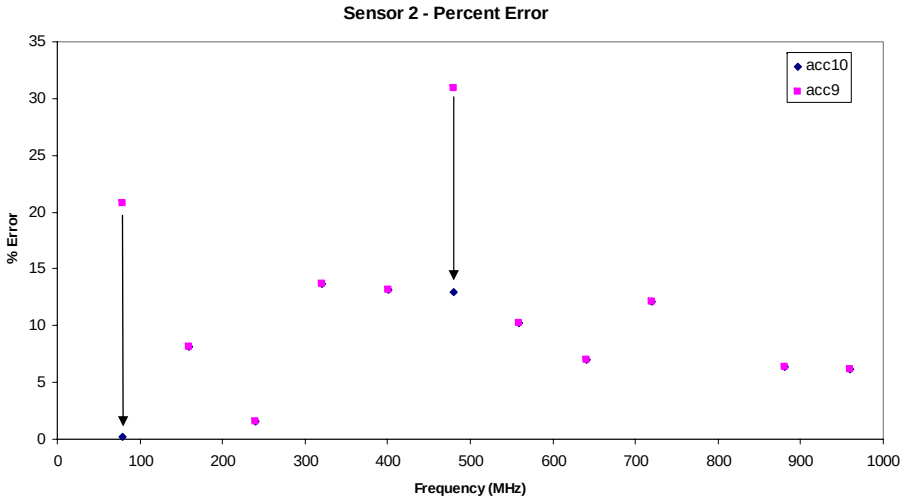


Figure 7-24: Percent error between SNAT and measurements at the right sensor location with and without circuit parasitics.

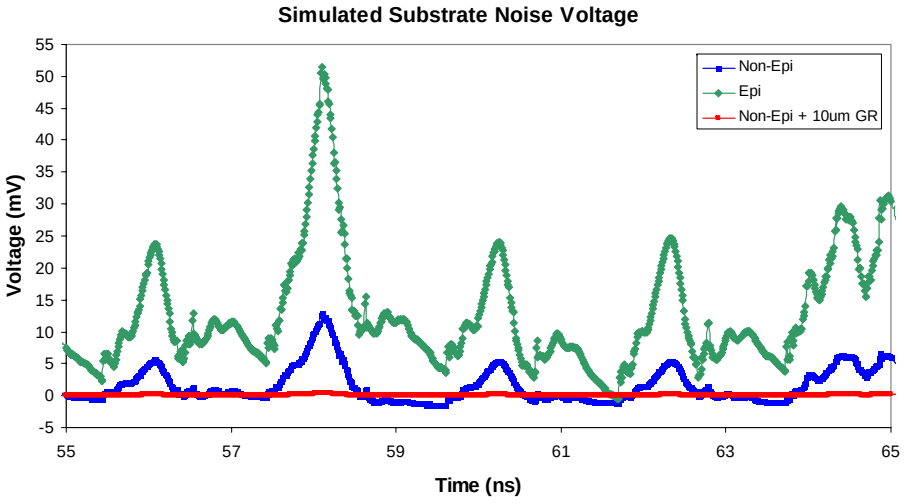


Figure 7-25: SNAT simulation for the DPLL on epi, non-epi, and non-epi with a 10 μm guard ring.

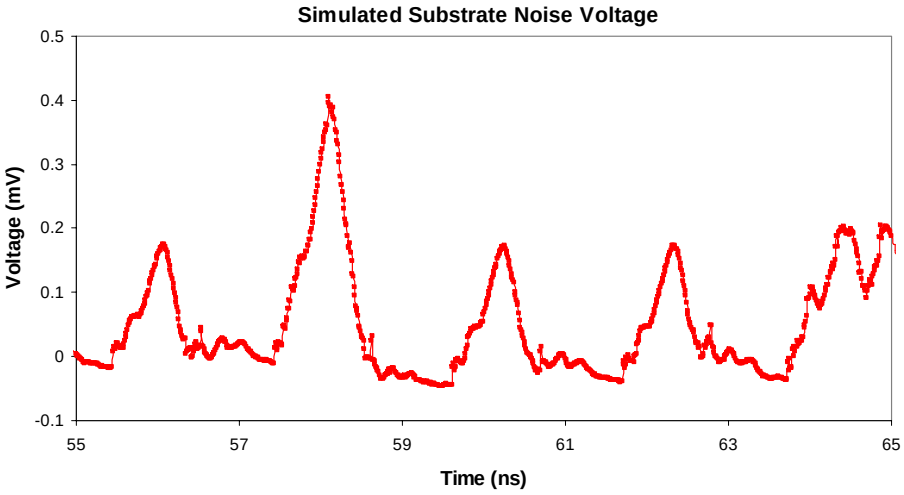
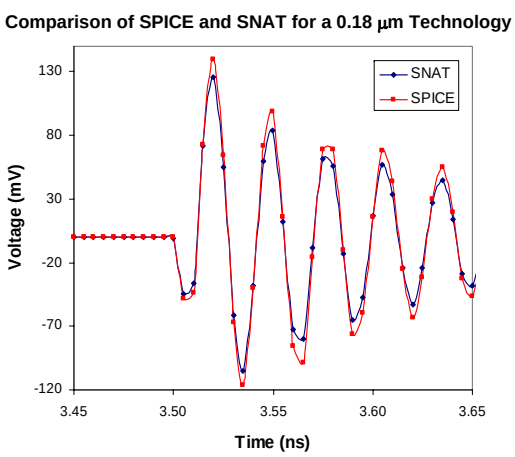
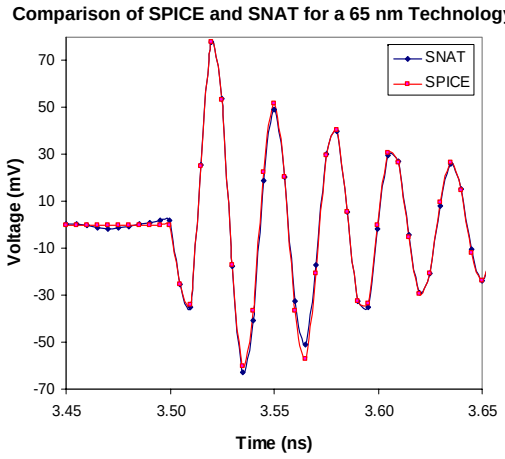


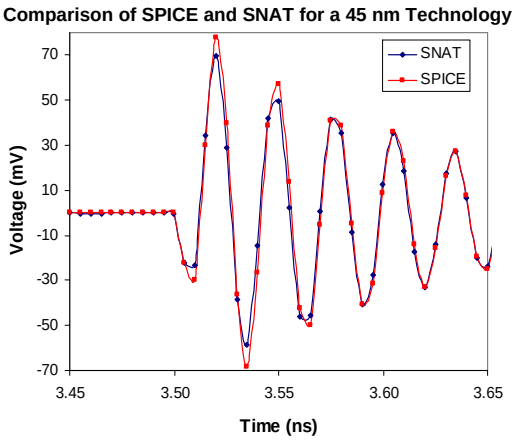
Figure 7-26: SNAT simulation for the DPLL on a non-epi substrate with a a 10 μm wide guard ring.



(a) 0.18 μm.



(b) 65 nm.



(c) 45 nm.

Figure 7-27: SNAT and SPICE simulation comparisons for future technologies.

Chapter 8

Noise Guidelines

8.1 Overview

In order to mitigate the effect of substrate noise in mixed-signal systems, the fundamental mechanisms behind substrate noise need to be altered. These mechanisms are generation, propagation, and reception and were discussed in detail in Chapter 3. Techniques to improve the substrate noise performance of a mixed-signal system are discussed in this chapter.

Techniques to reduce the amount of noise generated and are discussed in Section 8.2. Most approaches to reduce the effect of substrate noise alter the propagation mechanism through the use of isolation structures. These structures were discussed in detail in Section 3.5 of Chapter 3. In Section 8.3, some guidelines in choosing the appropriate isolation structure for a particular application are discussed. Finally, circuit techniques to alter the reception mechanism are discussed in Section 8.4.

8.2 Reducing Coupled Noise

This section discusses both low noise architectures that can be implemented to reduce the amount of substrate noise injected and guidelines that are more generic to all designs.

8.2.1 General Guidelines

Noise is generated in digital systems through switching inputs and outputs, impaction ionization, and power supply noise. The amount of noise injected through capacitive coupling depends on the capacitance of the node, the rise and fall time of the switching signal, and the frequency of the that signal. Supply networks, output drivers, and clock distribution networks all have large capacitances to substrate. These capacitances are difficult to minimize as other constraints such as timing and power set the size of these interconnects. Fast voltage transitions on these nodes will couple significant levels of noise into the substrate. To minimize this coupling, rise and fall times should be set as large as the design constraints will allow. Slowing the transition time not only reduces the capacitively coupled noise but also reduces the current transient drawn from the supply resulting in a reduction of the power supply noise.

Furthermore, timing tricks to minimize the instantaneous current drawn from the power supply also reduce the amount of substrate noise. Drivers pull large amounts of current from the supply. By offsetting the switching timing instants of these drivers, the instantaneous current demand can be reduced.

The amount of capacitive coupling reduces with technology scaling as depletion capacitances scale down with decreasing feature sizes. In addition, reduced output voltage swing also reduces the coupled noise [15].

Coupling from the power supply contributes the most substrate noise. During logic transitions, current spikes from the supply are used to charge the output load. These current spikes flow through the parasitics of the package and bond wires to induce ringing on the power and ground lines. The substrate is connected to ground through low resistance substrate contacts; thus, any noise that appears on the ground line appears on the substrate.

On-chip decoupling helps to keep the supply current constant by locally supplying the required charge [28]. Decoupling minimizes fluctuations on the supply lines; however, the addition of on-chip decoupling will lower the package resonant frequency. Thus, care must be taken to ensure that the circuit operating frequencies do not near

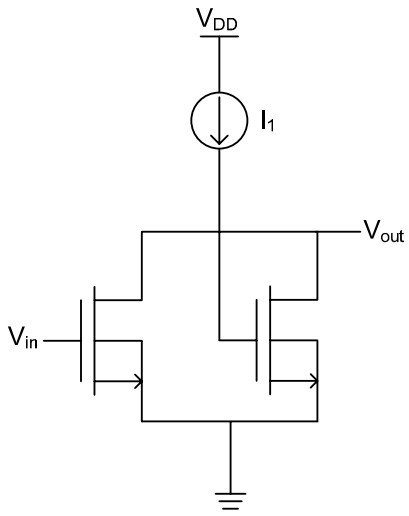


Figure 8-1: CSL inverter [10].

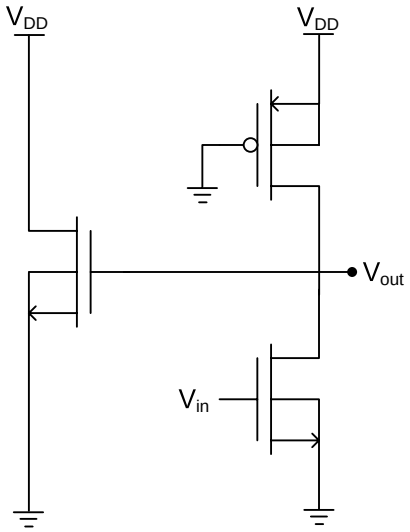


Figure 8-2: CBL inverter [9].

the package resonant frequency.

8.2.2 Low Noise Digital Architectures

The aim of low noise logic is to reduce power supply current spikes by keeping the output current constant or by reducing the output swing.

In current steering logic (CSL), the output swing is reduced thereby reducing the power supply current spike. A CSL inverter is shown in Figure 8-1 [10].

In current balanced logic (CBL), the supply current ideally remains constant during switching [9]. Figure 8-2 shows a CBL inverter.

At higher package inductance values, CSL and CBL are effective in reducing power supply noise over conventional CMOS for large circuits. However, these techniques have the downside of increased power consumption.

Another technique to maintain a constant supply current is the reduced supply bounce (RSB) technique proposed in [40]. In RSB CMOS, pairs of small decoupling capacitors and series resistors formed by a MOSFET biased in the linear region are provided locally for each V_{DD} and ground path in the digital system as shown in Figure 8-3.

The decoupling capacitors serve as local charge reservoirs for the fast logic tran-

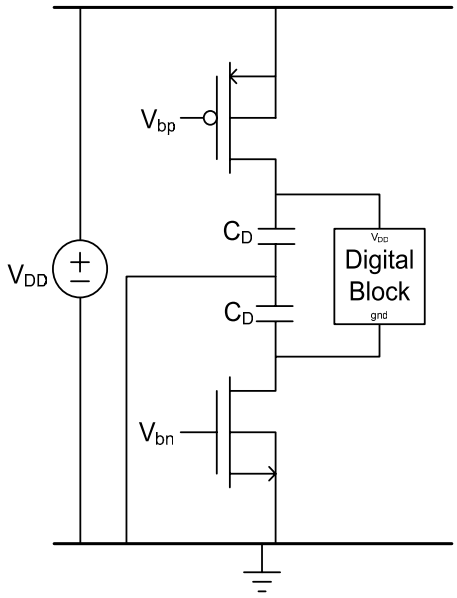


Figure 8-3: RSB-CMOS circuit configuration [40].

sitions and are recharged continuously by an external supply. Because the supply bounce is reduced and decoupled locally, the supply current profile remains approximately constant. In [40], it was shown that the noise generated can be reduced by as much as 67%.

Another technique to mitigate substrate noise coupling is to employ active substrate noise cancelation. The principle behind this technique is to cancel the substrate noise by injecting "antinoise" back into the substrate. Most techniques involve sampling the substrate noise signal and then directing this noise into a negative feedback loop. After the phase has been reversed, the created "antinoise" is injected back into the substrate. These techniques have demonstrated almost 16 dB of attenuation at low frequencies [36]. The main limitations are that it is only suitable for low frequencies (below a few MHz) set by the bandwidth of the amplifier and that high-power amplifiers are required to drive the "antinoise" signal back into the substrate.

An alternative implementation is to use a discrete time feedback loop using digital inverters to shape the substrate noise selectively [44]. The shaping in this implementation can be designed to be effective at any frequency; however, the band from 0-20 kHz was targeted.

A switched-capacitor loop filter is used to sample the substrate noise with one differential input connected to the substrate and the other connected to an off-chip reference. A Flash A-D converter converts the output of the filter into a thermometer code output that is used to drive an array of inverters. These inverters are used to generate the "antinoise". The output of the array is capacitively coupled to the substrate creating the "antinoise" in the substrate.

There are two main limitations to this technique. The work in [44] was implemented on an epi substrate; thus, a single substrate node could be assumed. To implement the substrate noise shaping on a non-epi substrate would require a more complicated feedback loop because of the two-dimensional nature of the substrate. Moreover, this technique relies on the ability of the array of inverters to generate the "antinoise" correctly. When the shaping loop was used to cancel the noise generated by an array of inverters, almost 10 dB of attenuation was reported in the band from 0-20 kHz [43]. However, when the technique was applied to a Digital Encryption Engine, a digital circuit that will generate a more random noise pattern, the shaping loop actually degraded the substrate noise performance by injecting more noise back into the substrate.

8.3 Isolation Structure Guidelines

The effectiveness of the various noise isolation techniques discussed in Section 3.5 of Chapter 3 depends on the type of substrate used. For this reason, this section is divided into two subsections depending on the substrate type.

In general, it is necessary to use separate supplies for the digital and analog subsystems. The digital supply can be extremely noisy and thus should not be shared by the sensitive analog subsystem. The use of separate supplies comes at the expense of extra package pins.

8.3.1 Epitaxial Wafers

Distance

Physical separation is a simple technique to lower noise coupling. However, on conventional CMOS epi substrates, the isolation achievable with physical separation reaches a maximum value and saturates. Su et al. found that for separation distances above four times the thickness of the epi layer, additional isolation was not achieved [55]. This implies that the bulk acted as a single resistive node. Thus, any noise injected in the substrate would appear at every other bulk node with no attenuation.

Substrate Contacts

In general, the bias for the substrate should be connected to a quiet ground. If the substrate is connected to the digital ground, the single node nature of the epi substrate results in the digital supply noise appearing across the entire chip. If a quiet ground is used, the power supply current spikes do not get absorbed into the substrate. If a dedicated supply cannot be provided, the substrate should be connected to the analog supply. Because of the low resistivity bulk, the backside connection is very important. A good backside contact with little inductance will result in better noise performance.

Guard Rings

Guard rings consist of heavily doped p+ regions that surround a noisy or sensitive portion of the circuit. They work by providing a low impedance path to ground. Ultimately, their effectiveness is limited by bondwire and package parasitics used to bias the guard ring.

In [55], it was shown that guard rings are ineffective in epi substrates. Depending on the guard ring connection, guard rings can even result in even worse noise performance. If the guard ring is connected to its own quiet ground, the guard ring only attenuates the noise by 20% (approximately 2 dB). However, if the guard ring is connected to all other substrate contacts, an increase in noise is observed. This

occurs because the guard ring is providing another low resistance contact into the substrate. Since it is connected to a noisy ground, it is essentially coupling noise back into the substrate.

8.3.2 Non-Epitaxial Wafer

Distance

In non-epi wafers, the bulk does not act as a single node. Thus, increasing separation distance does result in more isolation. However, the increase in isolation is not significant. Increasing the separation distance by a factor of four from 50 μm to 200 μm resulted in only 8 dB additional attenuation as shown in Figure 3-11.

Substrate Contacts

For non-epi wafers, ideally more than one ground should be used to bias the substrate. At the digital subsystem, the substrate should be connected to the digital ground. Any substrate current will then be sinked to the digital ground as it is the lowest impedance path. At the analog subsystem, the substrate should be connected to the quiet analog ground. The high-resistivity of the bulk provides adequate isolation between the different power supply domains.

As with epi wafers, reduced inductance in the supply lines will reduce the noise injected. The inductance can be reduced by using multiple pins or by using a package with lower inductance leads.

The backside contact is not as important in non-epi wafers as the substrate is of higher resistivity and because most of the noise of the noise current will propagate closer to the surface.

Single Guard Ring

In contrast with epi substrates, guard rings are effective in mitigating substrate noise as discussed in Section 3.5 of Chapter 3. A single guard ring can provide between 20 dB and 30 dB of isolation at 1 GHz depending on the guard ring geometry. Figure 8-4

shows the amount of isolation afforded by guard rings of different widths. At lower frequencies, the widest guard ring provides more isolation. In general, the guard ring should be made as wide as possible so that the impedance to ground is minimized.

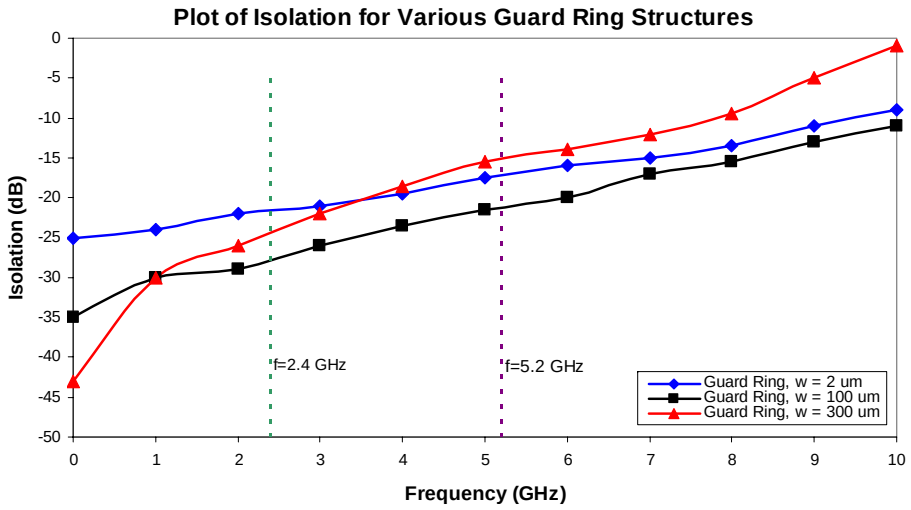


Figure 8-4: Isolation for different guard ring widths. Data from [16].

Double Guard Rings

Double guard rings consist of two p+ guard rings: one surrounding the sensitive portion of the circuit and the other surrounding the noisy portion as shown in Figure 8-5. Over a wide frequency range, the use of double guard rings provide approximately 5 dB of additional isolation over a single guard ring. The isolation performance of a guard ring is largely set by the impedance between the structure and the ground connection. The lower the impedance, the better the isolation. The double guard ring yields improved isolation because the addition of the second guard ring lowers the impedance to ground. A single guard ring can be modeled with a series resistance and inductance. The double guard ring consists of two branches of the series resistance and inductance in parallel as shown in Figure 8-6. As a result, the effective impedance from the substrate to the guard ring ground is halved resulting in the improved isolation.

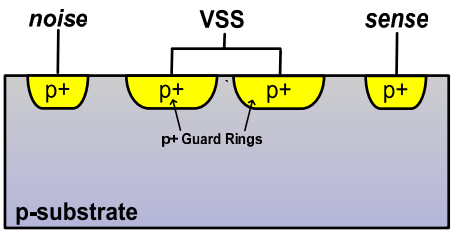


Figure 8-5: Cross-section of double guard ring isolation.

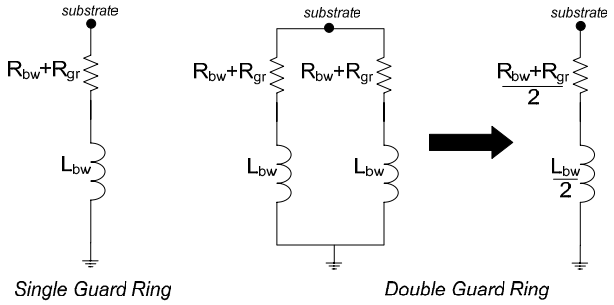


Figure 8-6: Models for a single guard ring and for double guard ring isolation.

Dual Guard Rings

Dual guard rings consist of p+ and n-well annular regions as shown in Figure 8-7. [55] and [30] found that dual guard rings only provide marginal improvement in isolation and often no effect on isolation. The n-well guard ring can have an effect if most of the noise current flows in the p+ field implant region. In this case, the n-well breaks the connection in p+ implant layer forcing the current to flow into the more resistive substrate.

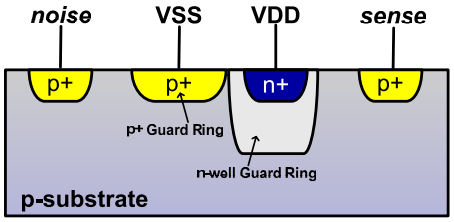


Figure 8-7: Cross-section of dual guard ring isolation.

Deep N-Well

[24] reported that the use of deep n-well technology provides approximately 50 dB of isolation over a wide range of frequencies (2.4 GHz to 24 GHz). A cross-section of deep n-well isolation is shown in Figure 8-8. The deep n-well traps the substrate noise created by the digital system preventing it from propagating to the analog subsystem.

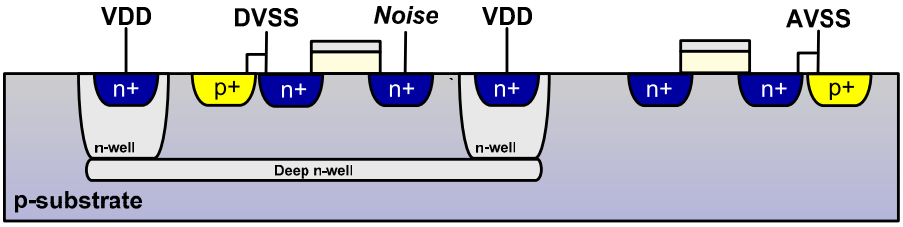


Figure 8-8: Cross-section of deep n-well isolation.

Triple Wells

A cross-section of a triple well technology is shown in Figure 8-9. Triple wells provide isolation through well shielding [51]. NMOS substrate contacts no longer contact the substrate itself; thus, ground noise does not directly appear on the substrate. Instead, any power supply noise is filtered through the well RC network. The use of triple wells provides approximately 25 dB of isolation at 2.4 GHz [50].

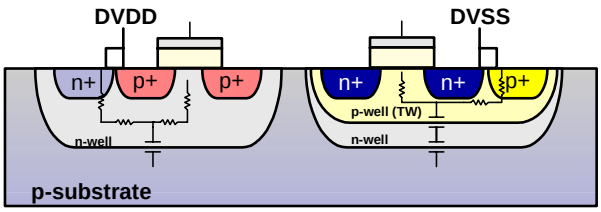


Figure 8-9: Cross-section of triple well isolation.

Faraday Cage

The technology that yields the most noise isolation is the on-chip Faraday cage [59]. The concept behind the Faraday cage is shown in Figure 8-10.

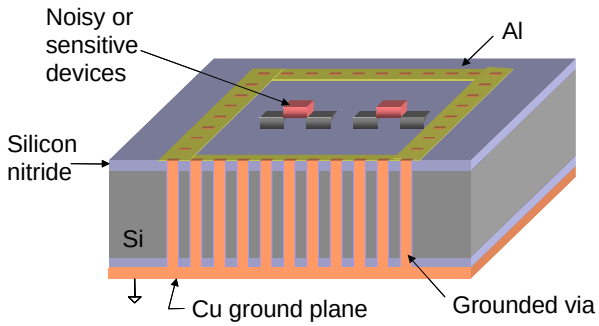


Figure 8-10: On-chip Faraday cage. Figure courtesy of J. Wu.

Grounded through-wafer vias surrounding the noisy or sensitive portions of a circuit sink any substrate noise current to a low impedance ground. Because the vias extend through the entire depth of the substrate, the vias are very effective in sinking noise. In [59], almost 75 dB of attenuation at 2.4 GHz was reported. The main limitation of this technology is in the fabrication of the vias themselves. Even with state of the art aspect ratios, extremely wide vias would be required in order to have the vias extend all the way through the substrate. The use of thinned wafers can help to alleviate this problem.

8.4 Noise-Resistant Analog Circuits

The most common technique to reduce the reception of substrate noise in analog subsystems is to use differential circuits. In this technique, noise appears as a common mode signal at the differential output and thus sees a large amount of attenuation set by the common mode rejection ratio (CMRR). The effectiveness of this technique depends on matching between the differential branches and also on the noise itself. If the same noise couples into both branches, then the noise rejection is high. However, due to the large size of the devices in analog circuits, the noise coupled into each branch will often not be identical. Differential circuits typically provide roughly 20 dB of attenuation [24].

8.5 Summary

In this chapter, guidelines were presented to assist the designer in mitigating the effect of substrate noise. A survey of low noise architectures were presented to reduce the injected noise. Technology and active circuit techniques were presented that lessen the effect of substrate noise. In addition, layout techniques that can be employed to diminish substrate noise were discussed. Finally, circuit architectures that are resistant to the effect of substrate noise were presented.

Chapter 9

Conclusion

9.1 Summary of Research Results

In this dissertation, all aspects of substrate noise were analyzed. The main contributions of this thesis are three-fold. First, the mechanisms behind substrate noise were analyzed thoroughly to develop a set of guidelines that designers can use to try and minimize the effect of substrate noise on their designs. These guidelines serve to try and demystify the subject of substrate noise. There has been much work in analyzing different isolation structures; however, conclusions on the effectiveness of one technique over another could not be determined as the structures used in the evaluations varied from experiment to experiment. Furthermore, the guidelines developed here present a survey of all the isolation techniques available, and how each should be used to yield the best isolation. Hopefully with these guidelines, ad hoc methods to design for substrate noise will give way to careful, methodical techniques that ultimately result in improved noise performance.

The second main contribution of this work was in the analysis of the effect of substrate noise on the performance of a VCO. Very little work has been done in the area of the effect of substrate noise on high frequency analog circuits. This is largely because RF circuits operated out of band of the majority of substrate noise. However, as operating clock frequencies increase, significant levels of substrate noise appear in the RF band. In fact, appreciable substrate noise tones of 10 GHz appear for 2 GHz

clocks, and tones at 2 GHz appear for clocks well below 400 MHz [21]. The effect of different VCO parameters such as center frequency, bias current, and isolation were evaluated.

It was found that there are two main coupling paths into the VCO. The first is through substrate contacts. The second is coupling through the inductor to substrate capacitance. For higher center frequency VCOs, the component from the inductor to substrate capacitance is reduced as the inductor size is smaller resulting in a reduced capacitance to substrate.

Furthermore, the VCO bias current plays an important role in the coupling of substrate noise into the VCO. When operating in the current-limited regime, increased bias currents improve the noise performance. However, once the VCO reaches the voltage-limited regime, further increases in bias current degrade the signal to noise ratio as the noise amplitude increases while the signal amplitude remains constant.

This dissertation has shown that the phase noise of a VCO is adversely affected by substrate noise. In the extreme, the VCO can lock to the substrate noise. VCO locking is a well known phenomenon. What is interesting about the locking observed in this work is that even for low substrate noise amplitudes, VCO locking is observed due to the resonant gain behavior of the VCO. As the noise frequency approaches that of the carrier, the noise sees an increased gain due to the resonance of the LC tank. This amplifies the noise with respect to the carrier. Even though the substrate noise level is 30 dB below the carrier, the amplified noise is comparable to that of the carrier power. Thus, the VCO can lock to the noise instead of the resonant frequency of the tank.

Moreover, it was found that guard rings are effective in reducing the noise that couples into the VCO. As expected, the effect of the guard ring degrades at higher frequencies. Guard rings were found to also be effective in reducing the VCO locking range.

The final and most significant contribution of this thesis was in the development of a substrate noise CAD tool (SNAT) that can be used at any point in the design cycle to predict the substrate noise profile of any large digital system. Very accu-

rate techniques to simulate for substrate noise result in prohibitively long run times. Techniques using noise macromodels sacrifice some accuracy; however, the speedup in simulation time is tremendous. The main drawback of existing approaches is that they can only be used for final verification. A complete SPICE level netlist and a full layout with substrate doping profiles is required to generate an estimate. While final verification is important, it makes any re-design cumbersome.

While the speedup over a full transistor level simulation is significant, the run times are still very long for use early in the design cycle. For example, if only a rough estimate is required, a simulation time of multiple days is excessively long. SNAT's flexibility with respect to the input description allows it to be used as both a final verification tool and also as a rough estimation tool.

An order of magnitude estimate can be generated on the order of a minute while an extremely accurate answer can be generated in three days. Because SNAT is computationally efficient, it can be used as a prototyping tool to evaluate the noise performance of different circuit architectures even without a layout. The noise isolation plug-in of SNAT can be used to evaluate the effect of different isolation techniques on the substrate noise performance of a system.

9.2 Future Directions

More work needs to be done in the area of isolation structure modeling. Test structures varying different geometrical parameters should be designed and measured so that accurate models can be developed to generalize the dependence of the isolation on these values. In doing so, the isolation structure plug-in can be used to determine the appropriate isolation structure in order to meet a specified noise target. This would greatly enhance the power of SNAT.

The results of this dissertation show that substrate noise is a problem that is only going to worsen with new applications. New isolation structures that can provide better isolation are required. In addition, more research needs to be done in creating low noise circuit architectures or in noise robust analog circuits. This dissertation

has explored the potential of advanced technologies such as the Faraday cage and 3-D integration for substrate noise mitigation.

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