CONSOLIDATION CIRCUIT FOR AN MHD CHANNEL

by

Rowley Lop-Wah Cheng

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ABSTRACT

As a result of the Hall field, electrodes of an MHD channel are at different electric potentials. In order to reduce the number of load circuits, electrical consolidation can be used to bring power extracted from these electrodes to a common potential.

The subject of this thesis is related to the analytical and experimental investigation of a scheme for consolidation first suggested at the AVCO Everett Research Laboratory. Analytic models were developed to investigate the steady state and transient behavior and also determine the parameters affecting the performance of the circuit. A version of the circuit to consolidate four electrode pairs was constructed and tested first under laboratory simulated channel conditions and afterwards on the AVCO Mark VII and the results are reported here. Lastly, an outline of a procedure for the design of this type of consolidation circuit is suggested.

Thesis Supervisor: John G. Kassakian
Assistant Professor of Electrical Engineering

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Chapter 1 Introduction and Background

To date, and probably for quite some time to come, the generation of large-scale electrical energy from thermal energy has required an intermediate step involving mechanical energy. The thermal energy from the primary source (e.g. coal, natural gas, or nuclear) is used to generate steam or high temperature gas which is then fed into a turbine coupled to an electrical generator. The turbine-generator set is then the mechanical link.

In its most simple form the mechanical energy in the form of shaft power is used to move some metal conductors (e.g. copper) through a stationary magnetic field. The relative motion of the magnetic field and the electrical conductor induces an electromotive force within the conductor given by Faraday's Law of Induction,

$$\mathcal{E}.m.f. = K\frac{d\phi}{dt}$$

where ϕ is the magnetic flux enclosed by the conductor and K is a proportionality constant. The electromotive force can then drive a current in the conductor given by Ohm's Law, and can be drawn off from the generator as either direct or alternating current.

The challenge to improve the thermodynamic efficiencies of thermal cycles and reduce mechanical losses in electricity generating processes has resulted in the exploration of a number of conversion processes. Among these is a group known as "direct conversion" processes where the intermediate mechanical link is eliminated (reference 1 and 2).

MHD power generation is a direct conversion process based on magneto-hydrodynamic principles.

The basic physics behind MHD power generation is simple and not different from the principle of the conventional turbogenerator. A stream of high temperature gas, made conducting by a process known as "seeding", flows through an orthogonal magnetic field. According to Faraday's Law, an electric field is induced in the gas just as it is in the armature coils of a conventional direct current generator. In an MHD machine, however, the current can be "collected" by electrodes instead of brushes. These processes take place in an MHD "channel" which is also called an MHD generator, schematically shown in Figure 1.1.

Here, positive ions travelling with the gas velocity $\bar{u}$ will feel the Lorentz force as given by

$$\bar{f} = \rho \bar{u} \times \bar{B}$$

which, with the directions shown in Figure 1.1, will propel them towards the top wall or cathode of the channel. Likewise, negatively charged particles (electrons, ions, etc.) are driven to the bottom wall or anode. When a load is connected between the anode and cathode, current will flow from cathode to anode through the load and power extracted. The flow of this current having a density $\bar{J}$ (amp/m^2) is controlled by Ohm's Law as:

$$\bar{J} = \sigma (\bar{u} \times \bar{B} + \bar{E}_L)$$

where σ is the electrical conductivity of the seeded gas (mho/meter) and $\bar{E}_L$ is the electric field (created by charge separation) opposing the direction

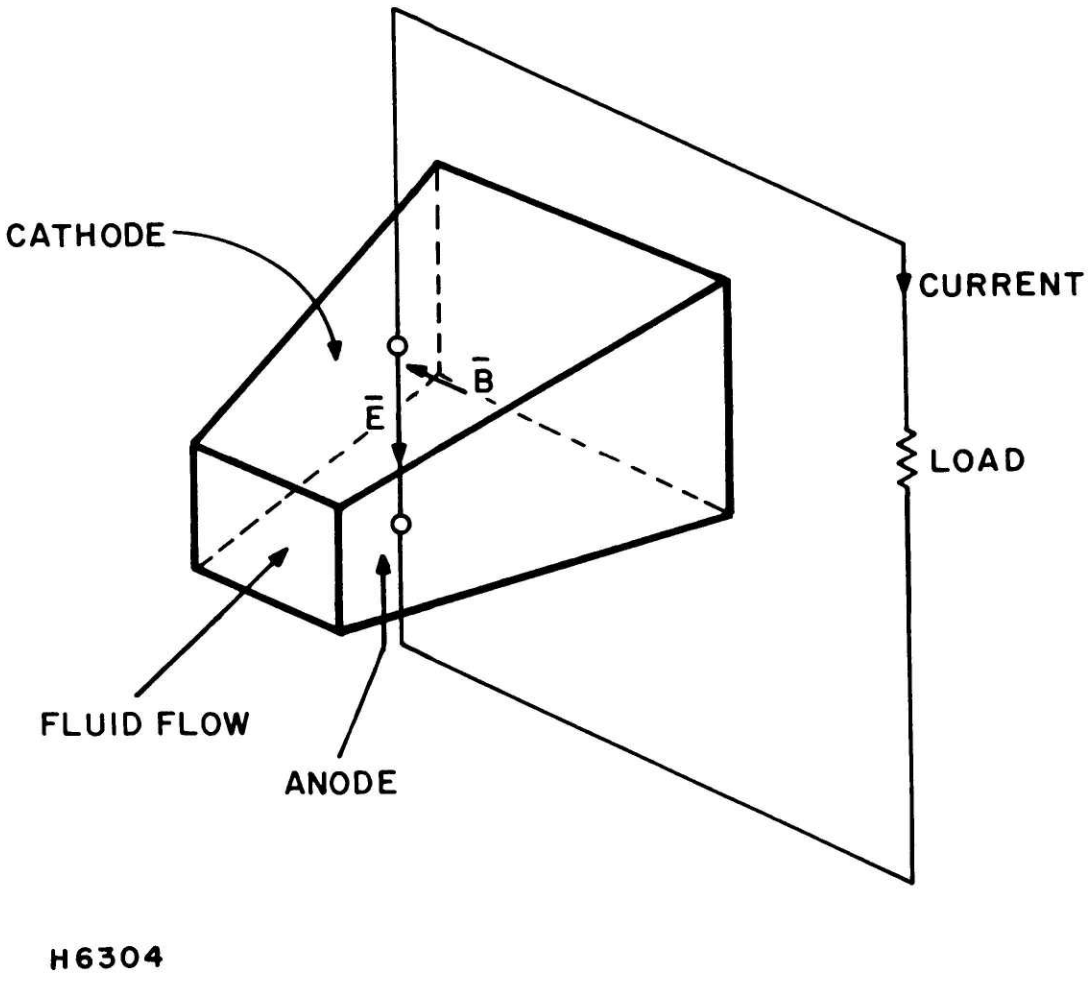


Figure 1.1 A Basic MHD Channel

of the induced ($\bar{u} \times \bar{B}$) field. This current interacts in turn with the magnetic field giving rise to an interaction force ($\bar{J} \times \bar{B}$ force) which give rise to an axial (Hall) field $\bar{E}_H$ as:

$$\bar{F} = \bar{J} \times \bar{B}$$

$$\bar{E}_H = \frac{\bar{F}}{q} .$$

These relationships are shown in Figure 1.2. The Hall field would circulate an axial current if the electrodes were continuous pieces of conductor, short circuiting the channel from end to end and dissipating electric power in the channel. To avoid this, electrodes are segmented in small sections with insulators in between providing the Hall field stand off. Through segmentation, output power can be boosted by an order of magnitude. (For a more detail treatment of MHD power generation and also a discussion of Hall field, see reference 3. Reference 4 is for those who want a less rigorous approach.)

There are several ways to extract power from these many electrodes (see Figure 1.3). The finer the electrodes are segmented, the higher the apparent conductivity of the gas and hence the higher the efficiency of the thermal cycle. As a result, in a large channel, there could be as many as a thousand electrode pairs. In a Faraday generator, each electrode pair (comprising of an anode and the cathode right opposite it) has its own load. In a Hall generator, opposite electrode are shorted and power is extracted at the ends of the channel. In a diagonal channel, electrodes lying on the same equipotential surface are connected together

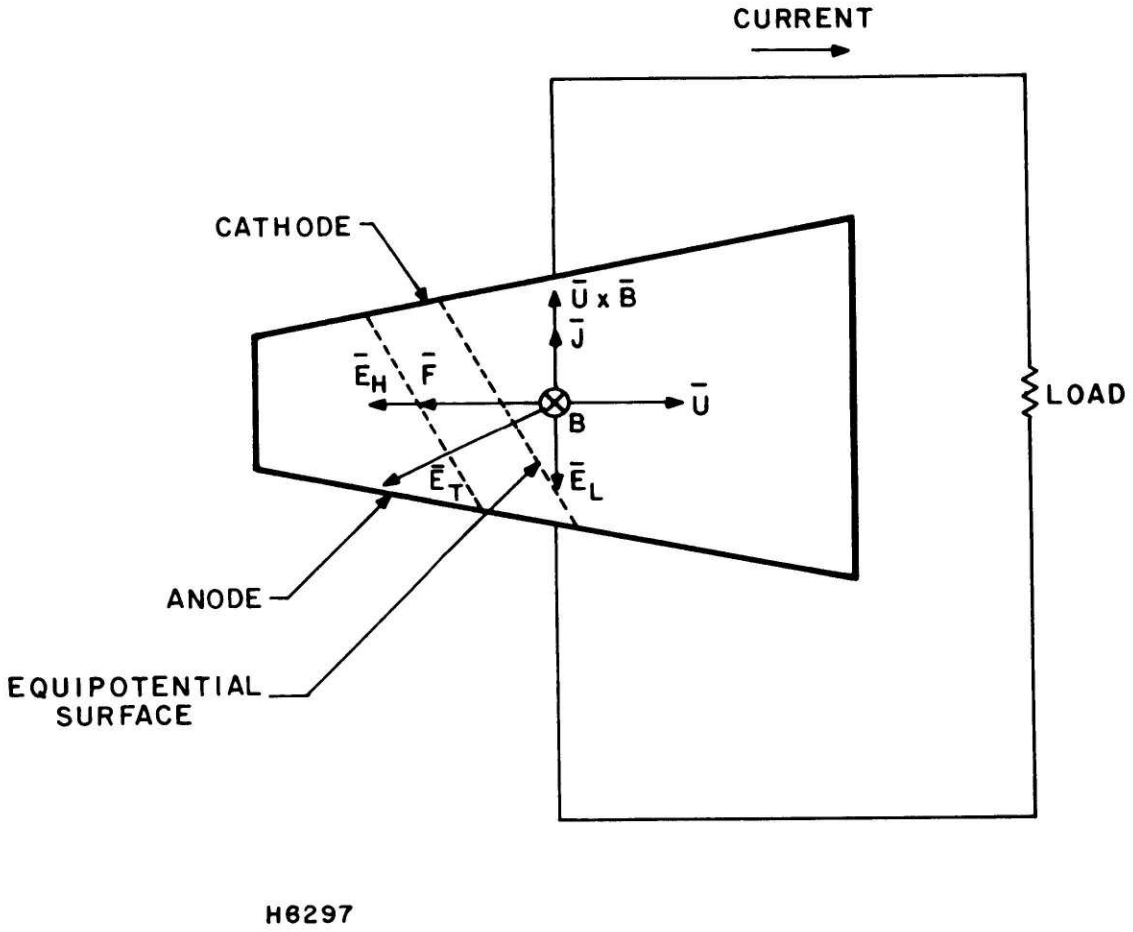


Figure 1.2 Fields Inside an MHD Channel

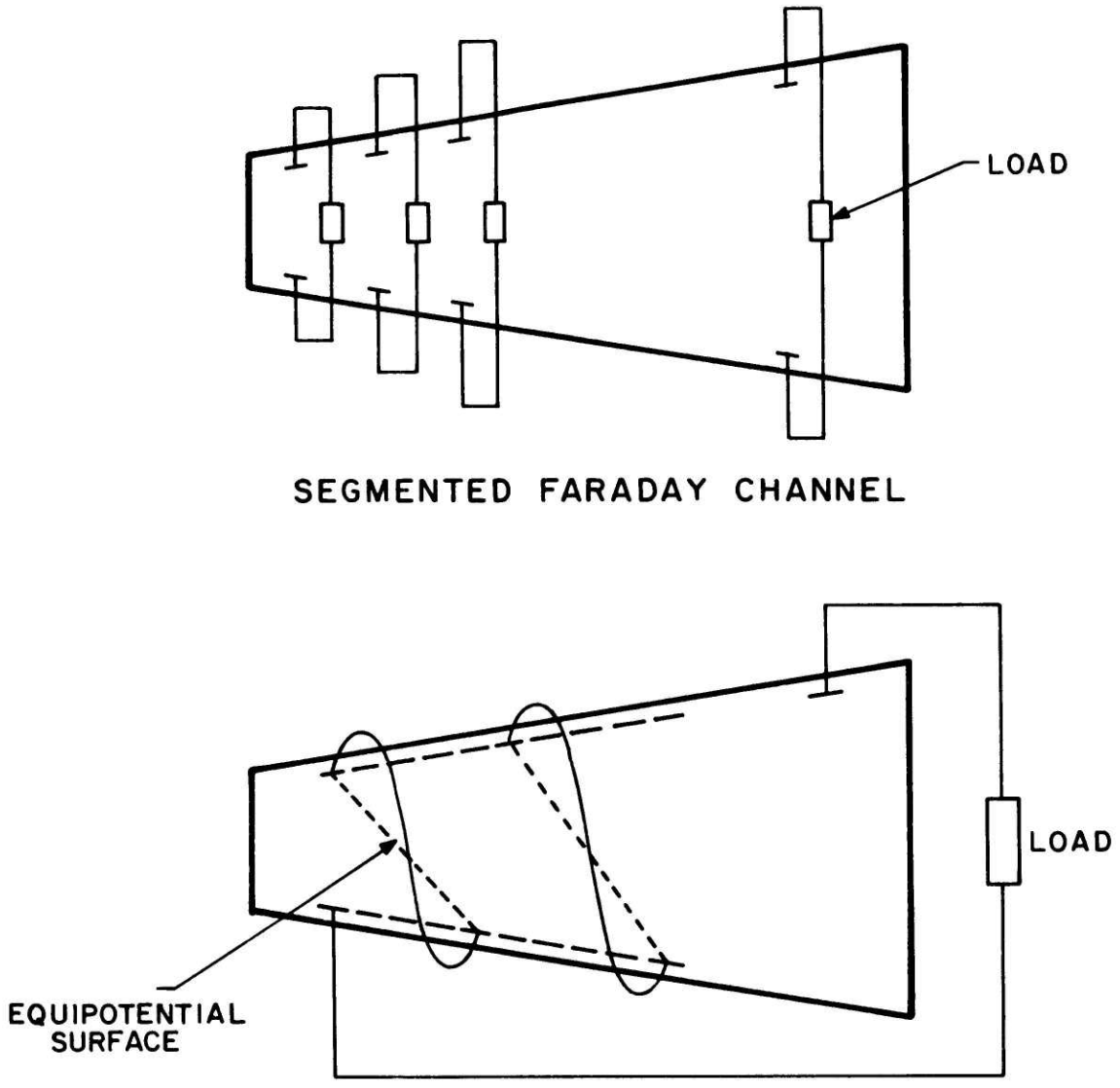
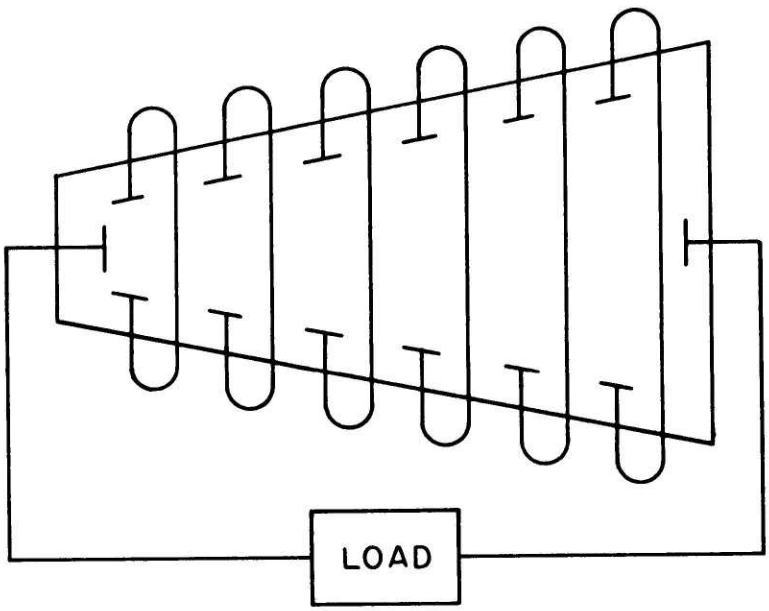


Figure 1.3 Different MHD Channel Connections



A LINEAR HALL GENERATOR

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Figure 1.3 Different MHD Channel Connections (Continued)

and power again extracted at the ends. (For detail, see Chapter 4 in reference 3.) For the purpose of ac power generation and transmission, the "loads" in Figure 1.3 are typically inverters that convert dc power generated by the MHD generator to ac power and feed it into the power line. From the point of view of economy, small number of large inverters is preferred to large number of small inverters. (Large inverters are inverters that can handle high power level.) So if there is a way to bring the output of the electrodes to one or a few common points without disturbing the field pattern inside the channel, the number of loads (inverters) can be reduced. This reduction is most significant in the case of a Faraday channel if each electrode pair is to have its own inverter. Current consolidation is a general idea that may accomplish this goal. However, before going into the philosophy, another factor has to be mentioned that moltivates an interest in the idea of a consolidation circuit.

Experience on the AVCO Mark VI at current densities and electric fields approaching baseload values has demonstrated that large current and voltage non-uniformities establish themselves on a time scale of an hour, and persist for long duration operation. Since these non-uniformities present high local electrical stress on the electrode and insulators of the channel, it is desirable to control them whenever practical. (Electrodes worn off due to high concentration of current on small areas of the electrodes in addition to the high temperature inside the channel is a major challenge to overcome in large scale development of MHD power generation.)

Consolidation circuits are intended to achieve the two afore mentioned goals. Since all the electrodes along a channel are at different electrical potentials, the basic philosophy behind consolidation circuits is to systematically bring the outputs of a group of electrodes to a common potential and feed it into a single inverter. Consolidation circuits can be either active or passive, dissipative or non-dissipative. However, from a practical point of view, several criteria can be established as a guideline for designing a consolidation circuit.

1. The circuit should be passive and non-dissipative. A consolidation circuit can be readily realized by a series connection of resistors as shown in Figure 1.4. However, dissipative loss can cost us more than the money saved in developing consolidation circuits.

2. The circuit should not short the Hall field in the channel which would result in reversing the segmentation.

3. The circuit should not induce arcing along the channel wall. Arcing can damage the electrodes as well as effectively shorting the Hall field.

4. The circuit should be able to maintain specific control over currents in the individual electrodes.

5. The circuit should not cost more than the dollar amount it is supposed to save by allowing use of small number of high power inverters. This criterion can be relaxed if the consolidation circuit can be shown to have a positive impact on the electrical performance (i.e. current uniformity).

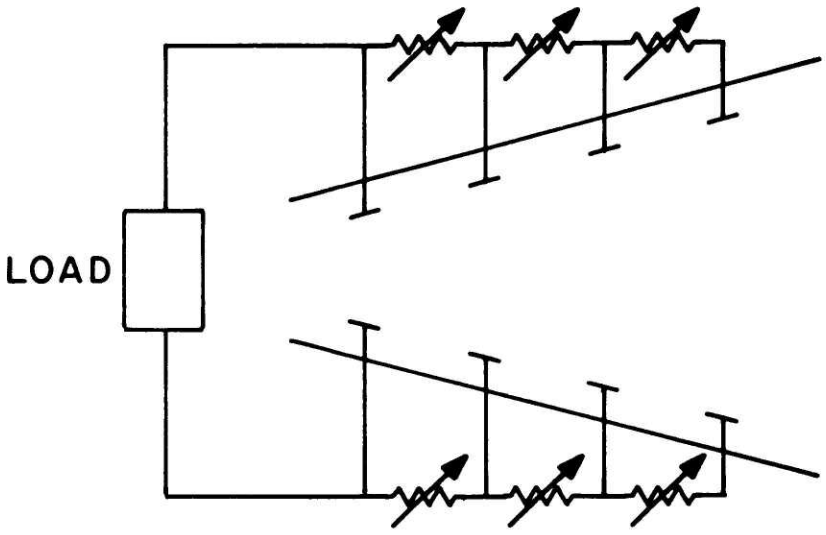


Figure 1.4 Resistive Consolidation Circuit

Chapter 2 The Circuit

Several schemes for consolidation have been proposed at AVCO. The basic idea is to start with a "one-stage" circuit that consolidates two electrodes by bringing up the potential of an upstream electrode and bringing down the potential of a downstream electrode to the same potential at a common point. The single output from these two electrodes can then be in turn consolidated with the output of neighboring electrode pairs and so on.

One of these schemes, shown as circuit I in Figure 2.1, was first proposed by Rosa (see reference 5). It utilizes the mutual coupling between two windings of an autotransformer to maintain a constant ratio between the two electrode currents. By changing the turns-ratio of the autotransformer, the ratio of the electrode currents is adjusted. To prevent saturation of the autotransformer, this scheme must continuously switch the electrode currents between two separate autotransformers. At present, this scheme is being tested on the AVCO Mark VII generator.

The second circuit shown in Figure 2.1 was proposed by Lowenstein (see reference 6) and is the theme of this thesis. A detailed analysis of the circuit can be found in Chapter 3. Here, a brief description of its operating principle is given.

Referring to Figure 2.1 (b), the two SCRs are driven with the same frequency but 180 degrees out of phase. The biasing for the SCRs comes from the capacitor C. A positive capacitor voltage v_c will forward bias SCR2 and reverse bias SCR1, whereas a negative v_c will forward

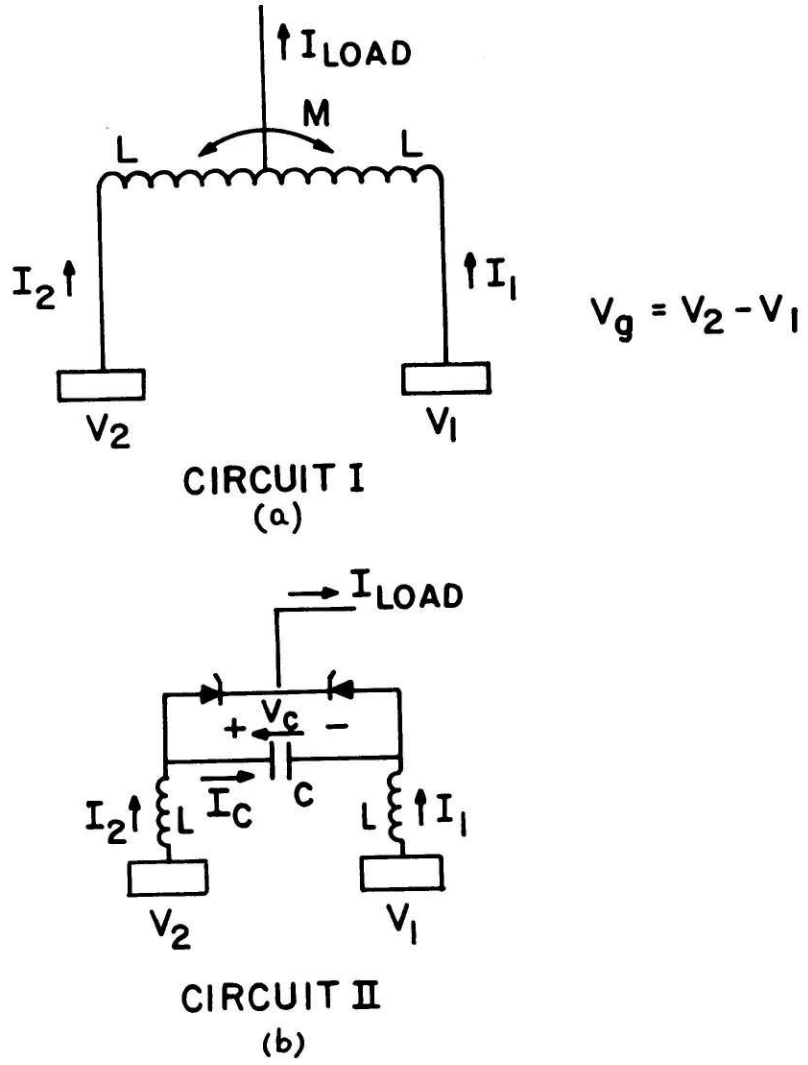


Figure 2.1 Two Different Consolidation Schemes
Circuit I
Circuit II

bias SCR1 and reverse bias SCR2. This way, no more than one SCR can be conducting at any given time.

In the steady state, just before SCR2 turns on, the capacitor voltage v_c will be maximum. Since SCR2 is on and SCR1 is off, current from terminal 2 (I_2) flows directly into SCR2 and current from terminal 1 (I_1) flows into SCR2 through the capacitor, discharging it and eventually charging it to a negative voltage. At this instant, SCR1 receives a gate pulse and starts conducting and simultaneously SCR2 is turned off. I_1 and I_2 now reverse roles. I_2 will be charging the capacitor positive until SCR2 receives it gate signal and the cycle is repeated.

The time average voltage of the capacitor over one cycle is equal to the gap voltage $V_g = V_2 - V_1$. The capacitor is thus providing the voltage isolation between the two electrodes. Potential stepping up and stepping down is realized by having fluctuating currents in the inductors. Voltage V_L across an inductor L is given by $L \frac{di}{dt}$, hence a positive $\frac{di}{dt}$ corresponds to stepping up and a negative $\frac{di}{dt}$ corresponds to stepping down. It can also be seen that the electrode current fluctuation $\frac{di}{dt}$ can be reduced by having a larger inductance L (and keeping V_L the same). Moreover, for

$$V_L = L \frac{di}{dt} \simeq L \frac{\Delta i}{\Delta t} = \text{constant}$$

$$\Delta i = \text{constant} \times \Delta t$$

a smaller Δt will result in a smaller current fluctuation Δi. Since a smaller Δt comes from higher SCR commutating frequency f, current

fluctuation is a decreasing function of frequency f.

The effect of the value of capacitance C is seen very clearly for period $\tau = 1/f$ smaller than $\sqrt{LC}$. The consolidation circuit can be looked upon as an LC circuit driven by a source V_g, the interelectrode gap voltage. In this case, at a fixed point in time equal to the period τ, the current will have changed less for larger value of $\sqrt{LC}$. Hence increase L or C can reduce currents fluctuation for the same commutating frequency.

Finally, current non-uniformity can also be controlled. In the steady state and assuming a lossless situation, the electric charge deposited in the capacitor by current 1 when SCR2 is conducting is equal to the negative of the electric charge deposited by current 2 when SCR1 is conducting. So if we define τ_1 to be the total time SCR1 conducts in one cycle, and τ_2 the total time SCR2 conducts in one cycle, we have the following relationship

$$\tau_1 I_2 = \tau_2 I_1$$

$$\text{or} \qquad \frac{I_1}{I_2} = \frac{\tau_1}{\tau_2}$$

where I_1 is the average current in electrode 1 and I_2 is the average current in electrode 2. Thus by varying τ_1 relative to τ_2, the relative current in the two electrodes can be adjusted.

The circuit shown in Figure 2. 1 (b) will consolidate two cathodes (current flows from cathode to anode through the load). The same circuit with the SCRs reversed will consolidate two anodes. A consolidation circuit that will consolidate three electrodes could be just a simple extension of the two electrodes circuit, as shown in Figure 2. 2. This

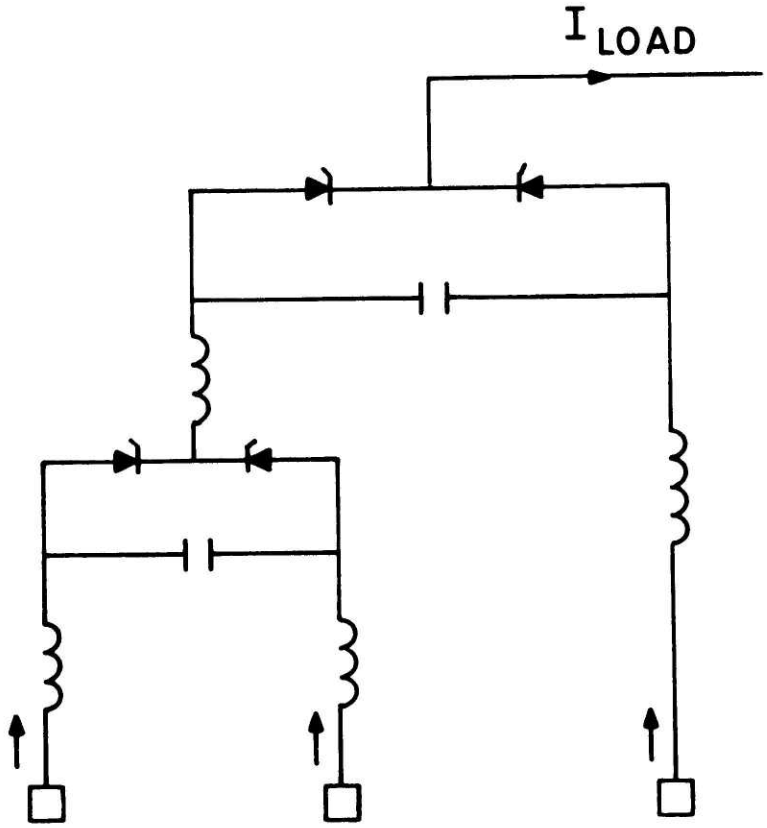


Figure 2.2 Consolidation Circuit for Three Electrodes

scheme has not been analyzed and tested, but if it works, with the two-electrode circuit and three-electrode circuit as building blocks, any number of electrodes can be consolidated.

Chapter 3 Analysis, Modelling, and Simulation

As a first step towards the achievement of consolidation by the circuit described in the previous chapter, an analysis was done to study the parameters that influence the performance of such a circuit.

Eventually, many of these one stage two electrodes consolidation circuits may be cascaded together as in Figure 3.1 to consolidate many electrodes. However, it is very tedious and unnecessarily complicated to analyze such a multi-electrode circuit. Since all the stages have basically identical configurations (although upper consolidation stages have larger components to handle higher currents and voltages), we can analyze a simple one-stage two electrodes circuit, and use the insight generated to understand the multi-stage circuit. Moreover, the circuit on the top and on the bottom of the channel are basically identical except with the SCRs reversed. So only half of the complete circuit (either the half on the cathode side or the half on the anode side) need to be analyzed.

A. Inductive Load

Consider a segmented channel as shown schematically in Figure 1.3. For a large channel, a potential drop of 1000 volts across the channel and a 20 volts difference between adjacent electrodes are typical. These voltages stay relatively constant under desirable operating conditions and so, as a first approximation, can be modelled as constant voltage sources. The load can be modelled as an inductor in series with a resistor. In the case of an inverter load, the inductance will be rather large. So,

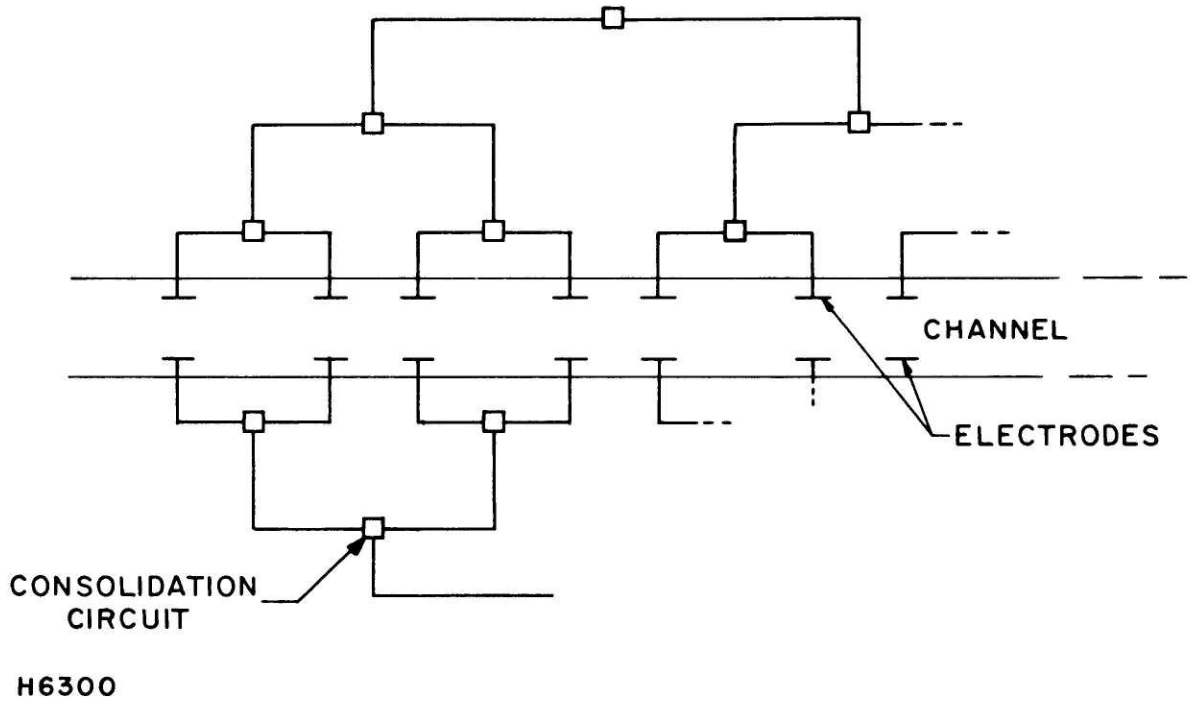


Figure 3.1 Multi-Stage Consolidation Circuit

in its simplest form, the channel- consolidation circuit-load system will be as shown in Figure 3.2a.

Two states of the circuit can be identified depending on whether SCR1 or SCR2 is conducting. The circuit is said to be in state 1 if SCR1 is conducting, and state 2 if SCR2 is conducting. In the analyses throughout this chapter the "method of assumed state" is used. That is, switching of the SCRs is always assumed even though the capacitor may not have the right polarity at the switching time. Also, to generalize the solution, all quantities will be non-dimensionalized by appropriate parameters.

State 1 (Figure 3.2b)

$$i_1 + i_2 = I$$

$$\ell \frac{dI}{dt} + IR - V + L \frac{di_1}{dt} = 0$$

$$-L \frac{di_1}{dt} + V_c + L \frac{di_2}{dt} - V_g = 0$$

$$i_2 = C \frac{dV_c}{dt}.$$

This is a set of four first order differential equations in the four unknowns i_1, i_2, I_1 and v_c. To solve it numerically, values for L, C, R, ℓ, V_g and V have to be specified and a general solution cannot be arrived at easily. On the other hand, this set of equations can be reduced to a single third order differential equation and be solved analytically using standard techniques. The results are complicated expressions in sines and cosines and exponentials. More insight can be gained, however, by solving these equations under two limiting regimes of operation of the circuit that is of most interest to us. These are the "constant current regime" and the

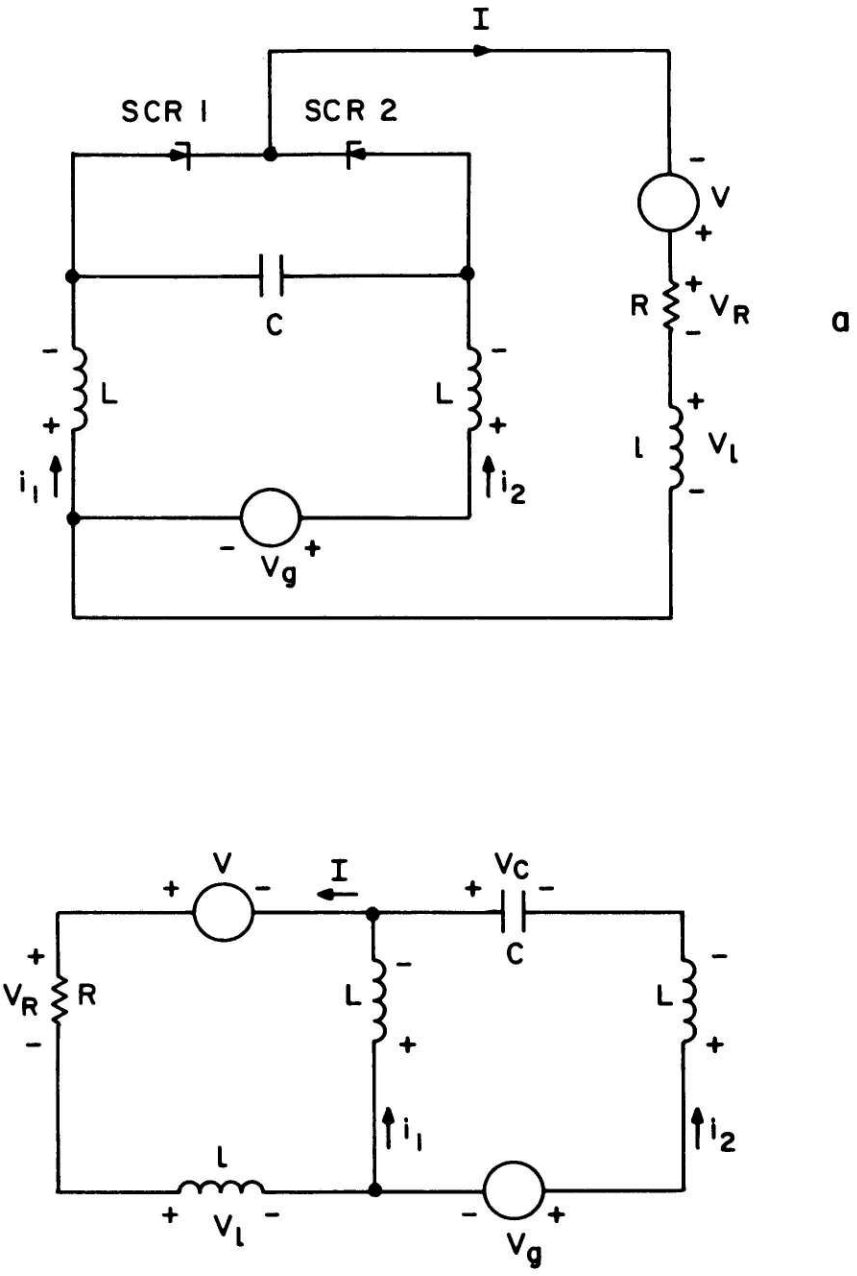


Figure 3.2 a. Simplified Channel - Consolidation Circuit - Load System

b. Same System in State 1

"resistive load regime". The constant current regime is important because in the case of inverter load, the load current approaches a constant value as the load inductance gets larger and larger. For other applications, the MHD generator may be used directly to power some machine the simplest of which can be idealized as a purely resistive load.

B. Constant Current Regime

In the constant current regime, the channel-consolidation circuit-load system is very simple as shown in Figure 3.3a.

State 1 (Figure 3.3b)

$$i_1 + i_2 = I$$

$$L\frac{di_1}{dt} + V_g - L\frac{di_2}{dt} + V_c = 0$$

$$i_2 = -C\frac{dV_c}{dt}.$$

Normalizing all currents by I, all voltages by V_g, and time by $\sqrt{2LC}$ and adding tildes to all normalized quantities results in the equations

$$\tilde{i}_1 + \tilde{i}_2 = 1$$

$$\Rightarrow \quad \frac{d\tilde{i}_1}{d\tilde{t}} + \frac{d\tilde{i}_2}{d\tilde{t}} = 0 \qquad (1)$$

$$\frac{I}{V_g}\sqrt{\frac{L}{2C}}\frac{d\tilde{i}_1}{d\tilde{t}} + 1 - \frac{I}{V_g}\sqrt{\frac{L}{2C}}\frac{d\tilde{i}_2}{d\tilde{t}} + \tilde{v}_c = 0 \qquad (2)$$

$$\tilde{i}_2 = -\frac{V_g}{I}\sqrt{\frac{C}{2L}}\frac{d\tilde{v}_c}{d\tilde{t}}. \qquad (3)$$

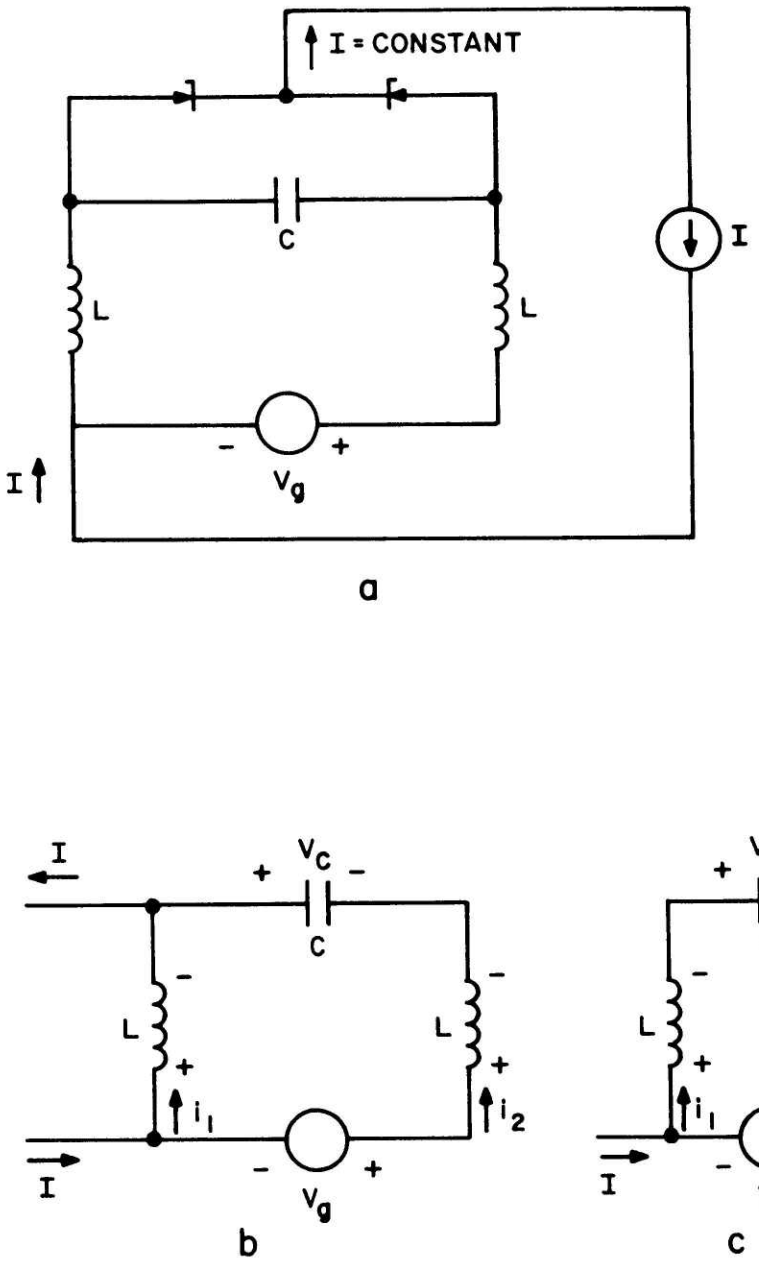


Figure 3.3 a. System in Constant Current Regime
b. Same System in State 1
c. Same System in State 2

Substitute equation (1) into (2), we have

$$-\frac{I}{V_g}\sqrt{\frac{2L}{C}}\frac{d\tilde{i}_2}{d\tilde{t}} + \tilde{v}_c + 1 = 0. \qquad (4)$$

Differentiate equation (4) with respect to $\tilde{t}$ and combine with equation (3), we have after simplifying,

$$\frac{d^2\tilde{i}_2}{d\tilde{t}^2} + \tilde{i}_2 = 0. \qquad (5)$$

Therefore, $$\tilde{i}_2 = K_1 \sin\tilde{t} + K_2 \cos\tilde{t} \qquad (6)$$

where K_1 and K_2 are constants. Define a non-dimensional parameter G,

$$G \equiv \frac{V_g}{I}\sqrt{\frac{C}{2L}}$$

and substitute into equation (4), we have

$$-\frac{1}{G}\frac{d\tilde{i}_2}{d\tilde{t}} + \tilde{v}_c + 1 = 0.$$

And from equation (6), we have

$$\tilde{v}_c = \frac{K_1}{G}\cos\tilde{t} - \frac{K_2}{G}\sin\tilde{t} - 1. \qquad (7)$$

To find out what K_1 and K_2 are, we have to define some initial conditions. We define time $\tilde{t}$ in such a way that $\tilde{t} = 0$ marks the beginning of state 1 and $\tilde{t} = T_1$ marks the end in each cycle. The initial conditions are:

$$\text{at} \quad \tilde{t} = 0, \quad \tilde{i}_1 = \tilde{i}_{11}$$
$$\tilde{i}_2 = \tilde{i}_{21} = 1 - \tilde{i}_{11}$$
$$\tilde{v}_c = \tilde{v}_{c1}.$$

(Notice that $\tilde{i}_{11}$, $\tilde{i}_{21}$ and $\tilde{V}_c$ are also non-dimensional.) Evaluate equation

(6) at $\tilde{t} = 0$ gives

$$K_2 = \tilde{i}_{21}.$$

Evaluate equation (7) at $\tilde{t} = 0$ gives

$$\frac{K_1}{G} - 1 = \tilde{v}_{c_1}$$

$$K_1 = G(\tilde{v}_{c_1} + 1).$$

Substituting K_1 and K_2 back into equations (6) and (7), we have

$$\tilde{i}_2 = G(\tilde{v}_{c_1} + 1) \sin \tilde{t} + \tilde{i}_{21} \cos \tilde{t}$$

$$\text{or} \quad \tilde{i}_1 = 1 - G(\tilde{v}_{c_1} + 1) \sin \tilde{t} - (1 - \tilde{i}_{11}) \cos \tilde{t} \qquad (8)$$

(since $\tilde{i}_1 + \tilde{i}_2 = 1$) and

$$\tilde{v}_c = (\tilde{v}_{c_1} + 1) \cos \tilde{t} - \frac{1 - \tilde{i}_{11}}{G} \sin \tilde{t} - 1. \qquad (9)$$

State 2 (Figure 3.3c)

Again, Kirchhoff's voltage and current laws give

$$i_1 + i_2 = I$$

$$L\frac{di_1}{dt} + V_g - L\frac{di_2}{dt} + V_c = 0$$

$$i_1 = C\frac{dV_c}{dt}$$

This set of equations can be solved by following exactly the same procedure used in state 1 above. Similarly, define $\tilde{t}$ to be 0 at the beginning of state 2 and T_2 at the end of state 2. The initial conditions for state 2 are:

$$\text{at} \quad \tilde{t} = 0, \quad \tilde{i}_1 = \tilde{i}_{12}$$

$$\tilde{i}_2 = \tilde{i}_{22} = 1 - \tilde{i}_{12}$$

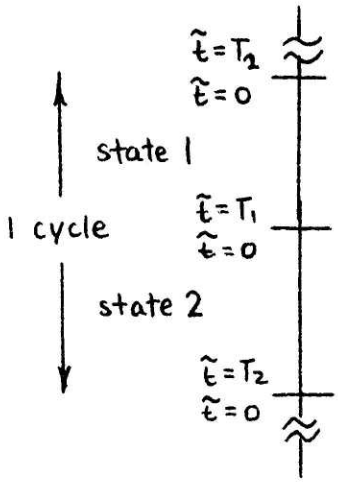
$$\tilde{v}_c = \tilde{v}_{c2}.$$

The solution is then given by

$$\tilde{i}_1 = -G(\tilde{v}_{c2} + 1) \sin \tilde{t} + \tilde{i}_{12} \cos \tilde{t} \qquad (10)$$

$$\tilde{v}_c = (\tilde{v}_{c2} + 1)\cos\tilde{t} + \frac{\tilde{i}_{12}}{G}\sin\tilde{t} - 1. \qquad (11)$$

Equations (8) to (11) then describe the circuit model as shown in Figure 3.3. They are repeated in the following chart.



$$\tilde{i}_1 = 1 - G(\tilde{v}_{c1} + 1)\sin\tilde{t} - (1 - \tilde{i}_{11})\cos\tilde{t} \qquad (8)$$

$$\tilde{v}_c = (\tilde{v}_{c1} + 1)\cos\tilde{t} - \frac{1 - \tilde{i}_{11}}{G}\sin\tilde{t} - 1 \qquad (9)$$

$$\tilde{i}_1 = -G(\tilde{v}_{c2} + 1)\sin\tilde{t} + \tilde{i}_{12}\cos\tilde{t} \qquad (10)$$

$$\tilde{v}_c = (\tilde{v}_{c2} + 1)\cos\tilde{t} + \frac{\tilde{i}_{12}}{G}\sin\tilde{t} - 1 \qquad (11)$$

In the steady state, all currents and voltages repeat themselves after one full cycle, that is

$$\tilde{i}_1\ (\tilde{t} = T_1,\ \text{state 1}) = \tilde{i}_1\ (\tilde{t} = 0,\ \text{state 2})$$
$$\tilde{v}_c\ (\tilde{t} = T_1,\ \text{state 1}) = \tilde{v}_c\ (\tilde{t} = 0,\ \text{state 2})$$
$$\tilde{i}_1\ (\tilde{t} = T_2,\ \text{state 2}) = \tilde{i}_1\ (\tilde{t} = 0,\ \text{state 1})$$
$$\tilde{v}_c\ (\tilde{t} = T_2,\ \text{state 2}) = \tilde{v}_c\ (\tilde{t} = 0,\ \text{state 1})$$

By direct substitution, we arrive at the following set of four equations in the four unknowns $\tilde{i}_{11}, \tilde{i}_{12}, \tilde{v}_{c1}, \tilde{v}_{c2}$ assuming G, T_1, T_2 are given,

$$1 - G(\tilde{v}_{c1} + 1)\sin T_1 - (1 - \tilde{i}_{11})\cos T_1 = \tilde{i}_{12} \qquad (12)$$

$$(\tilde{v}_{c1} + 1)\cos T_1 - \frac{1 - \tilde{i}_{11}}{G}\sin T_1 - 1 = \tilde{v}_{c2} \qquad (13)$$

$$-G(\tilde{v}_{c2} + 1)\sin T_2 + \tilde{i}_{12}\cos T_2 = \tilde{i}_{11} \qquad (14)$$

$$(\tilde{v}_{c2} + 1)\cos T_2 + \frac{\tilde{i}_{12}}{G}\sin T_2 - 1 = \tilde{v}_{c1}. \qquad (15)$$

These four equations can be solved for different values of G, T_1 and T_2

to get $\tilde{i}_{11}$, $\tilde{i}_{12}$, $\tilde{V}_{c1}$ and $\tilde{V}_{c2}$. It is convenient to define three non-dimensional quantities T, f, and ρ, where

T ≡ normalized period in one full SCR switching cycle

($T = T_1 + T_2$).

f ≡ SCR switching frequency ($= 1/T\sqrt{2LC}$)

and $\rho \equiv T_1/T_2$.

As a reminder,

$$G = \frac{V_g}{I}\sqrt{\frac{C}{2L}}$$

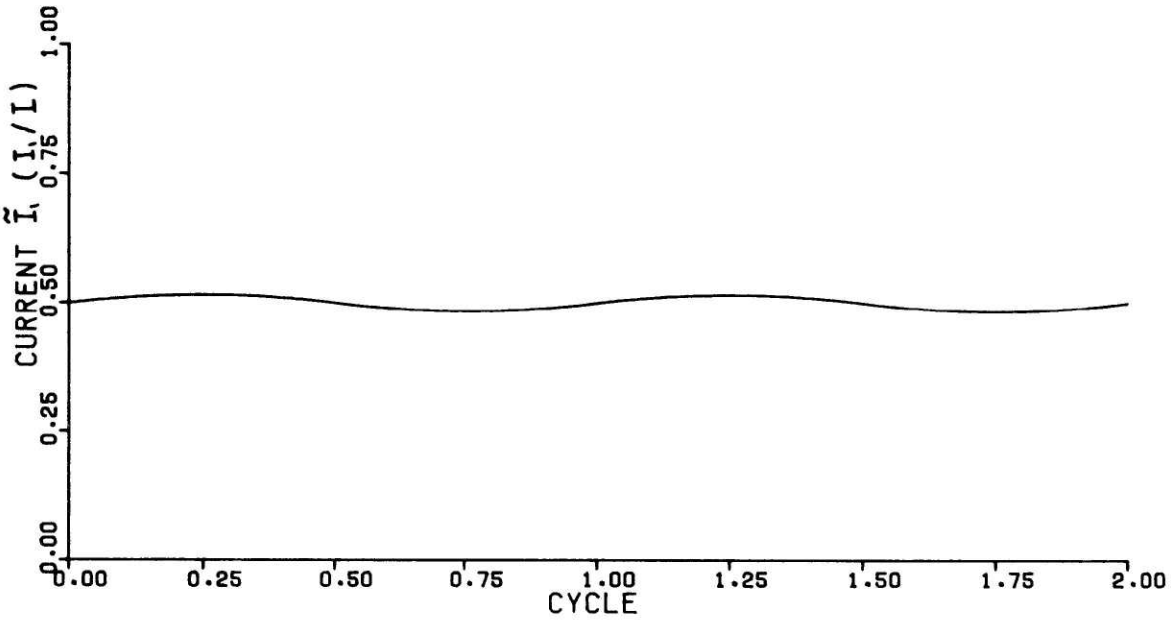
B. 1 Steady State Dynamic Solution

A computer program was written to solve this set of four simultaneous linear equations for different values of G, T, and ρ. The steady state current through electrode one $\tilde{i}_1$ ($= i_1/I$) and the voltage across the capacitor $\tilde{V}_c$ ($= V_c/V_g$) are plotted for some values of G, T, and ρ in Figure 3. 4 through Figure 3.8.

Several observations can be made by looking at the computer printout (not included) and the plots.

1. The dependence of electrode currents ($\tilde{i}_1$ and $\tilde{i}_2$) and capacitor voltage ($\tilde{V}_c$) on V_g, I, C, and L comes only in the form of two nondimensional parameters, namely $G = \frac{V_g}{I}\sqrt{\frac{C}{2L}}$ and $T = \frac{1}{f\sqrt{2LC}}$.

2. A comparison of Figure 3.4 with Figure 3.8 (or similarly, by looking at the computer printout) shows that the normalized electrode current $\tilde{i}_1$ is not a function of the parameter G. Moreover, the electrode currents $\tilde{i}_1$ and $\tilde{i}_2$ are always at the same value when the circuit changes state, that is



G = 0.02
T = 1.00
ρ = 1.00

a

H6332

Figure 3.4a Steady State $\tilde{i}_1$ Plot for $\rho = 1$

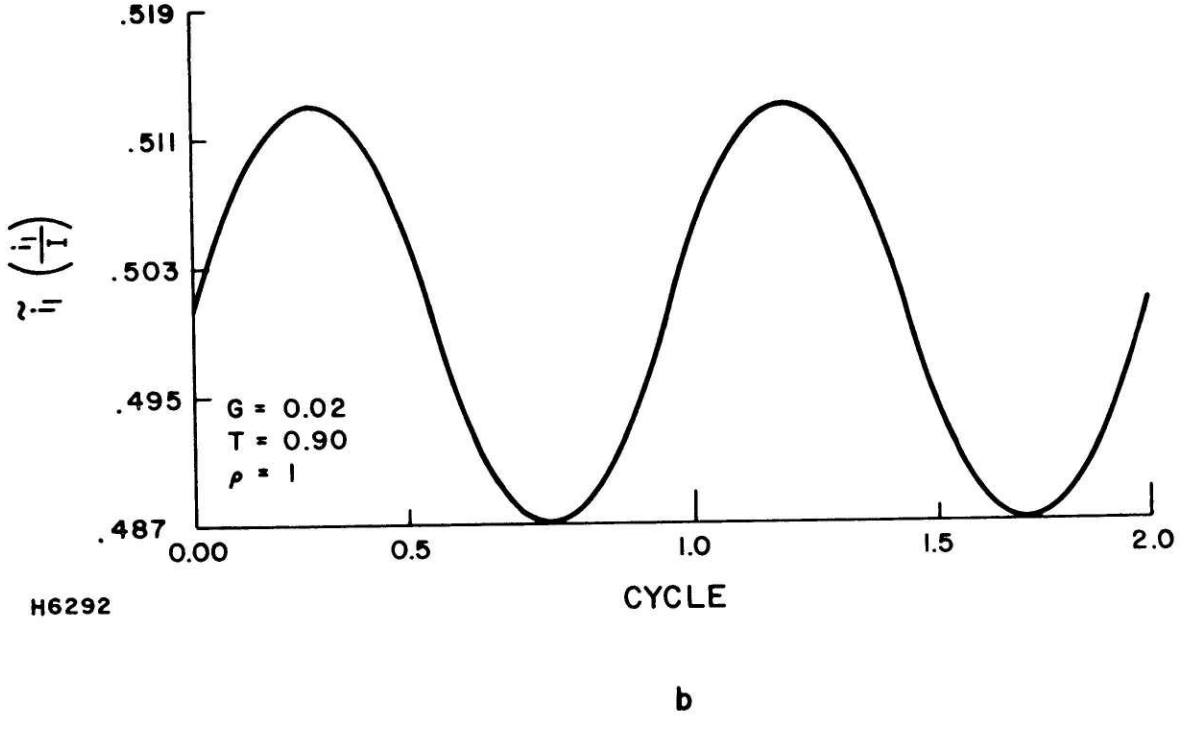


Figure 3.4b Steady State $\tilde{i}_1$ Plot, Exploded to see the Wave Shape

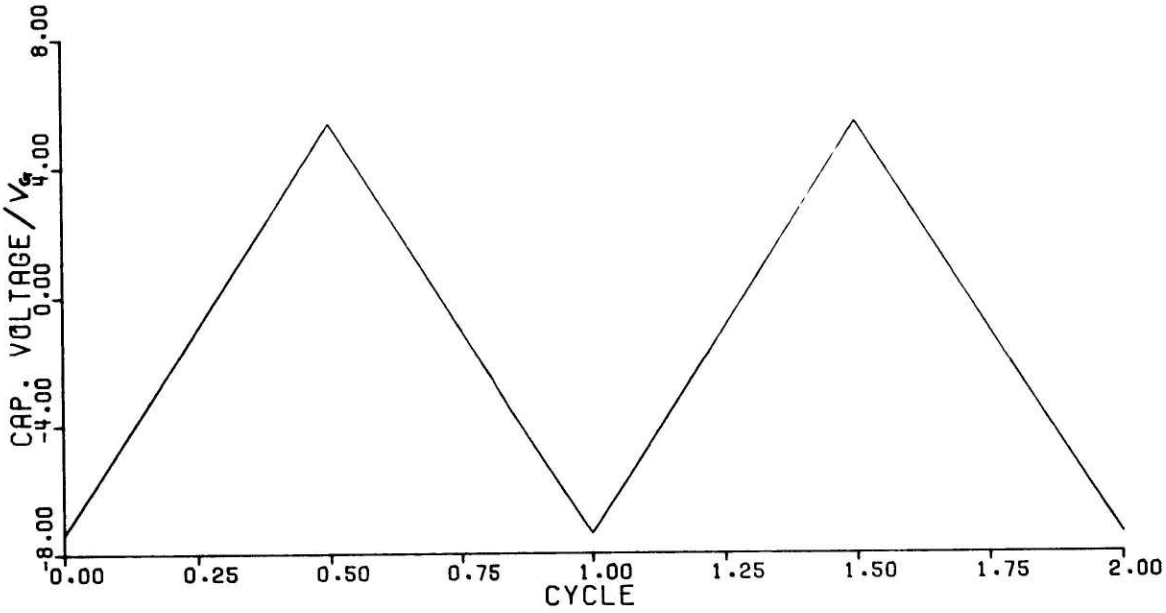
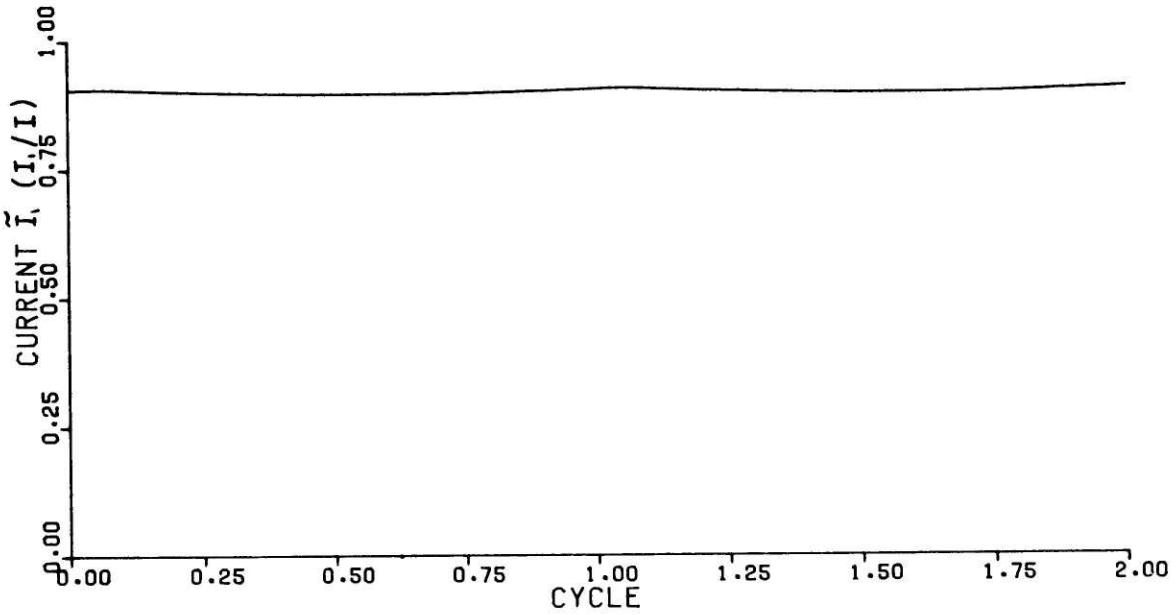


Figure 3.5 Steady State $\tilde{V}_c$ Plot for $\rho = 0.11$



G = 0.02
T = 1.00
ρ = 0.11

H6331

Figure 3.6 Steady State $\tilde{i}_1$ Plot for $\rho = 0.11$

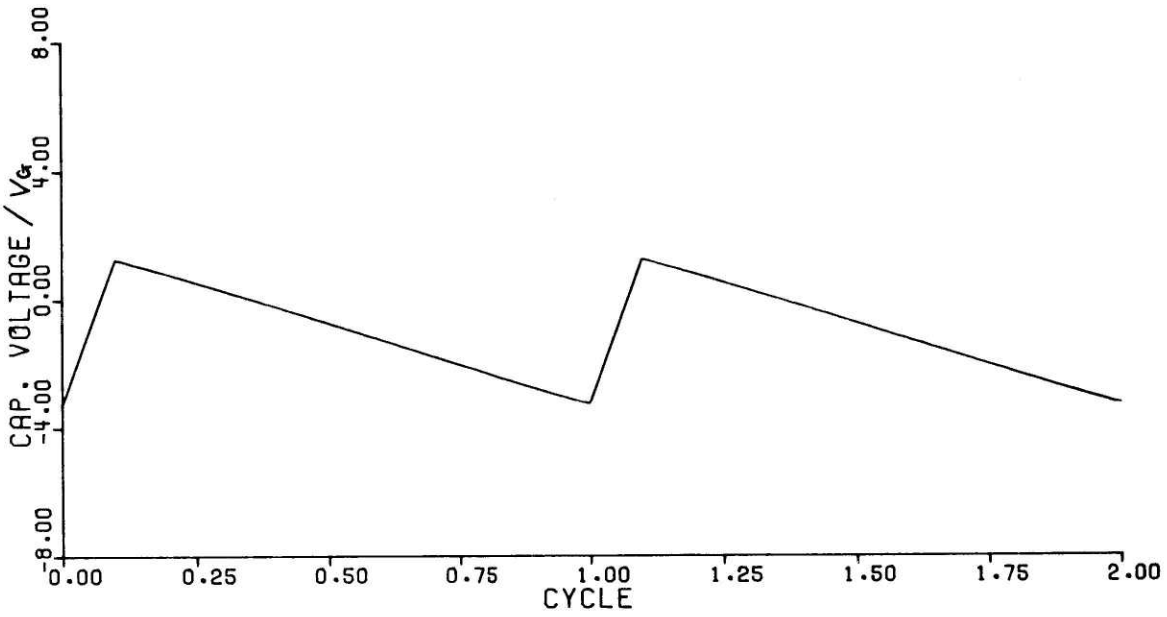


Figure 3.7 Steady State $\tilde{V}_c$ Plot for $\rho = 0.11$

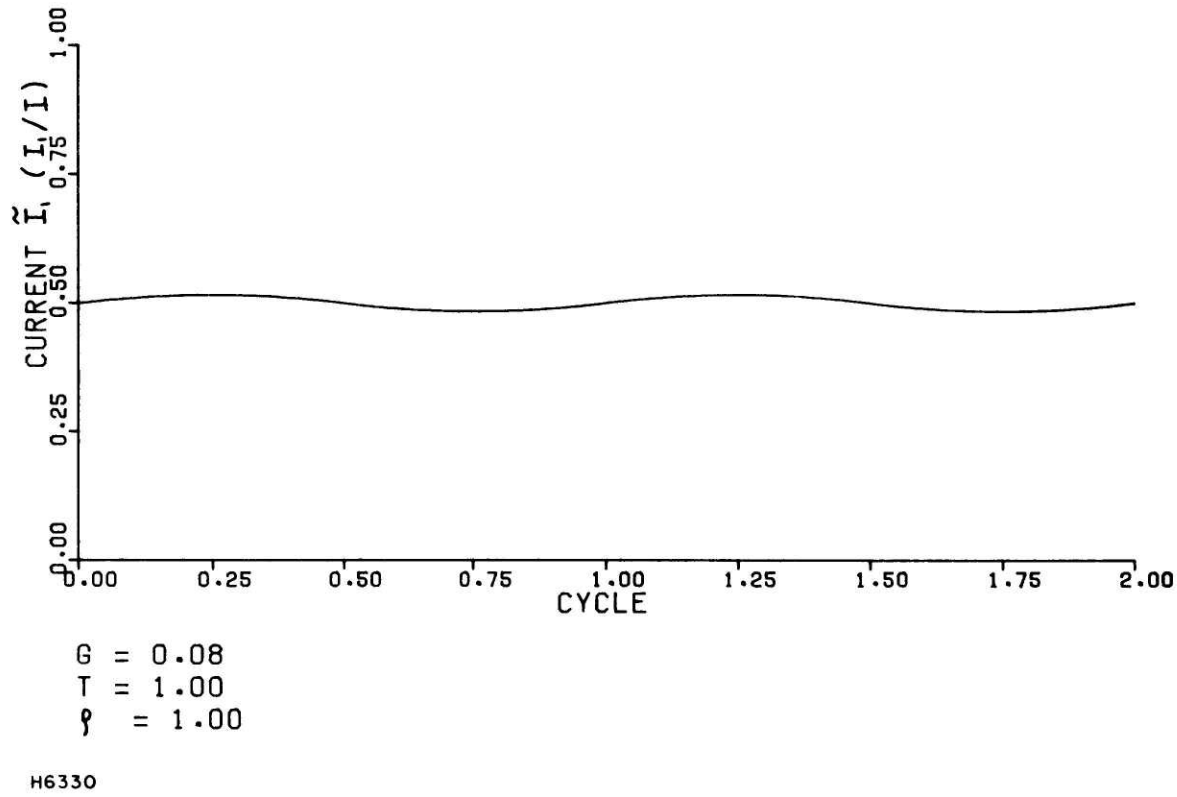


Figure 3.8 Steady State $\tilde{i}_1$ Plot for G = 0.08

$$\tilde{i}_{11} = \tilde{i}_{12}$$

and is a function of $\wp\left(\frac{T_1}{T_2}\right)$ only.

These results are not that shocking if we go back and look at the equations that generate these plots. Substituting

S_1 for $\sin T_1$,

C_1 for $\cos T_1$,

S_2 for $\sin T_2$,

and C_2 for $\cos T_2$,

equations (12) to (15) become

$$1 - G(\tilde{V}_{c1} + 1) S_1 - (1 - \tilde{i}_{11}) C_1 = \tilde{i}_{12}$$

$$(\tilde{V}_{c1} + 1) C_1 - \frac{1 - \tilde{i}_{11}}{G} S_1 - 1 = \tilde{V}_{c2}$$

$$-G(\tilde{V}_{c2} + 1) S_2 + \tilde{i}_{12} C_2 = \tilde{i}_{11}$$

$$(\tilde{V}_{c2} + 1) C_2 + \frac{\tilde{i}_{12}}{G} S_2 - 1 = \tilde{V}_{c1}$$

Solving this set of equations yeilds

(a) $\tilde{i}_{11} = \tilde{i}_{12}$

(b) $\tilde{i}_{11} = \dfrac{S_2 + C_2 S_1 - S}{S_2 + S_1 - S}$, where $S = S_2 C_1 + S_1 C_2$

or

$$\tilde{i}_{11} = \tilde{i}_{12} = \frac{\sin T_2 - \cos T_1 \sin T_2}{\sin T_2 + \sin T_1 - \sin T_1 \cos T_2 - \sin T_2 \cos T_1}$$

hence, $\tilde{i}_{11}$ and $\tilde{i}_{12}$ are independent of G.

To see why the electrode current $\tilde{i}_1$ is not a function of G, go back to equation (8),

$$\tilde{i}_1 = 1 - G(\tilde{V}_{c1} + 1) \sin \tilde{t} - (1 - \tilde{i}_{11}) \cos \tilde{t}. \qquad (8)$$

Look at the terms on the right hand side of equation (8). We just showed that $\tilde{i}_{11}$ is independent of G. If we can show that G ($\tilde{V}_{c1}$ + 1) is independent of G, then $\tilde{i}_1$ has to be independent of G. (Equation (8) describes $\tilde{i}_1$ for state 1 only, but a similar argument can be gone through for equation (10)).

The term G ($\tilde{V}_{c1}$ + 1) is not a function of time. Pick $\tilde{t} = T_1$ and substitute into equation (8). We have

$$\tilde{i}_{11} = 1 - G(\tilde{V}_{c1} + 1)\sin T_1 - (1 - \tilde{i}_{11})\cos T_1,$$

and

$$G(\tilde{V}_{c1} + 1) = \frac{(1 - \tilde{i}_{11})(1 - \cos T_1)}{\sin T_1}$$

None of the terms to the right of the equality sign is dependent on G, hence G ($\tilde{V}_{c1}$ + 1) is independent of G, and so, $\tilde{i}_1$ is independent of G.

That $\tilde{i}_1$ is independent of G has a very important consequence. As explained in Chapter 1, one of the moltivations for developing consolidation circuits is such that current non-uniformity can be reduced. One type of current non-uniformity is electrode current fluctuation which can be expressed as

$$\frac{\Delta i}{i} \equiv \frac{\text{maximum i - average i}}{\text{average i}}$$

where i can be the current in any electrode. (The other type of current non-uniformity is current distribution between electrodes, and is taken up in the next paragraph.) From equation (8), we found that, for $\rho = T_1/T_2 = 1$,

$$\frac{\Delta i_1}{i_1} = \sec\left(\frac{T}{4}\right) - 1$$

$$= \sec\left(\frac{1}{4f\sqrt{2LC}}\right) - 1.$$

Thus, current fluctuation is independent of G, and decreases as f, SCR switching frequency, increases.

3. If we write I_1 as the time average of $\tilde{i}_1$, and I_2 as the time average of $\tilde{i}_2$, then

$$\frac{I_1}{I_2} \cong \rho \quad \left(= \frac{T_1}{T_2}\right).$$

To demonstrate, in Figure 3.4, $\rho = 1$, and

$$I_1 = 0.5$$

$$I_2 = 1 - I_1 = 0.5$$

therefore $$\frac{I_1}{I_2} = 1 = \frac{T_1}{T_2}.$$

In Figure 3.6, $$\rho = 0.9$$

$$I_1 = 0.906$$

$$I_2 = 1 - I_1 = 0.094$$

and $$\frac{I_1}{I_2} = 9.6 = \frac{T_1}{T_2}.$$

4. Time average of voltage across the capacitor $\tilde{V}_c = -1$ (or equivalently, time average of $V_c = -V_g$). This is a direct consequence of the fact that time average of the voltages across the two inductors being equal to zero.

$$\frac{1}{T}\int_0^T L \frac{d\tilde{i}_n}{d\tilde{t}}\, d\tilde{t} = \frac{1}{T}\int_0^{T_1} L \frac{d\tilde{i}_n}{d\tilde{t}}\, d\tilde{t} + \int_0^{T_2} \frac{1}{T} L \frac{d\tilde{i}_n}{d\tilde{t}}\, d\tilde{t}$$

$$= 0 \qquad \text{for} \quad n = 1, 2$$

since $\tilde{i}_{11} = \tilde{i}_{12}$.

5. Maximum voltage across the capacitor V_{MAX} (equals to the maximum value of $\tilde{V}_c$) is an inverse function of G. This can be seen from the computer printout (not shown). For the same T (equals to 0.9) and ℓ (equals to 1),

$$V_{MAX} = 6.722 \text{ for } G = 0.02,$$

and

$$V_{MAX} = 2.43 \text{ for } G = 0.08.$$

This result makes sense because $G = \frac{V_g}{I}\sqrt{\frac{C}{2L}}$. Decreasing G corresponds to decreasing V_g or C or increasing I or L. Since

$$\tilde{V}_c = \frac{1}{C}\int \tilde{i}\, d\tilde{t},$$

increasing I or decreasing C obviously increases V_{MAX}. The effects of changing V_g and L is not as obvious because V_{MAX} is normalized by V_g, and increases L decreases G but also decreases T, which is another parameter that determines V_{MAX}.

For the sake of completeness, the energy stored in the two inductors and in the capacitor normalized by $1/2\ L\ I^2$ is plotted in Figures 3.9 and 3.10 for G = 0.02, T = 0.90, and ℓ = 1.

Energy stored in the capacitor is maximum at the switching point when the voltage is at maximum. Energy stored in the two inductors is maximum when the current in one electrode reaches maximum (and the current in the other electrode reaches minimum).

B.2 Two Important Parameters - G and T

There are three operating parameters for the circuit of Figure 3.1

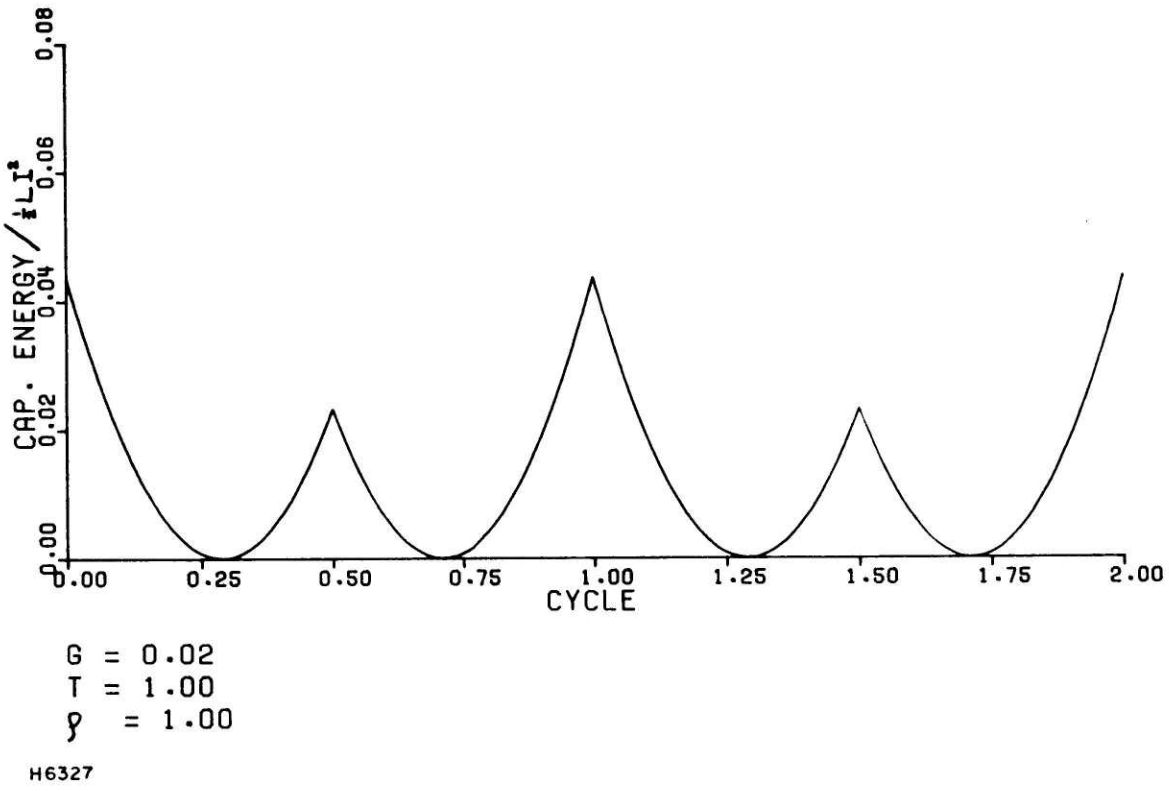


Figure 3.9 Steady State Capacitor Energy Storage

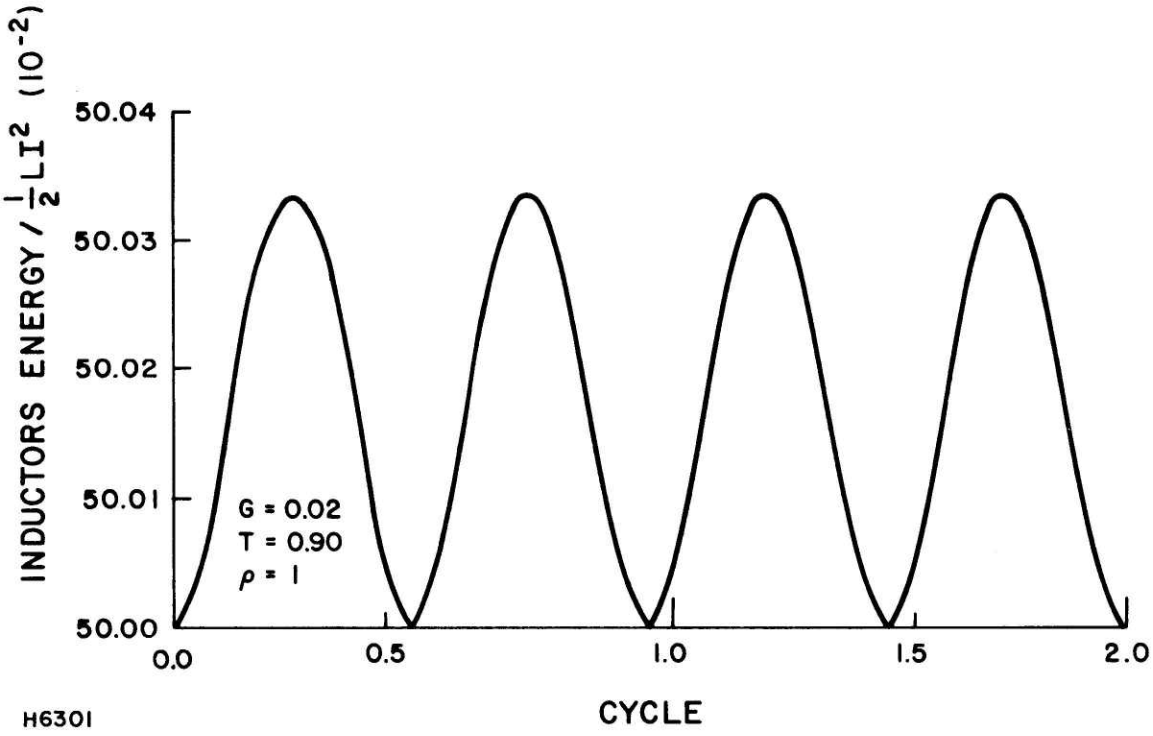


Figure 3.10 Steady State Inductor Energy Storage

which are of interest:

1. Electrode current fluctuation $\frac{\Delta i}{i}$. This has been mentioned in Chapter 1 and again, in the previous section (B. 1). In short, one purpose of having a consolidation circuit is to keep the current generated by the MHD channel evenly distributed between all electrodes and keep current fluctuation in each individual electrode low.

2. Available SCR turn-off time, τ_c (normalized on $\sqrt{2LC}$). For proper operation, the time between the SCRs switch and the capacitor changes polarity, which we call the "available SCR turn-off time", is longer than the actual time required for the SCR to turn off.

3. Maximum capacitor voltage V_{MAX} (normalized on V_g). Excessive voltage can damage the SCRs.

In Figure 3. 11 to Figure 3. 15, the three operating parameters mentioned above are plotted against either G or T. Notice that the available turn-off time τ_c is non-dimensionalized on $\sqrt{2LC}$. As an example, if

$$L = 5 \text{ millihenrys}$$

$$C = 4 \text{ microfarads,}$$

then $$\sqrt{2LC} = 0.2 \text{ milliseconds.}$$

So, $\tau_c = 0.1$ corresponds to available turn-off time of 20 microseconds.

As the non-dimensional period T ($= \frac{1}{f\sqrt{2LC}}$) is increased:

i. Electrode current fluctuation $\frac{\Delta i}{i}$ increases

ii. More current flow into the capacitor and therefore increases V_{MAX}.

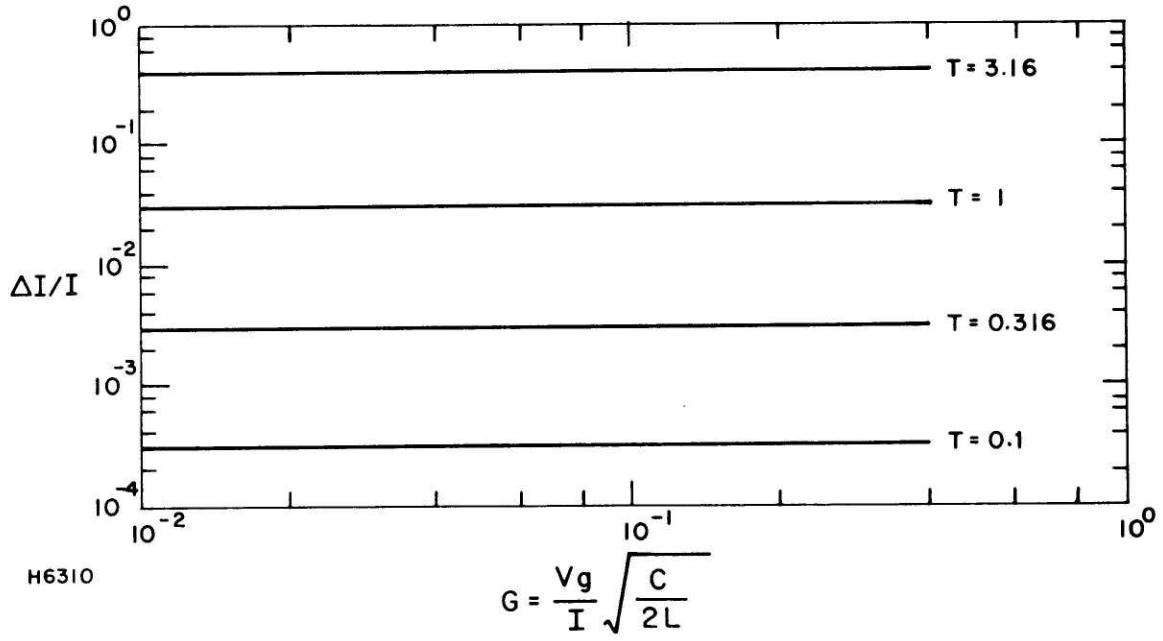


Figure 3.11a ΔI/I vs G for Different Values of T, Constant Load Current

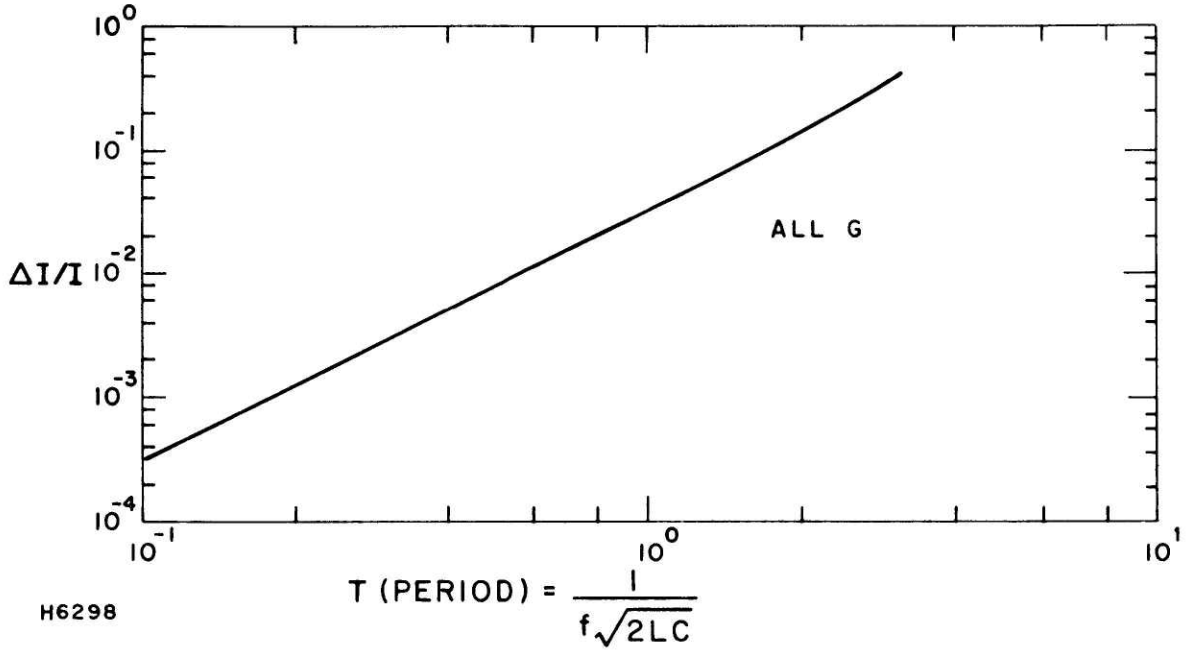


Figure 3.11b $\Delta I/I$ vs T, Constant Load Current

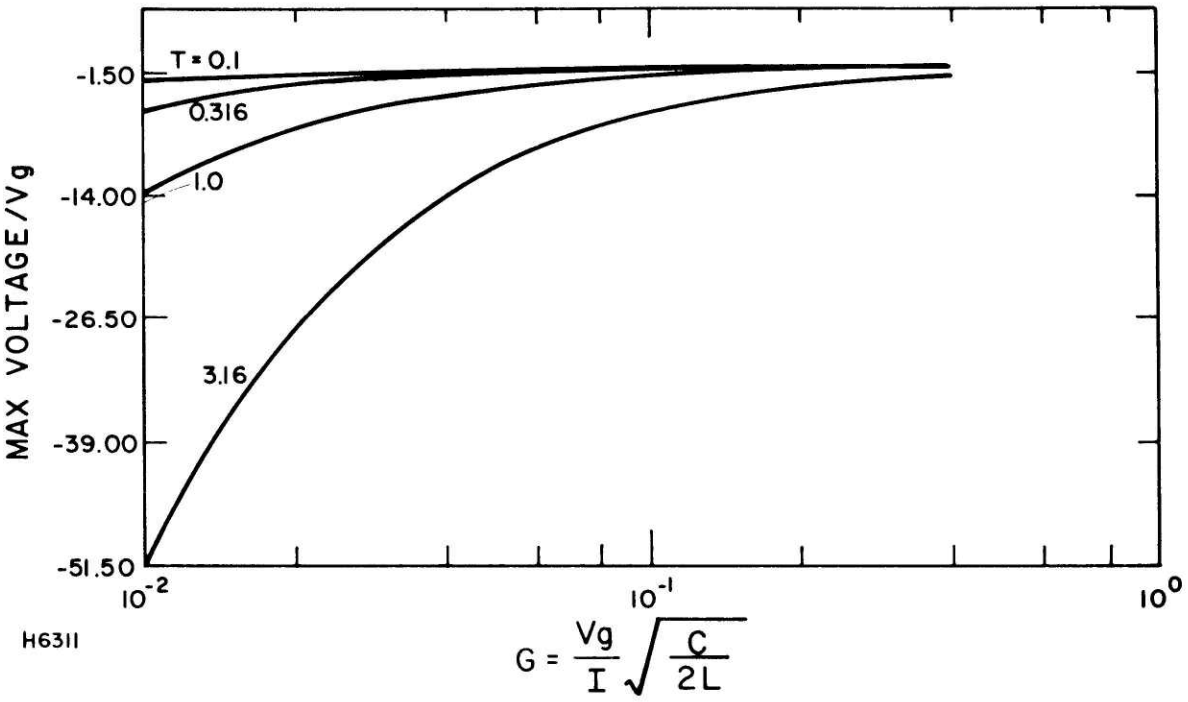


Figure 3.12 V_{MAX} vs G for Different Values of T, Constant Load Current

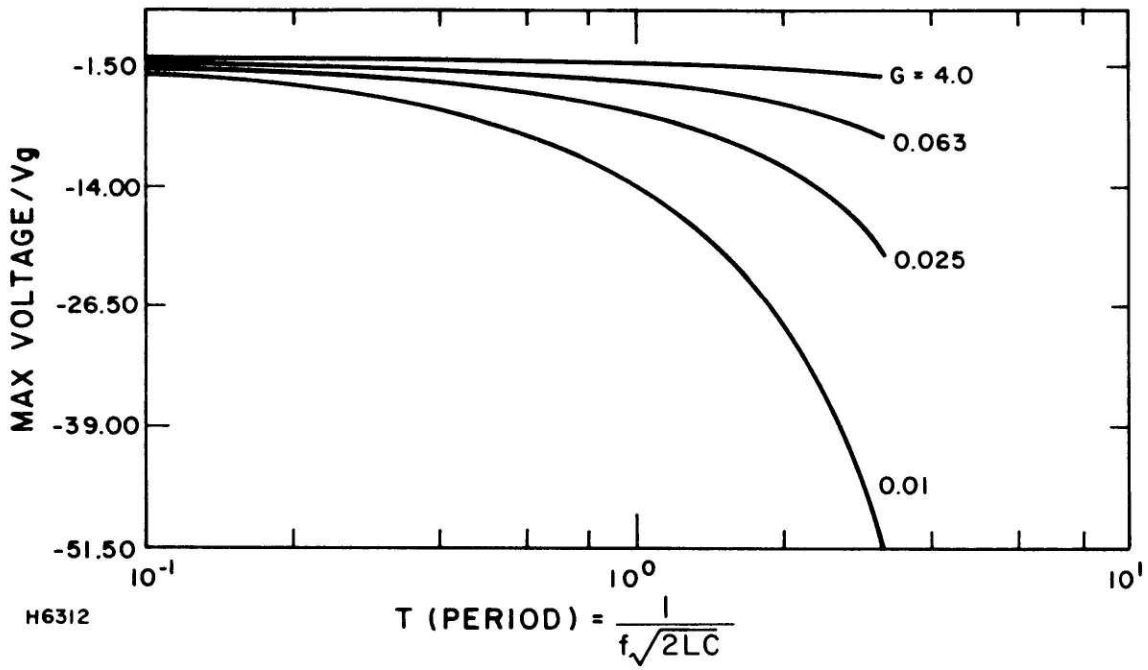


Figure 3.13 V_{MAX} vs T for Different Values of G, Constant Load Current

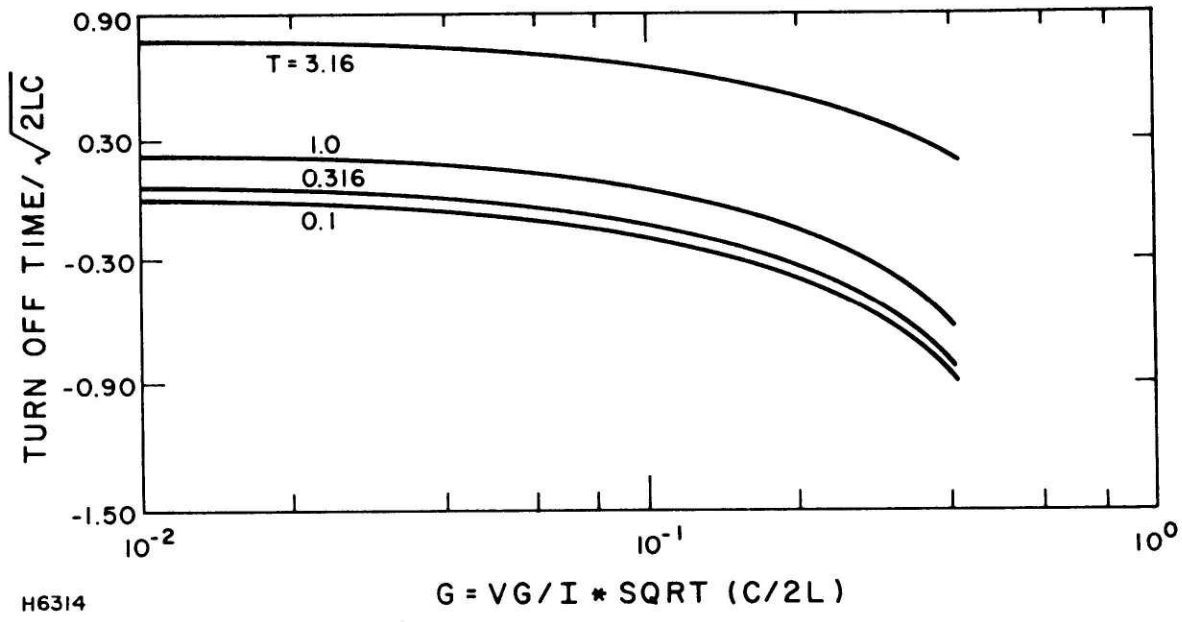


Figure 3.14 Turn-Off Time vs G for Different Values of T, Constant Load Current

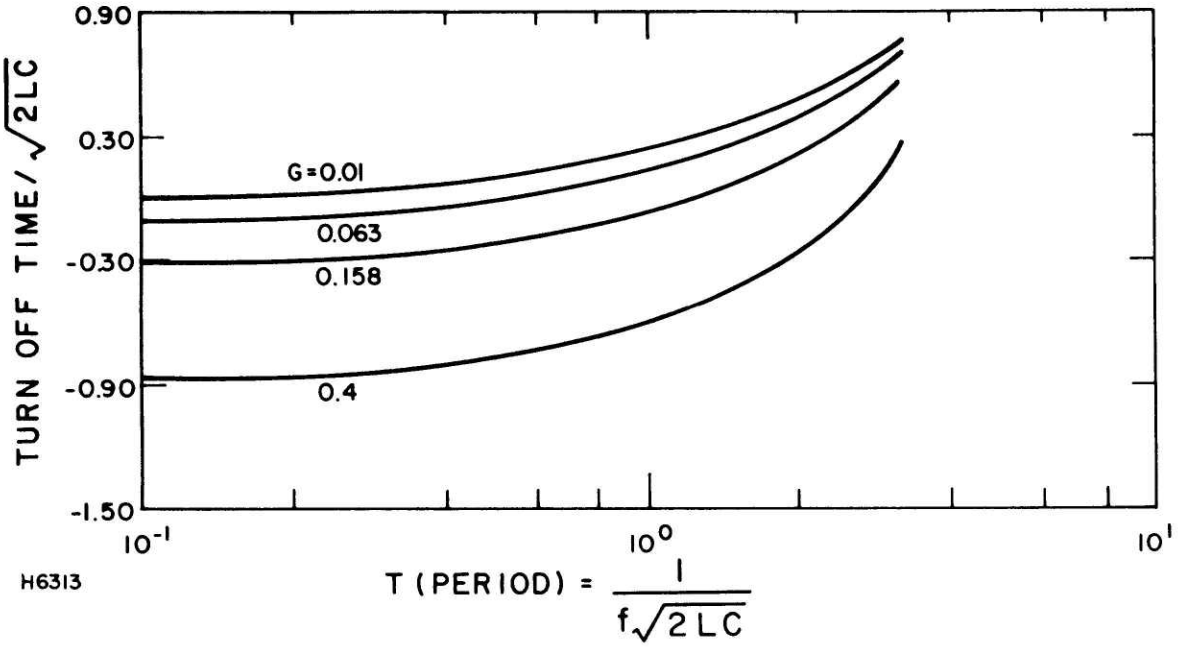


Figure 3.15 Turn-Off Time vs T for Different Values of G, Constant Load Current

iii. As V_{MAX} increases, the available turn-off time τ_c also increases.

As the non-dimensional parameter G is increased:

i. Electrode current fluctuation is unaffected.

ii. V_{MAX} decreases (alaready discussed in Section B. 1 above).

iii. τ_c also decreases.

B. 3 Performance Map

The varies dependence as noted in Section B. 2 can be conveniently put together into what will be called a performance map which is constructed by lines of constant electrode current fluctuation $\frac{\Delta i}{i}$ (written as $\frac{\Delta I}{I}$ in the map), maximum capacitor voltage V_{MAX}, and available SCR turn-off time τ_c all plotted together on a T versus G axis where T and G are the two nondimensional parameters discussed in Section B. 2. A performance map is shown in Figure 3.16 for $\rho = \frac{T_1}{T_2} = 1$, that is, equal conducting times for the two SCRs.

The performance map is very helpful in designing a consolidation circuit, as explained in Chapter 5. For a particular application, the maximum electrode current fluctuation tolerable may be five percent. In a channel with a nominal interelectrode gap voltage of 20 volts, requiring that $V_{MAX} = 20$ corresponds to putting no more than 400 volts across the SCRs. For demonstration purpose, pick the normalized available turn-off time τ_c to be no less than 0. 1. Then, the operating domain will be the region enclosed by the shaded lines as shown in Figure 3. 16. Any value-pair of G and T that falls inside the operating domain satisfies the three conditions stated above. Given the values of

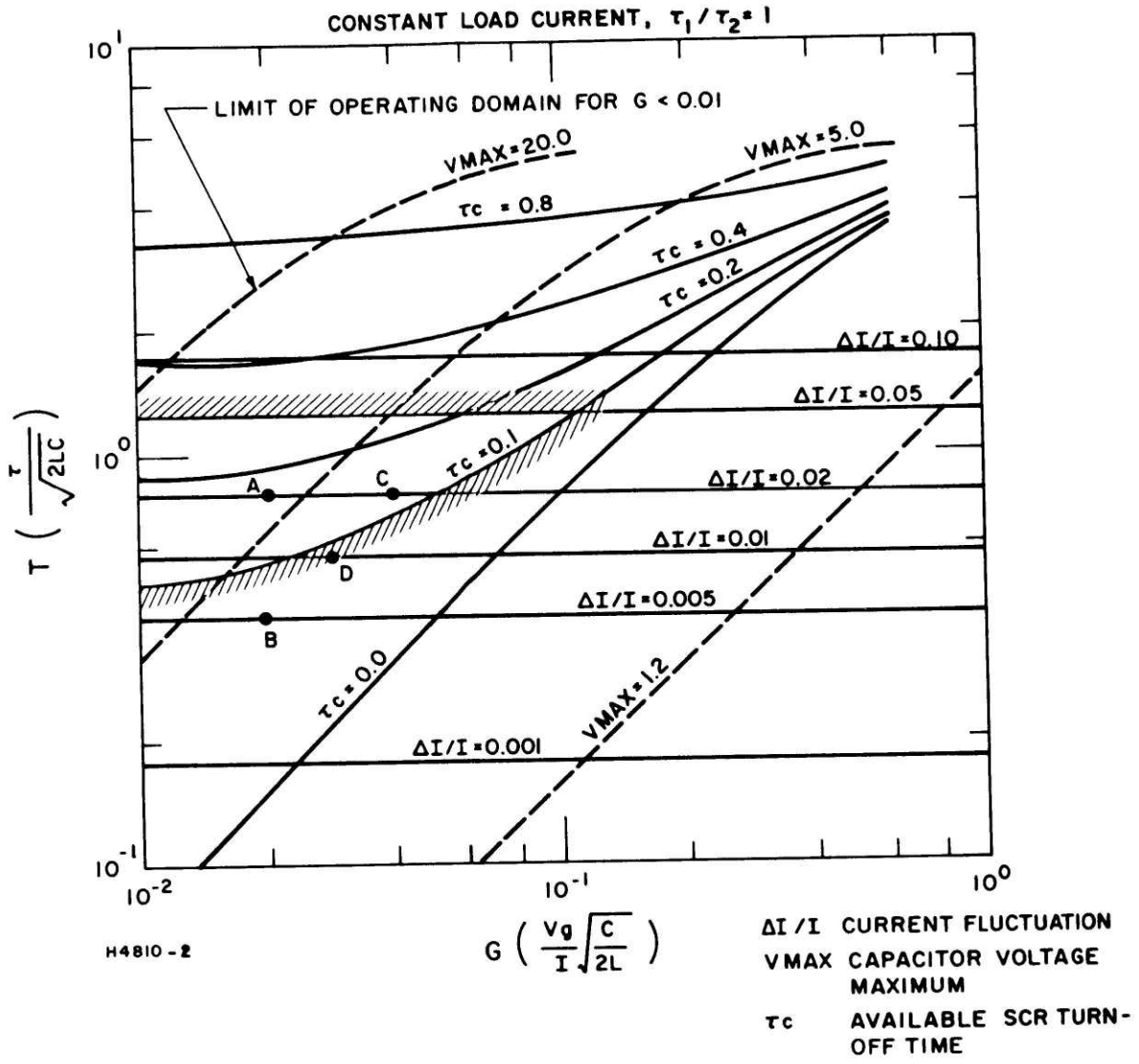


Figure 3.16 Performance Map for Constant Load Current, $\tau_1/\tau_2 = 1$

G and T, the values of L and C is a function only of the SCR switching frequency f, as follows:

since $$T = \frac{1}{f\sqrt{2LC}}$$

$$G = \frac{V_g}{I}\sqrt{\frac{C}{2L}},$$

then $$\sqrt{LC} = \frac{1}{\sqrt{2}\, f\, T}$$

$$\sqrt{\frac{L}{C}} = \frac{V_g}{\sqrt{2}\, G\, I},$$

and $$L = \frac{V_g}{2GIfT}$$

$$C = \frac{GI}{V_g f T}$$

where V_g and I, interelectrode gap voltage and total load current is assumed to be known. After the values of L and C are known, the time value of the available turn-off time is given by $\tau_c \sqrt{2LC}$. This value can then be compared to the turn-off time of the SCR to be used.

Because of the finite non-zero value of gap voltage, the circuit as shown in Figure 3.1 is not completely symmetrical. Performance map for $\rho = \frac{T_1}{T_2} = 0.5$ and $\rho = 2$ are shown in Figure 3.17 and 3.18 respectively. Of course, all the results we have so far in this chapter, including these performance maps, are for constant load current only.

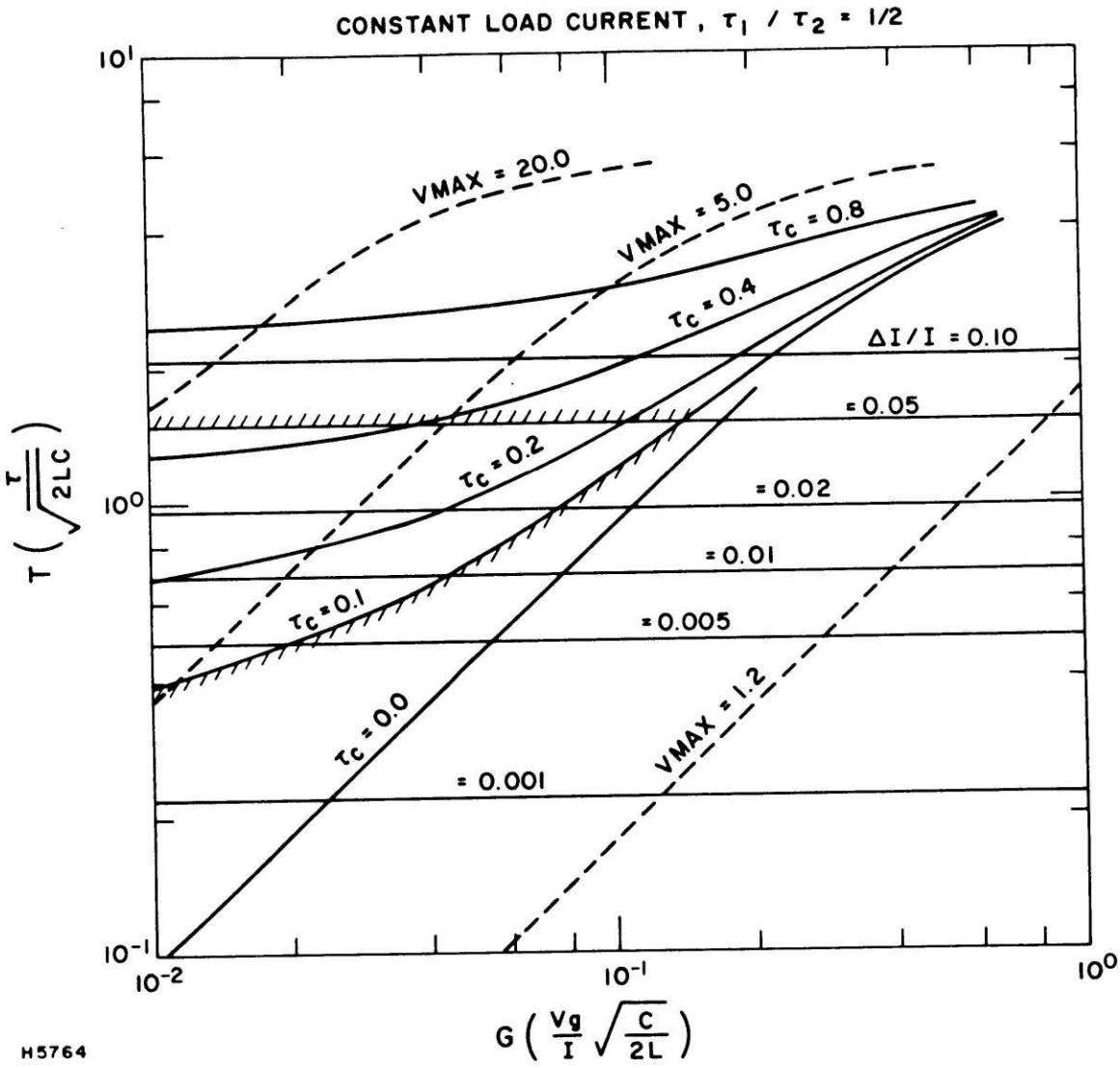


Figure 3.17 Performance Map for Constant Load Current, $\tau_1/\tau_2 = 0.5$

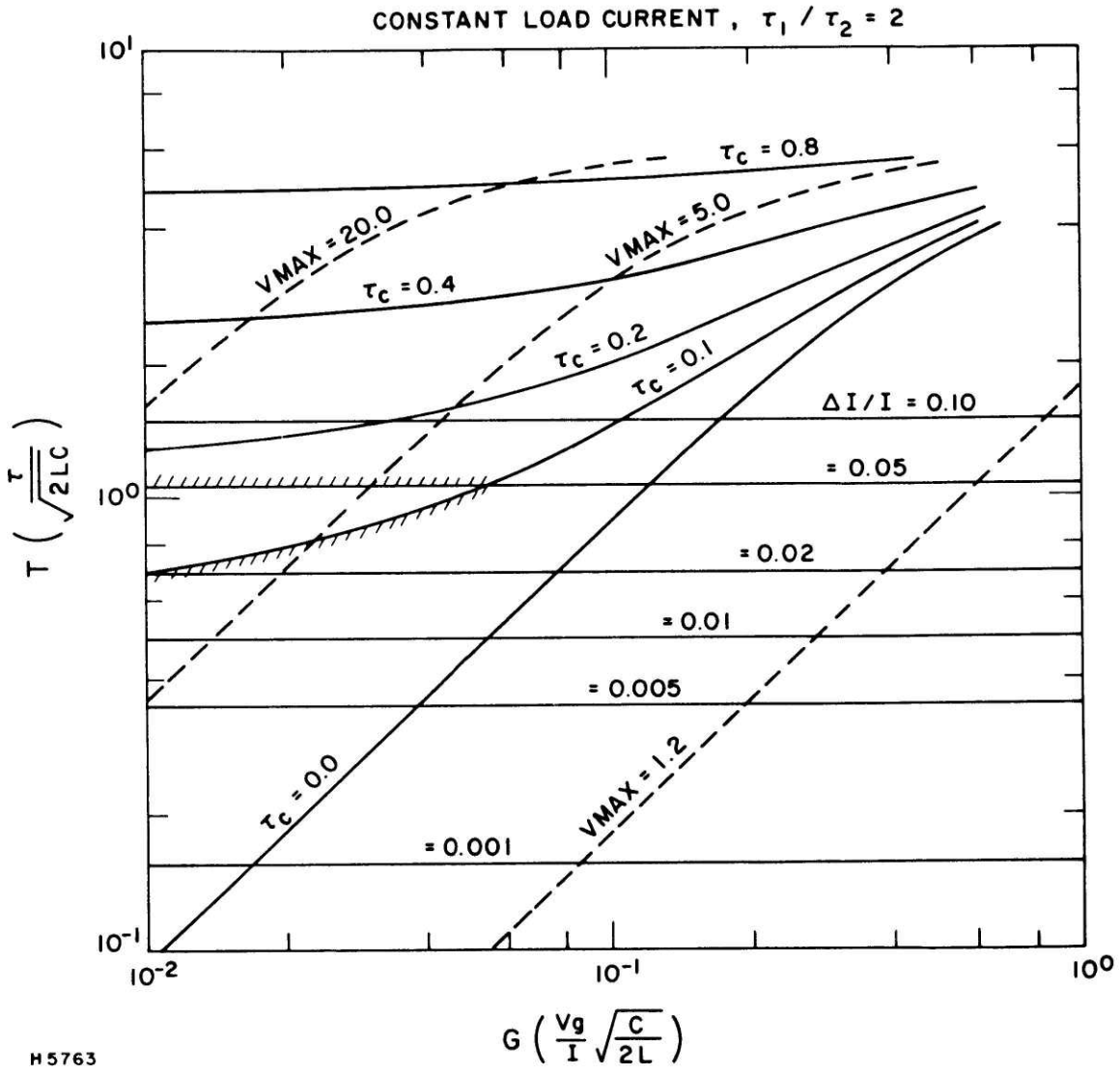


Figure 3.18 Performance Map for Constant Load Current, $\tau_1/\tau_2 = 2$

B. 4 Transient Solution

In a transient situation, a constant interelectrode gap voltage assumption is no longer valid. The gap voltage can fluctuate from negative to more than twice its nominal value depending on the current distribution between the electrodes. The V-I characteristic is roughly shown in Figure 3.19. I_1 and I_2 are the time average currents in any two adjacent electrodes and V_g is the voltage between them.

To take the fluctuation of gap voltage into account, the channel-consolidation circuit-load combination will be as shown in Figure 3.20a where a constant load current is again assumed. For this model to resemble the V-I characteristic shown in Figure 3. 19, we want:

i. $V = V_g$ when $i_1 = i_2$

i.e., $\frac{I}{2}(R_1 - R_2) = V_g$

or $$R_1 = \frac{2V_g}{I} + R_2$$

ii. $V = -\sigma V_g$ when $i_1 = 0$

i.e., $IR_2 = \sigma V_g$

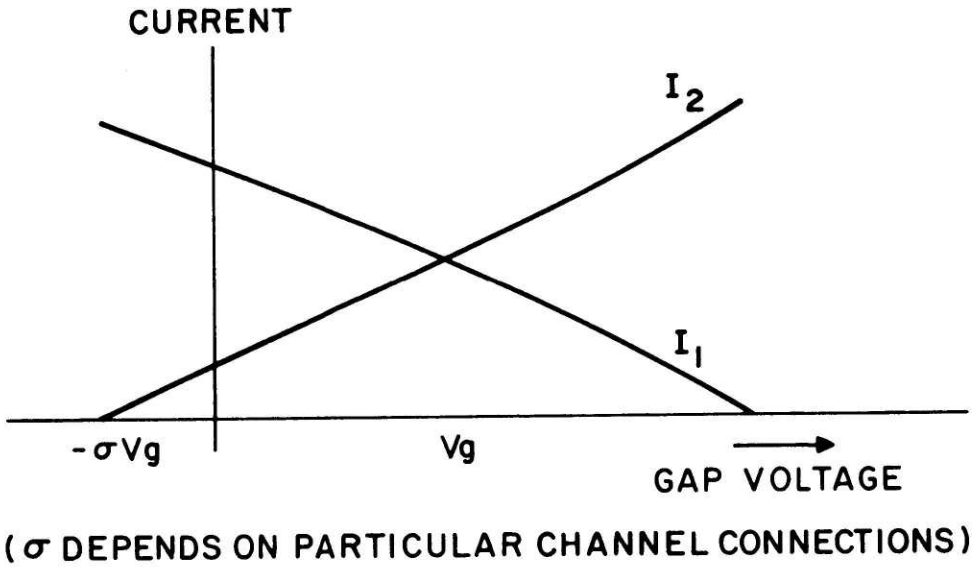
or $$R_2 = \sigma \frac{V_g}{I}$$

Define $R = R_1 + R_2$, then, we can eliminate V_g and I:

$$R_1 = 2\frac{R_2}{\sigma} + R_2 = \left(\frac{2}{\sigma} + 1\right) R_2$$

$$R = 2\left(\frac{1}{\sigma} + 1\right) R_2$$

$\therefore$ $$R_2 = \frac{R}{2}\frac{\sigma}{\sigma+1}$$



H6100

Figure 3.19 V-I Characteristic for Two Adjacent Electrodes Inside an MHD Channel

$$R_1 = \frac{R}{2}\frac{\sigma+2}{\sigma+1}.$$

State 1 (Figure 3.20a)

From Kirchhoff's current and voltage laws,

$$V_C + L\frac{di_1}{dt} + i_1R_1 - i_2R_2 - L\frac{di_2}{dt} = 0 \qquad (18)$$

$$i_1 + i_2 = I$$

and it follows that

$$\frac{di_1}{dt} + \frac{di_2}{dt} = 0.$$

Equation (18) becomes

$$-2L\frac{di_2}{dt} + V_C + IR_1 - i_2R = 0. \qquad (19)$$

We also have

$$i_2 = -C\frac{dV_C}{dt}. \qquad (20)$$

Non-dimensionalizing all current quantities by I,

all voltage quantities by IR,

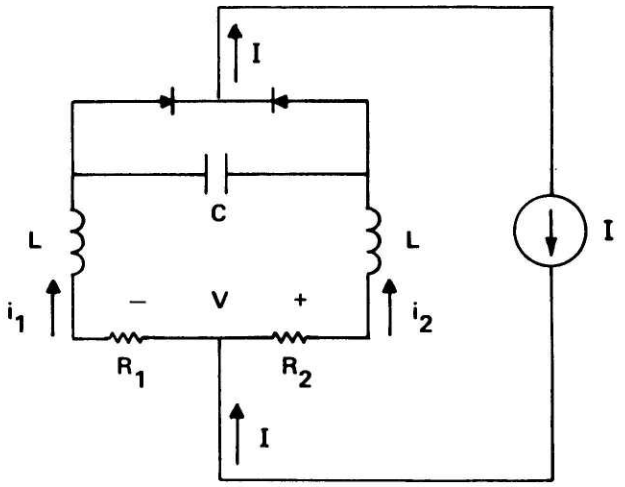
and time by

$$\left[\frac{1}{2LC} - \left(\frac{R}{4L}\right)^2\right]^{-\frac{1}{2}}$$

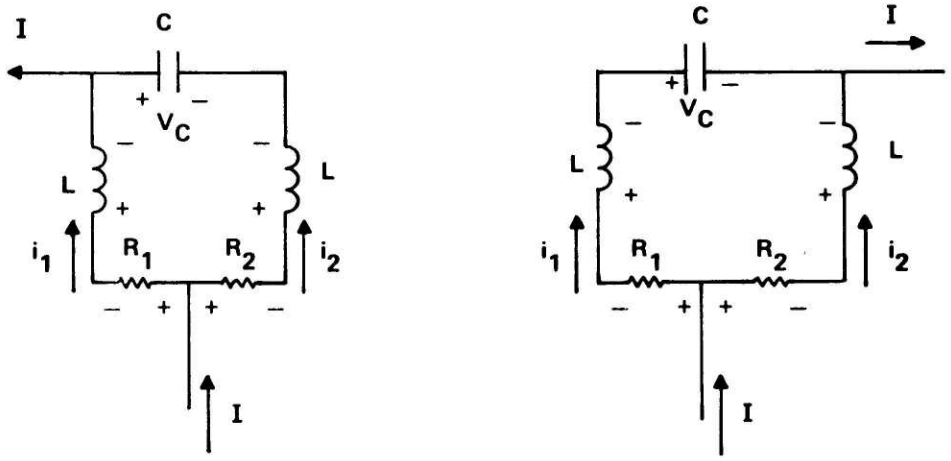
$$= \left[\frac{8L - R^2C}{16L^2C}\right]^{-\frac{1}{2}}$$

$$= \frac{4LC}{\sqrt{8LC - (RC)^2}} \equiv \theta.$$

Adding tildes to the normalized quantities, equations (19) and (20) become,



(A)



H6095 (B) (C)

Figure 3.20 a. System Model for Transient Analysis
b. Same System in State 1
c. Same System in State 2

after simplifying

$$-2\frac{L}{R\theta}\frac{d\tilde{i}_2}{d\tilde{t}} + \tilde{v}_c + \frac{R_1}{R} - \tilde{i}_2 = 0 \qquad (21)$$

$$\tilde{i}_2 = -\frac{RC}{\theta}\frac{d\tilde{v}_c}{d\tilde{t}} \qquad (22)$$

Expand and simplify,

$$\frac{2L}{R\theta} = \sqrt{\frac{2L}{R^2C} - \frac{1}{4}} = \sqrt{\alpha - \frac{1}{4}}$$

$$\frac{RC}{\theta} = \frac{\sqrt{\frac{2L}{R^2C} - \frac{1}{4}}}{\frac{2L}{R^2C}} = \frac{\sqrt{\alpha - \frac{1}{4}}}{\alpha}$$

where

$$\alpha \equiv \frac{2L}{R^2C}.$$

Substituting into and combining equations (21) and (22), we have

$$\sqrt{\alpha - \frac{1}{4}}\,\frac{d^2\tilde{i}_2}{d\tilde{t}^2} + \frac{\alpha}{\sqrt{\alpha - \frac{1}{4}}}\,\tilde{i}_2 + \frac{d\tilde{i}_2}{d\tilde{t}} = 0.$$

Introduce the differential operator $D = \frac{d}{dt}$, we have

$$\left(D^2 + \frac{1}{\sqrt{\alpha - \frac{1}{4}}}\,D + \frac{\alpha}{\alpha - \frac{1}{4}}\right)\tilde{i}_2 = 0,$$

and

$$D = -\frac{1}{2\sqrt{\alpha - \frac{1}{4}}} \pm \sqrt{\frac{1/4}{\alpha - 1/4} - \frac{\alpha}{\alpha - 1/4}}$$

$$= -\frac{1}{2\sqrt{\alpha - 1/4}} \pm j \qquad \text{where } j = \sqrt{-1}.$$

Therefore,

$$\tilde{i}_2 = \exp\left(-\frac{\tilde{t}}{2\sqrt{\alpha - 1/4}}\right)\left[\gamma_1 \cos\tilde{t} + \gamma_2 \sin\tilde{t}\right].$$

From equation (21),

$$\tilde{V}_c = \frac{R_1}{R} - \exp\left(-\frac{\tilde{t}}{2\sqrt{\alpha - 1/4}}\right)\left[\gamma_1 \cos\tilde{t} + \gamma_2 \sin\tilde{t}\right]$$
$$-\sqrt{\alpha - 1/4}\left\{-\gamma_1 \sin\tilde{t} + \gamma_2 \cos\tilde{t} - \frac{1}{2\sqrt{\alpha - 1/4}}(\gamma_1 \cos\tilde{t} + \gamma_2 \sin\tilde{t})\right\} \exp\left(-\frac{\tilde{t}}{2\sqrt{\alpha - 1/4}}\right).$$

$$= \frac{R_1}{R} - \exp\left(-\frac{\tilde{t}}{2\sqrt{\alpha - 1/4}}\right)\left\{\sqrt{\alpha - 1/4}\,(-\gamma_1 \sin\tilde{t} + \gamma_2 \cos\tilde{t}) + \frac{1}{2}(\gamma_1 \cos\tilde{t} + \gamma_2 \sin\tilde{t})\right\}.$$

The initial conditions are $\tilde{i}_2\,(\tilde{t} = 0) = \tilde{i}_{21} = 1 - \tilde{i}_{11}$

and $\tilde{V}_c\,(\tilde{t} = 0) = \tilde{V}_{c_1}$

where $\tilde{t}$ is measured from the beginning of each occurrence of state 1.

Substitute the initial conditions in the expressions for $\tilde{i}_2$ and $\tilde{V}_c$,

$\tilde{i}_2$ at $\tilde{t} = 0$: $\qquad \gamma_1 = 1 - \tilde{i}_{11}$ (23)

$\tilde{V}_c$ at $\tilde{t} = 0$: $\qquad \frac{R_1}{R} - \sqrt{\alpha - 1/4}\,\gamma_2 - \frac{\gamma_1}{2} = \tilde{V}_{c_1}$

therefore $\qquad \gamma_2 = \dfrac{\frac{R_1}{R} - \frac{1 - \tilde{i}_{11}}{2} - \tilde{V}_{c_1}}{\sqrt{\alpha - 1/4}}$ (24)

Define some new variables,

$$\beta \equiv \frac{R_1}{R} \tag{25}$$

$$\phi_1 \equiv \gamma_2 \sqrt{\alpha - 1/4} + \frac{\gamma_1}{2} = \beta - \tilde{v}_c \tag{26}$$

$$\phi_2 \equiv -\gamma_1 \sqrt{\alpha - 1/4} + \frac{\gamma_2}{2} \tag{27}$$

$$a \equiv \frac{1}{2\sqrt{\alpha - 1/4}} \tag{28}$$

and as defined already,

$$\alpha = \frac{2L}{R^2 C}. \tag{29}$$

We then have

$$\tilde{i}_1 = 1 - e^{-a\tilde{t}} (\gamma_1 \cos \tilde{t} + \gamma_2 \cos \tilde{t}) \tag{30}$$

$$\tilde{v}_c = \beta - e^{-a\tilde{t}} (\phi_1 \cos \tilde{t} + \phi_2 \sin \tilde{t}) \tag{31}$$

State 2 (Figure 3.20b)

Going through the same procedure as in State 1, and using the initial conditions $\tilde{i}_1 (\tilde{t}=0) = \tilde{i}_{12}$ and $\tilde{v}_c (\tilde{t}=0) = \tilde{v}_{c2}$ where $\tilde{t}$ is now measured from the beginning of each occurrence of State 2, one obtains the following:

$$\tilde{i}_1 = e^{-a\tilde{t}} (\gamma_3 \cos \tilde{t} + \gamma_4 \sin \tilde{t}) \tag{32}$$

$$\tilde{v}_c = 1 - \beta - e^{-a\tilde{t}} (\phi_3 \cos \tilde{t} + \phi_4 \sin \tilde{t}) \tag{33}$$

where

$$\gamma_3 = \tilde{i}_{12} \tag{34}$$

$$\gamma_4 = \frac{1 - \beta - \frac{\tilde{i}_{12}}{2} - \tilde{v}_{c2}}{\sqrt{\alpha - 1/4}} \tag{35}$$

$$\phi_3 = 1 - \beta - \tilde{v}_{c2} \tag{36}$$

$$\phi_4 = -\gamma_3\sqrt{\alpha - 1/4} + \frac{\gamma_4}{2} \qquad (37)$$

To get an idea of what these current and voltage waveforms represent, the above equations are plotted with

$$\left.\begin{aligned} L &= 5 \times 10^{-3} \text{ H} \\ C &= 4 \times 10^{-6} \text{ F} \\ R &= 20\Omega \end{aligned}\right\} \quad \alpha = 6$$

and $\sigma = 0.2$.

From equation (17), $\beta = \frac{R_1}{R} = \frac{1}{2}\frac{\sigma+2}{\sigma+1} = 0.92$.

Figures 3.21 through 3.23 show the predicted currents and voltage for different values of SCR switching period T and ratio of SCR conducting time ρ. Again, the method of assumed states is used. It can be observed that in some cases, the capacitor does not have the right polarity when the gate signal arrives.

C. Resistive Load

For a purely resistive loading, the load inductance is zero and the load is idealized as a simple resistor. Here, we are interested in the steady state operation so the interelectrode gap voltage can again be modelled by a simple voltage source. The channel-consolidation circuit-load system will then look like what is shown in Figure 3.24a.

State 1 (Figure 3.24b)

Again, using Kirchhoff's current and voltage laws, we get

$$i_1 + i_2 = i$$

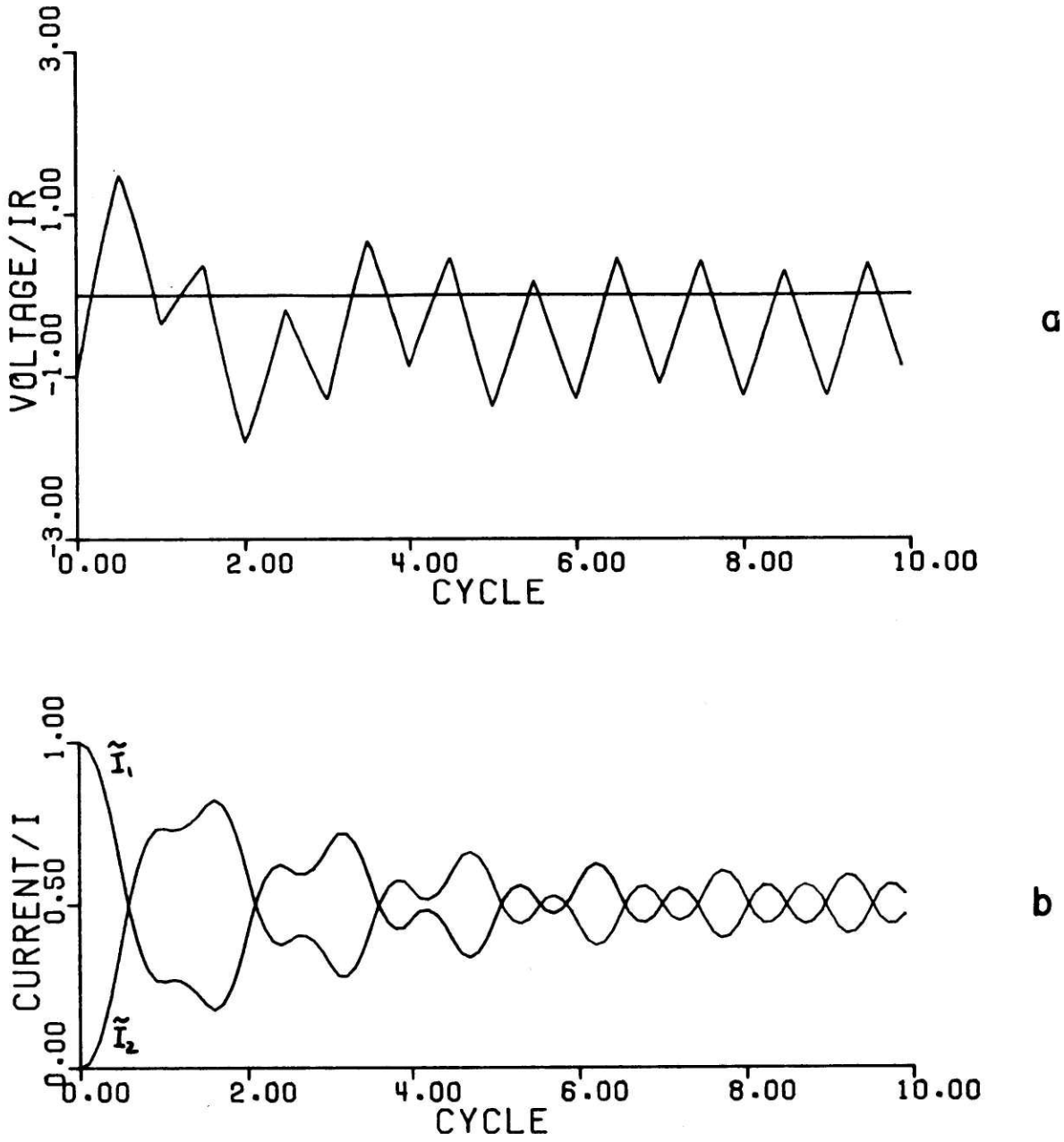


Figure 3.21 Transient Waveform for System in Constant Current Regime, T = 2, ρ = 1

a. voltage

b. current

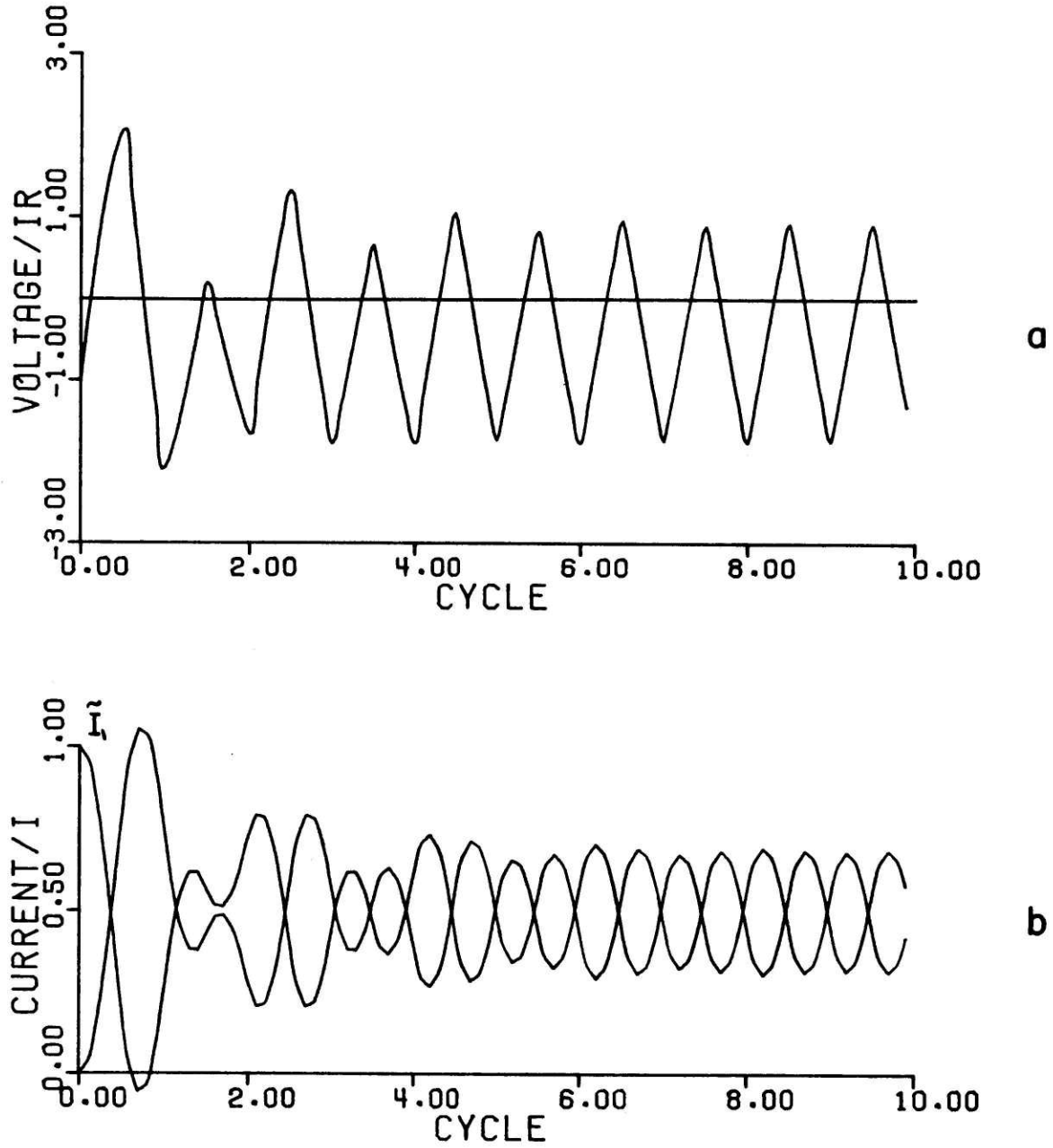


Figure 3.22 Transient Waveform for System in Constant Current Regime, T = 3, ρ = 1

a. voltage

b. current

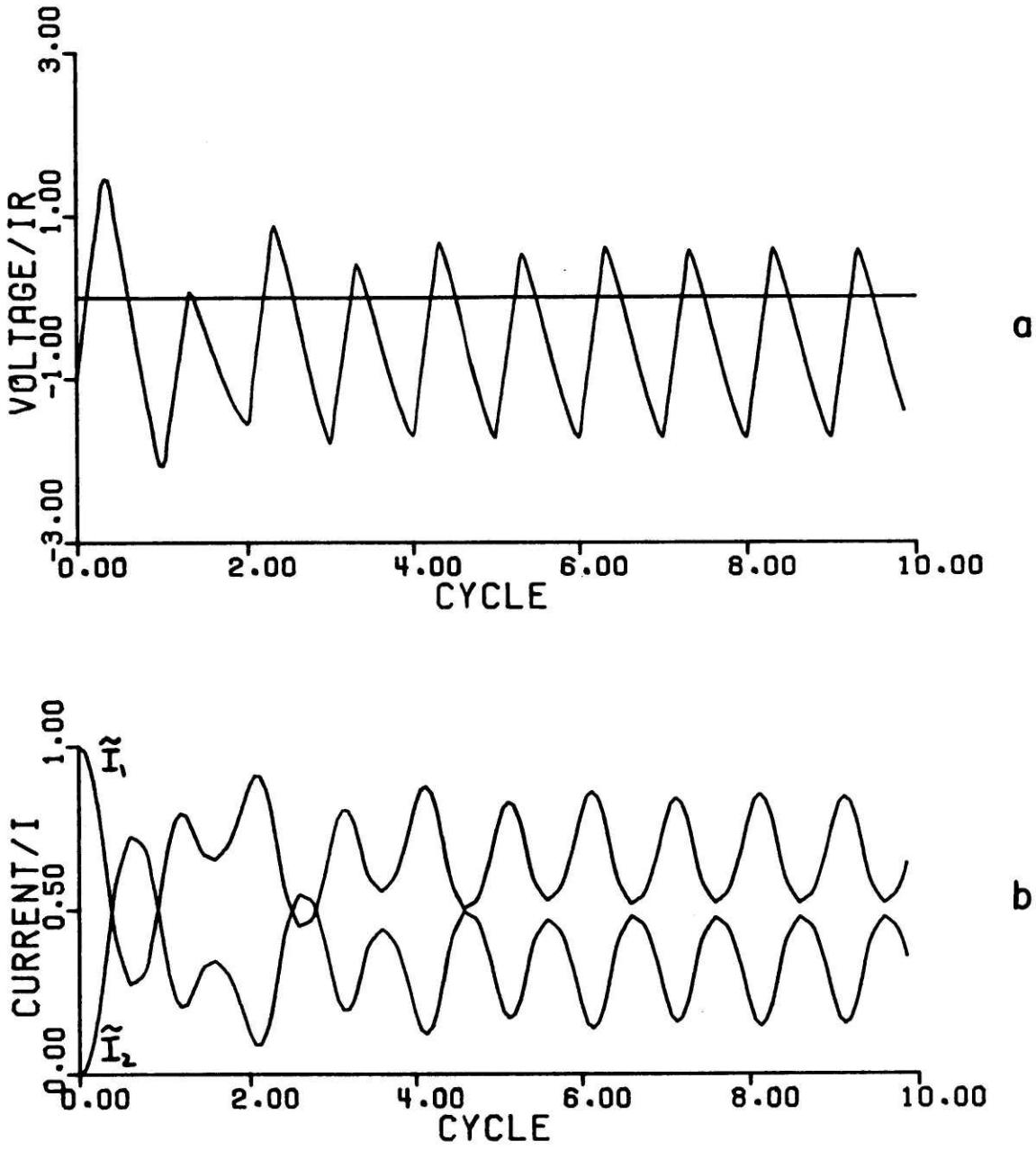


Figure 3.23 Transient Waveform for System in Constant Current Regime, T = 3, ρ = 2

a. voltage

b. current

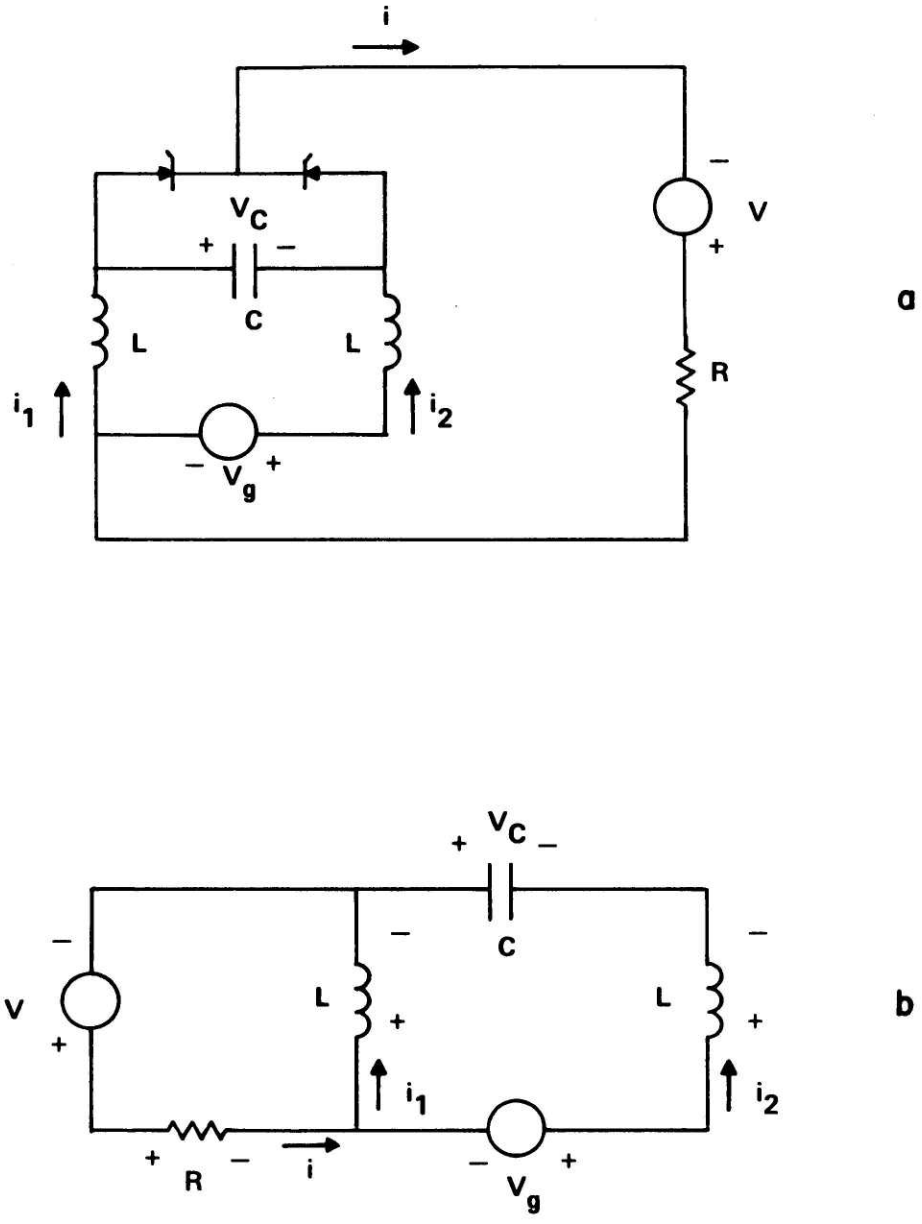


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Figure 3.24 a. Model for the Channel - Consolidation Circuit - Load System in the Resistive Load Regime

b. Same System in State 1

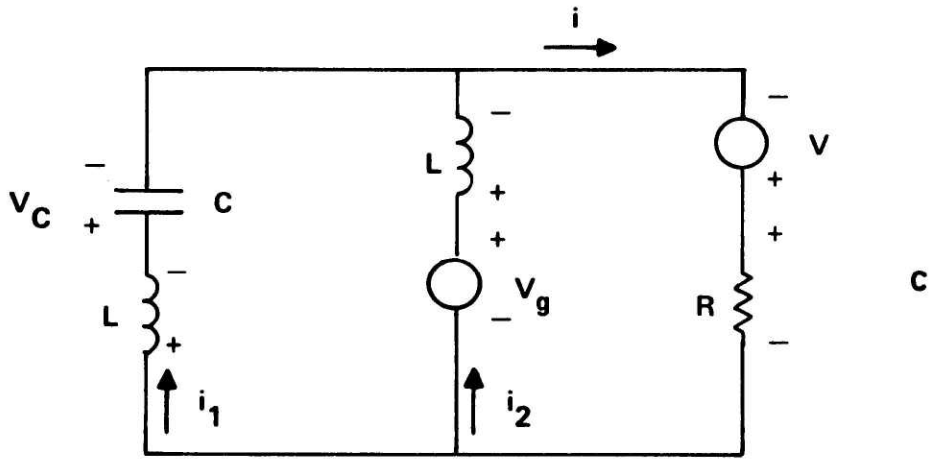

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Figure 3.24c Same System in State 2

$$V - iR - L\frac{di_1}{dt} = 0$$

$$V - iR + V_g - L\frac{di_2}{dt} + V_c = 0$$

$$i_2 = -C\frac{dV_c}{dt}.$$

Non-dimensionalize all current quantities by $\frac{V}{R}$, all voltage quantities by V, time by $\sqrt{LC}$, and add tildes to the resultant non-dimensionalized quantities.

Define $A = \frac{V_g}{V}$

$$B = R\sqrt{\frac{C}{L}},$$

and use "prime" to stand for time derivative, we have the following set of linear, first order differential equations:

$$\tilde{i}_1' = B(-\tilde{i}_1 - \tilde{i}_2 + 1)$$
$$\tilde{i}_2' = B(-\tilde{i}_1 - \tilde{i}_2 + \tilde{V}_c + A + 1)$$
$$\tilde{V}_c' = 1/B(-\tilde{i}_2)$$

State 2 (Figure 3.24c)

A treatment similar to the one given to the circuit in State 1 yields the following set of equations:

$$\tilde{i}_1' = B(-\tilde{i}_1 - \tilde{i}_2 - \tilde{V}_c + 1)$$
$$\tilde{i}_2' = B(-\tilde{i}_1 - \tilde{i}_2 + A + 1)$$
$$\tilde{V}_c' = 1/B(\tilde{i}_1)$$

A computer program (not included in the thesis) was written to solve these two sets of linear first order differential equations using the Runge Kutta routine. Again the method of assumed states was used. The program

went through a loop many, many times to bring the circuit to steady state. From the computer printout (again not shown), a performance map was constructed and shown in Figure 3.25.

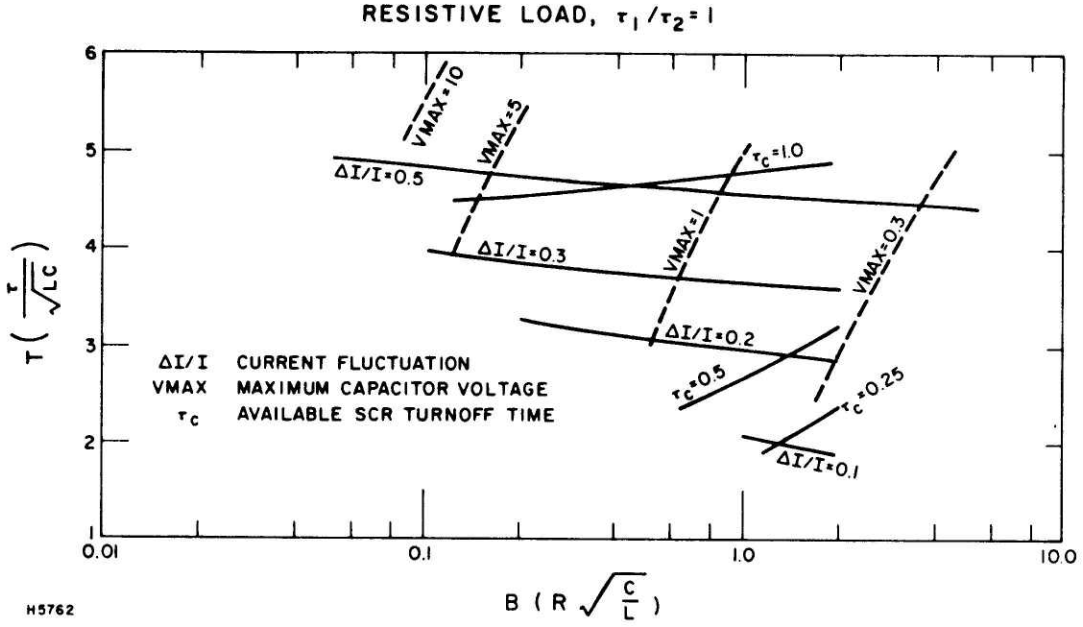


Figure 3.25 Performance Map for System in Resistive Load Regime, $\tau_1/\tau_2 = 1$

Chapter 4 Experimentation

A. Bench-Top Experiment

A bench-top experiment was set up to demonstrate the validity of the consolidation concept presented in this thesis.

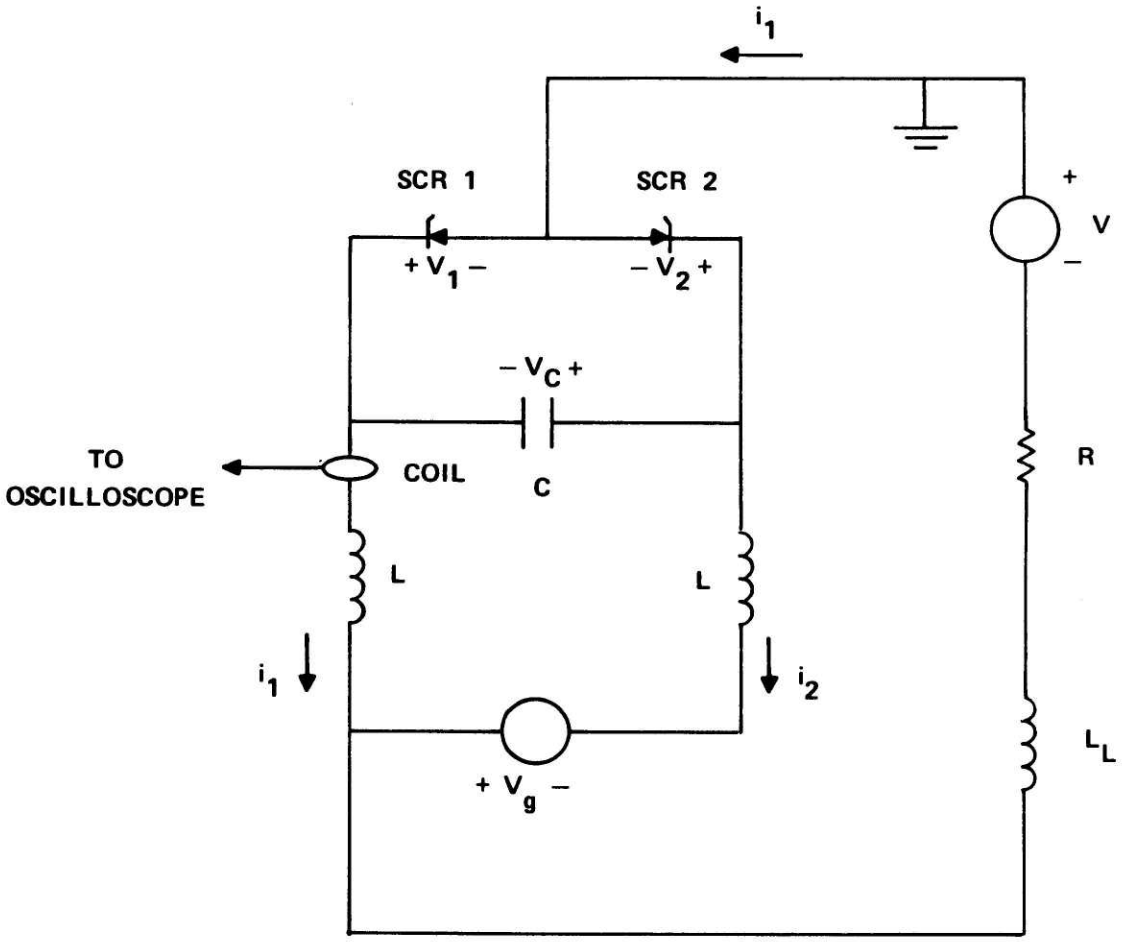
A. 1 The Circuit

Figure 4. 1 shows a very simple circuit built to verify the consolidation concept and also aid us later on in designing the consolidation circuit. Here, simulation of the interelectrode gap voltage V_g was achieved using a power supply and the simulated load current was generated by another power supply, V. The choice of L and C was guided by the results of Chapter 3. For reasonable values of current fluctuation, the $\sqrt{LC}$ time constant should be large compared to the period of SCR commutation, T.

A. 2 Starting

Circuit was started by first gating SCR1 on. When the power (V) came on, it drive a current through SCR1. The gap voltage power supply V_g was then turned on. This gap voltage (or a large portion of it) appeared across SCR2 favorably and when SCR2 got its gate signal it started conducting and the whole circuit started commutating.

The circuit was test started using different values of SCR commutation frequency. It was found that the circuit got more and more difficult to start as the commutation frequency got higher and higher. (By difficult to start, I mean that the circuit may start two out of four



V	=	160 volts	L	=	10 MH
R	=	32 ohms	C	=	31 μF
V_g	=	7 volts	$\sqrt{LC}$	=	550 μsec

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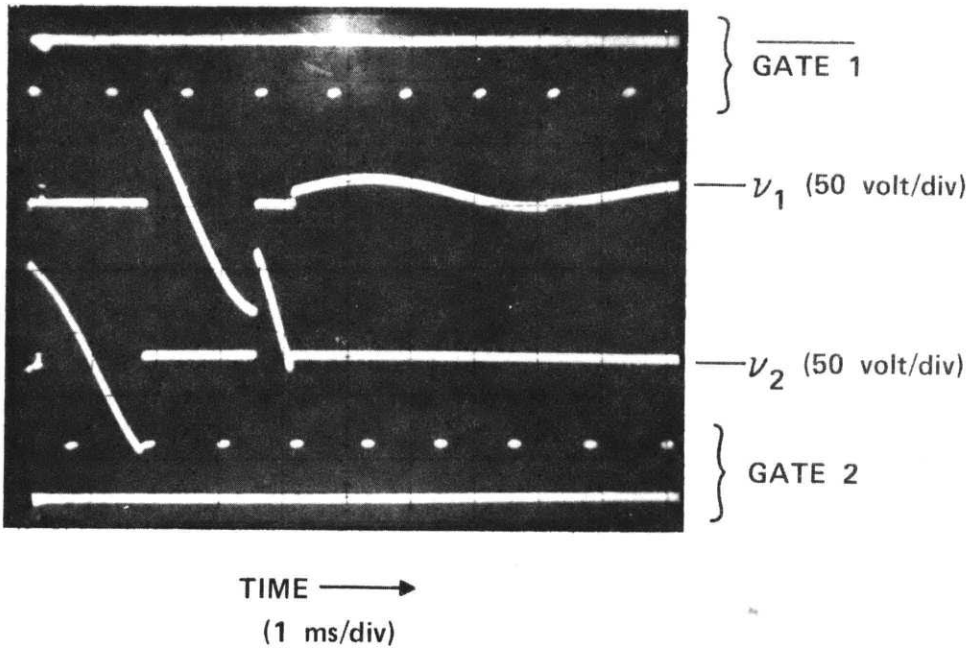
Figure 4.1 Circuit Configuration in the Bench-Top Experiment

times.) The pulse rate is controlled by the SCR drive which is independent of the dynamic response of the circuit elements. The rate of change of voltage in the capacitor is controlled by the amount of inductance (L) and capacitance (C). Hence, it is possible that at high frequency f, a gate signal arrives before a sufficient voltage in the capacitor is built up for sustaining commutation. When the circuit did not start; typically what happened was that one of the SCRs failed to commutate and current all flowed into the other SCR. Figure 4.2 shows a typical case when the circuit failed to start. Gate 2 and $\overline{\text{gate 1}}$ are the gate signal and inverse of the gate signal that drove SCR2 and SCR1 respectively. V_1 and V_2 are the voltages across SCR1 and SCR2 respectively as defined in Figure 4.1. It is seen from Figure 4.2 that the voltages sometimes missed the gate signal, that is, it did not have the right polarity when the gate signal arrived. At the arrival of the fourth gate pulse (of gate 2), the bias voltage across SCR2 was very small. Equivalently, the voltage across the capacitor was very small. This small voltage turned SCR2 on and turned SCR1 off. However, the gap voltage V_g was large compared to V_c and started charging the capacitor to favor SCR2's conduction.
As a result, SCR1 never got a chance to conduct anymore.

A.3 Measurements and Observations

Once the circuit is commutating properly, its behavior resembles rather closely what the analytical model described in Chapter 3 predicts. Figure 4.3 shows a typical current and voltage waveform along with the gate drives. The notations used here is the same as in Figure 4.2,



(TRIGGERED OFF v_2 ON A POSITIVE SLOPE)

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Figure 4.2 Starting Transient When the Circuit Fails to Commutate

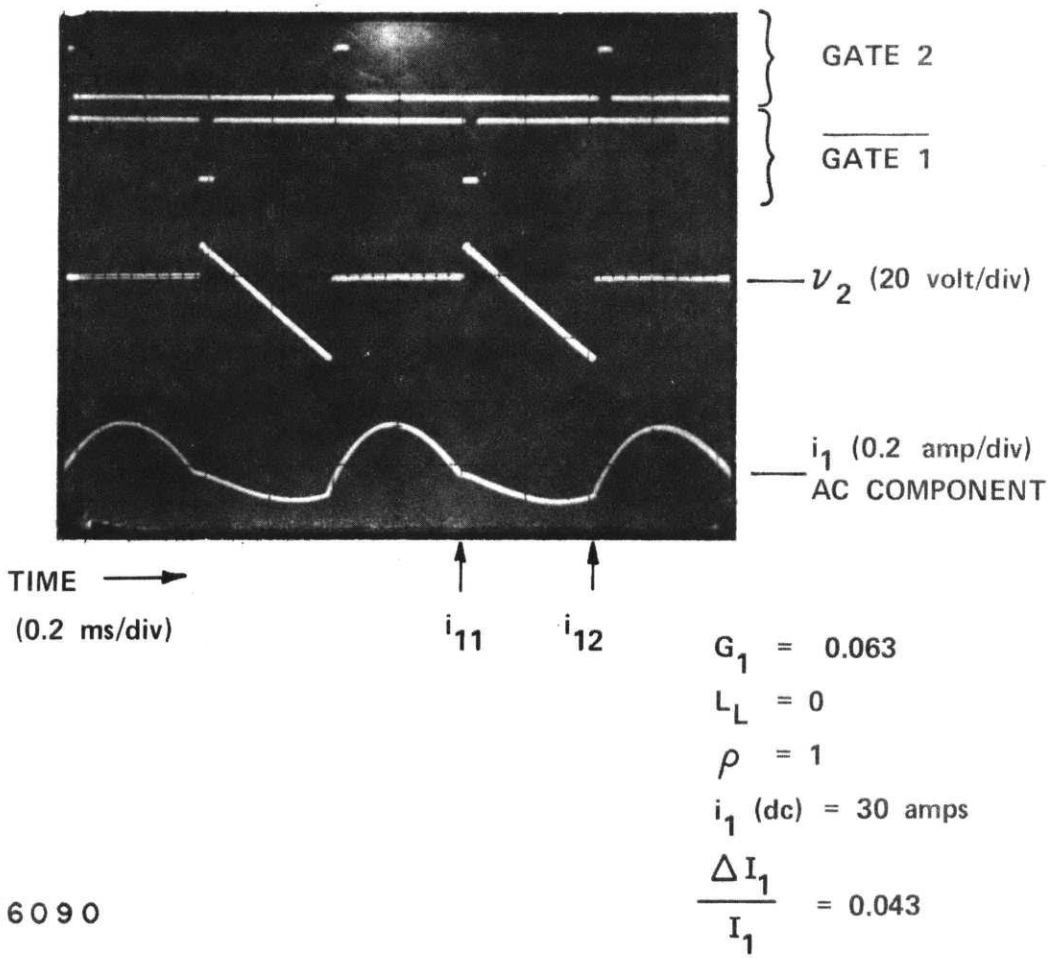


Figure 4.3 Current and Voltage Waveforms of the Bench-Top Circuit

except i_1 is the ac component of the current i_1 in Figure 4.1. Several observations can be made as follows:

i. i_{11}, value of i_1 when SCR1 just begins to conduct, is not equal to i_{12}, value of i_1 when SCR2 just begins to conduct, contradicting the prediction of the analytic model. They are not very much off though. From Figure 4.3, $i_{11} - i_{12} \cong 0.067$ amps. Since the dc component of i_1 (I_1) equals 3 amps, the percentage difference is equal to 2.2.

ii. It was verified that current distribution between the two leads I_1 and I_2 can be varied by varying $\rho = \frac{T_1}{T_2}$. To close approximation, $\frac{I_1}{I_2} = \rho$ where I_1 and I_2 are the time averages of i_1 and i_2, currents in the two leads.

iii. Figure 4.3 is obtained for load inductance $L_L = 0$, in which case, $\frac{\Delta I_1}{I_1} = 0.043$. As L_L was increased to 150 millihenrys, i_1 became more symmetrical about its mean value I_1 and $\frac{\Delta I_1}{I_1}$ reduced to 0.032. i_{11} and i_{12} got a little bit closer to each other. The current waveform did not change when L_L was increased from 100 mH to 200 mH.

iv. Figures 4.4 and 4.5 are comparisons between the results of the bench-top experiment and the predictions of the analytic model. The three data points were obtained for three different values of the SCR commutating frequency.

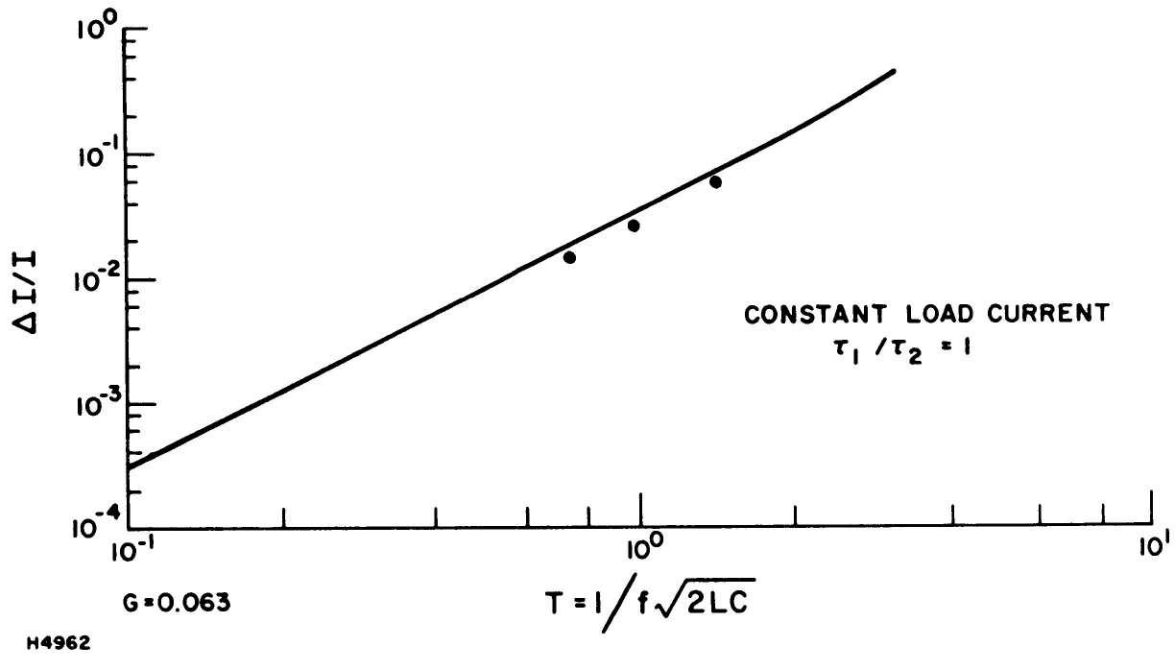


Figure 4.4 ΔI/I vs T, Period of Commutation. A comparison of experimental results (dots) with values predicted by analytic model (line).

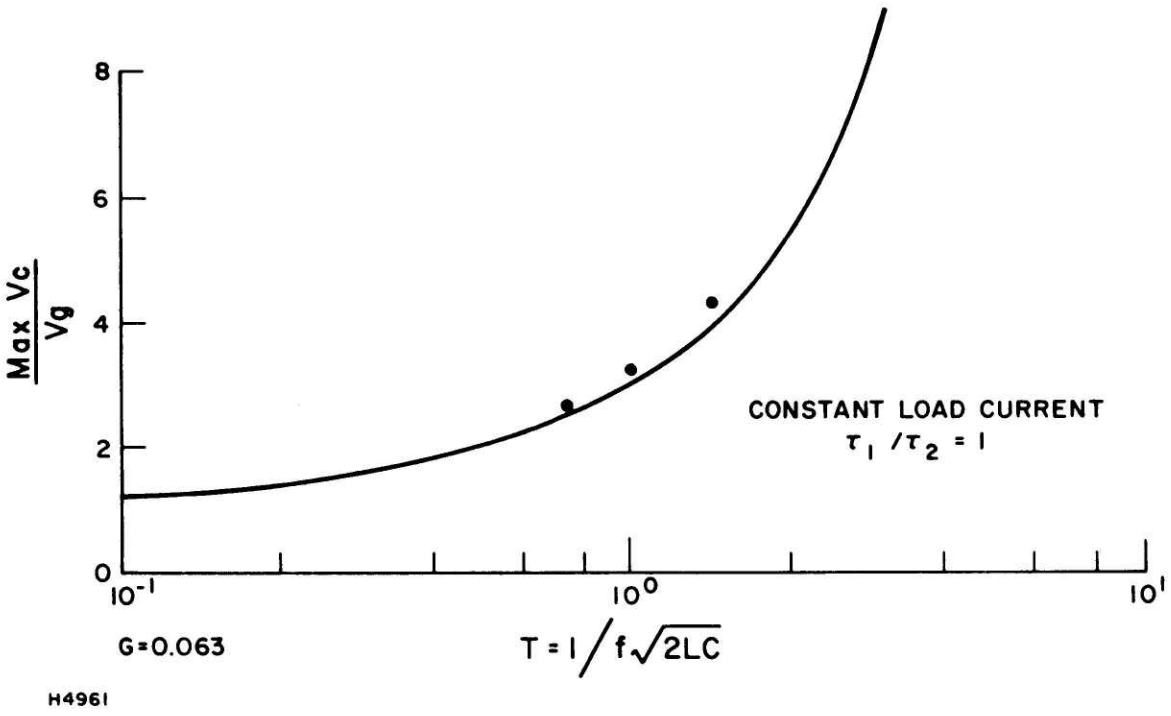


Figure 4.5 V_{MAX} vs T. A comparison of experimental results (dots) with values predicted by analytic model (line).

v. Figure 4.6 shows an oscillograms of the ac component of the total load current I. The fluctuation in I is less than 1% so, to good approximation, the circuit can be regarded as operating in the constant current regime.

vi. The mean value capacitor voltage V_c is equal to the negative of the gap voltage, as predicted. (The dc line of V_c is not shown).

vii. Even though the circuit can only be started for relatively low values of the commutation frequency f, once started however, f can be increased to give better circuit performance.

B. Two-Level Four-Electrode Consolidation Circuit

The results of the bench-top experiment are favorable and suggest further investigation. To get a feeling for the real operation while staying away from much complexity at this early stage, a two-level circuit was constructed to consolidate four electrode pairs. This circuit was first tested under laboratory simulated conditions. The complete set up is as shown in Figure 4.7. The testing and results are described in this section. The final test runs in the MHD generator are described in Section C.

B.1 Circuit Configuration

The two parts of the circuit - anode circuit and cathode circuit - were first tested separately. The anode circuit is the half that is connected to the anodes of the channel and the cathode circuit is the half connected

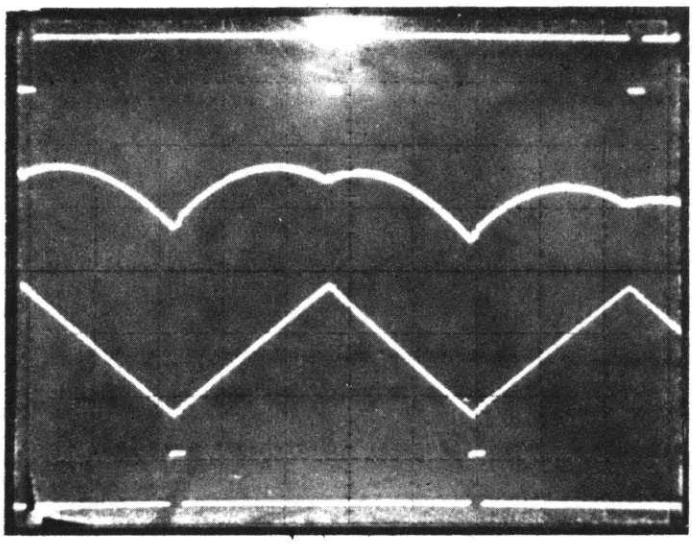


Figure 4.6 Load Current and Capacitor Voltage Waveforms of the Bench-Top Circuit

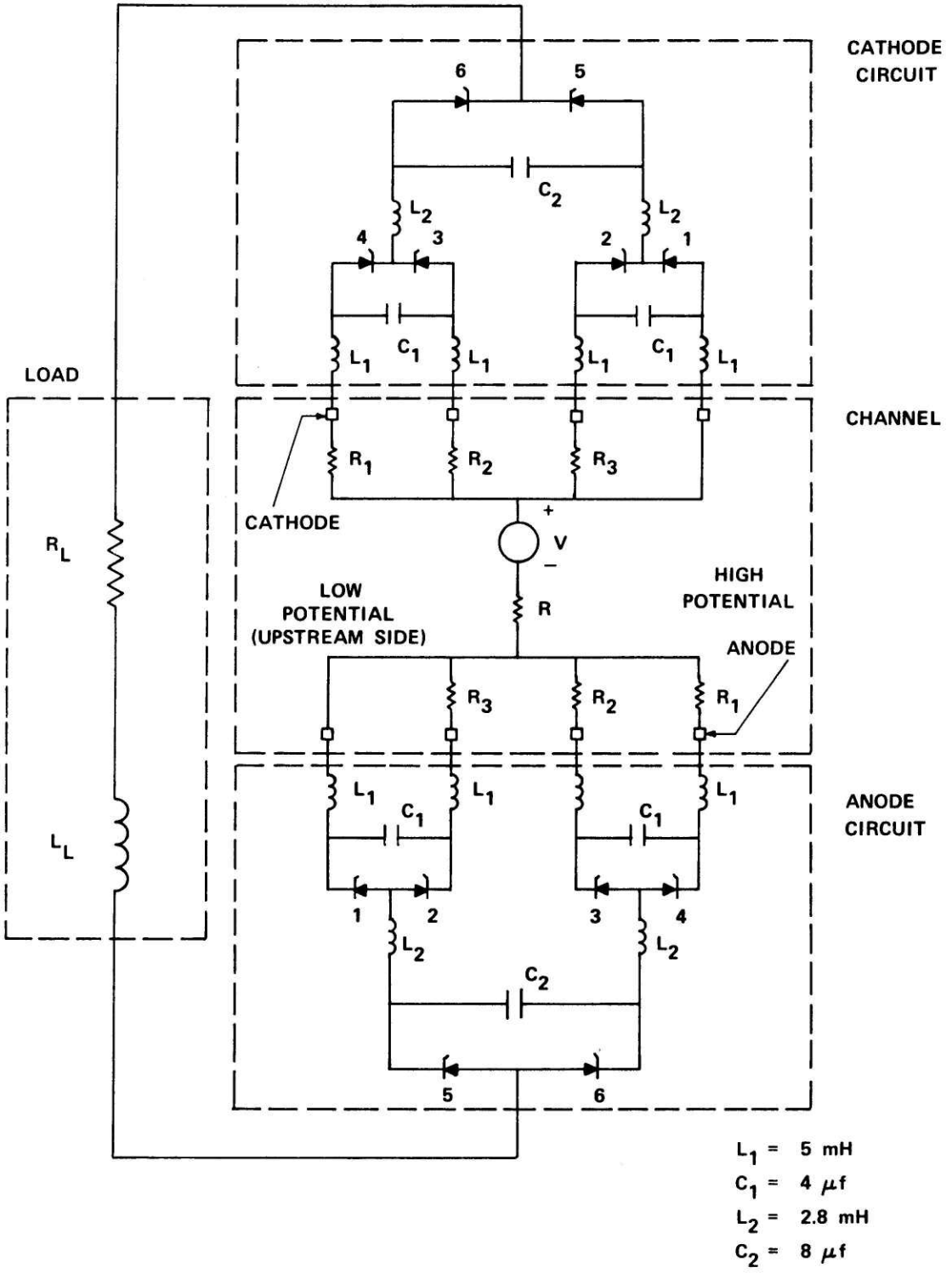


Figure 4.7 Two-Level Four Electrode Consolidation Circuit Connected to Simulated Channel and Load

to the cathodes. The anode circuit with the circuitry simulating the channel is shown in Figure 4.8. The values of the circuit elements were determined by going through a process similar to the following:

i. Values of the gap voltage V_g and current per electrode i is obtained for the channel which the consolidation circuit is designed for.

ii. Refer to Figure 4. 8. Twice as much current flow through R_2 and three times as much current flow through R_1 as there is through R_3. Therefore, to get a uniform gap voltage throughout, we want

$$R_3 : R_2 : R_1 = 3 : 1\frac{1}{2} : 1.$$

Moreover, with the information in (i) above,

$$R_3 = \frac{V_g}{i} .$$

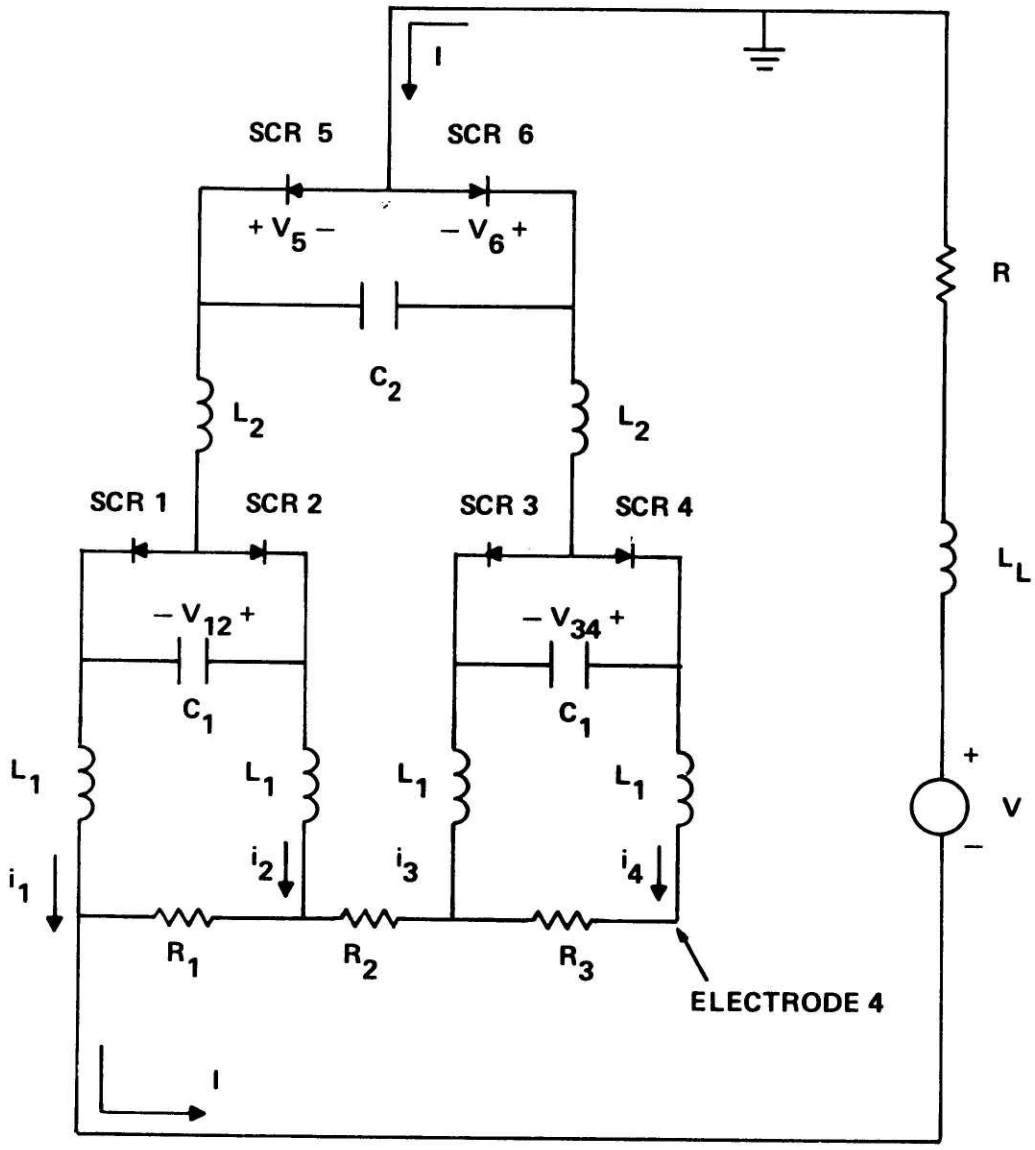
iii. A value for the SCR commutation frequency f is chosen.

iv. Pick an operating point in the performance map which is repeated in Figure 4. 9. This can be guided by certain criteria that the circuit has to satisfy, for example, maximum electrode current fluctuation tolerable. Once an operating point is picked, the values of G and T are specified.

Since
$$G = \frac{V_g}{I}\sqrt{\frac{C}{2L}}$$

$$T = \frac{1}{f\sqrt{2LC}}$$

we can solve for L and C in terms of G and T,



L_1 = 5 mh		R = 6 ohms	
C_1 = 4 mf		R_1 = 1 ohm	
L_2 = 2.8 mh		R_2 = 1.5 ohms	
C_2 = 8 mf		R_3 = 3 ohms	

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Figure 4.8 Simulated Anode Circuit - Channel - Load System

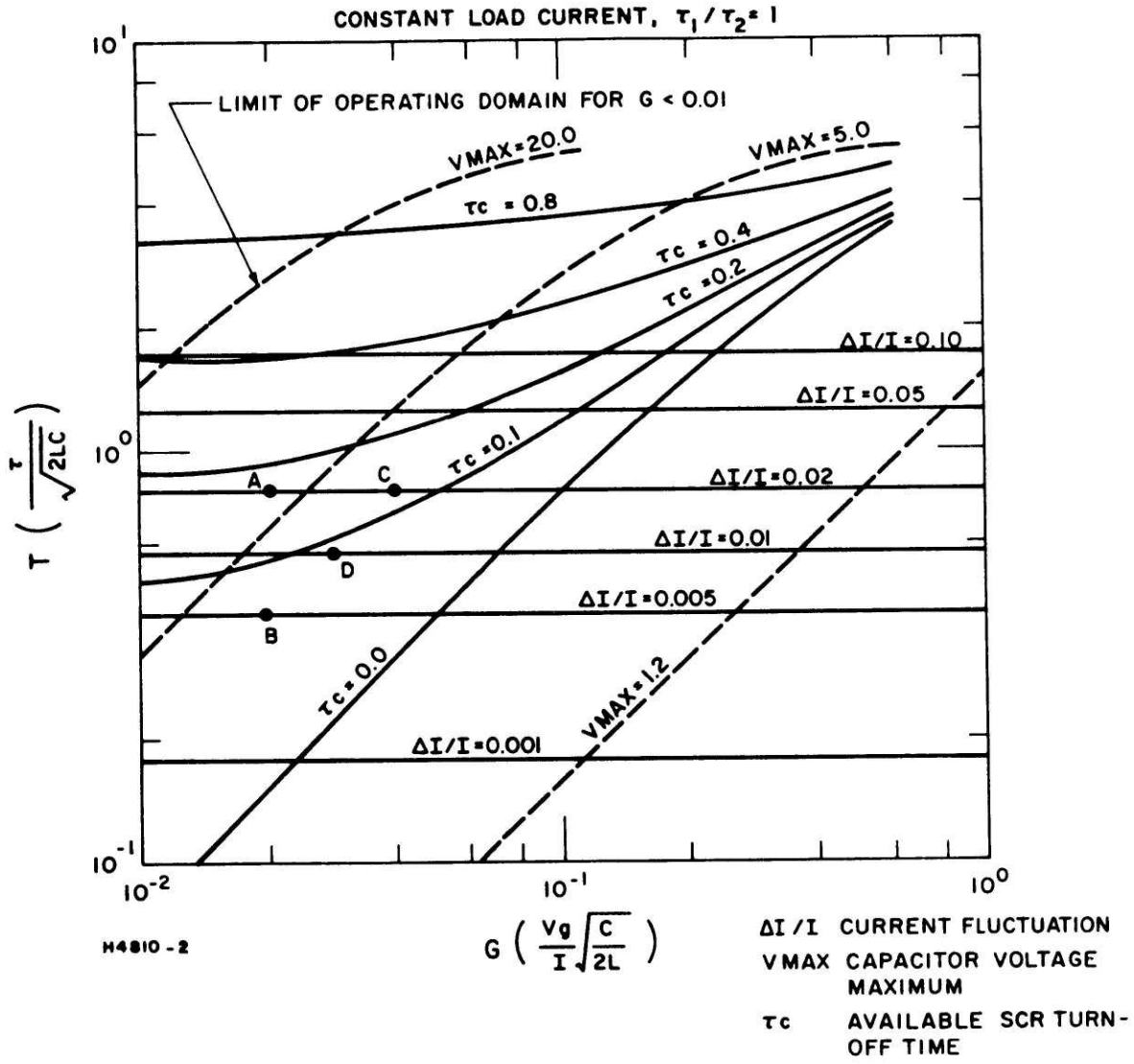


Figure 4.9 Performance Map for Constant Load Current, $\tau_1/\tau_2 = 1$

$$\sqrt{\frac{C}{L}} = \sqrt{2}\, G \frac{I}{V_g}$$

$$\sqrt{LC} = \frac{1}{\sqrt{2}\, f T},$$

and

$$C = \frac{G I}{f T V_g}$$

$$L = \frac{V_g}{2 f T G I}.$$

Thus, for a channel with V_g = 20 volts

$$I = 4 \times i = 80 \text{ A.},$$

if operating point A is picked (see Figure 4.9) corresponding to G = 0.02

T = 0.8

then C = 20 μF

F = 1.5 mH for a commutation frequency f of 5 KHz.

After obtaining the values of L and C, a check to see whether the SCRs have enough time to turn-off is done. τ_c for point A is 0.17, thus available turn-off time $= \tau_c \sqrt{2LC}$

$= 42$ μsec

for the values of L and C above. If the time it takes for the SCRs used to turn-off is over 42 μsec, another operating point has to be picked.

At the second stage of the consolidation circuit, both the gap voltage V_g and total current I double leaving G unchanged. So if the commutation frequency in the second stage is the same as the first, the same operating point yeilds the same values for L and C. (This is true for even higher up stages in a multi-stage consolidation circuit). Using

the same values for L and C in every consolidation stage is good except that the value of the maximum capacitor voltage is doubled in the second stage and quadrupled in the third stage and so on. To withstand the higher voltage (and also higher current), higher power SCRs have to be used.

Another design approach is to operate at different operating points at different stages. Thus, we can double the value of C at the second stage. Then we can use SCRs of higher current rating but the same voltage rating. For this value of C, we can double L which brings the operating point to point B in Figure 4. 9 since this leaves the value of G unchanged and reduce the value of T by a factor of 2. On the other hand, we can reduce L by a factor of 2 which brings the operating point to point C. We can leave L unchanged which brings the operating point to point D. Any combinations of Ls and Cs are potentially possible. The effect will be to move the operating point on the T-G plane. At different operating points the circuit performs differently.

B. 2 Starting

In the configuration shown in Figure 4. 8, many different procedures can be used to start the circuit commutating. They all are, however, a modification of one of the following two procedures:

Procedure ONE: turn SCR2, SCR4, SCR6 on

turn power on (current into electrode 4)

turn SCR5 on (SCR5 and SCR6 commutates; current into electrode 2)

turn SCR3 on (SCR3 and SCR4 commutates; current into electrode 3)

turn SCR1 on (SCR1 and SCR2 commutates; current into electrode 1)

Procedure TWO: turn SCR3, SCR4, SCR6 on

turn power on (SCR3 and SCR4 commutates; current into electrodes 3 and 4)

turn SCR1, SCR2 on

turn SCR5 on (SCR5 and SCR6 commutates; SCR1 and SCR2 commutates; current into electrodes 1 and 2)

Procedure ONE is a little bit more reliable in the probability of starting the circuit. Procedure TWO has the advantage that current starts flowing into two electrodes at once. The probability of damaging an electrode resulting from excessive current is reduced.

It is noticed that as the load inductance (L_L in Figure 4. 8) becomes large, it takes very high voltage to start the circuit. This is a result of finite holding current in the SCRs. Holding current is the value of forward anode current which allows the SCR to remain in conduction. Below this value the device will return to a forward block state at the prescribed gate conditions. If after the gate pulse is over, the current in the SCR still has not exceeded the holding current, the SCR will drop out of conduction and the consolidation circuit will never start.

Refer to Figure 4. 8, to start current flowing in electrode 4 is equivalent to energizing a series RL circuit with a step voltage. The current is then given by

$$i = \frac{V_o}{R} \left(1 - e^{-\frac{R}{L} t}\right)$$

i will be equal to the holding current if

V_o is the lowest voltage to start the circuit

R is the sum total resistance in the circuit loop

L is the sum total inductance in the circuit loop

and t is the duration of the gate pulse.

Note that the holding current i is for that SCR which has the highest holding current if there is morethan one SCR in the loop.

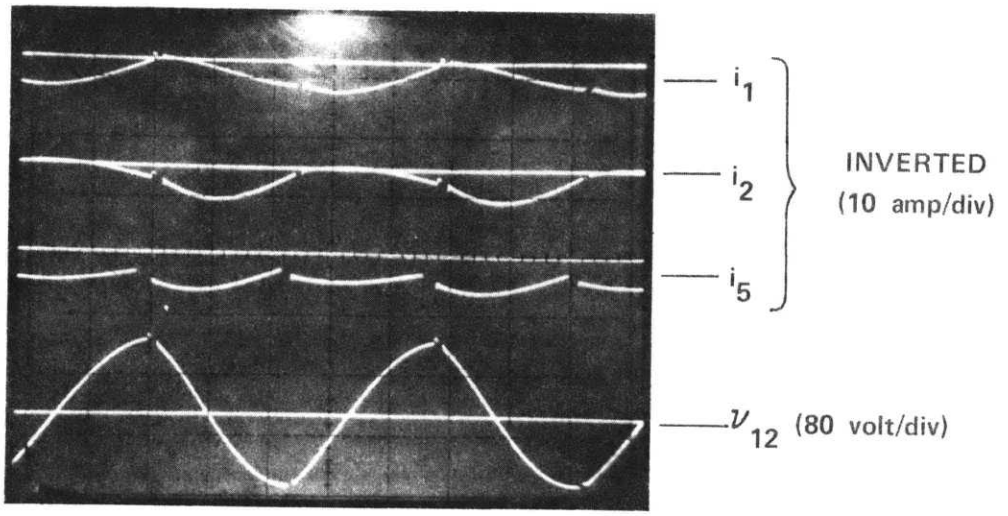
B. 3 Measurements and Observations

Figure 4. 10 shows some current and voltage waveforms of the circuit operating at a relatively low frequency of one kilohertz. The horizontal lines in Figure 4. 9 (a) are the ground lines for the respective waveforms. The scales for current measurements are positive down. At this low commutating frequency, currents i_1 and i_2 actually go negative in some instances. The maximum voltage across SCR1 or SCR2 is given by the peak value of the waveform of V_{12} and is about 100 volts when the current in each electrode is equal to 4 amps and gap voltage equals 12 volts.

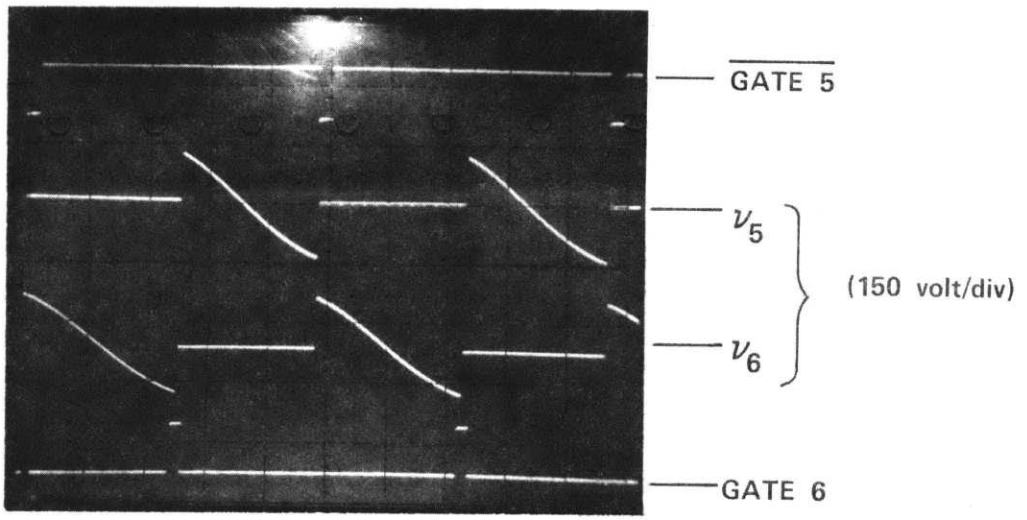
From Figure 4. 11, we see the following equation easily:

$$V_{12} + L \frac{di_1}{dt} = V_g + L \frac{di_2}{dt}.$$

For a positive constant V_g, when V_{12} changes sign, i_1 and i_2 change their slopes to maintain the above equality. This can be seen very clearly in Figure 4. 10 (a).



(A)



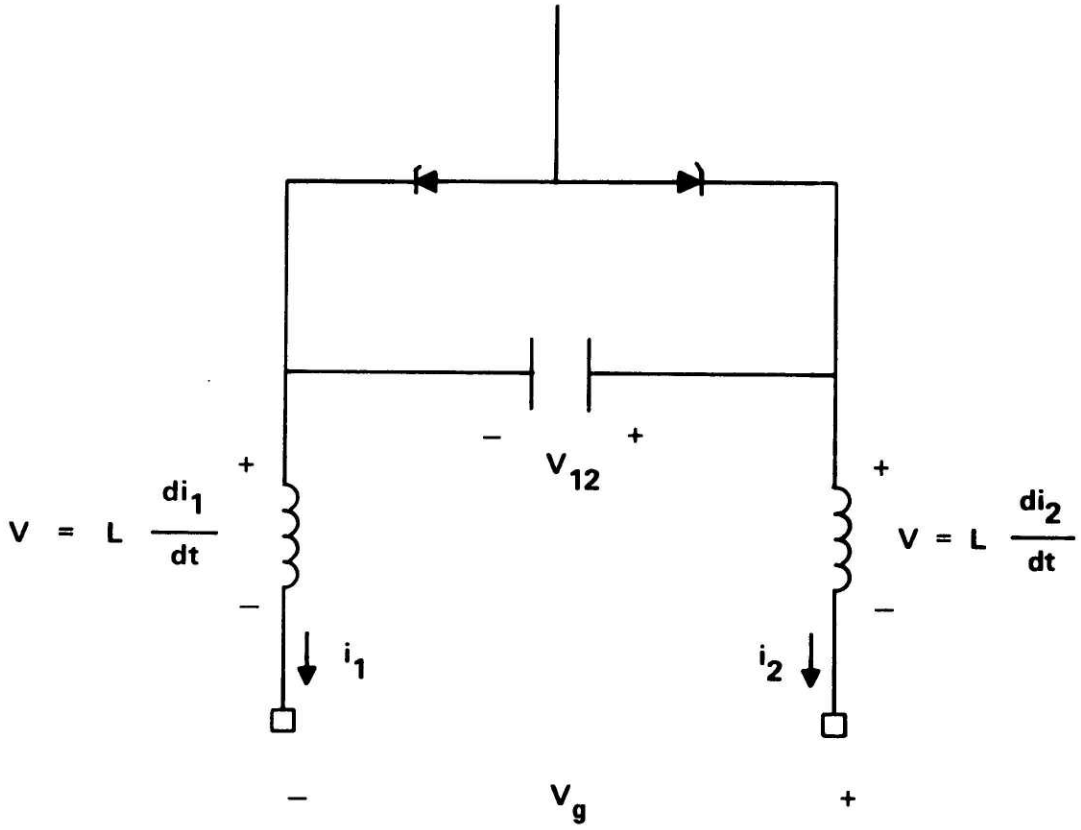
(B)

ρ = 1

f = 1 KHz

H6088

Figure 4.10 Current and Voltage Waveforms for the Anode Circuit System of Figure 4.8



$$V_{12} + L\frac{di_1}{dt} = V_g + L\frac{di_2}{dt}$$

H6097

Figure 4.11 Basic Two-Electrode Consolidation Circuit

Current controllability among the electrodes by varying the relative conducting periods of the SCRs was demonstrated. The analysis in Chapter 3 shows that for the circuit in Figure 4.8 operating in the constant load current regime,

$$\frac{I_1}{I_2} = \frac{\tau_1}{\tau_2}$$

where I_1 and I_2 are respectively the time averages of i_1 and i_2, and τ_1 and τ_2 are respectively the conducting time of SCR1 and SCR2 in one cycle. This equation implies that

$$\frac{I_2 - I_1}{I_2 + I_1} = \frac{\tau_2 - \tau_1}{\tau_2 + \tau_1}$$

and since $\tau_1 + \tau_2 = \tau$ where τ is the period of SCR commutation,

$$\frac{I_2 - I_1}{I_2 + I_1} = 1 - \frac{2\tau_1}{\tau} .$$

This is plotted in Figure 4.12 for a commutating frequency of 2.5 KHz. For comparison, data points actually observed are plotted on the same figure. It is seen that they agree very closely to each other.

B.4 The Complete Circuit

The cathode circuit, which is similar in its details to the anode circuit except for the polarity of the SCRs, was tested and its operation verified. The two half-circuits were then joined together as shown in

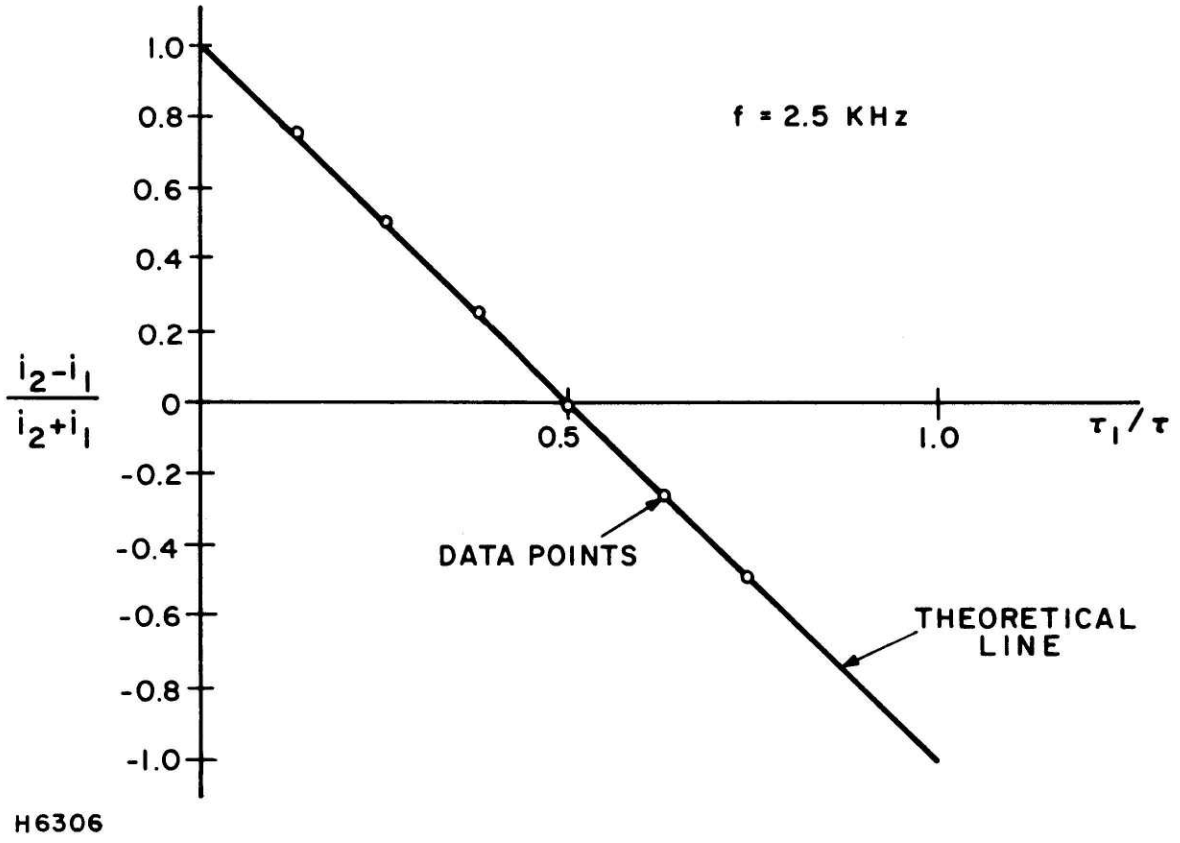


Figure 4.12 Verification of the Relationship $I_1/I_2 = \tau_1/\tau_2$

Figure 4.7 for an MHD channel simulation test. The values of R_1, R_2, and R_3 are chosen such that the simulated gap voltages are uniform for equal current in each electrode.

B.4.1 Starting

A flow of current to charge the commutating capacitors with the proper polarity has to be maintained prior to commutation. Since current build up in an MHD channel is relatively fast (few seconds), should commutation be delayed, the MHD generator will overload the electrode through which this "charging current" passes causing possible damage. For this reason, a starting circuit was built which senses the level of the charging current and sequentially fires the SCRs to start commutation according to the starting procedures described in Section B.2.

B.4.2 Measurements and Observations

Current distribution between the electrodes is not a function of the total current level. Once the currents in the four electrodes are balanced, the load current level can be raised or lowered without affecting the current distribution. Current fluctuations of individual electrodes however, have a slight dependence on the total current level as shown in Figure 4.13. I is the total current in amps. $\frac{\Delta i}{i}$ is the maximum current deviation from its mean value divided by its mean value.

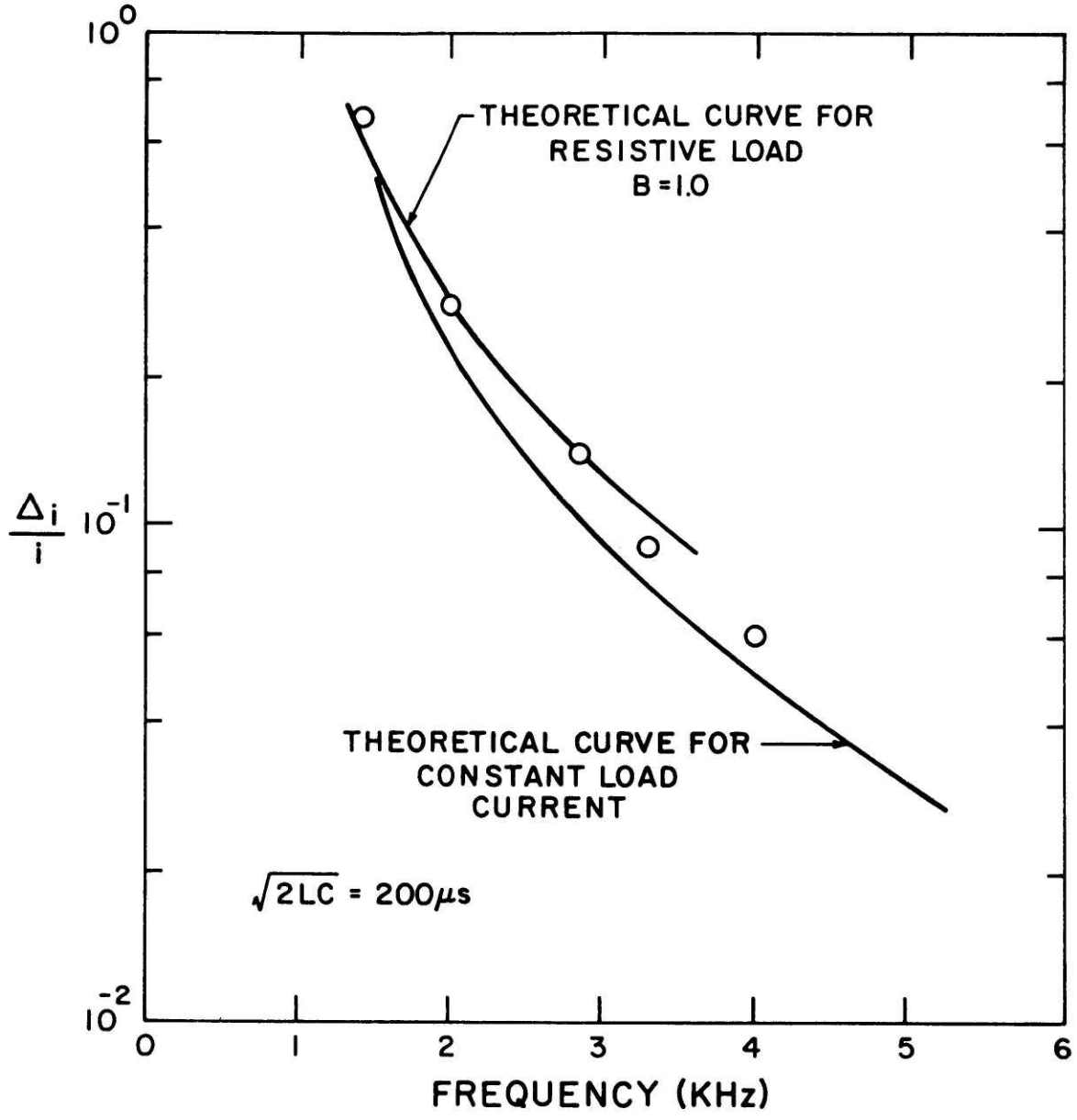
Electrode current fluctuation varies inversely with the commutation frequency. In Figure 4.14, the theoretical curves of this dependency is displayed for the cases of constant load current and purely resistive load. The data points obtained for the circuit are displayed as

I(AMPS)	5	10	15	20
$\frac{\Delta i}{i}$ ANODE 1	0.42	0.41	0.46	0.49
$\frac{\Delta i}{i}$ ANODE 4	0.4	0.34	0.35	0.30

f = 2 KHERTZ

H6093

Figure 4.13 Dependency of Electrode Current Fluctuation on Total Current Level I



H6101

Figure 4.14 Δi/i vs Commutation Frequency. A comparison between theoretical predictions and experimental results.

circles.

C. Channel Testing

The two-level four-electrode consolidation circuit as shown in Figure 4.7 was tested on the AVCO Mark VII MHD generator. The circuit was connected up to electrode pairs 28 through 31. The results are reported in this section.

C.1 Starting

The two procedures as described in Section B.2 were able to start the circuit commutating. However, when gap voltage non-uniformity developed (the gap voltage sometimes went negative), the circuit did not always start commutating.

The circuit was test started with all the SCRs left on. In the absense of gap voltage non-uniformity, the circuit started beautifully. This seemed to be the best starting procedure.

C.2 Measurements and Observations

Some current and voltage waveforms are shown in Figure 4.15. The notations used are the same as in Figure 4.8. Once agains, the scales for current measurements are positive down.

Current controllability was again demonstrated by varying the relative conducting times of SCRs. The relationship

$$\frac{I_1}{I_2} = \frac{\tau_1}{\tau_2}$$

was again testified and the results shown in Figure 4.16. (Refer to

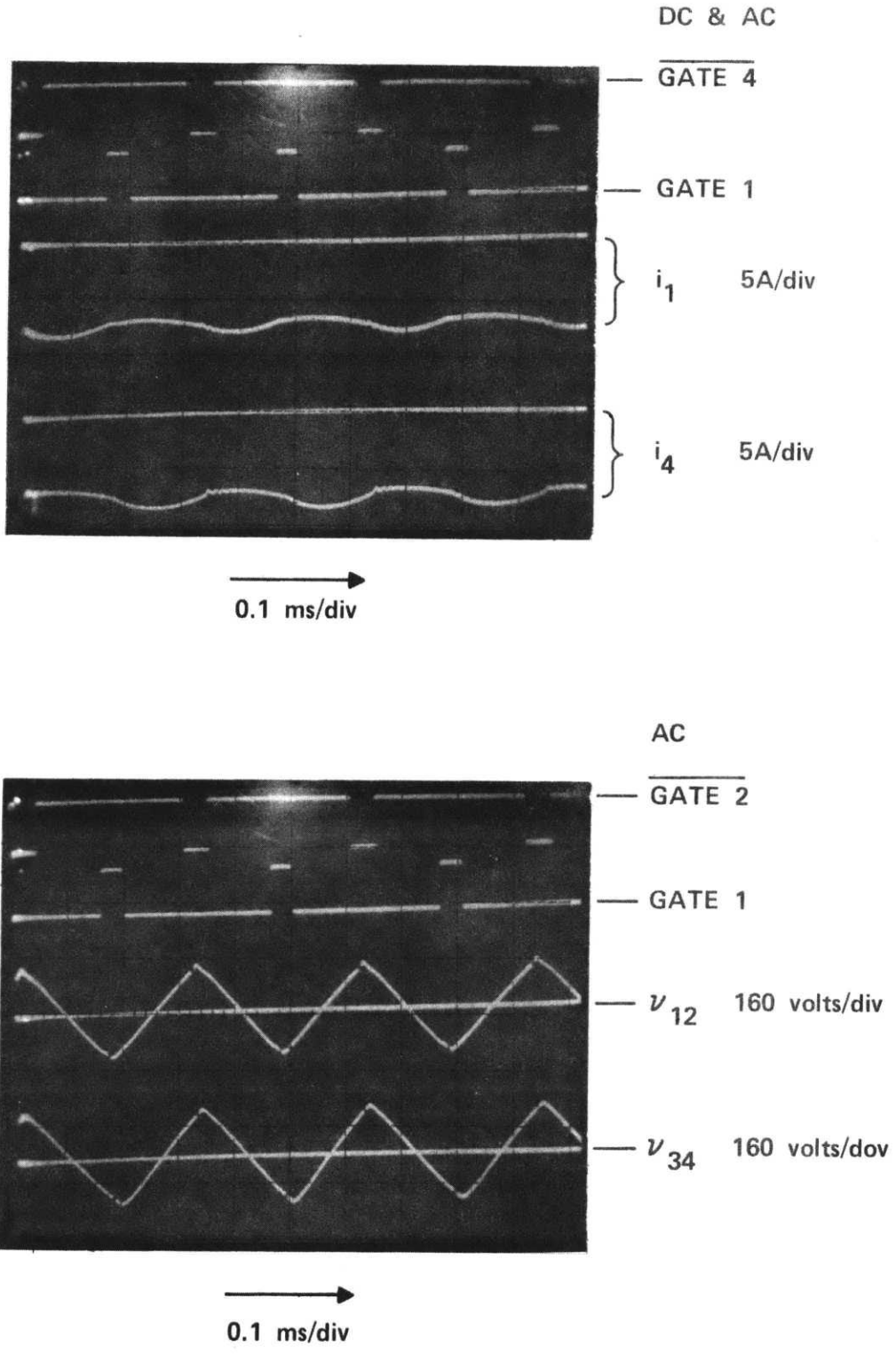


Figure 4.15 Current and Voltage Waveforms of the Consolidation Circuit When Testing on the Mark VII

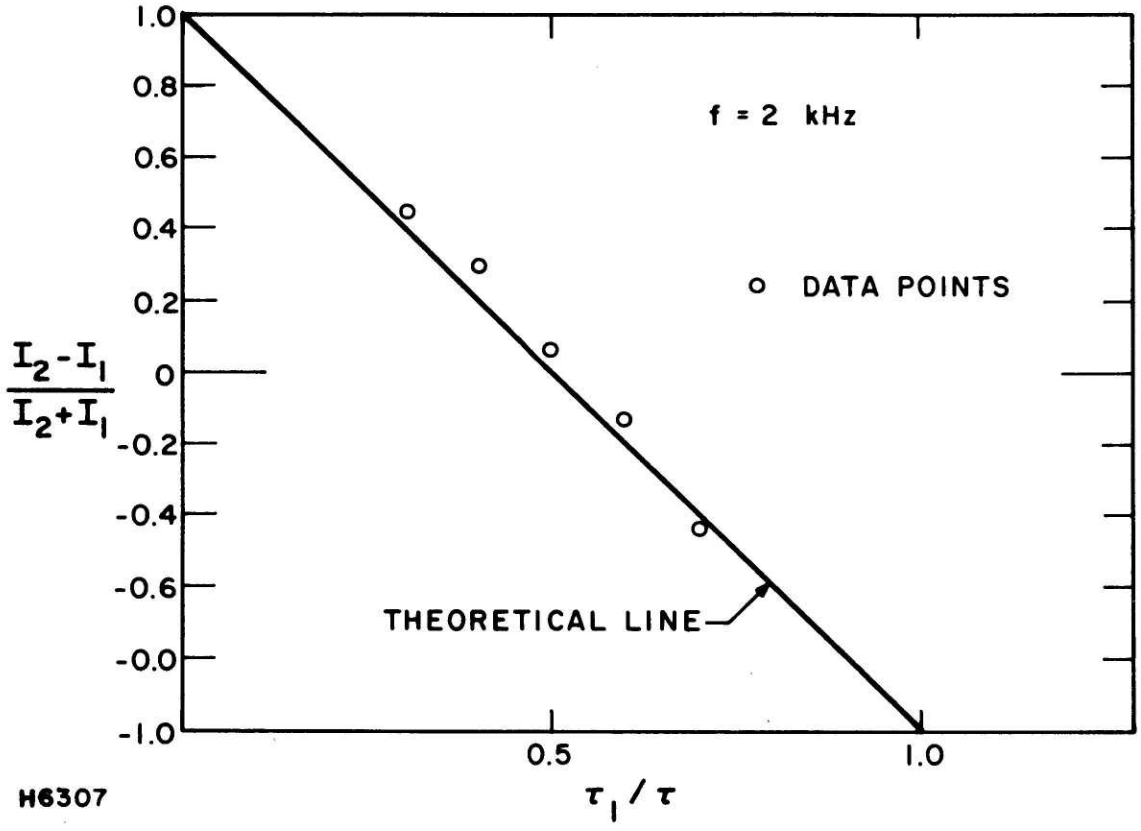


Figure 4.16 Verification of the Relationship $I_1/I_2 = \tau_1/\tau_2$ with Channel Results Obtained in the Test

Section B. 3 for detail discussion).

Lastly, current fluctuation for anode number 28 and anode number 31 as a function of SCR commutating frequency is plotted in Figure 4. 17. (Compare with Figure 4. 14).

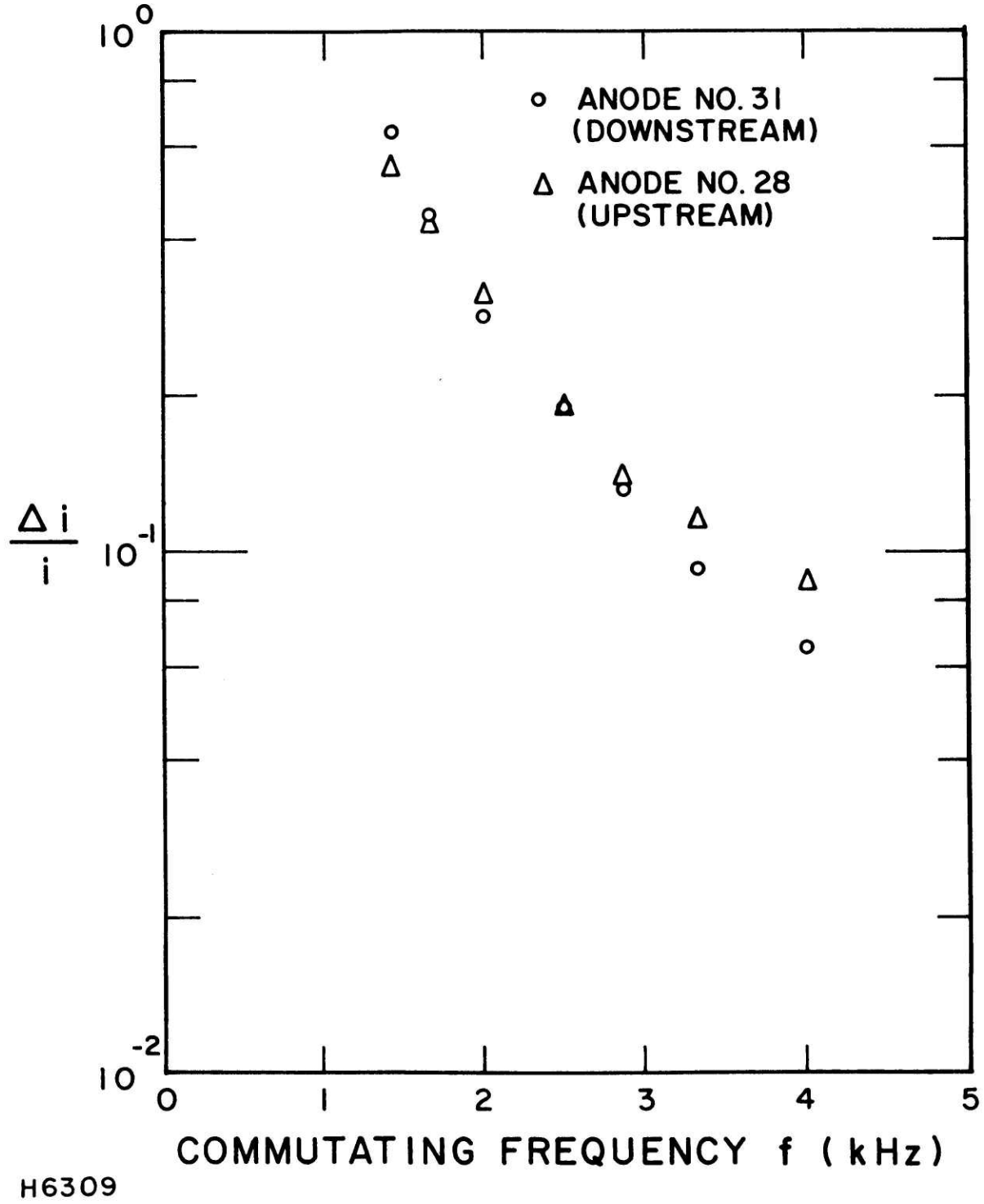


Figure 4.17 $\Delta i/i$ vs Commutation Frequency - Results of the Channel Test

Chapter 5 Design Considerations

A method for choosing the values of L and C for any particular consolidation application is outlined in Chapter 4 Section B. 1. With the insights gained, a systematic method to aid the design of the consolidation circuit is developed and is presented here.

The parameters of importance in an MHD channel from the point of view of consolidation is the nominal value of the interelectrode gap voltage V_g and the load current per electrode. A criterion may be set to limit the current fluctuation (amplitude, rms, etc.) $\frac{\Delta I}{I}$ for a particular application.

The design procedure outlined below is for one stage of consolidation involving two current leads out. Exactly the same procedure can be followed for the stages higher up. The design problem can be stated as to find the values and ratings of the inductors and capacitors, the commutation frequency, and the SCR ratings under the specified condition of gap voltage, current per electrode, and maximum tolerable electrode current fluctuation.

An example is used to demonstrate this design process. In this example, the two SCRs are assumed to have equal conducting periods. Assume the channel concerned has an interelectrode gap voltage of 20 volts and current per electrode equal to 20 amps. The total current in the circuit I_T is therefore 40 amps (two electrodes). The circuit is to be designed to have no more than 5% current fluctuation. Stated more explicitly with the notation used before,

$$V_g = 20\,V$$

$$I_T = 40\,A$$

$$\frac{\Delta I}{I} \leq 0.05$$

Referring to Section B. 1, Chapter 4, we can calculate:

$$G = \frac{V_g}{I_T}\sqrt{\frac{C}{2L}} \qquad (1)$$

$$T = \frac{1}{f\sqrt{2LC}} \qquad (2)$$

Step 1

From the results in Chapter 3 and 4, it can be concluded that current fluctuation $\frac{\Delta I}{I}$ is independent of G and depends only on T, the normalized period of commutation (or equivalently the commutation frequency). From the performance map (Figure 3.16), T = 1.25 for $\frac{\Delta I}{I} = 0.05$, and from Equation (2), $LC = \frac{1}{2\,(fT)^2}$. A reasonable frequency is then picked. This may be quided by experimental results. Later on, the effects of varying the frequency will be investigated. For the numerical demonstration here, 5 kilocycle is picked. Therefore, for

$$\frac{\Delta I}{I} = 0.05 \quad (T = 1.25)$$

and

$$f = 5 \times 10^3\ H_z$$

$$LC = 1.28 \times 10^{-8}\ sec^2.$$

This describes a curve in the LC plane. Any point falling on this curve satisfies the criterion that current fluctuation $\frac{\Delta I}{I} = 0.05$ for a

commutation frequency of 5 kilocycle. For the same driving frequency, any point to the right of this curve will result in $\frac{\Delta I}{I}$ less than 0.05. This is intuitive since any point to the right of this curve means either larger capacitance or inductance or both. Curves for $\frac{\Delta I}{I}$ = 0.015, 0.05, and 0.10 are plotted for commutation frequency f = 5 KHz in Figure 5.1. Therefore, to satisfy the requirement that the current fluctuation be no more than 5%, the operating point should be to the right of the $\frac{\Delta I}{I}$ = 0.05 curve for operation at 5 kilocycle.

Step 2

The procedure that follows locates points that result in the same maximum capacitor voltage.

From Equation (1) and (2), putting in the values for V_g and I_T,

$$C = \frac{2G}{fT} \tag{3}$$

$$L = \frac{1}{4f\,GT} \tag{4}$$

Referring back to Figure 3.16, having in mind that V_{MAX} is normalized to the gap voltage V_g, if one wants to draw a curve for maximum capacitor voltage equal to 600 volts, one looks for the curve $V_{MAX} = \frac{600}{20} = 30$. (Not shown in the figure.) Values of G and the corresponding values of T are then picked off from the curve. Equations (3) and (4) give us a pair of value for L and C for each pair of values of G and T for each frequency f. These LC pairs then describe a curve of constant maximum capacitor voltage for that particular frequency. For the same commutating frequency, any point to the right of this curve results in a smaller

maximum capacitor voltage and the reverse is true for points to the left. Curves for maximum capacitor voltage of 600 volts and 1200 volts are plotted for f = 5 KHz in Figure 5. 1.

Step 3

For proper operation, enough time has to be allowed for an SCR to turn-off before the voltage across it changes polarity. This so-called available turn-off time is only a function of f, the SCR commutation frequency, and V_g, the gap voltage. Since V_g is fixed, it is only a function of f. Therefore, a plot can be made for the available turn-off time versus commutation frequency. (To make the plot, some arbitrary values for L and C are picked. G and T as given in Equations (1) and (2) are then a function of commutation frequency f only. From Figure 3.16, a value of τ_c can be obtained for each value of f. The available turn-off time is then given by $\tau_c \sqrt{2LC}$.)

For a typical commercially available SCR, the maximum repetitive forward voltage is 600 volts and the turn-off time is 20 μsecs. The corresponding available turn-off time for a commutation frequency of 5 kilocycle is 50 μsecs, so there is no problem about turning off. Any value pairs of L and C falling to the right of the dashed curve therefore satisfy all the set criteria.

Step 4

Here, the effect of changing the commutation frequency is investigated.

First of all, as explained in Step 3 above, how high f can be

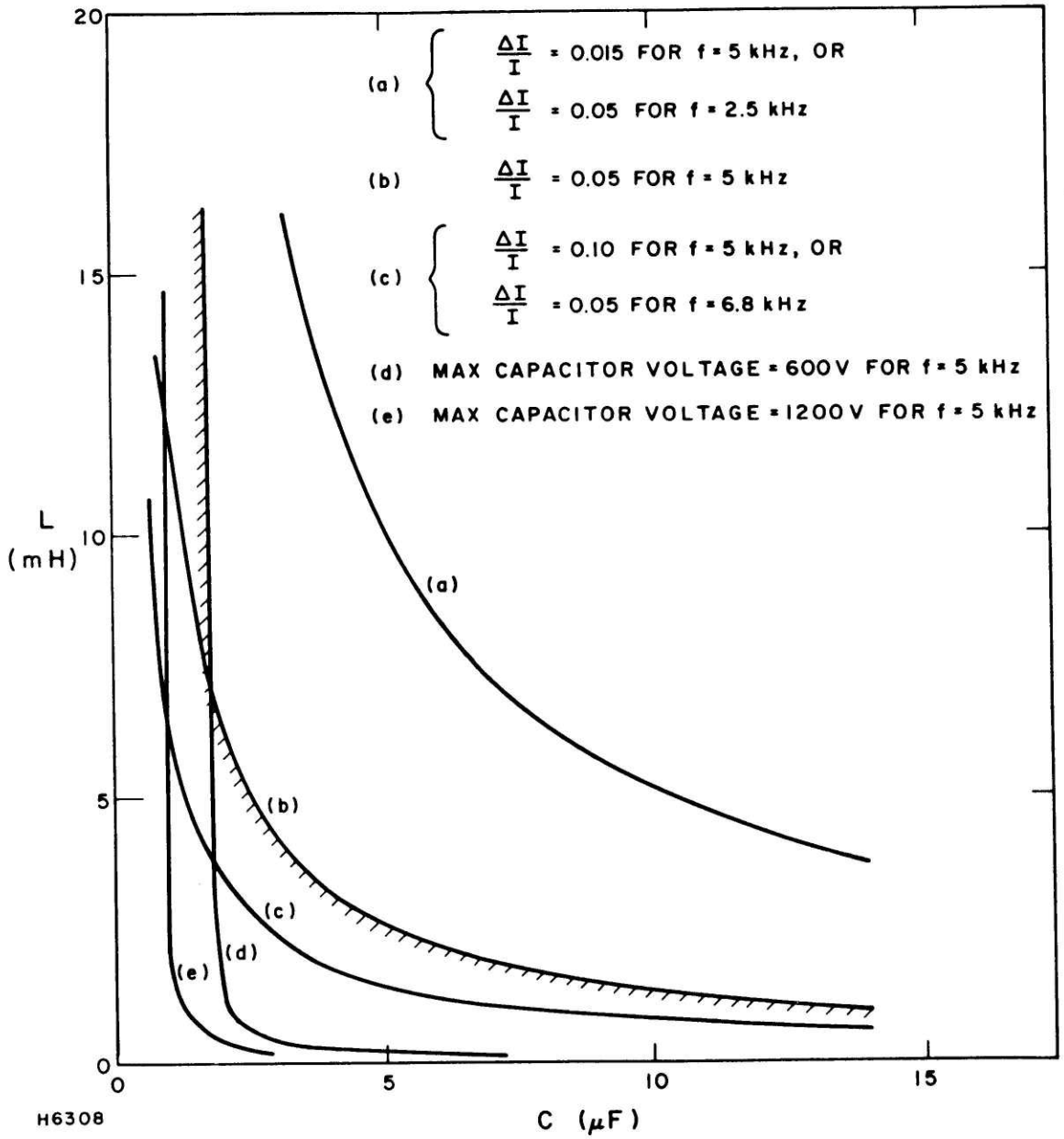


Figure 5.1 Performance Characteristics of the Consolidation Circuit for Different Values of L and C

is limited by requiring the corresponding available turn-off time to exceed the turn-off time specification for the particular SCR used.

For the same values of L and C, increasing the frequency decreases the current fluctuation. Equivalently, for the higher frequency, we can afford to use smaller C and L and still get the same percentage current fluctuation. As a result, the same curve that describes $\frac{\Delta I}{I} = 0.05$ for f = 2.5 KHz describes $\frac{\Delta I}{I} = 0.015$ for f = 5 KHz. (See Figure 5.1).

Similarly, the curves for constant maximum capacitor voltage shift left for higher frequency and right for lower frequency. So, the allowable region as bound by the shaded line on the left shifts left for higher frequency and shifts right for lower frequency.

Step 5

The commutating frequency is the most inexpensive parameter to increase. So probably, the highest possible frequency should be used. It should be borne in mind that the higher the frequency the larger the losses even though the sizes of capacitors and inductors become smaller. An analysis can be made to determine the break-even point.

A trade-off can be established between so many units of capacitance versus so many units of inductance. The trade-off can be expressed in the form of a relationship in the LC plane. Incorporated into the relationship can be cost, availability, reliability, personal preference, etc. This relationship can then be added on to Figure 5.1 to help establish the desirable operation point.

The minimum power ratings required for the inductors and

capacitors can be determined from the total current, current fluctuation, and maximum capacitor voltage. Of course, another degree of freedom comes from a choice of SCRs which may have different turn-off time and maximum on-state repetitive voltage limitation.

Other Consideration

Holding current - as discussed in Chapter 4, Section B. 2, as the load inductance becomes large, high voltage is required to start and build up enough current to sustain the SCR in the on-state. In designing the circuit then, it may be more desirable to choose SCRs that have lower holding current. Also, if this problem of holding current limits the operation of the circuit, the pulse width of the gate signal may be increased to reduce the high voltage requirement since, from equation (1) in Chapter 4,

$$i = \frac{V_o}{R} \left(1 - e^{-\frac{R}{L} t} \right)$$

increasing the pulse width t will decrease the voltage requirement V_o for the same value of holding current i.

Appendix: Gap Voltage Non-Uniformity

MHD research in the United States has been focussed on coal-fired generators. Coal combustion gives off a by-product known as slag that deposit on the channel walls. This slag layer has a lot of interesting effects on channel performance, some favorable and some unfavorable. Here, its effect on the consolidation circuit will be looked at.

The slag layer on the electrode wall may electrically short out two or more electrodes. This has little effect on the circuit though when the circuit is on and all the SCRs commutating. The circuit in the configuration of Figure 4. 8 was tested with all combinations of the inter-electrode gaps being shorted, and it was found that this has no effect on the current pattern in the circuit.

However, with no interelectrode voltage, the consolidation circuit may not be able to start. The forward bias voltage required for the SCR to conduct comes from the capacitor voltage which in turn originates from the gap voltage when the circuit is starting to commutate. This problem about starting is in a sense of secondary importance and has not been looked deep into.

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