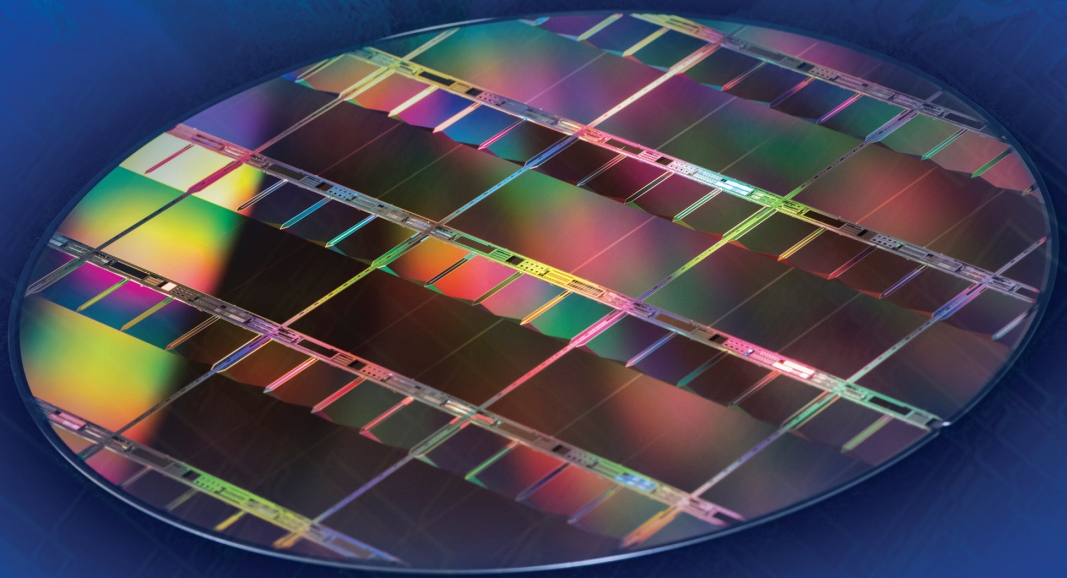
Reasserting U.S. Leadership in Microelectronics

- A White Paper on the Role of Universities

SEPTEMBER 2021



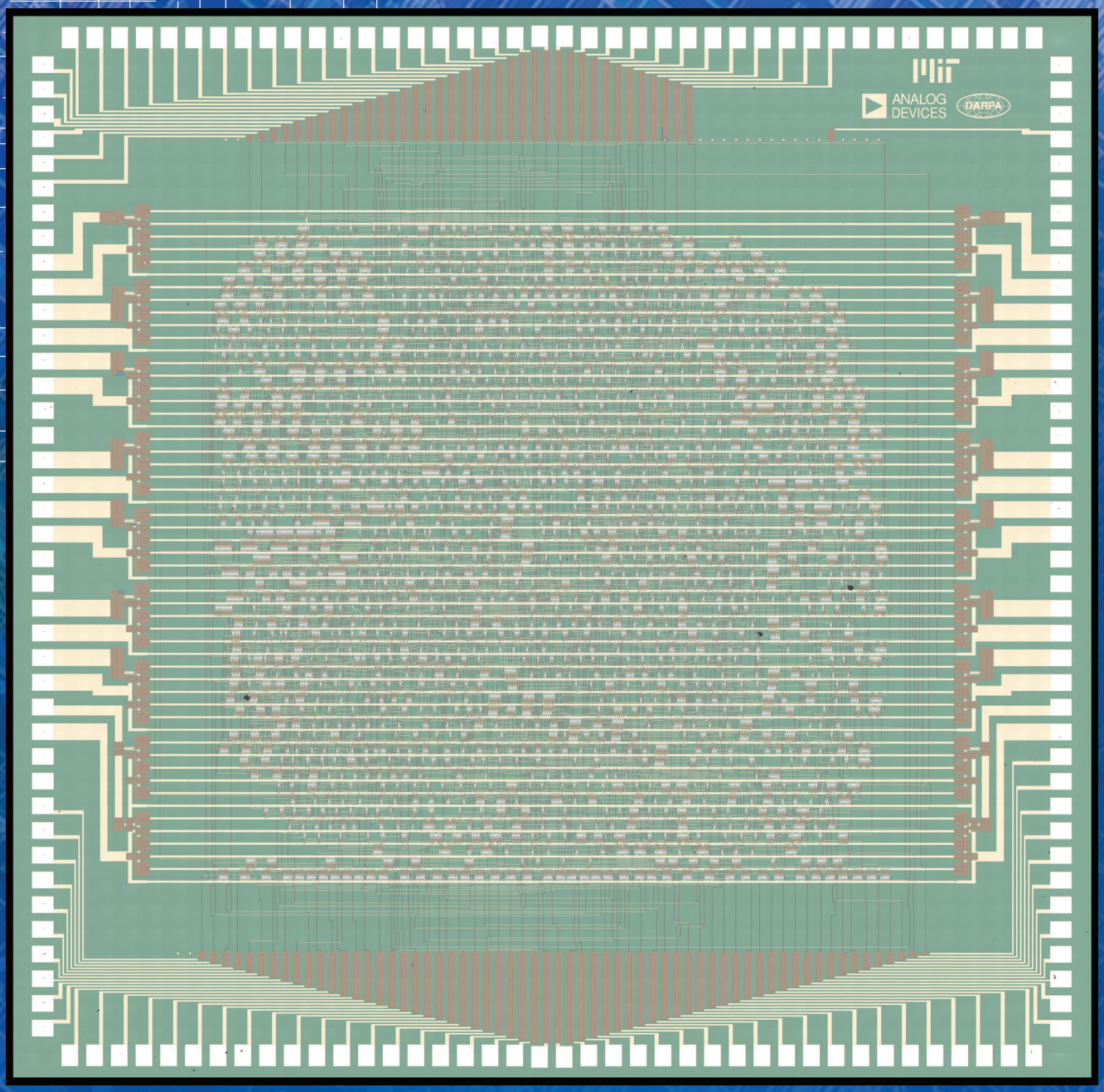


Fig. 1

Authors:
Jesús A. del Alamo, Dimitri A. Antoniadis, Robert G. Atkins, Marc A. Baldo, Vladimir Bulović, Mark A. Gouker, Craig L. Keast, Hae-Seung Lee, William D. Oliver, Tomás Palacios, Max M. Shulaker, Carl V. Thompson

Acknowledgements:
Anantha P. Chandrakasan, Martin A. Schmidt, Joel Voldman, H.-S. Philip Wong, Deirdre Zammit, Maria Zuber

The following university colleagues endorse the messages and sentiments captured in this document:
Tsu-Jae King Liu, Dean and Roy W. Carlson Professor of Engineering, **University of California, Berkeley**
H.-S. Philip Wong, Willard R. and Inez Kerr Bell Professor in the School of Engineering, **Stanford University**
More endorsements at **http://usmicroelectronics.mit.edu/**

Graphic Design:
Sampson Wilcox

v 13.4

Contents

Executive summary

"U.S. strength in semiconductor technology and fabrication is vital to U.S. economic and national security interests." [1]

The United States' longstanding leadership in the realm of semiconductors and microelectronics is today under serious challenge. The solution: a concerted and ambitious national response that emphasizes manufacturing, innovation and workforce development. As a key element in the rich ecosystem that has underlaid U.S. preeminence in microelectronics for more than 50 years, universities play a significant role in this national quest.

This white paper synthesizes a high-level vision for how universities can best contribute towards the national priority of reasserting U.S. leadership in microelectronics. With a "first-principles" approach, we propose a process for deliberation and resource allocation that looks at three key questions: what are the needs of the country, how do they map onto the core competences of universities, and which programs and partnerships are most likely to deliver the desired results. It should be noted that in this document, we do not attempt to match the proposed programs to specific initiatives currently under discussion, such as those spelled out in the CHIPS Act (National Semiconductor Technology Center, National Network for Microelectronics R&D, National Advanced Packaging Manufacturing Program and others) or the Endless Frontiers Act.

The study presented in this white paper leads to several recommendations. We bin them into five categories:

[1] "Semiconductors: U.S. Industry, Global Competition, and Federal Policy" by Congressional Research Service, October 26, 2020.

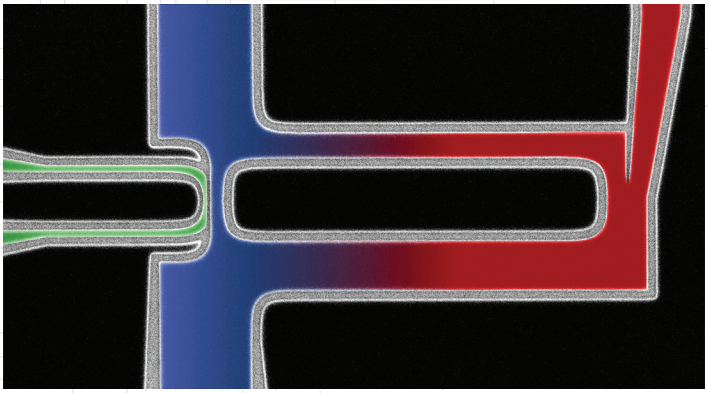


Fig. 2

1. Education and workforce development

- Create a nationwide university/industry/government program to develop educational content for broad dissemination and to support **outreach initiatives** designed to expose and attract high-school students and first-year college students from diverse backgrounds.
- Invest in and support the maintenance of educational facilities in and programs at universities designed to foster hands-on, project-based, design-oriented, multidisciplinary **research and educational experiences for undergraduates**.
- Create nationwide **fellowship and internship programs** for undergraduate, masters, PhD students and postdocs.

2. Research

- Establish **research programs** that foster a broad range of research, from fundamental to industry and national-security oriented, from single-investigator to multidisciplinary and multi-institution. Research programs must pay the full cost of research (salaries, materials, fab expenses, etc.), and Intellectual Property (IP) terms must equally support all commercialization pathways.

3. Technology translation, startups and intellectual property

- Develop programs designed to facilitate **the maturation of technology** in appropriate university environments and the subsequent translation to external foundries and corporate R&D laboratories.
- Create programs to support the generation and nurturing of microelectronics **startups** by partially underwriting user fees at shared university facilities. Establish translational fellows' programs to facilitate the exploration of startups by students and postdocs.

4. Academic infrastructure

- Make large, sustained investments in updating fabrication and metrology equipment in **university research facilities** with emphasis on outfitting a few with flexible, production-class but research-oriented, 200 mm tools.
- Establish programs to provide sustained support for **operational costs** of the national university tool base.
- Invest in a nationwide program to underwrite the creation of new faculty positions, to provide flexible career-initiation grants to **junior faculty**, and to engage industry researchers in university activities.

5. Regional networks

- Foster regional networks to create and manage research programs, educational programs, startup support, outreach, and internship programs with a regional dimension and that are designed to facilitate the involvement of **educational institutions previously on the sidelines** of the national microelectronics enterprise.

US leadership in microelectronics

Microelectronics underpin our modern information society. The extraordinary progress—within a single human generation—that we have witnessed in health, communications, computation, energy, transportation and so many other areas of human endeavor stem from the revolutionary advancements of microelectronics technologies over the last 50 years. Arguably, no other technology in history has advanced so fast or delivered so much to human society. The unrivaled leadership of the U.S. in microelectronics since its inception has brought enormous economic progress to our nation and deterred adversaries that could threaten our security.

That commanding role, however, has eroded over time. Other countries are now vigorously contesting U. S. leadership in microelectronics, and that includes countries often at odds with our nation's interests and values. As leading-edge semiconductor manufacturing capacity has dramatically dwindled in the U.S., concerns about vulnerable supply chains in the event of natural disasters, trade disputes, or military conflict have come to the fore. This realization has prompted a healthy degree of introspection and a deep examination of the entire ecosystem in which microelectronics thrives. This analysis has revealed multiple weaknesses and gaps that the U.S. government is committed to address through the CHIPS Act and other legislation.

This white paper aims to contribute to the synthesis of a national vision for the role of universities as part of an ambitious holistic drive for the U.S. to reassert its leadership in microelectronics. U.S. universities play a unique role in the ecosystem that supports the nation's excellence in advanced technology and can provide a singular perspective.

The terms "microelectronics" and "semiconductors" are often used as short-hands to refer to a broad range of technologies involving multiple material systems, processes, and devices performing various functions. As ubiquitous hardware technology, nanoscale logic CMOS technology based on Silicon is at the core. Equally strategic are memory technologies, signal processing, power electronics, communication chips, system integration technologies, sensors, photonics, as well as the broader context of manufacturing equipment, advanced materials, packaging, circuit and system design and verification tools, and the large system integrator industry that aggregates it for the end customers.

To ensure long-term leadership, leading-edge semiconductor manufacturing in the U.S. must be prioritized and universities activities must be closer to it.

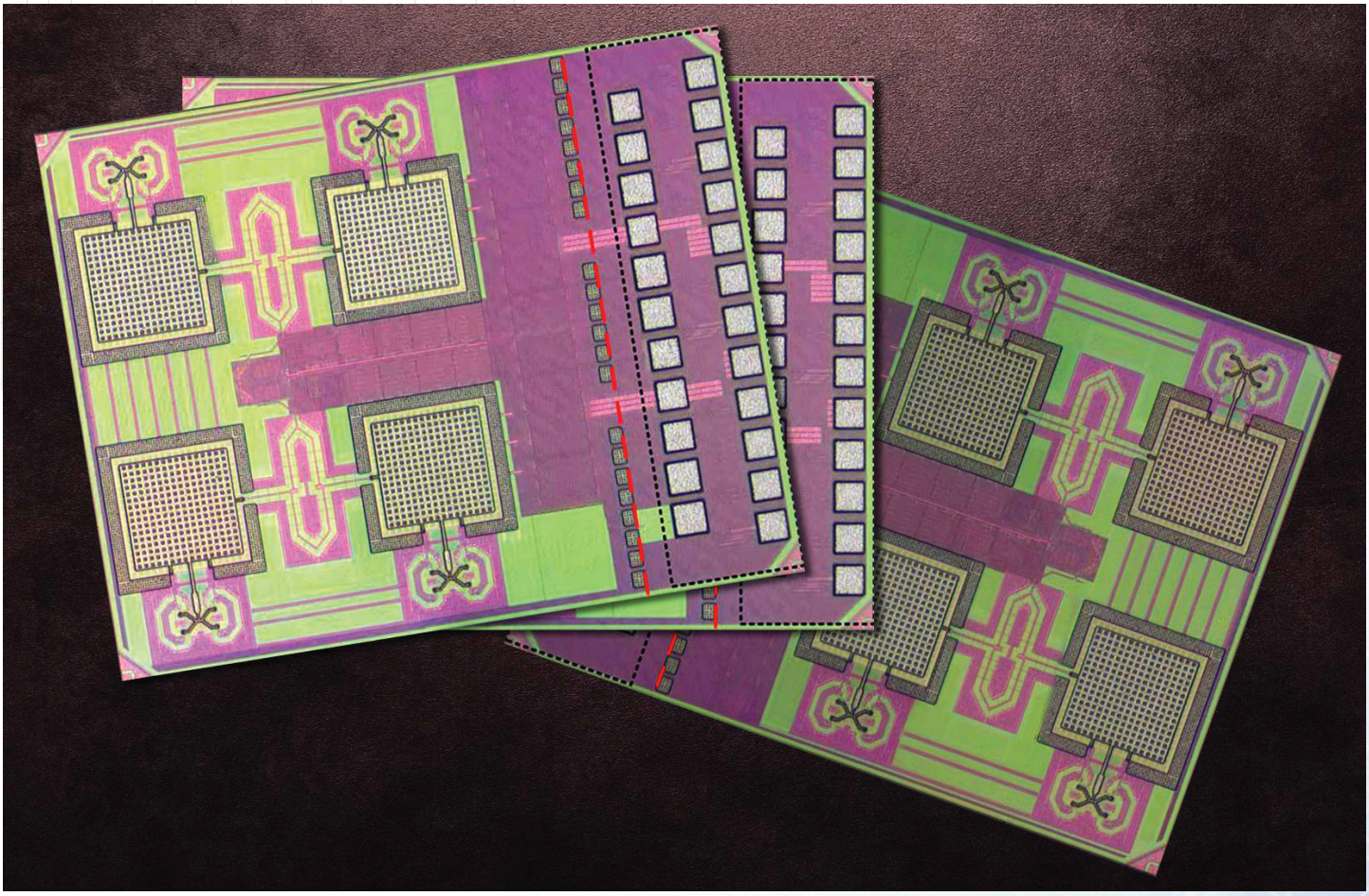


Fig. 3

The ever-expanding diversity of materials, processes, and functions makes microelectronics a rich and rapidly changing field, one that is forever spawning surprises and unexpected opportunities. A deep reexamination of all the elements of the microelectronics ecosystem and their symbiotic interactions is now warranted. Traditional geometrical scaling of logic CMOS will continue to be central to virtually all applications despite a slowdown in performance gains and increasing costs with each new node. Innovative application-specific architectures and algorithms will contribute significant enhancements in performance as already evidenced by data-intensive artificial intelligence applications that are demonstrating seemingly superhuman capabilities in solving previously intractable problems. New material systems, devices, and integration technologies are opening unprecedented capabilities in communications, memory, computation, power management, and interfaces with the human body.

Fig. 4

Opportunities abound. Seizing them, however, is not straightforward. Hardware innovation is significantly constrained in the absence of a deep understanding of manufacturing systems. This requires the physical proximity of those doing the production to those doing the innovating. The hollowing out of semiconductor manufacturing in the US is compromising our ability to innovate in this space and puts at risk our command of the next technological revolution. To ensure long-term leadership, leading-edge semiconductor manufacturing in the U.S. must be prioritized and universities activities have to get closer to it.

"Without scaling [to volume manufacturing], we don't just lose jobs - we lose our hold on new technologies. Losing the ability to scale will ultimately damage our capacity to innovate." - Andrew Grove, Bloomberg Businessweek, 2010

Universities in the microelectronics ecosystem

Institutions of higher learning are central actors in the microelectronics enterprise. Universities, together with colleges and community colleges, contribute virtually the entire workforce in the microelectronics ecosystem. Universities also generate the lion's share of fundamental research that identifies early opportunities and show stoppers. It is in university labs that the application potential of a new technology is often recognized first, and it is university facilities that often spawn the new companies that bring pioneering concepts to the world. Most major innovation hubs around the world are in close proximity to university campuses.

U.S. universities have long enjoyed an enviable preeminence in science and technology that has contributed to the long-standing U.S. microelectronics leadership. The country's universities attract the very best graduate students and postdocs from across the planet. They join our labs and contribute to the research enterprise, and most remain in the U.S. upon graduation. This pool of talent also rejuvenates the faculty ranks and launches new commercial ventures. There has long been great respect in U.S. academia for "the dignity of useful knowledge" and the translation of fundamental research into practical technologies that better the world. The engagement of industry in university research activities has been productive and valued by all involved. Since Vannevar Bush's post-world-war "Endless Frontier," the U.S. government has vigorously championed fundamental research in microelectronics and fostered academia-industry partnerships that address major challenges and exploit new possibilities.

Alas, the pride that we take in our many achievements in microelectronics risks obscuring the challenges that we face as the U.S. seeks to reestablish dominance in this crucial area. In this extraordinarily fast-moving field of microelectronics, the technological landscape that we navigate is changing at an ever-increasing pace. Staying on top has grown precarious given the aging facilities and inadequate resources of U.S. universities. Societal changes are also a factor as interest in "hard tech" among U.S. students wanes. Hidden deep inside shiny boxes, microchips are taken for granted, and STEM-inclined students today cannot see a fulfilling career in the microelectronics industry that creates them. Meanwhile, other countries, including our adversaries, have made it a national priority to wrestle the microelectronics future away from the U.S.

This white paper summarizes the role of universities in the microelectronics ecosystem, highlighting areas of strength and identifying challenges and opportunities for universities to contribute to a renewed U.S. leadership. The following sections focus on the four key aspects of the university enterprise:

- **education and workforce development,**
- **research,**
- **technology translation, startups and intellectual property,**
- **and academic infrastructure.**

In addition, we discuss **regional network efficiencies** that can be exploited in realizing this national quest.

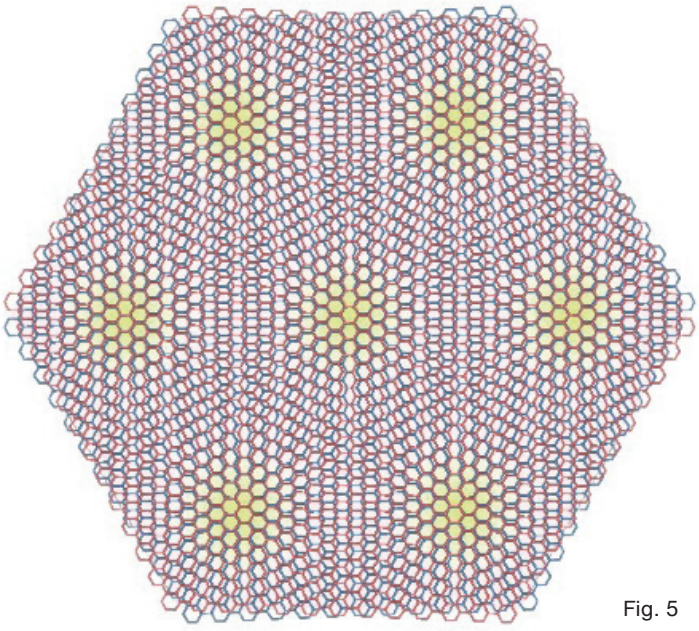


Fig. 5

Universities, together with colleges and community colleges, contribute virtually the entire workforce in the microelectronics ecosystem.

Education and workforce development

Education is, of course, at the core of the university mission. After all, an educated, motivated and diverse workforce is essential for industry to thrive. For the U.S. to regain worldwide leadership in microelectronics, a dramatic expansion of the size and diversity of the microelectronics workforce is imperative. There is no more strategic convergence of interests among university, industry, and government than the education of the next generation of technicians, engineers, scientists, and technical leaders in microelectronics.

The university system in the U.S. attracts the best talent from all over the world to its graduate and postdoctoral programs. Our resources, our meritocratic system, and promising long-term career prospects constitute the magnet. The bulk of this talent remains in the U.S. and joins the university ranks or transitions to industry or national labs. The roster of extraordinarily accomplished leaders who have taken this path is long and distinguished.

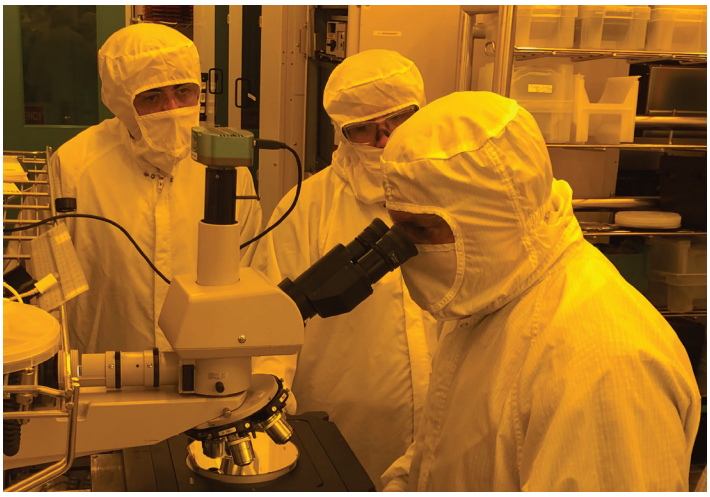


Fig. 6

Considerably more so than in other countries, U.S. educational programs have combined hands-on education involving rich project-based experiences, design exercises and research projects, with a well-balanced grounding in fundamentals. The guiding principle is that active student engagement promotes better learning. U.S. educational programs also enjoy a rich culture of industry internships at the graduate and undergraduate level, when students have an opportunity to acquire practical skills, learn about career prospects, and contribute towards college costs.

Still, in the words of industry insiders, "the U.S. educational system is failing to produce a sufficient number of American workers and students with the necessary STEM expertise to meet the needs of the semiconductor industry." [2] Among undergraduates with interest in STEM disciplines, enrollment in the "hard disciplines" has been withering for many years in favor of majors such as computer science. That this is also a worldwide trend should not serve as consolation. The challenge goes beyond the training of engineers and PhD candidates in microelectronics. Indeed, it is commonly estimated that 50 technicians are needed to support every PhD working in the industry.

Underlying this apathy towards microelectronics-related disciplines is a lack of awareness of how microelectronics can help address the world's most pressing problems, something that undergraduates tell us is motivating. They also do not see fulfilling careers at the other end of a very demanding course of study. This is a systemic failure that will require concerted collective action to correct. We need to come together through system-oriented multidisciplinary subjects, hands-on lab courses, research experiences, design exercises using modern computer-aided design (CAD) tools, well-crafted internship programs in industry, and support from industry mentors to attract students back to our disciplines. Research on pedagogy should explore new teaching methodologies that substantially shorten the long learning curve and reduce the high barrier for technology access that sits on the way to fulfilling project

We need to come together through system-oriented multidisciplinary subjects, hands-on lab courses, research experiences, design exercises using modern computer-aided design (CAD) tools, well-crafted internship programs in industry, and support from industry mentors to attract students back to our disciplines.

[2] 2019 SIA Blueprint for Sustained U.S. Leadership in Semiconductor Technology

and internship experiences. Implementing these initiatives will require sizable investments in research and educational facilities and in staff support. All this should be done without distracting ourselves from teaching the fundamentals—more important than ever in these rapidly evolving disciplines.

Fellowships for master's level studies would also drive promising students to seek higher-level specialization through advanced courses, more intense design and project experiences, and rewarding internships. At present, stand-alone master's level studies that require a thesis but do not lead to a PhD have a high cost that is tough to justify through involvement in research via research assistantships. A well-targeted masters-level scholarship program, perhaps involving industrial internships as some universities have done, would expand the pool of qualified graduates around the country. In addition, fellowships at the PhD and postdoc levels will enlarge the ranks of highly qualified engineers and scientists in microelectronics and contribute to innovation by derisking the launch of new initiatives and smoothing research support fluctuations.

A national microelectronics workforce development initiative must seek not just to expand the pool of qualified graduates in all relevant disciplines and at all levels but to also dramatically enrich its diversity in every dimension. Straightforward scale up of existing programs at institutions that are well established in the ecosystem will not accomplish this. The involvement of educational institutions that for much too long have been on the sidelines of the microelectronics enterprise is imperative. Well-established universities should open their facilities and share their resources and know-how with a wide range of colleges and community colleges and should support the creation of educational programs, hands-on and research experiences, and internship opportunities for their students. Outreach efforts to middle school, high school, and community colleges must expand and deepen their reach. In all these programs, particular attention must be given to underserved institutions across the entire geography of the U.S. Many opportunities exist for economies of scale here if industry and academia coordinate activities across the country to develop and share resources and best practices.

Universities also should play a role in supporting the continuing education needs of the microelectronics industry workforce. In such rapidly changing disciplines, new materials, technologies, processes, and techniques emerge all the time. Universities originate many of these innovations and are in a privileged position to prepare the existing workforce to take advantage of them. Recent advances and experiences in online pedagogy make it eminently feasible to create and share educational materials on a national scale.

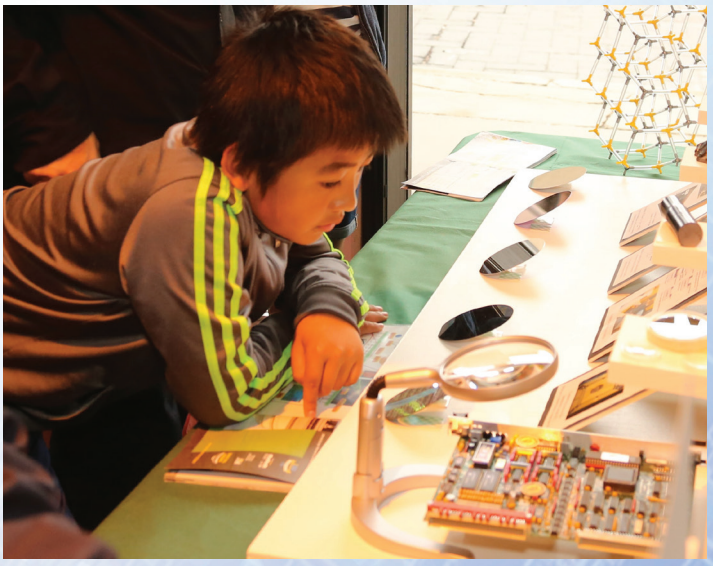


Fig. 7

Research

Research is central to the modern university. Universities attract the most gifted graduate students, postdocs, and junior faculty from all over the world by promising resources and an environment where they can carry out world-class research and launch fulfilling careers. Curiosity-driven, single-investigator research is the cornerstone of new discoveries and constitutes the foundation upon which most innovative technologies are built. Multidisciplinary, vertically-integrated, collaborative research with industry participation brings into focus promising technologies and facilitates commercialization. Partnerships that include industry, universities, and national labs are routinely assembled by mission-oriented agencies to attack ambitious projects with relevance to national security. The U.S. can pride itself on a meritocratic system of research support whereby universities and their investigators routinely compete but also collaborate and where resources are channeled in the most promising directions.

In microelectronics, the record of accomplishments by U.S. universities is unmatched. Fundamental research in advanced lithography, strain engineering, scaled transistors, wide bandgap semiconductors, THz devices, MEMS, 2D materials and devices, circuits and systems, AI hardware, among many examples, has fueled a long pipeline of technological innovations with tremendous economic significance. U.S. universities have contributed to this extraordinarily expensive enterprise by pooling resources and creating and managing shared facilities that can support a broad range of fabrication processes and materials.

As distinguished as that record is, U.S. universities confront mounting challenges to their relevance in the face of outsized investments by other countries. A widening chasm has been growing for some time between university facilities and the state-of-the-art tools and processes used in industry. Not only is the maximum wafer diameter that university facilities can handle in multi-step fabrication mismatched with industry (at best, 150 mm vs. 300 mm, see Appendix A) but the performance, productivity and reliability of the university toolsets is in decline. This greatly limits competitiveness, inhibits collaborations with industry or national labs, and compromises technology translation. At the heart of this problem are aging facilities, obsolete tools, unaffordable equipment service plans, and inadequate technical staff support.

Universities attract the most gifted graduate students, postdocs, and junior faculty from all over the world by promising resources and an environment where they can carry out world-class research and launch fulfilling careers

To compound the difficulties of operating in this resource-starved environment, many research contracts do not cover the true cost of research that requires large integrated facilities with multi-step semiconductor fabrication processes. Faculty, in their role as university facility administrators, must devote substantial efforts to raising additional resources within or outside the university to make ends meet. A culture of scarcity permeates the whole operation.

What can be done? The U.S. urgently needs a national plan of investment in both human and capital infrastructure. Appropriate emphasis needs to be given to establishing 200-mm wafer diameter capabilities, the “sweet spot” for collaborations with industry and national labs and for technology translation today (see Appendix A). Sustained investments are required to keep the facilities relevant, including mechanisms that provide stable support for equipment service plans and technical staff. A national coordination body should be established to provide users across the country (not just research universities but also colleges, community colleges, start-ups, corporations, and national labs) with agile access to many university facilities across the U.S. as well as unique resources such as a national 300-mm R&D center (National Semiconductor Technology Center).

Research programs need to be expanded and their costs fully covered. Essential also is the establishment of a healthy mix of single-investigator grants, multi-disciplinary vertically-integrated programs, and collaborative university/industry/national lab initiatives over a broad intellectual front in a competitive, meritocratic framework that supports a diverse community of researchers and students.

Technology translation, startups and intellectual property

U.S. universities are hotbeds of innovative technologies and new knowledge. That knowledge is disseminated into the world through multiple mechanisms. Symposia, conferences, research papers, mutual visits, and other academic activities are effective paths to broadly share the fruits of research. Graduating students and postdocs who continue their careers outside the university bring a strong fundamental education, in-depth understanding, and practical research experience that benefits their new employers.

Many effective technology-transfer avenues from universities to industry exist. Companies that directly sponsor research programs at a university—either individually or through consortia—enjoy early and privileged exposure to research results through periodic updates, progress reports, and formal project reviews. Informal interactions between the company sponsor and the university research team are effective means for sharing detailed insights and know-how that might never be published. Joint research projects that bring together university and industry collaborators are particularly effective in enabling fruitful direct exchanges. Through periodic formal and informal interactions, industry sponsors can become aware of valuable new directions or significant roadblocks well ahead of the rest of the world.

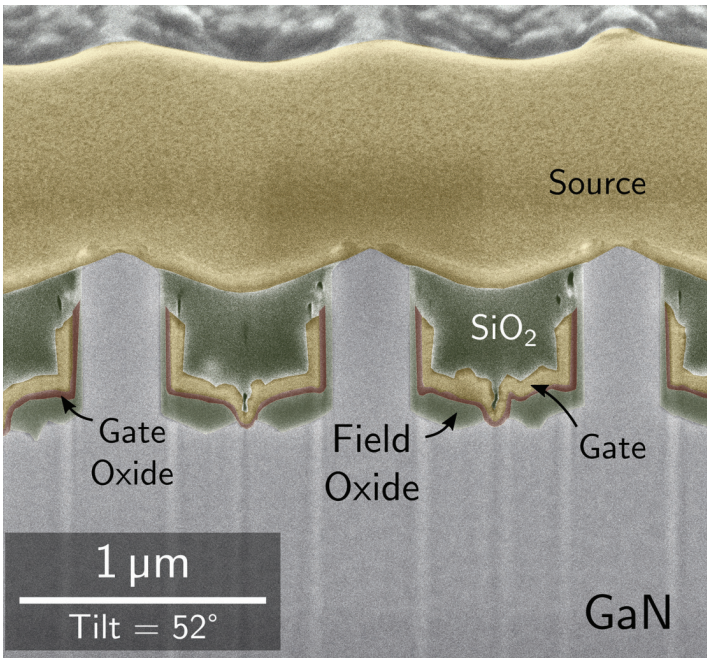


Fig. 8

Graduating students and postdocs who continue their careers outside the university bring a strong fundamental education, in-depth understanding, and practical research experience that benefits their new employers.

It is often the case that the products of university research do not initially reveal their ultimate commercial value. This makes it difficult for companies to decide to license university intellectual property (IP) soon after it is conceived. In microelectronics hardware, where the typical time for an invention to reach the marketplace is 10 years, it takes a certain degree of technology maturation for the value of a new concept to become apparent. This advanced research phase generally implies: 1) scaling down from the relatively large dimensions typical of academic research to state-of-the-art manufacturing feature sizes, 2) developing additional fabrication process modules required to enable the demonstration of sufficiently complex systems, and 3) creating models that can be used to design and predict the performance of future systems enabled by the new technology. At the end of this exercise, one should be able to assess with reasonable confidence the functionality, performance, manufacturability, and reliability, among many other issues, that the new technology will ultimately deliver and thereby decide whether the technology is suitable for transition to volume production.

Microelectronics technology maturation requires a tool set, a baseline of established process modules, functional block designs, and strict execution protocols that reflect the ultimate manufacturing environment. Shared university facilities generally cannot meet these high standards. Instead, an effective path for translation of new university technologies is through partnerships with prototyping facilities, national labs and commercial foundries. These entities embody the rigor of a manufacturing environment, while preserving a relatively high degree of flexibility that enables them to embrace new disruptive technologies. The engagement of pro-

totyping facilities lowers the risk and costs associated with elevating university research to manufacturable technology. Prototyping facilities in national labs play the unique and critical role of facilitating the translation of technologies with strategic national security significance. Fostering prototyping facilities and subsidizing engagement with universities to promote technology maturation should be a high priority in a national microelectronics program. Established companies will find it increasingly attractive to directly license university IP once the university has had an opportunity to demonstrate its commercial potential through partnerships with prototyping facilities.

University-generated tech startups also can have considerable impact in the world. Flourishing innovation ecosystems have emerged around university campuses in the U.S. They attract venture capital, research labs within well-established companies, and startup incubators. These ecosystems support the launch of new companies, enable economic development, and push the next wave of electronic systems. Countless microelectronics startups have evolved into world-class corporations. In addition, many startups are acquired by well-established companies allowing the acquirer to quickly enter a new field at reduced risk and relatively low cost. In all cases, even when they do not ultimately succeed, startups provide extraordinary training opportunities for scientists and engineers that eventually come to benefit future employers. Successful startups generate considerable buzz on campus, which can be effective in rejuvenating the waning student interest in microelectronics. Bottom line: the U.S. innovation ecosystem is the global gold standard, and many countries strive to replicate it.

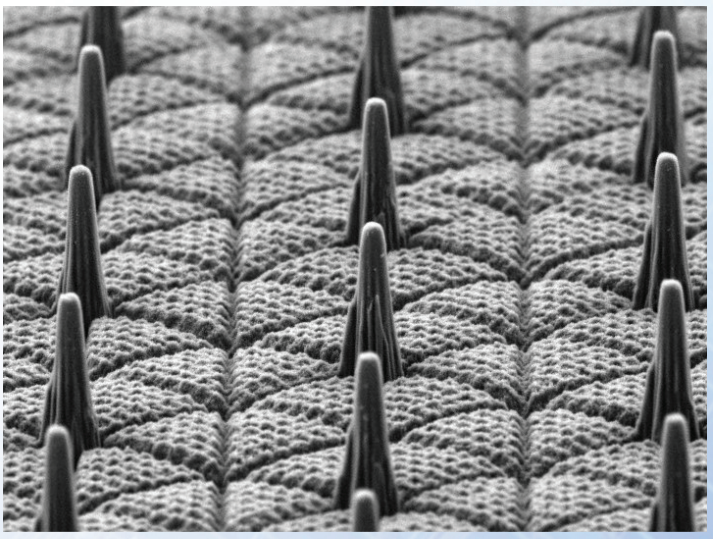


Fig. 9

Fostering the formation and growth of startups should be among the core goals of a comprehensive national microelectronics strategy. While the U.S. innovation and commercialization record is impressive, many obstacles remain, including the high costs associated with development of microelectronics technologies and access to fabrication facilities. Startup activities could be fostered by providing subsidized access to university facilities when compatible with the university's core research and educational mission. This access broadens the user pool of a university's shared facilities, lowering the cost to all players. It further allows startups to build quickly on demonstrated technologies in their native environment without having to invest enormous time and resources in establishing and operating their own facilities, only to replicate results that their founders have already obtained.

The inventors of a technology are often the best entrepreneurs to transition their innovations to market. Incentives for students and postdocs to engage in technology translation activities, whether through startups or by participating in a rigorous prototyping effort, can be created by means of translational fellows programs. These programs would support students and postdocs outside their regular research activities as they explore the commercialization of the technologies they have created.

U.S. universities can retain ownership of inventions created with federal funding under the Bayh-Dole Act. This legislation was established to encourage universities to engage in technology transfer activities. When it comes to technology translation, adequate handling of university-owned IP is key. From the perspective of industry, "robust intellectual property protection is essential to preserving incentives for innovation." [3] Fostering IP generation and nurturing IP through the long road to societal impact is critical to the long-term competitiveness of the U.S. microelectronics industry. The role of universities in this regard is to create an environment that stimulates and protects innovation and incentivizes its commercialization through commercial licensing.

U.S. universities grant licenses to their patented and copyrighted inventions to both established companies and startups if the licensee demonstrates the technical and financial capabilities to develop the early-stage technology into commercially successful products. Research contracts with industry generally include terms

Fostering the formation and growth of startups should be among the core goals of a comprehensive national microelectronics strategy.

[3] 2019 SIA Blueprint for Sustained U.S. Leadership in Semiconductor Technology

Fig. 10

A new compact for microelectronics IP generation and protection in a university environment must be established that respects the spirit of the Bayh-Dole Act. An organization with representatives from government, industry, academia, and the venture capital community should be created to generate policies and provide oversight.

that create options for the sponsor to license the IP that is generated in the course of the research in a non-exclusive or exclusive form in a field of use. An exclusive license within a field of use is a crucial asset for a start-up, as it confers to it a higher valuation and increases its ability to attract capital.

In recent times, research contracts with industry consortia have come with IP terms that severely limit the ability of universities to license technology in exclusivity—in effect, disincentivizing IP generation. In a way, these terms prioritize existing companies at the expense of future companies. When mixing industry consortia and US government research funds, as is desirable in the launch of ambitious, multidisciplinary, multi-university research programs, much more restrictive IP terms than those typical for U.S. government contracts are ultimately adopted. The sheer size of these programs and the number of consortia players that are involved make IP negotiations highly unbalanced.

As we seek a greater role for public/private partnerships in microelectronics research, a new compact for microelectronics IP generation and protection in a university environment must be established that respects the spirit of the Bayh-Dole Act. An organization with representatives from government, industry, academia, and the venture capital community should be created to generate policies and provide oversight.

Academic infrastructure

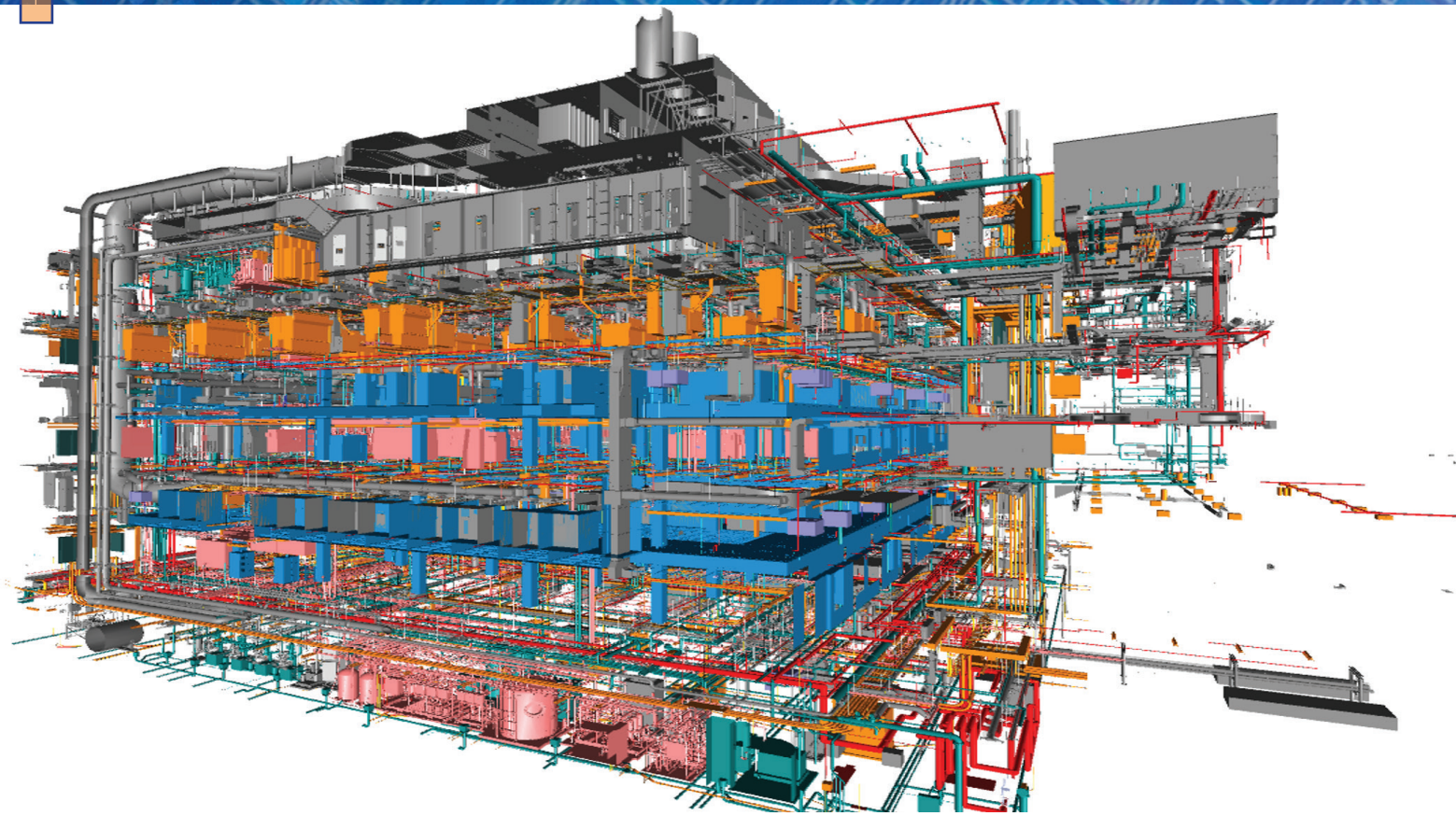


Fig. 11

We make the case above for the expanded role of universities in education, research, and IP generation and translation as part of a comprehensive national drive to regain leadership in semiconductors and microelectronics. Key to accomplishing these goals is a robust university infrastructure—facilities and tools but also the staff support structures that make everything hum.

We noted earlier the inadequate state of university research facilities for advanced microelectronics research and the need for a crash program to rejuvenate, expand, and subsequently sustain and periodically refreshen the capabilities. We further made a case for the importance of establishing new 200-mm facilities that combine the performance, reliability, and reproducibility of commercial manufacturing tools with the flexibility to handle a wide range of materials and sample sizes and shapes. These tools, as well as smaller, more versatile research tools, can be operated in an economically sound model if they are shared by a broad community of investigators, educators, startups, companies, universities, colleges, community colleges, and national labs.

Attention to university infrastructure should extend to facilities for metrology, CAD, system design and prototyping, testing and packaging, and access to integrated circuit (IC) shuttle runs.

Attention to university infrastructure should extend to facilities for metrology, CAD, system design and prototyping, testing and packaging, and access to integrated circuit (IC) shuttle runs. It is often the case that these capabilities sit in private labs or are otherwise out of reach to students taking classes. Existing shared facilities should support these resources for the benefit of the entire community and CAD licensing arrangements and necessary cyberinfrastructure should be put in place to allow flexible access by the at-large student body.

A national program that aims to restore U. S. microelectronics leadership should also invest in the creation of new faculty slots at U.S. universities and colleges and provide flexible start-up funds for equipment and research support in the early years of a faculty career.

The human factor is as critical as buildings and instruments. Highly qualified, well-motivated technical staff is an integral element of a successful operation. It is our experience that universities can create an attractive working milieu that is capable of hiring and retaining competent personnel even in a field rich in employment opportunities. These personnel become the heart and soul of educational and research activities. Threatening this is understaffing, scarce resources, and inadequate salaries. A crash tool expansion and modernization program, as argued here, must come with a concomitant increase in the technical staff ranks with support for service contracts by outside professional entities.

When thinking about the human factor in university microelectronics activities, junior faculty play a singular role. U.S. universities frown upon faculty inbreeding and rely on the hiring of junior faculty to rejuvenate the faculty ranks, acquire new ideas, and launch new initiatives. Junior faculty are selected through an extremely competitive process, generally with the goal of establishing new and promising research programs that expand university offerings. They are expected to quickly gain recognition in their chosen field and are given a great deal of autonomy to design their paths. This academic environment differs from that in many other countries, where junior faculty toil under the tutelage of a senior professor. In the U.S., junior faculty have to be ambitious and resourceful risk-takers and, as a result, are highly productive and innovative. A national program that aims to restore U. S. microelectronics leadership should also invest in the creation of new faculty slots at U.S. colleges and universities and provide flexible career-initiation grants for equipment and research support in the early years of a faculty career.

Further, a renewed partnership in microelectronics between industry and academia should recruit seasoned and experienced researchers from industry to participate in university education and research activities. It will be essential to develop programs that foster the on-campus presence of industrial experts as visiting scientists, professors of practice, guest lecturers, and mentors. In the other direction, it is equally important to establish research sabbaticals for faculty and university research personnel at prototyping facilities and industry research R&D laboratories.

Regional network efficiencies

The efficacy of the comprehensive and ambitious plan that is proposed here can be enhanced considerably by exploiting substantial regional network efficiencies that are available. We see ample experience in our university community of multi-disciplinary, multi-institution research programs that span the entire country. This approach–one that pools capabilities and expertise from those best qualified, regardless of geography–has proven to be highly effective. The core of a scaled microelectronics research plan should, likewise, have a nationwide dimension.

Nevertheless, accomplishing the goals articulated in this white paper will involve the engagement of institutions (colleges, universities, community colleges, high school and middle schools, community centers such as science museums) that have not traditionally been part of the U.S. microelectronics enterprise. Further, smaller educational institutions with distinguished educational or research programs that are limited in scope and size could enlarge their involvement under the proposed initiative. Widely expanding the number of players, scaling up their activities, and engaging a highly diverse population of students is singularly essential to accomplishing the workforce education goals of this plan. It is in this quest that regional network effects can be helpful.

Fig. 13

Widely expanding the number of players, scaling up their activities, and engaging a highly diverse population of students is singularly essential to accomplishing the workforce education goals of this plan.

We envision a loose confederation of institutions that coordinate research, education, outreach, and internship activities at a regional scale. The notion of "region" will necessarily differ around the country. To the first order, we think of this as empowering access to substantial resources within a two-to three-hour car drive. This makes possible the regular use of facilities, routine participation in established programs, and the construction of day-long and multi-day programs that cater to a large geographically dispersed community.

Programs should be created to facilitate access to technical expertise and shared experimental and design facilities if regional institutions are to support existing and new research and educational programs. Joint research projects that engage neighboring institutions previously sitting on the sidelines should be created. Funding for visiting appointments, internships, and summer research experiences will greatly assist this mission.

Educational facilities, content and know-how also can be effectively pooled at a regional scale through a mixed in-person/online approach, as we have come to appreciate over the last year. Similarly, outreach and industrial internship programs can be coordinated and expanded on a regional scale. Startup support and technology transition efforts also benefit from regional proximity by cataloging regional resources and coordinating access protocols.

Across all these dimensions, regional-level meetings, conferences, informal get-togethers, career fairs, start-up exchanges, educational competitions, and other networking events can contribute greatly to the whole.

Appendix A
200 mm: the "sweet spot" for industry-relevant microelectronics research in universities

The tool base in the most advanced U.S. university facilities today is designed to handle 150-mm (~6-inch) wafers. The equipment includes general-purpose research tools as well as production tools destined for boutique technologies. A significant portion of the university-installed 150-mm tool base was donated by the Si industry when 200-mm Si wafers (~8 inch) became mainstream in the 1990's. In a university environment, these tools are often modified to accommodate smaller wafers and odd-shaped samples and thus support a wide range of research programs. The 150-mm tool base in U.S. universities has served academia, industry, and the country well for many years. After three decades, this flexible foundation of general-purpose research tools must be updated and selectively complemented by 200-mm capabilities so that it can support the next generation of discoveries.

Universities have shown repeatedly over the years that industry-relevant research can be carried out with a 150-mm tool set despite industry's continuing march to 200-mm and more recently 300 mm tools. After all, university research excels when it is of an exploratory nature that thrives on flexibility. University facilities are uniquely equipped to investigate new materials, processes, structures, and devices. In fact, it is often the case that industry reaches out to universities to explore new concepts that they cannot pursue in their more rigid facilities.

The flexibility of the university tool set comes at the price of repeatability, uptime, and performance. Limited repeatability and uptime are a consequence of the instrument age as well as the broad parameter space in which they typically are operated. Also, the capabilities of 150-mm tools are very far from state-of-the-art production 200-mm and 300-mm equipment.

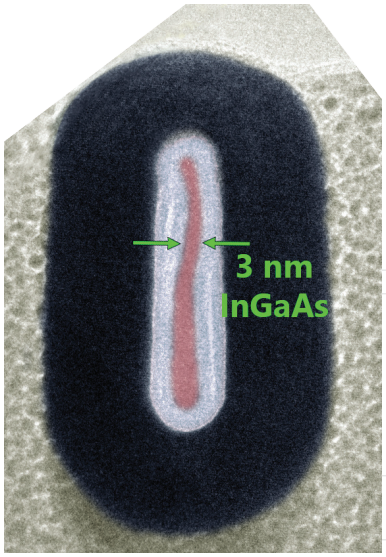


Fig. 14

At 200 mm, the balance among economics, performance and flexibility of semiconductor fabrication equipment is far more advantageous for a university environment.

The limited capabilities of the 150-mm tool set particularly hamper universities' ability to participate in technology translation activities, whether in collaboration with external prototyping foundries or by supporting the advanced development efforts of startups. Success stories do exist but a concerted effort to enhance the relevance of university research and its technology transfer activities calls for a major upgrade in the equipment base of universities.

Given that 300-mm (~12 inch) diameter Si wafer processing is the state-of-the-art today and will remain so for the foreseeable future, it is tempting to think that a few universities in the country ought to entirely bypass 200-mm capabilities and retool their facilities with 300-mm equipment. Surely this approach would dramatically increase the productivity and industrial relevance of university research and expedite technology transfer. However, this simple view clashes, not just with its daunting economics, but also with the flexibility that is the hallmark of a university research environment.

The 300-mm fabrication tools are generally designed for manufacturing throughput and repeatability within narrow process windows. As a result, they are large, highly automated, and extremely costly to acquire and maintain. This is the antithesis of what is desired in a flexible research environment where resources are also at a premium. The narrow usage profile of 300-mm tools makes shared use among a wide range of users very difficult. Even if the facilities and associated support services could be provided on a university campus, the economics of operating a 300-mm university facility are untenable.

At 200 mm, the balance between the economics, performance, and flexibility of semiconductor fabrication equipment is far more advantageous for a university environment. The first consideration is that 200-mm wafer fabs are the preferred manufacturing environment for many commercially important families of products such as ICs based on legacy nodes (for automotive, industrial, and power markets, among others), specialty products such as MEMS, smart power, CMOS image sensors, analog, RF, LEDs, and strategic technologies such as 5G and millimeter-wave, GaAs, GaN power electronics, and SiC. Research and innovation carried out in a 200-mm environment is of immediate applicability for many nascent technologies of economic and strategic significance to the U.S. Further, the process capabilities of 200-mm manufacturing tools approach, in many ways, those of 300-mm equipment while being significantly more flexible. This makes it easier to address problems and opportunities of relevance to the leading-edge CMOS nodes. Perhaps of greatest importance, the economics are vastly more favorable for 200-mm tools when compared with 300-mm equipment. If configured to run wafers of smaller diameters and odd-shaped samples, as we believe can be done, their use could be pooled among a large user community making the costs manageable.

The table below gives a sense of proportion of the cost, under current economic models, of outfitting and operating university research facilities equipped with a full suite of 150-mm, 200-mm, and 300-mm tools assuming that an adequate clean-room environment to host these tools is already available. Depending on the configuration, a 300-mm equipment set is six to seven times more expensive than a 200-mm set. Experience shows that the annual cost of maintenance and staffing is about 20% of the tool cost. A six to seven multiplier, therefore, exists here as well. These costs need to be recovered through user fees. Fabrication-heavy research projects typically can afford to devote about 20% of their budget to user fees. This yields a requirement for an annual research base that is essentially identical to the original cost of the tool base with a corresponding number of researchers, as shown in the table.

At 300 mm, a single facility would require an annual semiconductor research volume and involve a number of fabrication-heavy students and postdocs that is at least one order of magnitude larger than what any U.S. university has ever managed. On the other hand, a few well-equipped 200-mm facilities across the country are entirely feasible. In addition, the enhanced capabilities offered by a flexible high-performance tool set provide a substantial collateral benefit on other disciplines that also contribute to the pool of knowledge, innovation and workforce.

With enhanced collaboration between university researchers and semiconductor tool companies, a small number of selected 300-mm “alpha-tools” (special-purpose research-oriented equipment) would be possible to accommodate within a well-equipped and maintained 200-mm facility. This will speed up technology transfer to 300-mm production tools in industry. Since these alpha tools are unlikely to be shared among a large population of users, appropriately managing them in a university environment will require the careful definition of research and development programs in close partnership with industry and the leadership of a faculty member that has a significant stake in their success.

TOOL SUITE WITH WAFER DIAMETER OF:	COST OF OBTAINING TOOL SUITE (LITHO/DEPOSITION/ ETCHING)	ANNUAL COST OF TOOL MAINTENANCE & STAFFING (20% TOOL COST)	ANNUAL RESEARCH BASE (5X MAINTENANCE & STAFFING COSTS)	#PHD/MASTER'S/ POSTDOCS
150 mm	$15M	$3M	$15M	100
200 mm	$80M	$16M	$80M	533
300 mm	$500M	$100M	$500M	3,333

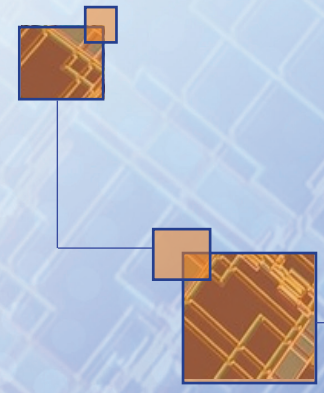


Figure Credits

Front Cover:
200-mm-diameter wafer of charge coupled device (CCD) imaging arrays optimized for use in an X-ray spectrograph. Photo courtesy of MIT Lincoln Laboratory.

Figure 1:
RV16X-NANO, a RISC-V microprocessor fabricated with over 14,700 complementary Carbon nanotubes in Prof. Max Shulaker's lab at MIT. Photo courtesy of Gage Hills.

Figure 2:
Scanning Electron Micrograph of NbN superconducting nanowire loop memory cell that includes a heat nanowire cryotron and a current crowding nanowire cryotron from Prof. Karl Berggren's laboratory at MIT. Photo courtesy of Qing-Yuan Zhao.

Figure 3:
CMOS THz-ID chip using 2x2 antenna array for 260 GHz backscatter communication and beam steering. Collaboration between Profs. Ruonan Han and Anantha P. Chandrakasan. Photo courtesy of researchers, edited by MIT News.

Figure 4:
Student in the clean room of MIT.nano. Credit: MIT.

Figure 5:
Illustration of Moire pattern formed by two sheets of graphene twisted at a "magic angle" of 1.1° by Prof. Pablo Jarillo-Herrero, MIT Department of Physics.

Figure 6:
Students in the clean room of MIT.nano as part of MIT nanoLab course activities. Credit: MIT.

Figure 7:
Young visitor exploring "Silicon Processing, from Rocks to Integrated Circuits" display at Microsystems Technology Laboratories booth during MIT 2016 Century in Cambridge Celebration. Photo by Paul McGrath.

Figure 8:
Scanning electron micrograph image of vertical GaN FinFET power transistor for electric vehicles applications from Prof. Tomás Palacios lab at MIT. This lab has spun off Cambridge Electronics, a start-up dedicated to developing GaN energy efficient electronics.

Figure 9:
SEM of micro-tips fabricated on carbon aerogel to be used as individual ion emitters for efficient electric propulsion for spacecraft from Prof. Paulo Lozano's lab on the Space Propulsion Laboratory, MIT Department of Aeronautics and Astronautics. This lab has spun off Accion Systems, a start-up dedicated to developing efficient micropropulsion system for space applications.

Figure 10:
Materials Science and Engineering undergraduate student Danielle Grey-Stewart at MIT's 2020 Microsystems Annual Research Conference. Upon graduation from MIT, Danielle Is pursuing graduate studies at Oxford University as Rhodes Scholar. Photo by Paul McGrath.

Figure 11:
3D Revit Model of MIT.nano showing the intricate network of duct work, air handling, plumbing, process gas, electrical conduits, and other building operation support systems across the 200,000 square foot facility. Image credit: Wilson HGA.

Figure 12:
A view of the fandeck at MIT.nano, showing exhaust pipes containing an array of control valves ready to accommodate new large-scale etch or deposition tools. Image credit: Wilson HGA.

Figure 13:
Every summer, MIT's Women's Technology Program (WTP) engages high-school students in a microfabrication project in which they reproduce a picture of the group on a 6"-diameter Si wafer. The picture shows a wafer in progress after exposure and development being held by a wafer wand in the yellow-light room. Photo courtesy of Paul Tierney.

Figure 14:
Transmission Electron Micrograph of 3 nm fin width InGaAs FinFET fabricated by in-situ Atomic-Layer Etching/Atomic-Layer Deposition in a collaboration between MIT and University of Colorado, Boulder. This work received the Roger A. Haken Best Student Paper Award at 2018 International Electron Devices Meeting. Photo courtesy of Jesús del Alamo.

Background images throughout:
Artwork by Sampson Wilcox.

Back Cover:
MIT.nano exterior view - Image credit: Wilson HGA.