Integrated Capacitive Sensors Using Charge-Redistribution Sense Techniques

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Abstract

An integrated capacitive pressure sensor whose transduction scheme is based on charge-redistribution techniques has been fabricated using MOS processing combined with surface and bulk micromachining techniques. The motivations behind the integration of sensor and circuit are to ease packaging and area constraints, but more importantly, to eliminate parasitic capacitances and to reduce noise which might otherwise exist in a hybrid environment. The latter two are necessary for the measurement of small capacitances.

The integrated pressure sensors are air-gap capacitors which are 100 μm square with a 0.7 μm air-gap, yielding capacitances in the 100 femtofarad range. This small capacitance requires a sensitive measurement technique. A charge-redistribution-based digital readout scheme has been developed and used to measure changes in capacitance with 30 attofarad resolution for a single measurement at sampling speeds greater than 10 kHz. The technique adequately reduces the error effects of MOS switch charge injection and its noise, parasitic capacitance, input offsets, and low-frequency noise components.

Experimental capacitance measurement results of fabricated polysilicon air-gap capacitors are correlated with finite-element analysis and optical deflection measurements. These pressure sensors have served as a convenient research vehicle for testing the sensitivity and generality of the sense technique, which may have significant applications where sensitive capacitance measurements are needed, especially in sensors that utilize small mechanical structures integrated with standard silicon processing.

Thesis Supervisor: Hae-Seung Lee
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To my colleagues, friends, and family
without whose help this thesis
would not have been possible.

Acknowledgments

> *Without discussion, the intellectual experience is only an exercise in a private gymnasium.*
>
> BOURNE

It has always been one of my tenets that almost nothing is accomplished by someone working entirely alone, with no help or assistance from people either within or outside his or her field of interest. To say that such an endeavor is a challenge is a severe understatement, not to mention a lack of judgment or humility on the part of the pursuer. The amount gained in collaboration is more than the results of a few immediate papers; it is the building of a foundation for the solving of more significant and challenging problems that lie ahead. Plus, it's simply fun.

With this in mind, this work could not have been accomplished without the help and support of numerous colleagues and friends. First, I would like to acknowledge the guidance and funding provided by my advisor, Prof. Hae-Seung Lee. Without his initial interest and research knowledge, I would not have entered this area of sensors and circuits. I would also like to thank Prof. Roger Howe at Berkeley for his enthusiasm and encouragement for entering this "forbidden" area of sensor and circuit integration. Thanks also go to Prof. Charles Sodini and Prof. Martin Schmidt for helpful comments on my thesis, and to Prof. James Chung for being a good friend all these years, for general technical and non-technical discussions which degenerated rather quickly, and for helping me to deal with the frustrations of being a graduate student living at poverty level.

Fabricating MOS circuits in a non-industrial, non-profit (or so they say) environment

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Chapter 1

Introduction

It is the mark of a good action that it appears inevitable in retrospect.

STEVENSON

1.1 Silicon Micromechanical Devices

The semiconductor electronics industry is one of the the largest manufacturing industries in addition to computer systems, automobiles, and chemical/petroleum products. The techniques and materials used to fabricate dynamic random access memories (DRAMs) and microprocessors in large volume are some of the most precise and exacting in all of manufacturing, and qualify silicon VLSI as a highly advanced technology which depends on volume, reliability, and quality in order to realize profitability. This established manufacturing base has provided the ability for system designers to incorporate inexpensive yet powerful components into more complex systems, and hence progress toward cheaper and more complex products in the market place. Workstation computers and advanced consumer electronics are a few examples of this growing trend.

It is inevitable that manufacturers of other mass-produced items will seek the use or extensions of the semiconductor manufacturing base and reap the rewards of such a highly efficient, volume-production industry. One such example is the sensor industry.

Silicon VLSI is an extremely reliable, meticulously characterized, and well-understood technology that uses the electrical, chemical, and mechanical aspects of silicon for fabrication of integrated circuits. However, the use of silicon strictly as a mechanical material in moving parts (as in sensors or actuators) rather than as a base for electrical devices (such as in a substrate) was not as effectively utilized as its electrical properties until much later. Silicon and its oxides/nitrides are fully exploited as masks, dielectric isolation, thermal or mechanical stability during wafer handling, and as material for active and passive semiconductor devices, but not yet fully as purely mechanical materials. Although considerations are given to the material properties of the films, they mostly relate to electrical characteristics, or to mechanical characteristics in terms of reliability (adhesion and/or cracking of films). This will significantly change, however, now that silicon-based materials have proven their suitability as mechanical structures.

Within the last 20 years, much work has gone into analyzing the mechanical properties of bulk silicon and its thin films [1],[2]. Various processes have been developed to etch either surface or bulk parts of silicon to form mechanical structures only. Silicon has proven to be such an interesting mechanical material that studying its mechanical properties and creating structures by themselves have already made a significant impact on sensors [3].

Nevertheless, the underlying reason for using silicon in sensors cannot be lost – that it is the same material that is used to make DRAMs, microprocessors, and other semiconductor chips in massive volume, and that this technology must be utilized in some way so that sensors can enjoy the same benefits as their somewhat distant silicon cousins – that of high reliability and performance with low cost through large production. In order for product designers to allow more flexibility and real-time control of their systems, sensors will invariably be needed, but with dramatically reduced cost, sensors will be used more frequently and allow more complex systems to be realized. In essence, the driving force behind the inclusion of sensors in many products is cost. Most "new" sensors are not really new sensors but simply ones that sense something "better" than their predecessors, and "better" usually translates as lower cost for equal or better performance.

This fact leads to one philosophy of integrating both circuits and sensors on the same chip. Since most sensors require some sort of signal conditioning and an eventual A/D conversion for later digital processing, this makes sense; however, this has proven quite challenging since the processes used to make sensors differ somewhat than the processes used to make circuits. There is also the issue of system partitioning – where does the sensor start and the circuit begin? Do they reside on the same substrate or are they uniquely packaged and separated for modularity and simplicity? The answer lies in the appropriate application of the sensor in the environment it is intended for, and in the eventual cost/performance of the sensor based on the technology chosen. In either case, whether packaging or integration is the solution for future sensors, one thing is clear. They both must try to utilize manufacturing techniques and processes common to mass-market semiconductor chips, else the price of these sensors will be too high to enable them to be used more frequently in products.

1.2 Sense Techniques

It has been shown that a variety of sensing techniques can be used to measure force, displacement, and other basic parameters that change with different stimuli. One of the

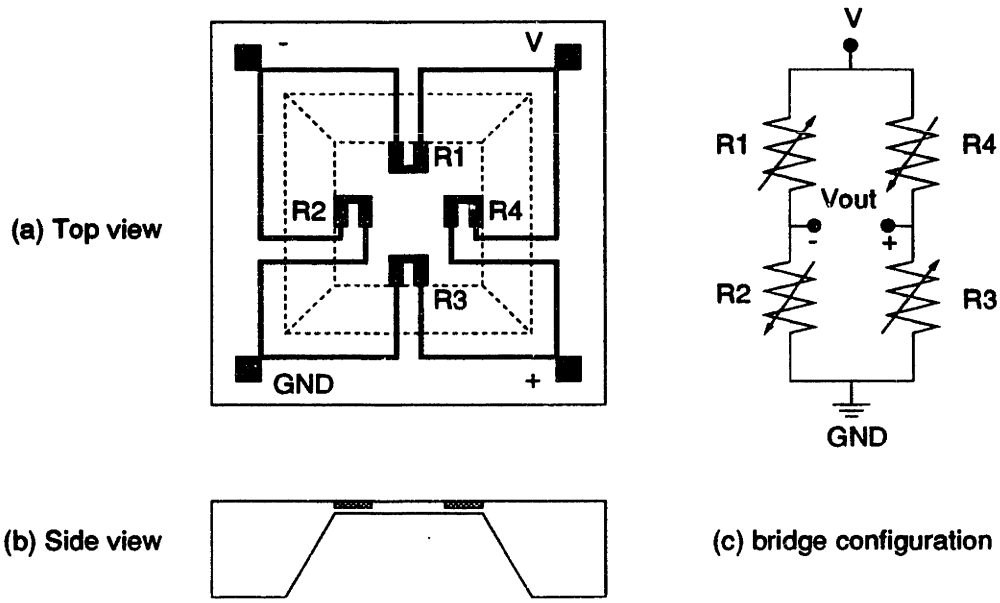
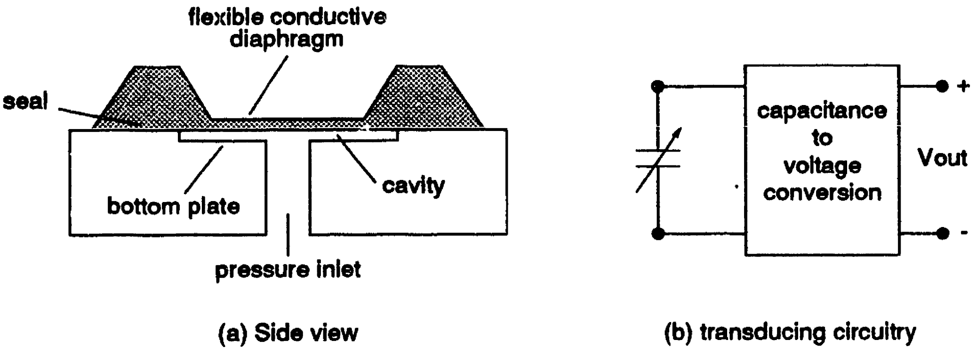

(a) Top view
(b) Side view
(c) bridge configuration

Figure 1.1: Typical piezoresistive pressure sensor configuration: (a) top view of a movable diaphragm with piezoresistors embedded in it; (b) side view of the diaphragm, and (c) Wheatstone bridge configuration for sensing with voltage output.

earliest techniques used to measure stress was the use of the piezoresistor. A typical configuration is shown in Figure 1.1 where 4 piezoresistors are placed on a diaphragm that is free to move in response to external pressure [4]. They are placed in stress concentration points for better sensitivity. A pressure load stresses the diaphragm, causing a change in resistance in the piezoresistors and thus a voltage change in the Wheatstone-bridge configuration. This is by far the most common configuration for piezoresistive-type pressure sensors, and is widely exploited in the silicon or polycrystalline silicon pressure sensor [4], [5],[6],[7], [8], [9]. Piezoresistive techniques are attractive since this type of transduction is relatively parasitic insensitive compared with traditional integrated circuits [9]. However, these resistors suffer from long-term drift and temperature dependencies which need either careful material characterization or circuit design for proper compensation, although not necessarily implemented on-chip [4],[5],[10]. Although their processing is easy compared to IC manufacture, they can be incompatible with conventional IC circuit fabrication and do not support active devices/interconnect on a VLSI scale. Nevertheless, these sensors are widely produced and packaged together with supporting circuit chips for signal conditioning, or with on-chip conditioning. Their cost, however, is still not as low as $5 per part as would be required in many mass-produced products such as automobiles. It should be pointed out, however, that this cost is dominated by the packaging used in many of these sensors.

Another sense technique widely exploited is the use of capacitance differences in sensing the parameter of interest. This has shown to be more sensitive and less dependent on temperature [6],[11],[12]. However, it is not as widely used for pressure sensing since it requires two plates and a narrow gap for the mechanical structure as opposed to a single deflecting mechanical structure and piezoresistors. The capacitive technique also needs conducting surfaces and sophisticated circuitry to convert the capacitance change into a voltage or current (Figure 1.2). This type of transduction can be sensitive to parasitics depending on the circuitry used [9],[13],[14]. These place constraints on what type of mechanical structures can be built. Nevertheless, many interesting structures have been built using a wide variety of methods that include bulk etching and wafer-bonding, anodic bonding to glass, or surface micromachining [15],[16],[17],[18],[19],[20], [21],[22],[23], [24]. As these structures are difficult to build, they usually do not incorporate active devices or circuits due to incompatibility with IC processing and manufacturing. They also are limited by the particular detection circuit chosen since this usually places a constraint on the minimum capacitance and resolvable change needed. For most sensors today, this capacitance is on the order of a few picofarads or larger with no better than 0.1 % accuracy. This causes most mechanical structures utilizing capacitance detection to be much larger than needed.

Other sense techniques involving resonant structures [25],[26] and optical techniques [27] offer exciting possibilities, but their fabrication and complexity may limit their cost-



(a) Side view

(b) transducing circuitry

Figure 1.2: Typical variable-gap capacitive pressure transducer : (a) side view and (b) capacitance transduction.

effectiveness. However, they are nonetheless important because the potential for these technologies is large.

In general, the capacitive technique is more robust in theory than the piezoresistive technique since the connection between stimuli and capacitance change is a more well-understood one than one involving a resistance change due to stress. Changes in dielectric constant can also be sensed using the capacitive technique, whereas the piezoresistive technique is limited to measuring changes in resistance due to stress only. However, the piezoresistive technique allows simpler mechanical structures, parasitic insensitivity, and simpler circuitry for voltage conversion. For both techniques, packaging is a major concern and must be addressed early in the design. For example, in both the piezoresistive and capacitive pressure sensor, provisions for pressure inlets and reference pressure cavities (for either absolute or gage pressure) must be made. In practice, because piezoresistive-type sensors are simpler to make than their capacitive counterparts, they have been more popular [9]. But their inherent *theoretical* limitations may defer to capacitive sensors in the future.

1.3 Capacitance Transduction

In 1987, [28] demonstrated a circuit architecture that enabled detection of changes in capacitance in fixed capacitors that were 26 fF in size (two orders of magnitude smaller than most capacitive sensor structures) in the presence of intentionally placed parasitics that were two orders of magnitude *larger*. The resolution was easily within the resolution limit of the A/D converter embedded in the topology (12-bits) and showed consistent results after testing the same chip years apart. Although certain offsets changed over time, the system was able to calibrate these out and measure only the change in capacitance of the on-chip structures.

This thesis deals with the logical extension of the previous work on this capacitive detection technique and primarily focuses on several ideas :

1. The use of the capacitive sensing technique for transduction.
2. The use of the digital capacitive readout with improved noise cancellation.
3. The integration of sensor and circuit in such a manner that conventional MOS processing can be utilized for most of the steps.
4. Simplified packaging for easy testing of a prototype pressure sensor.
5. Process integration within a standard laboratory.

The first item is an important one since it exhibits characteristics desirable in sensors (high sensitivity and potentially low temperature dependence). At the same time, the ability of the digital capacitive difference detection technique [28] relaxes the constraint of minimum capacitance and this translates to smaller sense structures – structures on the order of the size of analog MOS transistors. This encourages integration since both sensor and circuit are of the same physical size, and could be made of similar elements. Also, with such small capacitances, active circuits must accompany the sensor structure to adequately detect small capacitive changes. All of these elements combine to form the integrated capacitive pressure sensor that forms the research test vehicle for the ideas outlined above. Within this research vehicle, efforts are also made to make the fabrication both safe and compatible within a standard research laboratory, and testing simple and reproducible.

This thesis consists of six chapters. Chapter 2 deals with the theoretical background of the capacitance difference detection, the architecture implemented to test capacitive sensors, and some of its limitations. Chapter 3 covers the fabrication issues associated with a capacitive pressure sensor. This includes the process flow as well as alternative fabrication methods, process integration issues, etch techniques, compatibility with existing processes and safety concerns, ease of packaging, and integration with the circuit architecture. This leads into Chapter 4 covering the circuit design of the on-chip electronics in the pressure sensor test chip, and how they are designed with the measurement system and mechanical structure in mind. Chapter 5 covers the experimental results, which details measured results in all stages of work. Included here also are capacitive and optical deflection data from a working pressure sensor correlated with finite-element modeling analysis. Finally, the last chapter discusses some conclusions and future trends.

Chapter 2

Capacitance Difference Measurement

> *Although this may seem a paradox, all exact science is dominated by the idea of approximation.*
>
> RUSSELL

2.1 Capacitive Sensing

It has been shown that capacitive detection is more sensitive than piezoresistive detection, and less temperature dependent [6],[11],[12]. This advantage is obscured however, by the difficulty in fabricating capacitor plates separated by a small gap, and in the increased circuit complexity needed to realize the detection. On the fabrication side, designing a smaller gap yields larger capacitances and allows thinner sacrificial films to be used (these are removed to form the gap), but with a small gap, large area plates may stick to each other after formation. Designing larger gaps is also difficult since thicker sacrificial film depositions may not be possible, and the reduced capacitance may be too small for the detection scheme to accommodate. On the circuit side, increased capacitance is desired due to the presence of parasitics (and reduction of kT/C noise), but this causes the mechanical structure to be larger, or with too small a maintainable gap.

The tradeoffs involved in using capacitance transduction for sensors involve the coupling of the circuit's ability to transduce capacitance with the physical size and shape of the structure which determines the capacitance. Due to these tradeoffs, it is difficult to fabricate a sensor using the capacitive technique, and the predominant sensing mechanism in most sensors today that measure deflection of a structure (due to pressure for example) are piezoresistive.

There are a variety of capacitive detection circuit topologies available [14],[15],[16], [19],[21],[22],[23], [29], [30],[31], [32],[33],[34],[35], [36], [37];however, most need complicated on-chip electronics, or do not provide adequate accuracy and sensitivity in the 100 femtofarad range in the presence of large parasitic capacitances. In addition, many do not provide a digital output, instead providing an analog output that it is digitized later. Others provide a frequency output which must be converted to an analog DC value and then digitized. Due to the nature of their performance limits and physical size, they are usually implemented side-by-side with circuit chips, and hence do not represent sensor and circuit integration on the chip-level, but rather at the package-level. The switched-capacitor sense technique [13],[14] circumvents some of these problems but still does not address the problems of charge-injection errors for small capacitive structures or high accuracy and sampling speed. This chapter will discuss in detail the charge-redistribution capacitance difference detection method which overcomes many of these problems and limitations, making the capacitive sense technique competitive to the piezoresistive sense technique.

2.2 Charge-Redistribution Capacitive Detection

Shown in Figure 2.1 is the block diagram for the architecture of the successive approximation difference detection system which can circumvent some of the tradeoffs between detection circuitry and sensor size [28]. The system consists of two major components. The first must be implemented monolithically since it handles very small signals (charge) : a sense and reference capacitor set (C_R and C_S), MOS switches S1-S3, coupling capacitor C_C, and a preamplifier that serves as a front-end to a more sensitive voltage comparator. The second component involves a successive approximation A/D converter which includes a voltage comparator, successive approximation register (SAR), a digital to analog converter (DAC), and control logic/memory for control of the components and storage of the data. The non-ideal components of the diagram include the parasitic capacitance to ground, C_P, the input offset V_{os} of the on-chip preamplifier, and the charge injection Q_{inj} from the NMOS switch S3.

In this block diagram, the architecture is modularized into discrete sections for simplicity of understanding. They could, in reality, be integrated together monolithically. In this case, certain interface stages (such as the preamp/comparator) could be merged.

This section discusses the qualitative concepts behind the charge-redistribution technique for capacitive sensing, and how different switching sequences of switch S1, S2, and S3 can be used to obtain different noise reductions while obtaining a voltage which is proportional to the difference of C_R and C_S. This is followed by a more quantitative discussion of the switching sequences.

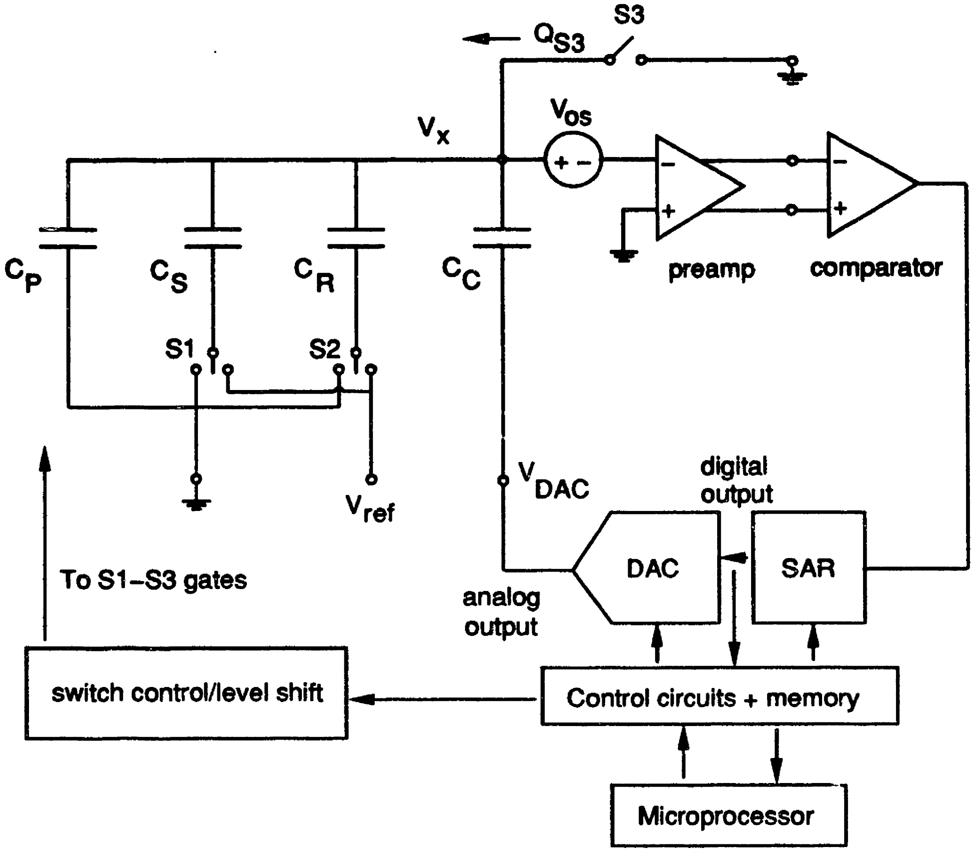


Figure 2.1: Open-loop charge-redistribution topology.

2.2.1 Charge Measurement

The basic concept in charge-redistribution capacitive sensing is to sample a certain fixed amount of charge on one capacitor and redistribute that charge on another capacitor. This can be illustrated by referring to Figure 2.1.

The sequence begins by grounding all capacitors using switches S1, S2, and S3, and applying ground through the DAC to C_C. Subsequently, capacitor C_S is charged to a reference voltage by switch S1 while C_R is discharged by switch S2, and S3 is connected to ground. This draws an amount of charge of $-V_{ref}C_S$ to node V_x. The next sequence involves opening switch S3 to isolate this charge. At the same time, this injects channel charge from the NMOS transistor that is used as switch S3.

A successive approximation register and digital-to-analog converter is used in a feedback loop to obtain a voltage $V_{DAC_{cal}}$ at C_C which nulls the voltage at V_x to V_{os}. This voltage is dependent on the value of the charge isolated on the node and the offset of the preamp (V_{os}), and is given by

$$V_{DAC_{cal}} = V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C},$$

where C_T is the total capacitance on the node V_x and Q_{inj} is the injected charge from S3. There are several different switching sequences from this point that can be used to make the capacitive difference measurement, and they will be qualitatively discussed.

2.2.2 Capacitive Measurement With Analog Error Cancellation

Once $V_{DAC_{cal}}$ is known, it can be stored (since it exists in digital form from the SAR) and used as a reference. Switch S3 is closed again, a reference voltage applied to C_S, C_R grounded, and $-V_{DAC_{cal}}$ applied from the DAC to C_C rather than ground. When switch S3 is opened again, it will inject a channel charge. Switches S1 and S2 are reversed, and the SAR/DAC feedback loop is initiated to obtain a voltage ($V_{DAC_{meas}}$) which again tries to null V_x to V_{os}. Because the switches S1 and S2 are reversed (charging C_R and discharging C_S), the isolated charge is redistributed among the capacitors in such a way that any difference between C_S and C_R manifests itself as a voltage proportional to their difference at the DAC output which is the desired result :

$$V_{DAC_{meas}} = V_{ref}\left[\frac{C_S - C_R}{C_C}\right].$$

A way of viewing this result is that due to symmetry, if $C_R = C_S$, then the initial charge on the sense capacitor will redistribute entirely to the reference capacitor, and the voltage at V_x will be only due to the charge sampled on the capacitors when switch S3 is opened. If $C_R \neq C_S$, then the voltage at V_x becomes non-zero and is captured by the A/D conversion. The application of $-V_{DAC_{cal}}$ before switch S3 is opened achieves an *analog subtraction* at V_x which subtracts out $V_{DAC_{cal}}$, the effects of charge injection, and offset.

2.2.3 Capacitive Measurement With Digital Error Cancellation

The analog error cancellation can reduce effects of charge injection and $1/f$ noise (evident in V_{os}), but cannot reduce thermal noise effects from switch S3. Another method can be used to cancel the thermal noise effects of this switch as well as the charge injection error, and this will be qualitatively explained here.

The voltage $V_{DAC_{cal}}$ is a sampling of the charge injection from switch S3 and also broadband noise. Rather than perform a subtraction in the analog domain, the switch can be left open after measurement of $V_{DAC_{cal}}$, switches S1 and S2 reversed, and the SAR/DAC initialized to make another measurement immediately after. This value obtained is given by

$$V_{DAC_{meas-d}} = V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C} - \frac{Q_{noise}}{C_C} + V_{ref}\left[\frac{C_S - C_R}{C_C}\right],$$

where Q_{inj} contains the charge injection from the MOS switch S3, Q_{noise} is the previously sampled broadband noise (kT/C noise), and $1/f$ noise embedded in V_{os}. Subtracting $V_{DAC_{cal}}$ from $V_{DAC_{meas-d}}$ cancels out the effects of Q_{inj}, Q_{noise}, and V_{os}, leaving $V_{DAC_{meas}}$. This is in effect correlated double sampling (CDS) and reduces $1/f$ noise and other slowly-varying noise components because it is assumed that these terms are correlated between the calibration and actual measurements. Note that the measurement immediately follows the calibration without resampling. For the charge injection and sampled broadband noise, they are sampled only once and *are identical between measurements*. Their effects are therefore canceled because the noise and charge injection form a sampled charge which is measured during calibration and subtracted from the measurement. Digital subtraction of $V_{DAC_{cal}}$ from $V_{DAC_{meas-d}}$ will yield $V_{DAC_{meas}}$ (the desired result) with a high reduction of charge injection, sampled noise, and $1/f$ noise, but will not reduce the direct broadband noise sources from switches S1 and S2, preamp, the DAC. The latter noise sources as well as quantization error will determine how much the sampled noise and $1/f$ noise get reduced. These are discussed at the end of the chapter.

2.3 Detailed Switching Sequences

There are two modes of operation within the architecture, and they will be explained quantitatively in the next few sections. They comprise different switching sequences of S1-S3 and different manipulations of the real-time data for noise and offset cancellations. The first mode discusses an analog method for subtracting out measurement errors, and the second mode details an all digital technique for cancellation of measurement errors and noise sources. Generalization to a closed-loop, continuous-time topology is briefly introduced after the analog mode is detailed. Errors associated with noise and quantization errors are treated after the switching sequences are detailed.

2.3.1 Analog Subtraction Error Cancellation

The method demonstrated in 1987 by [28] used a method for calibrating out the offsets and charge injection errors that relied on analog subtraction. This method is explained in detail here.

Measurement of Non-Idealities

The first step in measuring accurately the difference in capacitances between C_S and C_R relies on properly eliminating the non-ideal effects such as offsets and charge injection. These represent charges or voltage effects that are not a function of the difference in the capacitance changes incurred during sensing, and hence represent an error in the measurement. This section discusses how this is accomplished.

The switching sequence starts by grounding all capacitors. This means that S1 and S2 direct the bottom plates of the sense and reference capacitors to ground, and switch S3 is closed. Also, the DAC output which is connected to C_C is also set to ground, although there is an error here of $\pm\frac{1}{2}$LSB due to the resolution limit of the DAC. This condition is the idle state of the system before any measurement begins.

The next step is to charge up C_S to the reference voltage by switching S1 to V_{ref}. This will draw a charge $-V_{ref}C_S$ on the capacitive node V_x. After this is achieved, switch S3 is opened, injecting a certain amount of undesired channel charge (Q_{inj}) onto the floating node. The total charge on the top capacitor plates is now

$$Q = -V_{ref}C_S + Q_{inj} \tag{2.1}$$

where Q_{inj} is the injected charge. This charge injected on the floating node causes a change in the voltage V_x which was originally 0 V due to the grounding action of S3.

At this point, the A/D conversion cycle is started with a signal sent from the control circuits to the successive approximation register (SAR). The goal of the external circuitry to is find a voltage that can be applied to C_C such that V_x becomes very close to the offset of the preamp, V_{os}. When the SAR begins, it outputs a digital code which represents a voltage value close to 0 V. When this code is applied to the DAC, it produces an analog value of 0 V and this is applied to C_C. The voltage V_x changes in response to this voltage since the charge on V_x is fixed and must redistribute itself in such a way so as to satisfy charge conservation. Since V_{DAC} was at 0 V initially, the first cycle of the A/D conversion does not change V_x and the preamp compares this voltage to ground, and this value is passed on to a fast, sensitive voltage comparator off-chip. Its digital output is relayed back to the SAR, and the successive approximation continues.

The voltage at the output of the DAC after the successive approximation search can be calculated by assuming that $V_x = V_{os}$ and that charge is conserved. The total charge on the capacitors should be the same as in Eq. (2.1),

$$\begin{aligned} Q &= -V_{ref}C_S + Q_{inj} \\ &= V_{os}(C_P + C_S + C_R + C_C) - V_{ref}C_S - V_{DAC}C_C. \end{aligned}$$

Solving for V_{DAC} and ignoring quantization error yields

$$V_{DAC} = V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C} = V_{DAC_{cal}} \tag{2.2}$$

where C_T is the total capacitance on the node V_x. When S3 is closed, it is connected to ground so that the NMOS transistor is in the linear region. The channel charge is negative and approximately given by the expression,

$$Q_{channel} = -WL_{eff}(V_{gs} - V_T)C'_{ox},$$

and the injected charge is

$$Q_{inj} = -\alpha WL_{eff}(V_{gs} - V_T)C'_{ox} - C_{gs0}WV_{gs}, \tag{2.3}$$

where

α = fraction of channel charge injected

W = MOS switch width

L_{eff} = effective channel length

V_{gs} = gate-to-source turn-on voltage

V_T = threshold voltage

C'_{ox} = gate oxide capacitance per unit area

C_{gs0} = gate-to-source overlap capacitance per unit length.

Ignoring the quantization error of the DAC and substituting Eq. (2.3) into Eq. (2.2) yields,

$$V_{DAC_{cal}} = W\left[\frac{\alpha L_{eff} C'_{ox} + C_{gs0}}{C_C}\right] V_{gs} + \frac{V_{os} C_T - \alpha W L_{eff} C'_{ox} V_T}{C_C}. \tag{2.4}$$

where the equation has been arranged as a function of V_{gs} indicating a gain and offset-like behavior. The initial charge on C_S was inconsequential since it existed before and after the measurement, and hence cancels out. The switching sequence is performed in this way, however, since it is crucial to measure the value of the offset and charge injection (as the measurement does by Eq. (2.2)) in the same configuration (and hence the same impedance as observed by switch S3) as when we actually make the measurement of the difference in C_R and C_S.

Once this value of charge injection and offset have been measured, it can be averaged over many switch openings/closings to reduce the sampled thermal noise and fluctuations in the exact percentage of channel charge injected. Thermal noise is white noise with a normal distribution for the instantaneous amplitude, and an average value of zero [38]. Averaging $V_{DAC_{cal}}$ can significantly reduce this noise, and can be used to obtain a relatively noise-free value for the charge injection and offset terms. This value can be stored for future reference.

2.3.2 Measurement of Capacitive Difference

Once the measurement of $V_{DAC_{cal}}$ has been made, averaged, and stored, the measurement of the capacitive difference between C_R and C_S can be made. S1 is switched so that C_S is charged to V_{ref}. The next step is to switch the output of the DAC from 0 V to $-V_{DAC_{cal}}$. This can be done through the DAC since the value of $V_{DAC_{cal}}$ obtained previously is stored in digital form, and can be easily inverted. The charge on the node V_x is

$$\begin{aligned} Q &= -V_{ref}C_S + V_{DAC_{cal}}C_C \\ &= -V_{ref}C_S + V_{os}C_T - Q_{inj}. \end{aligned}$$

Switch S3 is then opened, injecting charge of approximately Q_{inj}, followed by the reversal of S1 and S2 such that the bottom plate of C_S is grounded while the bottom plate of C_R is switched to V_{ref}.

The A/D conversion cycle is then initiated, bringing V_x close to V_{os} by a successive approximation search as before. Using the same analysis as before and assuming charge conservation during the time that S3 is opened, the charge before and after the measurement are equal. The charge on the capacitors right after switch S3 is opened and before S1 and S2 are switched is

$$\begin{aligned} Q &= (-V_{ref}C_S + V_{os}C_T - Q_{inj}) + Q_{inj}. \\ &= -V_{ref}C_S + V_{os}C_T \end{aligned}$$

The charge injection term cancels because the applied voltage initially at C_C is different from 0, and this voltage is just enough to cancel the effect of Q_{inj}.

Assuming charge conservation and calculating the charge after A/D conversion while assuming that V_{DAC} has forced $V_x = V_{os}$, then the charge after A/D conversion is the same before A/D conversion, and hence

$$\begin{aligned} Q &= V_{os}C_T - V_{ref}C_R - V_{DAC}C_C \\ &= -V_{ref}C_S + V_{os}C_T. \end{aligned}$$

Solving for V_{DAC} yields

$$V_{DAC_{meas}} = V_{ref}\left[\frac{C_S - C_R}{C_C}\right]. \tag{2.5}$$

This is the central result. It indicates that the DAC voltage that is used to bring $V_x = V_{os}$ is a voltage that is strictly proportional to the difference in C_R and C_S only. The initial measurement of $V_{DAC_{cal}}$ allows the cancellation of the charge injection and preamp offset terms when the measurement is made. In Eq. (2.5), parasitic capacitances to ground do not affect the measurement because C_P is always present as a source or sink for charge before and after S3 is opened. The charge on the parasitic capacitance represents a reference charge value that always is returned to its initial value. However, too large a parasitic capacitance will pin V_x and not allow any control via C_C so there is a maximum allowable parasitic.

An intuitive description of what is happening is as follows. A certain fixed amount of charge is placed on one capacitor which is based solely on the value of the capacitor since the reference voltage is fixed. That charge is isolated and allowed to redistribute itself on other capacitors. If $C_R = C_S$, then the charge initially gathered on C_S would redistribute itself entirely to C_R (due to symmetry of the switching), and hence there would be no voltage change at V_x. However, if $C_R \neq C_S$, the charge will redistribute itself on the capacitors in such a way that so that it satisfies charge conservation and the fact that a feedback mechanism is used to force $V_x = V_{os}$.

It is important to note that this architecture can also be implemented in a continuous-time feedback topology whereby the A/D loop is replaced by a wire, the preamp/comparator combination replaced by a high-gain, unity-stable op-amp, with S3 connected to its output. This is shown in Figure 2.2. In this configuration, the same analysis applies, except that the voltage offset is automatically canceled since when S3 is closed, the op-amp operates in unity gain, and the reference voltage at V_x becomes $V_{os}A/(1+A)$, or virtual ground. This topology is similar to a switched-capacitor integrator architecture, and has been utilized in capacitive sensors [14]. However, it suffers from several drawbacks. Although offset and charge cancellation are possible, the op-amp requirements are stringent if more than 8-bit accuracy at high speed is required. This is because the op-amp must settle very fast before any A/D conversion is done. Presently, capacitors on the order of 10 picofarads are used in this architecture, with no charge cancellation (in the form described here) and a slow sampling speed [14]. It is unclear whether this implementation of this topology can be used to measure small capacitive changes in small capacitors at greater than 12 bit accuracy (because of a lack of good charge cancellation), and at speeds higher than 20 kHz (because of op-amp constraints).

The analog subtraction algorithm described in this section is sufficient to bring the level of noise below the 12-bit level when measuring sub-100 fF capacitors only after extensive averaging of the data [39]. It only cancels out to first order the charge injection, but not the thermal noise which causes a variation in the charge injection. The effects of quantization error and thermal noise will be discussed at the end of the chapter.

2.3.3 Digital Subtraction Error Cancellation

There are two digital methods for canceling out charge injection and preamp offset in the measurement, and they will be described here. The first involves partial error cancellation, while the other offers full cancellation of the error terms and noise.

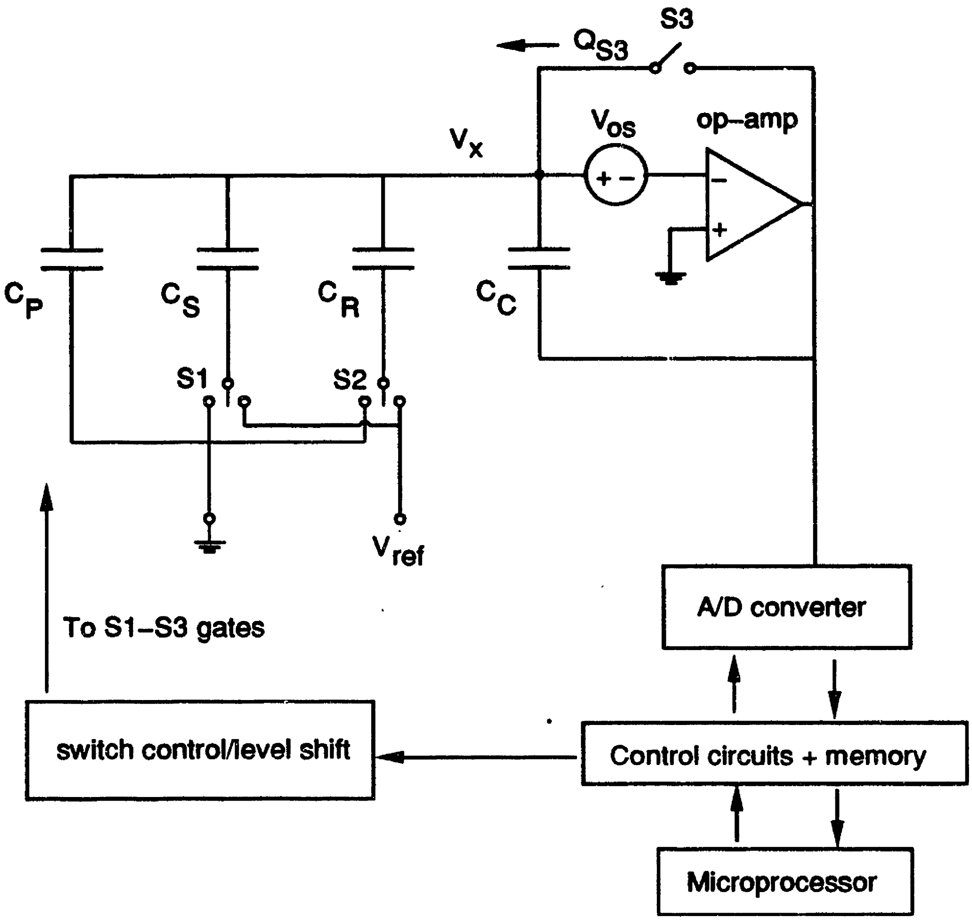


Figure 2.2: Closed-loop charge-redistribution topology.

Digital Error Cancellation

This method involves a switching sequence identical to the analog subtraction method mentioned earlier, except that the negative of the calibration voltage $V_{DAC_{cal}}$ is not applied back to C_C but rather is digitally subtracted from the measurement. This yields essentially the same results as the analog subtraction method, but has the advantage of subtraction in the digital domain with no added quantization error from the DAC due to reapplication of $-V_{DAC_{cal}}$ to C_C. This is only true, however, if the $-V_{DAC_{cal}}$ is an averaged value. It may suffer from potential overflow problems since if $V_{DAC_{cal}}$ is large, it may cover the entire full-scale range of the DAC. In the analog subtraction case, this value is subtracted out *before A/D conversion* and hence the full-scale range of the DAC can be used for the measurement of $C_R - C_S$. In the digital subtraction case, this is not possible since subtraction is performed *after A/D conversion* and hence if $V_{DAC_{cal}}$ is large, this may leave little dynamic range for the measurement if the error is large. However, for most of the capacitors and switches used in this study, it was found that $V_{DAC_{cal}}$ takes up at most 10% of the full-scale of the DAC, and this leaves more than enough range for the measurement. Hence the advantage of this technique outweighs the disadvantages when compared to the analog subtraction method.

Digital Error And Noise Cancellation

The final method to be discussed here is the most accurate without the need for averaging. The switching sequence begins as in all the methods by starting in the idle state whereby all capacitors are grounded. This means that S1-S3 are all connected to ground, and V_{DAC} is set to ground. The next step involves switching S1 to V_{ref} and grounding S3. This samples a certain amount of charge on C_S that varies with the size of C_S since V_{ref} is constant. Switch S3 is then opened, injecting an amount of charge Q_{inj} on the node. The total charge on the node is then :

$$Q = -V_{ref}C_S + Q_{inj},$$

where Q_{inj} is a negative quantity. An A/D conversion sequence is initiated, whereby V_{DAC} is found to null the voltage V_x close to V_{os}. After the A/D conversion, the charge on the node V_x should not have changed from before (assuming charge conservation), and hence

$$\begin{aligned} Q &= -V_{ref}C_S + Q_{inj} \\ &= V_{os}(C_P + C_S + C_R + C_C) - V_{ref}C_S - V_{DAC}C_C. \end{aligned}$$

Solving for V_{DAC} yields

$$V_{DAC} = V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C} = V_{DAC_{cal}} \tag{2.6}$$

which is the identical sequence and value obtained before (Eq. (2.2)) in the analog subtraction/cancellation method. The major difference is that this value is not averaged or subtracted later, but rather subtracted digitally right after the measurement is made *while switch S3 is still open.* There is no second sampling of the signal as in other correlated multi-sampling analog or digital techniques. The charge on the capacitors is only sampled once, but is measured *twice* in such a way that different components can be discerned.

This value $V_{DAC_{cal}}$ is stored digitally in a register. The next switching sequence involves reversing the positions of S1 and S2 so that C_S is grounded while C_R has V_{ref} applied. The charge is allowed to redistribute itself, and another A/D conversion is initiated. The key thing to note is that S3 remains open during both A/D conversion cycles. Following a similar analysis for finding the value V_{DAC} yields :

$$\begin{aligned} Q &= -V_{ref}C_S + Q_{inj} \\ &= V_{os}(C_P + C_S + C_R + C_C) - V_{ref}C_R - V_{DAC}C_C, \end{aligned}$$

and solving for V_{DAC} yields

$$\begin{aligned} V_{DAC_{meas}} &= V_{ref}\left[\frac{C_S - C_R}{C_C}\right] + V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C} \\ &= V_{ref}\left[\frac{C_S - C_R}{C_C}\right] + V_{DAC_{cal}}. \end{aligned}$$

The most important part of this equation is the fact that both A/D conversions have captured the injected charge Q_{inj} *twice*, and assuming that the conversions are spaced reasonably close together in time, the charge in both cases should be very close (assuming no large leakage, polarization, or transistor hysteresis effects), and hence the charge injection and preamp offset can be canceled out almost completely, leaving the term

$$V_{DAC_{meas}} = V_{ref}\left[\frac{C_S - C_R}{C_C}\right] \tag{2.7}$$

which is the desired result – a voltage proportional to the difference in two capacitors.

2.4 Noise and Error Sources

2.4.1 Quantization Error

In the previous analyses, the DAC was assumed to be perfect, yielding a voltage value which perfectly nulled the voltage V_x to a voltage equal to V_{os}. In reality, this is not possible since the DAC output is quantized, yielding a quantization error.

Each time the DAC is used, it produces a error of $\pm\frac{1}{2}$LSB. This means that the DAC can only get within $\pm\frac{1}{2}$LSB of the true voltage needed to null V_x to V_{os}. In the analog subtraction algorithm, the DAC is used 4 times : grounding C_C before the calibration sequence begins, obtaining $V_{DAC_{cal}}$, reapplying $-V_{DAC_{cal}}$ to C_C, and obtaining $V_{DAC_{meas}}$. This means that in the worst case, the measurement voltage will be in error ±2 LSB, although the central limit theorem indicates that the error is usually smaller.

The digital algorithm has the advantage that the DAC is used only three times – once for grounding C_C, once when obtaining $V_{DAC_{cal}}$, and once when obtaining $V_{DAC_{meas}}$. This means a worst case error of ±1.5 LSB, with a smaller typical value dictated by the central limit theorem.

Errors such as differential non-linearity (DNL is the deviation of the step size when changing the LSB to the ideal step of full-scale/2^n), and integral non-linearity (INL is the deviation of the output from what it should be given no DNL, or can be viewed as the summation of the DNL up to a particular code) can affect the measurement during A/D conversion. They make the quantization error of the DAC dependent on the output code rather than being a constant.

2.4.2 Thermal and $1/f$ Noise

Thermal noise appears predominately in three places : the resistance of of the NMOS devices used in S1-S3, the preamplifier, and the DAC output. $1/f$ noise manifests itself in the V_{os} term due to the input transistors of the preamplifier. The NMOS switch is a resistor with a power spectral density (PSD) given by

$$S_R(f) = \frac{\overline{v_{nR}^2}}{\Delta f} = 4(kT)R_{on}$$

where $\overline{v_{nR}^2}$ is the mean square of the noise voltage in the frequency range Δf, k is Boltzmann's constant, R_{on} is the on-resistance of the MOS transistor, and T is the absolute temperature [40].

The preamplifier input contains MOSFETs, and this embodies both thermal noise and flicker $1/f$ noise which can be referred to the input of the preamp. The flicker noise of the MOSFET is given by

$$S_f(f) = \frac{\overline{v_{nf}^2}}{\Delta f} = \frac{K}{C_{ox}^2 WLf}.$$

where C_{ox} is the oxide capacitance per unit area, WL is the area of the gate, and K is a parameter dependent on temperature and the process [41]. The noise generated in the preamplifier (implemented as a MOS op-amp since it must have very low input currents to reduce charge leakage) is dominated from the input devices, and its spectrum has the same general shape, with the $1/f$ component having a corner frequency (f_{cr}) typically from 1 - 50 kHz [40].

The DAC contains a current output converter and a current-to-voltage converter consisting of resistors and an op-amp, and thus broadband noise can emanate from this component.

When the calibration voltage measurement begins, the noise sources apparent are the thermal noise in the NMOS switches S1-S3, the broadband noise at the output of the DAC (with an output of 0, disregarding quantization error), and the input-referred noise of the preamp. It is assumed that the flicker noise inherent in V_{os} is a slow process compared to the sampling frequency, and can be treated as an offset. The power spectral density for the thermal noise due to S3 is filtered by a low-pass RC filter comprising the equivalent on-resistance of the MOS transistor and the total capacitance, C_T. The power spectral density across the capacitor is [40]

$$S(f) = S_R(f)|\frac{1}{1 + j\omega R_{on}C}|^2 = \frac{4kTR_{on}}{1 + (2\pi f R_{on}C)^2}.$$

The root mean square voltage for all frequencies is

$$\overline{v^2} = \int_0^\infty S(f)\, df = \frac{4kTR_{on}}{2\pi}\int_0^\infty \frac{d\omega}{1 + \omega^2(R_{on}C)^2},$$

and the integral gives $\pi/2R_{on}C$. This yields the familiar result that the noise power is

$$\overline{v_R^2} = \frac{kT}{C}.$$

When switch S3 turns off, the variance of the sampled noise on the capacitors is the same as kT/C, which includes aliasing [42]. For all other noise sources, the noise power spectra referred to the voltage across C_T is more complicated than from switch S3, but will manifest itself as an rms voltage across C_T which is sampled when switch S3 is opened, and can be represented as sampled noise on node V_x.

When switch S3 is opened and the A/D conversion performed, the value at the DAC is

$$V_{DAC} = V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C} - \frac{Q_{noise}}{C_C} + V_{n1} \pm \frac{1}{2}\text{LSB},$$

where V_{os} is the offset of the preamp, Q_{inj} is the charge injection from the channel of S3, Q_{noise} is the sampled noise, and V_{n1} is the noise from the DAC. Also, there is a quantization error from the DAC of $\pm\frac{1}{2}$LSB.

To minimize the charge injection, S3 is made small, but large enough so that the RC time constant between the switch resistance and C_T is small enough to accommodate the sampling frequency. S1 and S2 are made arbitrarily large to reduce their on-resistances which reduces their thermal noise. With a small RC time constant, the broadband noise from S1 and S2 is limited by the preamp bandwidth. Also, a large C_P will attenuate the noise due to the capacitive divider from the noise sources to V_x. The charge injection from switches S1 and S2 is not an issue since they always connect the bottom plates of the capacitors to a fixed potential. For these reasons, switches S1 and S2 should be made as large as possible.

The value $V_{DAC_{cal}}$ is stored and while switch S3 *remains open*, switches S1 and S2 are reversed, and another A/D conversion is initiated. This is the measurement cycle A/D conversion. Crucial in the understanding of this step is that switch S3 remains open, and hence the sampled thermal noise due to this switch and other broadband sources which were sampled remain in the charge domain *unchanged as the noise in* Q_{noise}.

When the A/D conversion is completed for the measurement cycle, the value obtained is

$$V_{DAC_{meas}} = V_{os}\frac{C_T}{C_C} - \frac{Q_{inj}}{C_C} - \frac{Q_{noise}}{C_C} + V_{ref}\left[\frac{C_S - C_R}{C_C}\right] + V_{n2} \pm \frac{1}{2}\text{LSB}$$

where this re-measures the offset, charge injection, and sampled noise terms, and includes an additional term which is proportional to the difference in C_R and C_S as well as the DAC output noise. Subtraction of $V_{DAC_{cal}}$ from the above voltage cancels the effect of sampled noise (kT/C) from S3 and charge injection. It should be noted, however, that the subtraction effectively doubles the noise power due to the DAC and preamplifier because the sampling noise from these sources is uncorrelated with the noise present during the measurement.

This cancellation is exactly analogous to an offset-cancellation technique, while the $1/f$

noise evident in V_{os} (and other low-frequency noise sources) are reduced due to CDS since the $1/f$ corner frequency is much lower than the sampling frequency [40],[42].

Correlated double sampling introduces an operation of subtraction of offsets at times nT and $nT - T/2$, and the effect is a transfer function of $H_{CDS} = 1 - z^{-1/2}$ or in the frequency domain,

$$H_{CDS}(e^{j\omega T}) = 1 - e^{-j\omega T/2}$$

with the power spectral density of the noise is multiplied by

$$|H_{CDS}(e^{j\omega T})|^2 = 4\sin^2(\frac{\omega T}{4})$$

where $T/2$ is the time between the calibration and measurement. This suppresses the noise not only at DC but at low frequencies. CDS reduces $1/f$ noise because typically $f_{cr} < f_s$ [40].

In summary, the thermal noise due to switch S3 and all other broadband noise sources which were sampled on C_T are canceled because they are sampled once, yielding noise electrons which serve as a charge reference in the measurement, analogous to how an offset voltage serves as a reference in offset-cancellation. The $1/f$ and other slow noise processes get reduced by CDS, but the sampled, broadband noise sources in the preamplifier (they are effectively sampled by the A/D conversion) and the DAC do not get reduced, but rather, the noise power is doubled by uncorrelated sampling. Switches S1 and S2 should be made as large as possible to reduce their thermal noise contributions during the measurement.

The quantization error of the DAC causes a smaller reduction of noise since it can only approximate the voltage in any A/D measurement. This causes incomplete CDS reduction of noise from the the $1/f$ noise of the preamp and other low-frequency noise sources, and an incomplete cancellation of the charge injection and the broadband noise sampled on C_T.

The major error sources are broadband noise sources in the DAC and preamplifier which cannot be reduced by CDS, and the quantization error of the DAC which prevents an accurate measurement. Since the major part of the error in the measurement emanates from the charge injection, the technique reduces errors significantly, while reducing noise from switch S3 and low-frequency noise sources.

A convenient way of viewing the noise as it relates to resolution is that the all broadband noise sampled on C_T when switch S3 is opened plus the charge injection contributes to a reference charge. How well this sampled charge serves as a reference (and hence how well it can be canceled) depends on how well the A/D conversion can exactly measure it. This is dependent on the DAC quantization error and the direct broadband noise sources.

For the implemented chip, the estimated total capacitance is 1 pF, and at 300 K, the quantity kT/C has the mean square value 40×10^{-10} V^2, giving a rms noise voltage of 63 μV. The kT/C noise gets reduced by the digital subtraction of the calibration voltage from the measurement. The preamp has a simulated input-referred noise of 10 μV (over a 1 MHz bandwidth), while the output of the DAC has an rms noise of 10 μV, but gets attenuated when reflected to the preamp input by the ratio C_T/C_C. The quantization error of the DAC for a LSB for 16-bits on a 10 V full-scale is 153 μV. With the ratio of 10 for C_T/C_C, this voltage is 15.3 μV and is larger than the other noise sources. This indicates that the major contributions of error (as seen from the input of the preamp) are from the quantization error of the DAC and the preamp thermal noise. This assumes that thermal noise from switches S1 and S2 is low due to their small on-resistances.

The dominant noise sources establish how well the sampled noise components and charge injection get reduced because they determine how accurate a measurement is made and how well the offset-cancellation techniques work. The quantization error can be reduced by reducing the full-scale voltage of the DAC to allow the full dynamic range of the DAC to be used.

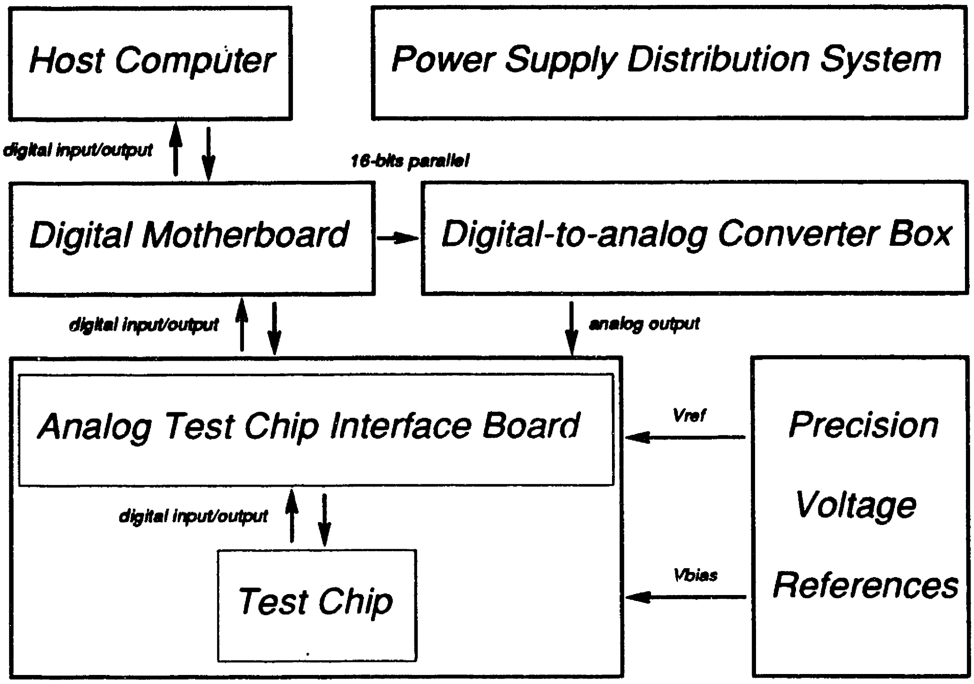


Figure 2.3: Capacitance measurement system block diagram.

2.5 Measurement System Partition and Design

To make the system general and non-application-specific, it was chosen to partition the system so that the sense, reference, and coupling capacitors, switches S1,S2,S3, and preamp are monolithic, with the rest off-chip and made with off-the-shelf components. This allows the system to test a wide variety of different sensor chips which follow the same architecture, but perhaps sense a different parameter.

The system in Figure 2.3 consists of 6 parts: the host computer, a digital board, analog test board, power supply distribution system, digital-to-analog converter, and reference voltage supplies. Details of this measurement system are contained in Appendix A.

Chapter 3

Sensor Design and Fabrication

Everything should be made as simple as possible, but no simpler.

EINSTEIN

3.1 Air-Gap Capacitor Structure

The research vehicle for testing the charge-redistribution sense technique is a variable air-gap capacitor fabricated on-chip with circuits. The air-gap capacitor is designed so that it can be used to detect changes in differential pressure, and hence be used as a gage pressure sensor in testing.

The air-gap structure is shown in Figure 3.1. It consists of a top plate separated by a small air-gap and a bottom plate which has an inlet hole for pressurized gas. This gas deflects the top plate upward, increasing the gap, and hence decreasing the capacitance. MOS electronics are also integrated with the structure.

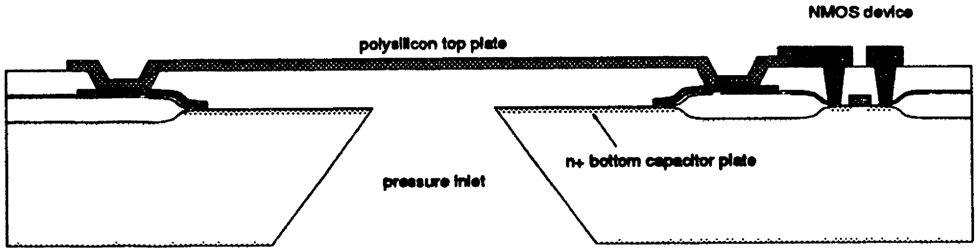


Figure 3.1: Process cross section for the air-gap capacitor structure and an NMOS device.

3.2 Air-Gap Capacitor Integration

The air-gap capacitor is designed in a process which allows integration with an existing NMOS or CMOS process. Initial research revealed that polysilicon used as the top plate would suffice since it is both rigid, conductive, and readily available in a MOS process. Many interesting structures have already been demonstrated using this material [43]. In addition, the fabrication of such a structure does not need wafer or anodic bonding techniques, which reduces the number of critical steps. It does, however, require back-to-front infra-red alignment to create the pressure inlet hole, but this photolithographic step will turn out to be non-critical, although the creation of the hole is critical.

Because of difficulties in protecting circuits and interconnect from the corrosive sacrificial etches used in surface micromachining and also due to the problem of sealing cavities formed after such etches, it was chosen to fabricate the air-gap capacitor using a combination of surface and bulk micromachining. Surface micromachining is used to underetch a sacrificial layer, but through a hole through the substrate formed using bulk micromachining. Surface micromachining enables easier integration with circuits while bulk micromachining provides better packaging options.

3.2.1 Fabrication Sequence Methodologies

There are three methodologies for integrating the mechanical structures with circuits :

1. Fabricate the air-gap capacitor *before* the circuits.
2. Fabricate the air-gap capacitor *after* the circuits.
3. Merge the two into one fabrication sequence with many shared steps.

If the sensor structure is to be made first, the advantages would be that all high-temperature processing could be achieved without affecting the devices (which are not yet formed, although epi-layers in CMOS wafers might move). Also, any critical alignment could be done by circuit-to-sensor alignment rather than vice versa. In the structure shown in Figure 3.1 this means that the hole would be formed first, and the circuits on the front-side would align to it, thus saving an IR alignment step needed if the converse were true. However, disadvantages to this process sequence is that the sensor must be able to withstand all subsequent circuit processing steps which include resist spin-on, diffusions, wet and dry plasma etching, and wafer handling. If the structure is delicate, or contains accessible cavities, it will not be possible to perform photolithography on them since resist would flow into such places and disturb the uniformity as well as become difficult to remove. Also, vacuum-chuck, wafer-handling techniques on the back-side might damage such structures.

If the sensors are made last, circuits can be made first and the sensor formed. But because of the back-end processing of most MOS processes, this limits the sensor processing temperature to less than 400°C , and many films cannot be deposited reliably or at all (most notably, silicon nitride and polysilicon). If the sensor processing follows device fabrication but occurs before metallization, then there still exists the problem of dopant profile movement of the threshold implants for the MOS devices if any high temperature stress anneals (above 950°C for 1 hour or more) are done, and typically these anneals are much higher [44]. Also, photolithography on subsequent metallization layers maybe difficult if the mechanical structure is freed before patterning.

The last methodology of making the sensor structure primarily out of existing steps in an established MOS process is the most sensible in terms of fabrication time, number of critical steps required, and sensor integrity. Releasing the mechanical structure as the last step solves many problems, but requires certain critical steps which are tractable and require few modifications to an existing MOS process.

3.2.2 High-Temperature Thermal Cycling

Polysilicon surface-micromachined structures usually need stress relief after deposition [45]. This is because the thermal coefficient mismatch between polysilicon and the underlying oxide layer is different, and upon cooling causes residual stresses. Also, film deposition conditions and grain structure also affect the residual stress of the as-deposited film [46]. Depending on the conditions, tensile to compressive stress can be built-in to the film. Normal polysilicon used as gates in MOS processes are in compressive stress and need some sort of relief [45]. However, thermal annealing (which is used to remove the stress) can be as high as 1050°C for 1-3 hours, changing the dopant profiles of devices which can cause undesirable alterations of electrical characteristics [9].

Possible solutions include careful control of polysilicon deposition conditions and/or rapid-thermal annealing which can reduce the stress without increasing the thermal budget allotted for the MOS devices [45]. Other solutions involve making structures more rigid and smaller to accommodate the stress, sandwich structures for stress-compensation, and more sensitive transduction methods to make up for any loss of sensitivity in the mechanical structure.

3.2.3 Sacrificial Spacer Layers

Since the MOS process contains dielectric layers between interconnect levels, it is natural to use them for etch spacer layers in the sensor process. Usually phospho-silicate glass (PSG) is used as a spacer layer since it etches quite fast in HF (> 1 μm/min); however, it is planarized at a higher temperature than boro-phospho-silicate glass (BPSG) [1050°C as opposed to 950°C]. BPSG etches slower in HF, but is still within a factor of 2 of the PSG etch rate. Most oxide dielectrics found in a typical MOS process would then be suitable as sacrificial spacer layers.

3.2.4 HF Etch Protection

When releasing the sensor structure, protection of on-chip electronics or oxide layers is critical. PECVD nitride (used in overglass) may be used to protect against short HF etches, but will fail in prolonged etching. LPCVD nitride or silicon-rich nitride may provide this protection, but must be deposited at 800°C and hence the interconnect used must be compatible [47].

Prevention of HF undercutting is an important issue in process integration with conventional MOS processes. Low-temperature HF-resistant films provide an answer, but are not yet available. Either low-temperature methods for silicon or silicon-rich nitride with better etch resistivity or higher temperature interconnect (800-900°C) will provide some answers in the long-term.

One-sided etching techniques can provide adequate prolonged protection depending on the process, although the practicality in a high-volume manufacturing environment is unclear [48].

3.3 Fabrication Sequence

The Integrated Circuits Laboratory at MIT operates a baseline 1.75 μm twin-well, double-level CMOS process of which a subset of it is used in the sensor/circuit process [49]. This subset consists primarily of the NMOS transistors and single-level metal. None of the critical implants or recipes are changed; in fact, only proper sequencing of available steps offered by the laboratory is needed to achieve the process integration of the NMOS transistors and air-gap capacitors.

The fabrication sequence is broken up into three phases. The first phase briefly covers device processing identical to NMOS, with easy generalization to CMOS. Phase II covers the steps used to integrate both the devices and sensor structure using shared steps, and finally phase III covers the back-side fabrication sequence used to form the air-gap capacitors and complete the process.

3.3.1 Phase I : Device Fabrication

The fabrication sequence begins with a 100 mm diameter p-type (boron) 100-orientation silicon wafer (15-20 Ω-cm) with its back-side polished to a mirror-like finish. This facilitates IR alignment at the end of the process.

Standard NMOS processing is used to obtain the cross section shown in Figure 3.2. The cross section shows device processing after patterning/etching of the polysilicon gates,

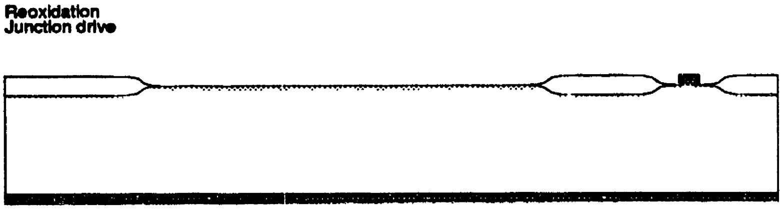


Figure 3.2: Cross section after device processing completion and before normal poly-to-metal dielectric deposition.

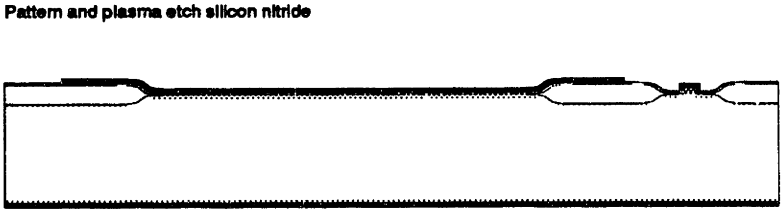


Figure 3.3: Cross section after oxide deposition, back-side strip, p+ boron implant, and nitride deposition, pattern, and etch.

reoxidation, and junction drive of the source/drain region. The cross section could equally apply to a CMOS process after all device processing has been completed prior to poly-to-metal dielectric deposition, or any similar process which utilizes a LOCOS-based scheme with self-aligned gates.

3.3.2 Phase II : Device/Sensor Integration

A 50 nm LPCVD low temperature oxide is deposited at 400°C followed by back-strip of the oxide and a p+ boron back-side implant (species = BF_2, dose = 7 x 10^{15}, energy = 30 keV) to yield a good electrical contact to the substrate. A 150 nm LPCVD silicon nitride layer is then deposited at 800°C , patterned, and plasma etched using SF_6. This is shown in Figure 3.3. The oxide deposition earlier allows for a good etch stop for the nitride plasma etch. The nitride is also deposited on the back-side, and will become the back-side silicon

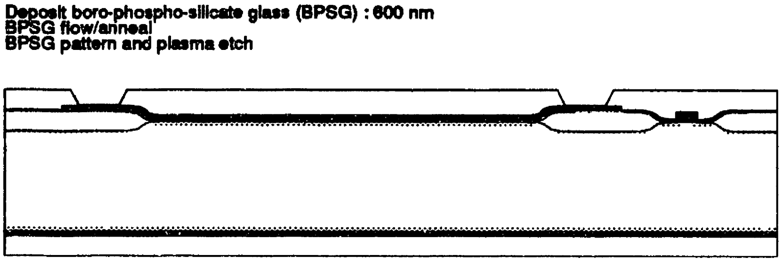


Figure 3.4: Boro-phospho-silicate glass deposition, flow/anneal, patterning, and plasma etching.

etch mask.

The resist is ashed and is followed by a 600 nm boro-phospho-silicate glass deposition at 400°C . This BPSG serves as the inter-level dielectric between poly and metal 1 (PMD) and also as the sacrificial layer that sets the gap distance in the air-gap capacitors. The BPSG is flowed/annealed for conformal step smoothing, then patterned and etched using a mask which forms a moat around the region where the air-gap capacitor lies (Figure 3.4). The etch is a careful plasma etch using CF_4 which is timed to stop on the silicon nitride and field oxide.

After resist ashing, 1 μm of LPCVD polysilicon is deposited at 625°C , doped with phosphorus using a $POCl_3$ source at 925°C , and the phosphorus glass wet-etched (Figure 3.5).

A front-coat resist is applied and a back-side polysilicon plasma etch is done using SF_6, stopping on the BPSG layer. The polysilicon layer serves as the top plate of the air-gap capacitor, and is patterned/plasma etched in CCl_4 (Figure 3.6).

After etching and a resist ash, the process returns to normal back-end MOS process consisting of patterning/etching contact cuts into the BPSG, then proceeding to a sputter deposition of aluminum-1% silicon to a thickness of 1.1 μm. The metal is patterned, plasma

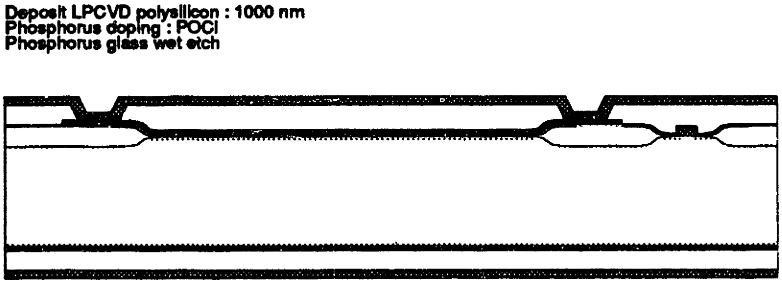


Figure 3.5: LPCVD polysilicon diaphragm deposition, phosphorus doping, and glass wet-etch.

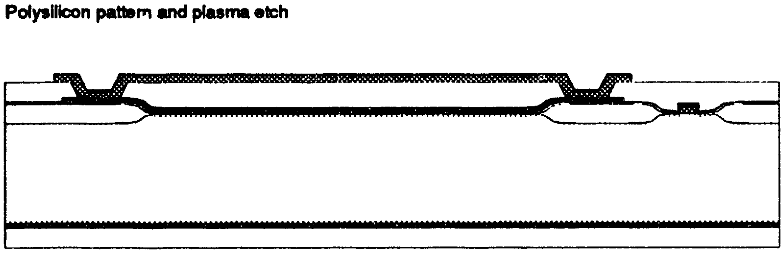


Figure 3.6: Polysilicon diaphragm patterning and plasma etching.

etched, and finally sintered to complete the front-side processing (Figure 3.7).

3.3.3 Phase III : Air-Gap Capacitor Formation

Back-to-front Alignment

For back-side processing, an infrared alignment is used to pattern the back-side BPSG and nitride layers. The contact aligner mask has been designed to align with alignment marks created by the 10X stepper on the front-side. After photolithography, the back-side is plasma etched in CH_4, removing the BPSG and the nitride in one etch step.

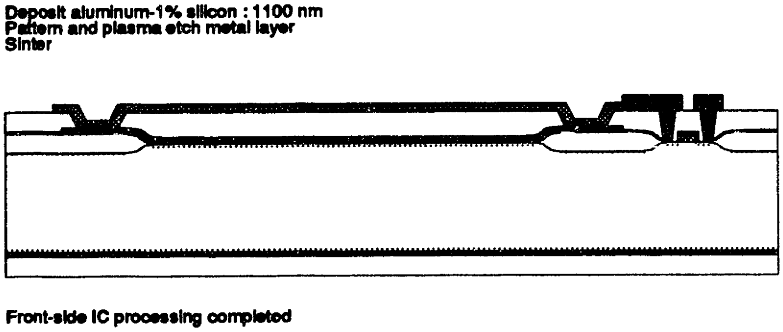


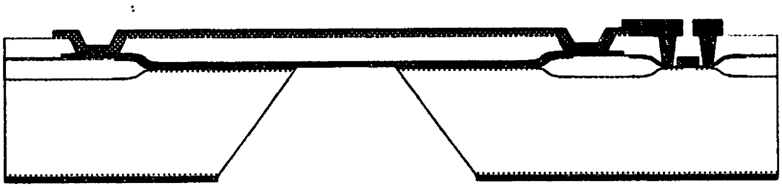
Figure 3.7: Metal pattern, plasma etch, and sinter.

One-sided KOH Etching

The wafers are individually placed in a custom-designed one-sided etching apparatus and immersed in a 20 % by weight (in pellet form) KOH solution at 80°C for 6 hours followed by 60°C for 2 hours using a custom-designed etching system which maintains constant water level, temperature, and stirring [48]. The one-sided etching apparatus is critical since the front-side circuits would be destroyed without it. Resist would dissolve rapidly, and epoxies would delaminate. There is no known photolithographic material that can survive an 80°C KOH etch for 8 hours or more.

The 60°C 2 hour etch after the 80°C 8 hour etch etch provides a gentler etch stop on the silicon nitride layer on the front-side. At this point, the wafer is checked by pulling the etch apparatus out of the etch and optically inspecting the etched hole. It is clear when the etch has finished when the stopped surface is smooth and transparent – revealing the nitride, BPSG, and poly layers. When this condition is reached, the apparatus is rinsed thoroughly in DI water, the wafer removed and rinsed extensively in DI water to prevent any KOH from harming the front-side layers, and prepped for another one-sided etch. The cross section appears in Figure 3.8.

The KOH etch preferentially etches the (100) planes, with a much lower etch rate for



One-sided anisotropic KOH etch : 80 C 6 hours, 60 C 2 hours

Figure 3.8: Back-side KOH etching.

the (111) planes, with the angle between the planes being 54.7 degrees [50]. A thicker wafer will yield a smaller front-side window and hence a larger capacitance because the front-side hole will be smaller, yielding more area for the bottom plate. Process variations and thickness variations were evaluated to allow a design which could tolerate them to an acceptable level. Circular patterns were used rather than squares since this insured that if the alignment (which was to the front-side) was off angle to the flat (which is common to a degree or more), then the undercutting would always produce a square regardless of orientation. This is not true of square masks, and has been experimentally verified that uneven undercutting can occur which can grossly enlarge the hole, destroying circuits on the front-side by engulfing them.

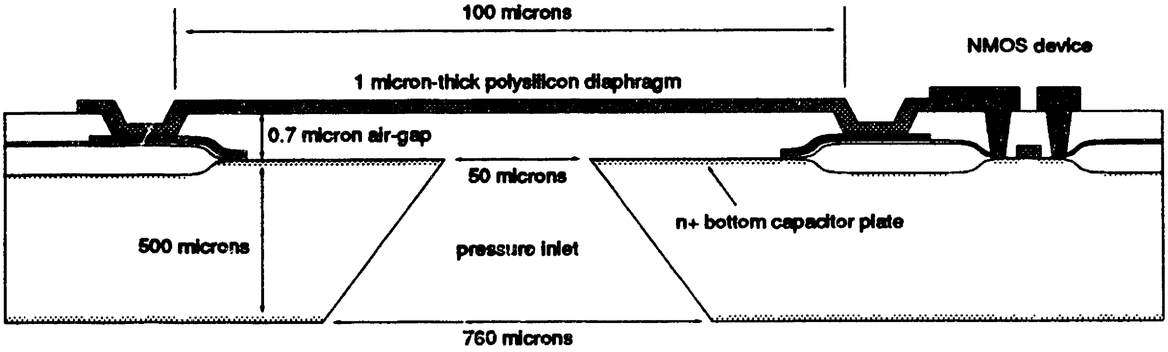


Figure 3.9: Final cross section after one-sided HF etching to release the diaphragm, form the air-gap, and complete the process. Note that the drawing is exaggerated in scale for illustrative purposes.

One-sided HF Etching

The wafer is placed in a one-sided etching apparatus similar to the KOH-etching apparatus, which is designed to protect the front-side of a 100 mm wafer from a 49 % by weight concentrated HF solution [48]. 10 ml of concentrated HF is poured into the cavity of the etching apparatus which uses the back-side of the wafer as its bottom. The HF enters the KOH-etched holes and attacks the silicon nitride. The nitride is not stoichiometric, and etches away in 10 minutes in concentrated HF, revealing the BPSG. This layer is rapidly etched so that in 10 minutes, this layer is consumed to the edge of the diaphragm, where the etch stops at the polysilicon. The front-side nitride layer under the BPSG is also etched, but only after the BPSG has been removed above it, so it provides some protection near the diaphragm anchors. The lateral etch rate has been experimentally determined by watching the etch front proceed under the polysilicon diaphragm (which is semi-transparent). The HF etch also removes the back-side nitride that is used as the KOH etch mask, and this allows electrical contact to the substrate (Figure 3.9).

After etching, the apparatus is thoroughly rinsed in DI water, the wafer removed and rinsed in DI water, blown dry using nitrogen, and placed in a methanol bath for 30 minutes. This removes any excess water that may be in the cavity after rinsing by evaporation. This is extremely important since during the wet HF etching process, the two plates of the air-gap capacitor may have a tendency to stick together due to surface tension.

After methanol rinsing, the wafers are blown dry using nitrogen and dehydrated at 200°C for 24 hours. The wafer is diced along KOH-etched groove lines manually, and the dies are packaged in ceramic PGA packages with specially drilled holes through their centers. Silver epoxy is used to attach the die to the package. The PGA hole is drilled to reveal centrally-located KOH-etched holes which allow pressure to reach the sense air-gap capacitors. The other holes that form the reference air-gap capacitors are sealed by the epoxy and blocked by the ceramic package, sealing the reference air-gap capacitor to external stimuli. The packaging is completed by epoxying a plastic tygon tube to the back of the ceramic package for testing.

Figure 3.10 shows a perspective view of the air-gap capacitor, and Figure 3.11 shows the same figure sliced through its center to show the underlying structure. The contact to the n+ bottom plate is made via n+ diffusion channels contacted by metal surrounding the diaphragm. Contact to the polysilicon is made directly via metal on top of the tab protruding from the square structure.

Appendix B describes in detail the processing used in the fabrication sequence, including detail on the one-sided etching apparatus and post-processing.

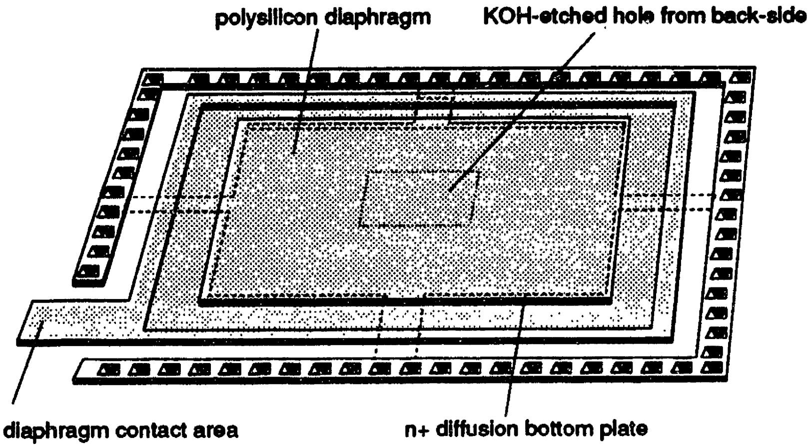


Figure 3.10: Perspective view of the polysilicon air-gap capacitor.

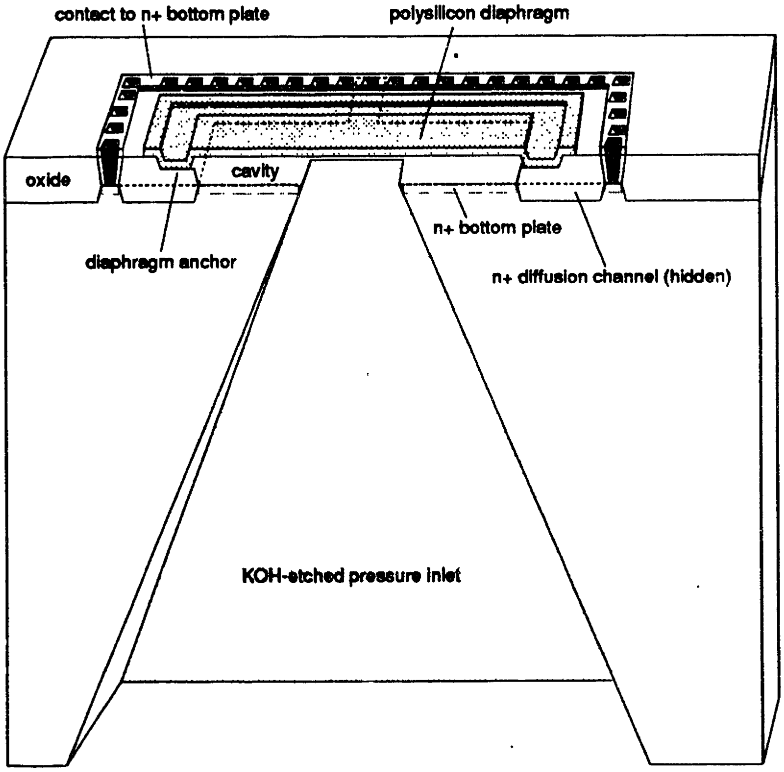


Figure 3.11: 3-dimensional cross section of the air-gap capacitor.

3.4 Alternative Process Methods

In the previous section, the process outlined is designed to balance issues of process safety, laboratory cleanliness, minimization of process steps, and finally, to use as many steps as possible in existing process flows with minimal modification to those flows that deal exclusively with electrical characteristics of MOSFETs. In this section, possible alternative steps are examined.

3.4.1 Fabrication Alternatives

For this research vehicle, surface micromachining is used to preserve MOS device processing while bulk micromachining is used for packaging. The sensor process uses conventional processing to dominate the process, reducing the number of critical, unconventional steps. The most critical etch occurs outside the MOS processing facility and does not require ultra-clean conditions or critical lithography.

3.4.2 Bulk Etching Solutions

The KOH-etching step at the very end necessitates the use of an infra-red aligner. The release of the air-gap structure from the back-side makes it convenient for testing purposes, although for practical commercial purposes, it may not be manufacturable in its present design. The structure also suffers from a lack of over-pressure protection if the pressure is applied through the KOH-etched hole. Nonetheless, it is a convenient structure for testing the capabilities and limitations of the charge-redistribution sense technique.

Several other wet-chemical solutions exist for etching bulk silicon (such as hydrazine or ethylenediamine pyrochatechol, EDP) but the former is explosive in some circumstances while the latter is suspected to be a known carcinogen [51]. Both are difficult to work with and to dispose of in an environmentally-sound fashion. However, EDP has the advantage that oxide can serve as a reasonable mask, and it selectively stops on p+ more readily than KOH (unless electrochemical etch stopping is used). Other laboratories have used different metallization layers to avoid front-side masking problems with a final EDP etch (using chromium/gold for example [52]), but this would never be allowed in most production MOS facilities, so this option is not viable.

KOH is a suitably benign solution compared to hydrazine or EDP, and can be easily disposed of by thorough dilution in water. It is a well-characterized etchant of silicon, and is highly anisotropic, preferentially etching along the (100) planes [50]. The problem with KOH is that contamination by potassium in most foundries is critical, and hence processing using this solution in the laboratory is prohibited. Recent work on ammonium hydroxide and TMAH (tetramethyl ammonium hydroxide) suggests the trend to search for suitable -OH-based etchants (which do not affect metals but etch silicon) rather than resort to using EDP [53],[54].

However, KOH-processing outside the IC facility on wafers after they leave the lab (never to return) is perfectly acceptable, and this is what is done in the design of the air-gap capacitors. Unfortunately, the use of such an etchant such as KOH which etches oxide, polysilicon, and aluminum would destroy the front-side circuits. Thus, a one-sided apparatus is used to circumvent this limitation, in the hopes that it would yield the same results as either a suitable masking material to protect the front-side, or an etchant which would preserve the circuits but etch silicon. In this sense, the manufacturability of the one-sided etching technique would not be an issue in later designs, although there still remains the question of back-to-front-side alignment using conventional photolithographic stepping equipment.

3.5 Polysilicon Diaphragm Stress

The polysilicon diaphragms (the top plates of the air-gap capacitors) consist of unannealed poly that is identical to the gate-level poly in a MOS process, and assumes that the residual stress level of the structure would be low enough to reduce buckling because of the reduced size of the structure. In the past, such polysilicon air-gap structures were made large so that a large enough capacitance could be obtained [55]. Also, gaps of 1 μm were common, and this necessitated larger areas for increased capacitance due to circuit limitations in the transduction process.

A design for air-gap diaphragms had been tried before using large-area polysilicon diaphragms, but it was found that the compressive stress in the poly film caused buckling and fracturing of the structure after release [55]. This stress can vary widely dependent on deposition conditions [46]. Thermal annealing can usually reduce this stress to an acceptable amount, but these temperatures usually exceed 1000°C [46]. Unfortunately, such high anneal temperatures can severely affect the doping profiles of any devices fabricated before the anneal, and hence change the electrical characteristics considerably.

However, such high-temperature anneals might not be necessary since the stress in the poly films might not be high enough to buckle a smaller structure. Such a structure is made possible by the fact that the charge-redistribution sense technique is capable of measuring small changes in small capacitors. Although it requires on-chip components, it significantly reduces the size of the sensor structure, and this in turn helps in making un-buckled diaphragms without high-temperature annealing.

To determine proper diaphragm size, fabrication of different size poly diaphragm structures needed to be done to determine their suitability and critical dimension. This will be the subject of the next section.

3.5.1 Polysilicon Plate Buckling

According to theory [56], for a square plate of thickness h and length a on a side that is clamped along its periphery and loaded with a uniform pressure q, the maximum deflection occurs at the plate center and is given by

$$d_{max} = \frac{0.0152qa^4(1-\nu^2)}{Eh^3} f(\epsilon_s) \tag{3.1}$$

where

$$f(\epsilon_s) = \left[1 + \frac{qa^2(1+\nu)\epsilon_s}{4\pi^2 h^2}\right]^{-1} \tag{3.2}$$

is an equation that is only a function of the strain, ϵ_s, and where negative values denote compressive strains while positive values denote tensile fields. With a very tensile strain, the film becomes increasingly more difficult to deflect, much like a drum head that has been tightened. On the other hand, an extremely compressive film will tend to buckle, and this is seen by noticing that the pole of Eq. (3.2) is a pole of Eq. (3.1). This pole occurs at

$$\epsilon_s = -\frac{4\pi^2}{9(1+\nu)}\left[\frac{h}{a}\right]^2 \tag{3.3}$$

so that given a certain compressive strain ($\epsilon_s < 0$), a maximum aspect ratio a/h can be determined to prevent buckling.

Previous work at MIT revealed that the 0.5 μm thick LPCVD polysilicon films used for gate and interconnect (silane reacted at 250 mT and 625°C and subsequently doped with a $POCl_3$ liquid source at 925°C for 60 min) had a strain of 0.41 x 10^{-3} [57]. This value was obtained through observation of buckling length of doubly-supported polysilicon beams [57].

With this information as well as Young's modulus of elasticity, Poisson's ratio, and density, one can analytically calculate for a clamped-clamped square plate the buckling ratio (a/h), the center deflection as a function of uniformly applied pressure, and the resonant frequency of the first mode. In addition, an estimate of the capacitance of the air-gap structure can be made as well as a crude estimate for the capacitance change as a function of applied pressure.

3.5.2 Diaphragm Size Experiment

Using Eq. (3.3) (and values of $E = 1.61 \times 10^{11}$ Pa, $\nu = 0.226$ [58]) the buckling ratio (a/h) for films with a compressive strain $\epsilon_s = 0.41 \times 10^{-3}$ is approximately 93.4. Thus, given a polysilicon thickness of 0.5 μm, the maximum size of the square diaphragm would be less than 50 μm. However, increasing thicknesses to 1 μm would make this be nearly 100 μm, a more acceptable number in terms of fabrication.

A test chip was initially fabricated to empirically decide the suitable size of the air-gap capacitor since the residual strain of the poly film could be lower if measured using buckling of clamped plates rather than doubly-supported beams. The diaphragm test chip consisted of square polysilicon diaphragms varying in size from 30 to 100 μm with some very large 500 μm diaphragms included also (Figure 3.12). The process used to make them was identical to the process outlined earlier, except that all device-related steps were omitted except ones that preserved topography.

It was determined that the 100 μm polysilicon diaphragm at a minimum thickness of 0.5 μm was acceptable, and was successfully fabricated and released without sticking and buckling. The former was confirmed by applying pressurized gas through the back-side hole and watching the diaphragm move up and down, while the latter was confirmed using a visual inspection. Deformation of less than 1 μm was detected over a 100 μm area by simple visual inspection and confirmed by Linnik interferometry.

The 100 μm size of the diaphragm makes it easier to allow for process variations in the

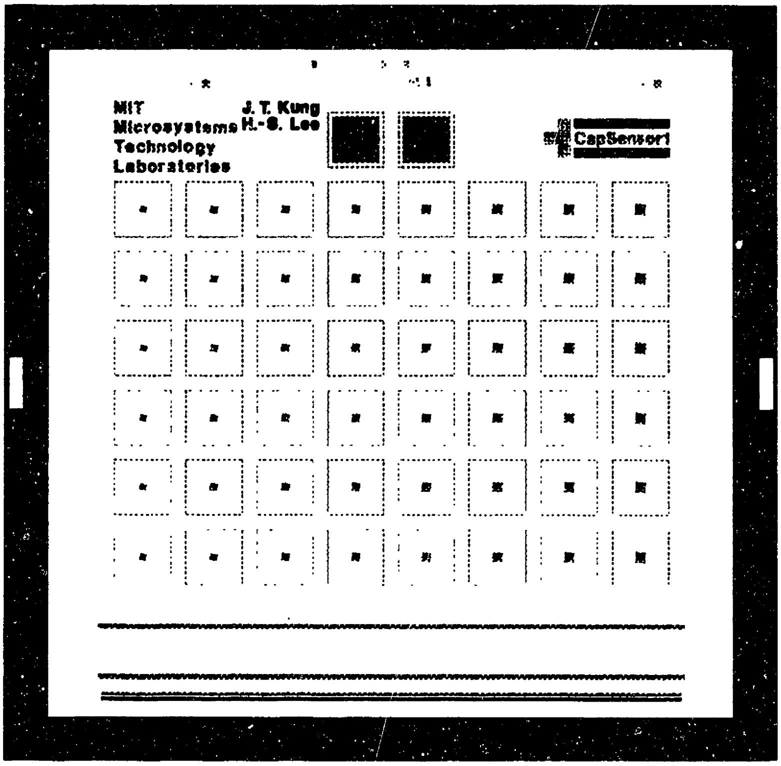


Figure 3.12: Diaphragm test chip layout.

size of the front-side hole. Calculations for the capacitance of this structure (assuming only a parallel-plate of area equal to the bottom plate) revealed a capacitance in the 100 fF range which is the nominal target.

Table 3.1 and Table 3.2 show the results of analytical calculations (based on Eq. (3.1) – Eq. (3.3)) on unstressed 100 μm x 100 μm, 0.5 and 1.0 μm thick polysilicon diaphragms respectively. Stress values using $\epsilon = 0.41 \times 10^{-3}$ are not valid for these diaphragms since the buckling ratio is exceeded; moreover, close to buckling, the deflection is no longer small, so the analytical solutions are not useful. The capacitance is calculated based on the capacitance of the air-gap only, assuming that the nitride and gate oxide layers have been removed by the HF etch. This gap is approximately 772 nm. The method using to determine the capacitance is by perturbation from a parallel-plate condition, assuming a

Pressure (mm Hg)	Deflection (nm)	Capacitance (fF)
0	0	74.9
10	95.4	69.8
20	191	65.5
30	286	61.7
40	382	58.4
50	477	55.5
60	572	52.8
70	668	50.5
80	763	48.3
90	859	46.4
100	954	44.6

Table 3.1: Analytical calculations on a 100 μm x 100 μm 0.5 μm thick, zero-stress diaphragm. Front-side hole is approximately 58 μm square. First resonant frequency is 4.4 x 10^6 rad/sec.

linear shape from the clamped ends of the diaphragm to the maximum deflection point at its center. Fringing fields are neglected so that the only contribution to capacitance is from the bottom plate to the top plate with the effect of the hole being negligible except for reducing the effective capacitance area of the bottom plate. Although this is a crude approximation, it nevertheless gives reasonable results within an order of magnitude of the finite-element modeling (FEM) simulation presented in Chapter 5. The lowest resonant frequency (in vacuum) of the unstressed diaphragm can be found using the equation,

$$\begin{aligned} \omega &= \frac{35.99}{a^2}\sqrt{\frac{D}{\rho h}} \\ D &= \frac{Eh^3}{12(1-\nu^2)} \end{aligned}$$

where D is the flexural rigidity and ρ is the density [55]. For the diaphragms of interest, this yields resonant frequencies in the MHz range.

These simulations along with the empirical data from fabricated diaphragms indicated that a 100 μm x 100 μm 1 μm thick polysilicon diaphragm would be an optimum choice in terms of size, capacitance, and reliability in terms of buckling and sticking. Although the

Pressure (mm Hg)	Deflection (nm)	Capacitance (fF)
0	0	74.9
10	11.9	74.2
20	23.8	73.5
30	35.8	72.9
40	47.7	72.2
50	59.6	71.6
60	71.6	71.0
70	83.4	70.4
80	95.4	69.8
90	107	69.2
100	119	68.7

Table 3.2: Analytical calculations on a 100 μm x 100 μm 1.0 μm thick, zero-stress diaphragm. Front-side hole is approximately 58 μm square. First resonant frequency is 8.9 x 10^6 rad/sec.

deflections are an order of magnitude smaller than for 0.5 μm diaphragms, the capacitance changes lie easily within the capabilities of the measurement system. In addition, the pressure ranges from 0 - 100 mm Hg make it easy to test since these are low pressures compared to atmospheric pressure.

3.6 Air-Gap Capacitor Circuit Element

The air-gap capacitor consists of a top plate and a bottom plate, but they are not interchangeable from a circuit point of view. This is because the bottom plate consists of a heavily-doped n+ region in a p-type substrate, and hence is part of a n+-p diode. Significant leakage currents can arise from this junction from either elevated temperatures or defects. Proper operation must maintain a reverse-bias on the junction.

In the charge-redistribution sense topology discussed previously in Chapter 2, any source or sink of charge on the top plates of the sense/reference capacitors must be suppressed during the calibration/measurement cycles, and hence the top plates are composed of polysilicon, and the bottom plates (which connect either to ground or a negative voltage reference) are fabricated using the n+ region embedded in the substrate.

Since only NMOS transistors are employed, the MOS switch circuit design made it possible only to use a negative reference no greater than -3 V. This is because the logic level low of the NMOS inverter used in switches S1 and S2 is the lowest voltage in the circuit (-5 V) and this will not be able to turn off a transistor with -3 V or higher at its drain. On the other end, a reference voltage no lower than -5 V can be used since anything lower would start to forward bias the n+-p junction and allow significant current to flow from the reference voltage source to the -5 V supply through the substrate.

Another important aspect of the air-gap capacitor is its potential capacitance change due to applied voltage. This voltage coefficient of capacitance is related to electrostatic pull-in effects. The electrostatic pressure on the diaphragm given an applied voltage V is

$$\frac{F}{A} = -\frac{1}{2}\epsilon_0 \left[\frac{V^2}{d^2}\right] \tag{3.4}$$

where d is the gap thickness and ϵ_0 is the permittivity constant. Table 3.3 tabulates this analytical calculation for several voltages, showing the effective pressure, change in deflection, and a rough estimate of capacitance change on a 100 μm x 100 μm, 1 μm thick polysilicon diaphragm. There is almost no change since the pressures are small, and hence the deflections are on the atomic scale. Moreover, during the switching sequence, the voltage is applied to the structure for only a few microseconds. This is lower than the resonant frequency of the diaphragm, so no appreciable resonance would occur. Also, depending on the switching sequence used, either the reference capacitor or the sense capacitor would have the full, applied reference voltage across it for a short amount of time. As the A/D conversion progresses, the voltage across one capacitor becomes negligible while the other approaches the full reference voltage. However, as long as this condition remains true for any applied pressure, then the result is that the electrostatic pressure effect

Voltage (V)	Pressure (mm Hg)	Deflection (nm)	Capacitance (fF)
0.0	0	0	74.87
1.0	0.0557	0.066	74.87
2.0	0.223	0.266	74.85
3.0	0.501	0.598	74.84
4.0	0.891	1.06	74.81
5.0	1.39	1.66	74.78

Table 3.3: Analytical calculations on the effect of electrostatic pull-in effects on a 100 μm x 100 μm 1.0 μm thick, zero-stress diaphragm. Front-side hole is approximately 58 μm square.

changes the nominal capacitance of the reference capacitor by a fixed amount regardless of applied pressure to the sense capacitor. In this sense, the effect only manifests itself as an initial mismatch offset, and can be easily calibrated out. Hence, it is possible for the system to detect changes in pressure in the presence of larger electrostatic pressure.

3.7 SUPREM Simulations

Simulations were carried out using SUPREM to see the effect of thermal cycling on the NMOS process borrowed from the baseline CMOS process used at MIT. Threshold voltages of approximately 1.1 V were simulated for the MIT NMOS process, and the simulation for the modified NMOS/air-gap-capacitor process yielded the same results with essentially no change, despite the added polysilicon doping step at 925°C for more than 1 hour. Since the circuits are implemented differentially, any possible change in threshold voltage is acceptable if matching is good. Appendix C contains the SUPREM input file and results of the simulation.

Chapter 4

Capacitive Sensor Circuit Design

The impulse is pure -
Sometimes our circuits get shorted,
By external interference

Signals get crossed -
And the balance distorted
By internal incoherence

RUSH, "Vital Signs"

4.1 Test Chip Requirements

As [28] had earlier shown, the charge-redistribution sense technique when applied to fixed capacitors works sufficiently well to detect mismatches in capacitance on sub-100 femtofarad capacitors to better than 12-bit accuracy with averaging. This translates to less than 0.1 fF resolution [28]. However, it had yet to demonstrate this performance on variable capacitors without the need for averaging. Furthermore, although the transduction scheme worked well for fixed capacitors, variable capacitors that could deform under electrostatic pressure from voltages applied to the capacitors could, in principle, induce errors in the measurement. Thus, a test chip was designed and fabricated to test the feasibility of the charge-redistribution sense technique on a real sensor structure.

From a system point of view, the test chip electrical requirements are :

- Assuming that variable capacitors are available, these capacitors only need contact access to both top and bottom plates.
- Switching pass transistors are needed to switch either ground or V_{ref} to capacitor plates (switches S1 and S2) and the implementation of a grounding switch S3.
- An on-chip preamplifier to buffer the signal off-chip to a high-speed voltage comparator.

4.1.1 Preamplifier Requirements and Design

The preamplifier does not have to operate in closed-loop, hence relaxing requirements of unity-gain stability. It acts solely as a fast, non-clocked, non-latched comparator which drives the input of a fast, off-chip comparator. Its voltage swing also does not have to be large since it is driving an off-chip comparator.

Also, due to the resolution of the off-chip comparator (1 mV), the gain of the preamplifier does not have to be significant. Assuming for the moment that noise levels in the tens of microvolts exist at the input of the preamp, a gain in the hundreds easily exceeds the resolution of the off-chip comparator. In addition, since the DAC's least significant bit is only 153 μV (for a 16-bit DAC, 10 V full-scale), this divides down by the capacitor divider ratio evident at the coupling capacitor, and attenuates it more, allowing control of the crucial node V_x to be in the sub-100 μV range. Thus only a gain of a few hundred is sufficient to trigger the off-chip comparator. But good amplification is still needed to reduce noise coupling.

Speed and noise are often competing specifications, and in this design, noise is somewhat sacrificed for speed. This is because the design hoped to sample the capacitance change fast enough for speeds in the 10-20 kHz range, but not necessarily 16-bit resolution. A low-noise preamp necessitates large input transistors with too much input capacitance, and hence slows the circuit down. This is why source-followers are implemented in the input. A fully-differential topology is used because of convenience, and common-mode rejection of power supply and clock noise signals.

Circuit Technology and Topology

A parallel effort is made in designing the circuits and the sensor/circuit fabrication process. Because the system does not have stringent requirements on the preamplifier, an NMOS enhancement-mode process is used as the process technology over an existing CMOS technology.

The topology is shown in Figure 4.1. It is a two-stage, differential-pair with resistive loads. A depletion-mode NMOS device is not available in the fabrication process, hence polysilicon resistors are used.

Key things to note about the design are :

- The two-stage design allows for optimization of the DC offsets for only one stage, and assumes that the second stage is identical.
- No compensation is used as it is intended that the preamp always operate in open-loop.

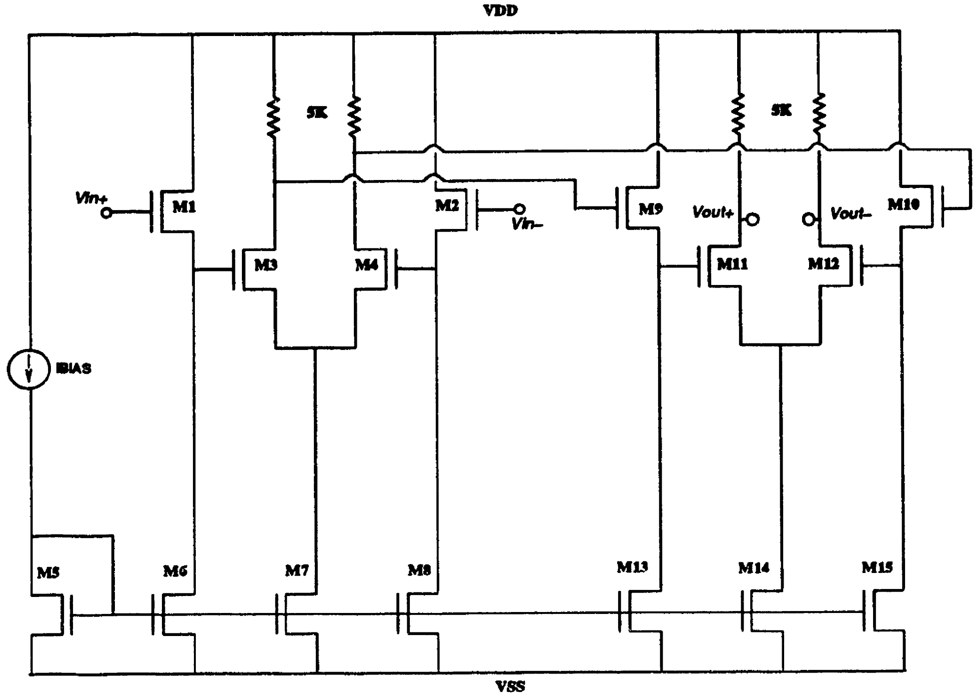


Figure 4.1: Preamplifier circuit topology.

- Power and area requirements are relaxed since the die area is 1 cm, and only one preamp is needed per sense/reference capacitor set.
- The preamp is designed to drive a 20 picofarad off-chip load.
- Source-follower inputs are needed to reduce input capacitances.

Table 4.1 shows the W/L ratios for the transistors, supply voltages used in the design, and other HSPICE simulated parameters. Detailed HSPICE simulations show that the preamp can respond to changes as fast as 1 μs, allowing system A/D conversions to be executed in 16-20 μs. Noise calculations were performed using HSPICE, yielding acceptable levels up to 1-10 MHz bandwidth. The version of HSPICE used BSIM parameters extracted from NMOS transistors in a baseline CMOS process at the Integrated Circuits Laboratory at MIT.

VDD	+5 V
VSS	-5 V
Bias current	2 mA
R	5 kΩ poly resistor
M1 W/L	100/3
M2 W/L	100/3
M3 W/L	510/3
M4 W/L	510/3
M5 W/L	510/5
M6 W/L	25/5
M7 W/L	510/5
M8 W/L	25/5
M9 W/L	100/3
M10 W/L	100/3
M11 W/L	510/3
M12 W/L	510/3
M13 W/L	25/5
M14 W/L	510/5
M15 W/L	25/5
DC gain	335
Phase margin at 10 MHz	60 degrees
Gain at 10 MHz	50
Offset	15 mV
Input noise (to 1 MHz)	8 μV

Table 4.1: HSPICE simulation of key parameters for the NMOS preamplifier.

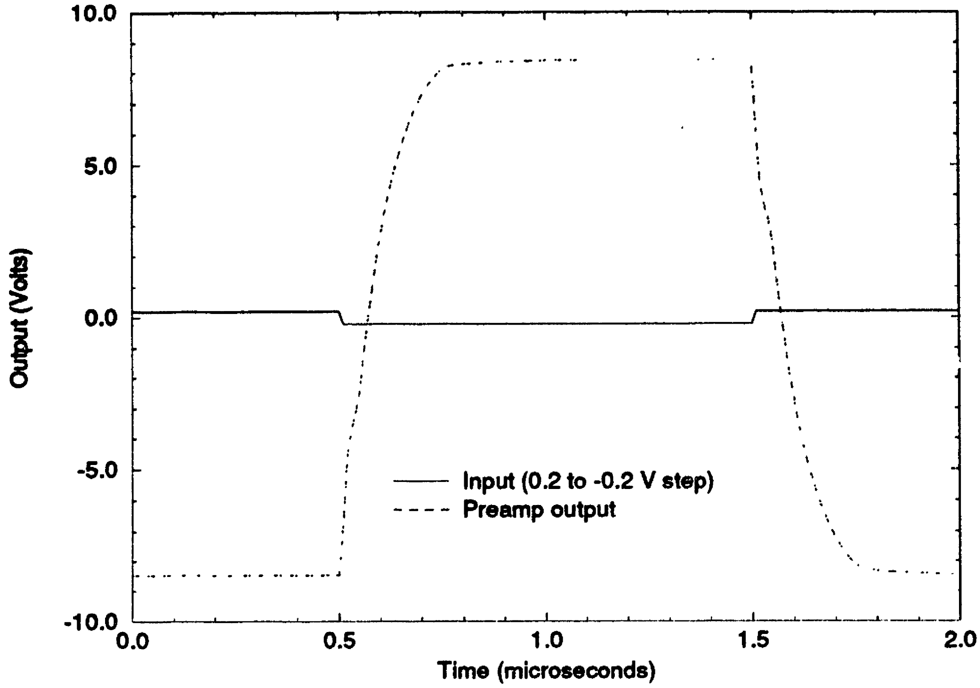


Figure 4.2: HSPICE-simulated switch transient of the NMOS preamplifier to a pulse 0.2 V to -0.2 V and back to 0.2 V. Output is taken differentially on nodes loaded with 20 pF capacitors

The preamplifier is designed to act as gain stage to a fast comparator off-chip. Figure 4.2 shows the response to a single-ended pulse from 0.2 V to -0.2 V. Each output is loaded with a 20 pF capacitor, and the output is taken differentially. Typical times for switching such that the output changes sign and exceeds a 10 mV swing (enough to trigger the external comparator) is approximately 80 ns. Combined with the 35 ns response time of the off-chip comparator, this yields an overall response time of 115 ns. Assuming a 2 MHz system master clock, this means that the time for response would have to be within 500 ns, and this easily makes it within the time window for one cycle of a successive approximation A/D conversion.

4.1.2 NMOS Switch Design

In a CMOS design, switch implementations are trivial since the availability of NMOS allows passage of low voltages while the PMOS passes high voltages. A single enhancement-mode NMOS transistor cannot pass 5 V using 5 V as the controlling gate voltage since in this case, V_{GS} is 0 V.

However, an NMOS switch can pass -5 V if the controlling gate voltage is high, and it is possible to construct a MOS switch that switches between 0 and -5 V by using the circuit shown in Figure 4.3. It consists of 4 transistors. M1 and M2 form a saturated-load enhancement-mode inverter, its input controlling M3 and its output controlling M4. M3 is used to pass 0 V and M4 is used to pass a negative reference voltage. Node 3 is a controlling voltage from off-chip which uses -5 V as a low level and +5 V as a high level. When this voltage is high (+5 V), M3 turns on and passes 0 V to node 5. At the same time, it turns M1 hard, which pulls down the voltage at node 4 to -5 V. This turns off M4 completely.

When node 3 goes low, M3 turns off, M1 turns off, allowing M2 to pull the voltage up, but not quite to VDD since it has its gate tied to its drain. This voltage is $VDD - V_T$ where V_T is the back-gate biased threshold voltage since in the NMOS/sensor process, the body is not connected to the source. This, however, is sufficiently high enough to turn on M4.

The inverter is asymmetrical in its pull-up/pull-down transfer characteristic, but can be designed to minimize the asymmetry. This is done by making the W/L ratio of M2 the reciprocal of the W/L of M1. An important thing to note, however, is that when M1 is on, the drain-to-source voltage across M2 is 10 V with a gate drive of 10 V (VDD = +5 V, VSS = -5 V). This exceeds the breakdown voltage of some of the NMOS transistors (W/L = 20/5) in some test devices, and hence this can cause a problem. Since the switch

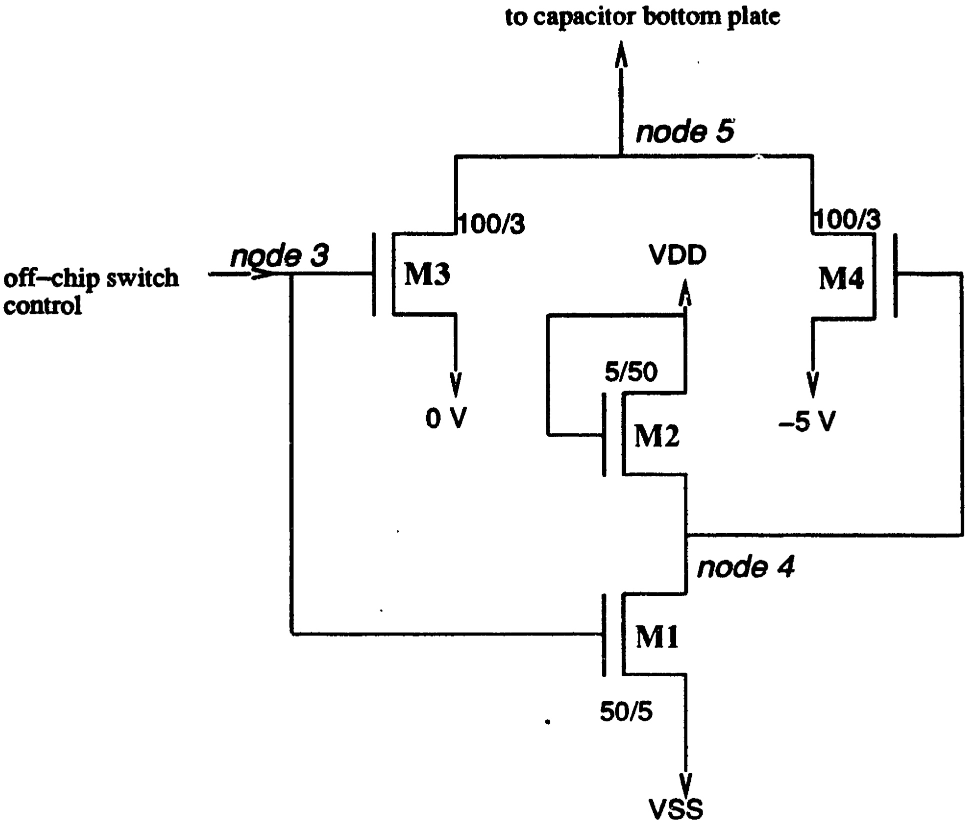


Figure 4.3: NMOS switch circuit. Load capacitance for the inverter is approximately 1 pF.

is normally operated in a mode where node 5 is grounded, this means transistor M2 has 10 V across it for a substantial period of time. A solution is to modify the VDD of the digital inverter by making it 0 V rather than +5 V. This limits the range of acceptable negative reference voltages between -5 and about -3 V, but makes the maximum source-to-drain voltage less than the breakdown. Figure 4.4 shows the simulated transfer characteristic for an inverter with $VDD = 0$ V.

The W/L ratios of M3 and M4 are chosen large enough so that their channel resistance combined with their capacitive loads yield a time constant small enough. W/L ratios of 100/3 yield low enough resistances and occupy little area when folded. In addition, they are already available from the preamp design. Charge injection from these switches is not

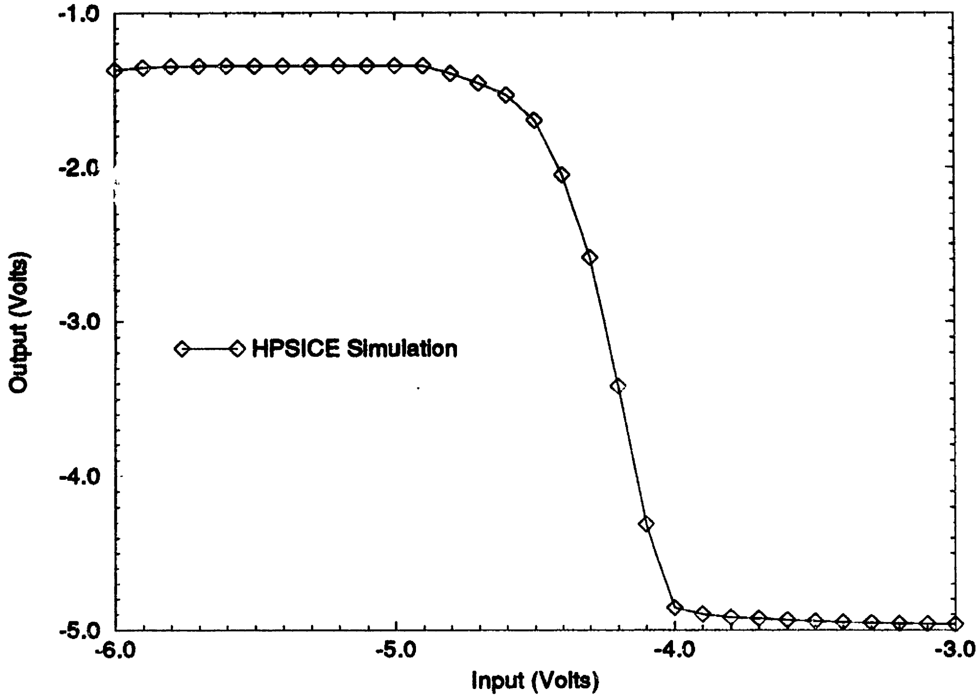


Figure 4.4: HSPICE-simulated NMOS inverter transfer curve.

an issue since they connect the bottom plates to a low impedance voltage source and never leave node 5 floating.

Figure 4.5 and Figure 4.6 show the response of the switch circuit to a pulse with VDD either 0 V or +5 V. In the latter figures, there is almost no difference in switching time, and the switch responds within 0.5 μs either rising or falling.

4.2 System Simulation

The entire system including the preamp, switches, and sense/reference/coupling capacitors was simulated in HSPICE to test functionality and the effects of delays and speed bottlenecks. The DAC/SAR combination output was simulated manually by observing the output

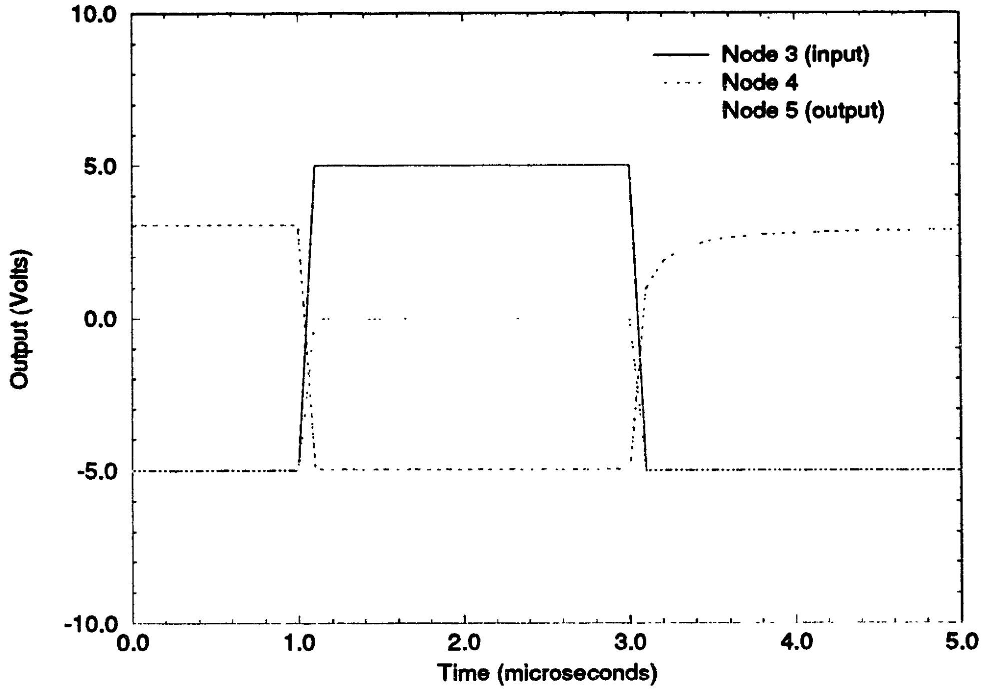


Figure 4.5: HSPICE-simulated switching waveforms for NMOS switch circuit with VDD = +5 V, and an inverter load capacitance of 1 pF.

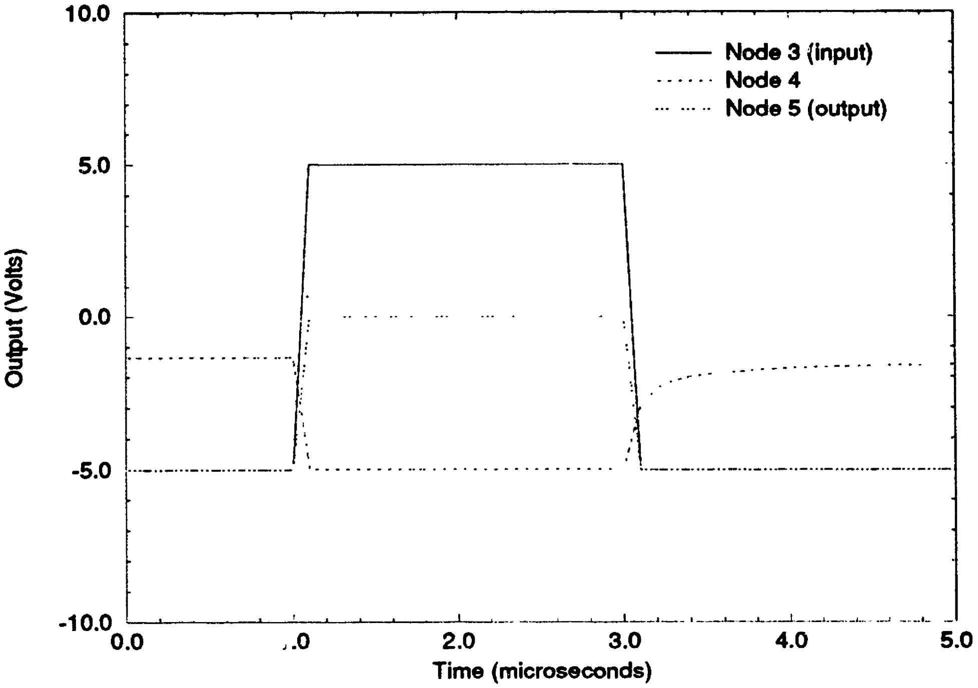


Figure 4.6: HSPICE-simulated switching waveforms for NMOS switch circuit with VDD = 0 V, and an inverter load capacitance of 1 pF.

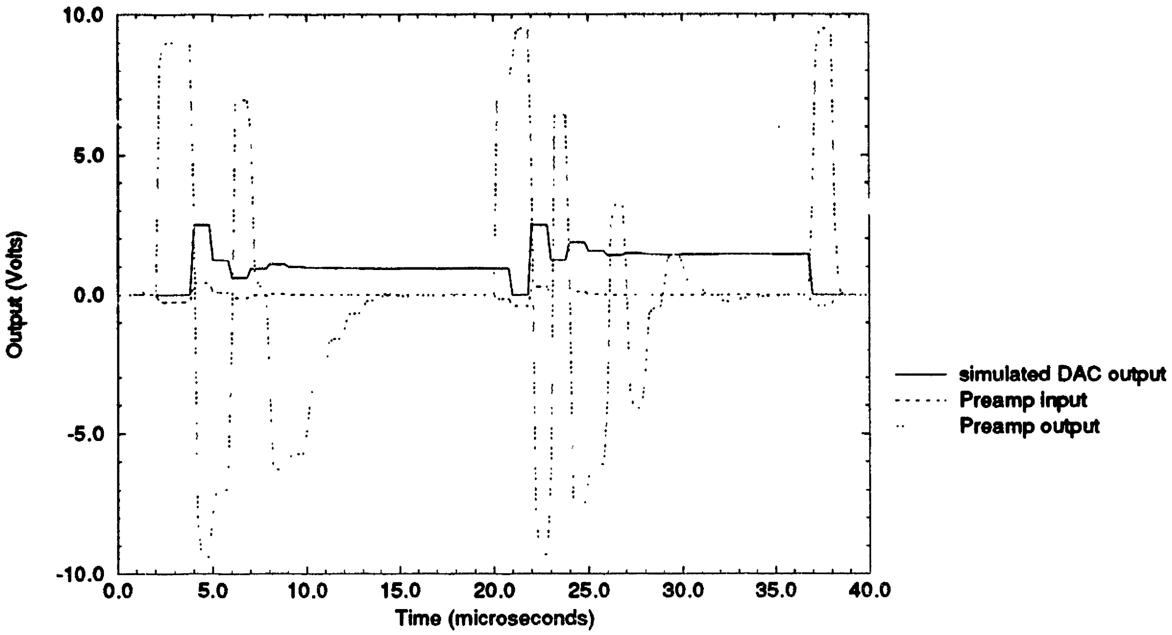


Figure 4.7: HSPICE-simulated switching waveforms for entire test chip, including sense, reference, coupling capacitors, NMOS switch circuits, grounding switch (S3) and NMOS preamplifier. DAC output after calibration cycle at t = 19 μs is 0.940399 V, and at the end of the measurement cycle at t = 38 μs is 1.4405823 V

of the preamp and re-simulating with the appropriate output to the coupling capacitor. Both calibration and measurement cycles were simulated at 1 MHz and 2 MHz clock cycles, and the switch size for S3 had a W/L ratio of 4/3.

Figure 4.7 shows the waveforms for the system simulation with a 1 MHz clock. The output of the preamp determines the digital code used in determining the DAC analog output sent to C_C and this repeats for 16 cycles in the calibration cycle, then another 16 for the measurement. In the simulations, the sense capacitor is 60 fF, reference capacitor is 50 fF, and the coupling capacitor is 100 fF. Parasitics are also included. The algorithm used is digital, where C_S is grounded initially, then switched to V_{ref}.

From the simulations, the analog voltage out at the end of the calibration cycle is

0.940399 V while at the end of the measurement cycle, it is 1.4405823 V. Digital representations are automatically obtained by recording the output of the preamp. Subtraction of these voltages yields 0.5 V ±183μV. Theory predicts using Eq. (2.5) that

$$\begin{aligned} V_{DAC} &= V_{ref}\left[\frac{C_R - C_S}{C_C}\right] \\ &= (-5)\left[\frac{50-60}{100}\right] \\ &= 0.5 \pm 153\mu\text{V} \end{aligned}$$

which correlates well with theory. Thus, the system functions properly and the preamp changes fast enough. It should be realized however, that the comparator/DAC/SAR module was simulated manually by looking at the preamp output, so the simulation is not complete. But it does demonstrate the behavior of the preamp embedded within the system architecture and proves that it is capable of responding fast enough to changes made by the DAC with a 1MHz clock.

4.3 Test Chip Layout

The test chip is organized as 4 separate but identical circuits on a 1 cm die. Symmetry is employed for convenience and allows sense capacitors to be placed near the center of the die. This facilitates ease of packaging. Figure 4.8 shows the layout of the NMOS preamplifier, Figure 4.9 shows the layout of a complete circuit which includes the sense and reference capacitors, coupling capacitors, NMOS switching circuits, and the preamplifier, and Figure 4.10 shows the complete die with 4 such circuits laid out in a symmetrical fashion.

Key things to note about the circuit layout :

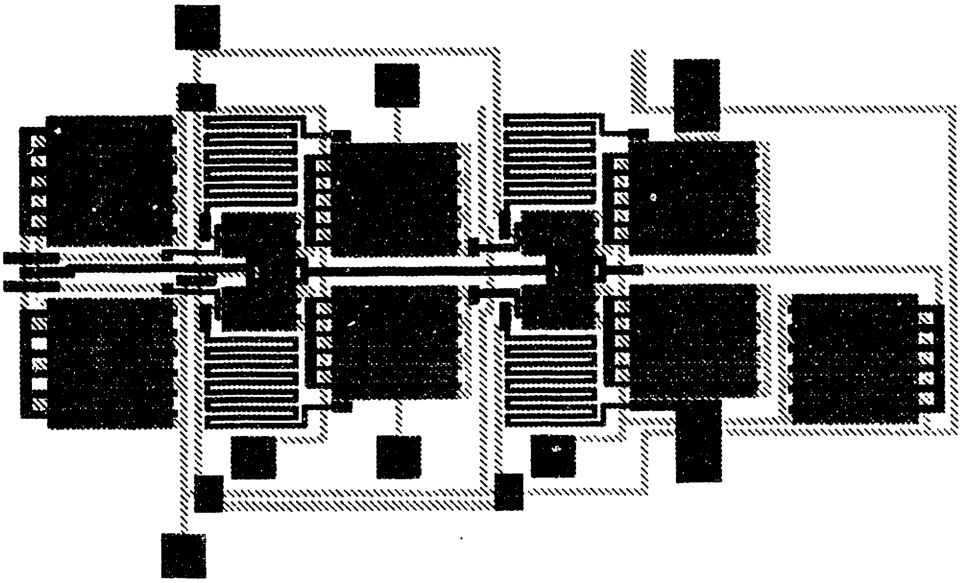


Figure 4.8: NMOS preamplifier layout.

- The sense and reference capacitors are laid out far apart because the back-side holes are much larger than the front-side holes. The sense and reference capacitors are identical.
- Three coupling capacitors of different size are provided to allow potential auto-ranging of the signal in case of overflow, and implemented with metal-to-poly capacitors with separate input lines to allow independent use. They are 50, 100, and 200 fF in value.
- Analog and digital signal lines are kept apart and are carefully laid out for minimal crosstalk. This is especially true for the voltage reference signal line.
- The drop-in test pattern (top of the die) contains a variety of NMOS devices, sense capacitor test structures, and sub-circuits such as the NMOS inverter.
- A separate preamplifier test structure is included in the bottom right corner to allow independent testing.

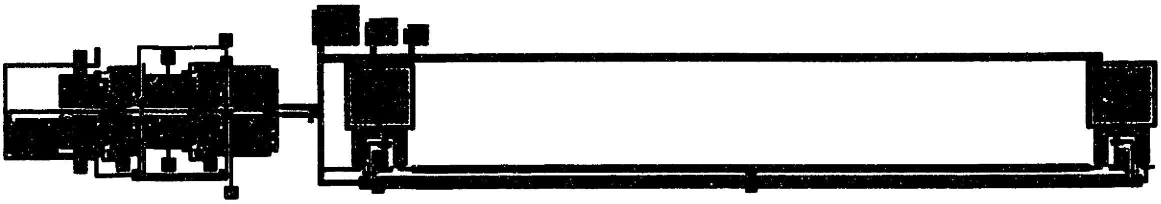


Figure 4.9: Circuit layout.

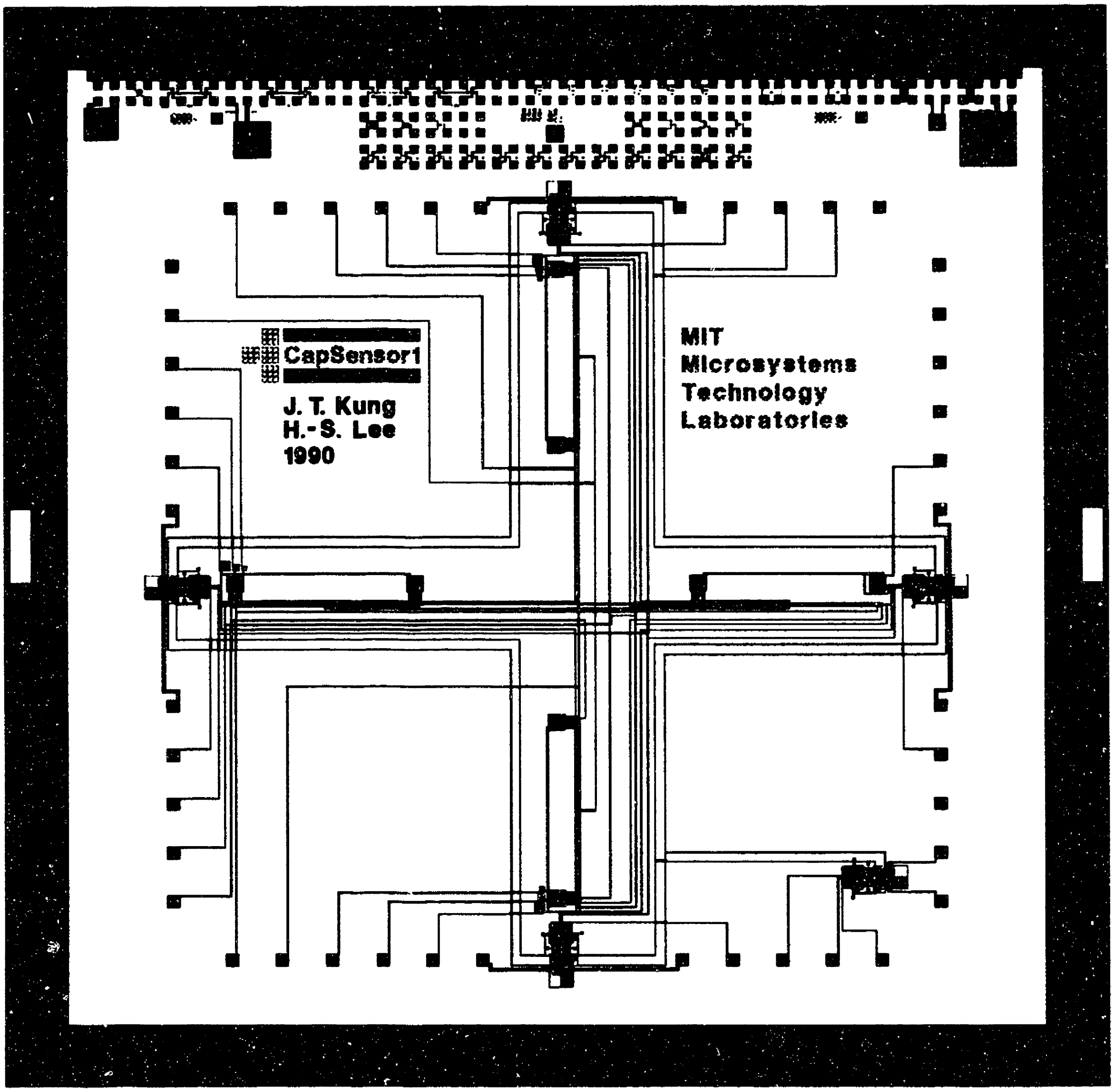


Figure 4.10: Test chip layout.

Chapter 5

Measurement Results

Be careful how you interpret the world: it is *like that.*

HELLER

5.1 Capacitive Pressure Sensor Test Chip

5.1.1 Fabrication Results

Figure 5.1 shows the die photo of the chip after front-side IC processing prior to the backside etching sequence. It is approximately 1 cm square and contains 4 separate capacitive pressure sensors arranged in a symmetrical manner so that the 4 sense air-gap capacitors reside in the center area while the reference capacitors reside on the periphery.

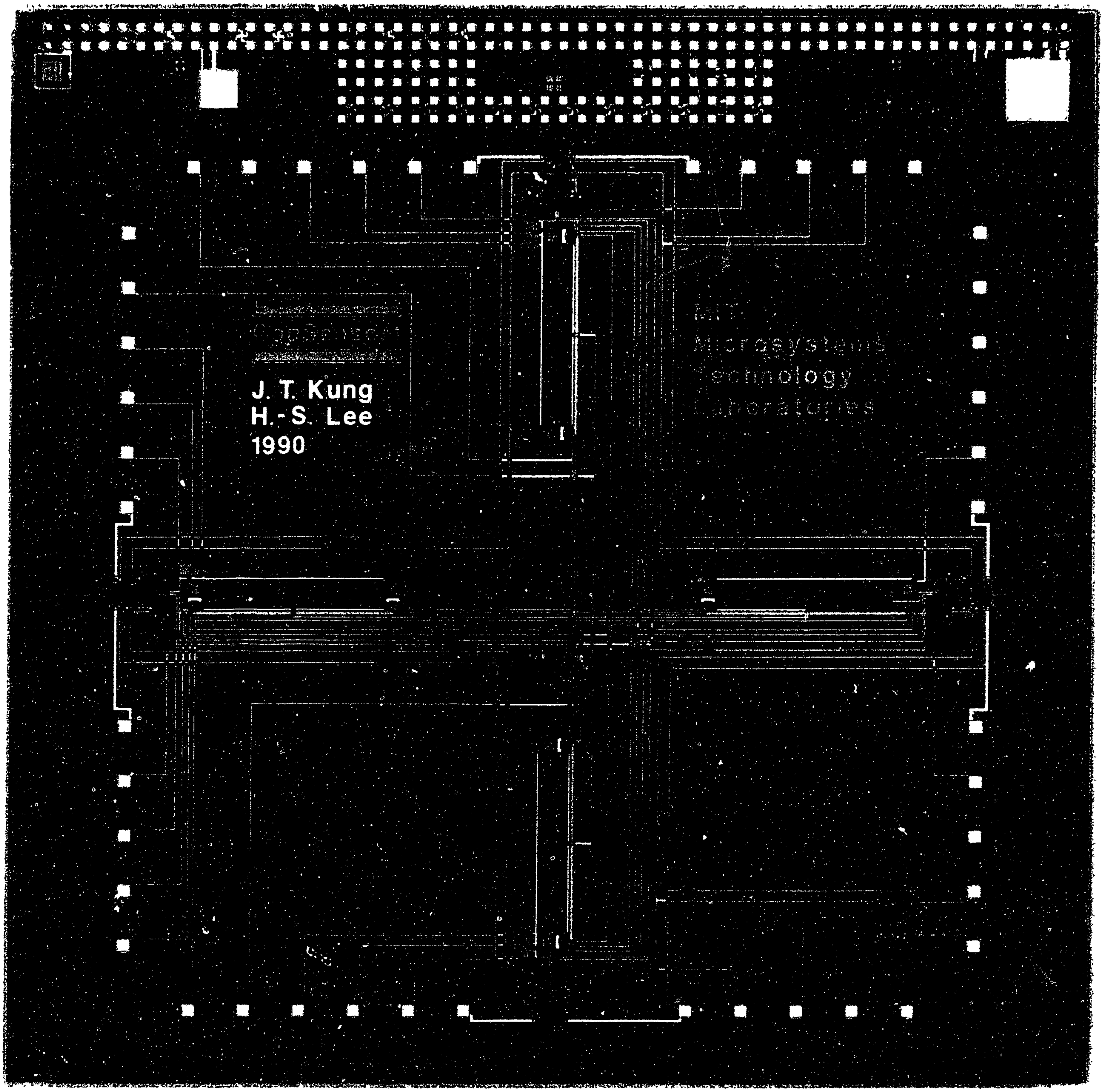


Figure 5.1: Die photo of the capacitive pressure sensor chip after front-side IC processing.

Sensor Packaging

The die is packaged in 65-pin ceramic PGA packages with an internal cavity size slightly larger than 1 cm. The ceramic PGA package is drilled through its center, forming a hole approximately 4 mm in diameter. This is done with a unique technique developed for brittle materials such as ceramic and glass whereby the drill bit is a stainless steel tube with an outer diameter of the desired hole size. Diamond slurry is placed in the tube, and is rotated at a low speed while manual pressure is applied. Drilling is complete in about 10-15 minutes. The hole is designed so that when the die is attached, only the 4 sense capacitors from each independent sensor circuit are uncovered. The reference capacitors are sealed and blocked by the epoxy and package.

The die is attached with silver epoxy and cured, then wire-bonded. A tygon tube is then epoxied to the back of the PGA package to complete the sensor. Figure 5.2 shows a photo of the completed sensor while Figure 5.3 shows the sensor in place in the capacitance measurement system.

For differential pressure testing, the front-side is kept at atmospheric pressure while an external pressure above atmospheric is applied through the tube to the back-side of the die.

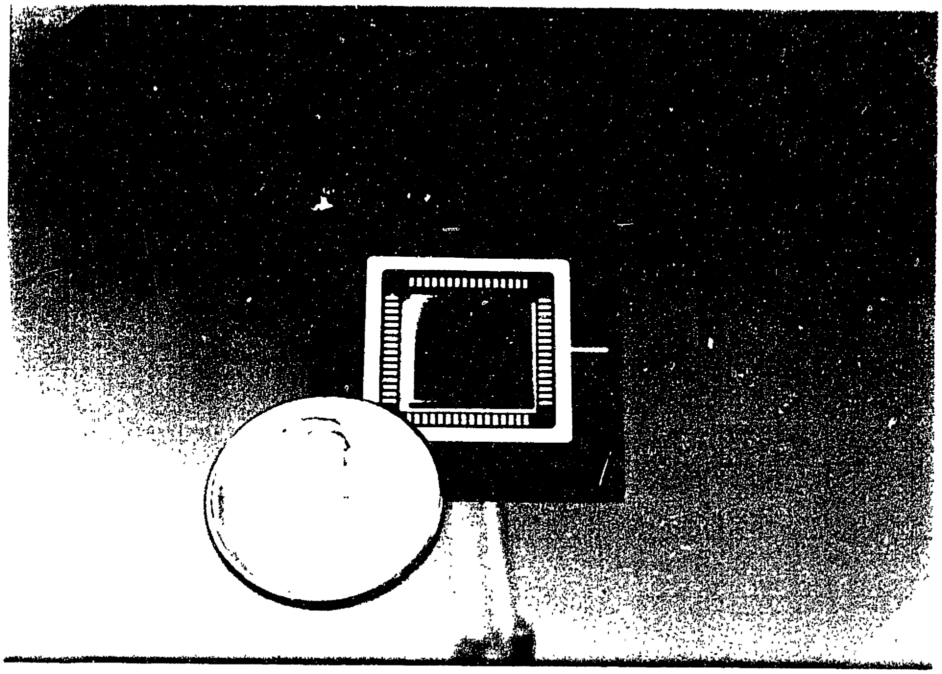


Figure 5.2: Photo of packaged capacitive pressure sensor.

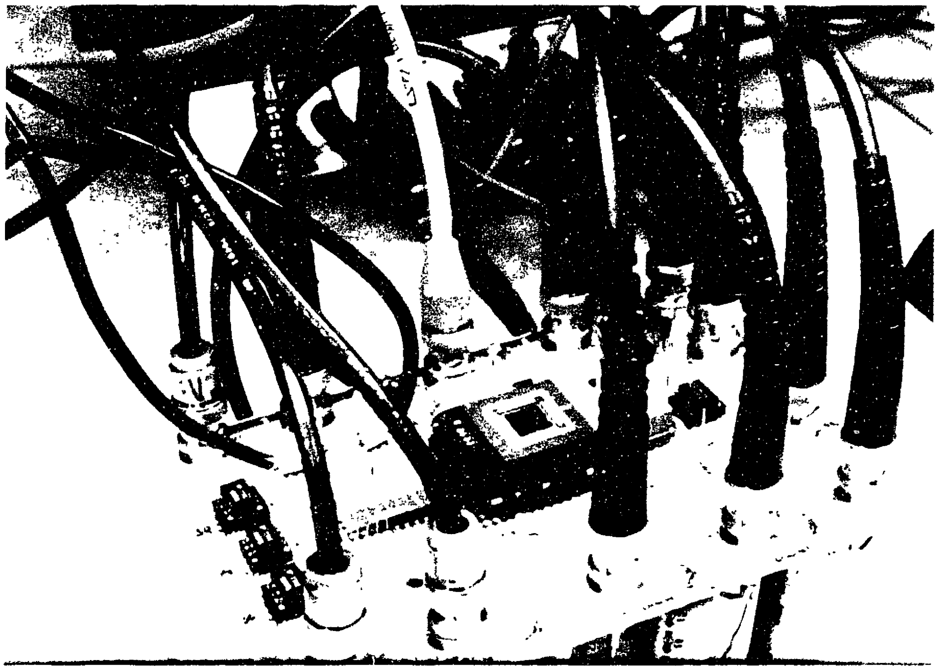


Figure 5.3: Photo of capacitive pressure sensor chip in place on the analog test board in the measurement system.

Fabricated Air-gap Capacitors

Figure 5.4 shows an SEM photo of an air-gap capacitor structure after the KOH etch. The polysilicon and surrounding metal and circuits are intact, demonstrating the success of the one-sided KOH etching system.

Figure 5.5 shows a similar diaphragm after a 25+ minute concentrated HF etch, methanol rinse, and dehydration. The metal interconnect and surrounding circuits are clearly intact, demonstrating the success of the HF one-side etching apparatus. Figure 5.6 shows a shot of another diaphragm and the NMOS preamp adjacent to it, demonstrating the protective capabilities of the one-sided etching apparatus to MOS devices and circuits.

Most of the fabricated diaphragms exhibit some degree of warping, although it is small compared to the horizontal length of the diaphragm. This indicates that some residual compressive stress has been relieved by the mechanical deformation of the structure. Most of the fabricated diaphragms deform downward about 1 μm or less; however, a few appear deformed in the opposite direction, as evidenced by Figure 5.7. The tendency to deform downward is probably due to the DI water rinsing which causes some degree of surface sticking.

The cause of the buckling is attributed to the polysilicon deposition conditions, which differed from the conditions earlier in the making of the non-deformed 100 μm square 0.5 μm thick diaphragms. The 1 μm polysilicon was hazy and difficult to etch. It also exhibited large grain size, and was not as smooth, containing much texture. Possible causes of this include high humidity conditions and/or cleanliness problems in the tube prior to deposition [59]. Since this deposition step is independent of device processing, it is expected that this problem can be solved without any effect on the overall process.

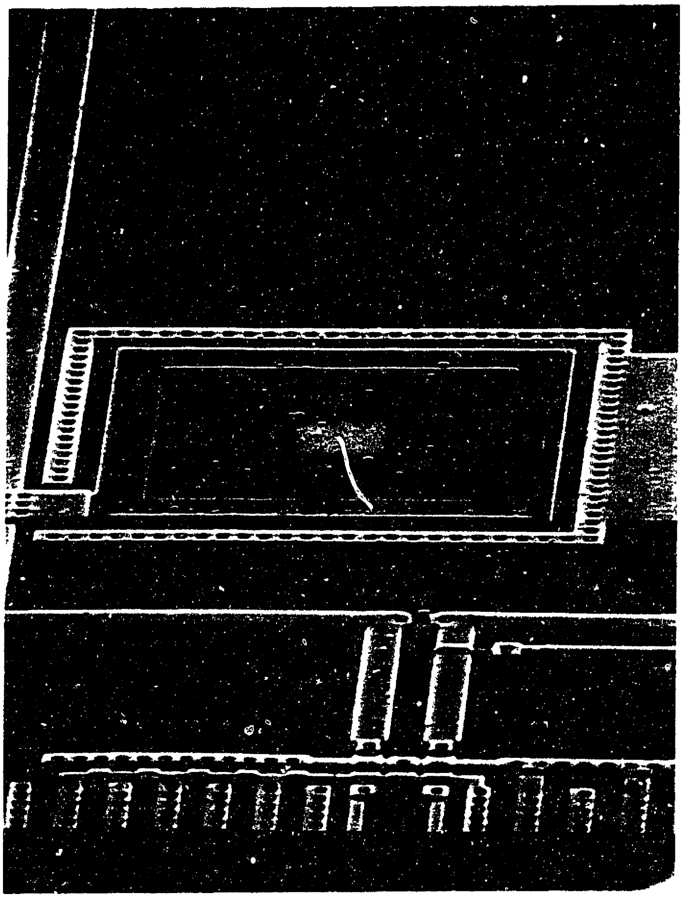


Figure 5.4: SEM photo of a polysilicon diaphragm after KOH etch.

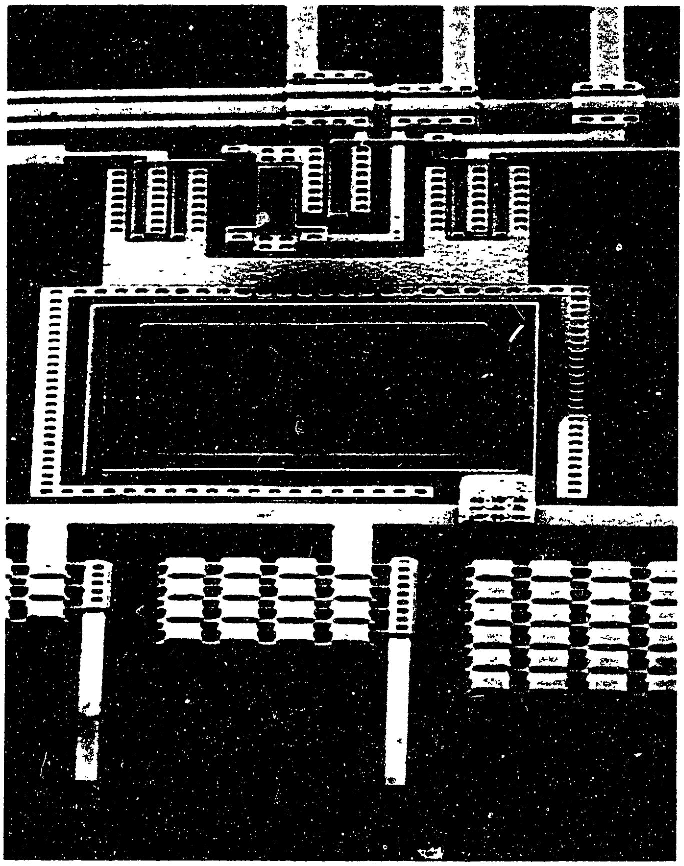


Figure 5.5: SEM photo of a polysilicon diaphragm after a 25 min HF etch.

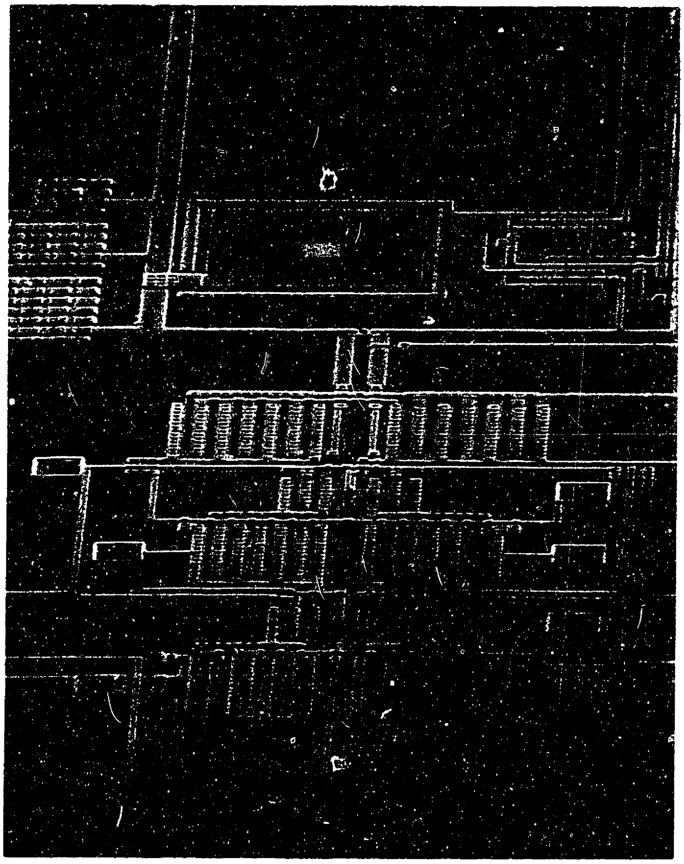


Figure 5.6: SEM photo of a reference air-gap reference capacitor adjacent to the NMOS preamplifier after all etching.

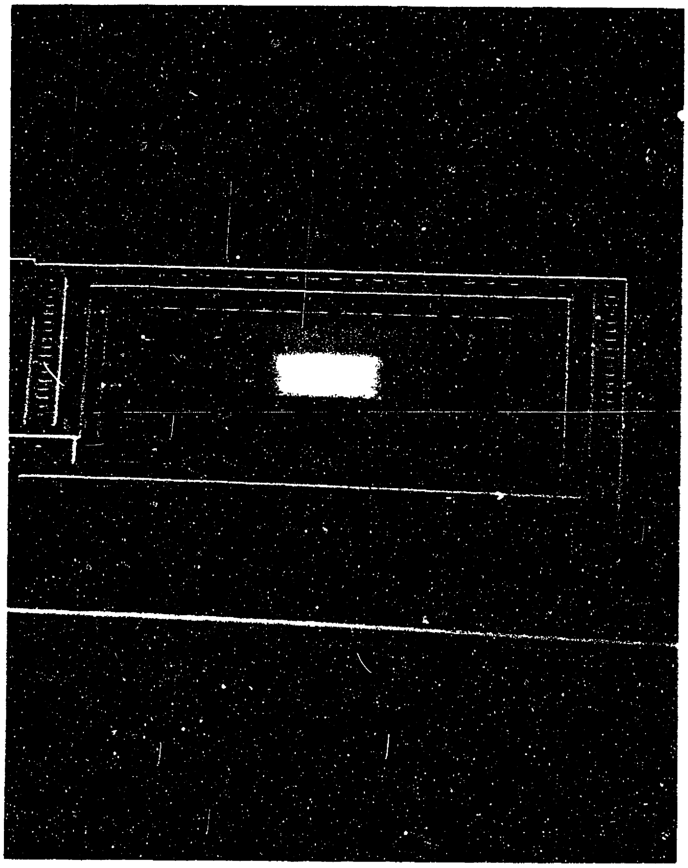


Figure 5.7: SEM photo of a polysilicon diaphragm deformed upward.

5.1.2 Device Results

Physically, the circuits appeared intact after fabrication and etching steps, but the true test of their integrity consists of testing their functionality on both a device and circuit level. On the device side, Figure 5.8 shows an I_D vs. V_D curve of a $W/L = 20/5$ NMOS device after all fabrication steps. The device exhibits characteristics nearly identical to the NMOS transistor in the CMOS process of which the NMOS/sensor process is a subset. This confirmed several things :

- The different substrate did not affect electrical performance.
- The added poly diaphragm level with its 925°C $POCl_3$ doping did not affect device performance.
- The KOH and HF etching steps did not affect the devices.

These are important goals which are met by the NMOS/air-gap-capacitor process. Table 5.1 shows some measured parameters of the process.

5.1.3 Circuit Results

Several sub-circuits were tested to confirm functionality of not only the devices (as was proven by wafer-probe measurements), but of circuits which demonstrate interconnect and contact integrity. The NMOS inverter embedded in the NMOS switch design was tested in the drop-in pattern, and the results plotted alongside HSPICE simulation results shown before (Figure 5.9).

The NMOS preamplifier was also tested separately after packaging. A bias current was supplied (2 mA) and a 1 MHz 20 mV peak-to-peak sine wave was applied to one of

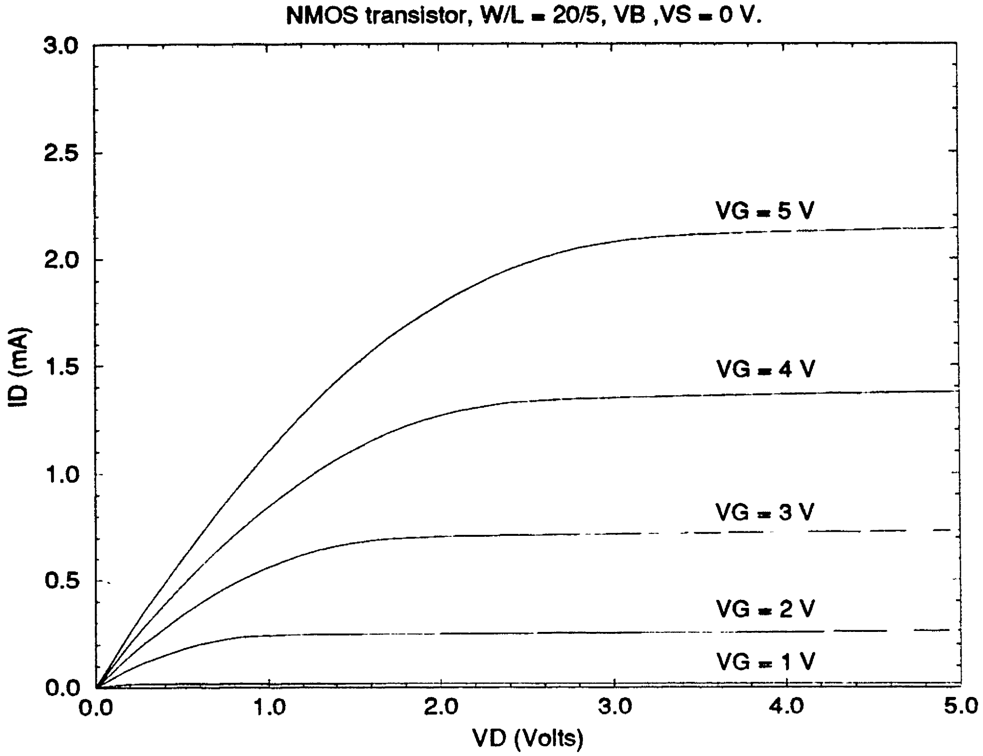


Figure 5.8: I_D vs. V_D for a $W/L = 20/5$ NMOS device after all processing.

Key Process Parameters	
NMOS threshold voltage	0.7 V
Gate oxide thickness	22 nm
Field oxide thickness	400 nm
Field threshold voltage	$>$ 12 V
Poly gate thickness	500 nm
Dielectric	600 nm BPSG
Metal	Al-1% Si, 1100 nm
n+ junction depth	350 nm
Junction breakdown	$>$ 10 V
Poly diaphragm size	100 μm square
Poly diaphragm thickness	1000 nm
Air-gap spacing	700 nm

Table 5.1: Key measured process parameters in the NMOS/air-gap-capacitor process.

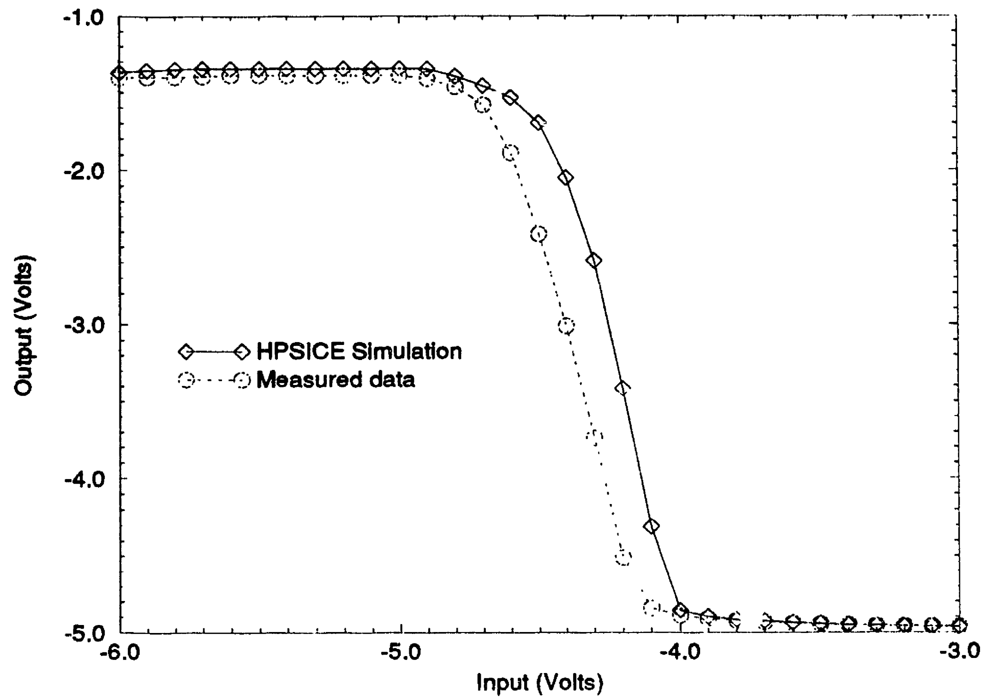


Figure 5.9: Measured and HSPICE-simulated results of the NMOS inverter transfer curve with $VDD = 0$ V and $VSS = -5$ V.

the inputs, with the other grounded (Figure 5.10). The differential output yielded a +5 V peak-to-peak sine wave with a phase shift of 30 degrees (HSPICE yielded 28 degrees). Gain is estimated to be 260 which closely matches HSPICE simulations. Polysilicon sheet resistance was lower than anticipated, causing the 5 KΩ load resistors to be 4.35 KΩ (measured from test structures) which lowered the gain from the HSPICE-simulated gain at 1 MHz of 297 to 258 which closely matches measured results.

5.2 A/D Conversion Test

To test the A/D conversion and the measurement system, a series of A/D conversions were performed by using the system as a successive approximation A/D converter [60].

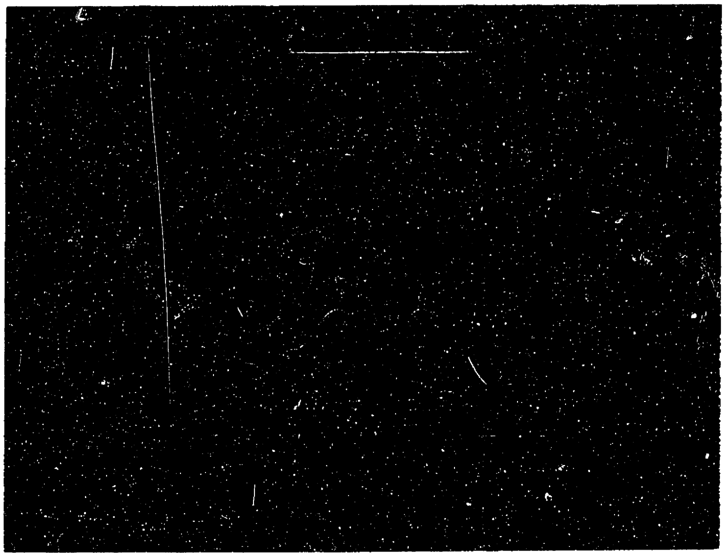


Figure 5.10: Oscilloscope photo of NMOS preamplifier performance. Lower trace is a differential input 20 mV peak-to-peak sine wave at 1 MHz, and the upper trace is the differential output of 5 V peak-to-peak. Gain at this frequency is approximately 260 with 30 degrees phase shift.

Reference voltages of 0 V and ±2.5 V at a master clock rate of 500 kHz were used as the input. The results are shown in Table 5.2.

This data was taken with unshielded voltages applied to the inputs of the off-chip comparator, and hence there was some noise. Data was taken with a 500 kHz clock which translates to a conversion every 32 μs. The data has been averaged 100 times. Since the digital algorithm was employed, the input to the system was converted twice, with the first result (the calibration) being this voltage while the measurement voltage being the subtraction between two conversions. The latter should ideally be zero. Standard deviations indicate noise in the system, and it is suspected that this is due to the unshielded input which does not exist when the test chip is in place. All subsequent capacitance data

A/D Conversion Test With 500 kHz Master Clock				
Reference Voltage	Calibration Voltage		Measurement Voltage	
	$\overline{x}$	σ	$\overline{x}$	σ
-2.5 V	-2.502273 V	1.693 mV	196 μV	2.380 mV
0 V	-1.819 mV	2.014 mV	12 μV	3.038 mV
+2.5 V	2.499355 V	1.792 mV	32 μV	2.401 mV

Table 5.2: A/D conversion test for the capacitive measurement system.

was extracted using a reference voltage of -4 V and a master clock of 500 kHz.

5.3 Capacitance Measurement Results

5.3.1 Measurement Algorithms

There are 4 possible measurement combinations that are implemented to study their differences as predicted by theory :

- Digital positive
- Digital negative
- Analog positive
- Analog negative

The first two are based on the digital subtraction method while the latter two are based on the analog subtraction method. The positive/negative designation refer to the way in which the switching signals are sent to the reference and sense capacitors. Since the measurement voltage is proportional to the difference in these capacitors, reversing the roles of C_R and C_S in the switching sequence should in principle reverse the sign of the output, and hence the designation of "positive" and "negative." These labels are arbitrary in the sense that positive means that C_R is charged initially, then C_S, and vice versa for the negative measurement.

5.3.2 Measurement System Operation

The computer sets up all the necessary initialization and sends the control signals to the digital motherboard. This board contains an EPROM which stores all the switching sequences, an on-board ALU for the digital subtraction and inversions, and on-board static RAM for capture of the sampled data. The system is capable of executing all 4 algorithms (digital/analog positive/negative).

The test chip is housed on the analog board which supplies it the proper supply and reference voltages. The switching signals from the digital board are level-shifted and isolated using opto-isolators. The digital-to-analog converter and successive approximation register are both 16-bits.

Data acquisitions can either be done slowly and displayed in real-time (meaning the data is acquired, then extracted from main memory, and displayed – called *meter mode*), or can be done fast by having the system repeat the measurements and fill the entire main memory (*fill-memory mode*). The host computer can then download this data (or parts thereof) and analyze it. The latter allows for fast sampling of the capacitance change.

A more detailed hardware and software discussion of the digital measurement system is contained in Appendix A and in [60].

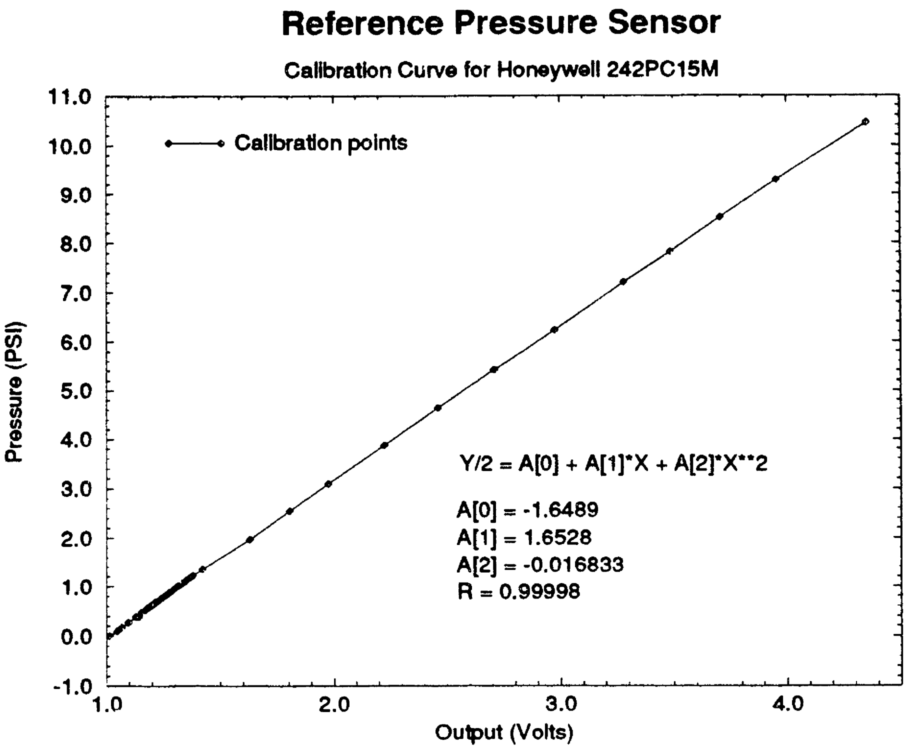


Figure 5.11: Honeywell reference pressure sensor calibration curve.

5.3.3 Capacitance Versus Pressure Measurements

The sensors after packaging were placed in the analog test board for capacitance testing. The board is designed to allow pressure to be supplied to the tygon tubing. This pressure is supplied by a two-step down regulation from compressed air. A Honeywell PC242PC15M pressure sensor was used as the reference sensor. It was calibrated while connected to the pressure system using water and mercury manometers (Figure 5.11) up to about 10 PSI.

The data extraction proceeded by setting the measurement system with a reference voltage of -4.000000 V from the Data Precision supply. The master clock was set at 500 kHz.

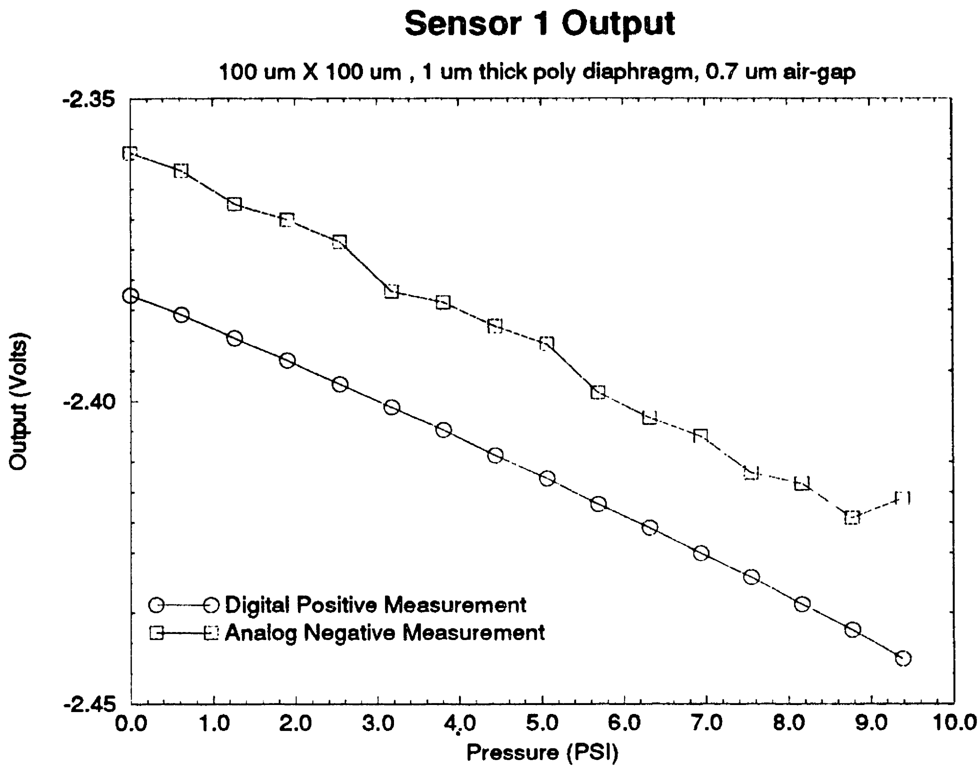


Figure 5.12: Output vs. input pressure for an integrated capacitive pressure sensor using the digital positive and analog negative algorithms.

A zero-pressure measurement was made using the *fill-memory mode* whereby data was taken until main memory in the system was full (262K measurements). This data was then extracted in 100-word blocks, stored, and subsequently analyzed. All 4 algorithms were used for capturing pressure data in the range from 0 to almost 10 PSI (the calibrated range of the reference sensor) in 0.66 PSI increments. The resulting data for one sensor (sensor 1) are plotted in Figure 5.12 and Figure 5.13.

The digital and analog algorithms which correspond to each other (similar switching) differ in their values because of a difference in offset when making the measurement. This can easily be calibrated out, however. They both exhibit linear characteristics due to the small change in capacitance. The initial offset in voltage is due to a large initial mismatch

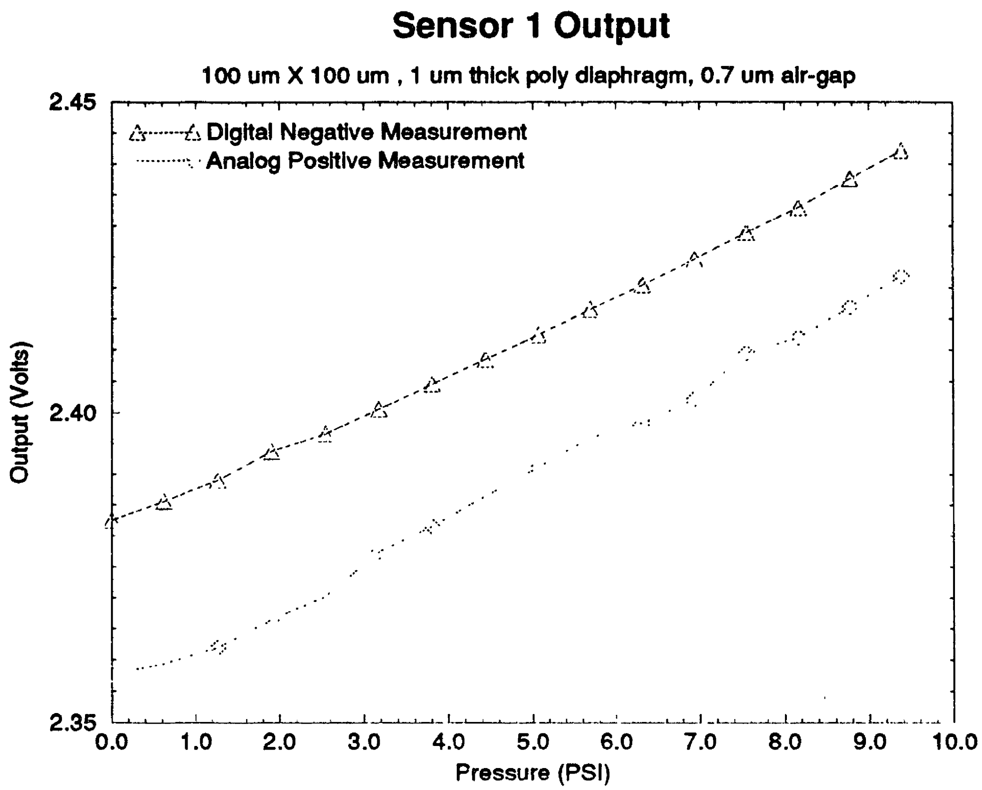


Figure 5.13: Output vs. input pressure for an integrated capacitive pressure sensor using the digital negative and analog positive algorithms.

between sense and reference capacitance. This can be large if the front-side holes are different (due to nitride mask degradation during KOH-etch), or if there is warping in the diaphragm which can cause the top plate to come very close to the bottom plate edges. Each pressure data point represents an average of 100 measurements taken at 90 μs intervals.

Figure 5.14 shows the calibration and measurement voltages for the digital positive algorithm in a zero-differential-pressure environment.

Figure 5.15 details the data using the analog algorithm which involves subtracting the calibration voltage from the measurement cycle by re-applying the negative of $V_{DAC_{cal}}$ back to the coupling capacitor C_C.

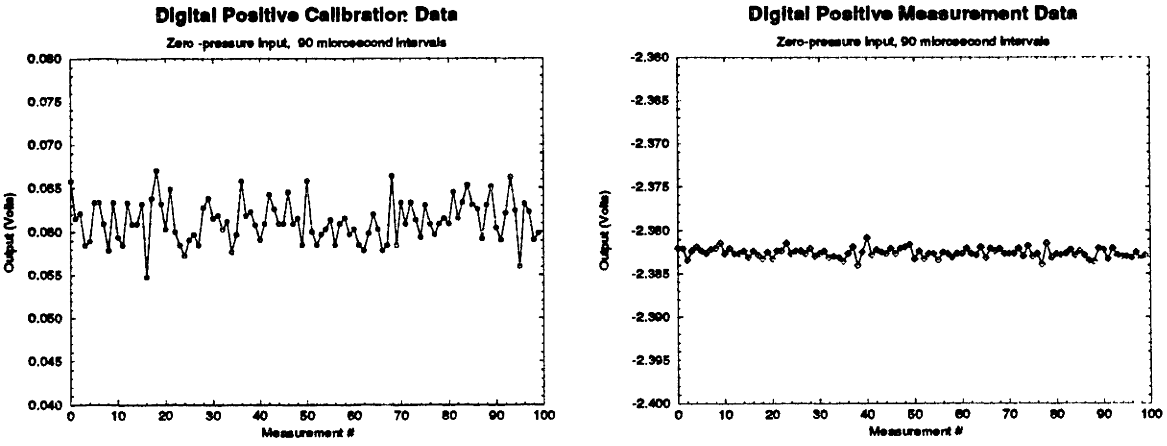


Figure 5.14: Digital positive algorithm raw data (zero-pressure).

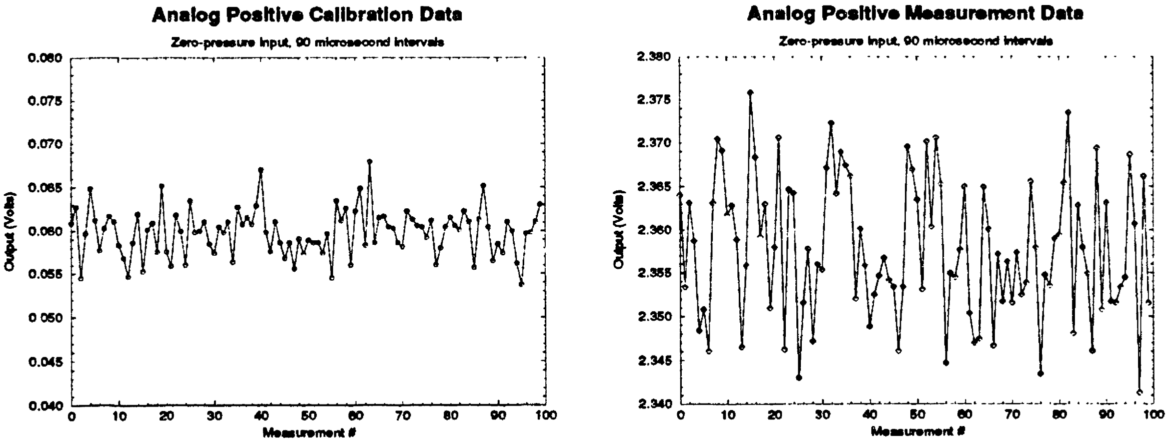


Figure 5.15: Analog positive algorithm raw data (zero-pressure).

Statistics on Raw Data				
Algorithms	Calibration	σ_{cal}	Measurement	σ_{meas}
Digital Positive	0.061198 V	2.390 mV	-2.382579 V	544 μV
Analog Positive	0.059795 V	2.701 mV	2.357751 V	7.934 mV
Digital Negative	0.036359 V	3.342 mV	2.382474 V	599 μV
Analog Negative	0.037433 V	3.143 mV	-2.359038 V	9.819 mV

Table 5.3: Typical statistics on raw data from sensors with zero-pressure input for all the algorithms.

Table 5.3 shows the characteristics in the raw data. The noise levels are much lower for the digital algorithms, approaching the last few LSBs of the DAC, perhaps 14-15 bit effective resolution. Although the negative algorithm data are not shown graphically, they resemble statistically the positive algorithm data, and are shown in the table.

The raw data shows the noise evident in the algorithms. All measurements were taken in 90 μs intervals in a zero-differential-pressure environment. For the analog and digital algorithms, the calibration voltage standard deviations are similar since there is no difference in switching sequence in obtaining this value. For the measurement voltages, the standard deviations for the digital algorithms are much lower than for the analog algorithms. This is probably due to low frequency noise (including 60 Hz noise and $1/f$ noise) which is not canceled in the analog algorithm compared with the digital algorithm.

In the data, the positive and negative calibrations are different because the switching sequence is different. In a true symmetric configuration where there is no difference in C_R and C_S, and their locations are symmetric with respect to switch S3, the calibration voltage should be the same using either the positive or negative algorithms. However, this is not the situation, and the impedance seen by switch S3 is slightly different due to different gate drives for turn on when passing -5 V rather than 0 V for switches S1 and S2. Since C_S and C_R are not equal, this is the asymmetry causing different charge injections and different calibration voltages for the positive and negative algorithms. This is evident in the data. Standard deviations for calibration raw data also seem to suggest large noise, and this will be quantified later in the acoustic FFT measurements, where it is identified as harmonics of 60 Hz from the AC power line.

On the particular sensor in Figure 5.12 and 5.13, the change in voltage from zero-differential-pressure to approximately 9.38 PSI or 0.064714 MPa is 60.03 mV. From capacitance extraction on metal-to-poly capacitors, it was determined that the dielectric thickness is 523 nm for poly-to-metal capacitors, giving a coupling capacitor size of 252 fF. This value could actually vary by quite a bit in practice due to fringing fields, variation in dielectric thickness, and non-uniformity of lateral dimensions. Using this value of C_C and Eq. (2.5) yields a change of capacitance of 3.78 fF for an applied pressure input of 9.38 PSI.

Assuming that the resolution of an individual measurement lies somewhere near the standard deviation, then assuming that 500 μV can be resolved, this yields a capacitance resolution of 0.0315 fF or 31.5 attofarads. On this sensor, this corresponds to a static pressure resolution of 0.07817 PSI. Crude analytical simulations show that a change of 31.5 attofarads corresponds to a deflection in the 1 nm range.

5.4 Optical Deflection Measurements

Optical deflection measurements were taken to correlate the electrical measurements with deflection of the diaphragm. The method employed to measure the small deflections of the diaphragm via pressure was phase-measurement interferometry (PMI). This technique works by changing a reference beam path relative to an object beam path (reflected off the sample) and measuring the change in intensity of the interference pattern at many different relative phase shifts [61]. A piezoelectric transducer (PZT) is used to move a reference mirror which controls the reference beam path (and hence an induced phase-shift). The PMI surface profiler used was a WYKO TOPO-3D surface profiler with a 40X head objective (Mireau interferometer) giving a 250 μm field of view with a lateral resolution of 1 μm (using a 256 x 256 detector array), a depth-of-field of 2.25 μm, and a vertical resolution less than 1 nm [62].

The sensor used in the data of Figure 5.12 and 5.13 was placed under the PMI surface profiler, and an *in situ* measurement was made while pressure was applied. The same pressure set-up used in the capacitance extraction was used in the deflection extraction. Data was taken at different pressures and stored for later analysis. Figure 5.16 shows a 3D plot of sensor 1 with zero pressure applied. The diaphragm is seen to sag into the bottom plate hole. Figure 5.17 shows another diaphragm stuck to the bottom plate. Capacitive extraction measurements corroborated this, since it was not possible to get capacitance data from this sensor due to the capacitance short. Further analysis of the optical data shows that the sticking diaphragm gives a good indication of the air-gap thickness – 725 nm. This is in the correct range since capacitive measurements as well as thin-film measurements during fabrication place the BPSG thickness at 520-540 nm, the silicon nitride at 150 nm, and the low-temperature oxide at 50 nm, giving a total cavity thickness of 720 nm which is close to the optically-measured deformation of the sticking diaphragm.

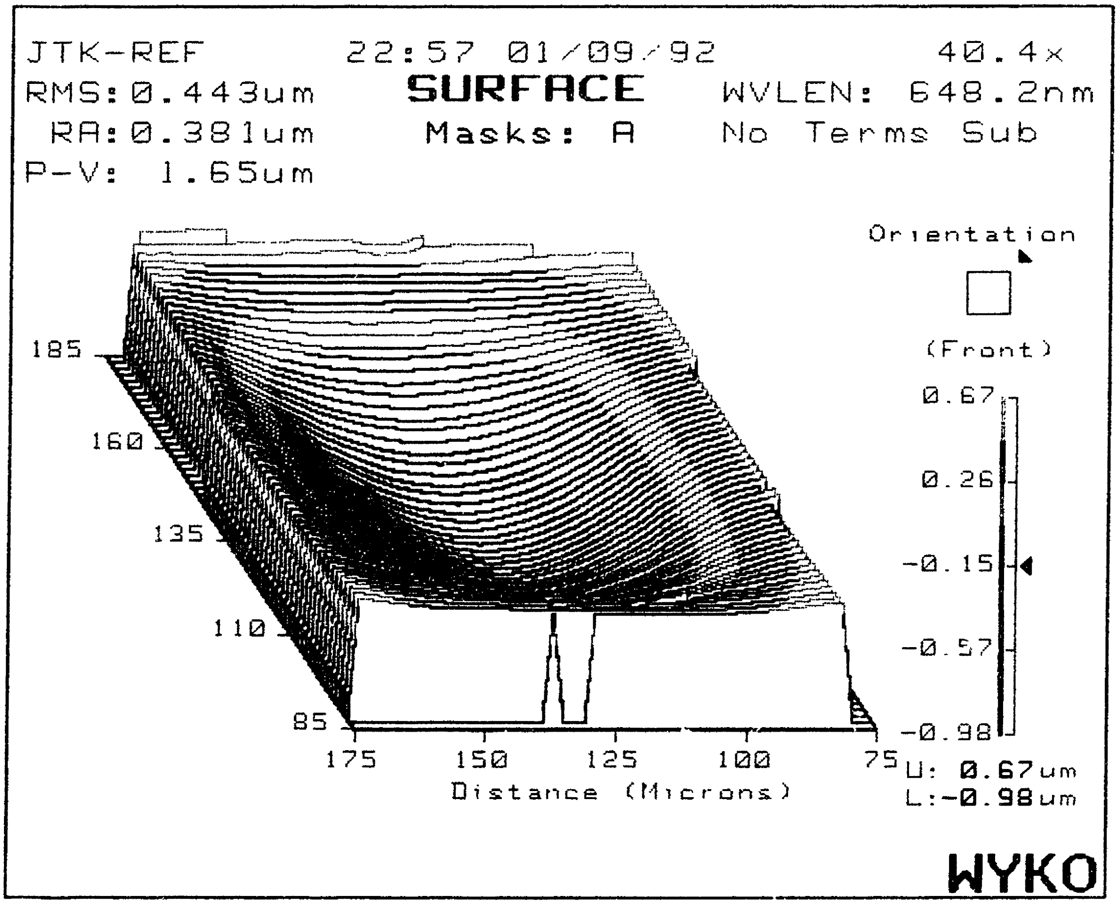
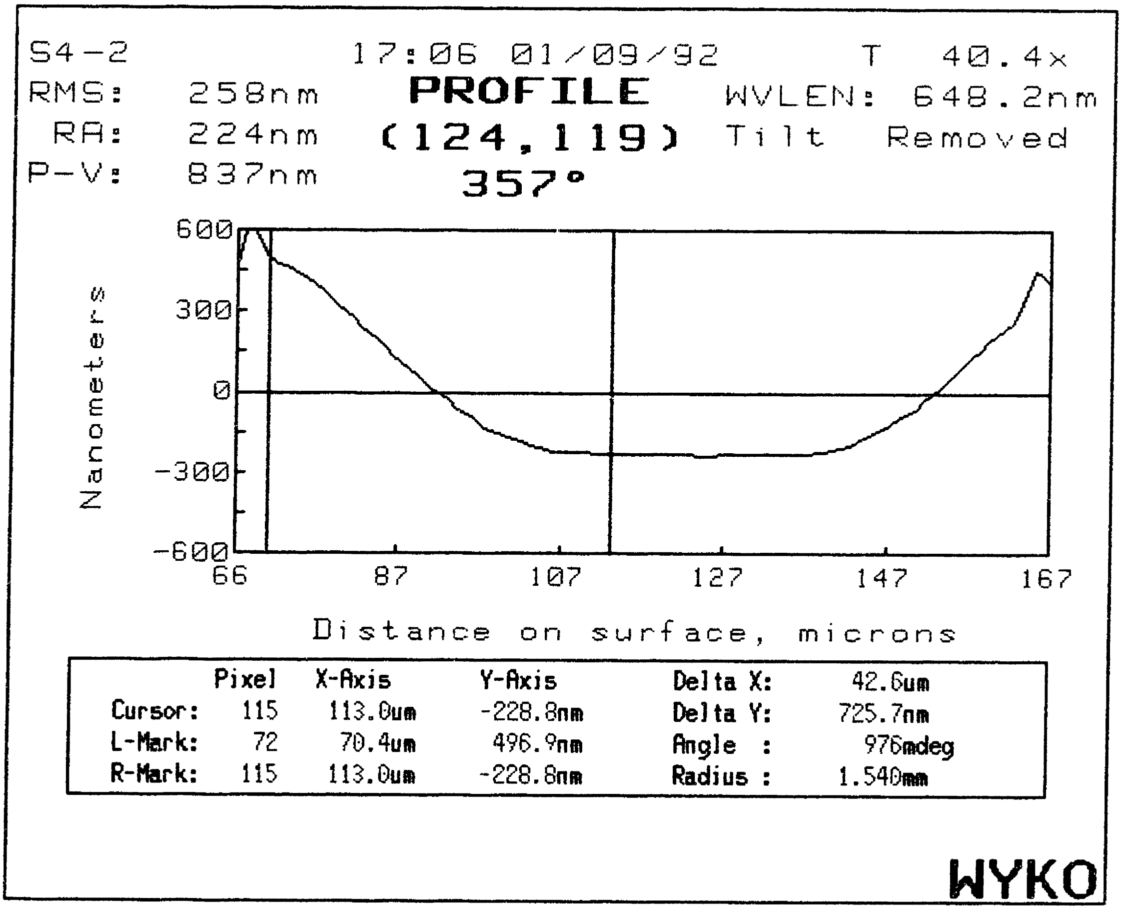


Figure 5.16: 3D surface topography of a air-gap sense capacitor under zero-pressure.



S4-2 17:06 01/09/92 T 40.4x

RMS: 258nm **PROFILE** WVLEN: 648.2nm

RA: 224nm **(124,119)** Tilt Removed

P-V: 837nm **357°**

	Pixel	X-Axis	Y-Axis		
Cursor:	115	113.0um	-228.8nm	Delta X:	42.6um
L-Mark:	72	70.4um	496.9nm	Delta Y:	725.7nm
R-Mark:	115	113.0um	-228.8nm	Angle :	976mdeg
				Radius :	1.540mm

Figure 5.17: 2D surface profile of an air-gap sense capacitor under zero-pressure that is stuck down to the bottom plate.

To measure the deflection of the middle of the diaphragm, the absolute data was stored, and later subtracted from the zero-pressure reference surface, giving the impression of a flat diaphragm pressurized upward. Tilt removal was used to auto-level the data from a known, flat region. This enabled a more accurate analysis of the deflection from a zero-pressure state.

Figure 5.18 shows the data on the shape of the diaphragm of the air-gap capacitor pressure sensor at zero differential pressure. The diaphragm deflects downward into the bottom plate hole by almost 1.5 μm. Since the air-gap is only 0.7 μm, this means that the top plate sags *below* the bottom plate by nearly 0.8 μm.

Optical measurements of the front-side hole reveal that it is 60 μm square, accommodating almost exactly the sagging diaphragm. This indicates that the two surfaces are in very close proximity. Capacitance measurements show that they are not in electrical contact.

Figure 5.19 shows the measured deflection versus pressure for one sensor taken using the PMI surface profiler.

5.5 Finite-Element Modeling

A mechanical structure similar to the one depicted in Figure 5.20 was simulated using PATRAN as a 3D model builder and ABAQUS as the FEM solver [63]. The FEM data was then passed to FASTCAP, a program designed for fast extraction of capacitances from complex 3D VLSI interconnect structures [64]. Three different simulations were performed, and they are described in Table 5.4.

The first FEM simulation is based on an idealized structure where there is no stress, the diaphragm is flat, and the edges are clamped (edges are fixed in displacement and in

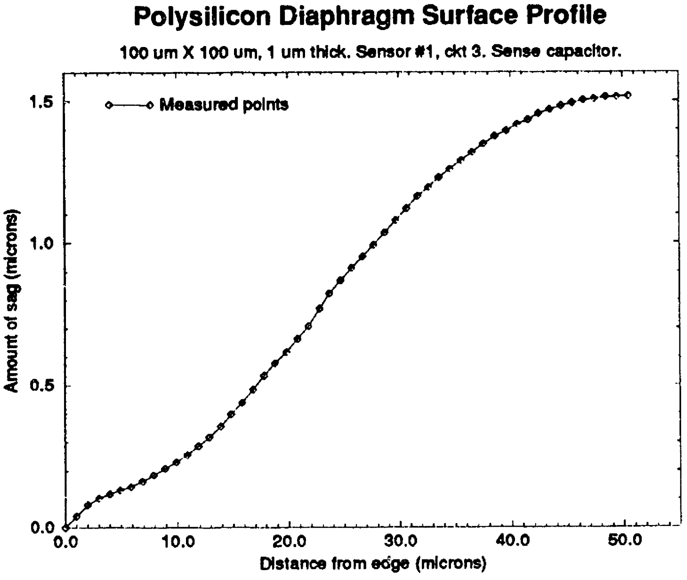


Figure 5.18: Surface topography data of an air-gap capacitor diaphragm obtained using PMI measurements.

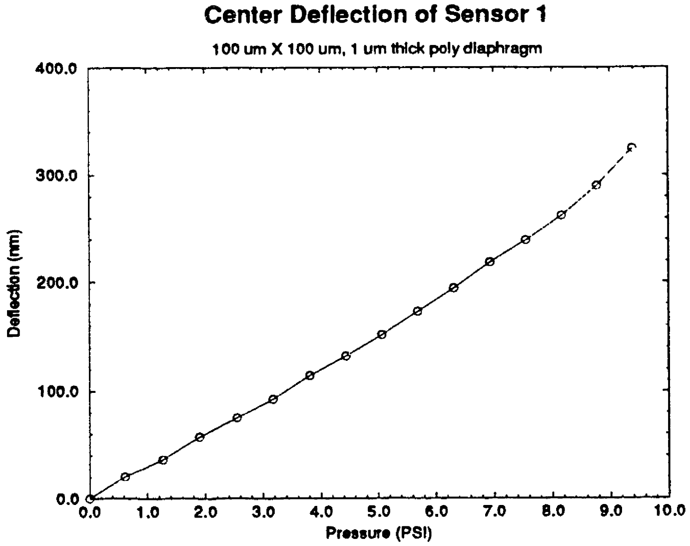


Figure 5.19: Measured deflection versus pressure obtained using PMI measurements for a real diaphragm.

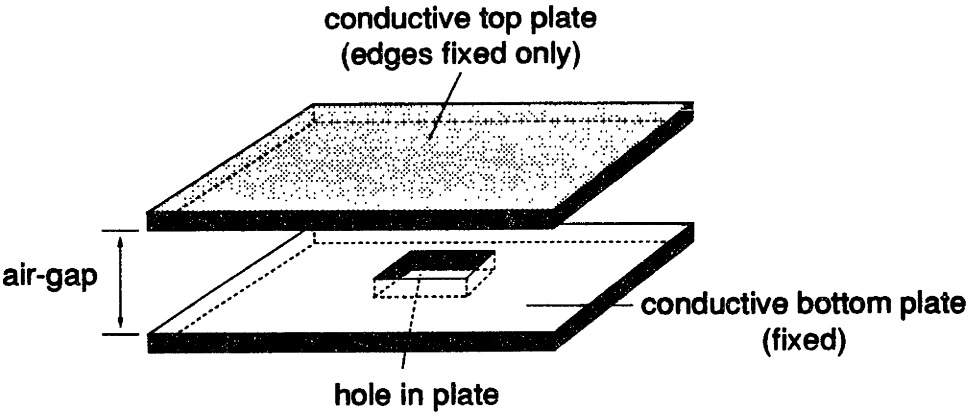


Figure 5.20: Finite-element 3D model for the diaphragm structure.

FEM simulations			
Parameter	**1**	**2**	**3**
Top plate shape	flat	warped	warped
Edge condition	clamped	clamped	pinned
Top plate	100 μm square		
Top plate thickness	1 μm		
Air-gap	0.7 μm		
Bottom plate	100 μm square with 62 μm hole in center		
Stress	zero		

Table 5.4: FEM simulation parameters.

rotation). The second FEM simulation is based on a non-ideal structure which closely resembles the actual sensor structure. This simulation tries to model only the difference in diaphragm shape, with all things else the same as the first simulation. Finally, the last simulation tries to account for changes due to the edge boundary conditions. It appears from optical deflection data that some diaphragms have edges which do not have a flat slope, indicating some possible rotation at the edges. Thus the last simulation establishes a pinned edge where rotations are allowed, but the edges are fixed in displacement. Values for Young's modulus used were similar to values used in previous analytical calculations : $E = 1.61 \times 10^{11}$ Pa, $\nu = 0.226$ [58].

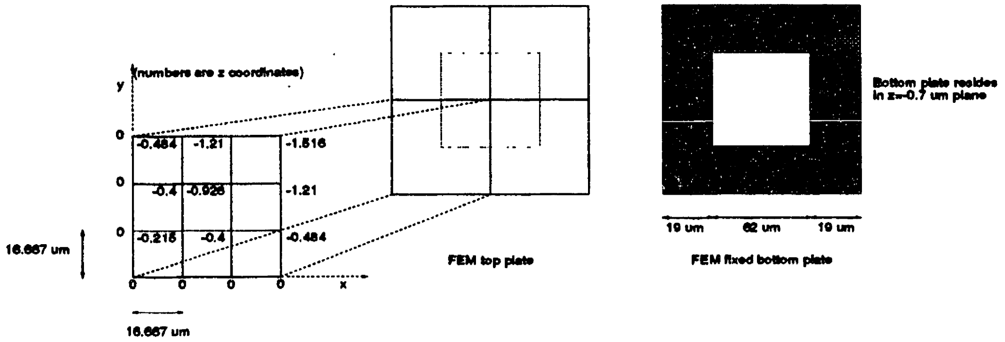


Figure 5.21: FEM modeling of the real air-gap capacitor structure, partially constructed from optical data.

All FEM simulations used a discretization of 50 element/side or 4405 elements and 4595 nodes. This was determined from sample tests where both stress and deflections converged to a value within a few percent, and where the simulation files were manageable in size and in simulation time. Simulation was accomplished using software which linked PATRAN (a 3D modeler), ABAQUS (a finite-element solver), and FASTCAP (a capacitance extractor), and which ran on a SUN/4. Simulation time for each pressure point was approximately 2 hours.

For the warped diaphragm, it was assumed that the diaphragm was symmetrical, so that real data from only one-quarter of the diaphragm were used to construct the shape. The shape was crudely constructed from 16 points in one quadrant of the real diaphragm, shown in Figure 5.21. The 3D modeler PATRAN interpolates a polynomial through the 4 points, constructing a surface, then extending it to the other quadrants by symmetry. The slope at the edges is initially zero. The surface is then discretized into elements. Smaller discretizations yielded errors while larger ones converged to more consistent results.

Figure 5.22 depicts the simulated deflection versus pressure for the three simulations in Table 5.4 as well as analytical calculations (based on Eq. (3.1)), and Figure 5.23 shows the simulated capacitance versus pressure curves for the three simulations and crude analytical

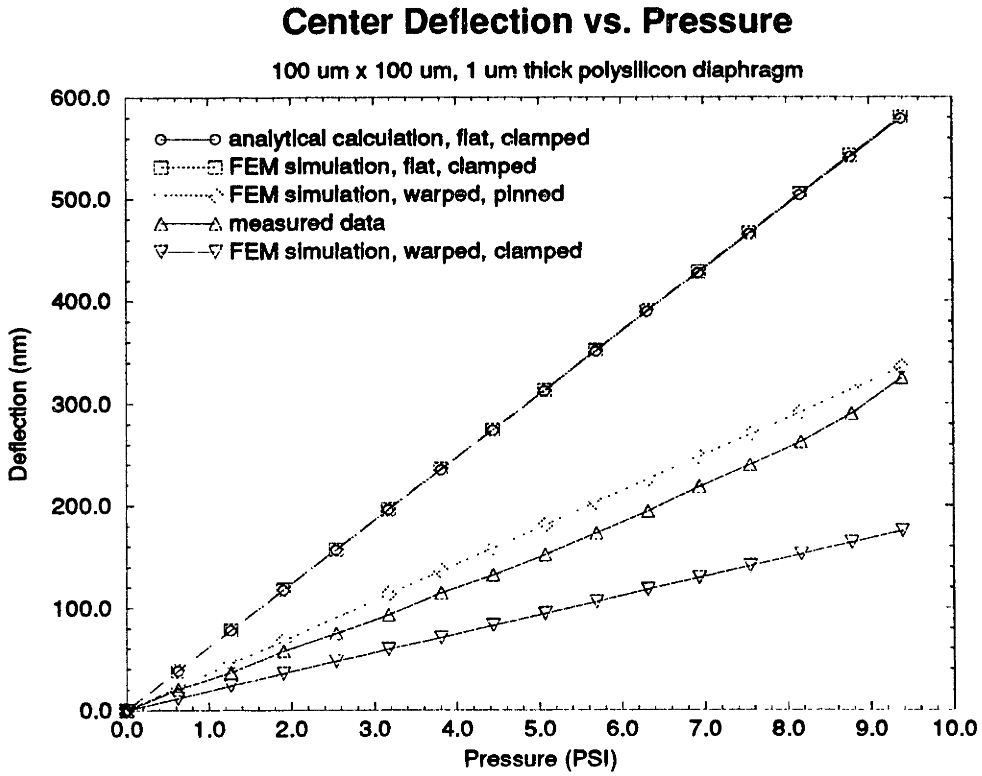


Figure 5.22: FEM simulations, analytical calculation, and experimental data for deflection versus pressure.

calculations estimating the capacitance change. Contrasted to the simulations are also shown the experimentally determined deflections obtained using optical measurements, and capacitance measurements. Since the latter detects only changes in capacitance, data is plotted assuming that the zero-pressure capacitance is the same as the simulated value (117.8 fF for the warped diaphragm case), and that the coupling capacitance value is 252 fF (the change in capacitance is calculated using Eq. (2.5)). The simulated capacitance for the flat diaphragm is approximately 82 fF, and is smaller since the effective gap is larger.

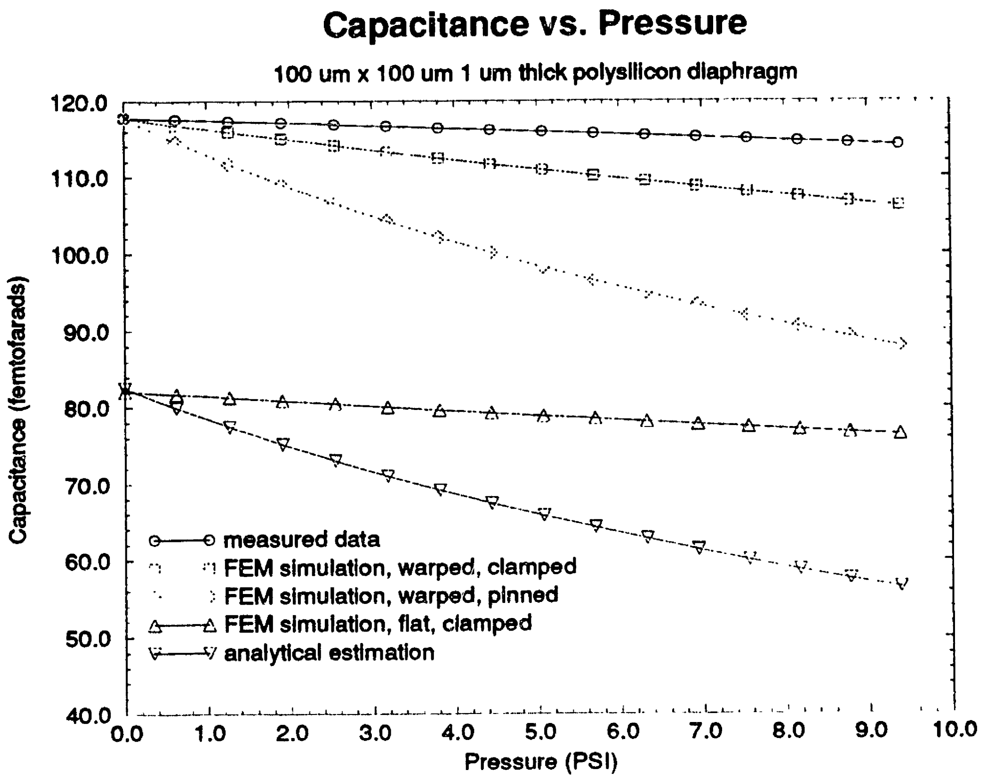


Figure 5.23: FEM simulations, analytical estimation, and experimental data for capacitance versus pressure.

5.6 Correlations of FEM Simulation to Measured Data

Correlation of analytical calculations of maximum center deflection to FEM analysis for the flat diaphragm agrees very well because Eq. (3.1) is exact. The deflections are much greater for the flat diaphragm case than all others, and this is because the warped diaphragm offers more stiffness due to its shape. Because the edge conditions of the real diaphragm lie somewhere between clamped (edges fixed in displacement and rotation) and pinned (edges fixed in displacement with rotations allowed), the measured deflection data lies within the window determined by FEM simulation, and the correlation is good, but takes into account only one point on the diaphragm (the center). The measured deflection data starts to curve upward as the pressure approaches 10 PSI, deviating from linearity, and this is because the shape of the diaphragm is starting to fundamentally change shape. This will be described later in the high-pressure data measurement section.

For capacitance changes in the flat diaphragm case, the analytical calculation overestimates the change, due to approximations of the actual diaphragm shape as deflections get larger, and also due to neglect of the fringing fields, especially near the bottom plate hole.

The correlation between FEM capacitance simulations of the warped diaphragm and experimental data differ due to several reasons :

1. The initial shape of the diaphragm is not modeled exactly. The capacitance is a strong function of this shape. The center deflection is not as dependent, and thus the data and FEM simulation are more in agreement for deflection, though perhaps coincidental since it is for only one point on the diaphragm.
2. The exact boundary conditions also determine the shape under deflection, and the capacitance change is a strong function of the shape.
3. Parameters which affect the exact shape of the diaphragm include residual stress and material properties of the film which are not exactly known for the buckled diaphragms.
4. Finally, the FEM modeling does not take into account the exact surroundings of the air-gap capacitor structure, which includes the pressure inlet and field oxidation regions. In the actual structure, the top plate sags into the bottom plate, causing it to nearly touch the bottom plate hole edge, and extend almost 0.8 μm into the hole. This was modeled in the FEM simulation as two conductors, one acting as the rigid bottom plate, while the the other as a warped plate sagging into the bottom plate. Field lines from the top plate can terminate on the underside of the bottom plate in the simulation, and this is not the case for the actual structure, which has lightly-doped silicon as sidewalls, and partly shields the bottom plate n+ region.

All of these contribute to the differences between the measured capacitance change and the simulated change.

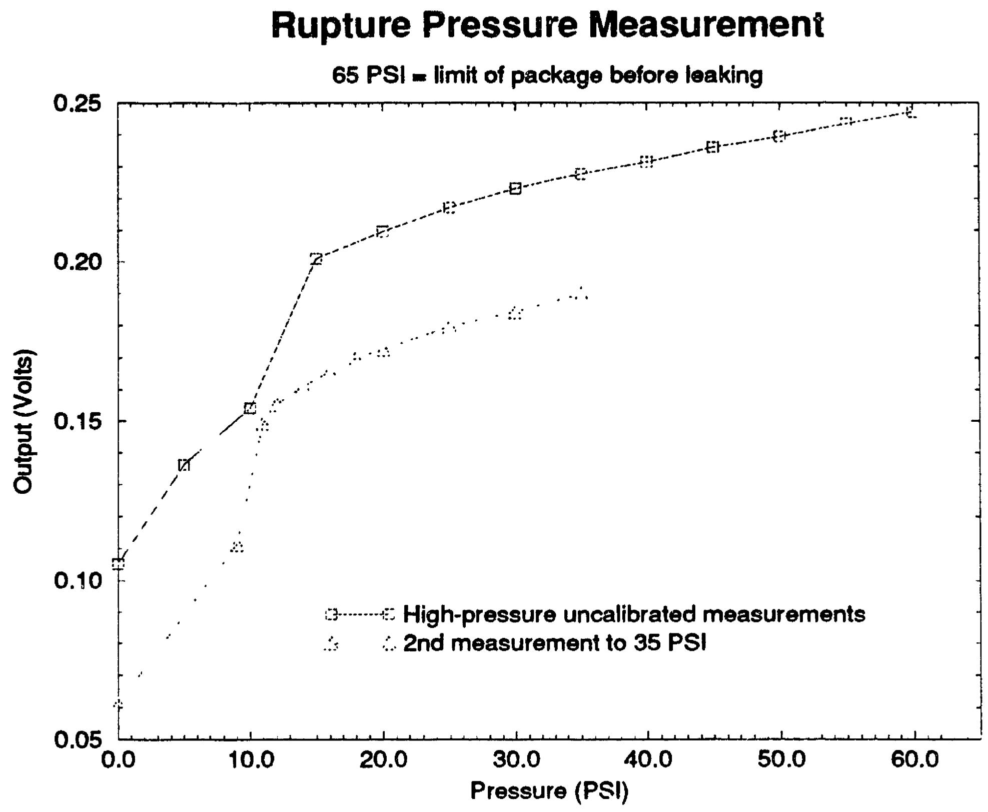


Figure 5.24: Capacitance versus pressure in the higher pressure ranges (65 PSI).

5.7 High-Pressure Measurements

A sensor was pressurized in the higher PSI range to observe fracture. Unfortunately, the PGA/tube interface is not designed to withstand larger pressures, and significant leakage occurred about 65 PSI. The diaphragms, however, could withstand this pressure without rupture.

Capacitance data was taken in the higher PSI range using an uncalibrated pressure gauge with an accuracy of 10%. Figure 5.24 shows this data. An unusual jump in capacitance occurs at around 10 to 11 PSI. From 0-10 PSI, the curve looks fairly linear, with a trend upward. At 15 PSI and above, the behavior asymptotically approaches a horizontal line. At

65 PSI, there was a leak in the packaging. The leak was temporarily fixed using epoxy, and the measurement retaken up to 35 PSI, with more measurements taken from 10 to 15 PSI to probe the anomalous region. Again, there is a jump in capacitance slightly past 10 PSI, consistent with the first measurement, along with a different offset voltage at zero-applied pressure. This offset is probably due to mechanical deformation of the diaphragm after the 65 PSI test.

From the capacitance data, it was conjectured that the cause of the discontinuity from 10 to 11 PSI was due to a radical change in the shape of the diaphragm. At zero-applied pressure, the diaphragm deflects downward, but at some critical pressure, the diaphragm might start to deflect upward, changing its shape dramatically. The change in offset at zero-applied pressure could be accounted for by considering that pressurizing up to 65 PSI and back down changed the mechanical structure. These hypotheses were experimentally verified shortly after the capacitance measurements by observing the diaphragm under pressure under an optical microscope. The diaphragm appeared to be flat at about 10 PSI, then started to bulge upwards slightly past this pressure. This data, however, was qualitative and gave only a visual record of the effect.

Quantitative results were obtained by pressurizing the diaphragm through the critical region (10-15 PSI) under the WYKO PMI instrument. Figure 5.25 shows the diaphragm at zero-applied pressure, while Figure 5.26 shows the diaphragm at 10 PSI. The diaphragm still retains its bowed shape downwards up to this point, so that the capacitance data has a slowly-varying slope. But at 11 PSI, the shape assumes a different form (Figure 5.27) and hence confirms the non-linearity of the capacitance data. From this point on, the bulge increases and the capacitance data approaches asymptotically a straight line.

There are three distinct regions in the capacitance and optical measurement data. The first region occurs from 0-10 PSI where the diaphragm essentially retains its bowed-down

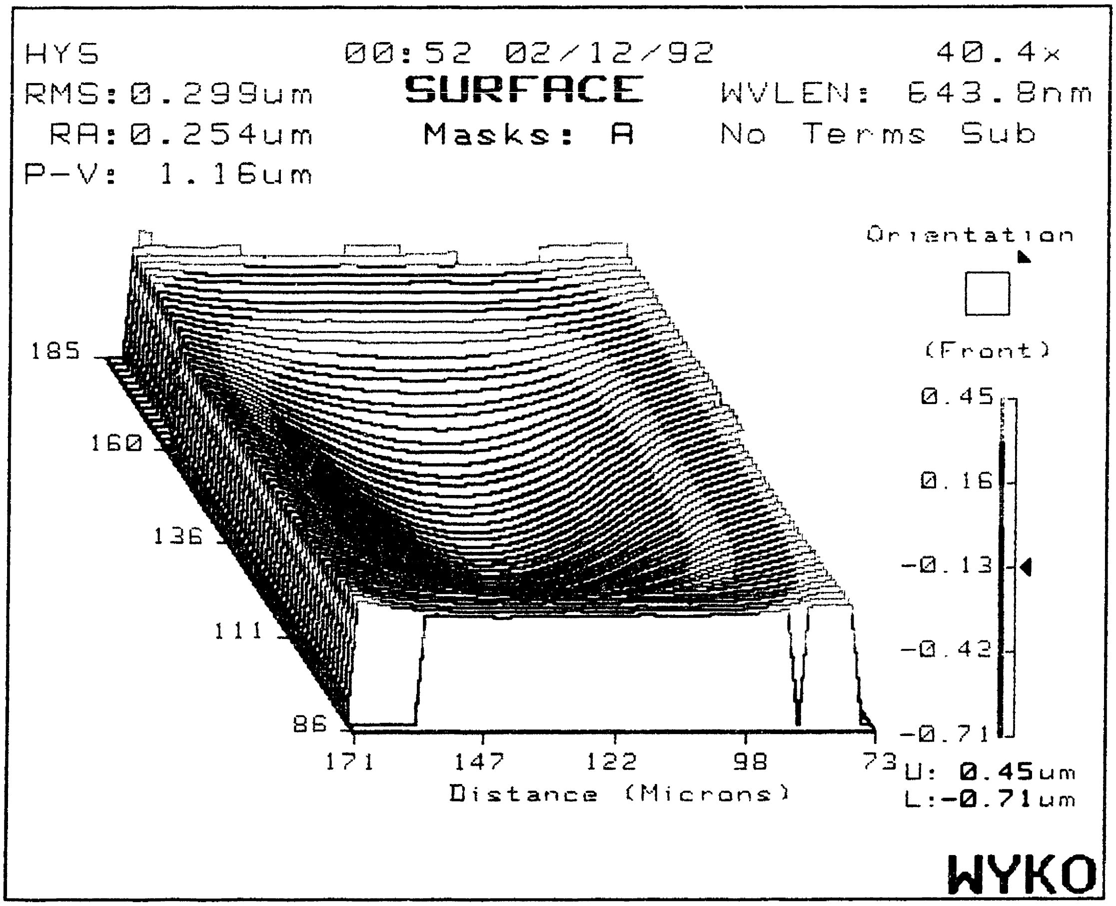


Figure 5.25: 3D surface mapping of a air-gap sense capacitor diaphragm with zero-applied pressure.

shape, deflecting in a range less than 1 μm. Capacitance data corroborates this, as it is linear in the low PSI range and starts to deviate from linearity. Slightly past this point, a critical transition region is reached where the shape of the diaphragm changes from deflecting downward to bulging upward in the center. This occurs at roughly 10-11 PSI. The capacitance data clearly shows this transition by a marked increase in capacitance which does not follow the previous behavior. Past the 11 PSI point, there seems to be a general trend upward with a capacitance roll-off that is expected since the diaphragm is moving away from the bottom plate incrementally with the same basic shape.

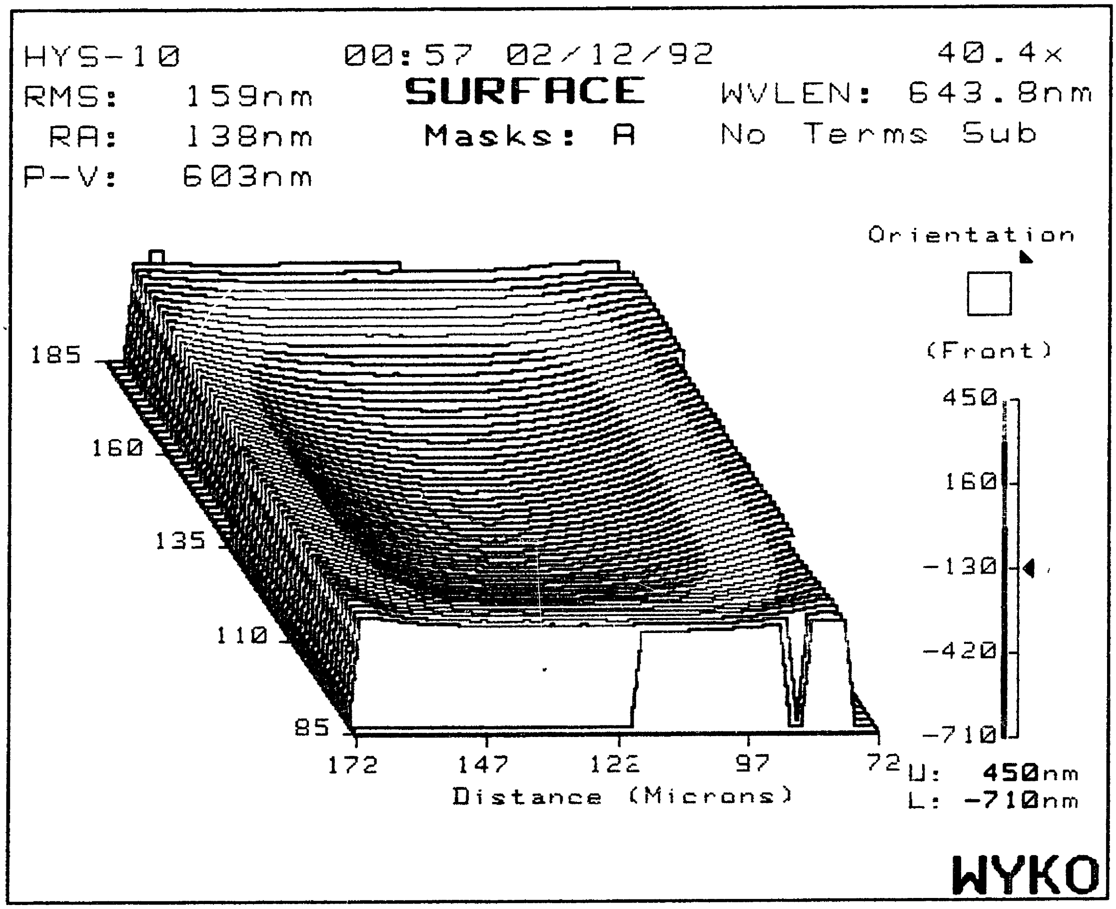


Figure 5.26: 3D surface mapping of a air-gap sense capacitor diaphragm at 10 PSI differential pressure.

To test mechanical hysteresis, the diaphragm was cycled up to 30 PSI, then back down to zero (Figure 5.28). Unlike the 65 PSI pressurization case where the drop in pressure from 65 PSI to zero was sudden due to a leak, this measurement was gradual and essentially static. Within the accuracy of the pressure gauge, there does not appear to be any mechanical hysteresis, and this was confirmed through visual monitoring. The diaphragm does dramatically change shape, but it is repeatable and smooth within the transition region.

The capacitance non-linearity at 10-11 PSI demonstrates a dramatic change in diaphragm shape as corroborated by optical PMI measurements. Similar behavior has been

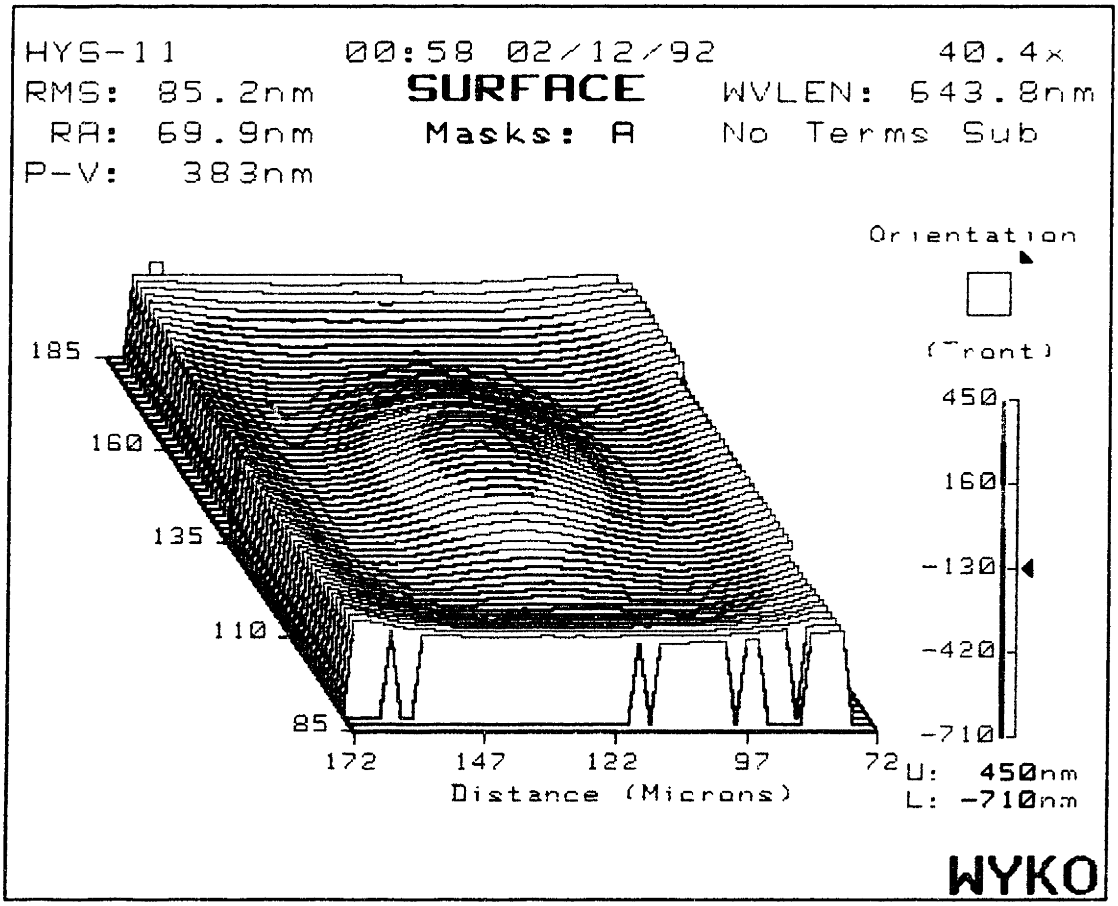


Figure 5.27: 3D surface mapping of a air-gap sense capacitor diaphragm at 11 PSI differential pressure.

observed before in silicon diaphragms in pressurized cavities where mechanical hysteresis was observed which allowed the diaphragm to pop in and out at different pressures [65]; however, in this case, it appears that the capacitance curve follows the pressure back down at approximately the same transition and does not demonstrate mechanical hysteresis.

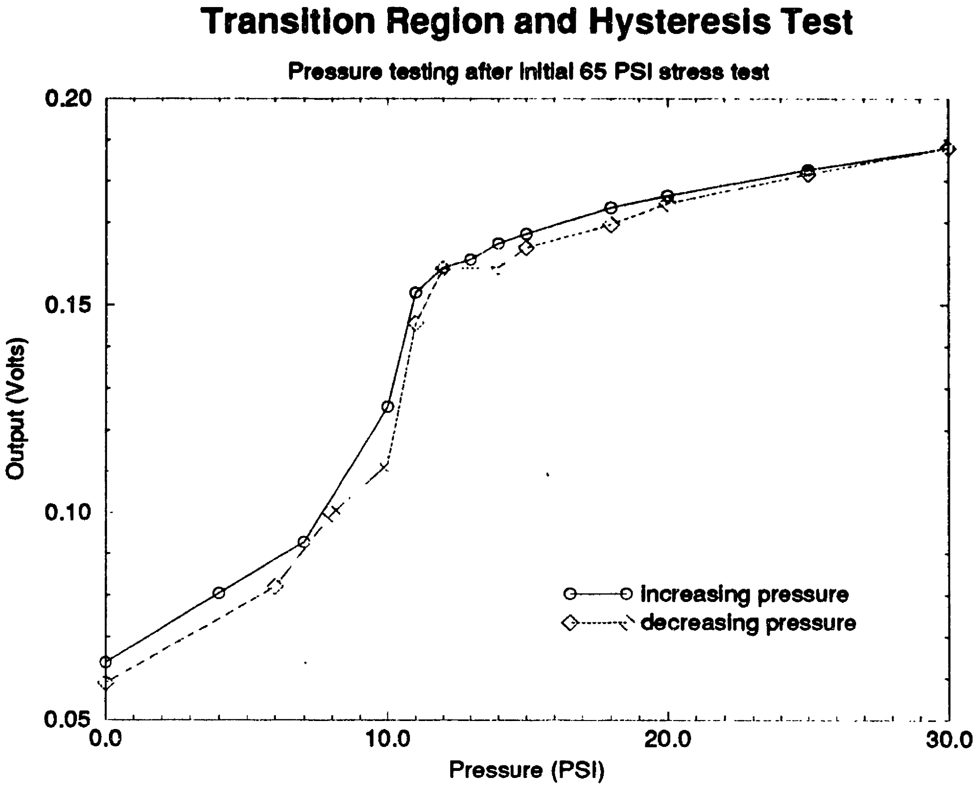


Figure 5.28: Critical transition region and hysteresis test.

5.8 Acoustic Measurements

The pressure resolution of the integrated capacitive pressure sensor is dictated both by capacitance change sensitivity and diaphragm compliance. The particular diaphragm tested within the capacitance measurement system exhibited about 60 mV change over 9.4 PSI yielding about 6.4 mV/PSI. Assuming that the resolution of the system for one isolated measurement is approximately 500 μV, then the pressure resolution is approximately 0.078 PSI.

The human ear has a frequency response of 20 - 20 kHz with a threshold of audibility of 2 x 10^{-5} Pa, and a threshold of pain of 20 Pa, all within a common-mode ambient of

0.1 MPa (atmospheric pressure) [66]. This threshold of pain corresponds to approximately 0.003 PSI and is an order of magnitude lower than the resolution of the static measurement. Thus it is expected that this sensor in its present form is not capable of measuring acoustic sound pressures common to human hearing without averaging. It does have an advantage, however, that the structural sizes and cavities involved are much smaller than the acoustic wavelengths common to human hearing, and hence there are no major resonance effects. Making the diaphragm thinner and stress-free may enable such a sensor to function as an acoustic microphone.

To probe the lower limit of pressure, however, acoustic measurements were performed. A 5-inch polypropylene midrange speaker with a response in the 500 Hz to 10 kHz range, and with a 94 dB sound pressure level (SPL) [1 watt input at 1 meter] was used to excite a diaphragm through the back-side hole of the substrate and the PGA package (with no tygon tubing attached) at a distance of 2.25 inches. A spectrum analyzer and a reference microphone (Shure SM57) at a distance of 2.25 inches was used to monitor the frequencies of an amplified sine wave input. Levels in the range of 20 - 40 Pa were generated, causing volume levels to equal or exceed the threshold of pain.

Measurement was performed by first using the reference microphone connected to a spectrum analyzer to search for any unusual resonances or response other than the frequency applied at the high-volume level. The Shure SM57 has a relatively flat frequency response in the 1 to 10 kHz range, and thus did not adversely affect the measurement. The loudspeaker did not show any unusually high distortion at high volume except for a small trace at 3.1 kHz, but this was at least 25 dB below the fundamental frequencies tested (1 to 5 kHz).

Following the measurement for unusual distortion in the loudspeaker, a sound pressure calibration measurement was performed using a Bruel & Kjaer Type 2235 precision sound level meter. A Type 1624 B & K octave filter was used and set on linear, capturing all

Frequency (kHz)	Sound Pressure Level (dB) [0 dB = 20 μPa]
0.00	84
1.00	120
2.00	122
3.00	126
4.00	125
5.00	128

Table 5.5: Sound pressure levels applied to the pressure sensor as calibrated by a B & K Type 2235 precision sound level meter.

frequencies. The position of the sound meter approximated closely the position of the actual chip while it was housed on the analog board. Measurements are in dB with 0 dB reference at 20 μPa (20 dB per decade change) which represents approximately the threshold of hearing for the human ear. Background noise of the measurement room was high, at 84 dB (approximately 40 dB higher than a quiet office room) but is probably still too low for the pressure sensor to detect.

The measurement then proceeded with the pressure sensor chip in place. Table 5.5 shows the SPL's for 6 differing levels applied to the pressure sensor.

The acoustic sound pressure data was taken on a pressure sensor chip that used a reference of -3 V. All FFTs unless otherwise noted were taken at a capacitance sampling rate of 11.111 kHz (master clock of 500 kHz) with rectangular windows. The x-axis represents frequency while the y-axis is magnitude, where a unit amplitude in time corresponds to a unit amplitude in frequency. The y-axis is plotted in power notation so that reading dB off the scale is easily done by multiplying the exponent by 2. Plotting in dB directly would not reveal so well the differences in the peaks and the noise floor (since the difference is not that great), so the scale is linear. Also, all FFTs were taken after the average value was removed from the data, thus removing the large peak at DC and enabling easier scaling.

Figure 5.29 shows the 4096 pt FFTs of the data with zero-input, The peak-to-peak

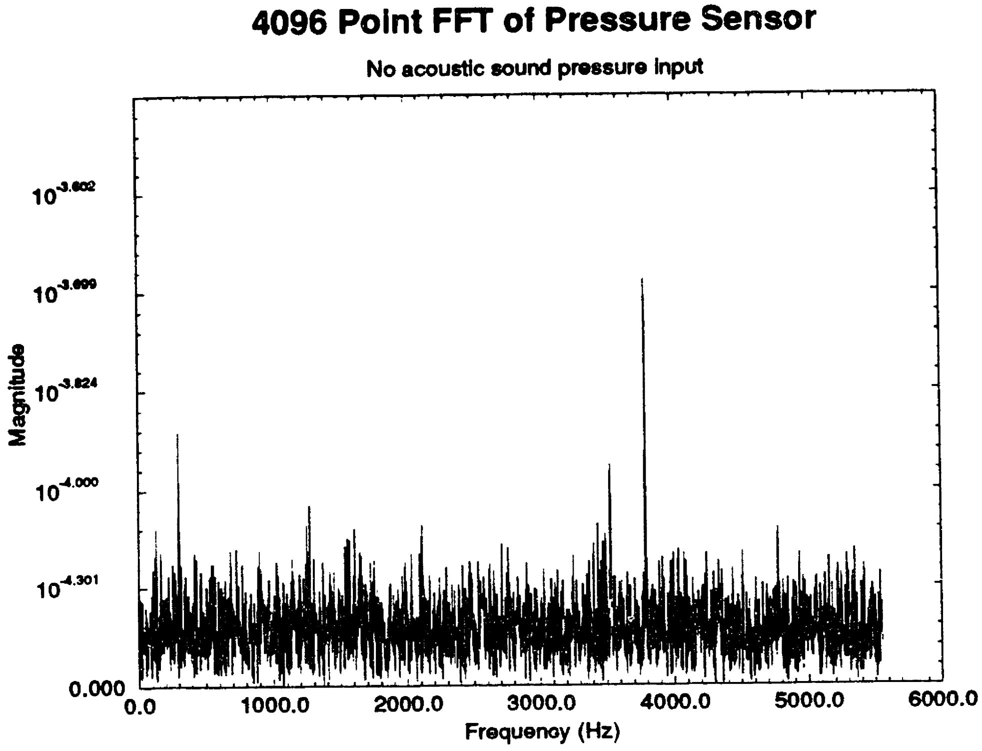


Figure 5.29: 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for no input.

amplitudes were only a few mV, indicating a code sweep of less than 16 codes at 16 bits, so there is quantization noise evident; however, the analysis is enough to indicate the presence of a sinusoidal signal as will be seen in the next few graphs.

In the zero-input data there appears to be a peak at 3.8 kHz, although it is only a few dB above the noise level. This peak could be due to some noise generated in the system, particularly the master clock. The ratio of 500 kHz to this peak is nearly 128, and since there are numerous counters and other digital circuitry in the system, this appears to be the cause. Several other FFTs were taken at master clock frequencies of 250 kHz and 1 MHz, and both indicate a shift of the noise peak from 3.8 kHz to about 1.76 kHz and 7.56 kHz respectively, indicating that the master clock or derivations of it are responsible for the 3.8

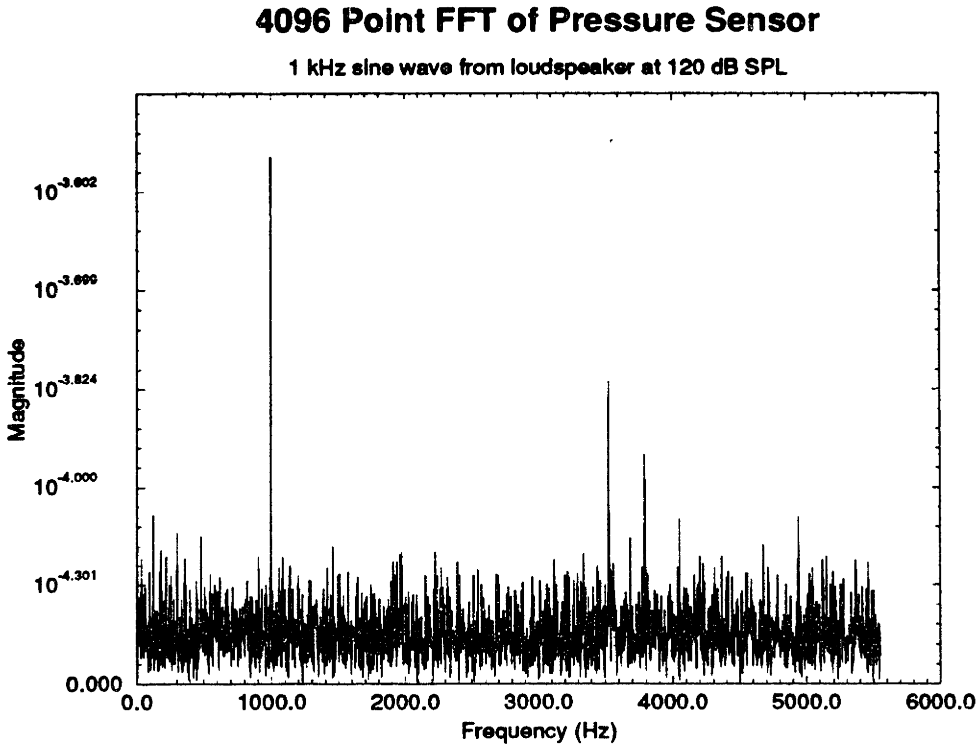


Figure 5.30: 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for 1 kHz sine wave input from a sound source at 120 dB SPL.

kHz peaks in the FFT data taken using a 500 kHz master clock in the system.

The next few graphs show the FFTs for frequencies of applied acoustic sound pressures. In Figure 5.30, the FFT at 1 kHz appears sharp, rising 6 or 7 dB above the noise floor, with another peak at 180 Hz probably due to harmonics of 60 Hz noise which are occasionally seen. In Figure 5.31 at 2 kHz, the FFT again appears sharp, but with peaks at 3.5 and 3.8 kHz. These peaks are probably associated with the master clock and the digital circuits. FFTs were taken up to 5 kHz, and all of them revealed these same features.

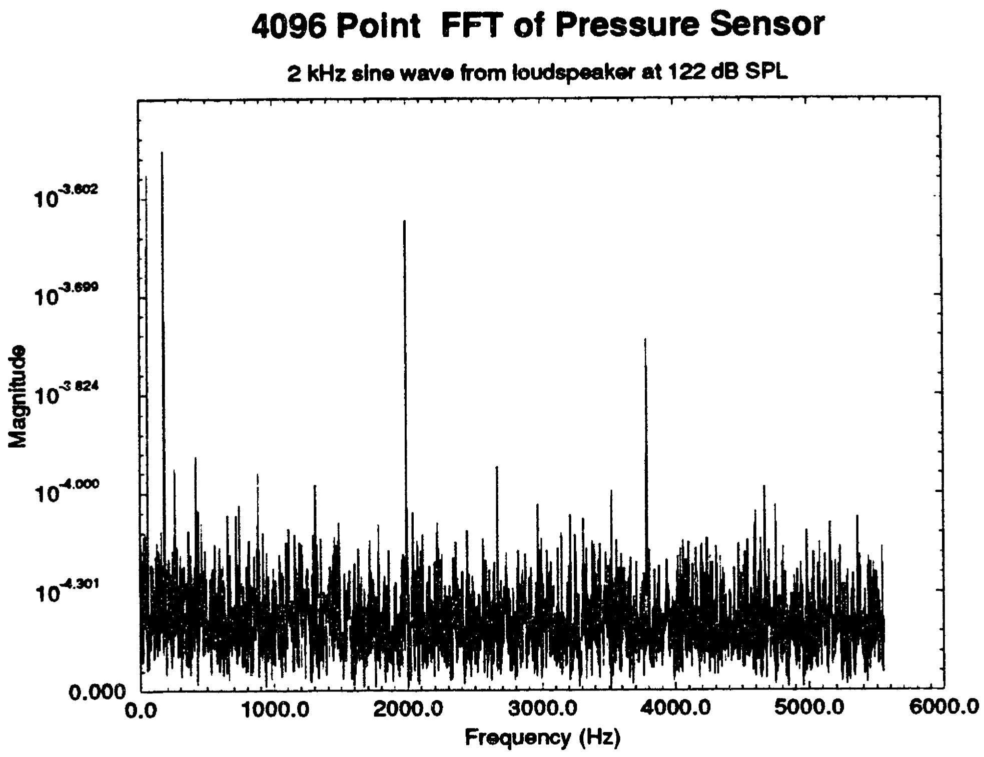


Figure 5.31: 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for a 2 kHz sine wave input from a sound source at 122 dB SPL.

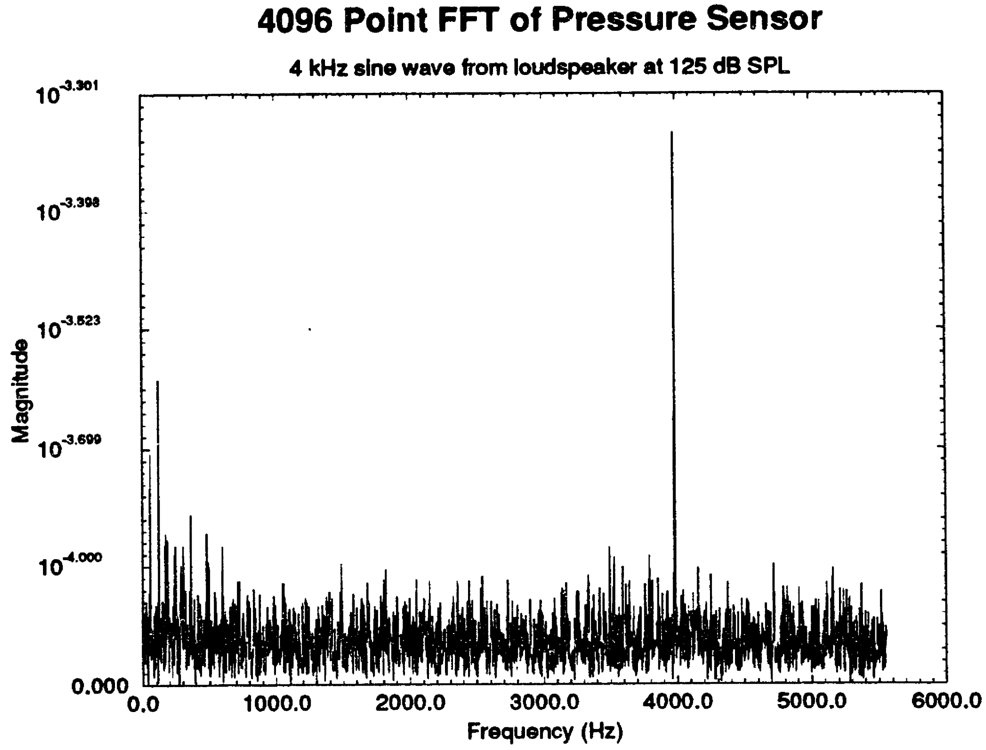


Figure 5.32: 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for 4 kHz sine wave input from a sound source at 125 dB SPL.

Since the loudspeaker and its input leads were not very far from the analog test board, it was possible that the low signals evident in the 4096-point FFTs were not due to acoustic pressure response of the diaphragm, but rather from the electrical signal emanating from the amplifier to the loudspeaker inputs. At 120 db SPL and higher, the voltage input to the loudspeaker is fairly high (25-30 V or so), so this source of noise was investigated. A 4 kHz sine wave signal was chosen as the input since it gave a larger response when the sound field was directed at the pressure sensor. A 4 kHz sine wave signal was applied to the loudspeaker with the speaker on-axis with the sensor (Figure 5.32). The 4 kHz signal is clearly detected. The test was then repeated, except that the speaker was positioned off-axis from the sensor at an angle of 90 degrees. This allowed for negligible sound pressure to reach the pressure sensor while at the same time allowing the capacitance measurement system to feel the full electrical noise effects of the large electrical signal reaching the loudspeaker inputs.

Figure 5.33 shows the results of the 4 kHz sine wave test with the sound field directed 90 degrees away from the pressure sensor. There is no 4 kHz signal, and a few peaks which seem to indicate noise sources similar to what was seen with no acoustic input. Hence, this test shows that acoustic sound pressure at approximately 125 dB SPL was the source of the FFT signal peaks seen earlier, and not the effects of electrical noise from the input of the loudspeaker.

Finally, Figure 5.34 and Figure 5.35 show a 4096 Point FFT of the *calibration voltage* for the 4 kHz sine wave measurement. The majority of the noise components in the calibration voltage are due to 60 Hz noise and its odd harmonics at 180 Hz and 300 Hz. It is suspected that these emanate from noise coupling from the AC power line. This FFT is typical of all the measurements. The magnitude of the noise is larger than in the actual capacitance measurements, demonstrating that the system can also attenuate these noise components, although not completely. Sampling at multiples of 60 Hz can be used to reduce these noise

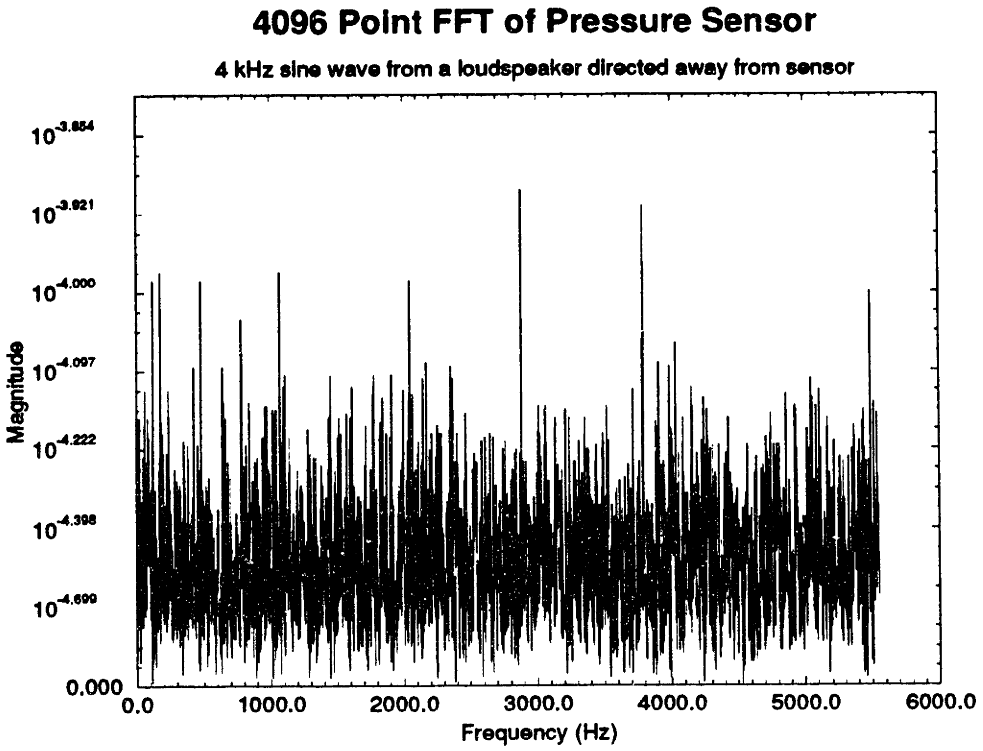


Figure 5.33: 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for 4 kHz sine wave input from a sound source at 125 dB SPL directed at 90 degrees away from the pressure sensor. Note the scale change.

components since they will appear as a DC offset.

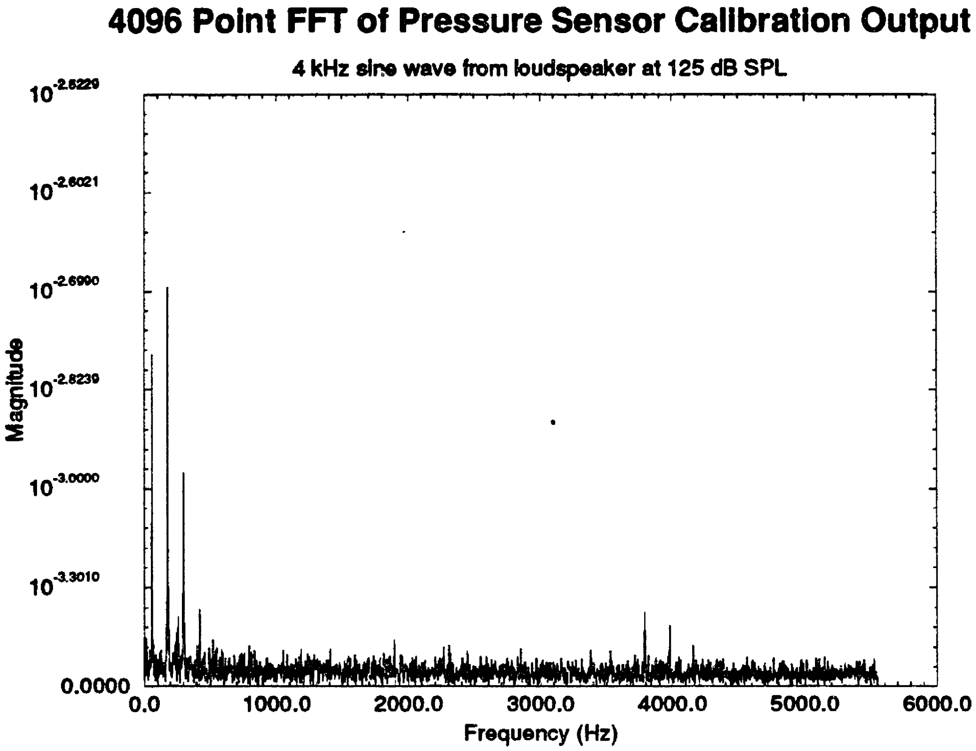


Figure 5.34: 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for 4 kHz sine wave input from a sound source at 125 dB SPL directed at the pressure sensor on the calibration voltage.

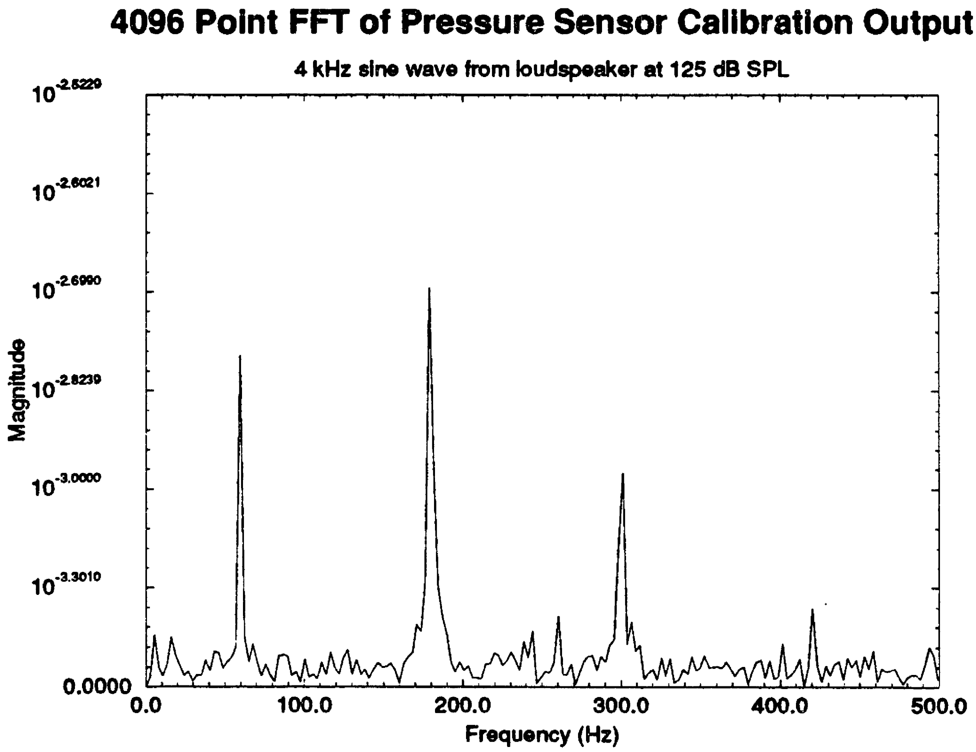


Figure 5.35: Closeup of 4096 point FFT using a rectangular window at a sampling rate of 11.111 kHz for 4 kHz sine wave input from a sound source at 125 dB SPL directed at the pressure sensor on the calibration voltage.

5.9 Resolution

Previously, it was deduced from standard deviations on static applied pressures that the resolution of the system approached the standard deviation of the measurement, and this in turn produced an approximate pressure resolution based on mV change/PSI as determined from empirically determined pressure curves. Using a resolution of 500 μV, this gives approximately 0.078 PSI as the resolution for a single measurement with no averaging, and corresponds to a capacitance change of 31.5 attofarads. However, acoustic sound pressure measurements at 125 dB SPL are 36 Pa in amplitude, yielding variations of 0.005 PSI, an order of magnitude smaller than the predicted resolution from standard deviations in static pressure tests. This increase in resolution is the FFT averaging out of spurious 60 Hz noise (and its harmonics) in the system which tend to increase the standard deviations of static pressure measurements, but do not mask the small signal measurements made at higher frequencies, and also due to effective averaging of random noise since a 4096-point FFT is used to resolve the small-signal inputs. If standard deviations are on the order of a few hundred microvolts, then extensive averaging on white noise can reduce the noise by a factor of 64 for 4096 samples. Thus, this is consistent with the fact that the 4096-point FFT can resolve smaller pressure inputs.

Optical measurements show that for static pressures, the deflection is approximately 70 nm/PSI in the small pressure regime (0-10 PSI). If the system is able to detect small-signal 0.005 PSI changes, this corresponds to 0.4 nm or 4 angstrom deflection, and a change in capacitance of 2 attofarads. This is possible, since common-mode vibrations are eliminated (because the sense and reference capacitor are similarly affected), or are suppressed because they are low-frequency vibrations which do not mask the higher frequency sound pressure inputs.

Chapter 6

Conclusions and Future Trends

The reasonable man adapts himself to the world; the unreasonable one persists in trying to adapt the world to himself. Therefore all progress depends on the unreasonable man.

SHAW

The obscurest epoch is today.

STEVENSON

6.1 Conclusions

An integrated capacitive pressure sensor research vehicle for charge-redistribution techniques has been presented which demonstrates capacitance-change resolution of 30 attofarads for a single measurement without averaging. With averaging in the digital domain, better than 3 attofarad resolution is demonstrated. A unique combination of surface and bulk micromachining integrated into a standard existing MOS process enabled reasonably fast development time without compromising system performance. A capacitance measurement system was designed as part of the integrated capacitive sensor system, enabling testing of future chips which may react to stimuli other than pressure.

The fabricated test chip within the measurement system responded to static pressures as high as 65 PSI, and to small signal acoustic sound pressure inputs in the 20 Pa range, or 0.0029 PSI.

Optical deflection measurements were performed using a phase measurement interferometry surface profiler, and this yielded unique results. This is the first load deflection measurement of this kind on capacitive integrated pressure sensors in the 100 fF range. Deflections in the 20 to 350 nm range were observed, plotted versus applied pressure, and compared with FEM simulations. At the same time, the PMI technique was used to quantify the buckled nature of the diaphragm and allow more accurate FEM modeling and simulation. Finally, the PMI technique was able to correlate with capacitance measurements in the critical transition region of the diaphragm where it dramatically changes shape. This enabled separate verification that the capacitance change detected by the system was due to deflection of the polysilicon plate by applied pressure, and not by some other physical mechanism.

6.2 Future Trends

Further work in the area of integrated capacitive pressure sensors include enhancements from two different directions. From the processing side, improvement of materials and reduction of stress in thin films, development of sandwich, composite thin film layers, and better uniformity and repeatability of films are a must in manufacturing highly sensitive and repeatable sensor structures. Surface micromachined structures rely on good thin films.

In surface micromachining, developments in dry-etching technology, resists and films for etch protection, and a better understanding of the surface-sticking mechanisms evident in releasing structures are needed to make surface micromachining more viable for sensor and circuit integration and manufacturing.

Bulk materials such as single crystal silicon, on the other hand, offer better control of material properties and reduction of stress, but are difficult to machine using bulk micromachining, where dimensions are not so well defined as in surface micromachining. Also, bulk micromachining is not as amenable to standard IC processing and hence process integration, yet it offers attractive packaging possibilities. Reliable, low-temperature silicon bonding and more suitable, compatible etchants are making this a viable alternative.

On the circuit side, improvements can be made in two areas. For higher accuracy and more immunity to noise, oversampling and sigma-delta techniques [67] may be used, whereas in less accurate but smaller systems, integration of the entire capacitance system may be implemented. In both cases, however, process integration of the sensor structures with circuits is desired.

This thesis has shown that aspects of surface micromachining can lead to easier integration with circuits and higher performance, yet also demonstrates that bulk micromachining can yield structures easier for packaging. It also demonstrates that using the capacitance transduction technique is technology independent to a large degree. Piezoresistive technology cannot claim such high accuracy or sensitivity, but can claim ease of manufacture and simplicity. However, as technology advances to the point where good thin films and/or machining techniques become integrable with MOS or bipolar circuits, capacitance transduction will become a competitive alternative.

Appendix A

Measurement System Components

A.0.1 The Host Computer

An important module in the measurement system is the host computer. It consists of an IBM PC XT running Borland C++ software written to control a Qua Tech PXB-721 parallel expansion board. This board consists of several Intel 8255's allowing both input and output on 3 34-pin headers. The computer's main role is to set up a user-friendly interface to control all aspects of the measurement, and to extract, store, and analyze the raw data from the main memory unit on the digital motherboard.

A.0.2 The Digital Motherboard

The block diagram of the digital motherboard is shown in Figure A.1. It consists of two Intel 2732-A EPROMs that contain the micro-code used to drive a finite-state machine which controls the switching sequences, on-board SRAM (Fujitsu CMOS 262,155 word x 1

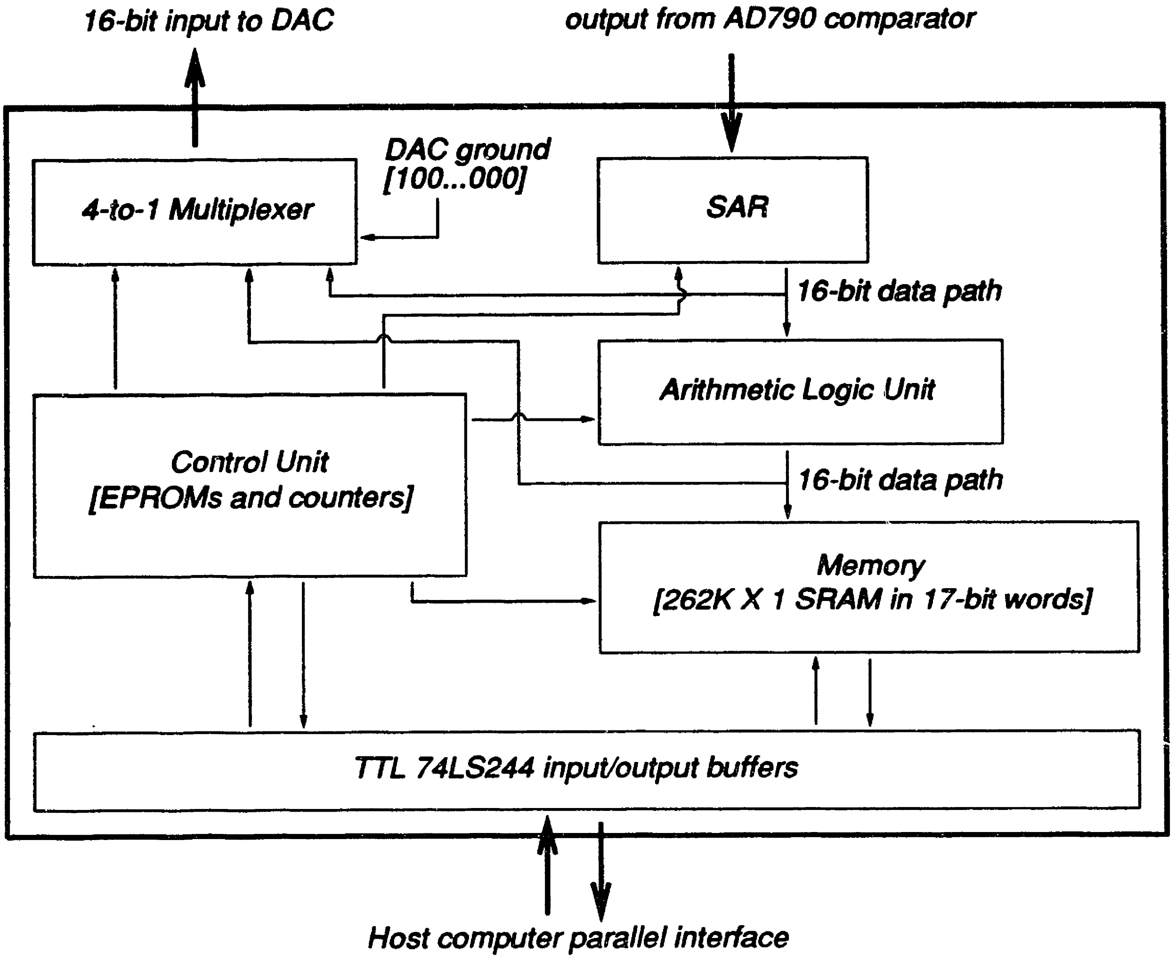


Figure A.1: Digital motherboard block diagram.

bit, MB81C81A), synchronous counters (National Semiconductor MM75H163 and/or TTL equivalents), temporary register latches (MM74HC573), random TTL logic, an ALU/carry-look-ahead for real-time subtraction and inversions (MM74HC181 and MM74HC182), TTL output buffers/drivers (74LS244), built-in master clock generator circuit, various multiplexers, and two fast, cascaded TTL SARs (DM2504) for 16-bit operation.

The master clock controls the clock inputs for the counters, and the inverse of this clock is used to control the de-glitch D-flip-flops which buffer the EPROM outputs to control other counters. This allows only one clock to be used as the master, but introduces a delay to the system of one-half the clock period. This is because the outputs of the EPROM change on the rising edge, but are not effectively latched until the falling edge. However, the clock period is slow enough that one-half the period at 1 MHZ is 500 ns which is enough time for most signals to settle before another change is initiated. The clock is generated internally using a Fox F1100 4 MHZ oscillator chip, divided down using a counter, and finally buffered using 74LS244's to an output BNC connector. This output can be manually switched on the board from 250 kHz, 500 kHz, 1, 2 and 4 MHz. A separate input for the master clock is provided so that an external clock generator can be used if desired.

The outputs of the digital board control switches S1 and S2 (this switches the bottom plates of C_R and C_S) and S3 which controls the grounding of the top plates of the capacitors. These outputs are open collector TTL inverters which are meant to interface with opto-isolators on the analog interface board since they are current-driven. There are also 16 digital outputs via ribbon cable to the DAC box, and digital inputs/outputs to the host computer. The other inputs are the master clock input, power supply, and the comparator output from the analog interface board. All of these enter via BNC coaxial connectors.

Although a ground plane is not necessary, one is employed for the digital motherboard. Gold DIP sockets soldered in place, point-to-point soldering with wire-wrap wire, and enclosure in a metal box complete the final assembly.

A.0.3 The Digital-to-Analog Converter Box

The DAC box was designed and implemented specifically for this application. It is a self-contained 16-bit non-clocked parallel-in digital-to-analog converter. It contains an Analog Devices hybrid, 16-bit current DAC (AD DAC72C-COB-I), a current-to-voltage conversion circuit (AD840JQ opamp), and a modular high-precision analog power supply (AD Model

905) built on a ground plane with gold DIP sockets, point-to-point wire soldering, power supply shielding, and enclosed in a grounded metal cabinet. It is a self-contained unit that is powered from a 120 V, 60 Hz EMI/RFI filtered outlet. This unit was carefully calibrated using an HP voltmeter (3468A multimeter) calibrated to a Data Precision voltage reference supply (model 8200), and was subsequently left on after calibration (1+ years) and checked before use. No re-calibration was needed.

The DAC72C-COB-I settles to 0.003% of FSR with a 1 kΩ load in 1-3 μs and with the AD840's 400V/μs slew rate, 0.01% settling in 100 ns, and 400 MHz gain bandwidth product (gain = 10) as the current-to-voltage converter, this DAC can be operated in a 16-bit parallel fashion at rates up to 1 MHz, with conversion times of 16 μs. Full scale voltage is 10 V from -5 V to +5 V, where 1 LSB is 153 μV. Output with all bits high is -5 V with a measured peak-to-peak noise of 45 μV.

Inputs are 16-bit parallel digital via ribbon cable, and output is a single analog output via a BNC coaxial connector.

A.0.4 The Analog Test Chip Interface Board

The interface board is necessary because for noise reasons, the test chip should be isolated from the digital part of the system. Figure A.2 depicts this fourth major component. It houses the test chip, opto-isolators (HPCL-2300), current source bias for the test chip (npn/pnp cascode mirror), and a high-speed comparator (AD790). It is built on a ground plane to minimize noise. All signals enter through BNC coaxial connectors as indicated by the circles in the figure.

The opto-isolators translate the signals from the digital motherboard (de-glitched EPROM outputs to open-collector inverters) to a -5V to +5V level in typically less than 100 ns. This

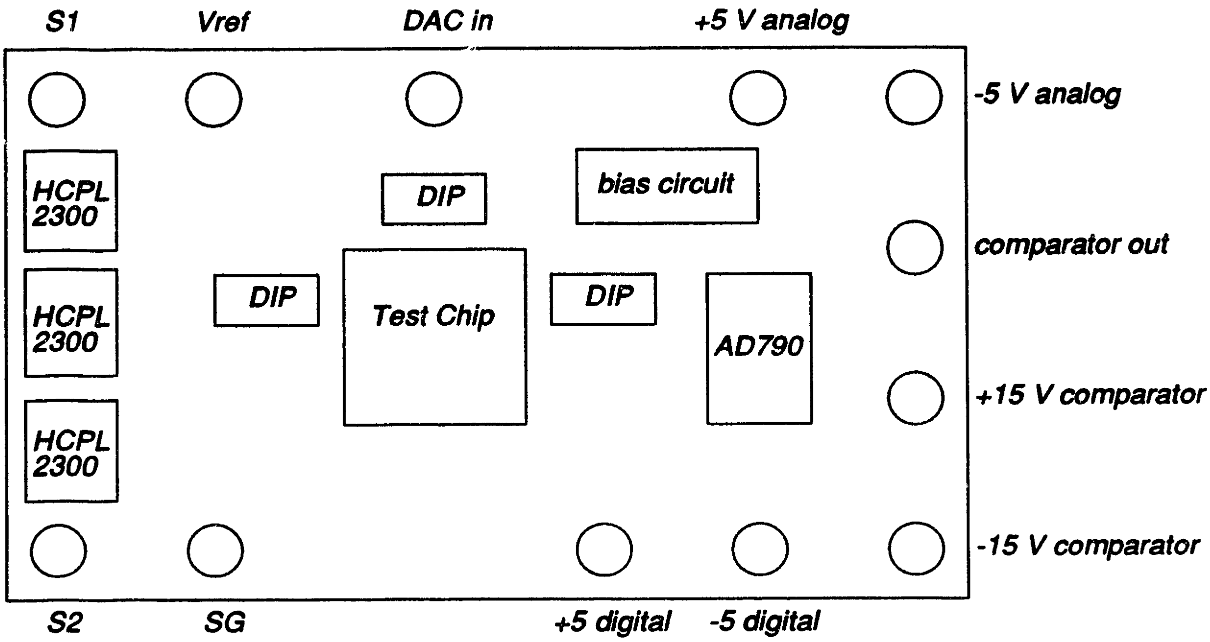


Figure A.2: Analog test chip interface board.

output controls the MOS switches on the test chip. This level-shift was necessary due to the requirements of the test chip switching transistors.

A current bias circuit is employed using a cascoded pnp (2N3906) transistor current mirror connected to the collector of an npn (2N3904) with its base grounded, and its emitter connected to a potentiometer, with the other end connected to a precision voltage source.

Various mechanical DIP switches are used to route signals from the interface board to the test chip since the chip houses several circuits. Electronic switches are not implemented due to possible noise from the digital control signals.

The output of the test chip is a differential analog voltage signal, but serves only as a pre-amp stage to the AD790, which is an extremely fast single-ended voltage comparator (35 ns) with low input offset (250μV) and high input voltage resolution (1 mV).

A.0.5 Power Supply Distribution System

The power supplies used in the system are extensive for noise de-coupling :

- The host computer resides on a separate AC outlet circuit and contains its own power supply. All other supplies are on EMI/RFI filtered taps from a separate AC power circuit.
- The digital motherboard contains many digital chips (including 17 262K x 1 SRAMs) which consume much power. Idle power is about 7.5 watts from a 5 V supply. This supply is a variable 0-10V, 0-10A HP power supply (model 6282A) which can handle 10 A at 5 V.
- The DAC box contains its own power supply.
- The analog interface board uses several supplies. The opto-isolators use 2 power supplies for +5V and -5V levels from an HP. power supply (model 6235A).
- A custom-built analog supply containing 2 AD Model 923 triple-output power modules power the following components : the AD 709 comparator (±15V, +5V), and the test chip, ±5 for the analog preamp. The digital VDD/VSS for the test chip uses the same supply as the opto-isolators. There is no crosstalk since when the opto-isolators are not active, neither is the digital circuitry on the chip.

Extensive, thick copper wire is used to tie the grounds of all supplies to the same point, avoiding ground loops. No daisy-chaining of supplies or grounds is employed.

All chips in all the components mentioned employ 0.1 μF bypass ceramic disc capacitors at VDD and/or VSS pins, and the boards employ large electrolytics at the BNC coaxial connectors for each supply.

A.0.6 Precision Analog Reference

A Data Precision voltage reference model 8200 is used as the reference for the test chip, and another one is used for the current bias reference circuit. These were calibrated before measurements were taken.

A.1 Measurement System Operation

Briefly, the system operates as follows. The computer sets up all the necessary initialization and sends the control signals to the digital motherboard via parallel interface I/O ports. The EPROM address is controlled by a counter, and the outputs of the EPROM represent the proper control signal sequences. These outputs change on one edge of the clock and are latched on the other edge of the master clock. This prevents any glitches from the EPROM output. All 4 measurement algorithms are implemented in one EPROM but at different addresses.

When a start signal is given to the digital motherboard, a counter counts through the EPROM. The EPROM outputs are latched and are sent to various places. For switching voltages on the capacitors, the signal is sent to open-collector TTL inverters that drive BNC cables to the analog motherboard which contain opto-isolators that level shift the TTL signal (0 V to 5 V) to -5 V to 5 V. They also isolate noise since the opto-isolators have their own power supplies. These signals are meant to drive MOS switches. The EPROM also controls the flow of digital information to the DAC since the DAC receives information from either a register or the SAR.

Once a switching sequence has been made, the EPROM starts the A/D conversion and waits approximately 17 cycles for the 16-bit conversion to finish. It then stores this into its main on-board memory. This memory is arranged in 17-bit words, and there are 262K words available. 17-bits are needed because for the digital subtraction algorithms, a possible overflow bit is stored.

If the analog algorithm is used, this first A/D conversion value ($V_{DAC_{cal}}$) is stored in a register, sent to the ALU for inversion, and sent to the DAC before the next switching sequence begins (the measurement cycle). When the measurement switching sequence finishes, another A/D conversion is initiated and this value is stored in main-memory. The EPROM controls all write functions into main memory as well as address increment.

For the digital algorithms, two latches are used to store the A/D conversion after calibration ($V_{DAC_{cal}}$) and after the measurement ($V_{DAC_{meas}}$), then a real-time subtraction using the ALU is performed, and this result written into main memory. This operation requires 17-bit memory words since the binary representation of the data after subtraction is not standard, and requires storage of the carry bit. This data is interpreted later in software.

This series of data acquisitions can either be done slowly and displayed in real-time (meaning the data is acquired, then extracted from main memory, and displayed – called *meter mode*), or can be done fast by having the system repeat the measurements and fill the entire main memory (*fill-memory mode*). The host computer can then download this data (or parts thereof) and analyze it. The latter allows for fast sampling of the capacitance change.

A more detailed hardware and software discussion of the digital measurement system is contained in [60].

Appendix B

Detailed Process Flow

B.1 Fabrication Sequence

The Integrated Circuits Laboratory at MIT operates a baseline 1.75 μm twin-well, double-level CMOS process in which a subset of it is used in the sensor/circuit process [49]. This subset consists primarily of the NMOS transistors and single-level metal. In the fabrication sequence, none of the critical implants or recipes are changed; in fact, only proper sequencing of available steps offered by the laboratory is needed to achieve the process integration of the NMOS transistors and air-gap capacitors.

The fabrication sequence is broken up into three phases. The first phase details device processing identical to NMOS, with easy generalization to CMOS. Phase II covers the steps used to integrate both the devices and sensor structure using shared steps, and finally phase III covers the back-side fabrication sequence used to form the air-gap capacitors.

B.1.1 Phase I : Device Fabrication

The fabrication sequence begins with a 100 mm diameter p-type (boron) 100-orientation silicon wafer (15-20 Ω-cm) with its back-side polished to a mirror-like finish (Figure B.1). This facilitates IR alignment at the end of the process.

A 43 nm stress relief oxide is grown at 950°C for 115 minutes before deposition of a 150 nm LPCVD silicon nitride layer at 800°C for 86 minutes (Figure B.2 and Figure B.3). This is used in a MOS process for LOCOS (local oxidation of silicon) field regions and active area definition.

The silicon nitride is patterned and plasma etched in SF_6, uncovering field oxide regions (Figure B.4). This is followed by a p-field ion implant. This lies under the field oxide and prevents parasitic MOS transistors from turning on by raising their threshold voltage (Figure B.5). The resist is then plasma-ashed and a 500 nm field oxide is thermally grown using a wet/dry/wet oxygen sequence of 30 min/160 min/30 min at 950°C (Figure B.6). The nitride is then wet-stripped in Transene etch (150°C for 45 minutes) after which the stress relief oxide is wet-stripped using 7:1 BOE etch for 35 seconds (Figure B.7).

A dummy gate oxide of 22 nm is thermally grown at 950°C for 35 minutes in dry oxygen (Figure B.8) and a series of ion implants are done to adjust electrical characteristics of the NMOS transistors (Figure B.9). The first is an N-punch-through ion implant (boron,

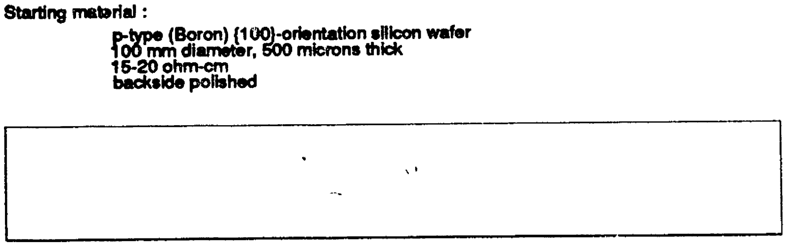


Figure B.1: Starting wafer material.

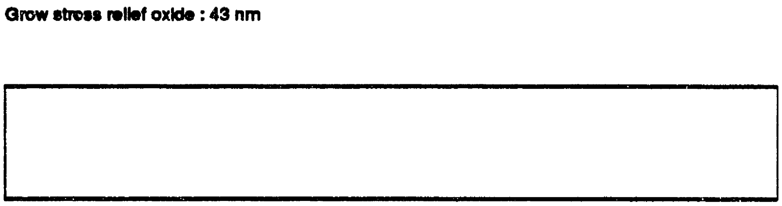


Figure B.2: Stress relief oxide growth.

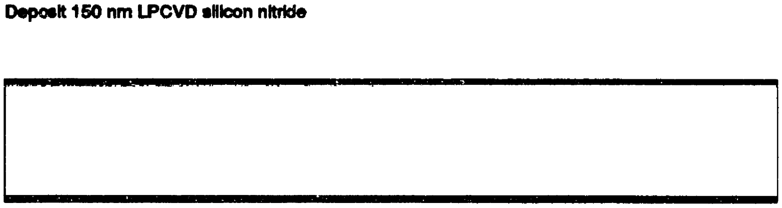


Figure B.3: Silicon nitride deposition.

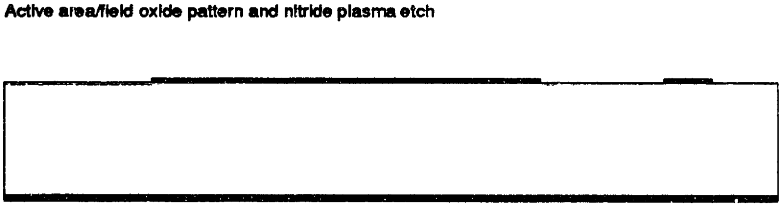


Figure B.4: Silicon nitride patterning and etching.

dose = 6 x 10^{11}, energy = 100 keV) which is a deep implant and prevents the drain-substrate depletion region from contacting the source-substrate depletion region. This is followed by another boron implant which is a shallow implant which adjusts the threshold voltage (boron, dose = 1.5 x 10^{12}, energy = 30 keV). The dummy gate oxide provides protection of the interface from implant damage as well as reducing the Kooi effect [47] which occurs during field oxide growth whereby a thin layer of nitride can form on the silicon surface. This can cause thin spots when the gate oxide is grown, but can be avoided by using a sacrificial "dummy" gate oxide which removes any nitride after stripping, which is the next step, and is done as part of the RCA clean before any diffusion/deposition except that a longer 50:1 DI/HF dip is done (5 minutes rather than 15 seconds) to remove this dummy

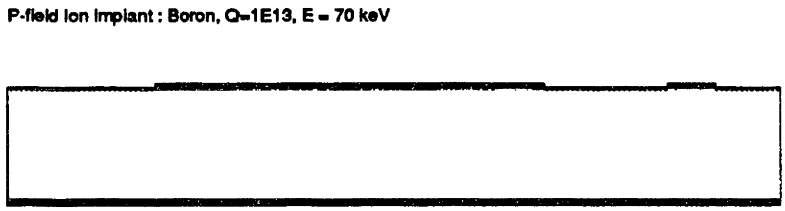


Figure B.5: P-field ion implant.

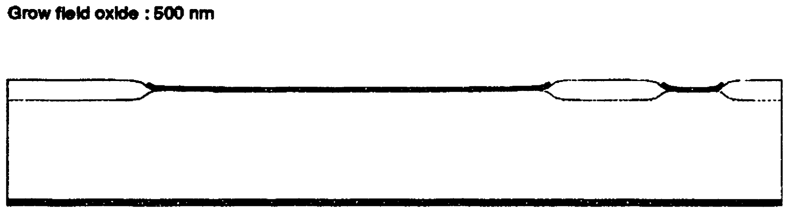


Figure B.6: Field oxide growth.

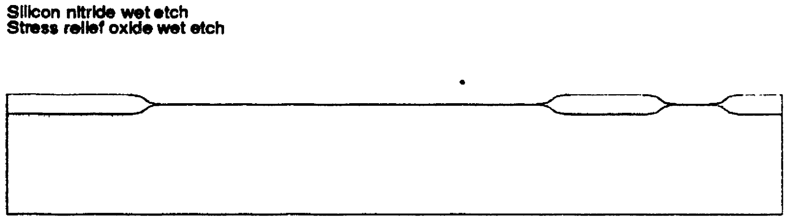


Figure B.7: Wet-strip of silicon nitride and stress relief oxide.

gate oxide (Figure B.10).

A 22 nm gate oxide is then grown (same conditions as the dummy gate) (Figure B.11) followed by 500 nm LPCVD polysilicon deposition using silane at 250 mT at 625°C for 148 minutes followed by a phosphorus doping using a $POCl_3$ source for 72 minutes and 15 minutes in dry oxygen, both at 925°C , and a phosphorus glass wet strip using 7:1 BOE for 70 seconds. These steps are very critical in terms of cleanliness and contamination-control. The polysilicon is then patterned and plasma etched using CCl_4 which provides a somewhat anisotropic etch. The cross section after these steps is shown in (Figure B.12).

The resist is plasma-ashed after the poly patterning/etching and an n+ ion implant is done

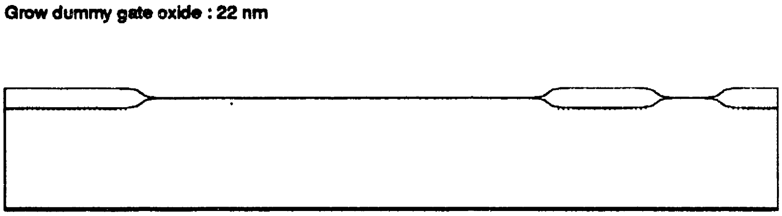


Figure B.8: Dummy gate oxide growth.

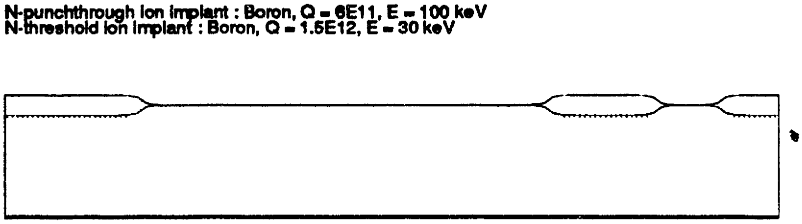


Figure B.9: Ion implant for punch-through and threshold voltage adjust.

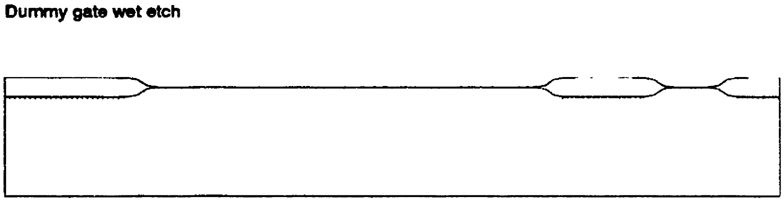


Figure B.10: Dummy gate oxide wet etch.

to create the source/drain regions (arsenic, dose = 7 x 10^{15}, energy = 90 keV) (Figure B.13). In addition, this dopes the gate even further, reducing its sheet resistance. Notice that the large active area in the figures is where the air-gap capacitor resides. Since no poly is patterned in this region, it automatically gets doped very heavy by the source/drain ion implant. This forms the bottom plate of the air-gap capacitor.

At this point, a reoxidation (dry oxygen at 900°C for 30 minutes) and junction drive (nitrogen/oxygen/nitrogen at 25/20/15 minutes at 950°C) are done to repair any oxide damage at the poly gate corners after plasma etching, and to drive in the S/D junctions (Figure B.14). The cross section in Figure B.14 represents NMOS device processing, and

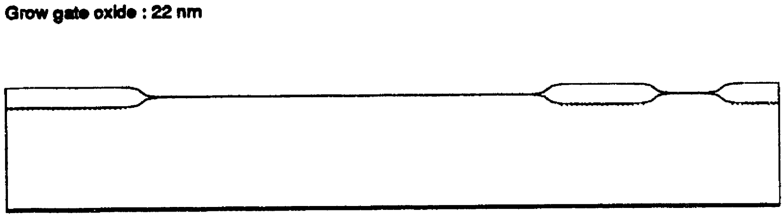


Figure B.11: Gate oxide growth.

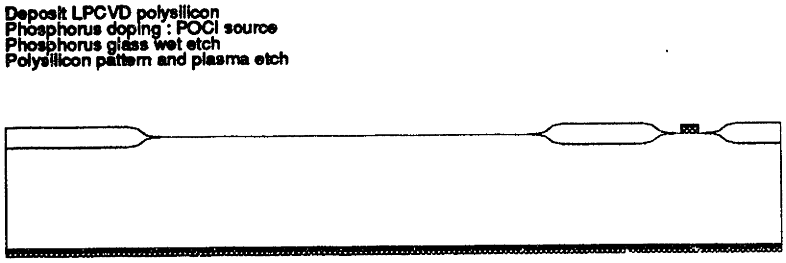


Figure B.12: LPCVD polysilicon deposition, phosphorus doping, patterning and etching.

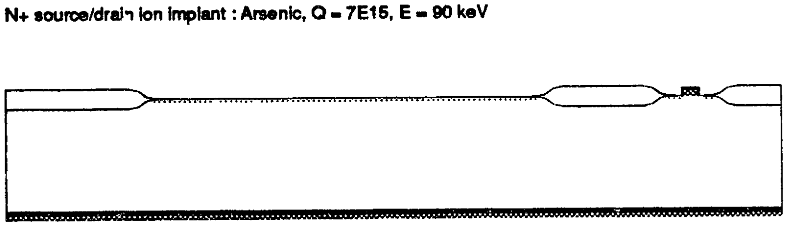


Figure B.13: Source/drain n+ ion implant.

has been taken directly from a CMOS process. Though the twin-well CMOS process uses an epi-layer on top of a heavily-doped substrate layer, the electrical characteristics of the NMOS transistors are determined more by the implants at the surface, and hence the difference in substrate doping from the p-type 15-20 Ω-cm wafers used in the NMOS/sensor process described here and the CMOS process is negligible and makes little difference. This is apparent in both SUPREM simulations and experimental measurements. Also, it is important to note that the cross section here could also have been achieved with the CMOS process if desired, enabling an easy extension from NMOS to CMOS.

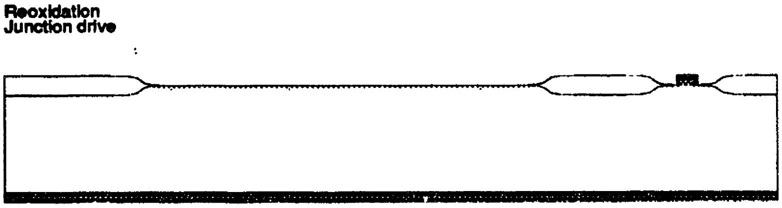


Figure B.14: Reoxidation and junction drive.

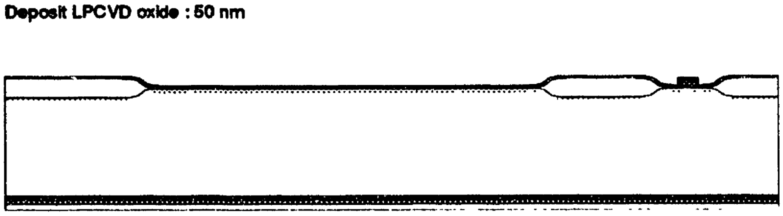


Figure B.15: LPCVD oxide deposition.

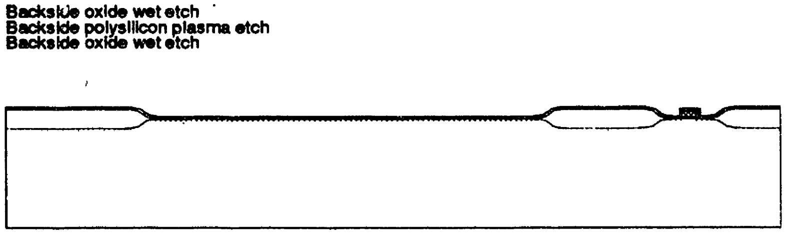


Figure B.16: Back-side layer removal.

B.1.2 Phase II : Device/Sensor Integration

After reoxidation and drive-in, a 50 nm LPCVD oxide is deposited at 400°C for 87 minutes (Figure B.15). This serves as an etch stop for a subsequent silicon nitride deposition. Without it, the SF_6 nitride etch could attack the underlying poly gate. A resist coat is applied to the front-side, and the oxide on the back-side is wet-stripped using 7:1 BOE for 40 seconds (Figure B.16). This is followed by a back-side polysilicon plasma etch in SF_6 to finally reveal the backside silicon. A quick wet oxide etch of 15 sec in 7:1 BOE may be used if there is still some oxide left (determined by sheeting). A back-side p+ ion implant is then performed to allow a good electrical contact to the substrate (Figure B.17). The

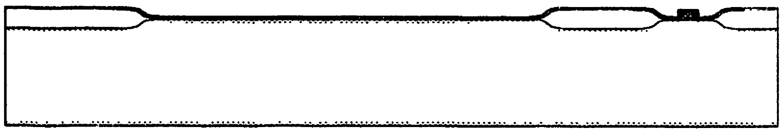

Backside p+ ion implant : BF2, Q = 7E15, E = 30 keV

Figure B.17: Back-side contact p+ ion implant.

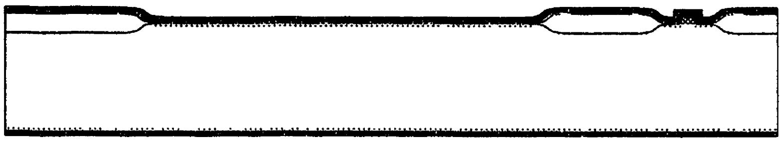

Deposit LPCVD silicon nitride : 150 nm

Figure B.18: LPCVD silicon nitride deposition.

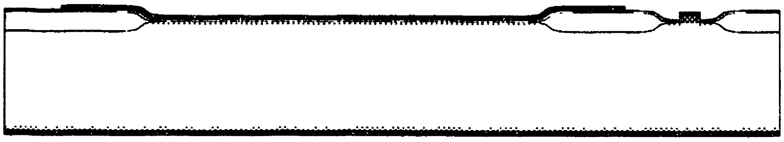

Pattern and plasma etch silicon nitride

Figure B.19: Silicon nitride patterning and etching.

implant available is the S/D implant for PMOS devices in the usual CMOS process (BF_2, dose = 7 x 10^{15}, energy = 30 keV). A sacrificial layer is not needed since the roughness caused by such a heavy, shallow implant will not diminish the mirror-like finish needed for later IR alignment. Damage to this surface due to this ion implantation is not critical, but care must be taken to avoid heavy damage which might affect the subsequent silicon nitride deposition and degrade the KOH-masking ability of this layer.

After back-side implant, a 150 nm LPCVD silicon nitride layer is deposited (same conditions as before) (Figure B.18), patterned, and etched in SF_6, similar to the steps used to form the active areas in the very beginning (Figure B.19). This layer also gets deposited

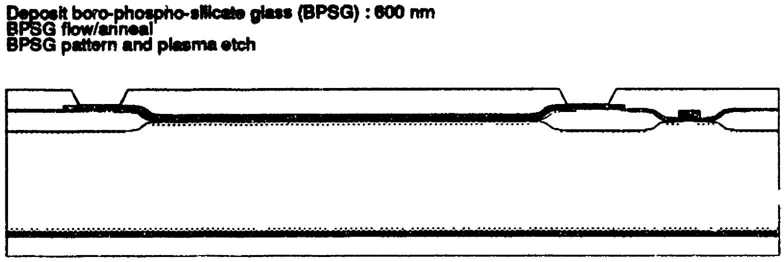


Figure B.20: Boro-phospho-silicate glass deposition, flow/anneal, patterning, and plasma etching.

on the back-side, and it will become important later. The resist is ashed and is followed by a 600 nm boro-phospho-silicate glass deposition which consists of 50 nm of undoped LTO followed by 550 nm of BPSG and finally 50 nm of undoped LTO, and occurs at 400°C for 143 minutes. This BPSG serves as the inter-level dielectric between poly and metal 1 (PMD) and also as the sacrificial layer that sets the gap distance in the air-gap capacitors. The BPSG is then flowed/annealed (at 925°C for 22 minutes in nitrogen followed by 15 minutes in dry oxygen) for conformal step smoothing, then patterned and etched using a mask which forms a moat around the region where the air-gap capacitor lies (Figure B.20). The etch is a careful plasma etch using CF_4 which is timed to stop on the silicon nitride. Though the etch proceeds through 150 nm of nitride in 30 seconds, this is slow enough to enable an etch which will not penetrate through the field oxide and eventually to the silicon substrate. Wet etching is a possibility, but poses other problems.

After resist ashing, 1000 nm LPCVD polysilicon (using the same conditions as the gate except the deposition time is twice as long) is deposited, doped using a $POCl_3$ source (same conditions as the gate poly), and the phosphorus glass wet-etched (Figure B.21).

A front-coat resist is applied and a back-side polysilicon plasma etch is done using SF_6 (similar to the back side gate poly removal step) (Figure B.22). The etch stops easily on the BPSG layer.

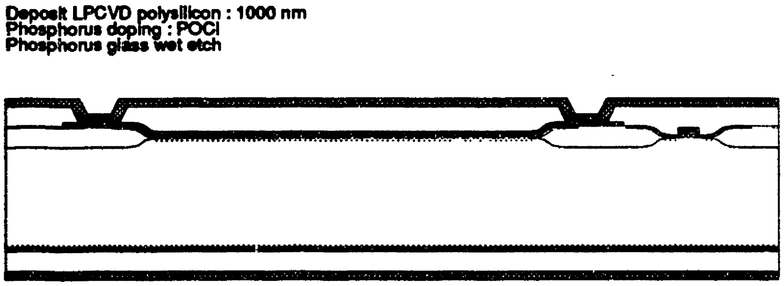


Figure B.21: LPCVD polysilicon diaphragm deposition, phosphorus doping, and glass wet-etch.

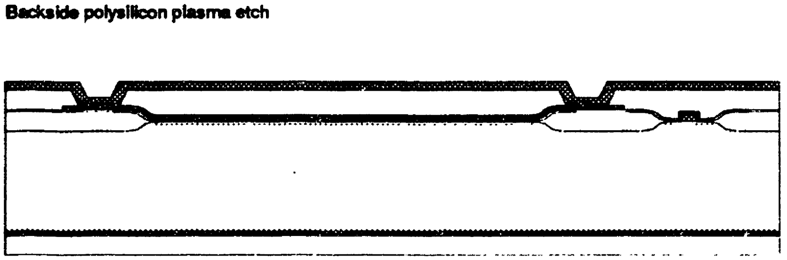


Figure B.22: Back-side polysilicon plasma etch.

This 1000 nm polysilicon layer serves as the top plate of the air-gap capacitor, and is patterned with a thicker coat of resist (1.7 μm rather than the normal 1.1 μm) due to the thicker poly level. Since this defines the edge of the diaphragm, the lithography on this level is relaxed. In addition, sloping sidewalls are desirable for step coverage of metal, and this is accomplished using an SF_6 etch which tends to undercut faster than CCl_4 (Figure B.23).

After etching and a resist ash, the process returns to normal back-end MOS process consisting of patterning/etching contact cuts into the BPSG using CH_4, then proceeding to an extensive pre-metal clean consisting of a 10 minute 5:1:1 sulfuric acid, hydrogen peroxide, and DI water (piranha) clean followed by a 1 minute dip in 50:1 DI/HF water solution. Aluminum-1% silicon is then sputter deposited to a thickness of 1.1 μm. The metal is patterned and etched in a combination of BCl_3, Cl_2, and $CHCl_3$. A plasma RF unloading chamber on the load-lock LAM etcher prevents further chlorine etching after the etch. A 5

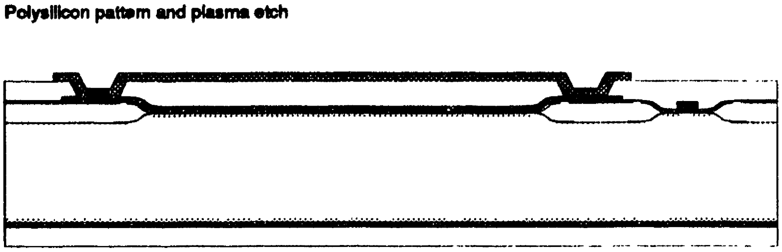


Figure B.23: Polysilicon diaphragm patterning and plasma etching.

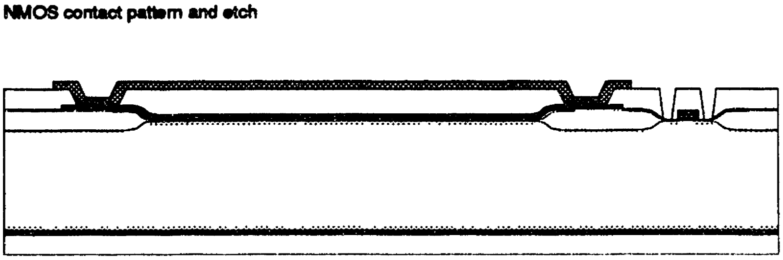


Figure B.24: NMOS contact pattern and plasma etch.

second wet PAN etch at 50°C is performed to remove any possible stray aluminum-silicon from the surface (Figure B.24). The resist is ashed and a metal sinter is performed at 400°C for 40 minutes. This completes the front-side processing and processing for all circuits/devices (Figure B.25).

B.1.3 Phase III : Air-Gap Capacitor Formation

Back-to-front Alignment

The wafers are then removed from the Integrated Circuits Laboratory and enter a different photolithography laboratory for back-side processing. A 1.6 μm front-side resist coat is applied, then a similar coat is applied to the back-side. A Karl Suss IR contact aligner is used in conjunction with a 5-inch, chrome 1X contact mask which has been especially designed

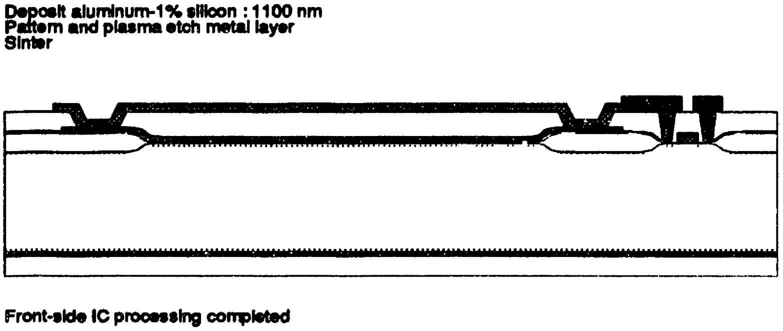


Figure B.25: Metal pattern, plasma etch, and sinter.

to align with alignment marks created by the 10X stepper on the front-side (Figure B.26). Since the dies are stepped 1 cm apart, any feature across the wafer could be used as an alignment mark, but special poly-gate crosses over active areas are used. The back-side mask uses alignment windows to match up with any set of alignment marks on the wafer that are 5 cm apart, but specifically those that are located so that the exposure is centered on the wafer.

The back-side mask consists of 16 distinct areas, each representing a 1 cm x 1 cm die. They are separated by grooves which serve as scribe lines for die separation later. Within each die are 10 circles. 8 of them represent windows that lie underneath the 4 air-gap capacitor circuits (sense/reference pair per circuit) and the other two represent test air-gap capacitors in the drop-in pattern. The circles are 724 μm in diameter, and are formed out of 20 boxes appropriately rotated to form the circles.

After photolithography, the back-side of the wafers are plasma etched in CH_4, removing the BPSG and the nitride in one etch step (Figure B.27).

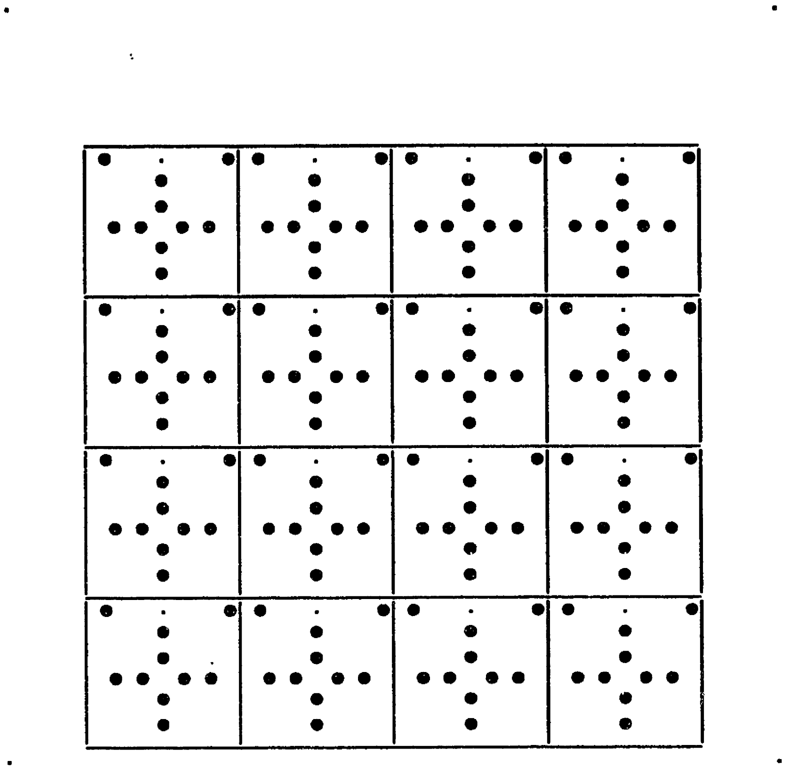
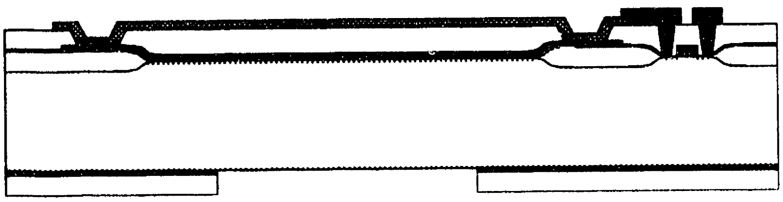


Figure B.26: 1X chrome back-side contact mask pattern. Each of the 16 squares is 1 cm wide, circles are 724 μm in diameter, and groove lines are 100 μm wide.

One-sided KOH Etching

The wafers are individually placed in a custom-designed, one-sided etching apparatus (Figure B.28) and immersed in a 20 % by weight (in pellet form) KOH solution at 80°C for 6 hours followed by 60°C for 2 hours using a custom-designed etching system which maintains constant water level, temperature, and stirring (Figure B.29) [48]. The one-sided etching apparatus is critical since the front-side circuits would be destroyed without it. Resist would dissolve rapidly, and epoxies would delaminate. There is no known commercial photolithographic material that can survive a 80°C KOH etch for 8 hours or more.



Initiate back-side processing sequence :
Back-side pattern using IR aligner
Back-side oxide/nitride plasma etch

Figure B.27: Back-side pattern and plasma etch for KOH mask.

During the anisotropic etch, the back-side BPSG is stripped off, revealing the KOH masking layer which is the silicon nitride. The BPSG is left on to protect the nitride layer from wafer handling and scratches which degrade the reliability of the mask. It is possible to remove this layer using a wet etch when the BPSG is etched to form the diaphragm anchor (thus removing a critical, timed plasma etch step), but a wet BOE etch might be non-uniform on BPSG (as is sometimes the case) so the trench will be erratic and enlarged due to the wet-etch isotropy. This is due to non-uniformities in the BPSG material which cause etch rates to differ locally, causing uneven underetching. Also, this wet etch leaves the back-side nitride uncovered, and scratch protection is lost. The scratch protection of the BPSG on the back-side is more critical than the timed plasma etch of the BPSG anchor trench, so that plasma-etching is favored over wet-etching for the diaphragm anchor.

The KOH etch undercuts the nitride mask by 18 μm on both sides, thus widening the hole by almost 36 μm. This undercut is repeatable, and is designed into the back-side mask. Given the thickness of the wafer to be nominally 500 μm, with a backside mask of 724 μm, this yields a front-side opening (in μm) of

$$724 + 36 - (500)\sqrt{2} = 53$$

since the KOH etch preferentially etches along the (100) planes and not the (111) planes, and this angle is 54.7 degrees. A thicker wafer will yield a smaller front-side window and hence a larger capacitance because the front-side hole will be smaller, increasing the bottom

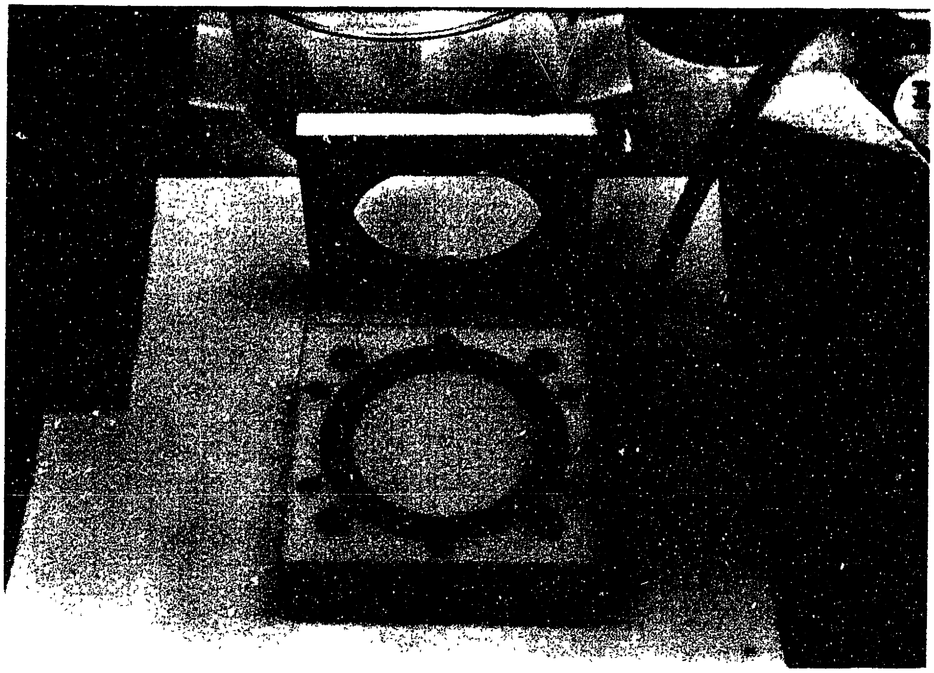


Figure B.28: One-sided KOH etching apparatus.

plate area. Process variations and thickness variations were evaluated to allow a design which could tolerate them to an acceptable level. Circular patterns were used rather than squares since this insured that if the alignment (which was to the front-side) was off angle to the flat (which it can be by sometimes a degree or more), then the undercutting would always produce a square regardless of orientation. This is not true of square masks, and has been experimentally verified that uneven undercutting can occur which can grossly enlarge the hole, destroying circuits on the front-side by engulfing them.

The 60°C 2 hour etch after the 80°C 8 hour etch etch provides a gentler etch stop on the silicon nitride layer on the front-side. At this point, the wafer is checked by pulling the etch apparatus out of the etch and optically inspecting the etched hole with a portable, high magnification plastic microscope. It is clear when the etch has finished when the stopped surface is smooth and transparent – revealing the nitride, BPSG, and poly layers. When

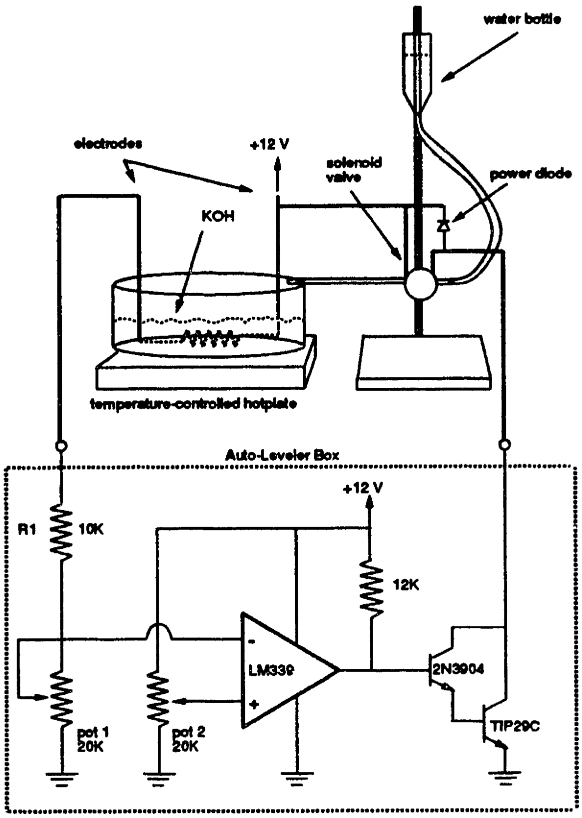


Figure B.29: KOH etching system block diagram with auto-level water system.

this condition is reached, the apparatus is rinsed thoroughly in DI water, the wafer removed and rinsed extensively in DI water to prevent any KOH from harming the front-side layers, and prepped for another one-sided etch. The cross section appears in Figure B.30.

One-sided HF Etching

The wafer is inspected to see the integrity of the etch as well as the formation of the square holes that penetrate the entire substrate. The wafer is then placed in a similar one-sided etching apparatus designed to etch in concentrated HF (Figure B.31). 10 ml of concentrated HF is poured into the cavity which uses the back-side of the wafer as its bottom. Mechanical

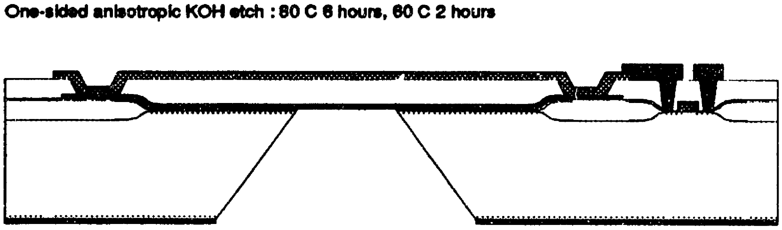


Figure B.30: Back-side KOH etching.

pressure, nitrogen flow, and DI water flow on the front-side prevent the HF from touching the front-side. The HF enters the KOH-etched holes and attacks the silicon nitride. The nitride is not stoichiometric and etches away in 10 minutes, revealing the BPSG. This layer is rapidly etched laterally so that in 10 minutes, it is consumed to the edge of the diaphragm where the etch stops due to the polysilicon. The front-side nitride layer is also etched, but much more slowly than the BPSG, and hence provides some protection near the diaphragm anchors. The BPSG etch rate has been experimentally determined by watching the etch front proceed under the polysilicon diaphragm (which is semi-transparent) for different timed HF etches. The HF etch also removes the back-side nitride that was used as the KOH etch mask, and allows electrical contact to the substrate (Figure B.32).

After etching, the apparatus is thoroughly rinsed in DI water, the wafer removed and rinsed in DI water, blown dry using nitrogen, and placed in a methanol bath for 30 minutes. This is believed to remove any excess water that may be in the cavity after rinsing by evaporation. This is extremely important since during the wet HF etching process, the two plates of the air-gap capacitor might have a tendency to stick together due to surface tension. Several alternatives have been sought, which include freeze-drying, HF vapor etching, and hot-solvent cleans, all which tend to replace the water with another agent which can readily be removed, usually by entering a gaseous phase quickly before sticking can occur. Unfortunately, these methods are rather cumbersome or dangerous, so were not employed.

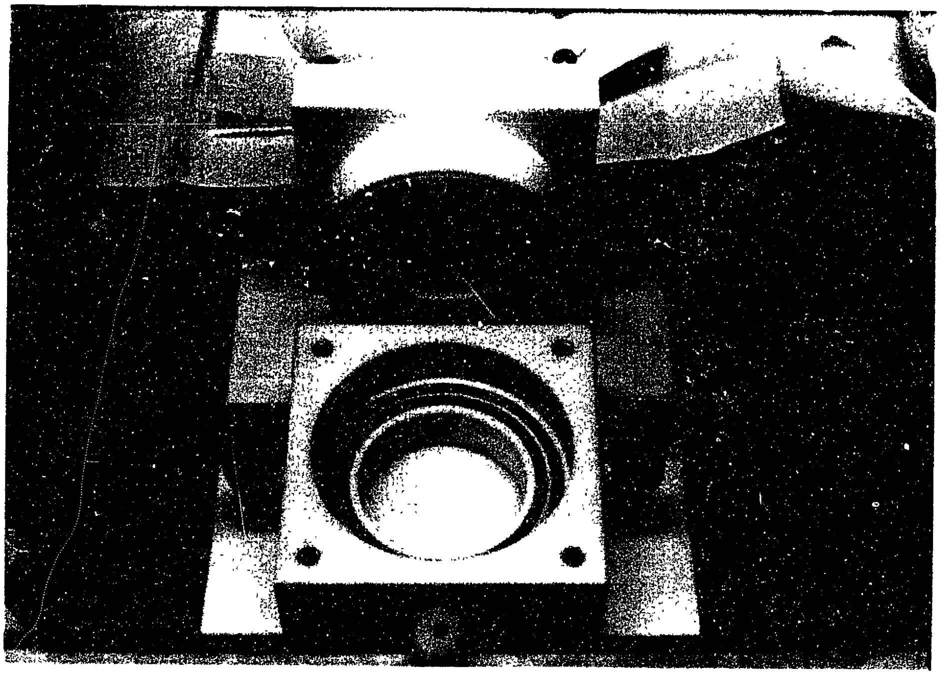


Figure B.31: One-sided HF etching apparatus.

After methanol rinsing, the wafers are blown dry using nitrogen and dehydrated at 200°C for 24 hours. The wafer is diced along KOH-etched groove lines manually, and the dies are packaged in 65-pin ceramic PGA packages (Kyocera KD-84343-A) with specially drilled holes through their centers. Silver epoxy is used to attach the die to the package. The hole in the PGA is specially drilled using diamond paste and stainless steel tubing at a slow rate, thus preventing fracturing of the ceramic substrate. The hole is centrally drilled to reveal the 4 center KOH-etched holes which allow pressure to reach the sense air-gap capacitors. The other 4 holes are sealed by the epoxy and blocked by the ceramic package, and hence seal the reference air-gap capacitor to external stimuli. The 1 μm thick polysilicon diaphragms are semi-transparent (goldish tint) and can be seen through the back of the PGA package. The packaging is completed by epoxying a plastic tygon tube to the back of the ceramic package. This withstands a pressure up to 65 PSI before leaking.

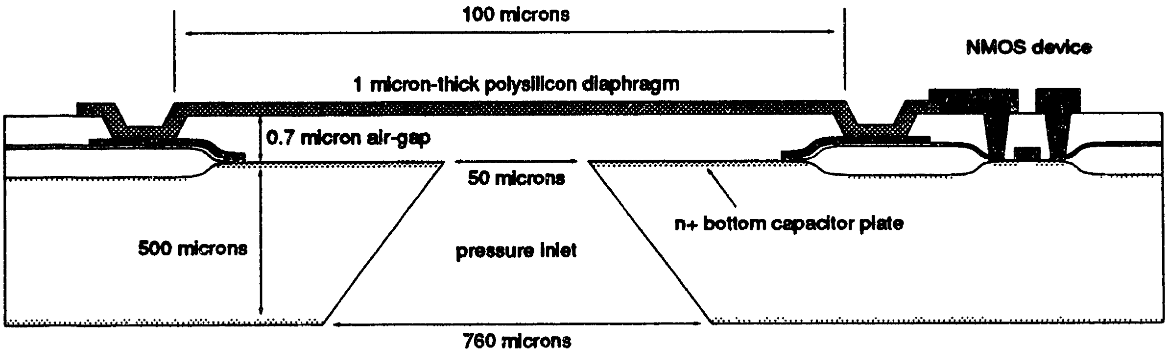


Figure B.32: Final cross section after one-sided HF etching to release the diaphragm and form the air-gap.

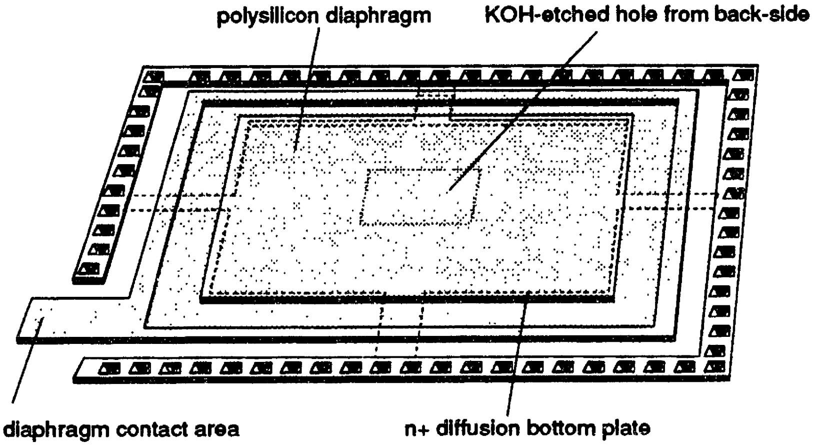


Figure B.33: Perspective view of the polysilicon air-gap capacitor.

Figure B.33 shows a perspective view of the air-gap capacitor, and Figure B.34 shows the same figure sliced through its center to show the underlying structure. Notice that the contact to the n+ bottom plate is made via n+ diffusion channels contacted by metal surrounding the diaphragm. The HF etch mentioned earlier must be a timed-etch because the HF can proceed through these channels and etch the metal. However, since the channels are fairly long (20 μm), it requires a long over-etch to reach the metal, and hence a timed etch is necessary but not critical.

Contact to the polysilicon is made directly via metal on top of the tab protruding from the

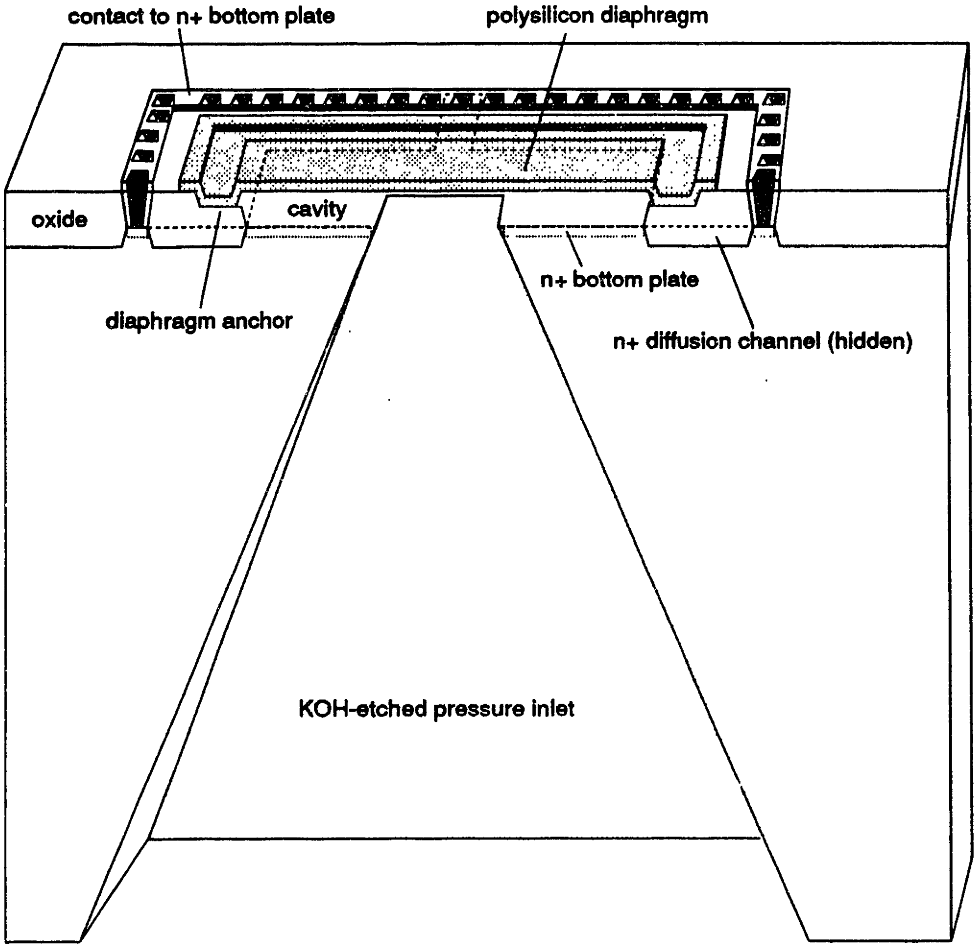


Figure B.34: 3-dimensional cross section of the air-gap capacitor.

square structure. This method of contact is much better than contacting via poly anchored to n+ diffusions (as was done in [14] and other polysilicon micromechanical processes) because there exist potentially large leakage currents from these junctions, high contact resistance, and high parasitic capacitance. The diaphragm in this design is anchored firmly to field oxide, providing good isolation from the substrate while offering sufficient adhesion. As was mentioned before, the sloping sidewalls of the polysilicon diaphragm etch allow good metal coverage over this 1 μm step.

A comprehensive list of equipment and facilities used in the sensor/NMOS process can be found in the 1991 annual report of the Microsystems Technology Laboratories, May 1991 [68].

Appendix C

SUPREM Simulations

```
*******************************************************************************

                              SUPREM-III
           Stanford Electronics Laboratories  Version 1B  Rev. 8507
              DEC/MIT  Version 2.04  SEG/CAD Release: 11-SEP-87
            Contact: Duane Boning   boning@caf.mit.edu   253-0450


                         Mon Nov 26 22:12:24 1990

*******************************************************************************

     Simulation commands input from nmos+sensor.in

   1... title Cross section through NMOS channel of SENSOR process for
   2... title 1 micron POCl-doped Polysilicon Diaphragm

   3... initialize silicon <100> concentration=1e15 Boron
    ... + thickness=3.0 dx=0.005 xdx=0.02 spaces=150

   4... comment * grow SRO [430 A]
   5... diffusion temp=800, time=10, nitrogen
   6... diffusion temp=950, time=25, nitrogen
   7... diffusion temp=950, time=115, dryo2
   8... diffusion temp=950, time=30, nitrogen
   9... diffusion temp=800, time=60, nitrogen
```

```
10... print layer

11... comment * deposit 1500A nitride + simulate thermal cycling
12... deposit nitride, thickness=0.1500, spaces=15
13... diffusion temp=800, time=86, nitrogen
14... diffusion temp=700, time=29, nitrogen

15... comment * pattern nitride, then ion implant p-field
16... implant dose=1e13, energy=70, Boron
17... print layers

18... comment * grow field oxide
19... diffusion temp=800, time=10, nitrogen
20... diffusion temp=950, time=25, nitrogen
21... diffusion temp=950, time=30, dryo2
22... diffusion temp=950, time=160, weto2
23... diffusion temp=950, time=30, dryo2
24... diffusion temp=950, time=30, nitrogen
25... diffusion temp=800, time=70, nitrogen
26... print layer

27... comment * Etch to silicon surface
28... etch oxide all
29... etch  nitride all
30... etch  oxide all
31... print  layers

32... comment * dummy gate oxidation
33... diffusion temp=800, time=10, nitrogen
34... diffusion temp=950, time=15, nitrogen
35... diffusion temp=950, time=35, dryo2
36... diffusion temp=950, time=30, nitrogen
37... diffusion temp=800, time=60, nitrogen
38... print  layer

39... comment * implant of punch-thru and channel for VT
40... implant  dose=6e11, energy=100, Boron
41... implant  dose=1.5e12, energy=30, Boron
42... print layers

43... comment * strip dummy gate oxide
44... etch oxide all

45... comment * gate oxidation
46... diffusion temp=800, time=10, nitrogen
47... diffusion temp=950, time=15, nitrogen
48... diffusion temp=950, time=35, dryo2
49... diffusion temp=950, time=30, nitrogen
50... diffusion temp=800, time=60, nitrogen
```

```
51... polysilicon semiconductor

52... comment * deposit poly gate + simulate thermal cycling
53... deposit polysilicon, thickness=0.5, temp=625
54... diffusion temp=625, time=148, nitrogen

55... comment * POCl dep on poly.
56... diffusion temp=800, time=10, nitrogen
57... diffusion temp=925, time=22, nitrogen
58... diffusion temp=925, time=72, dryo2 solidsol phos
59... diffusion temp=925, time=15, dryo2
60... diffusion temp=925, time=10, nitrogen
61... diffusion temp=800, time=60, nitrogen

62... comment * strip P-glass off of poly [1200 A]
63... etch oxide all

64... comment * S/D implant
65... implant arsenic dose=7e15 energy=90

66... comment * reoxidation
67... diffusion temp=800, time=10, nitrogen
68... diffusion temp=900, time=20, nitrogen
69... diffusion temp=900, time=30, dryo2
70... diffusion temp=900, time=30, nitrogen
71... diffusion temp=800, time=50, nitrogen

72... comment * junction drive
73... diffusion temp=800, time=10, nitrogen
74... diffusion temp=950, time=25, nitrogen
75... diffusion temp=950, time=20, dryo2
76... diffusion temp=950, time=15, nitrogen
77... diffusion temp=800, time=60, nitrogen
78... print layers

79... comment * 565 A LTO deposition + thermal cycling
80... deposit oxide, thickness=0.0565
81... diffusion temp=400, time=87, nitrogen

82... comment * deposit 1500A nitride etch stop + simulate thermal cycling
83... deposit nitride, thickness=0.1500, spaces=15
84... diffusion temp=800, time=86, nitrogen
85... diffusion temp=700, time=29, nitrogen

86... comment * deposit 1000A LTO + 5000A BPSG + simulate thermal cycling
87... deposit oxide, thickness=0.55
88... diffusion temp=350, time=17, nitrogen
89... diffusion temp=400, time=143, nitrogen
```

```
 90... comment * BPSG reflow
 91... diffusion temp=925, time=22, nitrogen
 92... diffusion temp=925, time=15, dryo2
 93... diffusion temp=800, time=50, nitrogen


 94... comment * 2nd poly for 1 micron diaphragm + thermal cycling
 95... deposit polysilicon, thickness=1.0, temp=625
 96... diffusion temp=625, time=86.75, nitrogen

 97... comment * POCl dep on poly.
 98... diffusion temp=800, time=10, nitrogen
 99... diffusion temp=925, time=22, nitrogen
100... diffusion temp=925, time=72, dryo2 solidsol phos
101... diffusion temp=925, time=15, dryo2
102... diffusion temp=925, time=10, nitrogen
103... diffusion temp=800, time=60, nitrogen

104... comment * strip P-glass off of poly [1200 A]
105... etch oxide all

106... comment * deposit A/Si
107... deposit aluminum thickness=1.0

108... comment * sinter thermal cycling
109... diffusion temp=400, time=40, nitrogen

110... print layers

111... Save structure file=nmos+sensor.sav

112... stop

Cross section through NMOS channel of SENSOR process for 1 micron
POCl-doped Polysilicon Diaphragm

* grow SRO [430 A]
1

layer    material type      thickness   dx     dxmin top  bottom  orientation
 no.                        (microns)   (microns)    node  node   or grain size
  2    OXIDE                   0.0461 0.0100 0.0010  348   352
  1    SILICON                 2.9797 0.0050 0.0010  353   500       <100>

                          Integrated Dopant
layer             Net                         Total
 no.       active       chemical        active       chemical
  2    -6.0161E+09  -6.0161E+09    6.0161E+09   6.0161E+09
```

```
  1    -2.9203E+11  -2.9203E+11   2.9203E+11   2.9203E+11
 sum   -2.9805E+11  -2.9805E+11   2.9805E+11   2.9805E+11

                          Integrated Dopant
layer            BORON
 no.       active      chemical
  2      6.0161E+09   6.0161E+09
  1      2.9203E+11   2.9203E+11
 sum     2.9805E+11   2.9805E+11

                Junction Depths and Integrated Dopant
               Concentrations for Each Diffused Region
layer  region  type  junction depth      net          total
 no.     no.            (microns)     active Qd    chemical Qd
  2       1     p        0.0000       6.0161E+09    6.0161E+09
  1       1     p        0.0000       2.9203E+11    2.9203E+11

* deposit 1500A nitride + simulate thermal cycling
Error number  45 detected in line number  14
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

* pattern nitride, then ion implant p-field
1

layer    material type      thickness   dx    dxmin top  bottom  orientation
 no.                        (microns)   (microns)   node  node  or grain size
  3   NITRIDE                  0.1500 0.0100 0.0010  332   347
  2   OXIDE                    0.0461 0.0100 0.0010  348   352
  1   SILICON                  2.9797 0.0050 0.0010  353   500      <100>

                          Integrated Dopant
layer            Net                         Total
 no.      active       chemical       active       chemical
  3    -2.6737E+12  -2.6737E+12   2.6737E+12   2.6737E+12
  2    -2.2066E+12  -2.2066E+12   2.2066E+12   2.2066E+12
  1    -5.4178E+12  -5.4178E+12   5.4178E+12   5.4178E+12
 sum   -1.0298E+13  -1.0298E+13   1.0298E+13   1.0298E+13

                          Integrated Dopant
layer            BORON
 no.       active      chemical
  3      2.6737E+12   2.6737E+12
  2      2.2066E+12   2.2066E+12
  1      5.4178E+12   5.4178E+12
 sum     1.0298E+13   1.0298E+13

                Junction Depths and Integrated Dopant
```

```
           Concentrations for Each Diffused Region
 layer  region  type  junction depth     net          total
  no.     no.           (microns)      active Qd     chemical Qd
   3       1     p       0.0000       2.6737E+12    2.6737E+12
   2       1     p       0.0000       2.2066E+12    2.2066E+12
   1       1     p       0.0000       5.4178E+12    5.4178E+12

 * grow field oxide
1

 layer    material type      thickness   dx    dxmin top  bottom  orientation
  no.                        (microns)  (microns)   node  node  or grain size
   4    OXIDE                   0.0081 0.0100 0.0010  330   331
   3    NITRIDE                 0.1451 0.0100 0.0010  332   347
   2    OXIDE                   0.0461 0.0100 0.0010  348   352
   1    SILICON                 2.9797 0.0050 0.0010  353   500       <100>

                          Integrated Dopant
 layer            Net                        Total
  no.      active       chemical       active       chemical
   4    -1.4766E+09  -1.4766E+09   1.4766E+09   1.4766E+09
   3    -2.6085E+12  -2.6085E+12   2.6085E+12   2.6085E+12
   2    -2.5049E+12  -2.5049E+12   2.5049E+12   2.5049E+12
   1    -5.1777E+12  -5.1777E+12   5.1777E+12   5.1777E+12
  sum   -1.0292E+13  -1.0292E+13   1.0292E+13   1.0292E+13

                          Integrated Dopant
 layer           BORON
  no.      active       chemical
   4     1.4766E+09   1.4766E+09
   3     2.6085E+12   2.6085E+12
   2     2.5049E+12   2.5049E+12
   1     5.1777E+12   5.1777E+12
  sum    1.0292E+13   1.0292E+13

            Junction Depths and Integrated Dopant
           Concentrations for Each Diffused Region
 layer  region  type  junction depth     net          total
  no.     no.           (microns)      active Qd     chemical Qd
   4       1     p       0.0000       1.4766E+09    1.4766E+09
   3       1     p       0.0000       2.6085E+12    2.6085E+12
   2       1     p       0.0000       2.5049E+12    2.5049E+12
   1       1     p       0.0000       5.1777E+12    5.1777E+12

 * Etch to silicon surface
1

 layer    material type      thickness   dx    dxmin top  bottom  orientation
  no.                        (microns)  (microns)   node  node  or grain size
```

```
   1    SILICON                   2.9797 0.0050 0.0010  353   500      <100>

                             Integrated Dopant
 layer              Net                          Total
  no.      active      chemical       active       chemical
   1    -5.1777E+12  -5.1777E+12   5.1777E+12   5.1777E+12
  sum   -5.1777E+12  -5.1777E+12   5.1777E+12   5.1777E+12

                             Integrated Dopant
 layer            BORON
  no.      active      chemical
   1     5.1777E+12   5.1777E+12
  sum    5.1777E+12   5.1777E+12

                  Junction Depths and Integrated Dopant
                 Concentrations for Each Diffused Region
 layer  region  type  junction depth     net          total
  no.    no.            (microns)     active Qd    chemical Qd
   1      1      p        0.0000      5.1777E+12    5.1777E+12

 * dummy gate oxidation
1

 layer    material type      thickness   dx    dxmin top  bottom  orientation
  no.                        (microns)   (microns)   node  node  or grain size
   2    OXIDE                     0.0215 0.0100 0.0010  351   354
   1    SILICON                   2.9703 0.0050 0.0010  355   500      <100>

                             Integrated Dopant
 layer              Net                          Total
  no.      active      chemical       active       chemical
   2    -6.6827E+11  -6.6827E+11   6.6827E+11   6.6827E+11
   1    -4.1344E+12  -4.1344E+12   4.1344E+12   4.1344E+12
  sum   -4.8027E+12  -4.8027E+12   4.8027E+12   4.8027E+12

                             Integrated Dopant
 layer            BORON
  no.      active      chemical
   2     6.6827E+11   6.6827E+11
   1     4.1344E+12   4.1344E+12
  sum    4.8027E+12   4.8027E+12

                  Junction Depths and Integrated Dopant
                 Concentrations for Each Diffused Region
 layer  region  type  junction depth     net          total
  no.    no.            (microns)     active Qd    chemical Qd
   2      1      p        0.0000      6.6827E+11    6.6827E+11
   1      1      p        0.0000      4.1344E+12    4.1344E+12
```

```
 * implant of punch-thru and channel for VT
1

 layer    material type      thickness   dx     dxmin top  bottom  orientation
  no.                       (microns)   (microns)   node  node   or grain size
   2    OXIDE                  0.0215 0.0100 0.0010  351   354
   1    SILICON                2.9703 0.0050 0.0010  355   500      <100>

                         Integrated Dopant
 layer             Net                        Total
  no.      active      chemical       active       chemical
   2    -6.8912E+11  -6.8912E+11   6.8912E+11   6.8912E+11
   1    -6.2136E+12  -6.2136E+12   6.2136E+12   6.2136E+12
  sum   -6.9027E+12  -6.9027E+12   6.9027E+12   6.9027E+12

                         Integrated Dopant
 layer            BORON
  no.      active      chemical
   2     6.8912E+11   6.8912E+11
   1     6.2136E+12   6.2136E+12
  sum    6.9027E+12   6.9027E+12

              Junction Depths and Integrated Dopant
             Concentrations for Each Diffused Region
 layer  region  type  junction depth     net          total
  no.     no.            (microns)      active Qd    chemical Qd
   2       1      p       0.0000        6.8912E+11    6.8912E+11
   1       1      p       0.0000        6.2136E+12    6.2136E+12

 * strip dummy gate oxide

 * gate oxidation

 * deposit poly gate + simulate thermal cycling
 Error number  45 detected in line number  54
 The temperature was specified with a value less than 800 degrees C.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 * POCl dep on poly.

 * strip P-glass off of poly [1200 A]

 * S/D implant

 * reoxidation

 * junction drive
1
```

```
layer    material type       thickness   dx     dxmin top  bottom  orientation
 no.                         (microns)   (microns)    node  node  or grain size
  4    OXIDE                    0.0635 0.0100 0.0010  302   306
  3    POLYSILICON              0.4454 0.0100 0.0010  307   352       1.2840
  2    OXIDE                    0.0215 0.0100 0.0010  353   355
  1    SILICON                  2.9608 0.0050 0.0010  356   500       <100>

                          Integrated Dopant
layer             Net                        Total
 no.        active      chemical      active      chemical
  4       1.6288E+14   1.6288E+14   1.6288E+14   1.6288E+14
  3       4.5846E+15   1.0348E+16   4.5846E+15   1.0348E+16
  2      -8.4237E+11  -8.4237E+11   8.7112E+11   8.7112E+11
  1      -5.0823E+12  -5.0823E+12   5.0830E+12   5.0830E+12
 sum      4.7416E+15   1.0505E+16   4.7535E+15   1.0517E+16

                          Integrated Dopant
layer        PHOSPHORUS                    ARSENIC
 no.        active      chemical      active      chemical
  4       2.1696E+13   2.1696E+13   1.4118E+14   1.4118E+14
  3       3.3575E+15   3.4630E+15   1.2271E+15   6.8849E+15
  2       1.4375E+10   1.4375E+10   3.8288E-15   3.8288E-15
  1       3.3580E+08   3.3580E+08   7.9959E-26   7.9959E-26
 sum      3.3792E+15   3.4847E+15   1.3683E+15   7.0261E+15

                          Integrated Dopant
layer          BORON
 no.        active      chemical
  4       3.2343E+08   3.2343E+08
  3       2.5067E+09   2.5067E+09
  2       8.5675E+11   8.5675E+11
  1       5.0827E+12   5.0827E+12
 sum      5.9422E+12   5.9422E+12

             Junction Depths and Integrated Dopant
            Concentrations for Each Diffused Region
layer   region  type  junction depth      net          total
 no.     no.            (microns)      active Qd    chemical Qd
  4       1      n        0.0000      1.6288E+14    1.6288E+14
  3       1      n        0.0000      4.5846E+15    1.0348E+16
  2       2      n        0.0000      1.8646E+10    1.8646E+10
  2       1      p        0.0072      7.5277E+11    7.5277E+11
  1       1      p        0.0000      5.0830E+12    5.0830E+12

* 565 A LTO deposition + thermal cycling
Error number  45 detected in line number  81
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
```

```
below this temperature.

* deposit 1500A nitride etch stop + simulate thermal cycling
Error number  45 detected in line number  85
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

* deposit 1000A LTO + 5000A BPSG + simulate thermal cycling
Error number  45 detected in line number  88
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
below this temperature.
Error number  45 detected in line number  89
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

* BPSG reflow

* 2nd poly for 1 micron diaphragm + thermal cycling
Error number  45 detected in line number  96
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

* POCl dep on poly.

* strip P-glass off of poly [1200 A]

* deposit A/Si

* sinter thermal cycling
Error number  45 detected in line number 109
The temperature was specified with a value less than 800 degrees C.
The default diffusion and oxidation coefficients are not reliable
below this temperature.
1

 layer    material type      thickness   dx    dxmin top  bottom  orientation
  no.                        (microns)   (microns)   node  node  or grain size
   8    ALUMINUM                1.0000 0.0100 0.0010   22   122
   7    POLYSILICON             0.9785 0.0100 0.0010  123   221       1.2235
   6    OXIDE                   0.5500 0.0100 0.0010  222   277
   5    NITRIDE                 0.1500 0.0100 0.0010  278   293
   4    OXIDE                   0.1200 0.0100 0.0010  294   306
   3    POLYSILICON             0.4454 0.0100 0.0010  307   352       1.5630
   2    OXIDE                   0.0215 0.0100 0.0010  353   355
   1    SILICON                 2.9608 0.0050 0.0010  356   500       <100>
```

```
                          Integrated Dopant
layer            Net                           Total
 no.       active      chemical      active      chemical
  8      9.1586E+12   9.1586E+12   9.1586E+12   9.1586E+12
  7      1.5003E+15   4.3573E+15   1.5003E+15   4.3573E+15
  6      1.3729E+09   1.3729E+09   1.3729E+09   1.3729E+09
  5      5.2290E+04   5.2290E+04   5.2290E+04   5.2290E+04
  4      1.6239E+14   1.6239E+14   1.6239E+14   1.6239E+14
  3      2.0392E+15   1.0349E+16   2.0393E+15   1.0349E+16
  2     -9.1459E+11  -9.1459E+11   9.3590E+11   9.3590E+11
  1     -5.0117E+12  -5.0117E+12   5.0136E+12   5.0136E+12
 sum     3.7052E+15   1.4871E+16   3.7170E+15   1.4883E+16

                          Integrated Dopant
layer         PHOSPHORUS                     ARSENIC
 no.       active      chemical      active      chemical
  8      9.1586E+12   9.1586E+12   0.0000E+00   0.0000E+00
  7      1.5003E+15   4.3573E+15   0.0000E+00   0.0000E+00
  6      1.3729E+09   1.3729E+09   0.0000E+00   0.0000E+00
  5      5.2290E+04   5.2290E+04   5.6324E-14   5.6324E-14
  4      2.1322E+13   2.1322E+13   1.4107E+14   1.4107E+14
  3      8.2330E+14   3.4634E+15   1.2159E+15   6.8851E+15
  2      1.0658E+10   1.0658E+10   7.4743E-10   7.4743E-10
  1      9.5589E+08   9.5589E+08   3.6868E-20   3.6868E-20
 sum     2.3541E+15   7.8512E+15   1.3570E+15   7.0261E+15

                          Integrated Dopant
layer           BORON
 no.       active      chemical
  8      0.0000E+00   0.0000E+00
  7      0.0000E+00   0.0000E+00
  6      0.0000E+00   0.0000E+00
  5      5.3342E-09   5.3342E-09
  4      5.0815E+08   5.0815E+08
  3      3.9406E+09   3.9406E+09
  2      9.2524E+11   9.2524E+11
  1      5.0126E+12   5.0126E+12
 sum     5.9423E+12   5.9423E+12

                Junction Depths and Integrated Dopant
               Concentrations for Each Diffused Region
layer  region  type  junction depth     net           total
 no.    no.            (microns)     active Qd     chemical Qd
  8      1      n       0.0000       9.1586E+12    9.1586E+12
  7      1      n       0.0000       1.5003E+15    4.3573E+15
  6      1      n       0.0000       1.3729E+09    1.3729E+09
  5      1      n       0.0000       5.2290E+04    5.2290E+04
  4      1      n       0.0000       1.6239E+14    1.6239E+14
```

```
   3       1      n      0.0000      2.0393E+15    1.0349E+16
   2       2      n      0.0000      5.4070E+09    5.4070E+09
   2       1      p      0.0072      8.2327E+11    8.2327E+11
   1       2      n      0.0000      7.7429E+07    7.7429E+07
   1       1      p      0.0020      5.0060E+12    5.0060E+12


----------------------


   NMOS Threshold of section: nmos+sensor.sav
1
 Threshold Voltage Calculation.

   Device Temperature:    27. degrees C.
   Fixed Oxide Charge Density:   1.0000E+10 per unit area
   Bulk Contact Concentration:   1.0000E+15 per cm-3, p-type
   Oxide Capacitance:   1.6049E-07 F/cm


   Vsub         Vth         Vpnch        Xdpl
 --------    --------    --------    --------
    0.000       1.101       1.064       0.098
    0.500       1.434       1.392       0.116
    1.000       1.707       1.662       0.143
    1.500       1.943       1.895       0.153
    2.000       2.155       2.105       0.173
    2.500       2.349       2.297       0.183
    3.000       2.528       2.474       0.204
    3.500       2.693       2.638       0.215
    4.000       2.849       2.792       0.226
    4.500       2.995       2.938       0.237
    5.000       3.134       3.075       0.249
```

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He received the Ph.D. degree in electrical engineering and computer science in 1992 on the subject of integrated capacitive sensors, where he worked on surface/bulk micromachining for microstructures, process integration with MOS processes, and on the development of a highly precise capacitance detection system for use in capacitive sensors. He is continuing work in the area of silicon micromachining integrated with circuits at Motorola in Phoenix, Arizona.

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