A Zero-Voltage Switching Technique for High Frequency Buck Converter ICs

by

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Abstract

This thesis explores a zero-voltage switching (ZVS) method that can be used to decrease the frequency dependent losses in a buck converter. The specific application for this thesis was a buck converter IC with an input voltage of up to 42V. The method utilizes the addition of an auxiliary circuit composed of a helper inductor and two helper power MOSFETs that compliment the switching transition of a conventional synchronous buck converter topology. It is shown in this thesis that by using the described topology, the switching losses of the high-side power MOSFET in a synchronous buck converter can be reduced by up to 45%. Furthermore, it is shown that a similar helper circuit could be used to reduce the gate drive losses for both power MOSFETs in a synchronous buck converter by up to 60%. Since the method requires the use of an additional helper inductor with a small value (10-50 nH), various methods to integrate this inductor into an IC package are investigated. 0.35μm BiCMOS technology was used to simulate and analyze the merits of the described topology and compare it to the LT8697, a hard-switched synchronous buck converter IC.

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Chapter 1

Introduction

The trend towards prevalent and more compact portable electronic devices in our daily lives means that it is becoming increasingly more important to shrink the physical size of the power converters inside these devices. Synchronous buck converters, like that shown in Figure 1-1, are one of the most widespread types of power converters inside the portable electronics. They generally consist of discrete passive components for filtering and feedback and active components for switching and feedback. A buck converter uses a complimentary PWM input drive to the switches S_T and S_B so that the node between them switches between V_{IN} and ground. The voltage on this switching node is then filtered by the ouput filter formed by L_o, C_0 and the load R_{Load}. A buck converter integrated circuit (IC) usually contains all of the necessary active components such as the N-channel power MOSFETs but requires the passive components to be supplied externally. The realization of Moore's Law [10] necessitates that buck regulator ICs shrink in size continuously, making the relative bulky size of the passive components a bottleneck for reducing the overall power converter size.

One of the most common approaches for shrinking the physical dimensions of the passive components in a switching converter is to increase the operating frequency of the converter [11]. A higher operating frequency reduces both the resonant frequency of an inductor-capacitor filter and the amount of energy stored in the components in each cycle, thus allowing the usage of inductors and capacitors with smaller physical

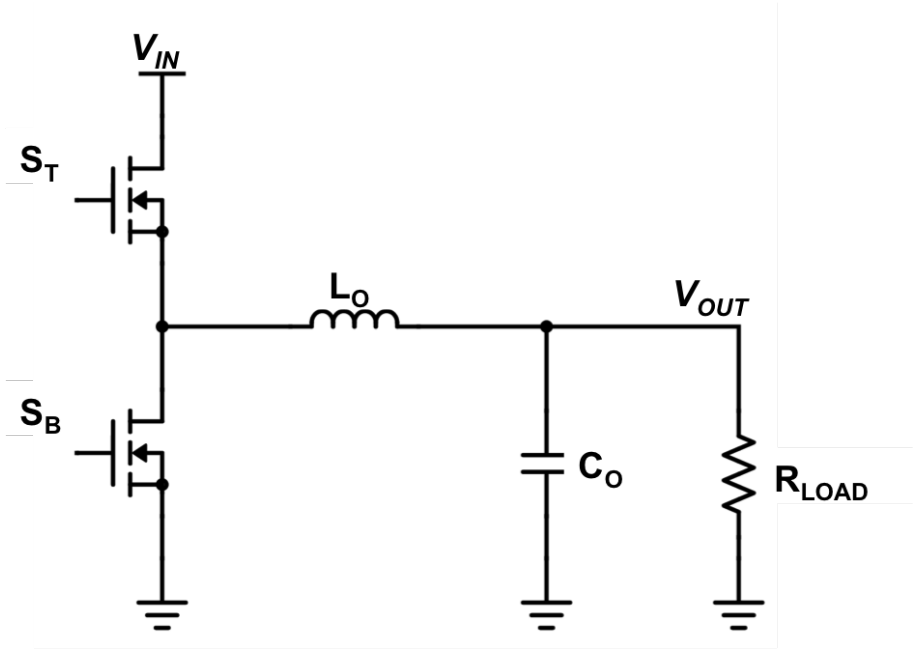

Figure 1-1: A synchronous buck converter

dimensions. Unfortunately, increasing the frequency does not come without drawbacks. Switching losses-the energy dissipated during the turning on and off of the power switches in each cycle-increases linearly as the operating frequency increases. Thus an increased frequency typically results in less efficient converters. Furthermore, electromagnetic interference (EMI) radiated by the high frequency switching currents can become an issue as the switching frequency is pushed higher.

Commercial buck converter ICs currently offer operating frequencies ranging between 100 KHz and 4 MHz for input voltages as high as 40 V. Although pushing this frequency range higher has the benefits of reducing both the overall size and cost of the converter, the lower efficiency and thermal issues caused by increased switching losses makes the use of the synchronous buck converter topology impractical above these frequencies for this voltage/power level.

The work described in this thesis is motivated by the goal of increasing the switching frequency in buck converter ICs and focuses specifically on the following three concepts to accomplish this goal: a zero-voltage switching buck converter topology, a method to reduce the gate drive losses and integration of the helper inductors into the IC package.

1.1 A Zero Voltage Switching Buck Converter

Among the switching losses in a synchronous buck converter IC, the turn on loss of the top switch is typically the dominating contributor. The body diode conduction in the bottom switch before turning the bottom switch on enables convenient zero voltage switching for the bottom switch. As a result the bottom switch does not dissipate the charge stored in its gate to drain capacitance. In addition the low gate drive requirements (VGS $\approx$ 3V) of the integrated power MOSFETs means that the gate drive losses also become less significant in the synchronous buck converter ICs. Therefore it is most important to address the losses caused by the top switch, particulalary during its turning on, in order to reduce the overall switching losses and increase the operating frequency of a synchronous buck converter IC.

This thesis proposes a modified synchronous buck converter topology that aims to reduce the top switch turn on losses through the addition of helper circuitry. With the proposed topology shown in Figure 1-2, it is possible to reduce the top switch turn on losses and push the frequency range of IC buck converters up to 10 MHz. This achievement would significantly shrink the overall converter size and cost compared to the ICs currently in the market.

In this proposed topology, after turning the main bottom switch S_B off, there is a large voltage difference ($V_{ds} \approx V_{in}$) across the main top switch S_T because the lower switch, S_B is conducting through its body diode. With such conditions it is inefficient to turn on the top switch because both the voltage across the switch and current through it will be high, resulting in large power losses. In order to create a zero voltage turn on condition for the top switch, before turning S_T on, first we turn the top helper switch S_{HT} on, thus charging up some current in the helper inductor L_H. When the current in L_H exceeds the current in the main inductor L_o, this excess current will start charging up the parasitic capacitance (mostly the Drain to Source Capacitance of S_B) in the main switch node, bringing the voltage up to the input voltage. Once the main switch node voltage is equal to the input voltage, we can turn S_T on with zero voltage across it, hence achieving zero voltage switching. We

then need to also turn the bottom helper switch S_{HB} on to discharge the current in the helper inductor L_H.

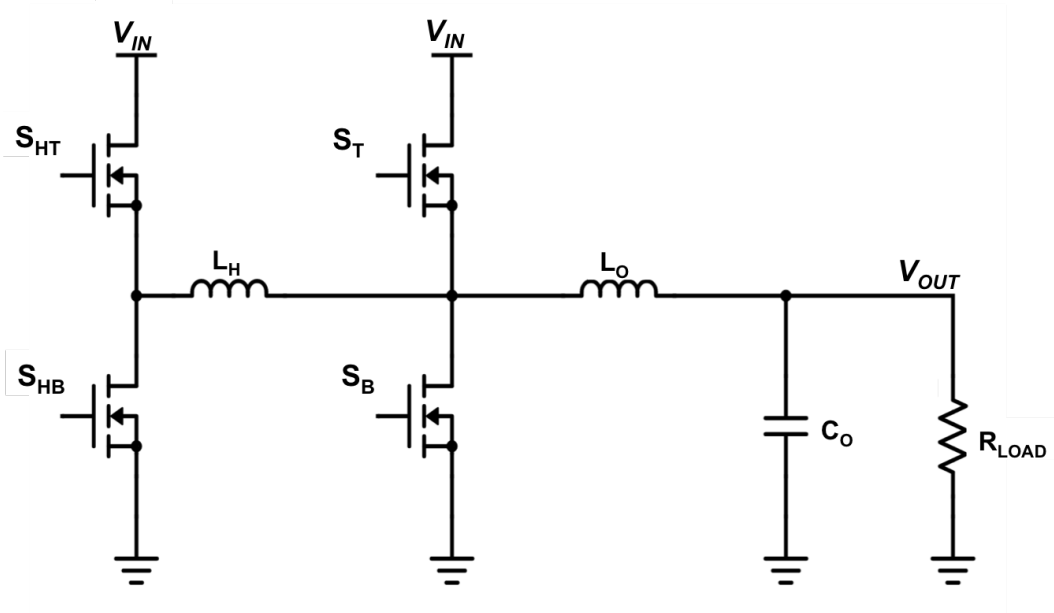

Figure 1-2: Proposed buck converter topology that accomplishes zero-voltage switching (ZVS) on the high side switch with the addition of helper circuitry

1.2 A Method to Reduce Gate Drive Losses

Energy dissipated when driving the gates of the main switches is another important source of frequency dependent loss in buck converter ICs. This loss needs to be addressed in order to achieve higher switching frequency in buck converter ICs. This thesis proposes a resonant gate driver shown in Figure 1-3, which utilizes a small valued (1-5 nH) helper inductor, L_{driver}. The inductor forms a resonant tank with the parasitic gate capacitance of the main switch and reduces the amount of energy required to charge up the gate.

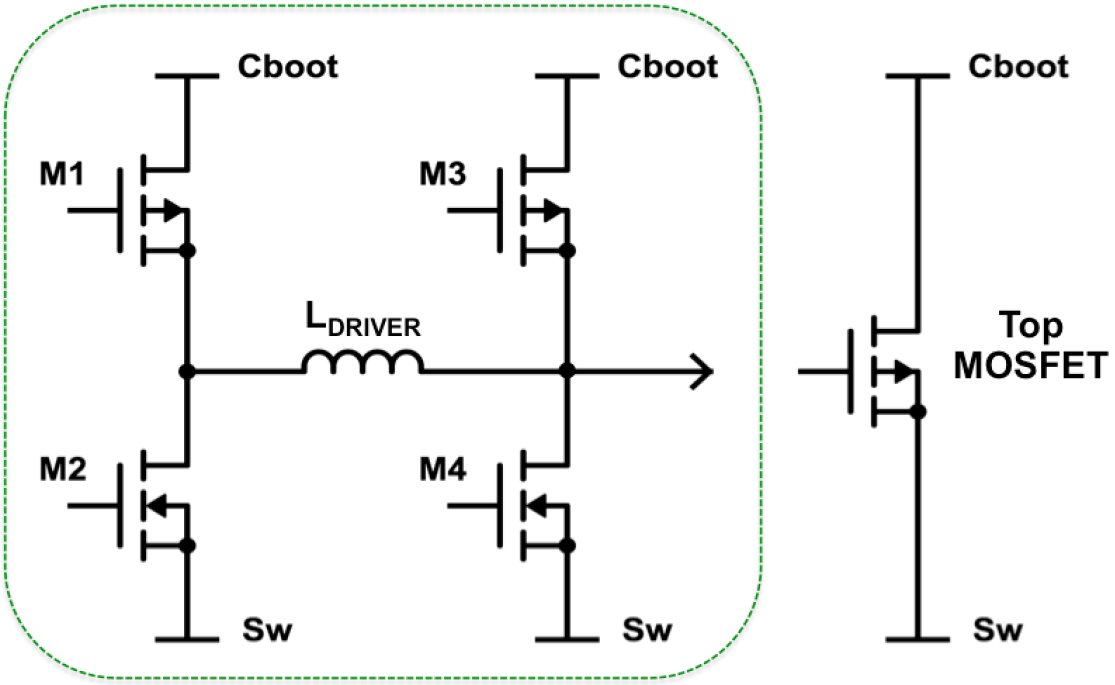

Figure 1-3: Proposed gate driver circuit (inside dashed lines) that utilizes gate charge recovery

1.3 Integration of the Inductors into the IC Package

Methods mentioned above help reducing the frequency dependent losses significantly, but they require the usage of inductors with fairly small values ($L_H \approx 10 - 50$ nH and $L_{driver} \approx 1 - 5$ nH). Making these helper inductors external to the buck converter IC increases the overall bill of materials and makes the board level design very difficult, due to the parasitic inductance of the PCB traces. Therefore, it is desirable to integrate these inductors into the IC package. Two possible methods for the integration of these inductors are investigated, both which are possible with flip-chip technology:

1. Spiral inductors formed by copper traces on a flip-chip die
2. Ferrite chip inductors soldered on a flip-chip die

1.4 Thesis Overview

This thesis is organized as follows. Chapter 2 presents the concept of frequency dependent losses in a buck converter and makes an analysis of those losses for the LT8697 [13], a hard-switched synchronous buck converter IC. Chapter 3 describes the proposed zero-voltage switching buck converter topology and compares the merits of this topology to the hard-switched LT8967 through simulations on 0.35μm BiCMOS technology. Furthermore, a closed-loop control circuitry that ensures the right timing of zero-voltage switching is implemented and simulated on 0.35μm BiCMOS technology. The results are compared to the open-loop controlled ZVS and LT8697. Chapter 4 describes the proposed resonant gate driver circuit and compares it to the nominal, hard-switched gate driver of the LT8697 through simulations on 0.35μm BiCMOS technology. Also an analysis for determining the optimal size of driver MOSFETs and helper inductor is carried out in this chapter. Chapter 5 focuses on the potential methods for integrating helper inductors into the IC package. Finally, chapter 6 summarizes the contributions of this work and gives a direction for future research.

Chapter 2

Frequency Dependent Losses in Synchronous Buck Converters

Synchronous buck converter ICs are one of the most efficient ways for stepping down a DC input voltage to a lower DC output voltage. However, they require physically large inductors and capacitors to eliminate the output current ripple and output voltage ripple that are caused by the switching nature of the converter. The necessary inclusion of large passive components makes synchronous buck converter ICs undesirable for space-constrained applications, such as portable electronics devices or automotive power converters.

Increasing the switching frequency of a switching converter is a common approach to reduce the size of passive components in the converter. This is because, as the switching frequency increases, the energy that needs to be stored and released by passive components in each cycle decreases, hence passive components with smaller values and dimensions can replace larger passive components. On the other hand, as the switching frequency increases, frequency dependent losses increase proportionally. Efficiency is affected adversely by the frequency dependent losses, shown in Figure 2-1 for the LT8610 [12], and drops sharply with the increased switching frequency. Furthermore, thermal issues might become a serious problem if the energy dissipated due to frequency dependent losses cannot be released out of the system. In order to limit the frequency dependent losses, semiconductor manufacturers limit the switching

frequency of their synchronous buck converter ICs.

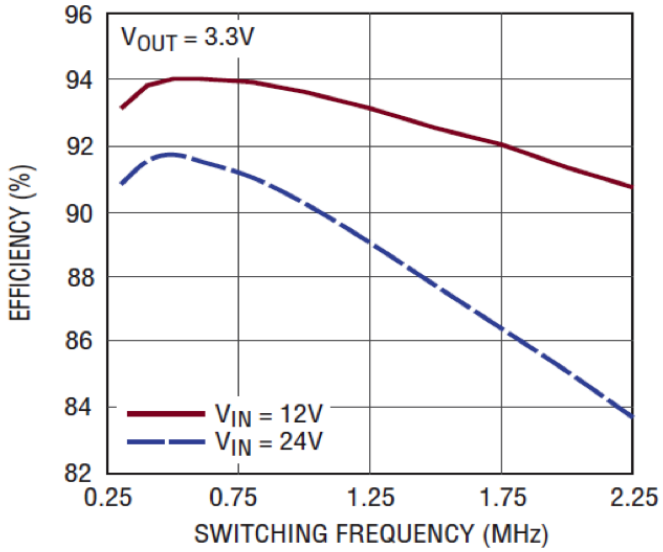

Figure 2-1: Efficiency decrease in LT8610, as the switching frequency is increased

2.1 Operation of the Synchronous Buck Converter

A synchronous buck converter like that shown in Figure 2-2 is mainly composed of two switches in the half bridge configuration, an output inductor and an output capacitance. It operates by switching the V_{SW} node between the input DC voltage (V_{IN}) and ground by periodically turning the two switches on and then off. The The square wave created at the V_{SW} node is then filtered through the output inductor L_O and capacitor C_O to generate a lower output DC voltage such that ($V_{OUT} < V_{IN}$).

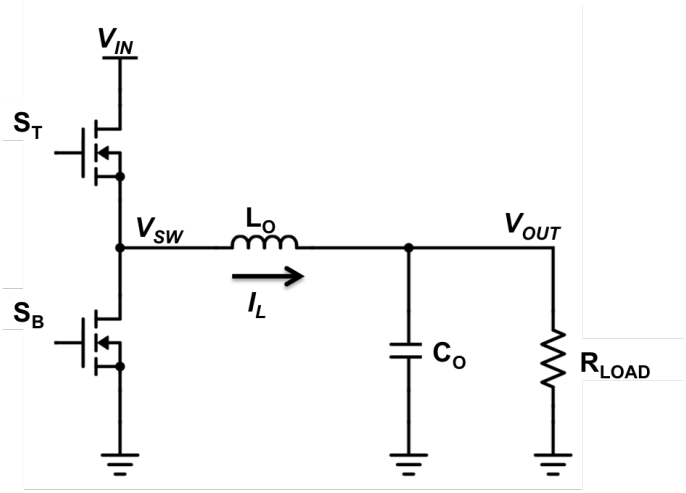

Figure 2-2: A synchronous buck converter

Operating waveforms for a synchronous buck converter can be seen in Figure 2-3. The top switch, which is a MOSFET in this case, is turned on with a duty cycle of D, during which time the switch node voltage (V_{SW}) will be equal to the input voltage V_{IN}. The bottom switch, also a MOSFET in this case, is turned on with a duty cyle of $1 - D$ and during this time the switch node voltage will be zero. The output voltage, which is the time averaged version of switch node voltage will be given by the equation:

$$V_{OUT} = D * V_{IN} \tag{2.1}$$

Frequency dependent losses in a synchronous buck converter include primarly the switching losses during the top MOSFET turn-on, switching losses during the bottom MOSFET turn-on, gate drive losses and inductor core losses. Since a typical synchronous buck converter IC will integrate power MOSFETs and their respective drivers into the semiconductor die, the energy dissipated due to these three sources will directly affect the thermal issues related to the IC, whereas the inductor core losses will not contribute to a significant temperature increase in the IC. Furthermore, it is easier to address the losses generated inside the IC with a smart topology implementation as shown in this thesis, whereas addressing the core losses would

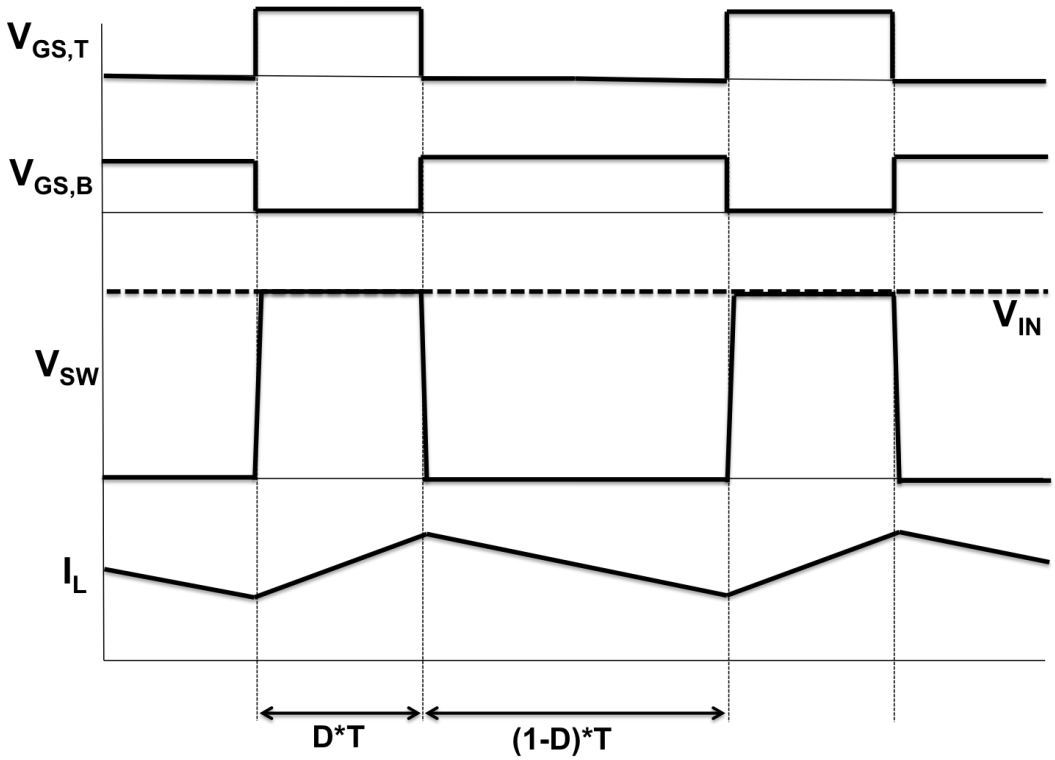

Figure 2-3: Operation of the synchronous buck converter

require detailed magnetics design and is outside of the scope of this thesis.

2.2 Switching Losses During the Top MOSFET Turn-On

During the switching cycle transition when the bottom MOSFET is turned off and the top MOSFET is turned on, there will be a significant turn-on loss on the top MOSFET since it will need to conduct some current when its drain to source voltage is a nonzero value. In order to prevent "shoot through" current as a result of both the top and bottom MOSFETs being on at the same time, a small time before the top MOSFET is turned on, known as the dead-time, the bottom MOSFET needs to be turned off. During this portion of the switching transition, the inductor current is carried by the body diode of the bottom MOSFET until the top MOSFET is turned on. This means that right before the top MOSFET is turned on, the voltage on the

switch node will be a diode drop below the ground, $V_{SW} = -V_{diode}$, meaning that the drain to source voltage of the top MOSFET will be large: $V_{DS} = V_{IN} + V_{diode}$.

During the turn on of the top MOSFET, until the parasitic capacitance on the switch node is charged all the way up to the input voltage, $V_{SW} = V_{IN}$, there will be a nonzero voltage and nonzero current across the top MOSFET (during time intervals t_1 and t_2 in Figure 2-4). The amount of loss can be approximately given as $P_{top_{on}} = V_{IN} * I_{OUT} * (t_1 + t_2)/2$. Here t_1 is the time interval spanning between the top MOSFET's gate drive voltage exceeding the threshold voltage ($V_{GS} = V_{th}$), until all of the inductor current ($I_L = I_{OUT}$) commutes to the top MOSFET. t_2 is the time interval between the point at which the bottom MOSFET's body diode stops conducting current, until the parasitic capacitance on the switch node charges up all the way to the input voltage V_{IN}.

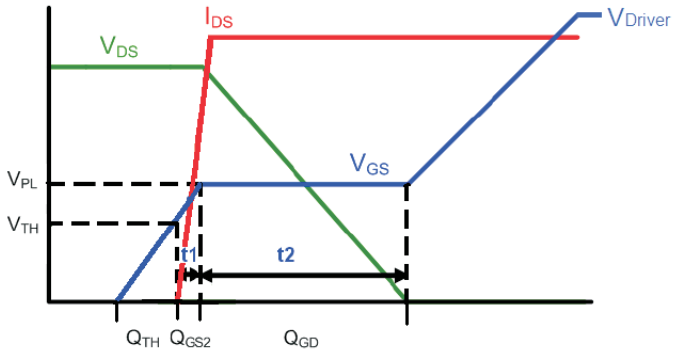

Figure 2-4: V_{DS}, I_{DS} and V_{GS} of top MOSFET during its turn on [4]

In addition to the conduction losses described above, during the turn-on of the top MOSFET there will be reverse recovery losses in the bottom MOSFET as the inductor current is commutated from the forward biased body diode of the bottom MOSFET to the drain-source channel of the top MOSFET. Figure 2-5 shows that as the current through the body diode goes to zero, the diode gets reverse biased. At this point the top MOSFET is conducting all of the inductor current and the switch node is being pulled to V_{IN} as the top MOSFET turns fully on. This means that the parasitic capacitance of the p-n junction in the bottom MOSFET body diode will need to be charged up to V_{IN} and the inrush of charges to this p-n junction capacitance

will generate a negative current in the body diode, which is called the reverse recovery current. As the reverse recovery current becomes zero again, there will be nonzero voltage and nonzero current across the body diode and the loss generated in the bottom MOSFET can be approximately given by $P_{bottom_{off}} = V_{IN} * I_{rr(peak)} * t_{rr2}/2$, where $I_{rr(peak)}$ is the peak value of the reverse recovery current and depends on the minority carrier concentration of the p-n junction as well as the turn on speed of the top MOSFET. If this switching loss is not properly addressed, reverse recovery can also become a significant source of losses in a buck converter.

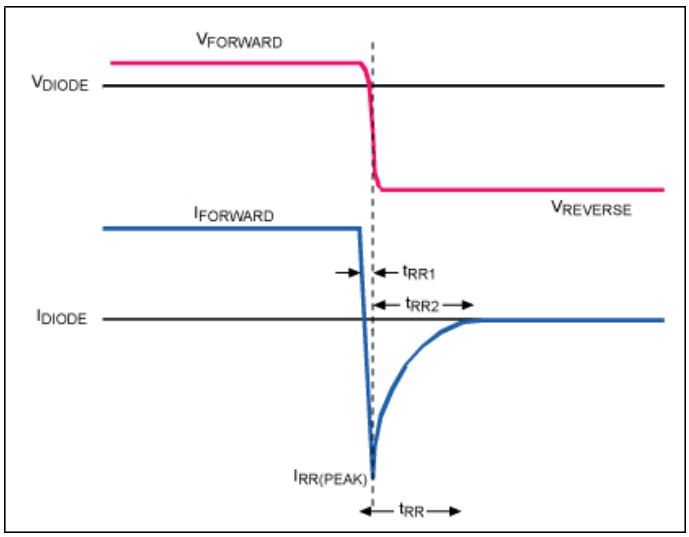

Figure 2-5: Voltage and current across bottom MOSFET's body diode during its turn off [5]

2.3 Switching Losses During the Bottom MOSFET Turn-on

During the switching cycle transition when the bottom MOSFET is turned on and the top MOSFET is turned off, there will be some turn-off loss on the top MOSFET due once again to simultaneous nonzero voltage and nonzero current across it. However the turn-on loss on the bottom MOSFET will be negligible, since it can be turned on with near zero voltage switching (ZVS) after its body diode is forward biased because

the top MOSFET as turned off and the inductor current has commutated its current to the body diode.

As shown in Figure 2-6, when the top MOSFET is turning off, the parasitic capacitance of the switch node, which was charged up to V_{IN}, will be slowly discharged during the time interval t_3. During this time the voltage across the top MOSFET is rising as the switch node voltage falls. Importantly, most of the inductor current is still being provided by the top MOSFET with only a small portion being provided by the parasitic capacitance of the switch node. When the capacitance of the switch node is fully discharged, the voltage of the switch node then goes below zero and the bottom MOSFET's body diode turns on and the inductor current begins to commutate its current to the body diode during time interval t_4. The overlap of nonzero voltage and current across the top MOSFET will generate a loss that can be approximately given by $P_{top_{off}} = V_{IN} * I_{OUT} * (t_3 + t_4)/2$.

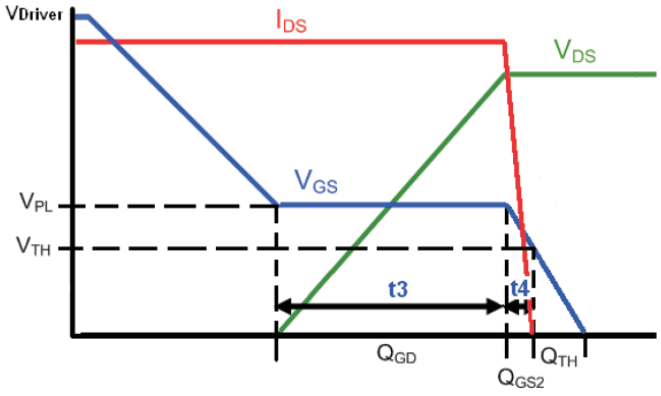

Figure 2-6: V_{DS}, I_{DS} and V_{GS} of top MOSFET during its turn off [4]

2.4 Gate Drive Losses

In order to turn on the top MOSFET and bottom MOSFET at each respective switching cycle, their gate capacitances, $C_{GS_{top}}$ and $C_{GS_{bottom}}$ will have to be charged up to the gate drive voltage V_{driver}. This charging of the gate capacitances has associated gate drive losses that can be given by $P_{top_{drive}} = C_{GS_{top}} * {V_{driver}}^2$ and $P_{bottom_{drive}} = C_{GS_{bottom}} * {V_{driver}}^2$. Half of this loss is incurred during the charging of

the gate capacitance because charging a capacitor mandates that the same amount of energy that is stored on the capacitor, ($\frac{1}{2}CV^2$), is also dissipated in the series charging resistance. The stored energy on the gate capacitance is then wasted when the switch is turned off when the gate drive is brought low. These gate drive losses can be a significant part of the frequency dependent losses if the gates are driven with a relatively large voltage.

2.5 Inductor Core Losses

During the operation of the buck converter, the inductor current will increase when the top MOSFET is on and it will decrease when the bottom MOSFET is on. This will generate a ripple current in the inductor given by $I_{ripple} = (1 - D) * T * V_{OUT}/L$, where D is the duty cycle in which the top MOSFET is on, T is the switching period, V_{OUT} is the output voltage and L is the inductance. This ripple current causes a swing in the magnetic flux in the inductor core and thus a frequency dependent core loss due to magnetic hysteresis, which can be given by the formula $P_{core} = \alpha * {B_{ripple}}^{\beta} * f^{\gamma}$ [7], where α, β, and γ are based on the magnetic characteristics of the core and are determined empirically. $B_{ripple} = L * I_{ripple}/A$ is the magnetic flux density and A is the cross section of the inductor core. Increasing the switching frequency will reduce I_{ripple} and thus reduce the magnetic flux ripple B_{ripple} for a given inductor value and since in most cases β is larger than γ,the overall core losses will be decreased as the result of a marginal increase in frequency.

2.6 Distribution of Frequency Dependent Losses

In order to analyze the distribution of frequency losses inside a synchronous buck converter IC in order to determine the largest contributor to the switching loss, a SPICE simulation of the hard-switched synchronous buck converter IC LT8697 was run. The results of this simulation are summarized in Table 2.1. Notice that the energy stored in the drain to source capacitance of the bottom MOSFET during the

rising of the switch node voltage is then recycled during the closing of the bottom MOSFET when the switch node voltage is falling. It should be noted that the charging of this capacitance during the top MOSFET turn on does dissipate $\frac{1}{2}CV_{IN}{}^2$ in the top MOSFET due to its on resistance.

Table 2.1: Distribution of losses in the LT8697 buck converter, at a typical operating point with $V_{OUT} = 5V$ and $I_{OUT} = 2A$

V_{IN}	$40V$	$25V$	$15V$	$9V$
Top MOSFET Turn On Loss	$505nJ$	$294nJ$	$125nJ$	$53nJ$
Bottom MOSFET Turn Off Loss	$145nJ$	$62nJ$	$24nJ$	$9nJ$
Top MOSFET Gate Drive Loss	$11nJ$	$11nJ$	$8nJ$	$6nJ$
Top MOSFET Turn On Loss	$68nJ$	$29nJ$	$12nJ$	$5nJ$
Bottom MOSFET Turn Off Loss	$-142nJ$	$-61nJ$	$-24nJ$	$-9nJ$
Bottom MOSFET Gate Drive Loss	$16nJ$	$15nJ$	$13nJ$	$9nJ$

The results show that Top MOSFET turn on loss is the main contributor to the frequency loss and not surprisingly, because of the V^2 relation, it becomes even more significant as the input voltage of the converter is increased. Furthermore, we can see from these results that the gate drive losses are smaller compared to other frequency dependent losses, that is because the MOSFETs integrated into the LT8697 IC have a very low gate threshold value and they are therefore driven with a small gate drive voltage of $V_{drive} = 3V$. However, since this gate drive voltage V_{drive} is always kept around $3V$, even when the input voltage V_{IN} is reduced, the gate drive losses become a larger proportion of the overall switching losses at smaller V_{IN} values.

Upon seeing these results it becomes clear that in order to reduce frequency dependent losses and increase the switching frequency of a buck converter, the Top MOSFET turn on loss is the most important one to tackle. In the next chapter, we will see a new buck converter topology which uses a helper circuitry to turn on the top MOSFET with zero voltage switching and thus eliminates the most significant

contributor to the frequency dependent losses. With the help of this topology, the frequency of the buck converter IC LT8697 could be increased from 2.2MHz to as high as 8MHz without running into thermal issues and maintaining at least the baseline efficiency of the converter.

Chapter 3

Zero Voltage Switching with the New Helper Circuit Topology

3.1 Topology Concept

As explained in the previous chapter, the main contributor to the switching losses in the hard switched buck converter LT8697 IC is the turn on losses of the top MOSFET. In order to eliminate these losses a modified buck converter topology with two additional helper MOSFETs and a helper inductor are included. The modified topology that is proposed in this thesis is shown in Figure 3-1. This topology uses a method similar to described in [3] to accomplish zero voltage turn on of the main top MOSFET, S_T.

The working principle of this new topology is explained with the help of the simplified switching waveforms shown in the Figure 3-2. In this figure S_T, S_B, S_{HT}, S_{HB} are the gate drive voltages of the main top MOSFET, main bottom MOSFET, helper top MOSFET and helper bottom MOSFET respectively. I_H is the current in the helper inductor, I_{OUT} (which is assumed constant for simplicity) is the current in the main inductor, V_{SW} is the voltage of the main switch node and V_{SWH} is the voltage of the switch node between the helper MOSFETs.

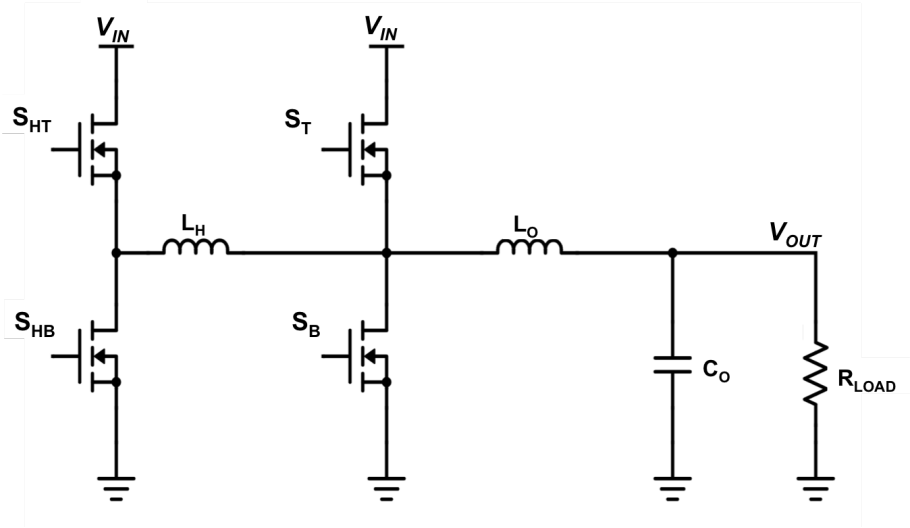

Figure 3-1: Proposed Topology for Significantly Reducing the Top MOSFET Turn on Losses

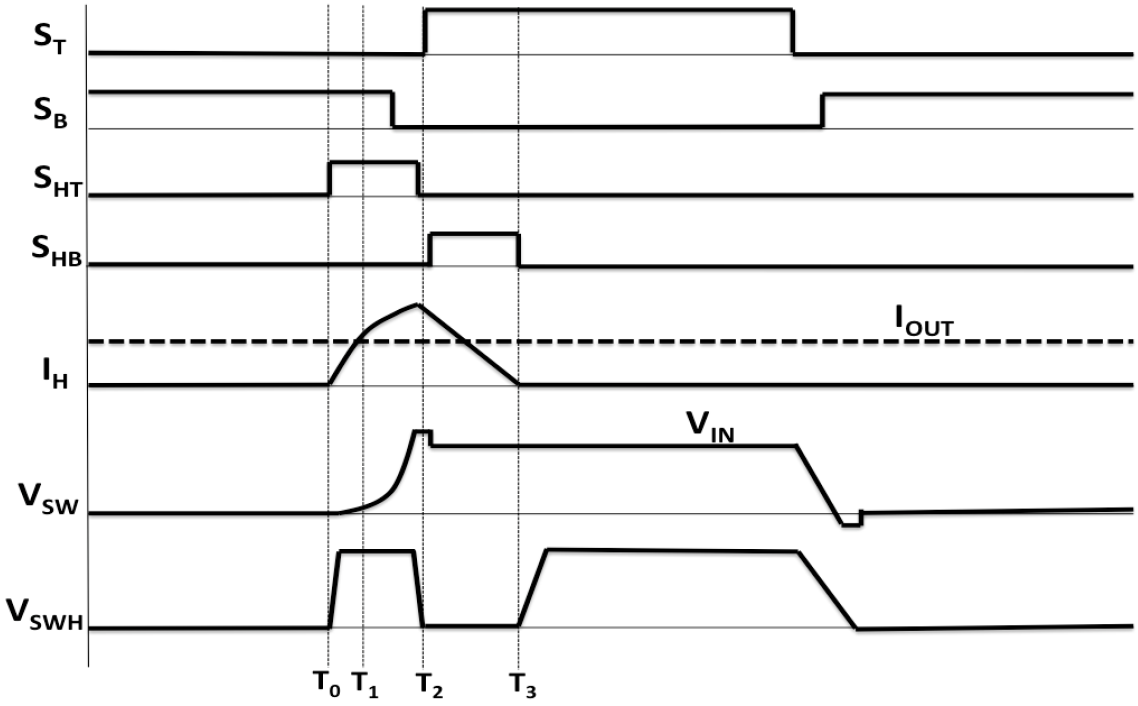

Figure 3-2: The waveforms of the zero voltage switching buck converter,

Zero voltage switching turn on of the main top MOSFET is accomplished as a result of the following sequence:

1- Before the main bottom MOSFET S_B is turned off, At time $t = T_0$ the top helper MOSFET S_{HT} is turned on.

2- Because the left end of the helper inductor L_H is connected to the input voltage source V_{IN}, and the right end is initially at ground, the current in the helper inductor builds up very quickly.

3- When the current in L_H exceeds the current in the main inductor L_O at time $t = T_1$, the parasitic capacitance in the switch node will start to charge up until the switch node voltage eventually reaches to the level of input voltage V_{IN}. A short time after the main inductor current has been commutated from the main bottom MOSFET to the helper inductor, the main bottom switch is turned off.

4- At time $t = T_2$ when the switch node voltage V_{SW} exceeds V_{IN}, due to the body diode drop of excess current going into the DC supply, the main top MOSFET is turned on with approximately zero drain to source voltage, hence we accomplish the zero voltage switching on this MOSFET. Also at this time the helper top MOSFET is turned off and the helper bottom MOSFET is turned on to attenuate the current built up in L_H to zero.

5- Now the right end of the helper inductor L_H is connected to V_{IN}, whereas the left end is at the ground level and the current I_H will diminish and eventually become zero at time $t = T_3$.

3.2 Sizing of the Helper MOSFETs

In order to determine the optimal size for the helper MOSFETs in the new buck converter topology we ran simulations using the $0.35\mu m$ BiCMOS process node, which is also the processing node in which our benchmark IC LT8697 was designed. We modified the LT8697's power stage by adding the helper MOSFETs and a high side/low side gate driver designed to drive these smaller MOSFETs. Since the turn on and turn off timing of the helper MOSFETs had to be adjusted very precisely for maximum efficiency, we initially controlled all the MOSFETs with open loop periodic gate drive signals.

For the simulations we ran, we chose the DC operating point to be $V_{IN} = 15V$, $V_{OUT} = 5V$ and $I_{OUT} = 2A$, since this is a typical automotive application of the

Table 3.1: Additional losses generated by the top helper MOSFET P_{HT} and bottom helper MOSFET P_{HB} for different MOSFET widths

W_{HB}, W_{HT} given in μm	$W_{HT} = 11000$	$W_{HT} = 22000$	$W_{HT} = 33000$	$W_{HT} = 44000$
$W_{HB} = 5500$	$P_{HT} = 70nJ$ $P_{HB} = 17nJ$	$P_{HT} = 39nJ$ $P_{HB} = 18nJ$	$P_{HT} = 35nJ$ $P_{HB} = 20nJ$	$P_{HT} = 33nJ$ $P_{HB} = 23nJ$
$W_{HB} = 11000$	$P_{HT} = 71nJ$ $P_{HB} = 16nJ$	$P_{HT} = 40nJ$ $P_{HB} = 18nJ$	$P_{HT} = 36nJ$ $P_{HB} = 21nJ$	$P_{HT} = 34nJ$ $P_{HB} = 22nJ$
$W_{HB} = 22000$	$P_{HT} = 71nJ$ $P_{HB} = 15nJ$	$P_{HT} = 42nJ$ $P_{HB} = 18nJ$	$P_{HT} = 37nJ$ $P_{HB} = 20nJ$	$P_{HT} = 35nJ$ $P_{HB} = 20nJ$
$W_{HB} = 44000$	$P_{HT} = 71nJ$ $P_{HB} = 16nJ$	$P_{HT} = 47nJ$ $P_{HB} = 17nJ$	$P_{HT} = 41nJ$ $P_{HB} = 19nJ$	$P_{HT} = 40nJ$ $P_{HB} = 19nJ$

benchmark IC LT8697. We used $L_H = 20nH$, which is the optimal helper inductor size as explained later in this chapter. We started with helper MOSFETs that were significantly smaller compared to the main MOSFETs in the LT8697 and we swept through increased width sizes of the helper MOSFETs to determine the optimal size of the helper MOSFETs. The results of these simulations are summarized in Table 3.1. Although not shown in the table, the turn on loss of the top MOSFET that was shown to be 125nJ at this operating point in Table 2.1, was completely eliminated in each of these different helper MOSFET sizes. This means that even when the helper MOSFETs are not sized optimally, (for example $W_{HB} = 44000\mu m$ and $W_{HT} = 11000\mu m$) the additional loss generated by the helper MOSFET was significantly smaller than the eliminated turn on loss.

In Table 3.1 we can see that the major contributor to the helper MOSFET losses are in the top helper MOSFET, since unsurprisingly it has high turn on loss just like the turn on loss of a hard switched buck converter's top MOSFET. Losses generated in the gate drivers of the helper MOSFETs were negligible (less than $1nJ$) and not shown in Table 3.1.

One of the trends seen in Table 3.1 is that the helper top MOSFET loss (P_{HT}) increases as the width of the bottom helper MOSFET W_{HB} is increased. That is because the parasitic capacitance on the node between the two helper MOSFETs increases with increasing W_{HB} and causes a larger amount of switching loss during

the turn on of the top helper MOSFET.

Another trend of Table 3.1 is that the loss of the helper top MOSFET (P_{HT}) decreases significantly as the helper top MOSFET width W_{HT} is increased from $W_{HT} = 11000\mu m$ to $W_{HT} = 22000\mu m$, however after that point the loss decreases only marginally as the width is increased further. That is because when W_{HT} is $11000\mu m$ most of the losses ($50nJ$ of the total loss of $P_{HT} = 70nJ$) are conduction losses generated due to the top helper MOSFET conducting the helper inductor current. Increasing the width to W_{HT}=$22000\mu m$ cuts these losses to halve by halving the $R_{DS(ON)}$ of the top helper MOSFET. On the other hand, increasing W_{HT} will increase the turn on loss of the top helper MOSFET due to an increased parasitic capacitance on the node between the two helper MOSFETs. When W_{HT} is increased further than $22000\mu m$, the increased turn on loss will cancel the benefits of the decreased conduction loss and the overall top MOSFET loss P_{HT} will only marginally decrease after this point.

One of the main considerations when sizing the helper MOSFETs was that the new topology should not increase the die area of the IC significantly, since this would increase the manufacturing cost of the IC. $W_{HT} = 22000\mu m$ and $W_{HB} = 5500\mu m$ were chosen as the optimal helper MOSFET sizes, which will significantly reduce the losses during the main top MOSFET's turn on from $125nJ$ (when the main top MOSFET is hard switched) to $P_{HT} + P_{HB} = 57nJ$ (which is less than half) while only requiring a small amount of die area.

3.3 Sizing of the Helper Inductor

In order to determine the optimal size for the helper inductor, we used a similar approach to determining the optimal helper MOSFET sizes. We ran simulations using the using the $0.35\mu m$ BiCMOS process node, where all four MOSFETs were controlled with open loop periodic gate drive signals.

For the simulations we ran, we again chose the DC operating point to be $V_{IN} = 15V$, $V_{OUT} = 5V$ and $I_{OUT} = 2A$, since this is a typical automotive application of

Table 3.2: Additional losses generated by the top helper MOSFET P_{HT} and bottom helper MOSFET P_{HB} for different helper inductor sizes

	$L_H = 10nH$	$L_H = 20nH$	$L_H = 40nH$	$L_H = 80nH$
P_{HT}	$36nJ$	$39nJ$	$40nJ$	$42nJ$
P_{HB}	$13nJ$	$18nJ$	$31nJ$	$49nJ$

the benchmark IC LT8697. We used top and bottom helper MOSFETs with sizes $W_{HT} = 22000\mu m$ and $W_{HB} = 5500\mu m$ respectively, since these were the optimal sizes determined in the previous section (section 3.3). Our optimization started with helper inductor sizes of $L_H = 10nH$ because inductance values smaller than that causes significant reverse current issues that will be explained in the next section (section 3.5). We swept through increasing helper inductor sizes to determine the optimal sized helper inductor by comparing the losses in the helper MOSFETs to the efficiency savings in the main top MOSFET. The results of these simulations are summarized in Table 3.2.

Table 3.2 shows that as the helper inductor size increases, losses in both the helper top MOSFET and helper bottom MOSFET increase. This is because when the helper inductor size is larger, it takes a longer time to build up or diminish a certain amount of current in that helper inductor and this causes higher conduction losses in the helper MOSFETs since they conduct the current for a longer duration. If the current in the main inductor L_O is I_O and the input voltage is V_{IN}, the time it takes for helper inductor current to exceed I_O and start charging the switch node will be given by the equation $T_{cond} = L_H * I_O/V_{IN}$. It is clear from this equation that, when a larger helper inductor is used, the process to build up a certain amount of current in the helper inductor will take longer, hence larger conduction losses in the helper MOSFETs.

Based on the simulation results in Table 3.2, we initially decided to choose $L_H = 10nH$. However, this inductance value later proved to be extremely hard to do closed loop control with because of the ns level delays needed in the comparators. We eventually decided to use $L_H = 20nH$ as our optimal helper inductor size because this was easier to implement the control with. Furthermore as explained in the

next section, the reverse current problem becomes worse when the inductor value is decreased.

3.4 The Problem of Reverse Current in the Helper Inductor

One of the main problems we discovered with this topology is the occurrence of a reverse current in the helper inductor. This problem is caused by the fact that after the zero voltage switching is accomplished on the main top MOSFET, S_T, and the helper inductor current diminishes to $I_H = 0$, this inductor will have a larger voltage on its right end at the main switch node ($V_{SW} = V_{IN}$), compared to its left edge at the helper MOSFET switch node, which will be at the ground level ($V_{SWH} = 0$). This voltage difference will induce a current in the helper inductor that is directed towards the switch node of the two helper MOSFETs. This reverse current becomes an even larger problem due to the turn off delays in the bottom helper MOSFET as explained with the help of Figure 3-3, which shows the initially proposed control algorithm that self-adjusts and finds the right switching time for the helper MOSFETs.

The details of the control algorithm will be explained in Section 3.6, however in this section we will focus on the turning on and off of the bottom helper MOSFET. In Figure 3-3, we can see that bottom helper MOSFET is turned on with the signal $PWMH\_ZVS$, which is also the turn on signal for the main top MOSFET and that moment corresponds to time $t = T_2$ in Figure 3-2. After this moment the current in the helper inductor will eventually diminish to zero due to the larger voltage on its right side ($V_{SW} = V_{IN}$), compared to its left side ($V_{SWH} = -I_H * R_{DS(HB)}$, where $R_{DS(HB)}$ is the on resistance of helper bottom MOSFET). The control algorithm compares the voltage $V_{SWH} = -I_H * R_{DS(HB)}$ to the ground level and then generates the turn off signal for the bottom helper MOSFET when this voltage crosses the ground level, meaning that the current in the helper inductor has completely diminished. In an ideal control structure without any delays that moment corresponds

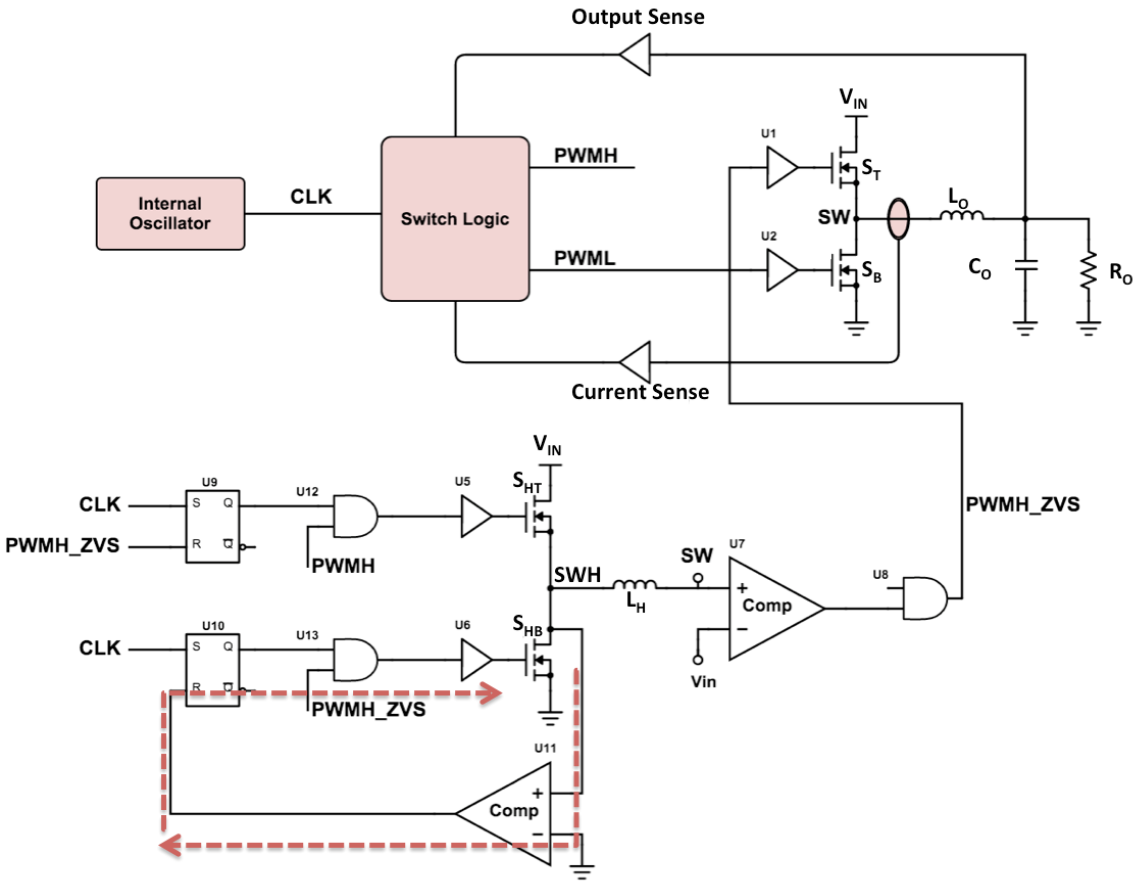

Figure 3-3: Initially proposed control algorithm for helper MOSFETs

to time $t = T_3$ in Figure 3-3. However, due to the propagation delay in the critical path from the ground level comparator to the bottom helper MOSFET driver, which is shown by the dashed red arrows in Figure 3-3, the bottom helper MOSFET will not be turned off immediately. During that delay (T_{delay}), the voltage difference on the helper inductor $V_H = V_{SW} - V_{SWH} = V_{IN}$ will induce a reverse current that is equal to $I_{rev} = T_{delay} * V_H/L_H$. Using the 0.35$\mu$m BiCMOS process node, we designed a very fast ground level comparator to reduce T_{delay} as low as possible, however $T_{delay} = 2.4ns$ was the smallest value we were able to achieve. This means that, when the input voltage is $V_{IN} = 15V$ and the helper inductor value is $L_H = 20nH$ (the optimal value from Section 3.3), a reverse current of $I_{rev} = 1.8A$ is generated. This reverse current would become even larger when the input voltage of the converter is close to the maximum range of $V_{IN(max)} = 42V$.

This reverse current problem causes an overall efficiency loss in this synchronous buck converter topology because this significant amount of current will be conducted through the body diode of the helper top MOSFET, S_{HT} until the main top MOSFET, S_T is turned off. Therefore, a solution for the reverse current is necessary to improve the efficiency of this topology.

3.5 Solution of Reverse Current Problem

In order to minimize the reverse current caused by the turn off delay of the bottom helper MOSFET we decided to slightly change our topology and use a diode connected bottom helper MOSFET, as shown in Figure 3-4. This topology will work in a similar way to the initially proposed topology, but without requiring the delayed control loop on the bottom helper MOSFET. At the moment when the top helper MOSFET is turned off, positive current carried by the helper inductor will commutate to the diode connected S_{HB}. This current will eventually diminish to zero like before, due to the voltage difference across the helper inductor ($V_H = V_{IN}$).

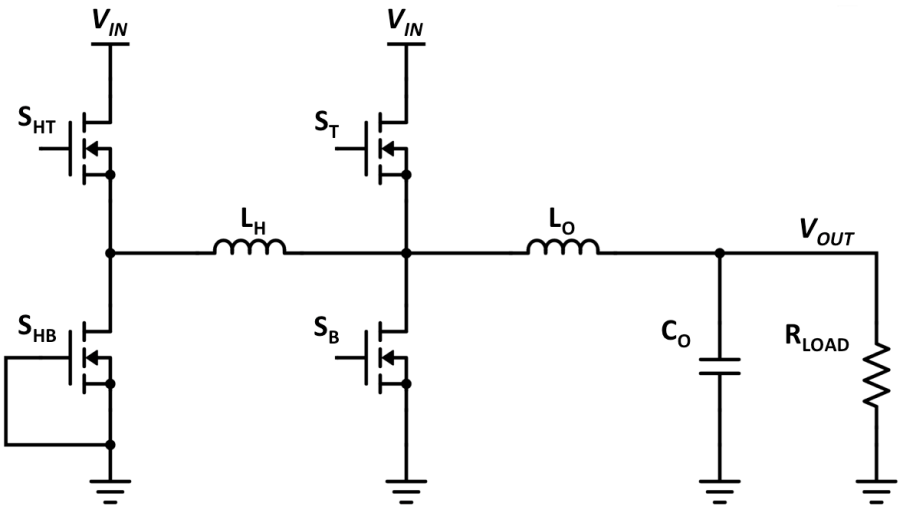

Figure 3-4: Proposed topology to minimize the reverse current in the helper inductor

Unfortunately this change in the topology does not completely eliminate the reverse current issue. At the moment when the helper inductor current I_H reduces

to zero, the node between the main MOSFETs will have a voltage of $V_{SW} = V_{IN}$, whereas the node between the helper MOSFETs will have a voltage of $V_{SWH} = 0$. This voltage difference will still induce a reverse current in the helper inductor, until the parasitic capacitance of the node between the helper MOSFETs gets charged up all the way to the input voltage ($V_{SWH} = V_{IN}$). The circuitry around the helper inductor can be simplified to that of Figure 3-5. Now, the reverse current can be calculated by solving the set of differential equations:

$$I_{rev}(t) = C_{SWH} * \frac{dV_{SWH}(t)}{dt} \tag{3.1}$$

$$V_{IN} - V_{SWH}(t) = L_H * \frac{dI_{rev}(t)}{dt} \tag{3.2}$$

Given the initial conditions of $I_{rev}(t = 0) = 0$ and $V_{SWH}(t = 0) = 0$, the solution of these equations will be $I_{rev}(t) = \omega * V_{IN} * sin(\omega t)$ and $V_{SWH}(t) = V_{IN} - V_{IN} * cos(\omega t)$, where $\omega = 1/\sqrt{L_H * C_{SWH}}$. Notice here, however, $V_{SWH}(t)$ can never exceed $V_{SWH}(max) = V_{IN} + V_{diode}$, since it will be clamped to the input voltage source by the body diode of the top helper MOSFET. Using these results, we can see that the peak value of the reverse current will be $I_{rev} = V_{IN}/\sqrt{L_H * C_{SWH}}$.

The comparison of the reverse current when the bottom helper MOSFET is diode connected vs when it is on/off controlled, can be seen in Table 3.3. In reality C_{SWH} will be a function of V_{SWH} since the parasitic capacitance of the top and bottom helper MOSFETs will be dependent on their drain to source voltages and the I_{rev} will not be exactly given by the simplified expression $I_{rev} = V_{IN}/\sqrt{L_H * C_{SWH}}$ when the bottom helper MOSFET is diode connected. Therefore, we used SPICE simulations to determine the reverse current values in the diode connected case. On the other hand we used the equation $I_{rev} = T_{delay} * V_H/L_H$, with $T_{delay} = 2.4ns$ to determine the reverse current values in the on/off controlled bottom helper MOSFET case.

After analyzing the results from Table 3.3, we decided to use the bottom helper MOSFET as a diode connected MOSFET, since this will significantly reduce the

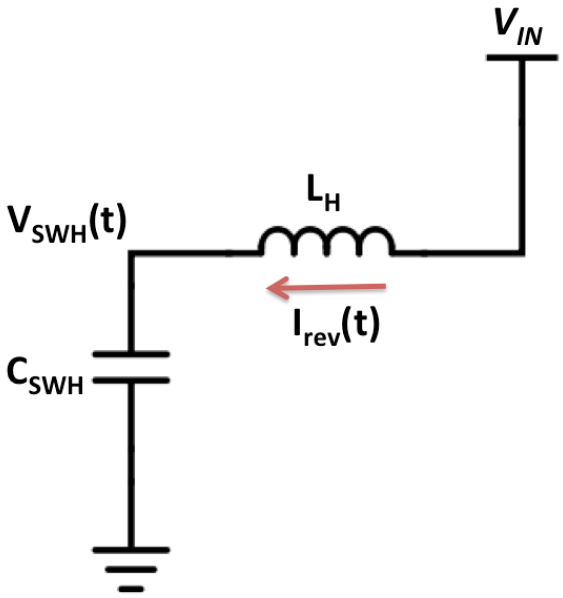

Figure 3-5: Simplified schematics of the reverse current generation when S_{HB} is diode connected

Table 3.3: Reduction of the reverse current values when S_{HB} is diode connected

V_{IN}	$40V$	$25V$	$15V$	$9V$
I_{rev} when S_{HB} is diode connected	$2.81A$	$1.72A$	$0.97A$	$0.51A$
I_{rev} when S_{HB} is on/off controlled	$4.8A$	$3.0A$	$1.8A$	$1.08A$

reverse current issue and improve the overall efficiency of the converter. This approach also simplifies the control algorithm of our zero voltage switching buck converter as will be seen in the next section.

3.6 Control Algorithm

Our benchmark LT8697 IC, is a hard switched synchronous buck converter and it is controlled through a current mode feedback control loop. Figure 3-6 shows a simplified block diagram of this current mode control scheme, without going into the details of each block. The IC has an "internal oscillator" which generates the clock signal, CLK, to synchronize the switching cycles. In the figure we can see another block named "switch logic", which uses the sensed output current and output voltage

values and generates the gate drive signals, $PWMH$ and $PWML$, which in order to set the output voltage at the desired value. Gate drivers, named "U1" and "U2" in the figure, take the gate drive signals as an input and turns the MOSFETs, S_T and S_B on or off.

Each switching cycle starts with the rising edge of the CLK signal. After the rising edge of the CLK, the bottom MOSFET S_B is turned off and the top MOSFET S_T is turned on, in a hard switched manner, hence the current in the inductor L_O will start rising. This current will be continuously sensed and will be compared to an internal current reference, which is variably set by the "switch logic" block in order to make the sensed output voltage value as close to the desired output voltage as possible. Once the sensed current value hits the set current reference, the top MOSFET S_T will be turned off and the bottom MOSFET S_B will be turned on until the beginning of next switching cycle.

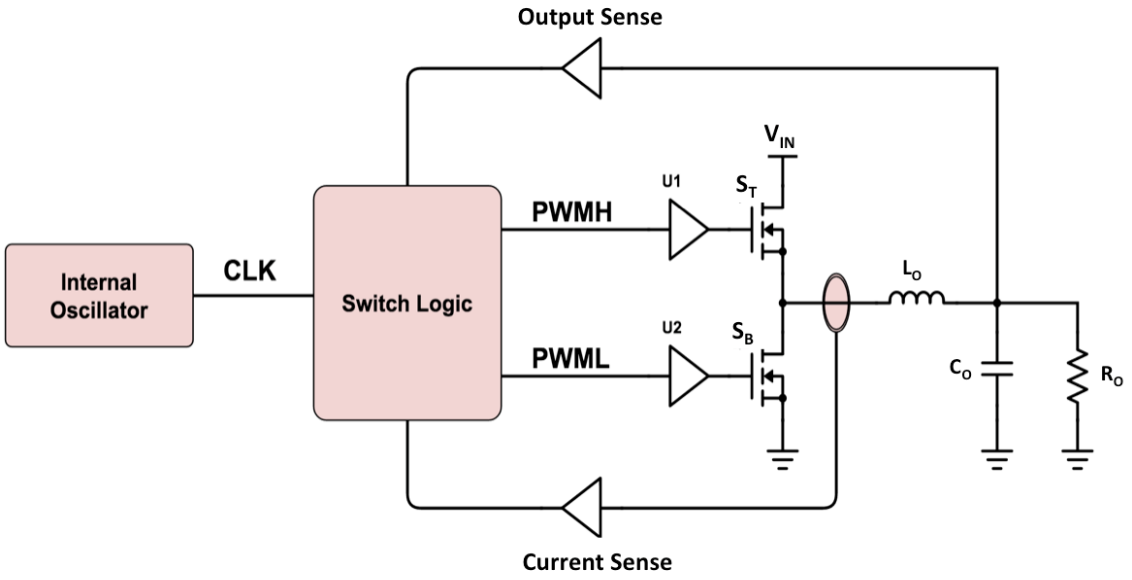

Figure 3-6: Simplified closed loop control of a synchronous buck converter

Our control algorithm that accomplishes zero voltage turn on of the top MOSFET S_T can be seen in Figure 3-7. Because of the reverse current problem mentioned in sections 3.5 and 3.6, we decided to use the bottom helper MOSFET, S_{HB}, in a diode connected configuration, which significantly simplified the control algorithm. When we designed the control algorithm, we realized that we can still use the same "switch

logic" block without any changes. We can use the signal $PWMH$ that is already generated in the "switch logic" block as a turn on signal for our helper circuitry and we can turn on the main top MOSFET S_T with another signal, $PWMH\_ZVS$, that is only generated after the switch node voltage is pulled to the level of the input voltage source, V_{IN}. Thanks to this design choice, our zero voltage switching helper circuitry becomes a modular block, that could be easily added to any hard switched buck converter IC without any changes to the other parts of the IC.

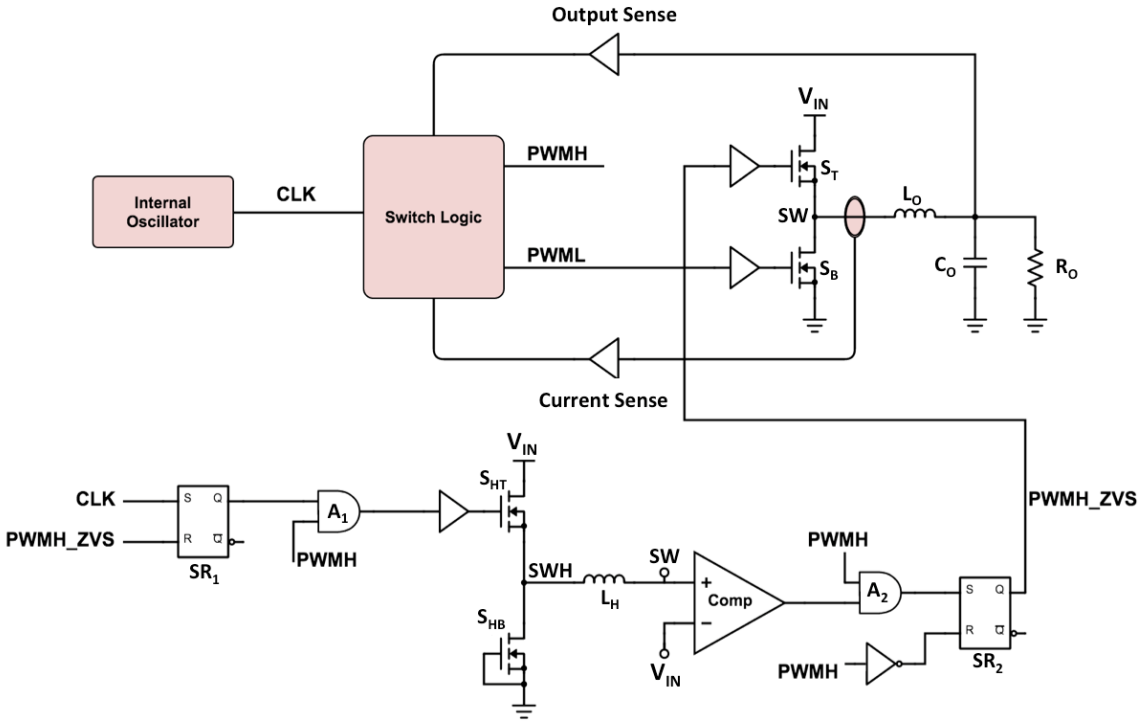

Figure 3-7: Control algorithm that accomplishes zero voltage switching of S_T

The detailed working principle of our control algorithm and how it accomplishes the zero voltage turn on of the top MOSFET, S_T, is explained through the steps below:

1-) With the rising edge of clock signal, CLK, the main bottom MOSFET gate drive signal, $PWML$, will transition from high to low, $PWMH$ will transition from low to high and the output of the "SR latch SR_1" will be set.

2-) When $PWMH$ transitions from low to high, the output of the "and gate A1" will also transition from low to high, turning on the helper top MOSFET, S_{HT}.

3-) After S_{HT} is turned on, the current in the helper inductor L_H will start rising and after this current exceeds the current in the output inductor L_O, the voltage on the switch node SW will start increasing.

4-) The "comparator $Comp$" compares the switch node voltage V_{SW} to the input voltage V_{IN}. When V_{SW} exceeds V_{IN}, the output of this comparator will become high, meaning that the main top MOSFET S_T can be turned on with zero voltage switching.

5-) Once the comparator output becomes high, the output of the "and gate A_2 will transition from low to high and the output of the "SR latch SR_2" will be set. The output of this SR latch is a signal named $PWMH\_ZVS$, which is the new turn on signal for the main top MOSFET, S_T.

6-) The same $PWMH\_ZVS$ signal which turns on the main top MOSFET will reset the output of the "SR latch SR_1" and the output of the "and gate A1" will transition from high to low, turning off the helper top MOSFET, S_{HT}.

7-) As the helper top MOSFET is turned off, the current in the helper inductor L_H will commute to the diode connected helper bottom MOSFET, S_{HB} and will eventually become zero due to the voltage difference between nodes SW and SWH.

With the help of this control algorithm, we designed a closed loop controlled version of our zero voltage switching buck converter on the $0.35\mu m$ BiCMOS process node. However, due to the delays in the control loop, the turn on and turn off timing of the MOSFETs were not as precise as the open loop controlled version and this caused a reduction in the efficiency benefits of the new topology as explained in the next section.

3.7 Results

After determining the optimal helper MOSFET sizes of $S_{HT} = 22000\mu m$, $S_{HB} = 5500\mu m$ and the optimal helper inductor size of $L_H = 20nH$, we used the $0.35\mu m$ BiCMOS process node to run full chip simulations of the open loop and closed loop controlled versions of our proposed zero voltage switching topology. We compared

the overall power dissipation values from these simulations to our benchmark LT8697 IC. The results of the comparison are shown in Figure 3-8 and Figure 3-9 below. In these simulations we used the bottom helper MOSFET, S_{HB}, in a diode connected configuration since this reduced the reverse current problem and had a greater efficiency benefit. For the closed loop controlled version of our topology we used the control algorithm described in the previous section.

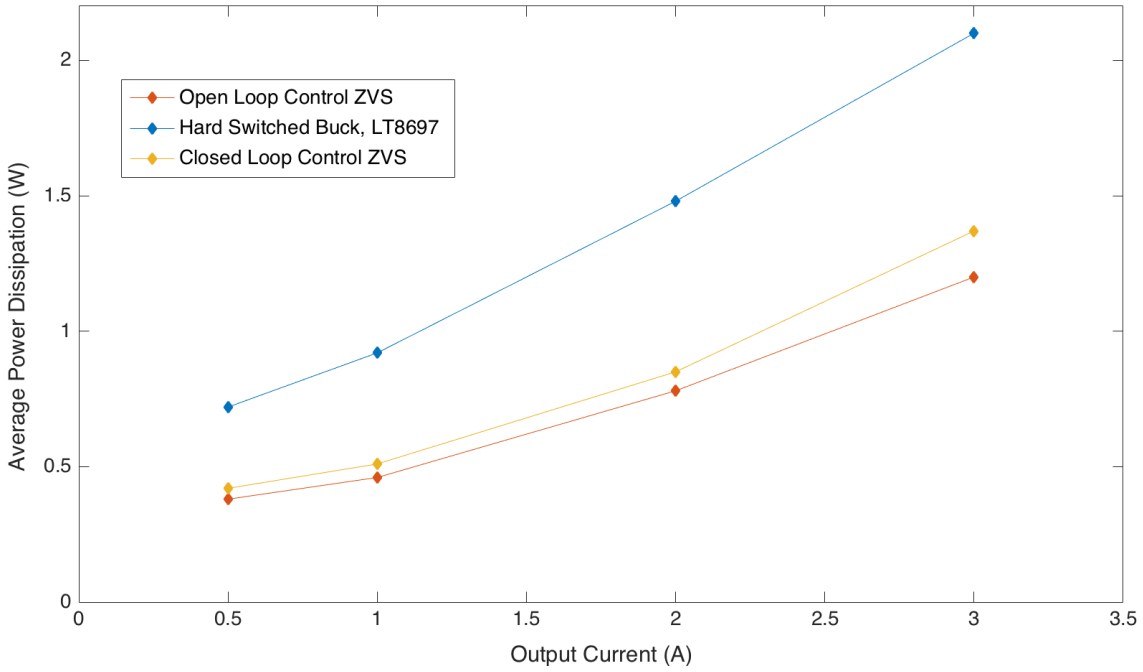

Figure 3-8: Comparison of overall power dissipation at varying output currents, for $V_{IN} = 15V$, $V_{OUT} = 5V$, $f_{SW} = 8MHz$

Figure 3-8 shows the overall power dissipation for the different configurations as the output current I_{OUT} is varied. We chose $V_{IN} = 15V$ and $V_{OUT} = 5V$ as the DC operating point, since this is a typical application for automotive applications of the LT8697 IC. We chose the switching frequency to be $f_{SW} = 8MHz$, since we wanted to highlight the benefits of zero voltage switching at higher frequencies. The results indicate that our proposed topology performs significantly better than LT8697 at all output current levels at this higher frequency. At the highest output current level, $I_{OUT} = 3A$, the open loop controlled version of our topology had a power dissipation of $P_{diss} = 1.2W$, which is a 43% reduction compared to the $P_{diss} = 2.11W$ power dissipation of the hard switched LT8697. On the other hand, the closed loop controlled

version of our topology had slightly more dissipation ($P_{diss} = 1.37W$) compared to the open loop controlled version, due to propagation delays in the control circuitry which made the timing of the gate drive signals less precise. However, despite these delays and imprecise timing, the closed loop controlled version of our topology still had a much better efficiency compared to the LT8697.

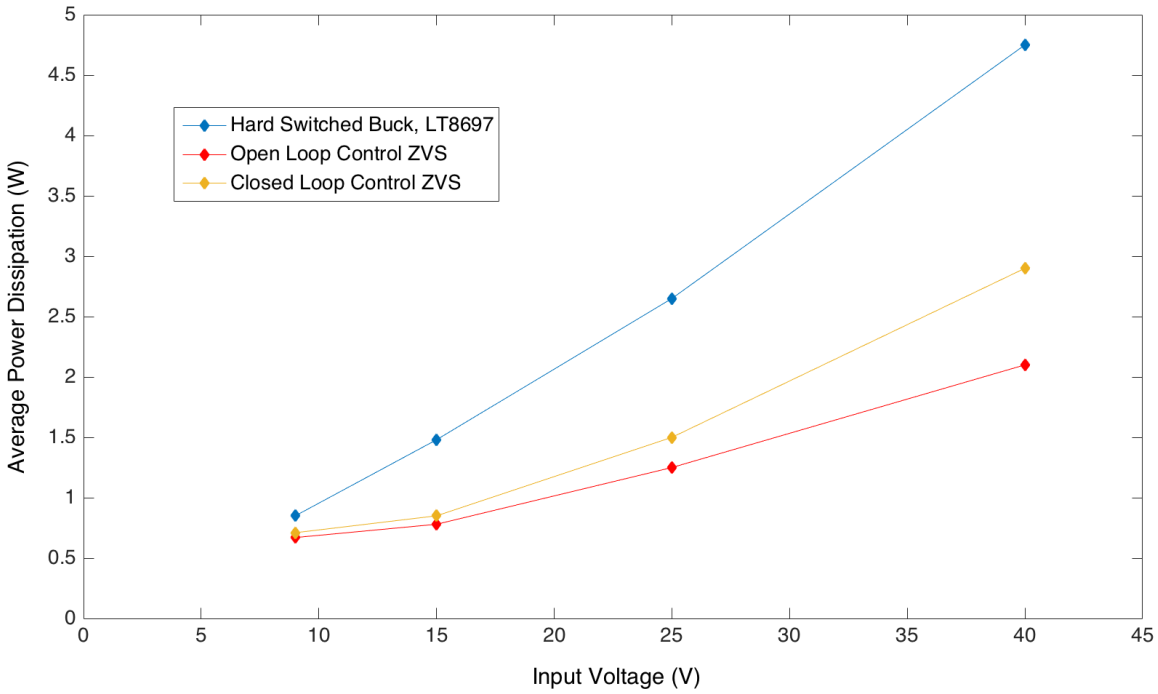

Figure 3-9: Comparison of overall power dissipation at varying input voltages, for $V_{OUT} = 5V$, $I_{OUT} = 2A$, $f_{SW} = 8MHz$

Figure 3-9 above shows a comparison of the overall power dissipation as the input voltage V_{IN} was varied. We chose $I_{OUT} = 2A$ and $V_{OUT} = 5V$ as the DC operating point, since this is a typical automotive application for the LT8697 IC. Although the efficiency benefits of our proposed topology is relatively small when the input voltage V_{IN} is less than $10V$, as the input voltage is increased, the advantage of zero voltage switching becomes more clear. This is due to the fact that the turn on loss of the main top MOSFET in a hard switched buck converter is given by $P_{top_{turnon}} = V_{IN} * I_{OUT} * (t_1 + t_2)/2$ (from Section 2.2), and so as V_{IN} is increased, this turn on loss dominates over the conduction losses.

At the highest input voltage level, $V_{IN} = 40V$, power dissipation of our benchmark

LT8697 IC is $P_{diss} = 4.75W$, which means the overall efficiency of the converter will be around 68% and more importantly the temperature increase on the die will prevent the LT8697 from operating at this high frequency of $f_{SW} = 8MHz$. This is because the junction to ambient thermal resistance of the LT8697 package is $\theta_{JA} = 46°C/W$ and a power dissipation of $P_{diss} = 4.75W$ would cause a temperature increase of $\Delta T = P_{diss} * \theta_{JA} = 218°C$ on the die compared to the ambient temperature. Due to these thermal issues, the maximum switching frequency of the LT8697 is limited to $f_{SW}(max) = 2.25MHz$.

On the other hand, at $V_{IN} = 40V$, the power dissipation of the open loop controlled zero voltage switching topology will be $P_{diss} = 2.14W$ and the power dissipation of the closed loop controlled version will be $P_{diss} = 2.84W$. Given the $\theta_{JA} = 46°C/W$, the thermal resistance of the LT8697 package, these power dissipation values would correspond to a temperature increase of $\Delta T_{OL} = 98°C$ and $\Delta T_{CL} = 130°C$, for open loop and closed loop controlled ZVS buck converters respectively. The actual manufactured ZVS IC would need to have closed loop control and with an ambient to junction temperature increase of $\Delta T_{CL} = 130°C$ it would still be impossible to operate this ZVS buck converter at $f_{SW}(max) = 8MHz$. However, if this IC is packaged with flipchip technology, rather than a wire bound package as it is currently, then the ambient to junction thermal resistance of the LT8697 package would be significantly reduced and increasing the switching frequency to $f_{SW} = 8MHz$ would be possible.

Chapter 4

Reducing the Gate Drive Losses with a Helper Circuit

4.1 Concept

Part of the frequency dependent losses in a synchronous buck converter is the gate drive loss as explained in Section 2.6. As shown in table 2.1, the gate drive losses become a larger proportion of the overall frequency dependent losses as the input voltage V_{IN} is reduced. Therefore it is necessary to reduce these gate drive losses, if we would like to limit the frequency dependent losses to a certain level so that that the switching frequency of the buck converter can be increased further.

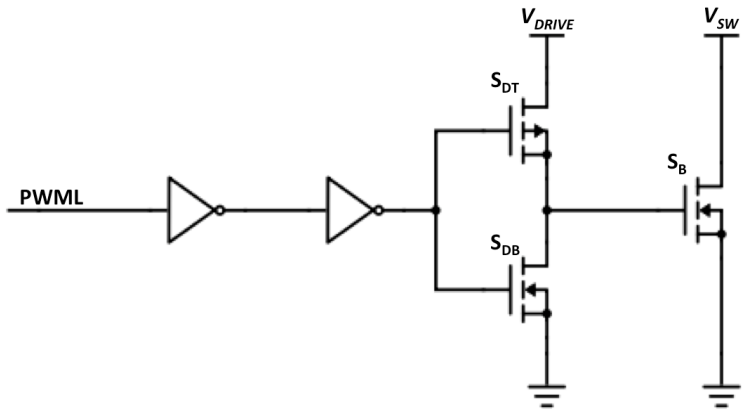

Figure 4-1: A simplified schematic of the hard switched gate driver

Figure 4-1 shows a simplified schematic of the hard switched gate driver that is used to drive the bottom MOSFET in the synchronous buck converter LT8697 IC. It is a chain of inverters with progressively increasing MOSFET sizes to quickly drive the larger capacitance in the next stage. Although not shown here, the gate driver for the top MOSFET can also be simplified as a chain of inverters, with an addition of the bootstrap circuitry to generate a switch node referenced power supply. In this gate drive topology, each of the inverters will generate some power loss due to the charging and discharging of the input capacitance of the next stage. However the input capacitance of these inverters are very small compared to the gate to source capacitance, C_{GS} of the main bottom MOSFET S_B, thus most of the gate drive losses happen in the last stage.

In order to turn on S_B, its gate to source capacitance, C_{GS_B} has to be charged to the gate drive voltage (around $3V$), which will happen when the top gate drive MOSFET, S_{DT}, is turned on and connects the gate of S_B to the gate drive power source, V_{DRIVE}. The amount of charge that is pulled from V_{DRIVE} will be equal to $Q_{GS_B} = C_{GS_B} * V_{DRIVE}$, and the amount of energy that is pulled from V_{DRIVE} will be $E_{DRIVE} = Q_{GS_B} * V_{DRIVE} = C_{GS_B} * {V_{DRIVE}}^2$. However, only half of this energy ($\frac{1}{2} * C_{GS_B} * {V_{DRIVE}}^2$) will be stored in the gate to source capacitance of the bottom MOSFET, whereas the other half will be dissipated through the on resistance ($R_{DS,DT}$) of S_{DT}, and the gate resistance (R_{G_B}) of S_B.

In order to turn off S_B, its gate to source capacitance, C_{GS_B}, needs to be discharged to the ground, which will happen when the bottom gate drive MOSFET, S_{DB}, is turned on and connects the gate of S_B to ground. This time all of the energy stored in C_{GS_B} (which is equal to $\frac{1}{2} * C_{GS_B} * {V_{DRIVE}}^2$) will be dissipated through the on resistance ($R_{DS,DB}$) of S_{DB}, and the gate resistance (R_{G_B}) of S_B.

Due to this resistive power dissipation during the charging and discharging of C_{GS_B}, the total gate drive loss in the bottom MOSFET will be $E_{LOSS_B} = C_{GS_B} * {V_{DRIVE}}^2$ and similarly the total gate drive loss in the top MOSFET will be $E_{LOSS_T} = C_{GS_T} * {V_{DRIVE}}^2$, during each switching cycle. The total gate drive power dissipation will be $P_{DISS} = f_{SW} * (C_{GS_T} + C_{GS_B}) * {V_{DRIVE}}^2$, where f_{SW} is the switching frequency.

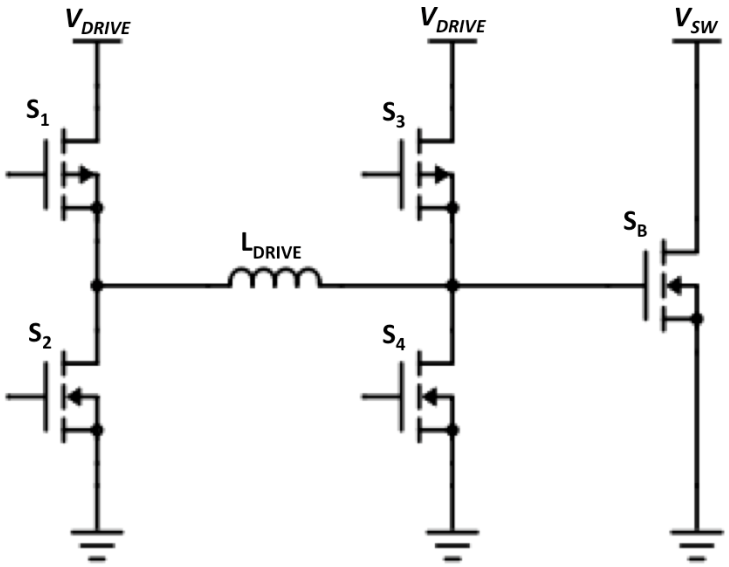

Figure 4-2: Proposed gate driver topology for reducing the gate drive losses

In order to reduce these gate drive losses, we decided to use a resonant gate drive topology with energy recovery, similar to the ones explored in [1], [2], [8], [17]. A simplified schematic of this topology is shown in Figure 4-2. By storing some portion of the excessive energy in an inductor, L_{DRIVE} and recovering this stored energy back to the gate drive power supply, V_{DRIVE}, this topology achieves a better efficiency compared to the nominal hard switched gate drive topology. The working principle of this topology is described below.

Sequence of Events During an Efficient Turn on of S_B

1- Initially, S_4 is on and the gate voltage of S_B is held at the ground level. This means the right side of L_{DRIVE} is at the ground level. Then, S_4 is turned off and S_1 is turned on connecting the left side of L_{DRIVE} to V_{DRIVE}. Because the gate capacitance of S_B is discharged, the voltage difference across L_{DRIVE} (initially equal to V_{DRIVE}) will induce a current in this inductor.

2- The current induced in L_{DRIVE} will charge up the gate of S_B until it becomes equal to V_{DRIVE}, meaning it is fully turned on. At this point we turn off S_1.

3- Now that S_B is turned on, we can recover the excess energy stored in L_{DRIVE}. This energy is a portion of the $\frac{1}{2} * C_{GS_B} * {V_{DRIVE}}^2$ that was dissipated during S_B's turn on in the hard switched topology. To recover that energy back to the source, we

turn on S_2 and S_3 which gives the inductor current a path to flow back into V_{DRIVE}.

4- When the current in L_{DRIVE} reduces to 0 this means all of the energy stored in this inductor is recovered and we can turn off S_2. We still keep S_3 on to hold the gate voltage of S_B at the V_{DRIVE} level.

Sequence of Events During an Efficient Turn off of S_B

1- Initially, S_3 is on and the gate voltage of S_B is held at the V_{DRIVE} level. This means that the right side of L_{DRIVE} is at the V_{DRIVE} level. Then, S_3 is turned off and S_2 is turned on connecting the left side of L_{DRIVE} to the ground. The voltage difference across L_{DRIVE} (initially equal to $-V_{DRIVE}$) will induce a current in this inductor.

2- The current induced in L_{DRIVE} will discharge the gate of S_B until it becomes equal to ground, meaning it is fully turned off. At this point we turn off S_2.

3- Now that S_B is turned off, we can recover the excess energy stored in L_{DRIVE}. This energy is a portion of the $\frac{1}{2} * C_{GS_B} * {V_{DRIVE}}^2$ that was dissipated during S_B's turn off in the hard switched topology. To recover that energy back to the source, we turn on S_1 and S_4 which gives the inductor current a path to flow back into V_{DRIVE}.

4- When the current in L_{DRIVE} reduces to 0 this means all of the energy stored in this inductor is recovered and we can turn off S_1. We still keep S_4 on to hold the gate voltage of S_B at the ground level.

This resonant gate drive topology has the potential to significantly reduce the gate drive losses depending on the sizing of the inductor. The approximate value of energy dissipated during S_B's turn on and turn off is given by [1]:

$$E_{DISS} = \frac{R_{TOTAL}}{R_{TOTAL}+Z_O} * C_{GS_B} * {V_{DRIVE}}^2 \tag{4.1}$$

Here $Z_O = \sqrt{\frac{L_{DRIVE}}{C_{GS_B}}}$ is the characteristic impedance of the resonant circuit formed by S_B's gate to source capacitance, C_{GS_B}, and the inductor L_{DRIVE}. $R_{TOTAL} = R_{G_B} + R_L + R_{DS,ON}$ is the total gate drive resistance, which includes S_B's gate resistance, L_{DRIVE}'s parasitic resistance and the on resistance of driver MOSFETs, S_1 and S_2. Notice, it is assumed that S_1 and S_2 are sized as $R_{DS,ON_{S1}} = R_{DS,ON_{S2}} = R_{DS,ON}$.

Table 4.1: Power dissipation of the high side and low side resonant gate drivers for varying L_{DRIVE} values, at $V_{IN} = 15V$, $V_{OUT} = 5V$, $I_{OUT} = 2A$

L_{DRIVE}	$1nH$	$2nH$	$4nH$	$8nH$
Power Dissipation of the High Side Gate Driver	$42mW$	$37mW$	$31mW$	$29mW$
Power Dissipation of the Low Side Gate Driver	$46mW$	$40mW$	$35mW$	$32mW$

4.2 Results

In order to determine the efficiency benefits of the proposed resonant gate driver topology in the $0.35\mu m$ BiCMOS process node, we did a full-chip simulation of a modified LT8697 with the resonant gate drive topology and compared the results to the LT8697's regular hard switched gate drive topology as a benchmark. For a fair comparison, we used resonant gate drive MOSFETs with the same width as the hard switched gate drive MOSFETs, such that $W_{S_1} = W_{S_{DT}}$ and $W_{S_2} = W_{S_{DB}}$. The results of the simulation for the resonant gate drive topology are summarized in Table 4.1 below. We used the DC operating point $V_{IN} = 15V$, $V_{OUT} = 5V$, $I_{OUT} = 2A$, since this is a typical application of the LT8697 and we used the switching frequency $f_{SW} = 8MHz$. At this operating point, the power dissipation of the hard switched low side gate driver is equal to $P_{DISS,GDL} = 101mW$ and the power dissipation of the hard switched low side gate driver is equal to $P_{DISS,GDH} = 60mW$. We can see that even using a small inductor value of $L_{DRIVE} = 1nH$, reduces the total gate drive power dissipation by 45%, from $161mW$ to $88mW$.

From Table 4.1, we can see that as the inductor value L_{DRIVE} is increased from $1nH$ to $8nH$, the resonant gate drive topology becomes more efficient. This is an expected result, according to Equation 4.1, which gives the approximate power dissipation for the resonant gate drive topology. However, it should be noted that increasing the inductor value comes with a cost trade-off, since these small valued inductors will need to be integrated inside the IC package. As the inductor gets larger, it will require more space and copper to generate on a flip-chip substrate. Chip integration is explained in the next chapter.

Chapter 5

Integration of Inductors into an IC Package

The optimal helper inductor value chosen for the zero voltage switching buck converter is $L_H = 20nH$ (Section 3.3) and the minimum inductor value required for an efficient resonant gate drive circuitry is $L_{DRIVE} = 1nH$ (Section 4.2). If external inductors are required for L_H and L_{DRIVE}, it will make the buck converter IC less desirable for customers who want to use it in their application. These three external inductors (one helper inductor and two resonant gate drive inductors) will not only increase the bill of materials of the application circuit, but they will also make the PCB design significantly more complex. That is because the PCB traces connecting these external inductors to the IC pins need to be kept short or else the parasitic inductance on these traces can be very large (10's of nanoHenries) [18], which creates a large difference between the desired inductance value and the actual inductance value. Therefore, it is necessary to integrate these three inductors inside the IC package.

A common approach for integrating power inductors inside the IC package is fabricating them on the silicon die [14], [15], [16]. However, these methods usually require a significant change of the common CMOS or BiCMOS fabrication methods and would not be suitable for the $0.35\mu m$ BiCMOS process node. We therefore explored a different approach to integrate these inductors inside the IC package by utilizing the flip-chip packaging technology to accomplish the integration without any

change in the silicon fabrication technology.

5.1 Spiral Inductor on a Flip-Chip Substrate

One method for integrating the inductors inside the IC package is fabricating spiral inductors on the substrate of the flip-chip package. For example, the helper inductor, $L_H = 20nH$, can be layed out as a square shaped spiral inductor as shown in Figure 5-1. One constraint here is to make the outer diameter of the inductor, d_{out}, as small as possible so that it does not use much space on the substrate. Another constraint is to make the overall copper length as short as possible, so that the parasitic resistance of the inductor would be small.

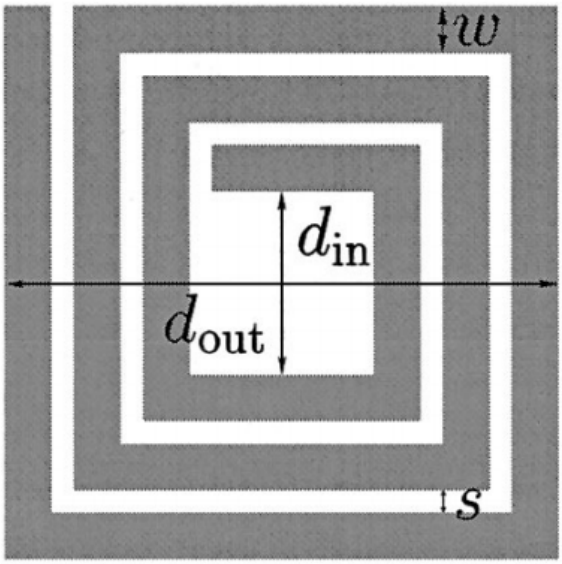

Figure 5-1: A square shaped spiral inductor with three turns ($N_{turn} = 3$)

Using an online spiral inductor calculation tool [6], we designed a spiral inductor with $N_{turn} = 3$, $d_{out} = 1.2mm$, $w = 30\mu m$ and $s = 30\mu m$, which yielded an inductance value of $L_H = 19.95nH$ with monomial fit approximation [9]. Using LT8697's $3mm$ by $5mm$ package size as a reference, this inductor would only use around 10% of the package surface. The thickness of the copper traces on the flip-chip substrate is $t_{cu} = 35\mu m$, which means the DC resistance of this inductor would be $R_{DC} = \rho_{cu} * l/(t_{cu} * w) = 0.207\Omega$, where $\rho_{cu} = 1.68 * 10^{-8}\Omega m$ is the resistivity of copper and

$l = 12.57mm$ is the total length of the traces that form this inductor. If a smaller DC resistance is desired, multiple layers of the substrate stack can be utilized. For example, if we use all 4 layers to fabricate the spiral inductor, the total DC resistance would be significantly reduced to, $R_{DC} = 0.052\Omega$.

5.2 Soldering Chip Inductor Inside the Package

Another alternative for integrating the inductors inside the IC package is soldering an off-the-shelf surface mount inductor on the substrate of the flip-chip package. Most recent flip-chip ICs from Linear Technology have 0402 sized SMD capacitors integrated inside the package using this method, which greatly reduces the parasitic effects of the traces that are present when the capacitors are placed outside the IC package. Similarly, 0402 sized SMD inductor PFL1005 (REF13) from CoilCraft would be an ideal choice for integrating the helper inductor inside the package. This inductor has an inductance value of $L_H = 18nH$ and a DC resistance of $R_{DC} = 0.032\Omega$. One other constraint of this method is that, the height of the inductor should be very low such that it would not increase the overall height of the IC package. The chosen inductor, PFL1005, has a maximum height of $t_{PFL1005} = 0.71mm$, which is smaller then most of the IC package heights, including LT8697's height, $t_{LT8697} = 0.75mm$.

5.3 Comparison of The Two Methods

We can see that both of these methods would be viable for integrating the helper inductor $L_H = 20nH$ inside the IC package. However, for the resonant gate drive inductors, L_{DRIVE}, it is difficult to find off-the-shelf chip inductors with an inductance of only a couple of nanoHenries. Therefore implementing the two resonant gate drive inductors as spiral inductors on the package would be a better choice.

The helper inductor, L_H, only conducts current during a short period of time in each cycle, right before and after the main top MOSFET, S_T, is turned on. However, there will still be some power dissipation during this short period that needs to be

considered. It is clear that the chip inductor PFL1005's DC power dissipation will be lower, since it has a smaller DC resistance. However, on the other hand, the composite core of PFL1005 will generate significant AC core losses, that will be larger than the AC losses of the air core spiral inductor.

One last thing to consider when comparing these two methods is the EMI radiated by the pulsating currents in these inductors. In this aspect, the off-the-shelf chip inductors will be more advantageous, since they will contain most of the magnetic field in their core, whereas the air cored spiral inductors will almost act as an antenna radiating EM waves caused by the pulsating current. Since these EMI effects would significantly affect the working of the buck converter located right next to it, implementing the helper inductor L_H as an off-the-shelf chip inductor would be a better choice.

Chapter 6

Conclusion

A zero voltage switching helper circuit to reduce the turn on losses of the high side MOSFET in synchronous buck converter ICs was explored. Sizes of the two helper MOSFETs and the helper inductor were optimized using simulation results. A closed control algorithm to control the helper circuit's operation was designed and implemented. The problem of reverse current problem in the helper inductor is investigated thoroughly and a solution to reduce the reverse current is proposed.

A zero voltage switching buck converter with the proposed helper circuit is implemented in $0.35\mu m$ BiCMOS process node, by modifying the power stage of synchronous buck converter IC, LT8697. Full-chip simulations of this new buck converter were ran and the results are compared to our benchmark IC, LT8697. Simulation results revealed that at 8MHz switching frequency the total power dissipation in a buck converter could be reduced by more than 40% with the help of this topology, which would eliminate the thermal limitations to clock the commercial buck converter ICs at this high frequency. This topology could also be implemented with in a process node with smaller features, which would increase the efficiency by reducing the propagation delays in the control circuitry. Furthermore, a similar helper circuit could be utilized to reduce the turn on losses of the low side MOSFET in synchronous boost converter ICs.

A resonant gate drive topology was designed and tested in $0.35\mu m$ BiCMOS process node. With a resonant inductor value of $8nH$, the simulation results showed a

62% reduction compared to the hard switched gate driver. This resonant gate drive topology could be also implemented in other switching power converters, if a high switching frequency is desired.

Both the zero voltage switching helper circuit and the resonant gate drive circuit requires the addition of inductors. Two different methods, both of which utilized the flip-chip packaging technology, were proposed to integrate these additional inductors inside the IC package and the merits of these two methods were compared.

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