Two-Dimensional Material based Layer Transfer of Thin Film Devices

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Abstract

The semiconductor industry has mainly centered around silicon-based technology due to its associated cost advantage stemming from the abundance of the element and well-established fabrication infrastructures. However, there exists a plethora of compound semiconductors that offer unique electronic properties that can enable high performance devices superior to silicon for a wide range of device applications. Unfortunately, compound semiconductors industries have seen limited adoption in industries except in occasions where silicon-based technology cannot be used. This is mainly due to the rarity and high production costs associated with alternative semiconductor wafers. There have been many proposals that attempt to reduce the cost of production of these compound semiconductors by offering reusable wafers. In this scheme, the wafer is used as a platform to fabricate devices, the device layer is subsequently exfoliated from the wafer via a layer transfer allowing for the wafer to be re-used for continuous fabrication of thin-film devices. However, the layer transfer techniques that have been proposed so far often damages the wafer substrate, limiting their reusability and adding additional costs for surface refurbishment processes. This thesis proposes a novel layer transfer process, termed two-dimensional material based layer transfer (2DLT), which prepares thin-film semiconductors by facile mechanical exfoliation to yield a clean wafer surface requiring minimal surface treatment. Moreover, this process can be applied to a wide range of material systems, suggesting a universal layer transfer process.

The 2DLT process discussed in this work is enabled by a novel concept of semiconductor epitaxy, termed remote epitaxy. This thesis explores remote epitaxial growth of compound semiconductors on a graphene coated substrates and exfoliation of epitaxial films grown on graphene. Due to the atomic-thickness of graphene and weak van der Waals interaction on the surface of graphene, semiconductor adatoms on the surface of graphene can be made to register to the substrate for growth of single crystalline semiconductor films. In addition, the weak interactions at the interface of graphene provides a well-defined cleavage plane for facile mechanical exfoliation of the epitaxial film. This thesis investigates the conditions and mechanisms that facilitate remote epitaxy in order to identify the fabrication processes that enable 2DLT for compound semiconductors. The materials grown via remote epitaxy exhibited comparable properties to that of epitaxial films grown by conventional homoepitaxy, this has been demonstrated by fabrication of thin-film light emitting diodes (LEDs) and metal-semiconductor field-effect transistors (MESFETs), the results of which are presented in this work.

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Chapter 1

Introduction

1.1 Motivation

Various semiconductors offer unique traits that make them ideal candidates for certain electronic devices, in particular compound semiconductor materials of the III-V and III-N groups offer many unique advantages compared to silicon in the field of integrated circuits (ICs), photovoltaics (PV) and optoelectronics. However, the semiconductor industry has fixated on silicon-based technology due to its associated cost advantage. The abundance of the element and well-established fabrication infrastructures for high throughput processing continue to promote its prolific use. Compared to silicon, many compound semiconductors offer higher carrier mobility, which translates to faster performance of electronic devices. In the PV and optoelectronic industries, the indirect bandgap of silicon results in poor absorption/emission of light requiring device thicknesses within hundred microns for complete absorption of sunlight as opposed to few microns needed for direct bandgap materials. Centering new device technologies on silicon limits the possibilities for novel, more efficient devices. Unfortunately, the rarity and high production costs associated with alternative semiconductor wafers are major deterrents for their adoption into industries.

The extreme cost of compound semiconductor wafers has pushed for the development of thin film exfoliation techniques to transfer the device layer from the wafer in order for the substrate to be re-used for processing. Notable layer transfer techniques include epitaxial lift-off (ELO)[1], laser lift-off (LLO)[2] and mechanical lift-off via controlled spalling[3]. Both ELO and LLO techniques are only applicable to specific material systems, ELO process is applicable to GaAs devices that have been epitaxially grown on an AlAs sacrificial layer, the device stack is made to come in contact with HF

acid which demonstrates high etch selectivity for AlAs in order to free the GaAs thin film with minimal damage to the GaAs film and GaAs substrate. The LLO process applies to GaN devices grown epitaxially on a AlO_3 substrates, taking advantage of the AlO_3 substrate's transparency to ultra-violet (UV) radiation, a pulsed UV laser irradiates the device stack from the backside of the substrate to locally heat and cause chemical decomposition at the AlO_3/GaN interface to release the GaN thin film. While these techniques present a well-controlled process that preserves the functional integrity of the device layer, they are time consuming and roughens the released interface after the process. The controlled spalling process is a much faster process that can be applied to many material systems, but it requires digital control of mechanical fracture dynamics in order to ensure uniform spalling depth and parallel crack trajectory to exfoliate the device layer. The device layer is deposited with metallic stressor film with uniform stress, an adhesive handle layer is applied to the stressor film to initiate the crack from the wafer edge to release the film. The techniques listed above have proven to prepare thin film devices without degradation in functionality compared to devices anchored onto its substrate; however, all processes lead to mechanical degradation of the substrate's surface requiring surface polishing treatment by chemical mechanical polishing (CMP) to re-prepare the wafer for the next epitaxial growth. CMP adds additional costs to the process and slowly depletes the substrate, thereby limiting the number of times the substrate can be re-used until the substrate breaks. In the figure below, data adapted from NREL's cost analysis of manufacturing GaAs solar cells based on ELO process shows that the levelized cost of energy ($\$/W_{p(DC)}$) (LCOE) as a function of reuse eventually falls down to a constant fixed cost associated with CMP process [4]. In order to promote the use of GaAs based solar cells in industries and displace silicon based technology for far more efficient devices, a LCOE less than 1$/W must be realized.

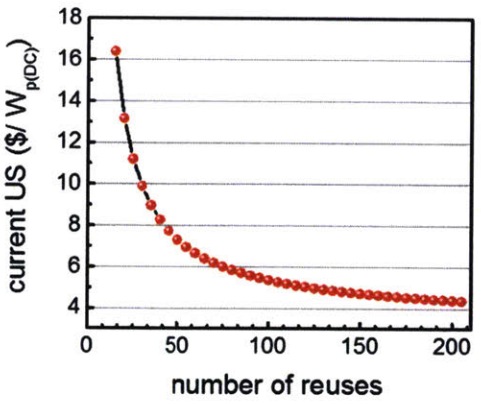


Figure 1-1: NREL cost analysis of ELO processing. From [4].

The ideal layer transfer process is one that can be universally applied to any material systems without the need for additional surface treatment. The work by Kim et al. [5] suggests the application of graphene for a two dimensional material based layer transfer (2DLT) technique that may pave the way for a universal layer transfer process. In this work 4H-SiC(0001) wafer was annealed at high temperature in low pressure under ambient gas to sublimate silicon from the surface of the wafer, carbon atoms re-arrange to form single-crystalline graphene in a self-limiting process on the surface of the SiC wafer. GaN was subsequently grown epitaxially atop the monolayer-graphene to yield single-crystalline GaN. Despite the large lattice mismatch of ~23% between graphene and GaN, a single crystalline GaN film was grown with defect density as low as 4E8 cm^{-2}. The findings suggest graphene may have a high tolerance for lattice mismatch to allow single-crystalline films to form on top of graphene. Moreover, due to the weak van der Waals interaction between the surface of graphene and the GaN film, the film was precisely exfoliated from the graphene-GaN interface using a metal stressor film akin to the controlled spalling technique. The fracture initiates from the weakly bonded interface allowing for well controlled fracture depth without the formation of spalling defects. A smooth surface is presented upon exfoliation allowing for the substrate to be re-used with minimal surface treatment. This proposed layer transfer process using van der Waals surfaces present a foothold

for fabricating thin films for general material systems with significant cost advantage associated with wafer re-usability.

The body of work presented in the thesis is mainly divided into two parts which explore van der Waals epitaxy for general materials systems and demonstration of a novel layer transfer process for general material systems. All results prepared in the thesis are derived as discussed in the work published by Kim et al. The first section will explore the mechanism by which single-crystalline material can form atop graphene and explore the reasoning and implications for achieving single crystalline growth on graphene. The second section will explore layer transfer process utilizing graphene in order to fabricate thin film devices based on compound semiconductors.

Chapter 2

Background

2.1 Van der Waals Epitaxy

In conventional heteroepitaxy, the growing overlayer lattice bonds with the substrate by covalent interactions, the overlayer crystal lattice must share a similar lattice with the substrate in order for pseudomorphic growth to proceed, whereby the film adopts the crystal structure and lattice parameter of the substrate. A lattice misfit as small as 0.1% can cause strain energy to build up rapidly in the film as the thickness grows, until eventually it becomes more energetically favorable to form misfit dislocations, thereby introducing crystalline defects in the film that are detrimental to device performance. Due to this limitation of strict lattice matching requirement in heteroepitaxy, van der Waals epitaxy (vdWE) was proposed by Koma et al. [6] to grow heterostructures with large lattice mismatch on top of van der Waals surfaces. VdWE studies the growth of crystalline layers on substrates without the formation of covalent bonds at the interface of the latticed mismatched systems, these materials are weakly connected by van der Waals interactions that would permit complete strain relaxation during epitaxial growth[5-14]. Two-dimensional (2D) materials such as graphene, h-BN, MoS_2, etc... or quasi-2D materials such as transition metal chalcogenides (TMDCs) present strong covalent interactions in-plane of the crystalline layers but present weak van der Waals interaction out-of-plane of the layers. It has been demonstrated that single crystalline films grown to the first atomic layer via vdWE present a fully relaxed state with its own unique lattice constant[15]. In an extended application, vdWE was investigated in the growth of non-planar nanostructures on top of a passivated surface, such as the growth of ZnO nanowires on the surface of muscovite mica substrate[16]. Through vdWE, strain-

relaxed single-crystalline growth can also be achieved for semiconductors despite the presence of dangling bonds on the surface of the crystalline structure. While this was shown in a limited case for nano-pillar type structures, it was found that the surface of a 2D-material does not interact with the crystalline overlayers, allowing for strain-relaxed incommensurate growth of semiconductors. The passivation of dangling bonds in semiconductor growths during vdWE can enable strain-relaxed growth of incommensurate overlayer films, but the potential for strain-relaxed incommensurate epitaxial films have been impeded by other difficulties in growth of planar semiconductors on 2D materials. The surface of 2D material present low adsorption binding energy for semiconductor adatoms, the poor wettability of semiconductors leads to Volmer-Weber (island) growth which often converges to poor quality epitaxial films. Conventional heteroepitaxy often proceeds by Frank-Van der Merwe (layer-by-layer) growth in order to achieve high quality epitaxial films, which requires high wettability of the substrate. Despite the low binding energy of the surface of graphene, Kim et al.[5] have demonstrated successful GaN growth on graphene with root mean square (rms) roughness of 3 Å. Epitaxy of GaN proceeds via Volmer-Weber growth in the initiation stage to form islands for nucleation seeds, after initiation GaN can planarize given suitable growth conditions, thus despite the poor adsorption of GaN adatoms, planar growth of strain-relaxed incommensurate layers can be realized for this material system. However, in order to extend vdWE for general material systems, the wettability issue of semiconductor adatoms on the 2D material surface must be addressed. Despite its potential for strain-relaxed heteroepitaxial growth, the poor wettability of 2D material surface is an impediment to achieving planar single-crystalline epitaxial films.

2.1.1 Van der Waals interaction on monolayer graphene

The interaction of graphene surface and semiconductor substrate have also been investigated in the work by Rafiee et al. [17] In this experiment the wetting behavior of water was studied on various substrates coated with graphene, including an oxide-etched silicon wafer. Contact angle studies and molecular dynamics simulations show that contact angle of water droplets increases to that of bulk graphite as more layers of graphene is added at the interface of water and substrate. It was found that monolayer graphene is wetting-transparent on copper, gold and silicon substrate. Due to the relatively long-range, van der Waals interaction between water molecules and the substrate, the presence of monolayer graphene barely screens this interaction resulting in the wetting-transparency of graphene. However, the case is different for interactions between water molecules and an oxide substrate. Water and glass have an inherent short range interaction characterized by hydrogen bonding, thus the presence of monolayer graphene is enough to disrupt this short-range interaction. The findings of this work entertains the idea that overlayer film on monolayer graphene may also interact with the substrate below graphene. Due to the atom-thick dimension of 2D materials, the presence of a monolayer 2D film may not completely passivate the dangling bonds of the overlayer film. While conventional heteroepitaxial growth is characterized by short-range, covalent bonding interactions between the substrate and epitaxial layer, there exists a critical range where short-range interactions can still occur[9, 17, 18].

2.2 Simulation

In order to investigate the role of the underlying substrate below 2D materials during vdWE, density functional theory (DFT) computation was performed to ascertain the electronic interaction between the substrate and the overlayer, epitaxial film when a separation gap is introduced. In the

vdWE of GaN(0001) film on graphene-coated 4H-SiC(0001) substrate, both the SiC(0001) substrate and graphene present a hexagonal lattice, thus it is difficult to determine whether the crystallographic alignment is made with the graphene or the underlying substrate. In order to isolate this conflicting factor, a simulation model was made for a zincblende GaAs(001) substrate and GaAs(001) epitaxial film which have a cubic crystal lattice, distinguishable from the hexagonal lattice of graphene.

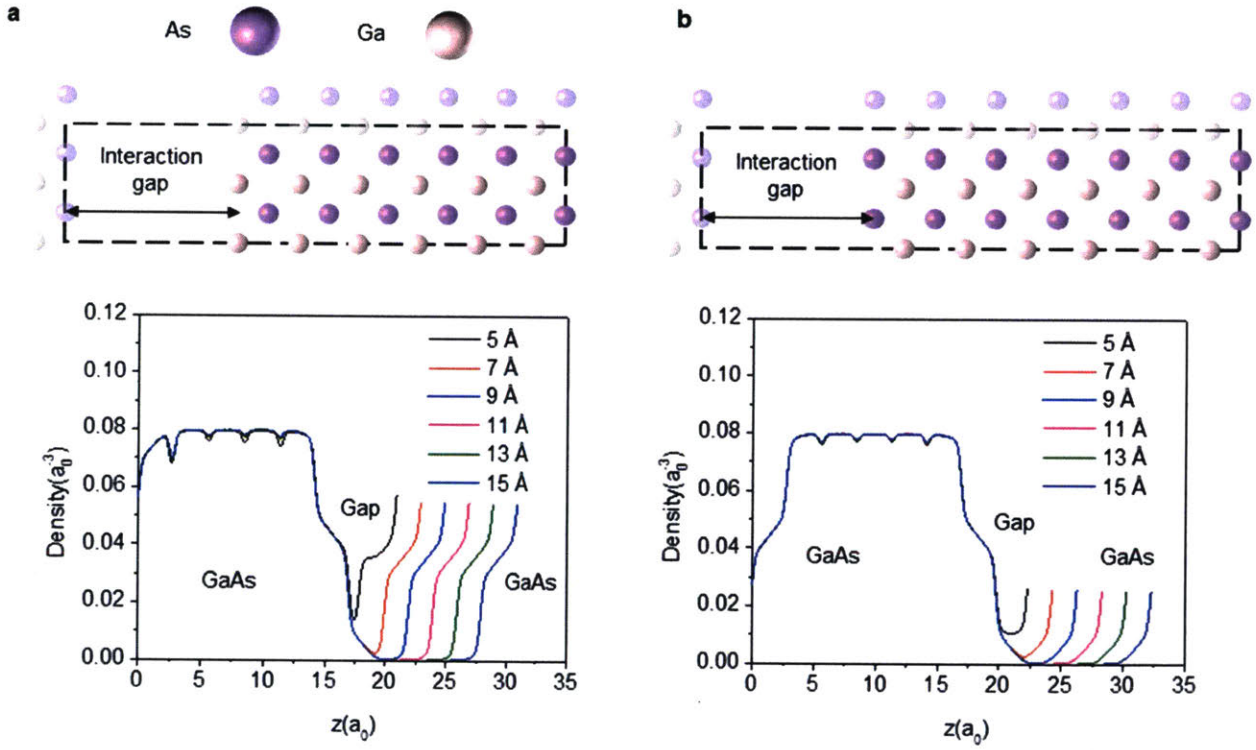
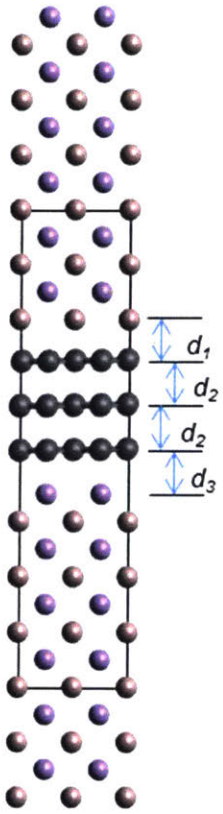


Figure 2-1: Substrate–epilayer remote interaction with different gaps created by different numbers of stacked graphene interlayers. a, b, Results of DFT calculations of averaged electron density along separated slabs of GaAs for As–Ga interaction (a) and As–As interaction (b). Periodic boundary conditions were imposed along the dashed lines of the simulation model (shown at top). From [19].

The DFT computations presented here were developed based on a simulation model by Babatunde Alawode with Professor Alexi Kolpak's group in the MIT Department of Mechanical Engineering. The computations were made using the plane-wave pseudopotential code as

implemented in Quantum Espresso[20]. In all calculations, all atoms (Ga, As) were relaxed, a k-point mesh of 4× 4× 1 was selected and convergence was achieved with 12 layers of GaAs(001) slab. For the local exchange correlation functional, the Perdew–Burke–Ernzerhof general gradient approximation was used[21]. The spacing between periodic images of the superstructure in the z direction was varied between 5 Å and 30 Å. The in-plane lattice constant was fixed to 1× 1 times the calculated lattice constant (5.63 Å) of bulk GaAs. An ideal case of a 1× 1 system was modelled for the simulation as surface reconstructions do not significantly affect the behavior of the surface at the interface[22, 23]. The relaxation calculations were set to complete when the forces on the relaxed layers were less than 1× 10−3 a.u. The simulation employed a wavefunction and charge density kinetic energy cut-offs of 50 Ry and 350 Ry, respectively. Figure 2-1a and Figure 2-1b illustrates the simulation model of a GaAs slab for As-Ga interaction and As-As interaction respectively, periodic boundary conditions were imposed along the dashed lines. The GaAs(001) slabs were made to interact with themselves with an imposed interaction gap between the top of the slab and bottom of the slab. As-terminated GaAs(001) slabs were selected for the computation model since epitaxial growth of GaAs requires an As pre-layer termination on the substrate. While Ga atoms are typically made to bond with the As pre-layer in homoepitaxial growth, this interaction could not be assumed with the presence of graphene at the interface of the GaAs(001) substrate and GaAs(001) epitaxial film. The interaction gap in the model was varied at incrementing distances as shown in the plots of Figure 2-1a and Figure 2-1b. Planar averaged electron density was calculated for each interaction gap to illustrate the electronic interaction of the Ga-initiated and As-initiated epitaxial film with the As-terminated substrate. In both models, electronic charge density diminishes when the interaction gap is increased beyond 9Å. This suggests that interaction between slabs can exists below a 9 Å gap, below this critical distance the

substrate may interact with the incoming adatoms to allow for homoepitaxial growth at a remote distance.



Terminations	Separation
Ga – As	$d_1 + (n-1)d_2 + d_3$
As – As	$2d_3 + (n-1)d_2$

$d_1 = 1.90$ Å $\quad d_2 = 3.15$ Å $\quad d_3 = 3.14$ Å

Graphene layers	Ga – As (Å)	As – As (Å)
1	5.04	6.28
2	8.19	9.44
3	11.35	12.59

Figure 2-2: Natural slab separation with n graphene layers present between GaAs slabs. The natural separation distance between graphene–As d_3 is 3.14 Å, the graphene–graphene distance d_2 is 3.15 Å and the graphene–Ga distance d_1 is 1.9 Å. Separation induced by graphene interlayers is shown in the table for both Ga–As and As–As terminated cases. From [19].

The natural separation that can be induced by inserting *n* graphene layers in GaAs–graphene–GaAs heterostructure are presented in the table of Figure 2-2. This suggests that the maximum number of graphene layers that can be inserted in the 9 Å critical gap is two layers for As-terminated and Ga-initiated slabs, and one layer for As-terminated and As-initiated slabs. In reality, interaction between GaAs slabs may be damped by the vertical van der Waals force exerted by interlayer graphene, though it is about an order of magnitude weaker than that of covalent

interactions. Therefore, the true charge interaction gap between the substrate and epitaxial layer through which electronic interaction occur may be less than that estimated from the calculations.

2.3 Experiment

To verify the simulation results, a growth study was designed in order to investigate the remote epitaxial growth through a gap induced by graphene interlayers. Initial investigation utilized graphene created using chemical vapor deposition (CVD) processes and transferred it to a host substrate for investigation. As referenced in the simulation, a GaAs(001) substrate wafer was selected as the crystal seed substrate for remote epitaxy. Graphene made from CVD processes was transferred on top based a process designed by Professor Jing Kong's group in the Department of Electrical Engineering and Computer Science at MIT.

2.3.1 Graphene synthesis and transfer

Preparation and transfer of graphene samples were prepared by Yi Song from Professor Jing Kong's group. CVD graphene was synthesized on a Cu foil in a low pressure CVD process. Cu foils were initially annealed in a quartz tube furnace at 1000°C for 30 min under 10 sccm of H_2 flow. Using CH_4 as the carbon source, graphene was grown under 4 sccm CH_4 and 70 sccm of H_2 for 30 min at 1.90 Torr. Growth of graphene is terminated by a self-limiting processing, yielding a monolayer of polycrystalline graphene. Poly(methyl-methacrylate) (PMMA) was spin-cast onto graphene coated Cu foil and baked at 80°C for 10 min. PMMA was applied onto graphene as a handle layer to adhere to graphene during the Cu etching process. The Cu foil was dissolved in $FeCl_3$ copper etchant solution for 15 min. During the etching process, the graphene-PMMA stack was let to float on the surface of the solution held by its surface tension. In a parallel process, the GaAs host substrate was etched in dilute 10% $HCl_{(aq)}$ solution to remove the oxide from the surface.

The native oxide removal was marked by the hydrophobicity of the surface. The graphene-PMMA stack was then transferred onto the oxide-etched GaAs substrate and dried at 80°C for 10 min and subsequently placed in acetone to dissolve the PMMA handle layer.

2.3.2 Epitaxial growth GaAs

Epitaxial growth of GaAs was performed using a close coupled showerhead MOCVD reactor. For GaAs growth, AsH_3 and trimethylgallium (TMGa) were used as the precursors for As and Ga sources, respectively. For all growths the precursors were flown using N_2 carrier gas, the total reactor pressure was set to 100 Torr and temperature ramp steps proceed under a group V overpressure with no group III precursors. First, the growth proceeded at a relatively low temperature of 450°C at 100 Torr for a short time to encourage the nucleation of GaAs islands on graphene to initiate the growth. The reactor temperature was then ramped to 650°C for normal growth of GaAs.

2.3.3 Characterization

In order to quantify the crystalline structure of the grown epitaxial layers of GaAs on CVD graphene, high resolution X-ray diffraction (HRXRD) was employed. An ω-2θ scan was run on the GaAs epitaxial film. A scanning electron microscopy (SEM) images of the samples were also taken to observe the morphology of the grown epitaxial films. Based on the DFT simulation, remote interaction between the epitaxial film and substrate is anticipated to be lost for gap spacing larger than two layers of graphene. Thus, epitaxial growth of GaAs was conducted on monolayer, bilayer and tetralayer graphene. Bilayer and tetralayer graphene were prepared by repeating the CVD graphene transfer process for each additional layer of graphene on a GaAs(001) substrate. Epitaxial GaAs films were grown to an anticipated thickness of 200 nm.

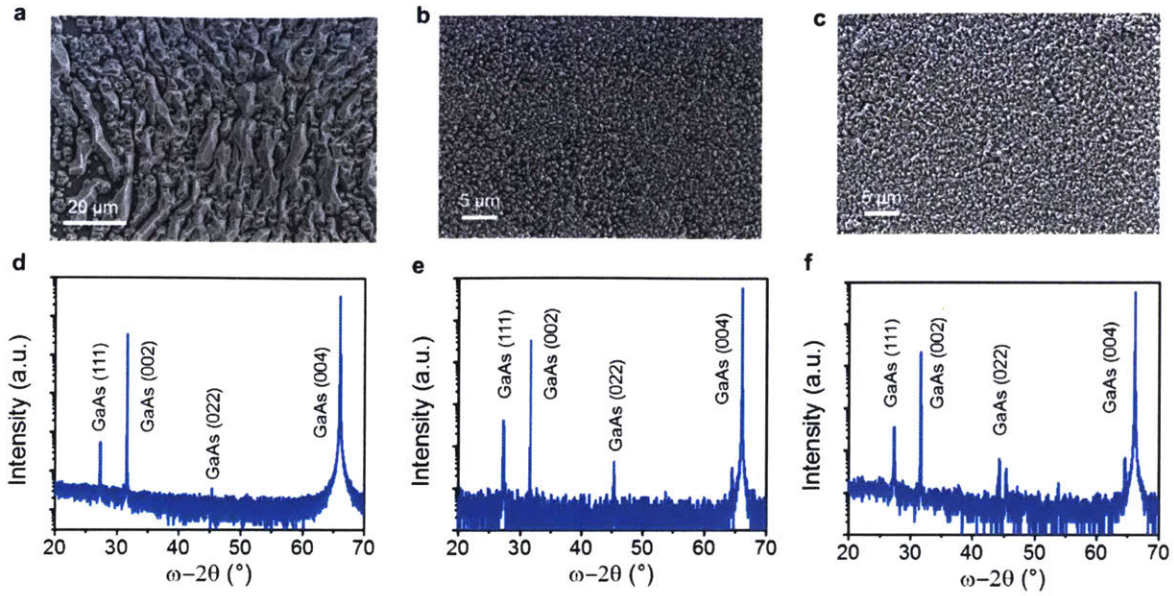


Figure 2-3: Characterization of GaAs grown on monolayer and bilayer graphene. a, b, c, SEM images of GaAs epitaxial films on monolayer, bilayer and tetralayer graphene transferred on GaAs(001) substrate, respectively. d, e, f, HRXRD ω-2θ scans of GaAs epitaxial films on monolayer, bilayer and tetralayer CVD graphene respectively. From [19].

Epitaxial GaAs on monolayer graphene reveal relatively weak diffraction peak from the (111) crystallographic plane compared to the (004) plane of the GaAs(001) substrate (Figure 2-3d). The presence of bilayer and tetralayer graphene on the substrate yields relatively stronger peaks for the (111) and (022) planes (Figure 2-3e,f). The peaks unassociated with the (001) planes, including (002) and (004), indicates the presence of polycrystalline film growth. These are visually observed by the SEM images as well, which show polycrystalline grains on bilayer and tetralayer graphene, but larger faceted nucleation islands on monolayer graphene. Epitaxial growth on bilayer graphene shows no discernible crystal faceting, indicating randomly oriented crystal planes which attribute to the polycrystalline nature of the film. The faceted nucleation islands on the monolayer graphene indicate the islands are single-crystalline in nature. However, the GaAs(001) planes in the epitaxial film cannot be characterized distinctly from the GaAs(001) planes of the substrate through HRXRD as the (002) and (004) diffraction peaks from the substrate harshly overshadows that of

the epitaxial film. In order to distinctly characterize the crystalline structure of the epitaxial layer from the substrate, an exfoliation process was devised to separate the epitaxial layer. The layer transfer process and characterization of the epitaxial layer is discussed in the next chapter.

Chapter 3

Two dimensional material based layer transfer (2DLT)

3.1 Exfoliation of epitaxial films

A similar transfer process as stated in the work by Kim et al. [5] was employed to exfoliate epitaxial films that have been grown on top of graphene. Since the graphene at the interface of the substrate and epitaxial film present weak van der Waals interactions between the epitaxial layer and substrate, the 2DLT process was expected to yield similar results to the GaN exfoliation experiment. Using a thermal evaporator, 100 nm of Ti were deposited on the surface of sample to form the adhesion layer, high stressed Ni was subsequently deposited using plasma sputtering. The Ni was deposited to a few microns in thickness to yield an internal stress within 500 MPa–1 GPa. The stress of the Ni film was initially calibrated on a Si wafer, measured based on the induced wafer curvature of the Si wafer. The Ni stressor film induces high strain in the GaAs film, the van der Waals bonding at the interface is broken when the strain energy built in the film exceeds the energy of the bonding. By applying a highly stressed Ni film below the threshold for spontaneous exfoliation, less external force is required to separate the epitaxial film from the substrate. To complete the exfoliation, an adhesive tape was applied on the Ni film and peeled off from the substrate, the Ni film was exfoliated along with the GaAs epitaxial film.

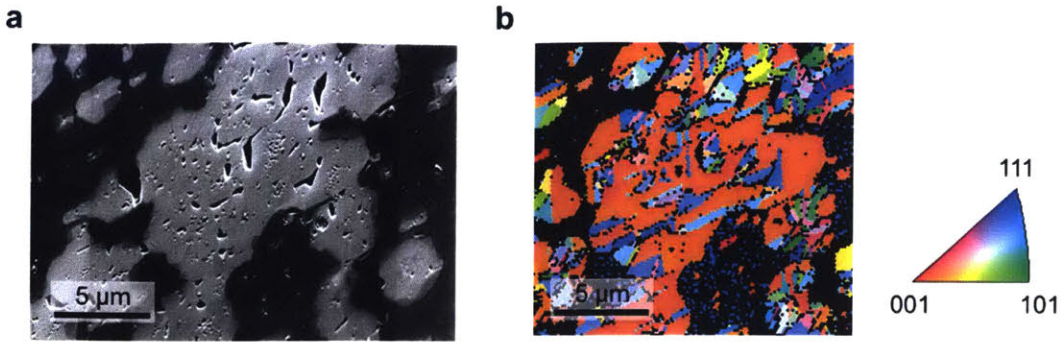


Figure 3-1: GaAs epitaxial film exfoliated on Ni film. a, SEM image of exfoliated side of GaAs epitaxial film. b, EBSD map of exfoliated film. On the right is the inverse pole figure colour triangle for crystallographic orientations. From [19].

The weak bonding interaction between the graphene coated substrate and epitaxial film offered a well-define cleavage plane for a clean exfoliation. In contrast to the rough topology on the top-face of the grown film as seen in Figure 2-3a, the smooth finish on the exfoliated side of the film enabled the use of electron backscatter diffraction (EBSD), for surface sensitive measurement of the sample crystallinity. The SEM image of the exfoliated face of the GaAs film in Figure 3-1a show dark regions attributed to the Ni film deposited during the exfoliation process. The EBSD map in Figure 3-1b show large domains of GaAs with (001) planes as labeled by the inverse pole figure (IPF) color triangle. This corresponds with the results in the HRXRD and TEM analysis which anticipated the dominant presence of GaAs(001) single-crystalline nucleation on monolayer graphene.

The domains of polycrystalline GaAs on monolayer graphene was attributed to the poor adhesion of monolayer graphene on the GaAs substrate. During the graphene transfer, process-induced adsorbates are expected to reside on the graphene surface and at the graphene-substrate interface [24, 25]. The presence of the adsorbates may unintentionally widen the interaction gap between the epitaxial layer and substrate beyond the critical gap, thereby losing the remote interaction. In order to remove residual material on graphene, such as PMMA, and promote

adhesion of graphene to the substrate, the stack was let to anneal in a quartz tube furnace at 350°C under H_2 for more than 30 min [26-28].

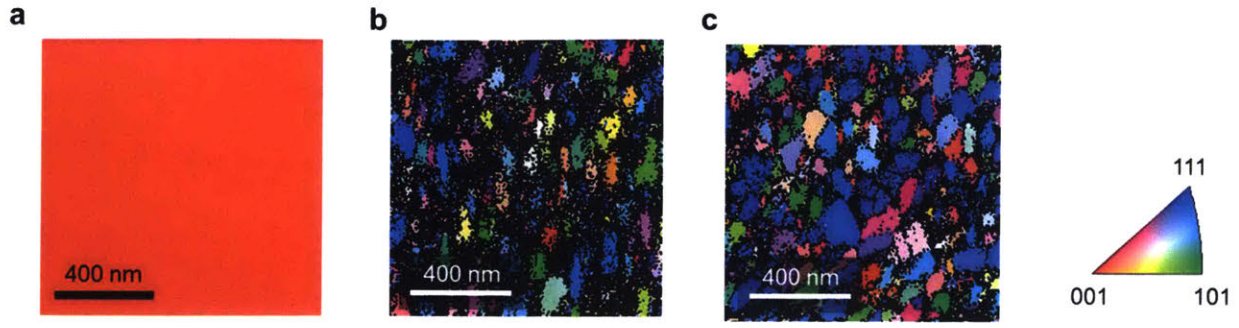


Figure 3-2: GaAs growth on annealed graphene. EBSD map of exfoliated GaAs film grown on monolayer (a), bilayer (b) and tetralayer graphene (c). IPF colour triangle on the right. From [19].

The H_2 annealing step made a marked improvement in the growth and exfoliation of the GaAs epitaxial film on monolayer graphene. The EBSD map in Figure 3-2a show a larger domain of GaAs(001) single crystals compared to the un-annealed sample. The graphene transfer process with annealing step was repeated for bilayer and tetralayer graphene transfer. Based on the EBSD maps (Figure 3-2b,c), growth of polycrystalline GaAs was observed for bilayer and tetralayer graphene, which verifies the calculation found in the DFT simulation and supports the HRXRD scans in Figure 2-3e, f which found large presence of polycrystalline crystals in the GaAs epitaxial film on bilayer and tetralayer graphene. As remote interaction is lost beyond one layer of graphene, the processing conditions during the graphene transfer become critical to minimize the spacing in order to achieve remote epitaxy at large scale.

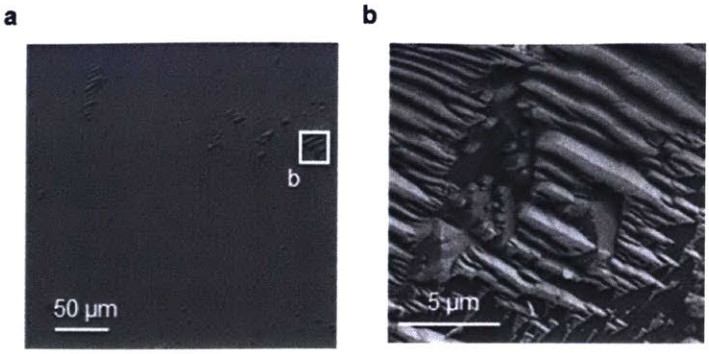


Figure 3-3: Plan-view SEM of exfoliated surface of GaAs. a, Smooth parts indicate release from graphene, and rough parts indicate spalling. b, Direct epitaxy of GaAs epitaxial layers on GaAs substrates causes jagged topology (spalling marks) upon exfoliation due to spalling. From [19].

Graphene is known to remain pristine during epitaxy without dissolving into substrates or epitaxial layers owing to its high thermal stability [5, 29, 30], thus all epitaxial materials investigated in this study were successfully exfoliated by Ti/Ni stressor films [5, 31]. Epitaxial layers failed to exfoliate when epitaxy was performed on a substrate with a graphene coating that had been pre-damaged by Ar plasma treatment. The smooth morphology of the exfoliated epitaxial layer surface suggests precise release from pristine graphene [5]. Rough spalling marks are observed in very limited areas originating from direct epitaxy on the substrate (Figure 3-3). If mechanical defects such as holes and cracks in graphene exist, they permit direct exposure of the GaAs(001) surface to adatoms, resulting in the direct binding of adatoms to the substrate. The defects can be addressed by improving the yield of graphene transfer.

3.1.1 Layer-resolved graphene transfer (LRGT)

To better improve the adhesion of graphene to the substrate, a dry transfer process was devised. The traditional transfer of CVD graphene onto the host substrate requires the graphene to make contact with an aqueous solution, thereby increasing the risk of residual adsorbates at the interface of graphene and substrate. By transitioning the process for dry conditions, the adhesion of

graphene to the substrate can be greatly improved. Using layer-resolved graphene transfer (LRGT), epitaxial graphene from SiC(0001) was exfoliated and directly transferred onto an oxide-etched GaAs substrate without the involvement of aqueous solutions [32].

Epitaxial graphene was prepared on a Si-face 4H-SiC(0001) wafer. Graphitization of SiC was performed at 1,575°C under ambient Ar for 1 hr to form monolayer graphene in a self-limiting process. The graphene was exfoliated using LRGT, in which a Ni stressor layer was deposited on epitaxial graphene and exfoliated from SiC using a thermally released tape. The tape was also used as the handling layer to transfer the graphene–Ni stack onto HCl-treated, oxide-etched GaAs substrates. The tape was removed by annealing above the release temperature of 90°C. The Ni stressor layer was then etched away in dilute acid.

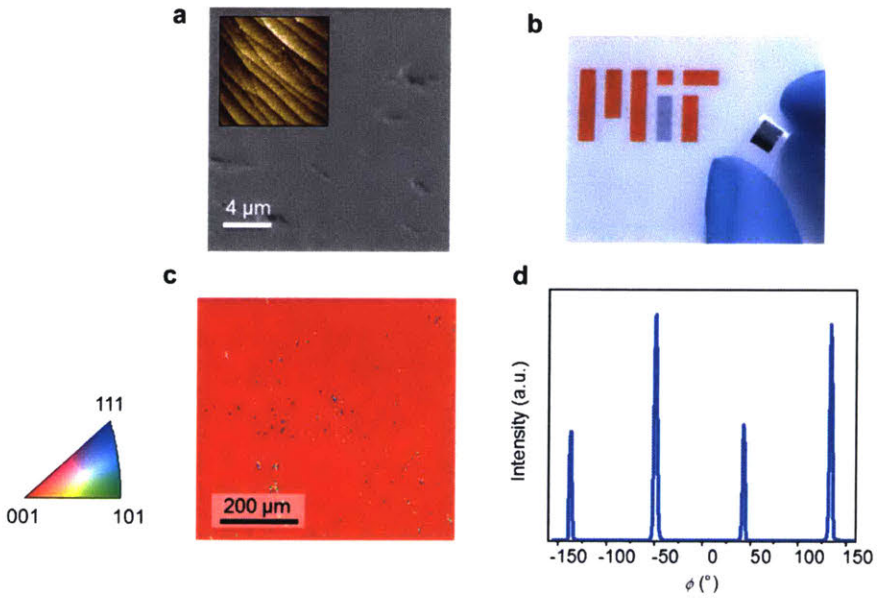


Figure 3-4: GaAs epitaxial film on epitaxial graphene transferred by LRGT. a, top-face of GaAs film after growth. Inset, 1 μm × 1 μm non-contact AFM scan. b, Macrograph of GaAs film on Ni adhered to adhesive tape. c, EBSD map of exfoliated GaAs. d, ϕ scan of GaAs(224) on exfoliated GaAs film. From [19].

Epitaxial growth of GaAs on graphene transferred by LRGT demonstrated enhanced wetting behavior and better coverage as shown in Figure 3-4a, growth artifacts are observed on the surface of the film caused by impingement of nucleation islands. The topology was characterized by non-contact atomic force microscopy (AFM), which revealed a rms surface roughness of 0.3 nm. Moreover, the formation of terraces, as observed in the AFM scan, imply that epitaxy proceeds via step flow growth, thus GaAs growth on graphene proceeds in the same manner as direct homoepitaxial growth after convergence of GaAs nucleation islands on graphene. The GaAs film was exfoliated using 2DLT process, revealing a large-area, specular finish on the exfoliated-face of the film (Figure 3-4b). EBSD map shows that the entire film is dominated by single-crystal GaAs(001) (Figure 3-4c). In order to verify that the epitaxial film is of single-domain, single-crystalline film, as opposed to multiple domains of azimuthially misoriented GaAs(001), a ϕ scan was conducted using HRXRD. The ϕ scan shows four-fold symmetry of diffraction peaks corresponding to GaAs(224) with 90° intervals, indicating that the GaAs grown on the GaAs(001) substrate through monolayer graphene is a single-crystalline zincblende phase without azimuthal rotations. The summation of these findings indicate that growth on monolayer graphene transferred by LRGT process is capable of growing large-scale, single-crystalline epitaxial films via remote epitaxy and exfoliated via 2DLT process. The LRGT process ensures a well-adhered graphene transfer without the need for annealing to yield single-crystalline growth via remote epitaxy. Though regardless of the transfer process and type of graphene, the study shows unequivocally that GaAs epitaxial films can be made to register with the GaAs substrate through monolayer graphene.

To observe the crystal structure of the epitaxial film in relation to the substrate, scanning transmission electron microscopy (STEM) and high resolution transmission electron microscopy

(HRTEM) were employed. TEM samples were prepared using focus ion beam (FIB) milling to cut out a cross-sectional slab of epitaxial GaAs on monolayer graphene in order to characterize the crystalline structure of the epitaxial film at the graphene interface. The TEM sample preparation and characterization were done by Jared M. Johnson from Professor Jinwoo Hwang's group in the Department of Material Science and Engineering at Ohio State University.

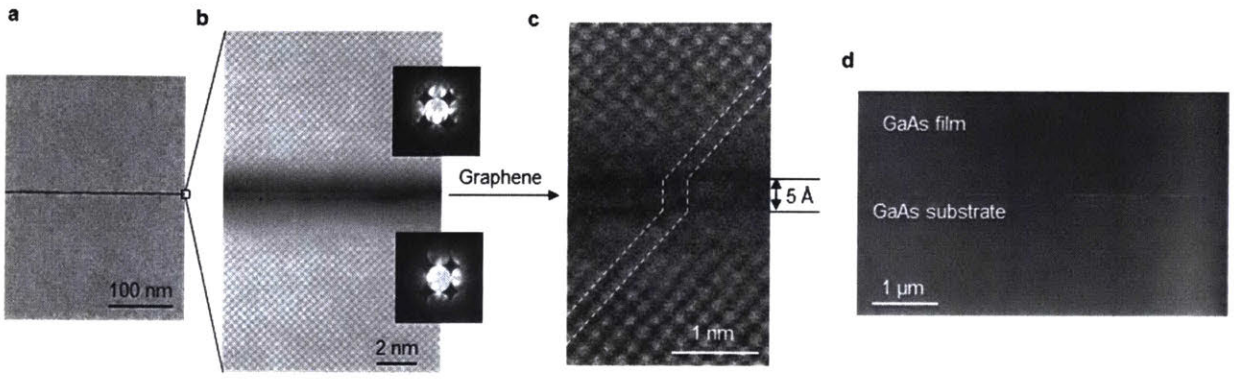


Figure 3-5: TEM characterization of epitaxial GaAs on monolayer graphene. a, STEM image of GaAs film near graphene interface. b, HRTEM image with convergent-beam electron diffraction patterns from the epilayer (top inset) and the substrate (bottom inset) showing identical zinc-blende (001) orientations. c, HRTEM image magnified near interface showing interaction gap induced by monolayer graphene. d, Low-angle annular dark field STEM image showing no dislocations. From [19].

The remote epitaxial alignment between the GaAs(001) epitaxial layer and GaAs(001) substrate was atomically resolved by performing cross-sectional scanning transmission electron microscopy (STEM). Figure 3-5a shows STEM image of the sample which was able to distinctly capture the epitaxial film at the graphene interface. Figure 3-5b, c shows HRTEM images at different magnifications which reveal that the GaAs(001) film is epitaxially aligned with the GaAs(001) substrate through the gap created by monolayer graphene. The measured gap between the GaAs epitaxial layer and the substrate is about 5 Å, which is below the critical gap calculated with DFT. Identical convergent beam electron diffraction patterns from the epitaxial layer and the substrate also confirm the epitaxial relationship. Figure 3-5d shows low-angle annular dark field

imaging of the GaAs–graphene–GaAs sample at low magnification in cross-sectional STEM which found no evidence for strain contrast at the substrate–epitaxial layer interface. The lack of strain in the epitaxial film implies that no dislocations are present, at least within the inspected area. While TEM inspection covered only a limited sample area, it confirms that remote homoepitaxial growth of GaAs can occur through flat graphene on GaAs substrates.

3.1.2 Thin film devices

In order to justify the application of these epitaxial thin-films fabricated through combination of remote epitaxy and 2DLT, optoelectronic characterizations and device fabrication was conducted on these epitaxial films.

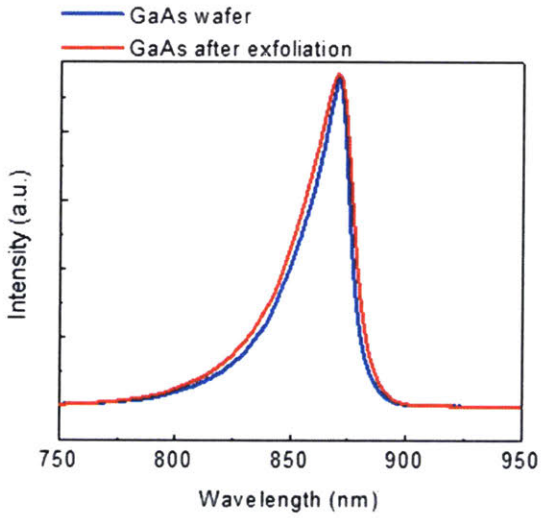


Figure 3-6: Steady-state room temperature photoluminescence spectra. Shown are steady-state photoluminescence spectra of GaAs substrate and exfoliated GaAs epitaxial layer grown by remote epitaxy. From [19].

Steady-state room temperature photoluminescence spectra of exfoliated GaAs, grown on graphene–GaAs substrates, are comparable to spectra recorded for GaAs wafers (Figure 3-6), indicating no degradation in material quality during growth and transfer processes.

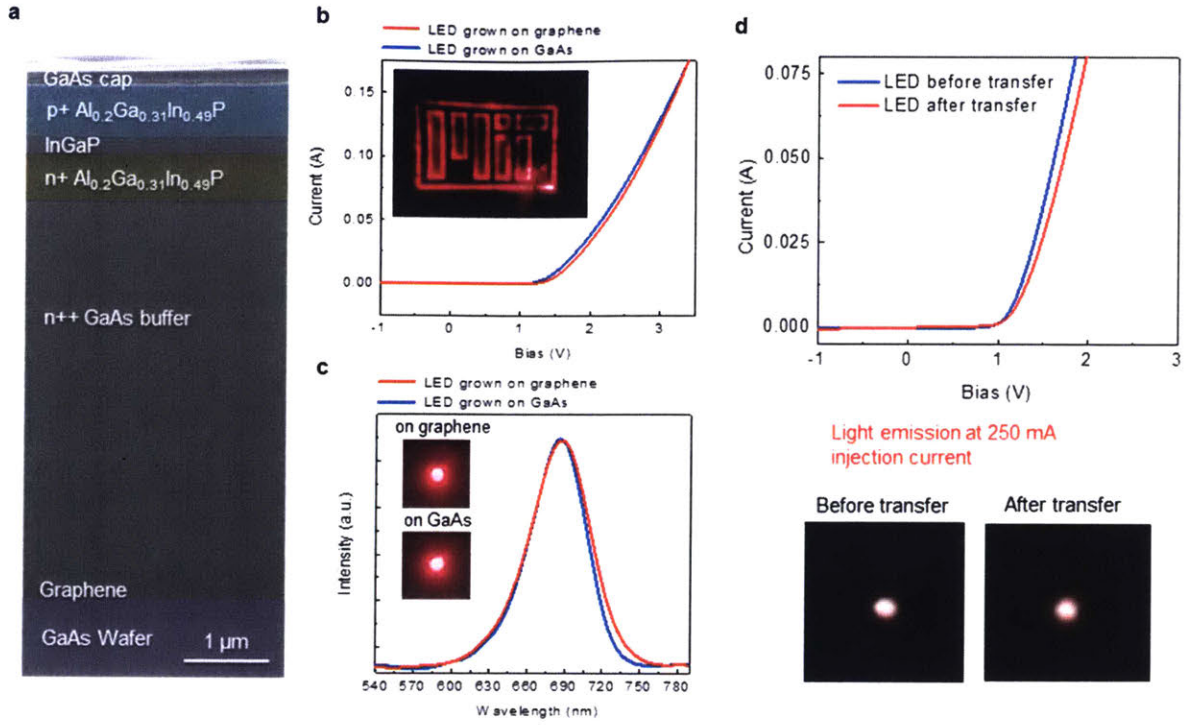


Figure 3-7: AlGaInP–GaInP double heterojunction LEDs on a graphene–GaAs substrate. a, Cross-sectional SEM image of heterojunction LEDs. b, I–V curves of LEDs grown on graphene–GaAs substrates and directly on GaAs. Inset, emitted red light from the LEDs grown on the graphene–GaAs substrate. c, Electroluminescence spectra of the LEDs grown on graphene–GaAs substrates and directly on GaAs, Inset, photographs of functioning LEDs grown on both substrates. d, I–V curves of LEDs grown on graphene–GaAs substrates before and after 2DLT process. Bottom, emitted red light of LED's before and after transfer. From [19].

Given the results, an AlGaInP–GaInP double heterojunction light-emitting diodes (LEDs) on graphene–GaAs substrates were grown. The LED device stack was grown on a 4 μm thick Si doped n-GaAs buffer layer in the MOCVD reactor, with 800 nm of n-AlGaInP, 100 nm of GaInP, 800 nm of Zn doped p-AlGaInP and 100 nm of p-GaAs as a capping layer. Si_2H_6 and dimethylzinc (DMZn) were used as precursors for Si and Zn dopants for n-type and p-type doping, respectively. Figure 3-7a reveals cross-sectional SEM of the grown heterojunction LEDs with each device layer artificially colored for distinction. After remote epitaxial growth of the device stack, the front contact is patterned by photolithography using an LOR 3A and SPR 220 bilayer photoresist

process. The metal contact was deposited in order of Pd(5 nm)/Ge(20 nm)/Au(100 nm) using e-beam evaporation. The 100 μm diameter contact pad is patterned at the center of the device. After the metal layer is lifted off, 200 μm × 200 μm mesas are defined by photolithography using SPR 220 and chemical etching using HCl:H3PO4 (3:1) solution. The LEDs are annealed for 1 hr at 200°C for ohmic contact formation. For 2DLT processed LEDs, 50 nm of titanium was deposited by thermal evaporation on the as-grown sample then nickel was sputter deposited to a thickness of 6 μm with argon plasma sputtering. Thermally released tape is applied on top of the metal stressor film and peeled to exfoliate the device stack from the graphene interface. For thin film transfer onto silicon, polydimethylsiloxane (PDMS) was spin-coated onto a Si(001) wafer at 2,000 rpm for 30 s, followed by baking at 80°C for 2 min. The exfoliated film is then placed on the PDMS and pressure is applied. The thermal tape holding the film is then removed by heating the entire structure on a hot plate at 125°C until the tape is thermally released. The bonded stack is left to cool at room temperature for 30 min. Nickel and titanium are removed by $FeCl_3$ solution (20% w/v) and dilute HF. After the film transfer, the same fabrication method is applied for the substrate-based LED described above. The devices exhibited *I–V* curves and turn-on voltages of 1.3 V that are comparable to those of LEDs directly grown on a bare GaAs substrate (Figure 3-7b inset illustrating red light emission from LEDs grown through remote epitaxy. Electroluminescence spectra of the LEDs grown on GaAs, either through remote epitaxy with graphene or conventionally without graphene, confirmed nearly identical performance, with very similar full-width at half-maxima of 45 ± 5 nm and peak electroluminescence intensities at an injection current of 250 mA (Figure 3-7c). The insets of Figure 3-7c show photographs of functioning LEDs grown on GaAs with and without graphene. The LEDs were subsequently exfoliated by 2DLT process and transferred to a Si substrate. Minimal degradation is observed in the LED performance as

indicated by the comparable *I–V* curves and light emission before and after the transfer (Figure 3-7d).

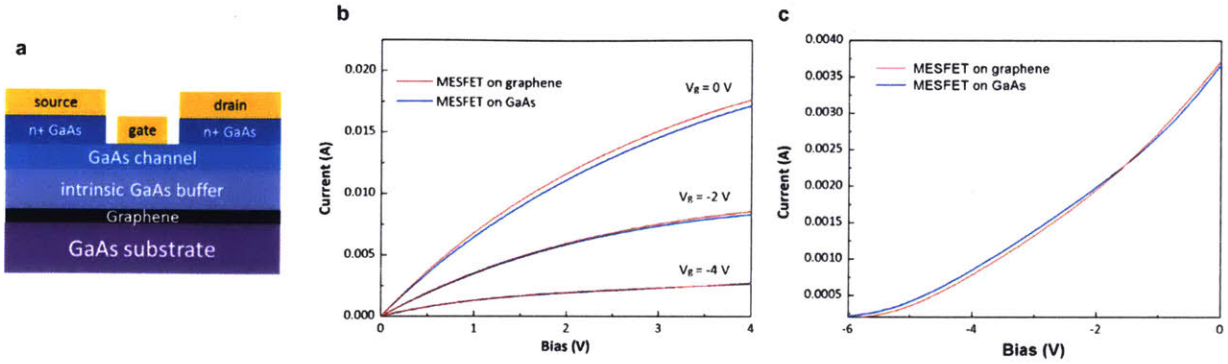


Figure 3-8: GaAs MESFET on a graphene-GaAs substrate: a, schematic illustration of MESFET stack. b, I_{DS} vs V_{DS} curves at varying gate voltages for MESFET grown on graphene-GaAs and MESFET grown directly on GaAs substrate. c, I_{DS} vs V_{Gs} curves at V_{DS} = 0.5 V for MESFET on graphene and MESFT on GaAs.

A depletion mode (normally on) GaAs metal-semiconductor field effect transistor (MESFET) was also devised, the schematic of the device stack is shown in Figure 3-8a. The MESFET was grown on a 3 μm thick intrinsic GaAs buffer layer in the MOCVD reactor, with 150 nm of n-GaAs doped with 4×10^{17} cm^{-3} Si to form the n-channel of the device and 50 nm of highly doped (5×10^{18} cm^{-3}) n-GaAs to form ohmic contact for the source and drain contacts. The source and drain contacts were patterned by photolithography using an LOR 3A and SPR 220 bilayer photoresist process. Metal contacts were formed by depositing Pd(5 nm)/Ge(20 nm)/Au(100 nm) by e-beam evaporation. After lift-off, the mesas were defined using SPR 220 and chemically etched down to the n-GaAs channel using $HCl:H_3PO_4$ (3:1) solution. The stack was annealed for 1 hr at 200°C for ohmic contact formation. Bilayer photoresist process was applied again to form gate contacts, metal contacts for the gate was formed with Ti(10 nm)/Au(100 nm) by e-beam evaporation. The device was complete after lift-off of the metal film. The I_{DS} vs V_{DS}

and I_{DS} vs V_{GS} curves in Figure 3-8b, c show similar performance of GaAs MESFET grown via remote epitaxy to one grown directly on GaAs substrate. I_{DS} vs V_{GS} curves present identical threshold voltage, V_{th}, of -6 V and transconductance, g_m, of 1 mS. Thus, the performance of GaAs MESFET demonstrates that the material platform grown via remote epitaxy offers the same quality compared to conventional homoepitaxial growth.

Chapter 4

Summary and Future Work

Conventional homoepitaxial growth relies on covalent interactions between the commensurate overlayer lattice to the substrate. However, there exists a limited distance where adsorbates are made to interact with the substrate to achieve single crystalline epitaxial growth without necessitating direct bonding of the epitaxial film to the substrate. By introducing graphene on a substrate to define the interaction gap between the epitaxial film and substrate, homoepitaxial growth can be achieved at a remote distance. Graphene weakly screens the electronic potential of the substrate, thereby allowing the substrate to guide the crystalline orientation of the overlayer lattice. The findings presented in this work suggest that epitaxial growth does not strictly require covalent interactions between incoming adsorbates and the substrate in order to achieve single-crystalline growth. The study of remote epitaxy initiated in this thesis opens a new avenue of research which challenge the current understanding of epitaxial growths. Exploring the potential and limitations of remote epitaxy may lead to larger application of this growth technique that may lead to discovery of new phenomena in epitaxy and the role of 2D materials in semiconductor industries.

The passivated surface of graphene is also important in the realization of a novel layer transfer techniques to exfoliate and transfer semiconductor thin films. 2DLT process discussed in this thesis offers rapid exfoliation with a well-defined cleavage plane at the graphene interface, requiring minimal surface treatment for the parent substrate, unlike ELO, LLO and controlled spalling. Thus, 2DLT significantly eases production costs in growing exotic semiconductor thin films and re-using template substrates for multiple re-growth and transfer processes. By relieving

the economic burden of utilizing exotic semiconductors, industries will be given the impetus to fabricate devices based on performance efficiency in lieu of cost efficiency.

The 2DLT process can enable semiconductor thin films to be stacked to other electronic and photonic materials. This enables monolithic integration of dissimilar materials without the limitation imposed by the lattice matching requirement in epitaxy. Defect-free heterointegration of unique material systems offers the potential to create highly efficient devices leveraging on the strengths of each material's properties. Proposed below are continuing investigations of novel heterointegrated devices that rely on remote epitaxy and 2DLT process in order to grow and integrate dissimilar exotic semiconductor thin films.

4.1 High resolution solid state displays

The application of 2DLT enables vertical stacking of semiconductor thin films in order to create monolithic device stack for red, green, and blue (RGB) LEDs which can be fabricated with conventional photolithographic techniques to create high resolution micro-LED displays. Current LED displays contain pixels that are composed of individual red, green and blue subpixels aligned together in an array, such as the Bayer array configuration. Packaging of these individual subpixel LEDs significantly limits the resolution and color accuracy of LED displays. While current LED displays cannot compare to resolution offered by OLED displays, which boasts one of the highest pixel densities[33], it performs worse than LED displays in terms of brightness, lifetime and power efficiency. Vertical stacking of micro-LEDs can improve the pixel density and color accuracy compared to LED displays based on Bayer arrays. In addition, stacking of thin film semiconductors enables the fabrication of flexible displays that can be applied to wider range of display applications, such as outdoor displays and wearable technology.

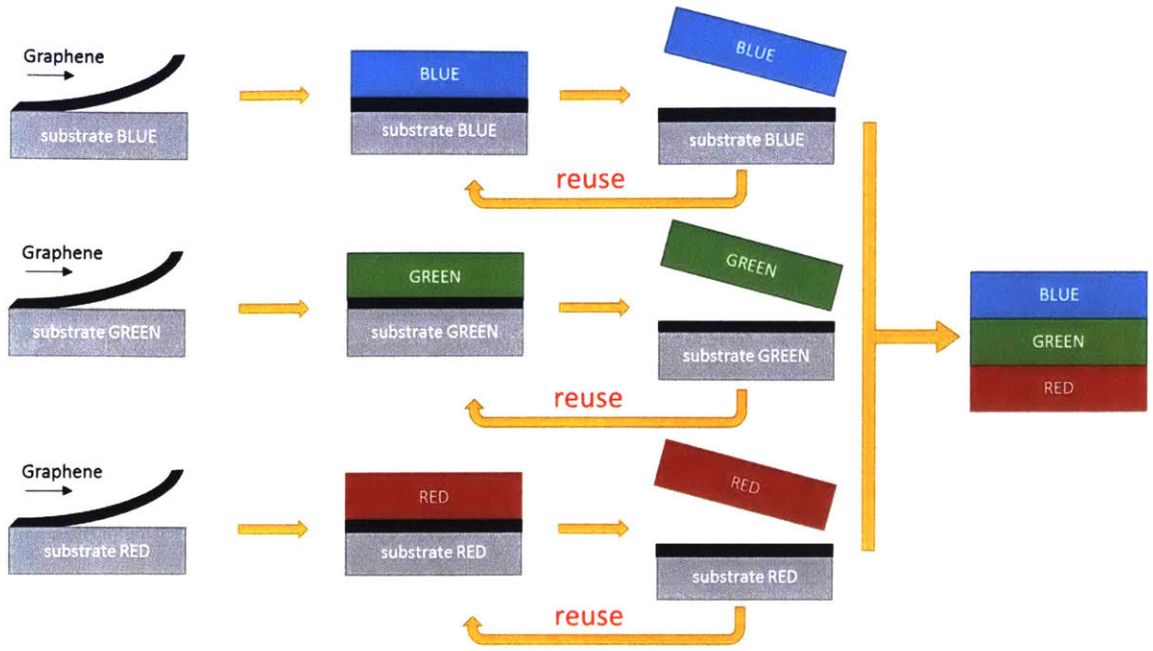


Figure 4-1: Process flow for fabrication of vertically stacked micro-LEDs.

The figure above illustrates the process flow of fabricating the proposed micro-LED device. Semiconductor wafers are coated with graphene and remote epitaxy is implemented to grow individual semiconductor films that will emit blue, green and red light. For example, graphene coated SiC substrate can be utilized to fabricate GaN-based blue and green LED films, while graphene coated GaAs substrate will form GaAs-based red LED films. These films are exfoliated by 2DLT and stacked vertically on top of each other, while the parent substrate is reused for further growth and transfers. Stacked LED films is transferred once more to be monolithically integrated with transistors to create micro-LED arrays with individually addressed pixels [34].

4.2 Low-cost compound semiconductor photovoltaic cells

Heterointegration of semiconductor films by 2DLT also enables the fabrication of highly efficient photovoltaic (PV) devices. PV technology promises to be a reliable source for alternative energy and for several decades a lot of effort have been invested by the PV industry to fabricate

ultrahigh efficiency PV cells while minimizing production costs. While compound semiconductor PV cells, such as GaAs-based multijunction PVs, exhibit the highest power conversion efficiency (PCE) > 44% they suffer from exorbitant production costs (~$50k/m^2) [4]. On the other hand, low cost solar cells with production costs of ~$200/m^2, such as poly-crystalline Si, provide relatively poor PCE of only ~15-20%. While there has been intensive research in integrating GaAs-based PV onto Si through metamorphic growth of GaAs using graded buffers, strained-layer superlattices, etc… it has been difficult to achieve high quality heterogeneous epitaxy of GaAs due to the large lattice mismatch of ~4% between Si and GaAs. Metamorphic growth techniques for highly lattice mismatched systems often yield high dislocation density and unsuitable rough surfaces, detrimental to PV performance. By leveraging on cost saving potential of the 2DLT process, the production cost of compound semiconductor PVs can be significantly lowered in order to be competitive with Si-based PV technology.

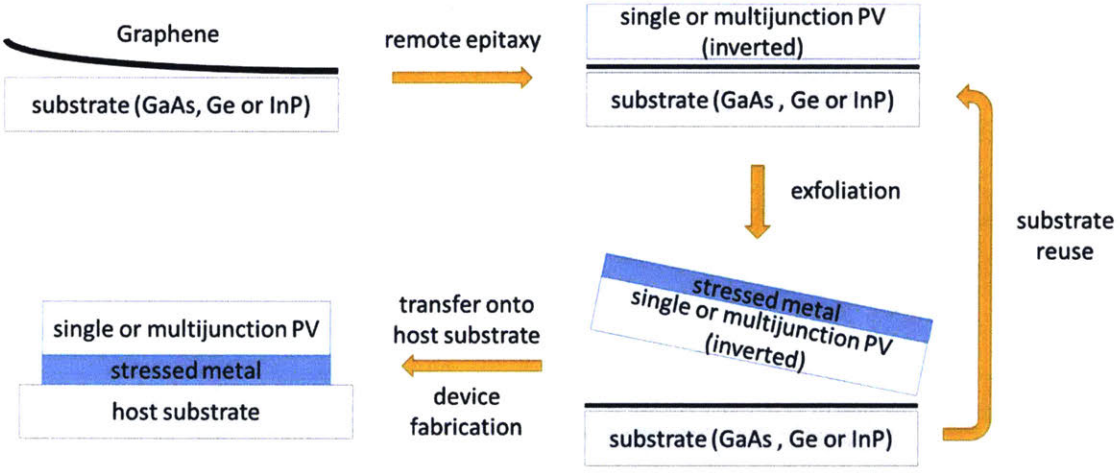


Figure 4-2: Process flow for fabrication of low-cost compound semiconductor PV.

The process flow for the fabrication of low-cost compound semiconductor PV is presented in the figure above. Analogous to the ELO process for fabricating thin film GaAs-based PV[35], graphene-coated compound semiconductor wafer is used as a template substrate to grow PV device

stacks via remote epitaxy. Initially an inverted PV stack is grown then exfoliated via 2DLT process on a stressed metal film. The stack can be left on the metal film and transferred onto a cheaper substrate to be further processed and packaged. During this process, a back surface mirror can be integrated with the metal stressor film in order to further enhance the device PCE. The material of the host substrate can also be selected in order to provide a more effective heat management of the device as well. The ease of exfoliation via 2DLT and re-usability of the template wafer with little surface treatment, offer high throughput in device fabrication at significantly reduced production costs. Moreover, the same process can be applied for a broad range of material systems, limited only by the available template wafer for remote epitaxy.

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