Design and Evaluation of Cellular Power Converter Architectures

by

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Abstract

Power electronic technology plays an important role in many energy conversion and storage applications, including machine drives, power supplies, frequency changers and UPS systems. Increases in performance and reductions in cost have been achieved through the development of higher performance power semiconductor devices and integrated control devices with increased functionality. Manufacturing techniques, however, have changed little. High power is typically achieved by paralleling multiple die in a single package, producing the physical equivalent of a single large device. Consequently, both the device package and the converter in which the device is used continue to require large, complex mechanical structures, and relatively sophisticated heat transfer systems.

An alternative to this approach is the use of a cellular power converter architecture, which is based upon the parallel connection of a large number of quasi-autonomous converters, called cells, each of which is designed for a fraction of the system rating. The cell rating is chosen such that single-die devices in inexpensive packages can be used, and the cell fabricated with an automated assembly process. The use of quasi-autonomous cells means that system performance is not compromised by the failure of a cell.

This thesis explores the design of cellular converter architectures with the objective of achieving improvements in performance, reliability, and cost over conventional converter designs. New approaches are developed and experimentally verified for highly distributed control of cellular converters, including methods for ripple cancellation and current-sharing control. The performance of these techniques are quantified, and their dynamics are analyzed. Cell topologies suitable to the cellular architecture are investigated, and their use for systems in the 5-500 kVA range is explored. The design, construction, and experimental evaluation of a 6 kW cellular switched-mode rectifier is also addressed. This cellular system implements entirely distributed control, and achieves performance levels unattainable with an equivalent single converter.

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Acknowledgments

The first place I visited when I arrived at MIT was the office of Professor John Kassakian, who had been assigned to be my academic advisor. In retrospect, it was that lucky happenstance that set the direction of my academic career. John's great enthusiasm for electrical engineering (and his encyclopedic knowledge of it) have made working with him the most enjoyable aspect of my tenure at MIT, and have kindled in me a desire to continue on in academics.

During my time at MIT, I have also had the opportunity to work closely with both of my thesis readers, Professors George Verghese and Dick Thornton. Both of them have been sources of inspiration for me, and I have always appreciated the ability to walk into their offices and take advantage of their vast wealth of engineering knowledge. Other LEES faculty and staff have also been very helpful, including Professor Steven Leeb (whose generosity with time and equipment are unbelievable), Wayne Hagman, Dave Otten, Wayne Ryan, and Vivian Mizuno (who keeps the whole place running). All of them have made LEES a great place to work.

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To Hideko,

Whose Companionship I Cherish

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Chapter 1

Introduction

1.1 Background and Motivations

Power electronic technology plays an important role in many energy conversion applications, including machine drives, power supplies, frequency changers, and UPS systems. Increases in performance and reductions in cost have been achieved through the development of higher power, fully controllable semiconductor devices, such as the GTO, power MOSFET, and IGBT, and integrated control devices with increased functionality, such as microcontrollers and integrated analog circuits. Manufacturing techniques, however, have changed little. High power is typically achieved by paralleling multiple die in a single package, producing the physical equivalent of a single large device. Consequently, both the device package and the converter in which the device is used continue to require large, complex mechanical structures and relatively sophisticated heat transfer systems.

An alternative to this approach is the use of a cellular architecture [1,2]. As shown in Fig. 1.1, a cellular architecture is based upon the parallel connection of a large number of quasi-autonomous converters, called cells, each designed for a fraction of the system rating. The cell rating, typically on the order of 1-5 kW, is chosen such that single-die devices in inexpensive packages can be used and the

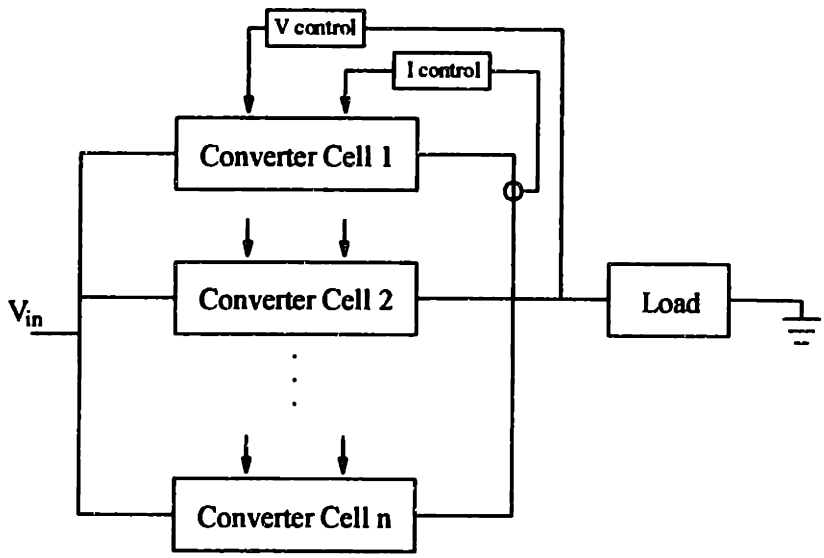


Figure 1.1 A cellular converter architecture supplying a single load.

cell fabricated with an automated assembly process. The use of quasi-autonomous cells means that system performance is not compromised by the failure of a cell.

Paralleled converter systems are often used when very high power levels are required [3,4], as well as in applications demanding high reliability [5,6]. However, paralleling on a scale discussed in this thesis, where mass production techniques can be used, remains relatively unexploited. It is anticipated that systems built using a cellular architecture can exhibit improved functional performance, improved maintainability and reliability, and reduced cost when compared to systems designed and constructed in a conventional manner.

1.1.1 Performance

The cellular architecture's potential for improved functional performance arises from the characteristics of both the individual cells and their aggregation. At the cell level, the smaller components and physical dimensions of interconnects make possible an appreciable increase in switching frequency. The power processing capability of system components such as devices, capacitors, etc, is directly related to their volume. As the size and spacing of these components become larger, so do the parasitic elements which limit performance. For example, a typical TO-247 plastic-packaged 40 A 600 V IGBT may have a package inductance on the order of 10 nH, while a 400 A 600 V IGBT module may have an inductance on the order of 30 nH. Because switching losses due to this parasitic inductance are proportional to frequency and the sum of Li^2 terms, the small devices have considerable advantage as the switching frequency is increased. Similarly, lead inductance values make it far easier to select and connect resonant or snubber capacitors for multiple small devices than for a single large module, especially if high-speed devices are being used. This means that the transient device overvoltage at turn off will be lower for the small devices than for the single large module, and less derating is required for them. Thus, the physical dimensions of the components and interconnects heavily favor a cellular architecture when high switching frequencies are desired.

The aggregation of outputs of many cells also yields significant performance advantages over a single large converter. The advantages of *interleaving*, in which multiple converters are operated out of phase, are well known [7-9]. These advantages include a decrease in ripple amplitude and an increase in fundamental ripple frequency. Paralleled converters which are controlled autonomously also possess advantages over the single converter alternative. Because they are controlled autonomously, the cells exhibit neither frequency nor phase coherence. Thus, their aggregated outputs produce a low energy density spectrum with stochastically reduced harmonic components. Figure 1.2 illustrates the ripple

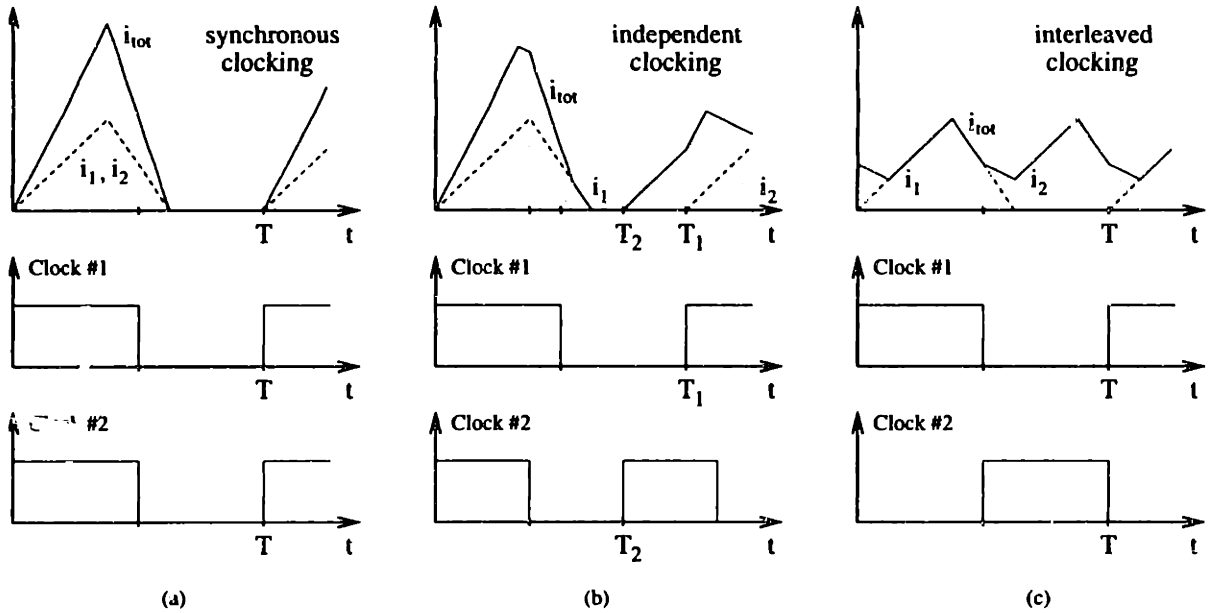


Figure 1.2 Clocking and cell current waveforms for paralleled power converters: (a) synchronous clocking, (b) independent clocking, and (c) interleaved clocking.

cancellation benefits that can be obtained from these techniques for a two-cell example. Figure 1.2 (a) shows the cell currents and the aggregate current for two cells operated with synchronized clocks. The aggregate current in this case is the same as that of a single large converter with the same total energy storage, switching frequency, and losses. Figure 1.2 (b) shows the results with independent clocks. In this case, the peak ripple amplitude does not decrease, but the rms of the ripple is significantly lowered. Figure 1.2 (c) shows the results of interleaving the clocks. The amplitude of the aggregate ripple current is decreased, and its fundamental frequency is doubled. What may be concluded is that the aggregation of cells allows significant reduction in the aggregate rms and peak ripple compared to a single large converter. This is important, since it makes possible considerable reductions in filter size and stress, EMI, and (for loads such as machines) acoustic noise.

1.1.2 Reliability

System reliability is determined by both component reliability and the results of component failure. Component reliability in a cellular system can be higher than in conventional systems for a number of reasons. First, automated assembly and test is known to produce more consistent and higher quality products than manual assembly. Second, many of the components, such as the semiconductor devices, are produced in high volume and are therefore better characterized than their larger, more complex counterparts in conventional systems. Finally, because its higher switching frequency allows a higher

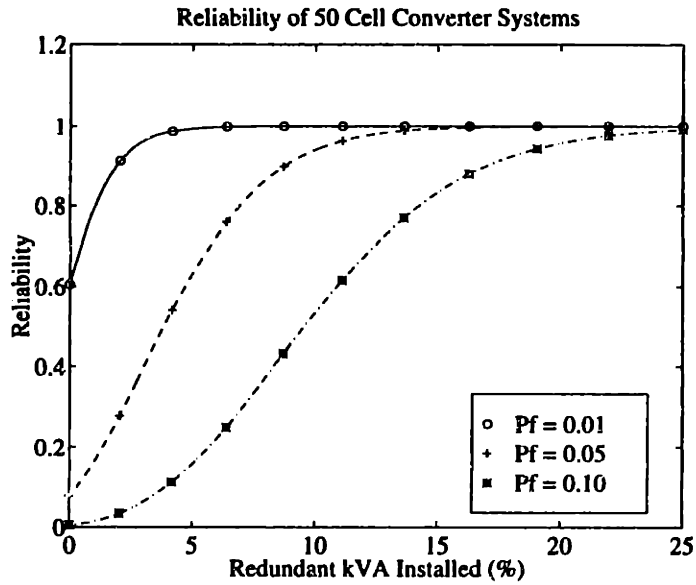


Figure 1.3 The reliability for a 50 cell converter for three cell failure probabilities.

control bandwidth, a cellular system can respond more quickly to abnormal and damaging system conditions, such as short circuits and overloads.

Nevertheless, the fact that a cellular system has more components must be addressed when considering the system reliability. High system reliability can be achieved by incorporating more cells than necessary to meet the required power rating, thus exploiting the inherent redundancy of the architecture.

Appreciation for the trade-offs among net component count, redundancy and reliability, can be obtained using relatively simple models. Consider a model which predicts the reliability of a (K,N) parallel converter system over a defined operating lifetime. A (K,N) converter system is one with N total cells, where K cells are required to meet 100% rated capacity (a conventional converter is thus a (1,1) system). Reliability is defined as the probability that the number of operational cells will not fall below K during a prespecified lifetime. We model the probability of failure of individual cells during the operating lifetime as independent Bernoulli trials, with probability of failure P_f. The reliability of the (K,N) system over its operating lifetime is thus [11]:

$$R = \sum_{i=K}^{N} \binom{N}{i} \left[1 - P_f \right]^i P_f^{N-i} . \qquad (1.1)$$

Figure 1.3 shows the reliability of a system with 50 cells for three different values of cell reliability ($1-P_f$). As can be seen, for a 50 cell system with relatively reliable cells, the redundancy needed to meet and

exceed the reliability of a single converter system, $(1-P_f)$, is modest, 6.4% for $P_f = 0.01$. That is, the reliability of a (47,50) cellular system (0.9984) exceeds that of a single converter (0.99). However, as the individual cell reliability declines, the redundancy required to attain the same reliability as a single converter is much higher. In the likely event that the individual cells are more reliable than the single large converter (due to the different component attributes, assembly processes, testing, etc), the cellular architecture becomes even more attractive.

Other reliability benefits of the cellular approach are not captured by this simple model. For example, with a cellular architecture, it is possible to design systems which are *gracefully degrading*. That is, a cellular converter can continue to function at reduced rating even after the number of cell failures exceeds N-K. In contrast, a conventional system could not operate at reduced rating- it can either supply the rated load, or it cannot supply any load. Furthermore, most large converter systems are designed to support some percentage of continuous overload, so that the redundant units in a cellular system may not represent any excess installed kVA at all.

Another aspect of reliability which is of interest in many applications is availability. Availability is defined as the fraction of time the converter is expected to be operational (for our purposes, at 100% rated capacity). To model the availability of conventional and cellular converters, we will assume independent, exponentially distributed time periods for failure and (one at a time) repair of individual converter cells. We can then construct a simple Markov chain model, as shown in Fig. 1.4, which probabalistically describes the evolution of the system operating condition based on cell failure rate λ, repair rate μ, and the current state of the system. We use this model to compute the steady-state probability that any number of converters in a (K,N) system will be operational, and hence find the availability of the system [11]. Consider the availability of a single converter using this model. If we use a Mean Time Between Failures (MTBF,$1/\lambda$) of 2 years, and a Mean Time To Repair (MTTR,$1/\mu$) of 185 hours as suggested by the range of values in [12,13], we find that the availability of the system

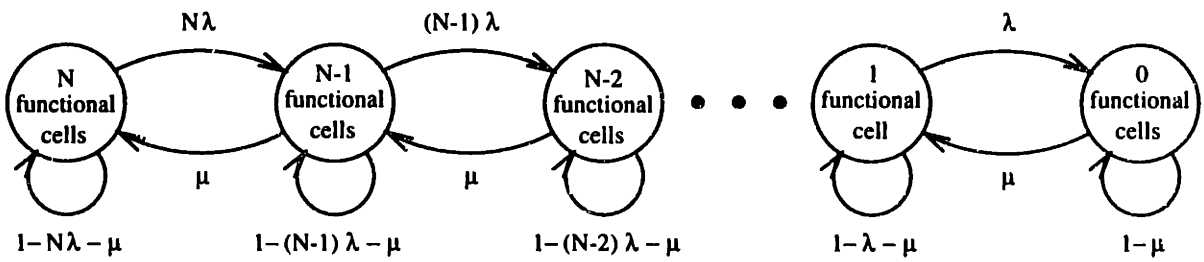


Figure 1.4 A Markov chain model for cellular converter availability calculations.

is 0.9895. Now consider the availability of a (45,50) cellular converter system. Using the same MTBF and MTTR values for the individual cells, we get a slightly lower availability of 0.9523. However, consider reducing the MTTR parameter of the cellular converter to 24 Hours. This is perfectly reasonable, since repairing a cellular architecture involves only replacing a single standard cell, and does not require the special labor and parts needed to repair a conventionally constructed converter. With these parameters, the availability of the cellular system is 0.999999924 - vastly superior to the conventional alternative. In fact, a more realistic model allowing multiple failed units to be repaired in parallel would favor the cellular converter even more heavily.

These simple arguments indicate that it is quite possible for the reliability of a cellular converter to far exceed that of the conventionally constructed alternative. To realize these potential benefits, methods must be developed to eliminate single-point failure modes in the distributed system so that the failure of a single converter cell does not cause a system failure.

1.1.3 Cost

The penetration of power electronics into commercial energy conversion applications has been driven primarily by economics and secondarily by performance. Thus, in all except for the few applications where reliability or performance are of primary importance, the success of cellular architectures in the marketplace will depend on economics.

One area in which cellular architectures have cost benefits is in the assembly and test process. Hand assembly and test is the standard method for constructing high power converter units. This process is both costly and complex. Conversely, automated assembly equipment can be used to manufacture and test the cells in a cellular architecture, reducing the hand assembly portions to a minimum and eliminating much of the more complex work. Furthermore, because large numbers of identical cells can be built (even for constructing converters of different ratings), economies of volume can reduce costs.

A second area in which a cellular system has economic advantages is in the cost of the thermal management system. At low power densities, inexpensive air-cooled extruded or bonded-fin heat sinks can be used for cooling. For higher power densities, much more expensive liquid cooling technologies must be employed. The thermal power density through the contact surfaces of plastic-packaged devices and large power modules are both in the same range (roughly 50-200 W/in^2). However, because a particular device can only transfer heat effectively through a limited surrounding heat sink area, the relative position of heat sources (devices) on the sink is important. By distributing the heat sources, a cellular architecture can take advantage of heat sink area much more effectively than can a single power

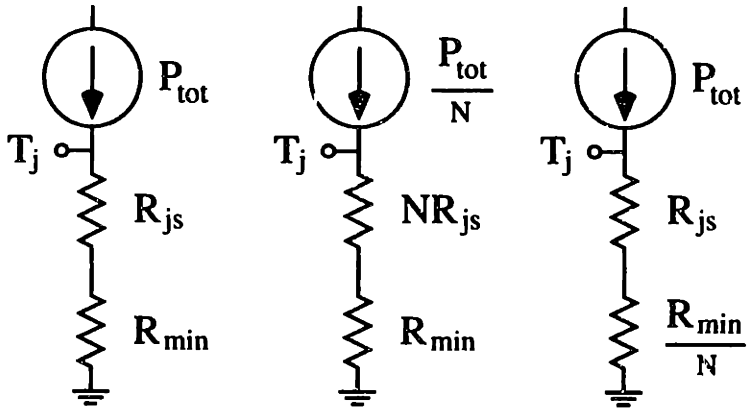


Figure 1.5 Thermal models for modules and distributed discrete devices.

module, which permits the use of lower-cost cooling technology.

To understand this quantitatively, consider the thermal models for single-module and distributed systems shown in Fig. 1.5. For devices with a constant on-state voltage (such as IGBTs), the junction-to-case thermal resistance (R_{jc}) of a plastic packaged device rated for I_o amperes will be roughly N times that of a module rated for NI_o amperes. This follows directly from the fact that the power handling capability of a package is thermally limited. The scaling of contact surface changes R_{cs} in a similar manner. Next, consider the thermal resistance of the heat sink. The sink-to-ambient thermal resistance (R_{sa}) of an air-cooled heat sink for a point-source of heat initially decreases with increasing sink size. However the thermal resistance stops decreasing as the size of the heat sink becomes larger because sections of the heat sink far from the point-source do not contribute to the heat transfer. Thus, to first order, there is a minimum R_{sa} that can be obtained for a given heat sink with a point-source load, which can typically be determined from manufacturer's derating tables. Now, if we divide the single point-source into N point-sources, we can obtain the same minimum thermal resistance *from each point source*. Applying these concepts, we obtain the thermal models of Fig. 1.5. As can be seen, distributing the single point source of heat can yield dramatically lower junction temperatures for the same total power dissipation and device area, due to improved utilization of the heat sink. Practically speaking, this allows a cellular converter to use a lower power density, lower cost thermal management system than a conventionally constructed converter.

While high volume and automated assembly surely reduce costs, as does the simplification of thermal management possible in a distributed system, there are several aspects of the cellular approach

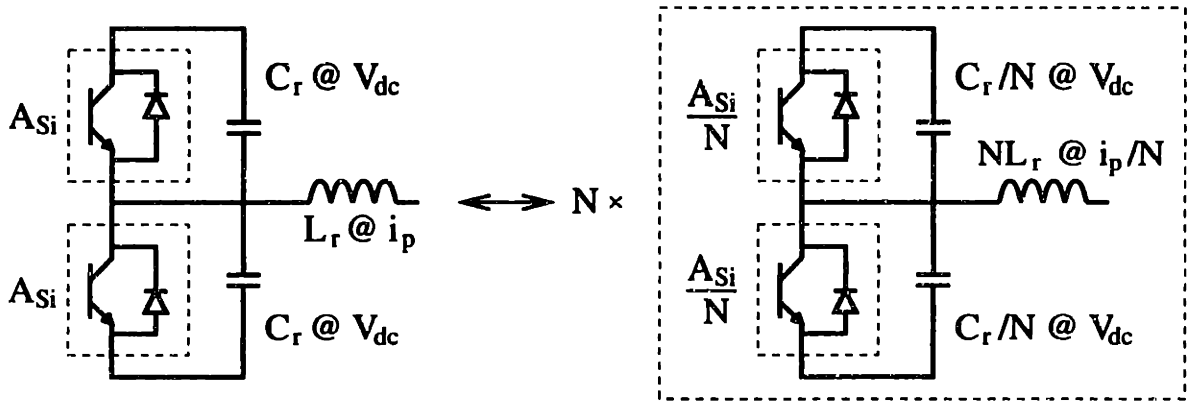


Figure 1.6 A resonant pole inverter leg and its equivalent components in a cellular system.

which increase cost. Some components in a cellular converter can be seen as a redistribution of the component parts of a single large converter, as illustrated in Fig. 1.6. However, other circuit components, such as sensing and control circuits, are not distributed among converters, but are replicated. As more and more cells are used, the replicated component costs become a higher fraction of the total, and degrade the economic benefits of the cellular approach (although this is partially offset by the ability to attain higher levels of integration of these components). The ultimate economic benefits of the cellular approach thus remain uncertain. However, it is clear that practical cellular architectures must be designed in a manner which mitigate the negative cost impacts, while taking advantage of the potential cost benefits of the approach.

The cellular conversion approach thus has the potential for improved functional performance, reliability, and cost compared to conventionally designed and constructed systems. Taken together, the previous discussions argue compellingly that this type of power converter architecture should be pursued aggressively.

1.2 Thesis Objectives and Contributions

This thesis explores the design of cellular converter architectures with the aim of achieving improvements in performance, reliability, and cost over conventional converter designs. The thesis has three objectives in this direction. The first is to develop fundamental, low-cost control methods for cellular power converters that allow new levels of performance and reliability to be achieved. Control system design is a crucial issue in a cellular power conversion system since it heavily impacts the performance, reliability and cost of the system. The thesis focusses on distributed control techniques due to the fact that centralized control becomes unattractive as the number of cells grows. New methods are developed and experimentally verified for current-sharing control of cellular converters. These

methods are unique in that they allow the isolation or elimination of the control interconnections used to communicate current-sharing information among converter cells, thus allowing improvements in system reliability and fault tolerance. In addition, the closed-loop dynamic behavior of systems implementing these current-sharing techniques are analyzed and compared to experimental results. It is demonstrated that accurate and stable current-sharing can be achieved in a cellular converter architecture without the need for control interconnections among cells.

Control techniques for passive and active ripple cancellation among cells are also investigated. A distributed implementation of the interleaving method of ripple cancellation is developed which requires only a single, noncritical, isolatable interconnection among cells. Unlike conventional interleaving methods, the new distributed implementation requires no centralized control, automatically accommodates varying numbers of converter cells, and is highly tolerant of subsystem failures. The thesis also quantifies the benefits of passive (stochastic) ripple cancellation, and validates the theoretical predictions against simulation and experimental results. The thesis demonstrates that a tremendous degree of ripple cancellation can be achieved in a cellular architecture without the need for centralized control.

The second objective of this thesis is to explore some of the key considerations in selecting and designing power stage topologies for cellular converter systems. Both the cost and performance of a cellular converter system heavily depend on the power stage topology, making its selection an important design decision. The thesis identifies some of the important issues in the design of cellular converter systems, including the impact of replicated and added components and the need for instantaneous current-sharing among cells. Cell topologies, including both an inverter topology and a rectifier topology, which address these design issues are investigated. We show that these topologies are well suited to the requirements of a cellular architecture, and mitigate some of the major drawbacks of the single large converters on which they are based.

To realize the potential advantages of cellular power conversion, and to allow the benefits and limitations of the approach to be fully evaluated, it is necessary to experimentally establish the viability of the cellular architecture concept at a reasonable power level. This allows the performance of the technology to be verified, and permits the identification of remaining barriers to its adoption. The final objective of this thesis is to develop a prototype cellular converter system at a realistic power level which is useful for evaluating the cellular design approach, and which can serve as a full-power test bed for the development of new cellular control methods. The thesis describes the design, implementation, and experimental evaluation of a six-cell, six-kilowatt cellular switched-mode rectifier. The cellular system

implements both distributed load sharing and distributed ripple cancellation, and achieves performance levels unattainable with an equivalent single converter. In addition to its function in aiding the evaluation of the cellular conversion approach, the prototype system is designed to allow other control methods to be easily implemented and tested through the use of "piggyback" control boards.

1.3 Thesis Organization

The thesis is divided in to nine chapters, including this introductory chapter. Chapter 2 introduces a new current-sharing approach for paralleled power converters which is based on frequency encoding of the current-sharing information. This approach has several advantages, including the ability to allow transformer isolation or elimination of current-sharing control connections.

Chapters 3 and 4 each present the design, implementation and experimental evaluation of current-sharing methods based on the frequency encoding approach introduced in Chapter 2. In the method developed in Chapter 3, current sharing information is encoded on small perturbations in output current, while in the method of Chapter 4, the cell switching ripple itself carries the current-sharing information. In each case, a three-cell prototype system implementing the method is developed and evaluated. The results of these chapters demonstrate that accurate and stable load sharing is obtainable over a wide load range without the use of intercell connections for communicating current-sharing information.

Chapter 5 addresses the dynamic analysis of systems employing nonlinear current-sharing control techniques. The ability to predict current-sharing and output dynamics is an important part of cellular converter design. The first part of the chapter analyzes nonlinear current-sharing control techniques which are linearizable about a constant operating point. To validate the analysis, it is applied to the current-sharing control scheme developed in chapter 3 and compared to experimental results. The second part of the chapter analyzes the dynamics of the widely-used UC3907 control scheme for an important special case. This analysis, which is applicable to the prototype converter system developed in Chapter 8, is also validated against experimental results.

Chapter 6 investigates ripple cancellation techniques which are well suited to a cellular architecture. The first part of the chapter analytically quantifies the amount of passive ripple cancellation that occurs among independently clocked cells in a parallel converter system. The second part of the chapter develops a distributed implementation of the interleaving method of ripple cancellation. Experimental results from a three-cell prototype system are used to corroborate the analytical predictions of the first part of the chapter, and to demonstrate the benefits of the distributed interleaving approach.

Chapter 7 discusses some of the key considerations in the design of cellular converter systems. The

chapter also presents a new cellular inverter implementation which addresses these design issues. It is shown that the architecture mitigates some of the major drawbacks of the single resonant pole inverter (RPI), on which it is based. Furthermore, the chapter presents an enhanced control algorithm which significantly reduces stresses and losses for many operating conditions, and is applicable to both the RPI and the parallel architecture.

Chapter 8 presents the development and evaluation of a six-cell, six-kilowatt cellular rectifier system. The first part of the chapter describes conventional approaches to high-power-factor rectification and limitations associated with them. The second part of the chapter analyzes the benefits that can be achieved through the use of a cellular architecture, and presents the design of the prototype cellular converter system. The final part of the chapter presents an experimental evaluation of the prototype cellular converter system. It is shown that the prototype system behaves as predicted, and achieves performance levels unattainable with an equivalent single converter.

Finally, Chapter 9 presents a summary of the ground covered in the thesis, and presents recommendations for continued work in the area.

Chapter 2

Frequency-Based Current-Sharing Techniques

Maintaining current sharing among cells in a cellular converter architecture is an important design goal. This chapter introduces a new current-sharing technique for paralleled power converters which is based on frequency encoding of the current-sharing information. This approach has several advantages, including the ability to transformer isolate or eliminate current-sharing control connections.

2.1 Introduction

One important characteristic of a cellular converter system is that the individual converter cells share the load current equally and stably. Good current-sharing behavior is important for a number of reasons. First, reliability of a system tends to be reduced in the absence of good current sharing. If some cells continuously operate under heavy load due to a lack of current sharing, their increased failure rate can strongly impact the overall system reliability. Second, system losses tend to increase in the absence of current sharing due to the poor utilization of semiconductor devices and magnetics. Finally, the current-sharing behavior of a parallel architecture strongly affects the output dynamics, and must be addressed as part of the system control design.

The current-sharing behavior of a parallel converter system is largely dependent on the manner in which the individual converter cells are controlled. Many parallel converter systems use some form of global control, in which a single, possibly redundant, controller directly regulates the load balance among the individual converters [3-6,14-20]. While this approach is sometimes appropriate, to enhance modularity and improve reliability it is often more desirable to have the load-sharing control distributed among the converter cells [1,2]. For this reason, this thesis will focus only on distributed load-sharing control approaches.

Only a limited amount of information needs to be shared among the individual cells to implement a distributed load-sharing scheme. For example, given information about the average of all the cells' output currents, each cell can regulate its output to be close to the average [22-29]. Other quantities valid for the ensemble of converter cells can also be used, including rms cell current [30], weighted cell current stress [31], and highest cell current [32].

Load-sharing information is most commonly generated and shared over a single interconnection

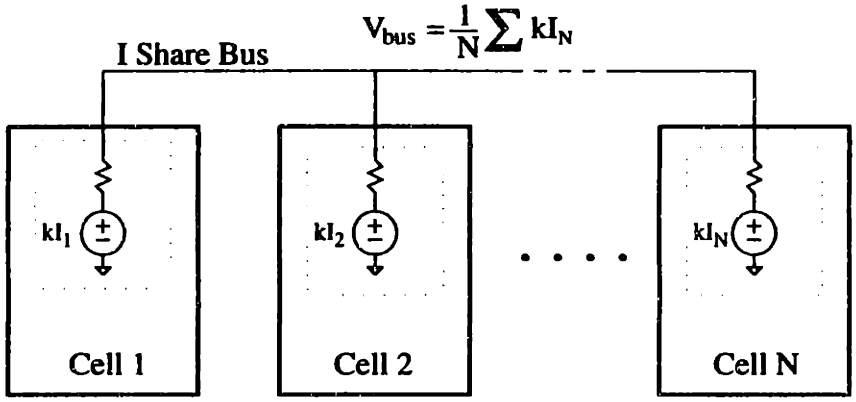


Figure 2.1 A method for computing the average cell output current using a single interconnection among cells.

among converter cells. Typically, the interconnection circuit is designed so that when each cell generates a signal proportional to its output, the voltage on the interconnection bus is the average (or maximum, etc.) of the individual signals. For example, Fig. 2.1 shows a possible implementation in which the interconnection bus voltage is proportional to the average of the cell currents. For ac output converters, the interconnection may sometimes be transformer isolated from the local cell control circuits [22,23]. However, for many applications transformer isolation cannot be employed using conventional methods since the current-sharing information has frequency content down to dc.

Approaches exist where current-sharing information is communicated implicitly via the output, and no additional interconnections among converter cells are required. For paralleled constant-frequency inverters, load balance can be achieved by implementing a frequency and voltage droop characteristic in each cell output. This technique, which is also used to regulate the power output of paralleled generators in an ac supply system, employs the ac bus voltage and frequency to communicate power-sharing information among the controllers [23,33]. Unfortunately, the complexity and cost of the approach limits its use to relatively large inverter cells. Dc output power supplies sometimes use output voltage droop characteristics to achieve a degree of current-sharing [19,34,35]. While simple, this approach yields heavy load regulation in the output and steady-state current imbalances, which are often unacceptable.

2.2 Frequency-Based Current Sharing

This chapter introduces a new, frequency domain based method for encoding and distributing current-sharing information among cells. This new scheme has significant advantages over existing

methods, particularly with respect to reliability. It operates in the following manner. Each converter cell generates a (typically sinusoidal) signal whose frequency is related to the average output current (or power or other variable to be regulated) of the cell. The signal frequency range used can be widely separated from the fundamental output frequency of the converter system. The signals from each cell are summed, with the result available to each cell. Each cell employs a frequency estimator circuit to calculate a weighted average, ω_{est}, of the frequency content of the aggregate signal. Each cell can then compare its own generated frequency, ω_k, to the weighted average ω_{est}, and adjust its output to make $\omega_k = \omega_{est}$. (Alternatively, functions of these frequencies, such as their squares or logarithms, can be compared yielding similar results.) With this method, a priori information about the number of cells in a paralleled system is unnecessary, since each cell needs only the aggregate signal for current sharing to be effected. Thus, current sharing is preserved even if cells fail or are added.

The frequency encoding approach circumvents some of the major limitations of existing current-sharing methods. The direct interconnection among control circuits present in conventional distributed load-sharing schemes is a source of single-point failure mechanisms which, in the worst case, can bring the entire converter system down. Elimination of single-point failure modes is a key design objective for achieving fault tolerance in distributed converter architectures [36]. It will be shown that with the frequency-based approach, current-sharing information can be encoded at high frequencies and distributed over the output or input bus, making additional control interconnections among cells unnecessary. Alternatively, if separate interconnections for current-sharing are used, they may be galvanically isolated using small, high-frequency transformers. Thus, the frequency encoding method allows improvements in reliability and availability by eliminating the failure modes associated with direct interconnections among the control circuits.

This new control approach has other potential advantages. In conventional schemes, current-sharing information is encoded and distributed at low frequencies (typically down to dc). With the frequency-encoding approach, the designer can select the frequency range over which current-sharing information is communicated, and can use this design freedom to achieve objectives such as noise minimization. Furthermore, with the frequency-based method, the aggregate current-sharing signal contains information about the total number of converter cells and their *individual* output currents in addition to information about the average output of the converters. This may have some benefits for system monitoring and fault detection.

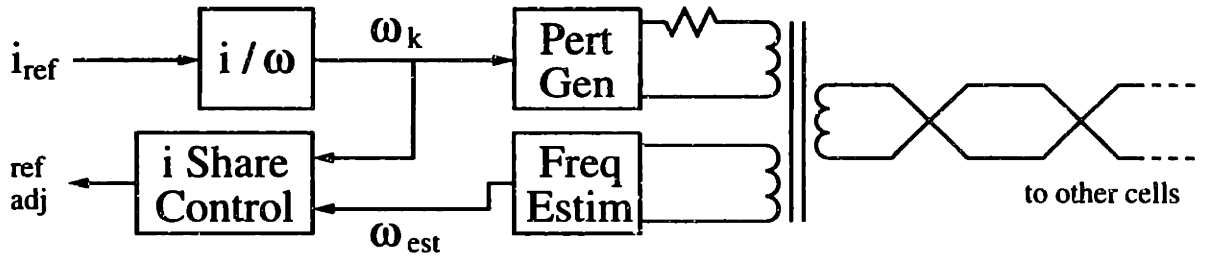


Figure 2.2 Schematic of the isolated single connection implementation of frequency-based load-sharing control. The transformer is series wound on one core. Current-sharing signals are injected from the primary winding (on the cell side) to the secondary (connected to the current-sharing bus). The current-sharing bus voltage is sensed with a tertiary winding.

2.3 Implementation Approaches

To implement load-sharing control using the frequency encoding method, the signals from the individual cells are summed at a node, and the sum is accessible to all the cells. There are several ways to do this. Three of them will be considered here: the isolated single connection implementation, the output perturbation implementation, and the switching ripple implementation.

2.3.1 The Isolated Single Connection Implementation

The *isolated single connection implementation*, shown in Fig. 2.2, communicates current-sharing information over a dedicated bus, similar to existing single connection approaches [22-29,31,32]. Each converter cell injects onto the current-sharing bus a signal whose frequency is related to its output current. The cell measures the aggregate signal on the bus to determine ω_{est} and control current balance. Transformer isolation can be employed because there is no low-frequency content to the current-sharing signals. Transformer isolation reduces the possibility that a single-point failure can damage the whole system via the current-sharing connections. Furthermore, this approach is advantageous for systems in which the converter control circuits do not share a common ground, such as isolated converter cells supplied from different power sources.

2.3.2 The Output Perturbation Implementation

The *output perturbation implementation* shown in Fig. 2.3 uses small sinusoidal perturbations in the cell output currents to encode current-sharing information. Each cell computes an estimate of the

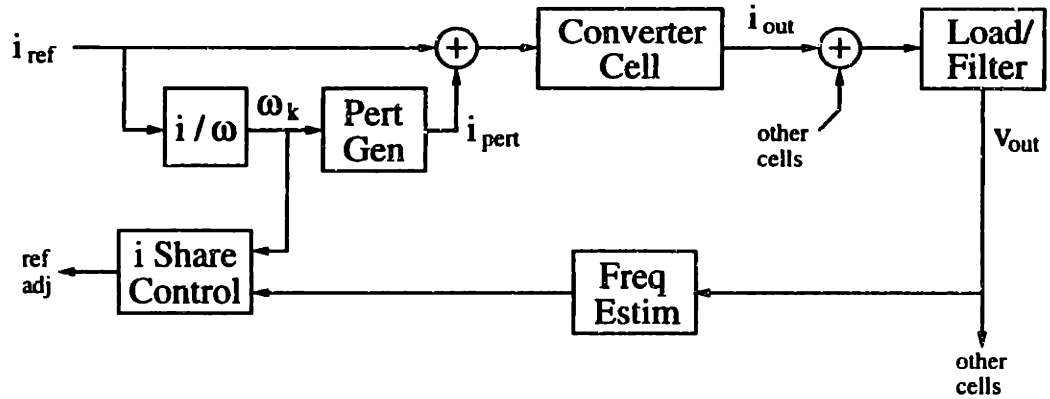


Figure 2.3 Schematic of the output perturbation implementation of frequency-based load-sharing control.

average output of all cells from the resulting aggregate perturbation in output voltage, which is locally measurable by each cell. This information, which can be computed using the same methods as employed in the isolated single connection implementation, is then used to achieve load balance among cells. The perturbation frequency range is typically selected to be well above the output voltage control bandwidth of the system, but well below the switching frequency. The needed perturbations in output current are easily generated in converters under current-mode control, and only very small perturbations in output current (and voltage) are necessary to communicate current-sharing information. The output perturbation implementation achieves current balance control using only variables measured locally at each converter cell, with no inter-cell connections for current-sharing. No additional power processing components or sensors are needed to communicate the current-sharing information across the output bus. This yields a potential reliability advantage over systems that require additional interconnections.

The use of the output bus to communicate current-sharing information has other interesting characteristics. For example, conditions which disrupt the distribution of current-sharing information (such as output short circuits) generally cause enough of a voltage error to drive all of the converters to full current, making current-sharing temporarily unnecessary. Furthermore, faults in an individual cell which cause it to be removed from operation (such as by the output fuse blowing) automatically prevent it from affecting current sharing among the remaining converter cells. These characteristics yield a current-sharing approach which is potentially very robust. The major challenges to implementing the approach are the selection of an appropriate perturbation magnitude and frequency range, and the design of appropriate estimation circuitry. These challenges will be directly addressed in Chapter 3, where a low-power prototype system employing the output perturbation implementation is presented.

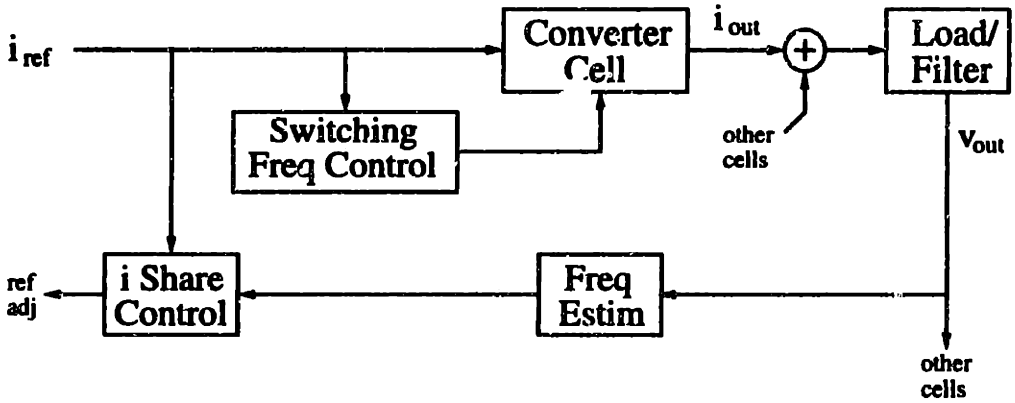


Figure 2.4 Schematic of the switching ripple implementation of frequency-based load-sharing control.

2.3.3 The Switching Ripple Implementation

The *switching ripple implementation* shown in Fig. 2.4 is similar to the output perturbation method, except that the switching ripple of the cell is used as the perturbation source. Each converter cell is controlled such that its average output current (or some other variable to be regulated) is directly related to its switching frequency. Each converter can locally measure the aggregate switching harmonics at the output, and use the information in the switching harmonics to achieve load balance with the other converter cells. This approach has the benefit that no additional ripple is injected into the output to encode current sharing information, and the information is communicated at the switching frequency (i.e., with high bandwidth).

Controlling the switching frequency of the converters is typically straightforward. For many converter types, there is a natural relation between switching frequency and control variables such as output current. Converter control strategies which do not exhibit such a relation can often be modified to achieve it. For example, such a relationship can be implemented in fixed-frequency PWM converters by modifying the clock frequency as a function of output current.

Estimating an average value for the current (or frequency, or other control variable) from the aggregated output harmonics is a more delicate task. Because the switching harmonic content of a single converter operating at any frequency/current is known, information about the average can clearly be extracted from the output voltage. However, the existence of (possibly large) harmonics of the fundamental ripple current from each cell makes the estimation task more complicated than that for other methods. Nevertheless, as will be demonstrated in chapter 4, some very simple estimation and control structures exist which are well suited for implementing the switching ripple method of current sharing.

2.4 Frequency Estimation

To reduce this new frequency-based current-sharing approach to practice, a means of estimating an average frequency ω_{rms} from the aggregate signal using simple, inexpensive circuitry is needed. Many different types of weighted estimates and estimator structures suited to this task are possible. This section considers the realization of an rms frequency estimator in which the estimated frequency ω_{rms} is the rms of the individual frequencies. This estimator structure is suitable for both the isolated interconnection and output perturbation implementations of frequency-based current sharing control.

Consider the aggregate current-sharing signal $x(t)$, which is made up of a group of N sinusoids $x_k(t)$ of frequencies ω_k, $k = 1,..., N$. The frequency of an individual sinusoid encodes information about the output current of a particular cell, while the rms frequency of the aggregate signal can be used to effect current-balancing control. The weighted rms frequency for all of the sinusoids is defined as:

$$\omega_{rms} = \frac{\sqrt{\sum_{k=1}^{N} c_k^2 \omega_k^2}}{\sqrt{\sum_{k=1}^{N} c_k^2}} \tag{2.1}$$

where the c_k's are weighting coefficients for different frequencies. For equal weighting, the c_k's can be considered equal to a single (arbitrary) constant. The power spectrum of $x(t)$ is:

$$S_x(\omega) = 2\pi \sum_{k=1}^{N} \frac{1}{2} |X_k|^2 [\delta(\omega - \omega_k) + \delta(\omega + \omega_k)] \tag{2.2}$$

where we have assumed that all of the $x_k(t)$'s are at separate frequencies. The violation of this assumption affects the weightings in the rms frequency estimate, but does not interfere with the overall operation of the current-sharing system. The rms value of $x(t)$ is then:

$$x_{rms} = \sqrt{\frac{1}{2\pi} \int_{-\infty}^{+\infty} S_x(\omega) d\omega} = \sqrt{\sum_{k=1}^{N} |X_k|^2} \tag{2.3}$$

If we pass the signal $x(t)$ through a filter with frequency response $H(\omega)$ to form a signal $y(t)$, we find the new signal $y(t)$ has the properties

$$S_y(\omega) = 2\pi \sum_{k=1}^{N} \frac{1}{2} |H(\omega_k)|^2 |X_k|^2 [\delta(\omega - \omega_k) + \delta(\omega + \omega_k)] \tag{2.4}$$

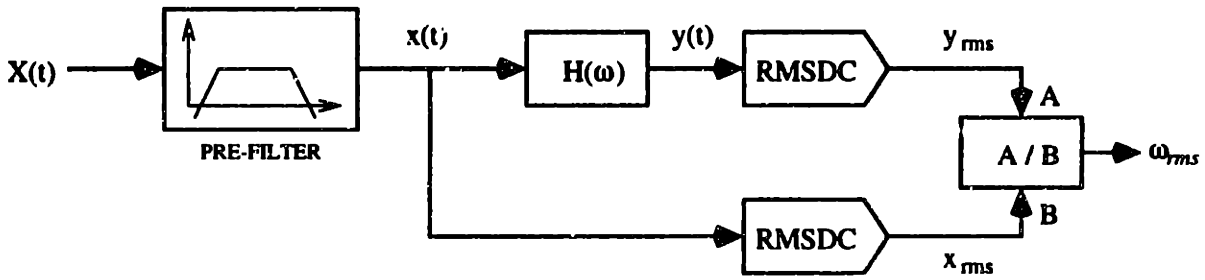


Figure 2.5 An approach for calculating the weighted rms frequency estimate of the aggregate signal. This approach is easily implemented in analog or digital hardware.

and

$$y_{rms} = \sqrt{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_y(\omega)d\omega} = \sqrt{\sum_{k=1}^{N} |H(\omega_k)|^2 |X_k|^2} \,. \tag{2.5}$$

Now consider the estimator implementation shown in Fig. 1. If we choose the filter $H(\omega)$ to be a differentiator over the encoding frequency range ($H(\omega) = j\omega$), we find that the ratio of the rms value of $y(t)$ to the rms value of $x(t)$ has the form of the desired rms frequency estimate (1), with the signal magnitudes as the weighting coefficients. This result means that the desired rms frequency estimate can be easily computed using simple analog or digital hardware. The rms frequency estimate can be calculated with analog circuitry using two (integrated circuit) rms-to-dc converters, a differentiator, and a divider. Alternately, the estimate can be computed digitally by sampling $x(t)$ and performing the equivalent calculations in software. We conclude from these results that if the individual cells encode information about their output current in the frequency of a signal, then information about the average output of all the cells can be easily extracted from the aggregate signal with very simple hardware.

It should be noted that these results have been derived for computations on fixed-frequency signals over all time. However, computation of these rms quantities over a sliding window allows the frequency content (and hence the current-balance information) to be tracked over time. The next section addresses the use of practical rms-to-dc converters for this purpose, and shows the effects of the averaging time constant of the rms-to-dc converters on frequency resolution and response speed.

2.5 Rms-To-Dc Conversion

This section addresses the application of practical rms-to-dc converters to the computations outlined in the previous section. Most integrated circuit rms-to-dc converters either explicitly or implicitly

calculate the rms value of a signal $f(t)$ as

$$f_{rms}(t) = \sqrt{LPF\{f^2(t)\}} \tag{2.6}$$

where *LPF* denotes a low-pass filtering operation, typically using a first or second order filter. We will focus on the effects of computing the mean square using this technique; the rms value is merely the square root of this. We define the weighted mean square of a signal $f(t)$ with respect to a weighting (or windowing) function $w(t)$ as

$$f_{wms} = \frac{\int_{-\infty}^{\infty} [w(\tau)\, f(\tau)]^2 d\tau}{\int_{-\infty}^{\infty} w(\tau)^2 d\tau} \; . \tag{2.7}$$

For the conventional mean square value f_{ms}, we use the weighting function

$$w_T(\tau) = \begin{cases} 1 & -\frac{T}{2} < \tau < \frac{T}{2} \\ 0 & otherwise \end{cases} \tag{2.8}$$

and take the limit as $T \to \infty$, which yields

$$f_{ms} = \lim_{T \to \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(\tau)^2 d\tau \; . \tag{2.9}$$

Now consider calculating the "computed mean square" of a signal $f(t)$ using a first-order butterworth filter with time constant τ_1. This filter has an impulse response

$$h(t) = \frac{1}{\tau_1} e^{-t/\tau_1} u(t) \tag{2.10}$$

which yields a computed mean square of $f(t)$

$$
\begin{aligned}
f_{cms}(t) &= f^2(t) * h(t) \\
&= \frac{1}{\tau_1}\int_{-\infty}^{t} e^{(\tau - t)/\tau_1} f^2(\tau)\,d\tau \\
&= \frac{1}{\tau_1}\int_{-\infty}^{\infty} [e^{(\tau - t)/(2\tau_1)} u(t - \tau) f(\tau)]^2\,d\tau
\end{aligned}
\qquad (2.11)
$$

Examining the form of the last line of **(2.11)**, we see that $f_{cms}(t)$ is equivalent to the weighted mean-square computation **(2.7)**, with weighting function

$$
w_c(\tau) = e^{(\tau - t)/(2\tau_1)} u(t - \tau)\ . \qquad (2.12)
$$

The fact that the weighting function is zero for values of τ greater than t makes physical sense, since computations in the actual circuit can only be based on past values of the input signal. This weighting function places a weight of one on the present value of the input signal, with weights for past times decaying exponentially to zero with time constant $2\tau_1$. Thus, the longer the time constant $2\tau_1$, the more heavily the past values of the input signal are weighted, and the slower the system responds to changes in the input.

The impact of computing the mean square as in **(2.11)** can also be examined from a frequency resolution point of view. This is important, since mean-square computations in the frequency-encoding method are typically made on signals composed of closely-spaced discrete frequency components. Applying Parseval's relation to **(2.7)**, we find

$$
f_{wms} = \frac{1}{(2\pi)^2 E_w}\int_{-\infty}^{\infty} |W(j\omega) * F(j\omega)|^2 d\omega \qquad (2.13)
$$

where E_w is the energy in the weighting function $w(t)$. From the frequency domain point of view, the mean square reflects the true content of $F(j\omega)$ to the extent that its content is not changed by convolution with $W(j\omega)$. The Fourier transformation of the conventional weighting function from **(2.8)**, $W_T(j\omega)$, is a sinc function with mainlobe width $\Delta\omega = 2\pi/T$. Thus, the conventional mean-square calculation accurately reflects the spectral content of $f(t)$ to within a resolution of approximately $2\pi/T$, and resolves frequencies with arbitrary accuracy as $T \to \infty$.

We now consider practical computation of the mean square using the weighting function of **(2.12)**, which has the transform

$$W_c(j\omega) = \frac{2\tau_1 e^{-j\omega t}}{1 - j2\tau_1\omega} \tag{2.14}$$

where τ is treated as time, and t is a constant parameter. The magnitude of this weighting function frequency response is plotted in Fig. 2.6. From this, we see that the effect of the weighting function is to "smear" the spectral content of $F(j\omega)$ by an amount depending on τ_1. There will be significant overlap and loss of resolution among spectral components of $F(j\omega)$ which are closer than roughly $3/\tau_1$ to $5/\tau_1$ apart. The spectral smearing caused by the weighting function affects the computation of the mean square, and limits the frequency resolution of a practical estimator.

Thus, practical rms-to-dc converters of the type (2.6) allow changes in spectral content to be tracked across time, while limiting the frequency resolution of the computation. Both tracking response speed and frequency resolution are controlled by the filter time constant τ_1, and must be traded off against one another in the design process. Similar design issues can be expected to arise in other approaches to the problem, such as with the use of higher order filters or with discrete-time implementations of the mean-square computation.

2.6 Conclusion

This chapter has presented a new method for achieving current-sharing among paralleled converters, based on frequency encoding of the needed information. Different implementation methods have been described, and one method of performing the frequency estimation task has been analyzed. The new approach has significant advantages over existing methods, including the ability to galvanically isolate or eliminate the current-sharing connections among cells and the freedom to select the frequency range over which information is communicated.

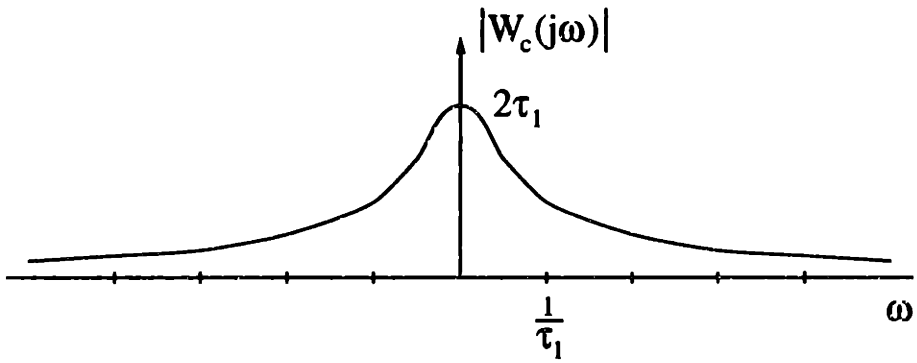


Figure 2.6 Frequency response magnitude plot for the weighting function of (2.12).

It should be pointed out that other approaches to current-sharing are possible which are similar to those presented here and which share some of the same advantages. For example, encoding and communicating current-sharing information on the *amplitudes* of *fixed-frequency* (and phase) signals can be employed to achieve galvanic isolation of current-sharing control circuits. Alternatively, frequency encoding of variables other than current or use of other estimation and control structures may be desirable for some applications. It may be expected that frequency-encoding and similar approaches to current sharing will have advantage whenever fault tolerance and high reliability are important system requirements.

Chapter 3

Implementation and Evaluation of the Output Perturbation Method of Current Sharing

This chapter presents the implementation and experimental evaluation of the output perturbation method of current sharing introduced in chapter 2. This technique is based on frequency encoding of the current-sharing information, and requires no inter-cell connections for communicating this information. Practical implementation of the approach is addressed, and an experimental evaluation of the approach based on a three-cell prototype system is also presented. It is shown that accurate and stable load sharing is obtainable over a wide load range with this approach.

3.1 Introduction

We consider the output-perturbation method of current-sharing control proposed in Chapter 2. In this method, each cell superimposes a small, high-frequency perturbation onto its output current. The magnitude and frequency of the perturbation is controlled as a function of the cell reference current (or some other variable to be regulated). The frequency content of the output voltage perturbation resulting from the aggregated current perturbations contains information about the cell output currents, and is measurable by each cell.

To effect current sharing, each cell employs a frequency estimator to calculate a weighted rms average, ω_{est}, of the output perturbation frequency content. This estimate has the form

$$\omega_{est} = \frac{\sqrt{\sum_{k=1}^{N} c_k^2 \omega_k^2}}{\sqrt{\sum_{k=1}^{N} c_k^2}} \tag{3.1}$$

where c_k and ω_k are the magnitude and frequency of the output perturbation due to the k^{th} cell. Each cell compares its own perturbation frequency to the estimated average and adjusts its output such that its own

perturbation frequency approaches the average. As the individual perturbation frequencies approach a single average value, the individual output currents will also approach a single value, achieving the desired load balance. For example, in a dc output supply, load balance can be achieved if each cell adjusts its local reference voltage to minimize the difference between the local perturbation frequency and the estimated rms frequency.

3.2 An Experimental Converter System

Here a full implementation of this current-sharing scheme is presented which uses low-power buck converter cells operating under current-mode control. In simplest terms, each cell can be viewed as having an inner current control loop, a middle voltage control loop, and an outer load-sharing control loop. Implementation of the outermost loop with the perturbation method requires that each cell encode information about its current onto the output (via a perturbation generator) and decode the aggregated information from the output (via a frequency estimator). Methods and circuits will be described for generating the proper perturbation signals, estimating the rms perturbation frequency from output voltage measurements, and controlling the load balance among cells. The structure of an individual cell implementing the perturbation method is shown in Fig. 3.1. The converter cell power stage generates an output current whose peak value is equal to the peak commanded current i_{cmd}. The commanded current is the sum of a reference current i_{ref}, generated by the output voltage controller, and a perturbation signal i_{pert}, generated by the perturbation generator circuit. The output voltage controller generates i_{ref} based on the difference between the output voltage v_{cf} and the reference voltage v_{ref} . The load-sharing controller adjusts v_{ref} based on the difference between the local perturbation frequency and the rms perturbation frequency calculated by the frequency estimator circuit. These subsystems operate together to regulate the output voltage while maintaining the desired load balance among cells.

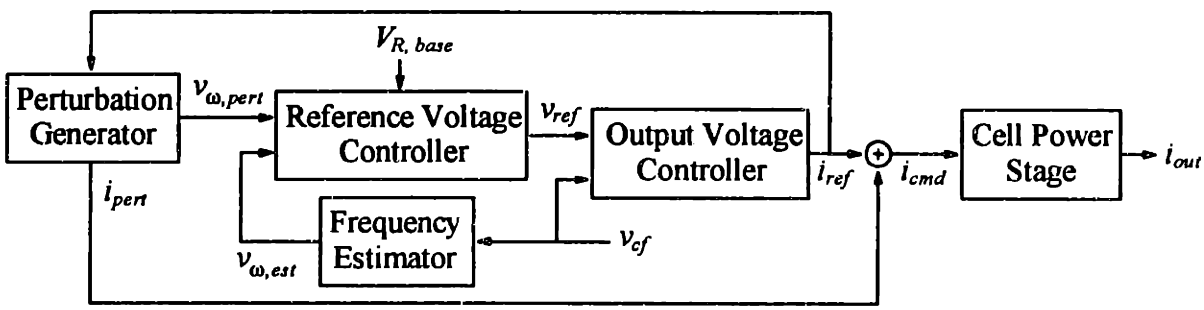


Figure 3.1 Block diagram of the control structure for a cell.

3.2.1 Prototype System Power Stage

A three-cell low-power buck converter system was constructed as a test bed. The buck converter system is designed to regulate the output to an adjustable reference of approximately 5.1 V from an input voltage of approximately 15 V. Each cell is designed to supply a full load output current of 25 mA, yielding a total load range of 5 to 75 mA. The system has an output filter capacitance of 0.33 μF, and is resistively loaded.

The buck converter cells ($f_{sw} \approx 200$ kHz, $L \approx 125$ mH) are operated under current-mode control using the UC3843 current-mode control chip. Figure 3.2 shows a schematic of the cell power stage and its associated current-mode control circuitry. The top transistor of the UC3843 output drive stage is used as the active power switch. The internal current-sense comparator and error amplifier of the UC3843 are overridden and replaced with external circuitry to allow direct control of the commanded peak turn-off current, i_{cmd}. The commanded peak current is the sum of a reference current I_{ref} (generated by the output voltage controller) and a perturbation signal I_{pert} (generated by the perturbation generator).

3.2.2 Perturbation Generation

To encode the current-sharing information, the perturbation generator implements an incrementally linear relationship between cell reference current and perturbation frequency, with cell currents from no load to full load yielding perturbation frequencies from 5 to 10 kHz. The perturbation frequency range is selected to be well below the 200 kHz cell switching frequency, but well above the output voltage control bandwidth of the system (~100 Hz). The perturbation magnitude is selected to be proportional to the perturbation frequency, with a maximum magnitude of approximately 0.25 mA at 10 kHz. This is done to yield output voltage perturbation magnitudes (across the capacitive output filter) which are approximately constant with frequency. The selected magnitude range yields very small (<1%) output voltage ripple for the three-cell system.

The perturbation generator is easily implemented using an Exar XR2206 monolithic function generator and an LF347 quad op amp as shown in Fig. 3.3. The XR2206 contains a voltage-controlled oscillator (VCO) and sine-wave shaping circuitry. The VCO input allows control of the perturbation frequency, and an amplitude modulation input allows easy control of the perturbation magnitude. The op amp circuitry is used to set up the proper bias voltages and gains for the XR2206 inputs and to filter out the dc component of its output. The resulting perturbation signal is superimposed on the reference current, and the result is supplied to the current-mode PWM controller.

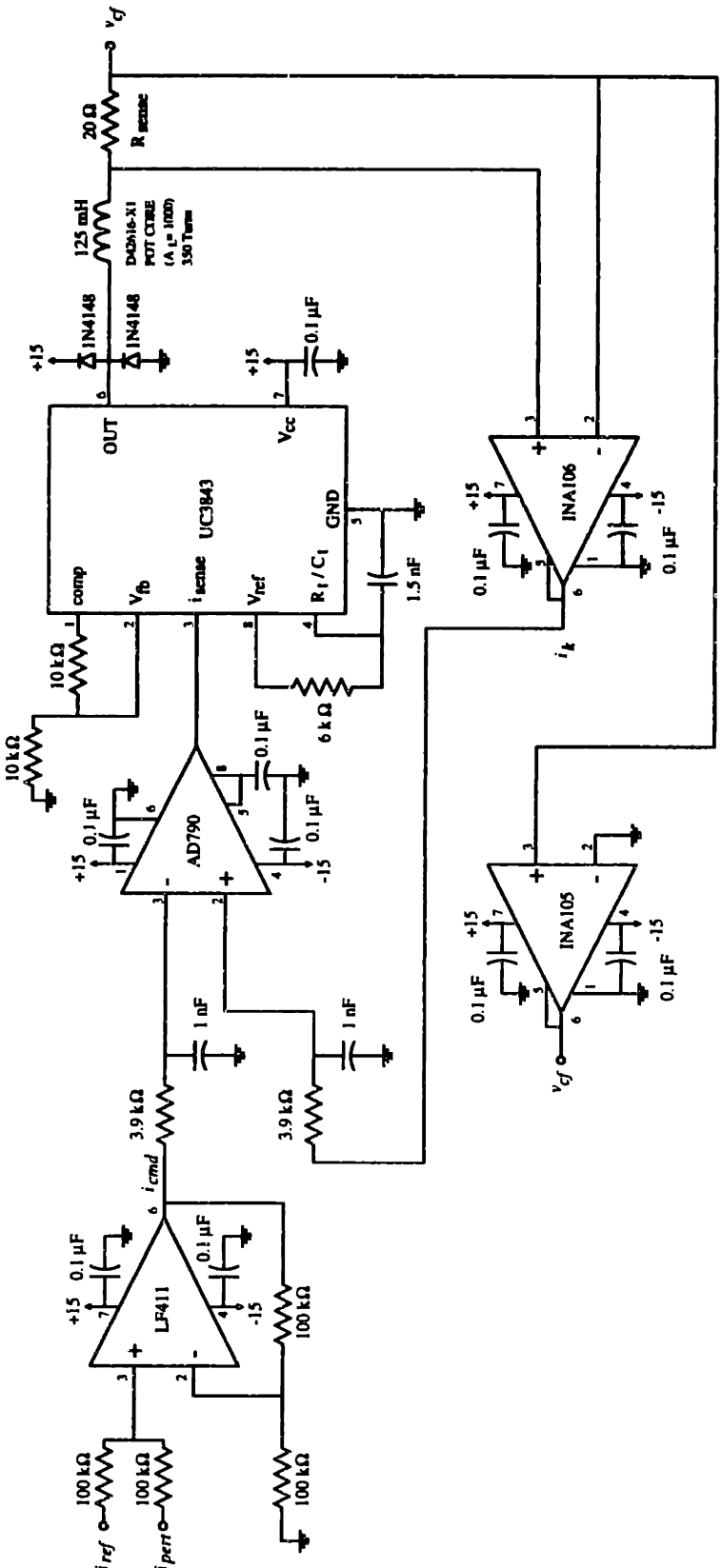


Figure 3.2 Cell power stage schematic for the prototype converter system which implements the output perturbation method of current sharing.

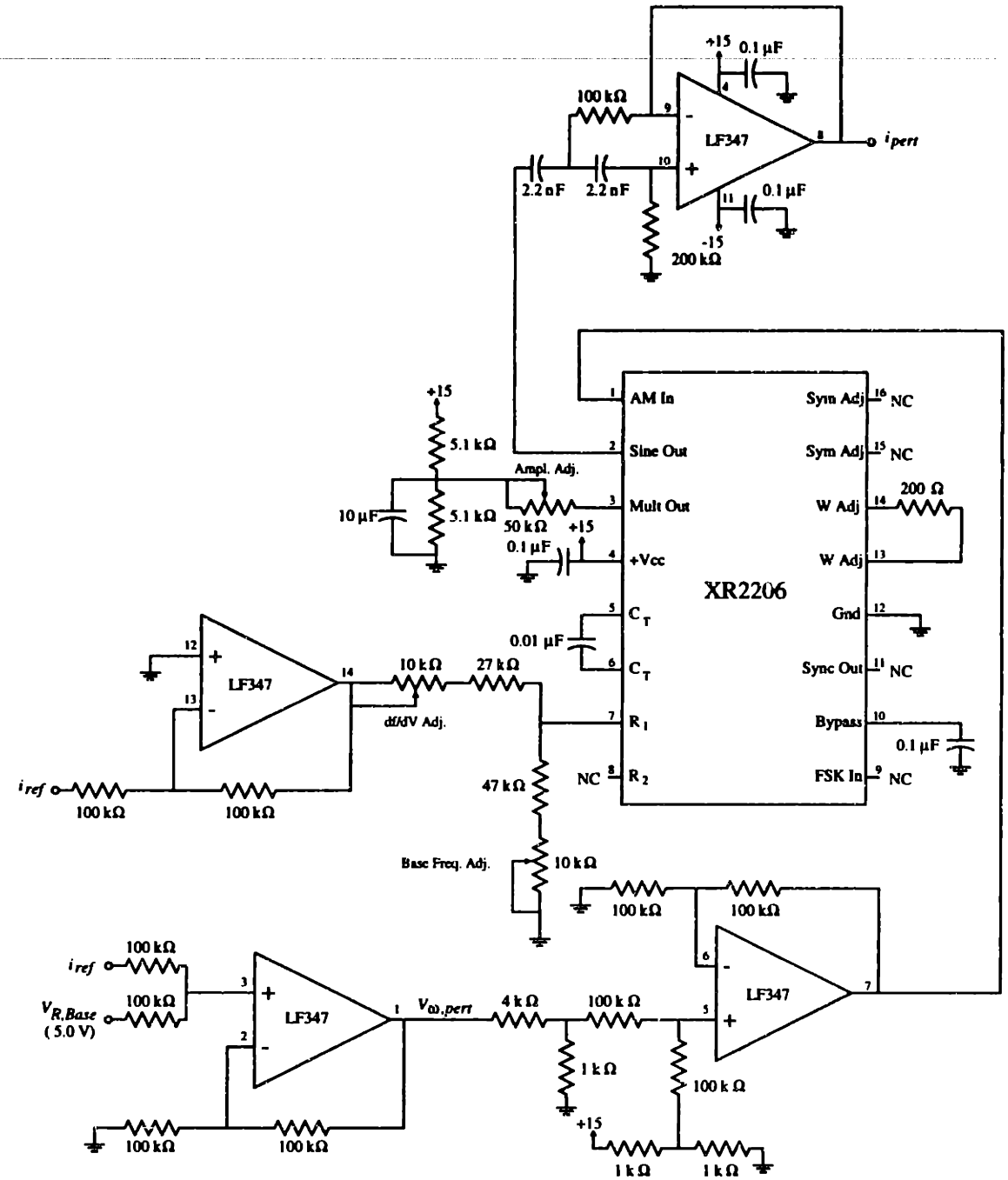


Figure 3.3 Schematic of the perturbation generator circuit used in the prototype system.

An alternative perturbation generator which allows arbitrary perturbation waveforms to be generated at the expense of complexity and higher chip count was also developed and tested in the system. In this implementation, shown in Fig. 3.4, an AD654 voltage-controlled oscillator is used to generate the clock signal for a counter. The counter output is used to address a ROM which contains the digitized perturbation waveform. The ROM output is in turn fed to an AD7524 multiplying D/A converter (DAC)

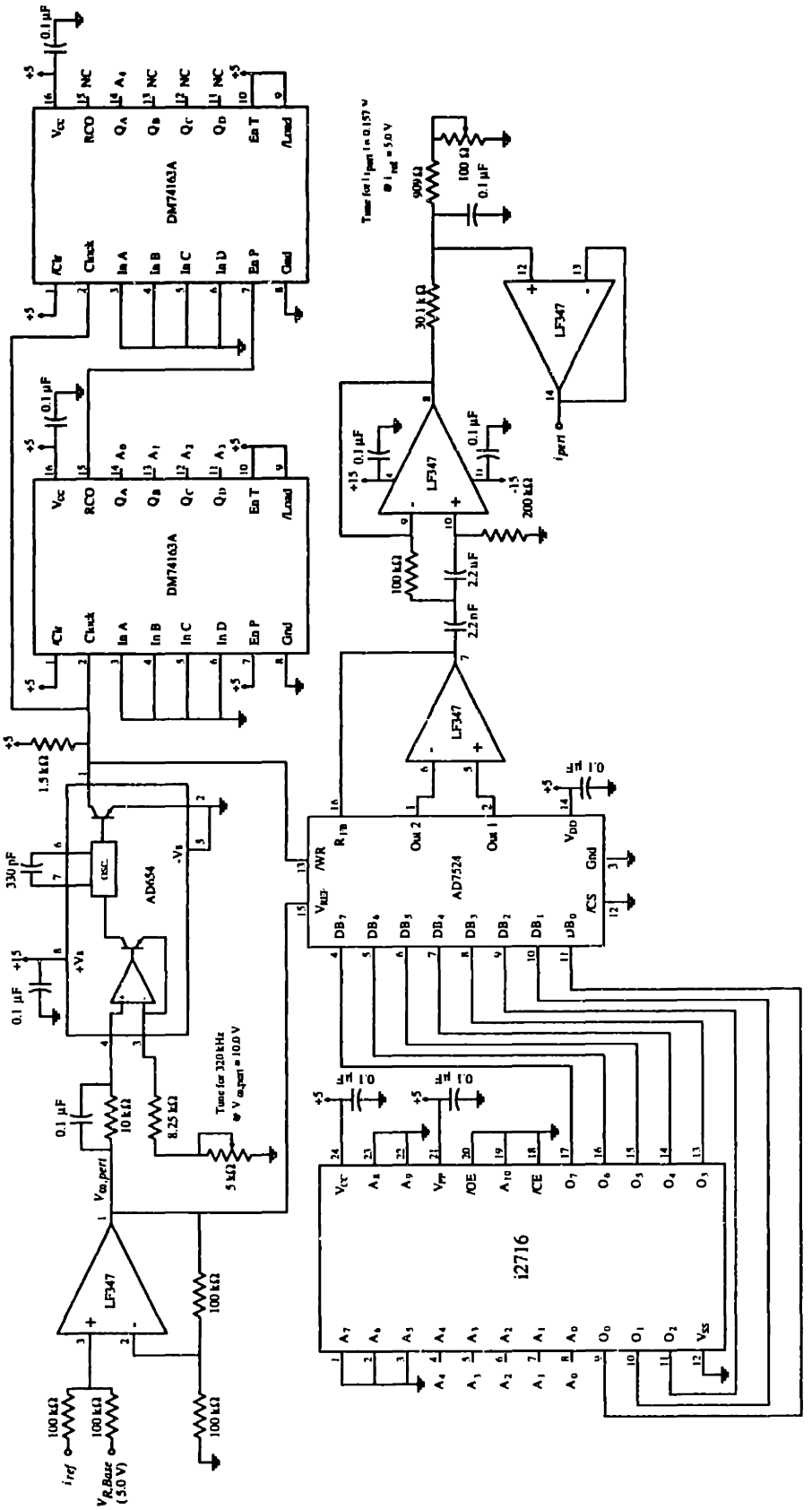


Figure 3.4 Schematic of an alternative perturbation generator circuit.

which generates the perturbation waveform. The frequency of the generated perturbation is controlled by the magnitude of the VCO input, while the magnitude of the perturbation is controlled via the multiplying input of the DAC.

3.2.3 Frequency Estimation

To achieve load balance, each cell compares its own perturbation frequency to the rms of all the perturbation frequencies. The rms perturbation frequency is estimated from the output voltage using the structure of Fig. 3.5, with $H(\omega) = j\omega$. This estimator structure was introduced and analyzed in Chapter 2. The estimator circuit is composed of four sections: (1) a bandpass filtering stage, (2) a gain and band-limited differentiation stage, (3) an integrated circuit rms-to-dc conversion stage, and (4) a division stage.

The bandpass filtering stage is shown in Fig. 3.6. It is implemented as a cascade of a second-order high-pass Butterworth filter, a fixed gain, and a second order low-pass Butterworth filter. The corner frequencies are set to 500 Hz and 20 kHz, in order to block out both the low-frequency and switching-frequency components of the output voltage. The passband gain of 10 amplifies the perturbation signal.

The gain and differentiation stage and the rms-to-dc conversion stage are both shown in Fig. 3.7. The gain and differentiation stage consists of a gain path and a differentiator path. The differentiator path contains a band-limited differentiator circuit which generates the derivative for frequency components in the range of interest, but is gain limited above approximately 50 kHz to limit the amplification of high frequency noise. The gains of this stage are set to keep the intermediate computation signals in range and to yield a scaling factor of 1 V/kHz in the final output. The rms-to-dc conversion stage (also in Fig. 3.7) is implemented using AD637 integrated circuit rms-to-dc converters connected in the two-pole Sallen-Key filter arrangement. The averaging and filter capacitor values (C_{AV} = 0.022 μF, $C_2 = C_3 = 0.047\mu F$) are selected to yield a 1% settling time of 8 msec, which represents a reasonable tradeoff between frequency resolution and response speed (see Chapter 2 for an analysis of

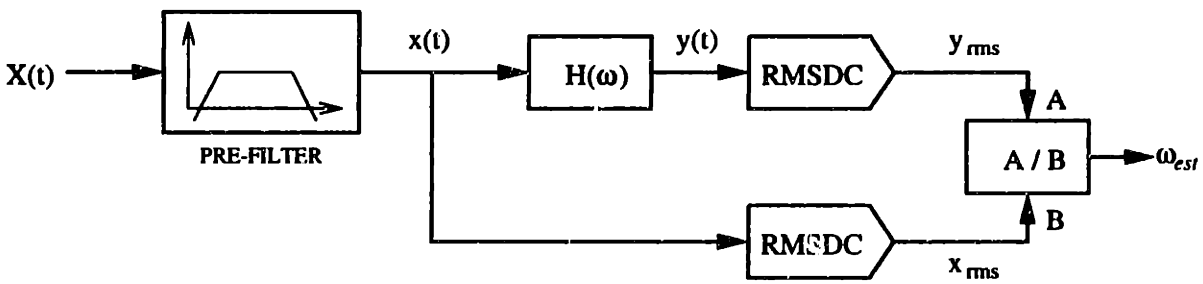


Figure 3.5 An approach for calculating the weighted rms frequency estimate of the aggregate perturbation signal.

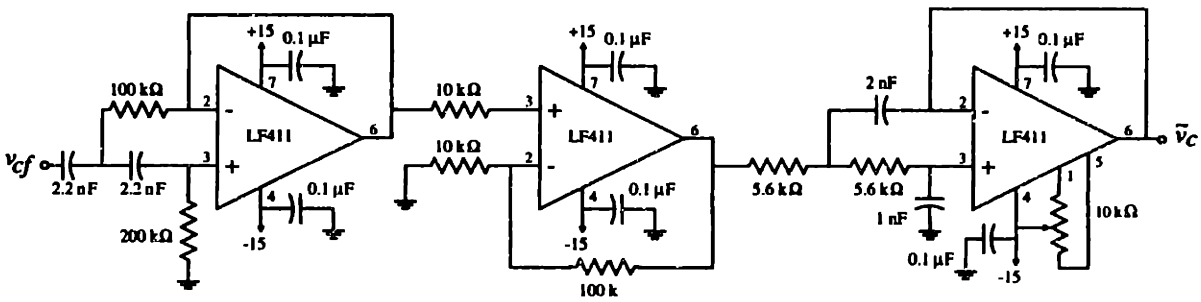


Figure 3.6 The bandpass filtering stage of the prototype frequency estimator.

this tradeoff).

The division stage is shown in Fig. 3.8, and is composed of a four quadrant multiplier placed in the feedback path of an operational amplifier. (The Exar XR-2208 Operational multiplier contains both the four-quadrant multiplier and an operational amplifier in a single monolithic package.) This approach is typically less expensive than the use of a logarithm-based division circuit, but requires careful attention to the compensation of the nonlinear feedback loop. The division stage also incorporates an output scale and offset compensation circuit for improved accuracy.

The resulting frequency estimator employs only simple, low-cost circuitry, and has sufficient accuracy to achieve a high degree of current sharing. Alternative approaches to implementing the estimator include sampling the perturbation waveform and performing the equivalent computations in software.

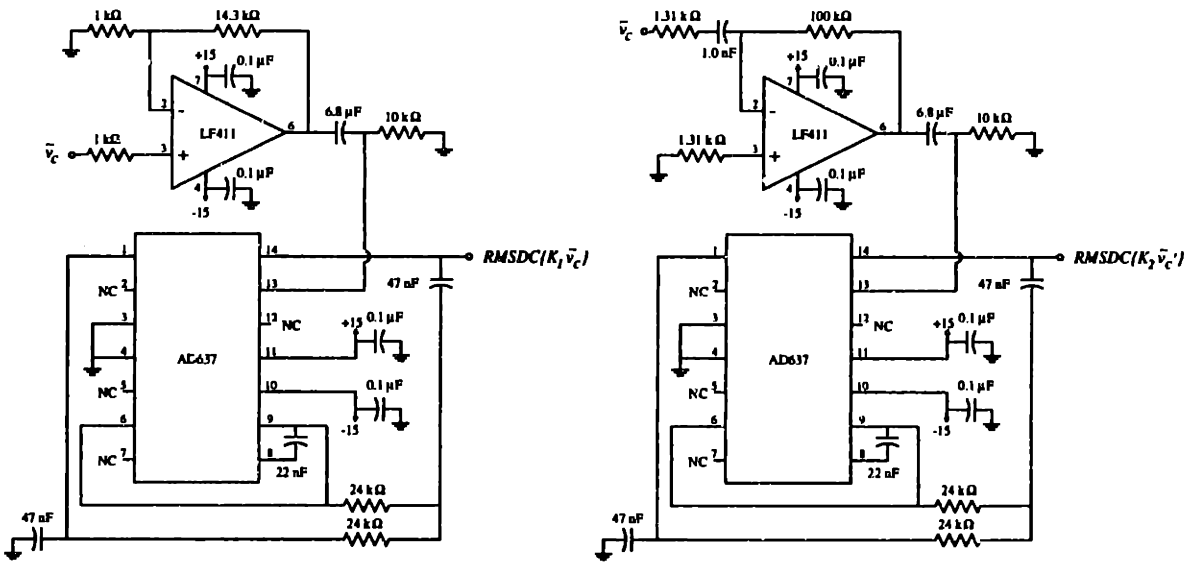


Figure 3.7 The gain and differentiation stage and rms-to-dc conversion stage of the prototype rms frequency estimator.

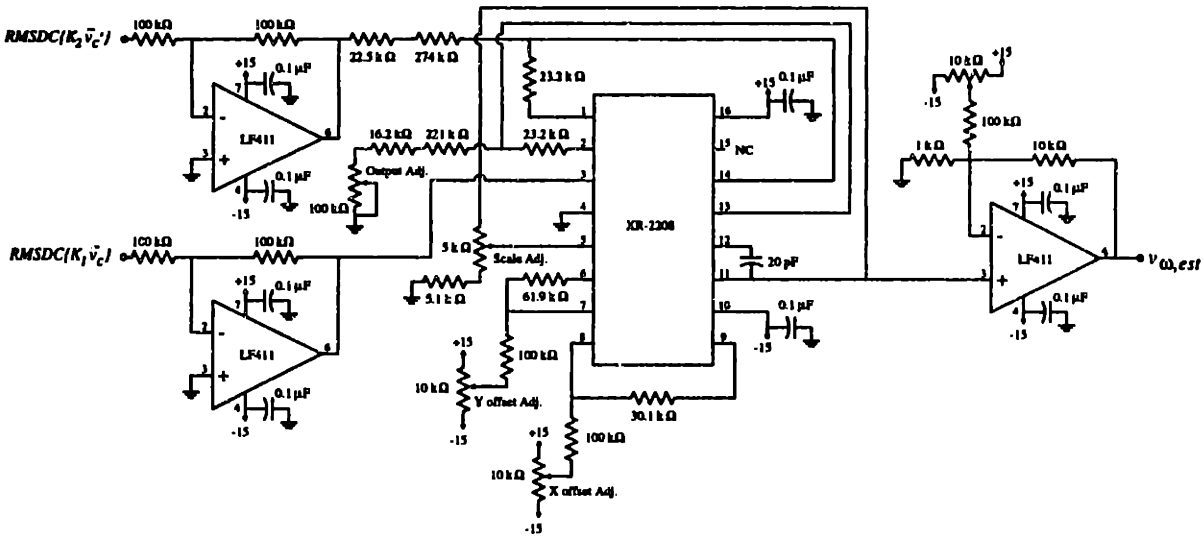


Figure 3.8 The division stage of the prototype rms frequency estimator.

3.2.4 Control Design

This section describes the design of the control circuitry used in the prototype converter system. The task of predicting the output and load-sharing dynamics for cellular converter systems is addressed in Chapter 5. A block diagram of the control structure used in the prototype system is shown in Fig 3.9. Each cell has an inner current loop which causes the cell's peak output current to track a commanded reference (peak current-mode control). (For purposes of clarity, the small perturbation current contributions are neglected in this section. Thus, we will not distinguish between the reference current i_{ref} and the commanded current I_{cmd}.) To regulate the system output voltage, each cell has a middle voltage-control loop which generates the (peak) current reference based on the error between the local reference voltage and the output voltage. To maintain load sharing among cells, each cell has a slow outer load-sharing control loop which adjusts the local reference voltage based on the difference between the local perturbation frequency and the rms perturbation frequency.

For the parameters of the prototype system, an individual cell under peak current-mode control can

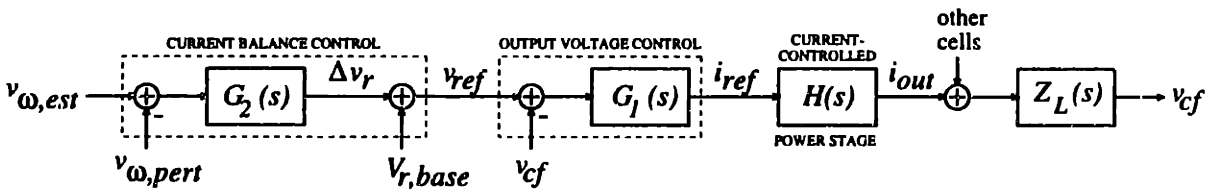


Figure 3.9 A block diagram of the control structure used in the prototype converter system.

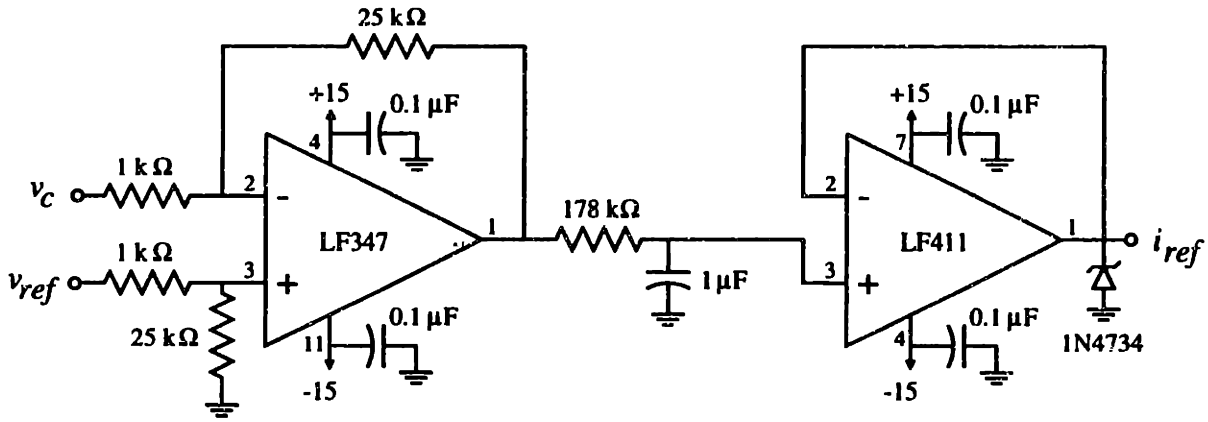


Figure 3.10 The output voltage control compensator used in the prototype system.

be modeled as a controlled current source of the value of the peak commanded current. To see this, consider the following. It can be shown via state-space averaging that the control-to-output transfer function for a single current-mode controlled buck converter cell (equal to $H(s)Z_L(s)$ in Fig 3.9) is

$$H(s)Z_L(s) = \frac{\hat{v}_{cf}}{\hat{i}_{ref}} = \frac{\frac{1}{C}}{s + \frac{RT(1-2D)+2L}{2LRC}} \tag{3.2}$$

where C is the output filter capacitance, R is the load resistance, T is the switching period, and D is the steady-state duty ratio. For the parameters of the prototype system (described in Sec 3.3.1), this is well approximated as

$$H(s)Z_L(s) = \frac{\hat{v}_{cf}}{\hat{i}_{ref}} \approx \frac{\frac{1}{C}}{s + \frac{1}{RC}} = Z_L(s) \quad . \tag{3.3}$$

Thus, the control-to-current transfer function $H(s)$ is approximately unity for the parameters of the prototype system, and we can treat an individual cell under current-mode control as a controlled current source of the value of the peak commanded current.

To achieve output voltage control, a high-gain, single-pole compensator (Gain = 125 mA/V, τ = 0.18 sec) is used to generate the peak commanded current from the error between the reference voltage (v_{ref}) and the output voltage (v_{cf}), as shown in Fig. 3.9. Figure 3.10 shows how this compensator is implemented. The compensator yields an output voltage control bandwidth on the order of tens of Hertz and a small but nonzero cell output impedance.

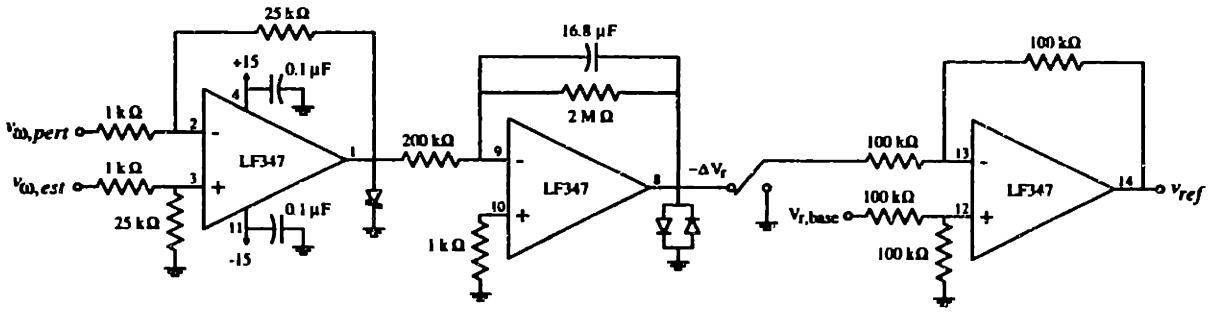


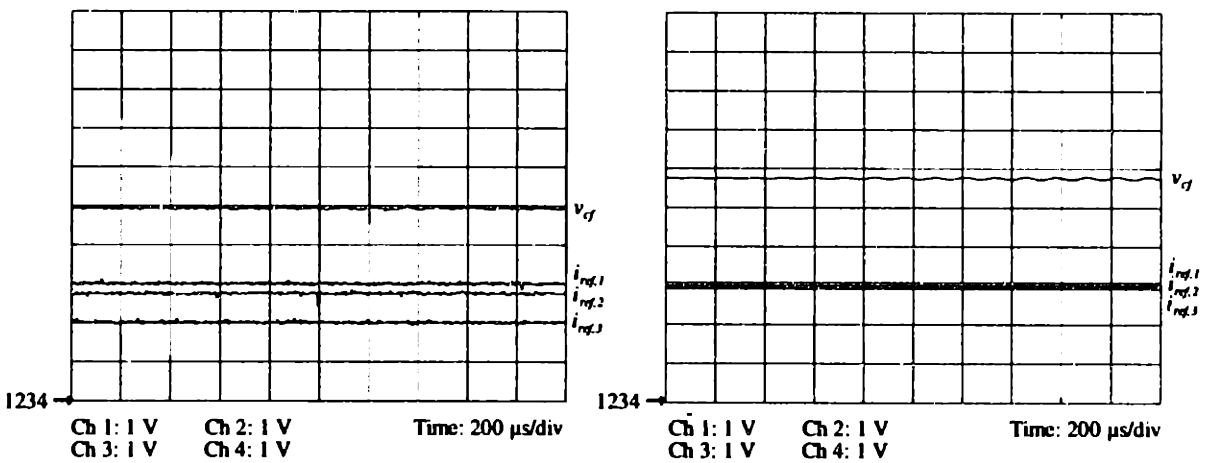
Figure 3.11 The load-sharing compensator used in the prototype converter system.

Load balance among cells is controlled by adjusting the local cell reference voltages within limits about a base value ($V_{r,base}$), as shown in Fig. 3.9. Each cell has a high gain, single-pole compensator (Gain = 10 V/kHz, τ = 33.6 sec) which generates a reference voltage adjustment based on the difference between the estimated rms perturbation frequency and the cell perturbation frequency (Fig. 3.11). This yields a load-sharing bandwidth on the order of Hertz (much slower than the voltage control loop) and a small but nonzero steady-state load-sharing error.

These control loops operate together to properly regulate the output voltage of the system while maintaining the desired load balance among cells. While other design approaches are possible, this multilayered control strategy has been found to be both simple and effective.

3.3 Experimental Results

Here we evaluate the new load-sharing control approach using the 3-cell prototype system described in Section 3.2. Figure 3.12 shows the load-sharing behavior at approximately 60% load both with and



(a) (b)

Figure 3.12 Load-sharing characteristic of the 3-cell prototype system at approximately 60% of full load ($R_{load} \approx 133\Omega$). (a) Without load-sharing control. (b) With load-sharing control.

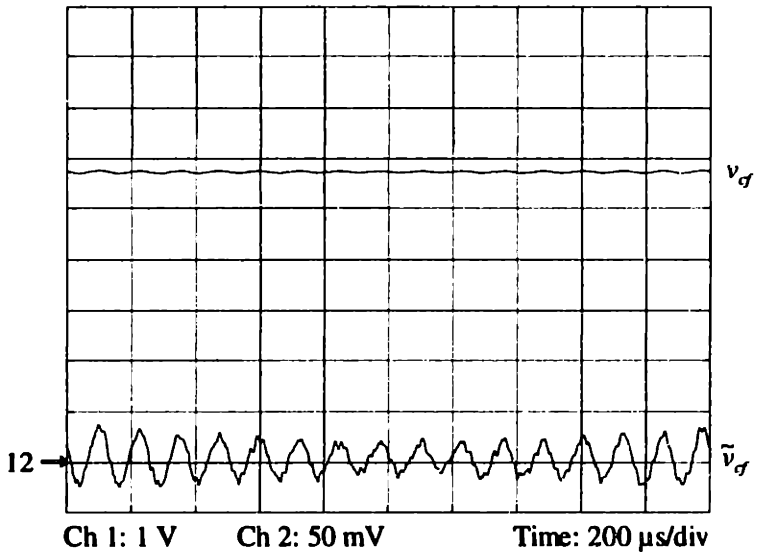


Figure 3.13 The output voltage and its ac perturbation component for the prototype 3-cell system at approximately 60% of full load.

without the load-sharing control. Without load-sharing control, a 3:2 imbalance between the highest and lowest cell currents is observed, with much worse imbalances sometimes occurring depending on the individual cell reference voltages and output impedances. With load-sharing control, the cell currents are all balanced within 3% of their average. (We point out that the perturbation method yields accurate load-sharing *regardless* of how the cells share current without active control.) This high degree of load

Figure 3.14 shows the static load-sharing behavior of the system over the whole load range, while

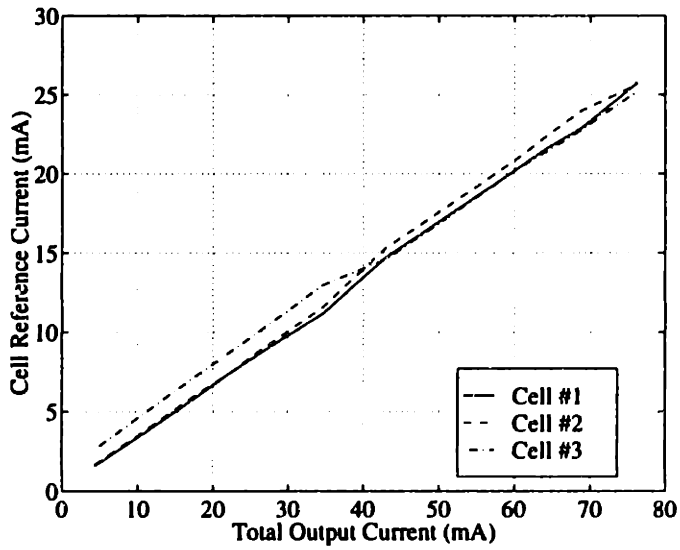


Figure 3.14 Static load-sharing characteristic of the prototype system.

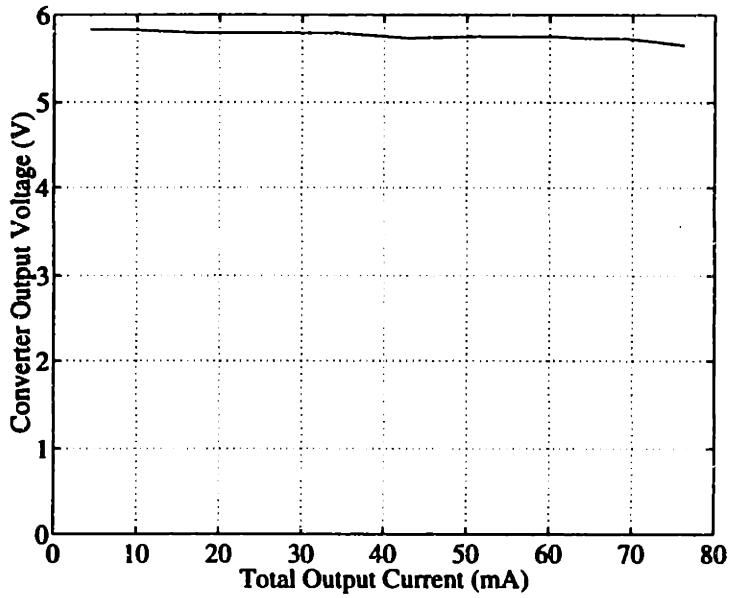


Figure 3.15 Load-regulation characteristic of the prototype system.

sharing is achieved using only very small (<1%) perturbations in output voltage to encode current-sharing information (Fig. 3.13).

Fig. 3.15 shows the load regulation characteristic of the converter system over the load range. The load sharing is quite good over the entire range, but is better at heavier loads both in absolute terms and as a percent of total current. (We point out that while good current sharing is desirable over the whole load range, it is much more important at heavier loads, where the cells are under higher stress.) Current sharing limitations are primarily due to the accuracy of the frequency estimators and the perturbation generators. The frequency estimator circuits have an absolute accuracy of about ±250 Hz over the 5 - 10 kHz range, which corresponds to an absolute current error of about ±1.25 mA. This maximum absolute error becomes more significant as a percentage at lighter loads. Furthermore, the estimators tended to be more accurate at frequencies above 8 kHz, leading to smaller absolute errors at heavier loads. Nevertheless, these results demonstrate that accurate static current sharing can be obtained over a wide load range with this approach.

Load-sharing behavior was also investigated under transient conditions. Figure 3.16 shows the current-sharing behavior for load steps between 681 Ω and 74 Ω, corresponding to approximately 10% and 100% of full load. (Figure 3.17 shows the frequency spectrum of the output voltage perturbations used to achieve current sharing at these load values.) The current-sharing behavior is seen to be very stable for even large load steps. Figure 3.18 shows the response to a current-sharing disturbance for two

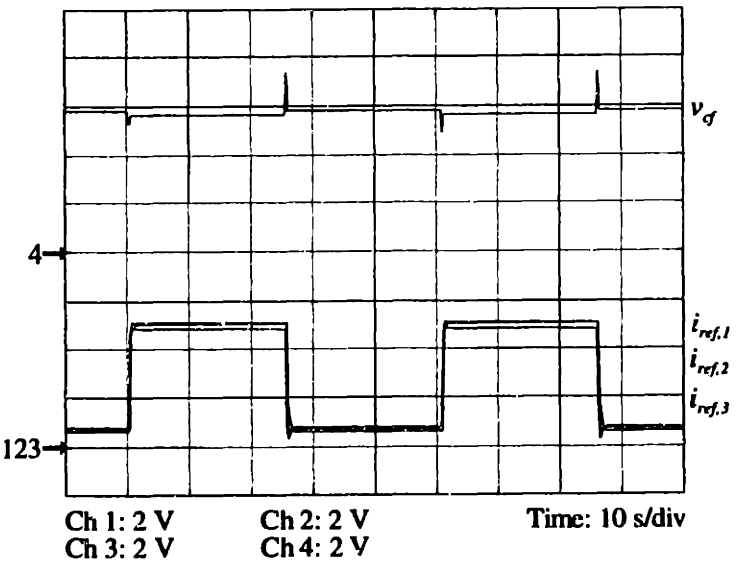


Figure 3.16 Current-sharing behavior for load steps between 681 Ω and 74 Ω (approximately 10% and 100% of full load).

cells operating at approximately 30% of full load. (The disturbance was created by making electrical connections in the compensators.) The dynamic response to current-sharing errors is also seen to be well behaved. What may be concluded from these results (and those in [37-39]) is that the presented output perturbation method can be used to achieve accurate static and dynamic load sharing without the need for additional interconnections among cells.

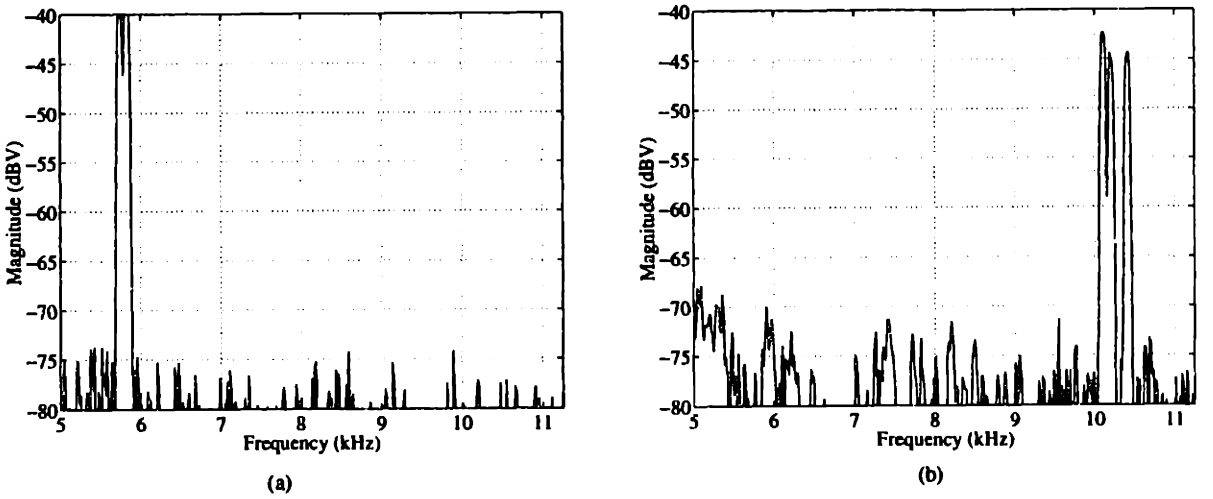


Figure 3.17 Frequency spectra of the output voltage perturbations used to achieve load sharing. (a) R_{load} = 681 Ω (approximately 10% of full load). (b) R_{load} = 74 Ω (approximately 100% of full load).

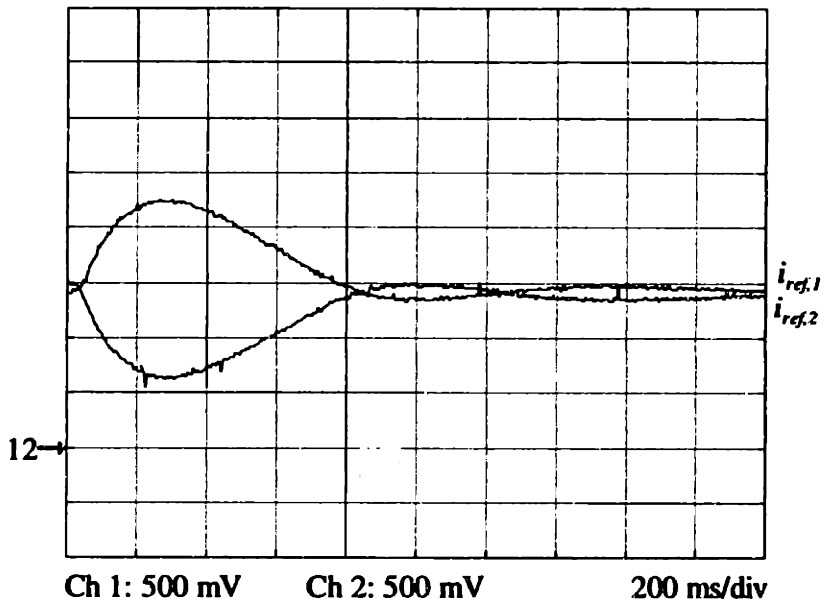


Figure 3.18 Dynamic response to a current-sharing perturbation for two cells operating at approximately 30% of full load.

3.4 Conclusion

This chapter has presented the design and experimental evaluation of a prototype system which implements the output perturbation method of current sharing introduced in chapter 2. The output perturbation method is based on frequency encoding of the current-sharing information, and requires no inter-cell connections for communicating this information. The design of a prototype converter system has been presented, including methods and circuits for generating the perturbation signals, estimating the rms perturbation frequency, and controlling the load balance among cells. Experimental results demonstrating the practicality of the approach have also been presented. Accurate static and dynamic load sharing is obtained over a wide load range using only very small perturbations in output voltage to encode the information. We conclude that the output perturbation method can be implemented with simple circuitry, and allows load sharing to be obtained without the need for additional interconnections among cells.

Chapter 4

Implementation and Evaluation of the Switching Ripple Method of Current Sharing

This chapter explores the switching ripple method of current sharing introduced in Chapter 2. This technique uses information encoded in the output switching ripple to achieve current-sharing among converter cells, and requires no inter-cell connections for this purpose. Practical implementation of the technique is addressed, and two approaches for decoding current-sharing information from output voltage ripple are explored. Experimental evaluation of the switching ripple method based on a low-power prototype system is also presented. It is shown that accurate and stable load sharing is obtainable over a wide load range with this method.

4.1 Introduction

We consider the switching ripple method of current-sharing control proposed in Chapter 2. This approach is similar to the output perturbation method considered in the last chapter, but uses the cell switching ripple as the perturbation source. In the switching ripple method, each converter cell is controlled such that its average output current is directly related to its switching frequency. As a result, the frequency content of the aggregate output ripple voltage contains information about the individual cell output currents. Each cell measures the output ripple voltage, and uses the information it contains to achieve current balance with the other cells (Fig. 4.1).

Implementing a relationship between cell output current and switching frequency is typically straightforward, as many conversion approaches yield a natural relationship between them. For example, controlling a buck converter to operate at the edge of discontinuous conduction results in an inverse relationship between switching frequency and average output current (Fig. 4.2). Conversion approaches which do not exhibit a relationship between output current and switching frequency can often be modified to do so. For example, such a relationship could be achieved in a fixed-frequency PWM converter by adjusting the clock frequency (and PWM ramp slope) as a function of output current.

There are many methods by which the information in the aggregate output ripple voltage can be

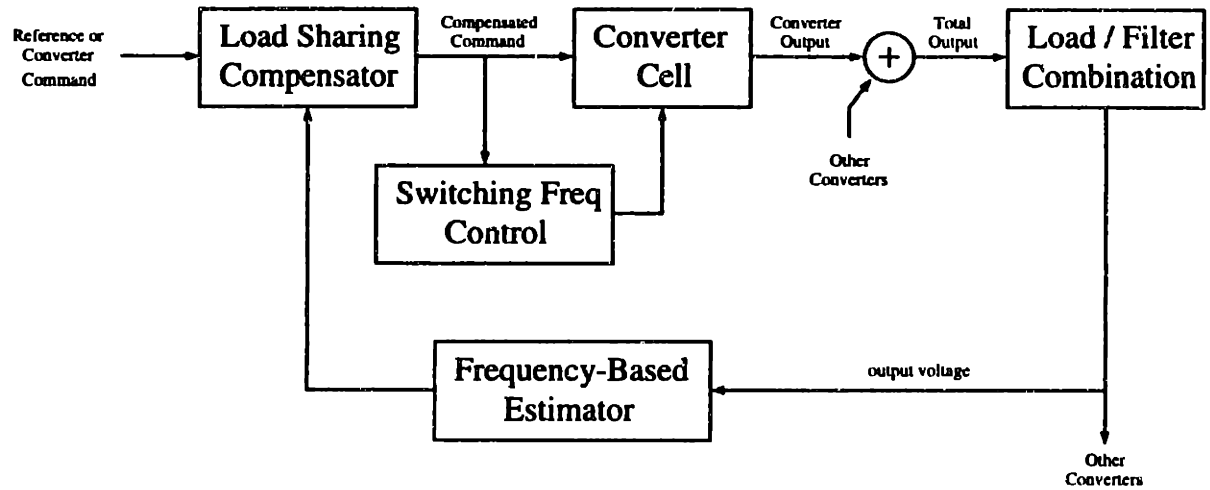


Figure 4.1 Schematic representation of the switching ripple method of current-sharing control.

extracted and used to achieve current sharing. Two such approaches will be considered here. Sections 4.2 and 4.3 consider an approach in which the individual cells adjust their outputs so that their switching frequencies converge on the lowest cell switching frequency, yielding current balance among the cells in the process. Section 4.4 explores an alternative approach in which each cell uses the frequency content of the output voltage ripple to compute an estimate of the rms cell reference current. Each cell adjusts its output to track towards the rms (average) cell current, thereby achieving load balance with the other cells.

4.2 An Implementation Method

This section describes a full implementation of the switching ripple method of current-sharing control. Each cell employs a frequency estimator which generates a positive (differential) signal when any other cell is operating at a lower switching frequency. Each cell uses this information to adjust its output such that no other cell is operating at a lower switching frequency. The cells thus converge to

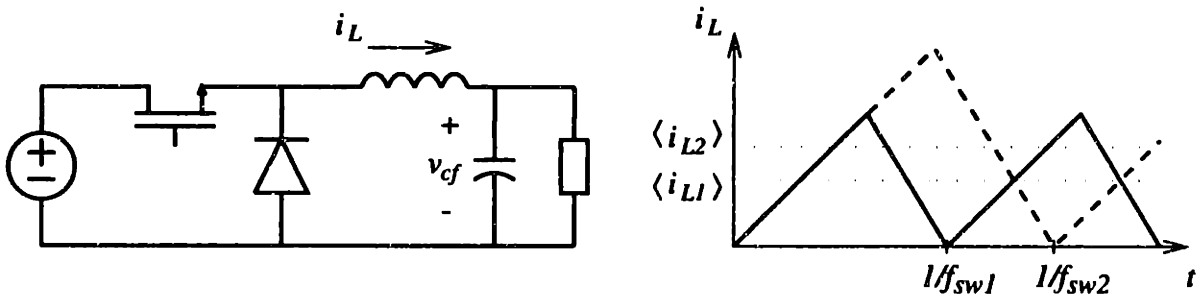


Figure 4.2 A buck converter cell operating at the edge of discontinuous conduction. The switching frequency is inversely proportional to the average output current.

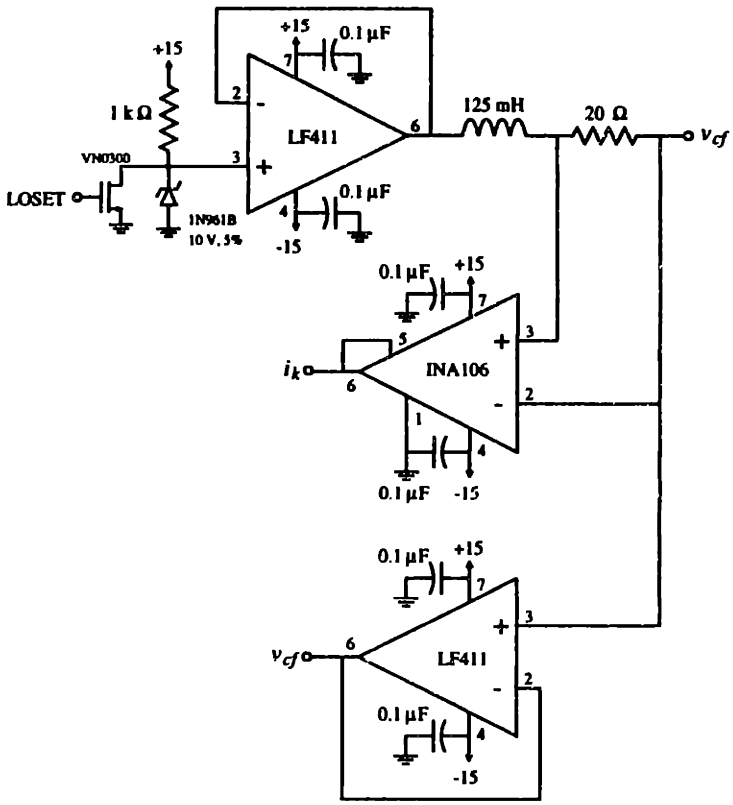


Figure 4.3 Schematic of the cell power stage.

operating at the same switching frequency, and achieve current balance as a result. This approach is both simple and robust, and is insensitive to the switching ripple harmonic content and waveform shape.

The current-sharing approach is demonstrated using a low-power prototype system composed of buck converter cells operating at the edge of discontinuous conduction. Each cell has an inner current control loop, a middle voltage control loop, and an outer current-sharing control loop. The inner current control loop maintains operation of the cell at the edge of discontinuous conduction and inherently enforces a relationship between cell switching frequency and average output current. Current-sharing control is achieved in the prototype system by having each cell adjust its local reference voltage (used by the voltage control loop) if any other cell is operating at a lower switching frequency. Methods and circuits will be described for controlling cell switching patterns, making estimates of switching ripple frequency content based on output voltage measurements, and controlling the output voltage and current balance among cells.

4.2.1 Prototype System Power Stage

The prototype system uses low-power buck converter cells operating at the edge of discontinuous

conduction under peak current control. Figure 4.3 shows the power stage design of the cells used in the low-power prototype system. For simplicity, a simple op-amp circuit is used to simulate the buck switch and diode and generate a 0 to 10 V switching waveform, controlled by the switching signal LOSET. To make the cell operate at the edge of discontinuous conduction while tracking an average output current reference, the current control circuit of Fig. 4.4 is used. This control circuit causes the cell output current to ramp between zero and twice the reference current i_{ref}, with an average value of i_{ref}. Each cell is designed to handle a peak current of 20 mA, yielding a per-cell load range of 1 - 10 mA. The system has a total output capacitance, C_f, of 45 μF, and is resistively loaded.

Operation at the edge of discontinuous conduction yields an average output current (which is one half of the peak output current) that is inversely proportional to the switching frequency. Specifically, for an approximately constant output voltage v_{cf}, we find

$$f_{sw} = \frac{v_{cf}(V_{in} - v_{cf})}{2V_{in}Li_{ref}} \quad . \tag{4.1}$$

For example, in the prototype system, with L = 125 mH, V_{in} = 10 V. and v_{cf} = 5 V, full load corresponds to a 1 kHz switching frequency, while 10% load corresponds to a 10 kHz switching frequency. The cell output current switching ripple causes a very small (<1%) ripple in the output voltage at the same fundamental frequency. It is the frequency content of this output voltage ripple which carries information about the average cell output current.

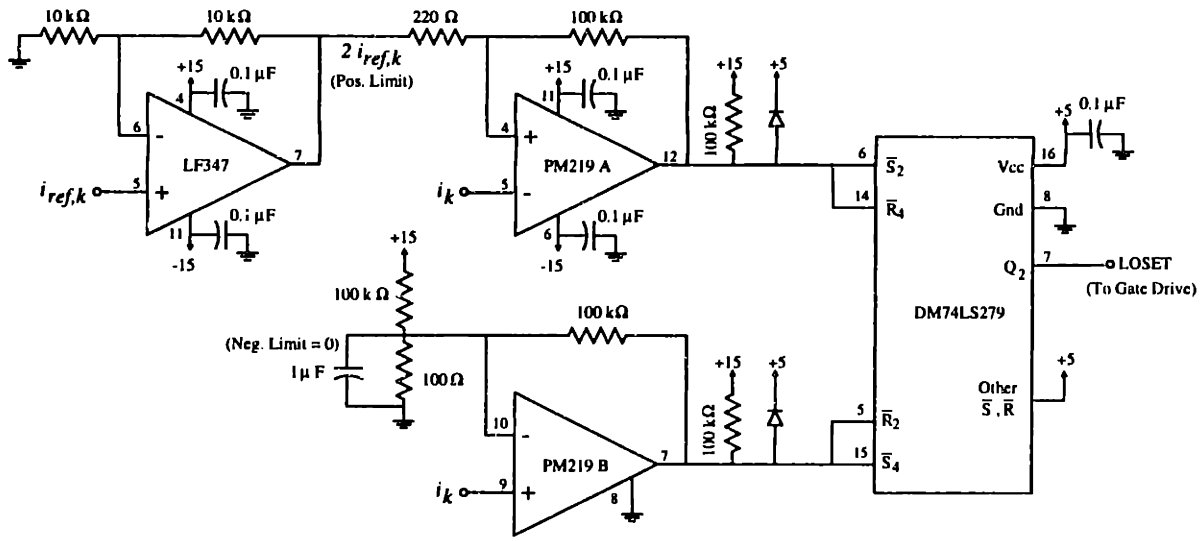


Figure 4.4 Schematic of the current control circuit used to control the cell power stage of Fig. 4.3. This circuit causes the cell to operate at the edge of discontinuous conduction.

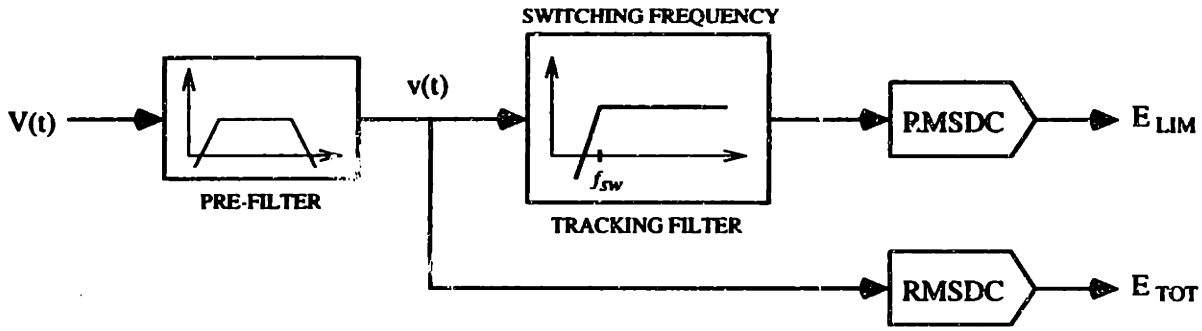


Figure 4.5 Structure of the frequency estimator used in the prototype system. E_{lim} is the rms of the filtered ripple, E_{tot} is the rms of the total ripple. These signals are used by the current-sharing controller of Fig. 4.13.

4.2.2 Frequency Estimation

To decode the current-sharing information contained in the output voltage ripple, each cell employs a frequency estimator which detects whether any other cell is operating at a lower switching frequency. The estimator structure used in the prototype system, shown in Fig. 4.5 , is composed of three stages: (1) a bandpass filtering stage, (2) a frequency-tracking filter stage, and (3) an rms-to-dc conversion stage. The bandpass filtering stage removes the low-frequency and high-frequency (noise) components of the output voltage, while amplifying the switching ripple component. The frequency-tracking filter is a high-pass filter whose cutoff frequency is continuously adjusted to fall just below the local cell switching frequency, in order to attenuate switching ripple components at frequencies below that of the local cell. The rms-to-dc conversion stage measures the rms of the switching ripple signals before and after the tracking filter. If the rms of the filtered switching ripple is lower than that of the unfiltered ripple, it indicates that one or more cells are operating at switching frequencies below that of the local cell. Thus, the estimator structure of Fig. 4.5 provides enough information to implement the current-

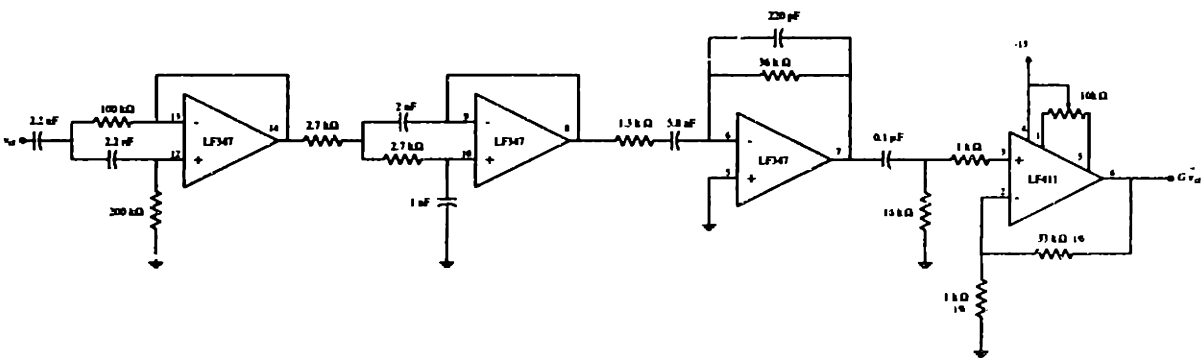


Figure 4.6 Schematic of the bandpass filtering stage of the prototype frequency estimator..

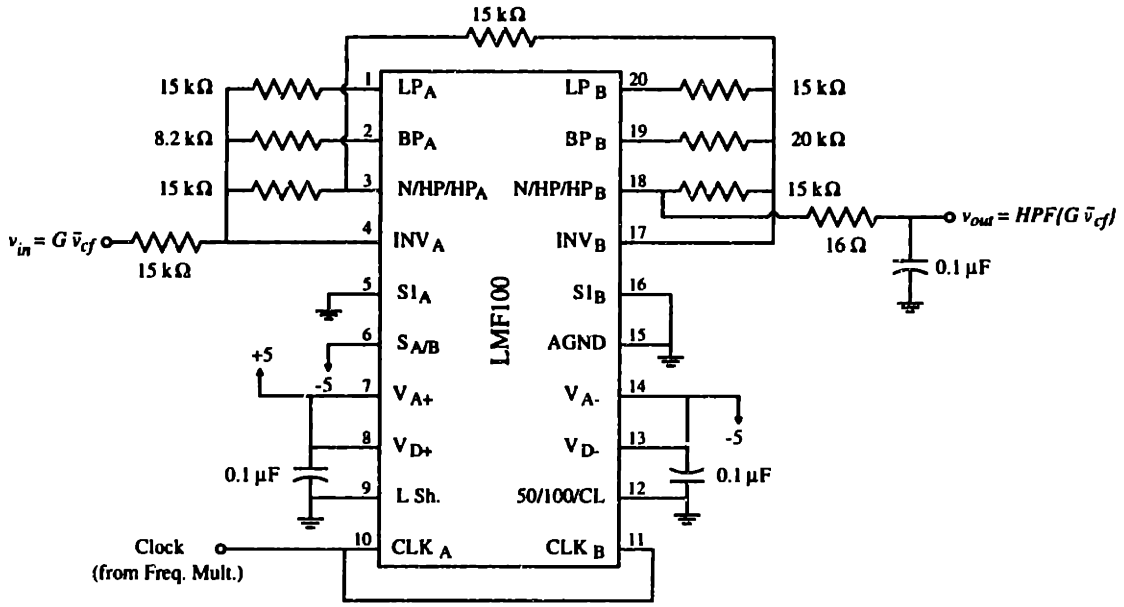


Figure 4.7 Schematic of the tracking filter used in the prototype frequency estimator of Fig. 4.6. The clock input comes from the frequency multiplier of Fig. 4.9.

sharing approach described previously.

The implementation of the bandpass filtering stage of the frequency estimator is illustrated in Fig. 4.6. The filtering stage is a cascade of a second-order Butterworth high-pass filter (f_c = 500 Hz), a second-order Butterworth low-pass filter (f_c = 40 kHz), and a frequency-dependent amplifier. The frequency-dependent amplifier compensates for the fact that the magnitude of the voltage ripple across the capacitive output filter decreases with increasing frequency. It implements a gain of zero at dc, increasing at 20 dB/decade to a gain of 44 at 1 kHz, breaks over to a gain of 450 at 20 kHz, and decreases at a rate of -20 dB/decade above that. The output of the bandpass filtering stage is thus a greatly amplified and frequency-compensated version of the output switching ripple, with high-order switching harmonics (and high-frequency noise) attenuated.

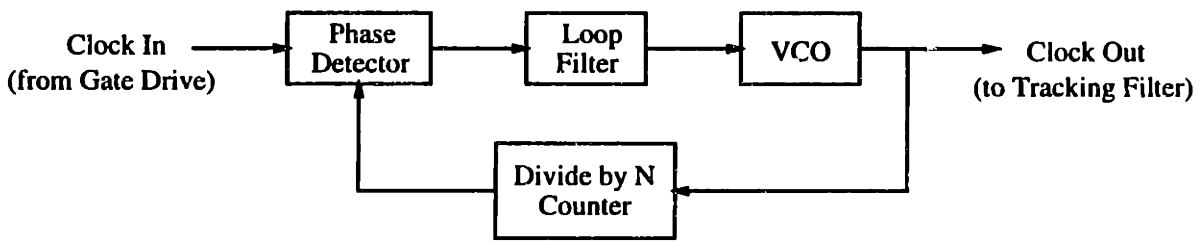


Figure 4.8 Structure of the frequency multiplier used to generate the tracking filter clock from the local gate drive waveform.

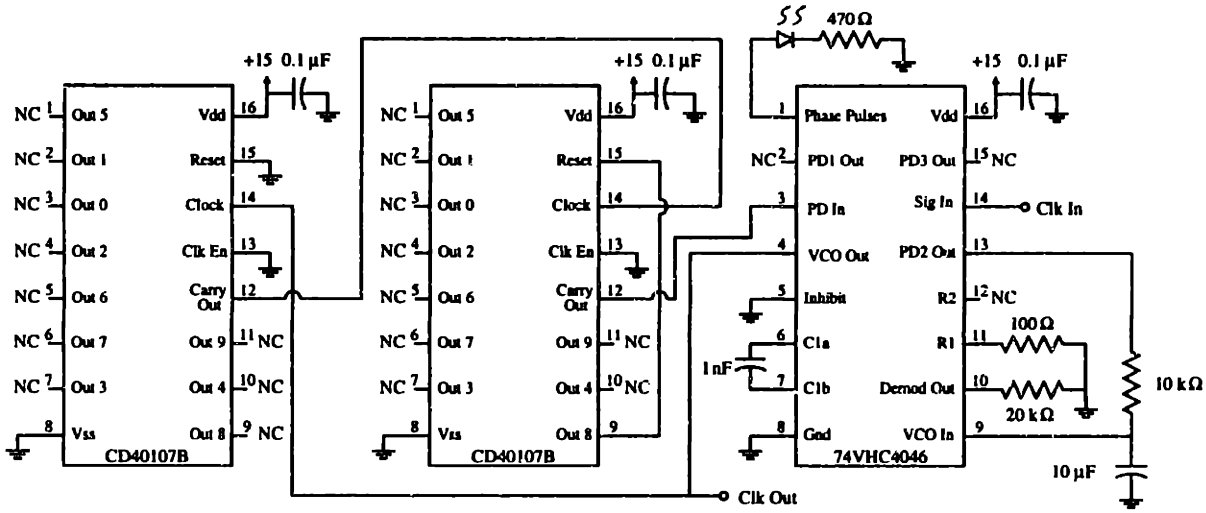


Figure 4.9 Schematic of the frequency multiplier used to generate the tracking filter clock from the local gate drive waveform.

The frequency-tracking filter stage is a fourth-order Butterworth high-pass filter whose cutoff frequency is continuously adjusted to 0.8 times the local switching frequency. A Butterworth filter is selected because it exhibits no peaking in its response near the cutoff frequency. As shown in Fig. 4.7, the tracking filter is implemented using an LMF100 switched-capacitor filter whose clock frequency is derived from the local switching frequency.

To achieve the desired tracking filter cutoff frequency , the LMF100 clock frequency must be 80 times the local switching frequency. A frequency multiplier of the structure shown in Fig. 4.8 is used to generate the LMF100 clock from the local gate drive waveform. As illustrated in Fig. 4.9, the frequency multiplier is implemented using the 74VHC4046 phase-locked loop (PLL) IC. Phase detector II of the 74VHC4046 is used because it does not exhibit harmonic locking and yields a suitable lock and capture range for the task. The time constant of the loop filter (0.1 s) is short enough to allow the

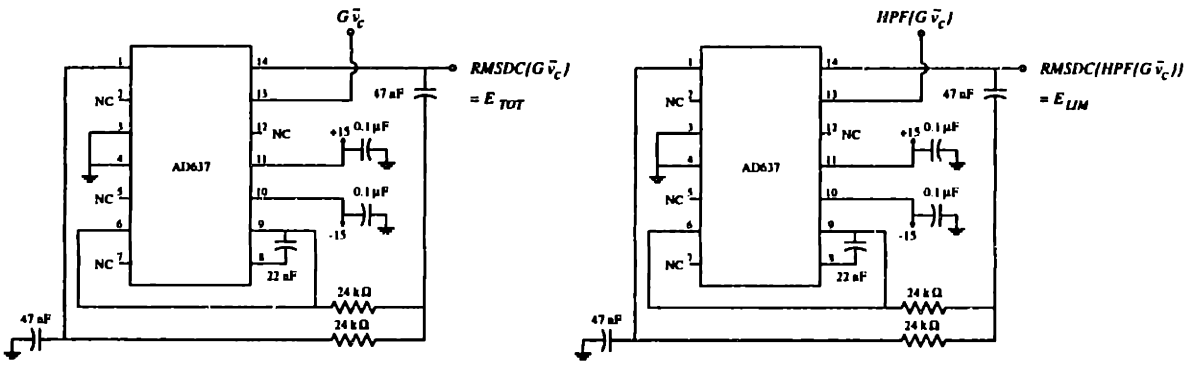


Figure 4.10 Schematic of the rms-to-dc conversion stage of the prototype frequency estimator.

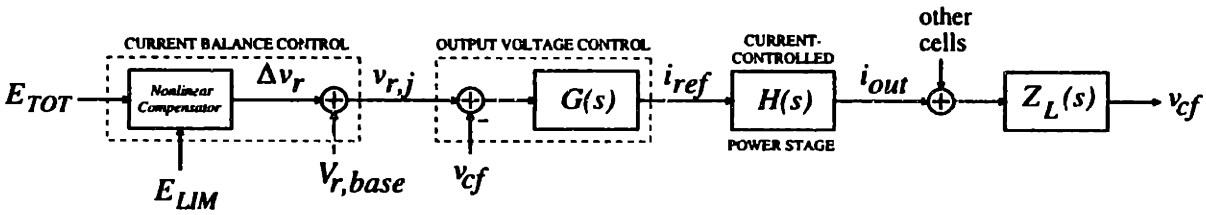


Figure 4.11 Block diagram of the cell control structure used in the prototype system.

frequency multiplier to track switching frequency variations due to the action of the cell output voltage control loop. The divide-by-eighty counter in the feedback path of the PLL yields a switched-capacitor filter clock frequency of 80 times the (input) switching frequency. This results in a tracking filter cutoff frequency of 0.8 times the switching frequency.

The rms-to-dc conversion stage of the frequency estimator measures the rms of the switching ripple signals before and after the tracking filter. It is implemented using AD637 integrated circuit rms-to-dc converters connected in the two-pole Sallen-Key filter arrangement (Fig. 4.10). The averaging and filter capacitor values (C_{AV} = 0.022 μF, $C_2 = C_3$ = 0.047 μF) are selected to yield a 1% settling time of 8 ms. This is considered fast enough to track the variations in switching ripple frequency content while still suppressing ripple in the rms-to-dc converter outputs. The two rms-to-dc converter outputs form the output of the frequency estimator stage. Any difference between these signals indicates that another cell is operating at a lower switching frequency. This information is used by the current-sharing controller to achieve load balance with the other cells.

4.2.3 Control Design

This section describes the design of the control circuitry used in the prototype converter system. The task of predicting the output and load-sharing dynamics for cellular converter systems is addressed in Chapter 5. A block diagram of the cell control structure used in the prototype system is shown in Fig. 4.11. In simplest terms, each cell can be viewed as having an inner current control loop, a middle voltage control loop, and an outer load-sharing control loop.

The design and operation of the inner current loop circuitry has been previously described in Section 4.2.1. The inner current loop causes the average output current i_{out} to accurately track a current reference i_{ref}, and allows the cell power stage to be modeled as a controlled current source of value i_{ref} (yielding $H(s) \approx 1$ in Fig. 4.11). It also inherently enforces a relationship between the cell switching frequency and average output current, thus encoding current sharing information on the output switching ripple.

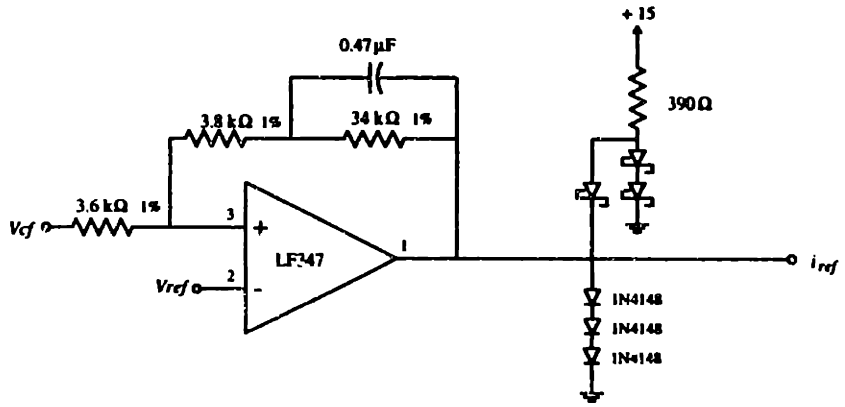


Figure 4.12 Schematic of the output voltage control circuit used in the prototype system.

To regulate the output voltage, each cell has a middle voltage control loop which generates the current reference for its inner loop based on the difference between a local voltage reference and the output voltage. The prototype system employs a lag compensator of the design shown in Fig 4.12 (τ_p = 0.0159, τ_z = 0.00159) for this purpose. This yields a voltage control bandwidth on the order of 100 Hz, with less than 5% load regulation over the load range of the cell. The output of the voltage control circuit has a clamp such that the commanded reference current is always within the allowed range of 1 - 10 mA.

To achieve load balance among cells, each cell has a slow outer current-sharing loop which operates by adjusting the local reference voltage v_{ref} over a limited range about a base value $v_{r,base}$. The individual converter references are shifted via integral control based on the difference between the two frequency estimator outputs minus a small offset. That is, the system uses the difference between the rms of the total switching ripple and the rms of the switching ripple components at frequencies of the local cell and higher, minus an additional offset; i.e.

$$\frac{dv_{r,j}}{dt} = \begin{cases} K_j[E_{tot} - E_{lim} - \Delta E] & for \quad v_{r,j,base} < v_{r,j} < v_{r,j,max} \\ 0 & otherwise \end{cases} \tag{4.2}$$

where K_j is the (integral) control gain, E_{tot} and E_{lim} are the two frequency estimator outputs, and ΔE is the offset. The j^{th} reference is adjustable over a small range from a base value $v_{r,j,base}$ to a maximum value $v_{r,j,max}$ (which is about 5% larger than the base value), and is prevented from going outside this range. The offset ΔE guarantees that the reference of the lowest switching frequency (highest current) cell will always be driven down towards its base value so that current sharing can be achieved.

To implement this outer-loop control structure, the prototype system uses the reference adjustment

circuitry provided in the UC3907 load-sharing IC (Fig. 4.13). The UC3907 is designed to implement a single-wire current-sharing scheme in which the local voltage reference is adjusted based on the difference between the highest cell current and the local cell current, minus a small offset [32]. By properly scaling and shifting the two outputs of the frequency estimator and using them in place of the local and highest current inputs of the UC3907, the UC3907 can instead be caused to adjust its local reference voltage as previously described. Because the UC3907 is designed to implement the voltage control loop internally, it does not directly provide the adjusted voltage reference at a pin. As shown in Fig. 4.13, the prototype system works around this by using external circuitry to compute the reference from available outputs of the UC3907, and to scale it to a 5 V base value. This reference is provided to the middle voltage control loop. The integrating compensator implemented in the UC3907 yields a current-sharing control bandwidth on the order of a Hertz.

The three control loops operate together to properly regulate the output voltage of the system while maintaining current sharing among cells. While other design approaches are possible, this multilayered control strategy has been found to be both simple and effective. It should also be pointed out that the control approach used in the prototype system can, in practice, be implemented in a much more compact manner. For example, single control ICs such as the UC3852 are available which can implement the entire inner current control loop [40], and both the middle voltage loop and much of the outer current-sharing loop can be implemented internally to the UC3907.

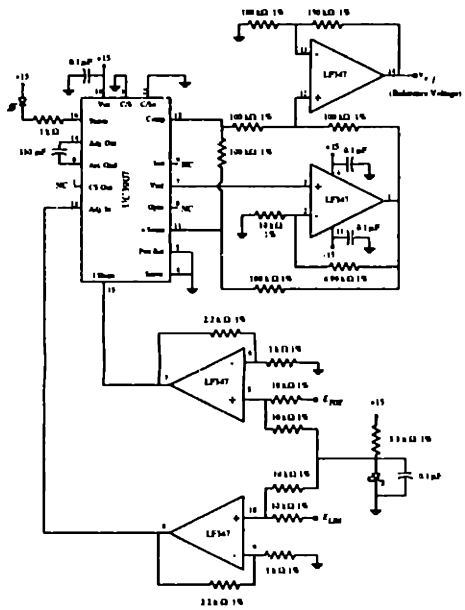


Figure 4.13 Schematic of the current-sharing control circuit used in the prototype system. This circuit generates the voltage reference used by the voltage control loop.

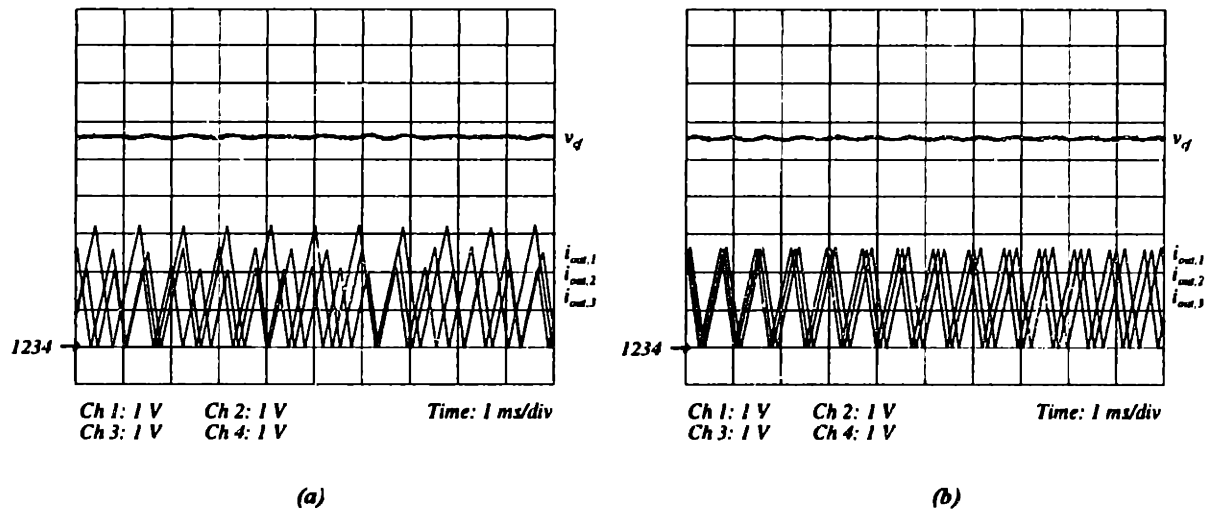
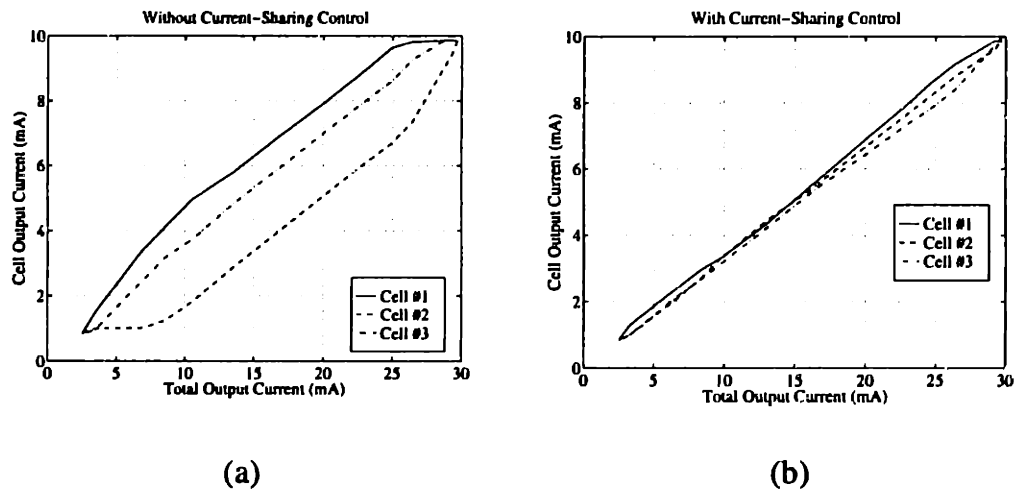


Figure 4.14 Current-sharing characteristics of the prototype system at approximately 66% of full load ($R_{load} \approx 278\Omega$). (a) Without current-sharing control. (b) With current-sharing control. Current signals are represented at a scale factor of 200 V/A.

4.3 Experimental Results

This section presents an evaluation of the switching ripple method of current-sharing control using a 3-cell prototype system of the design presented in the previous section. Additional results can be found in [41]. It should be noted that the approach is independent of the number of cells in the system, and can be directly applied to systems with an arbitrary number of cells. Figure 4.14 shows operation of the



(a) (b)

Figure 4.15 The static current-sharing characteristic of the prototype system. (a) without current-sharing control. (b) with current-sharing control.

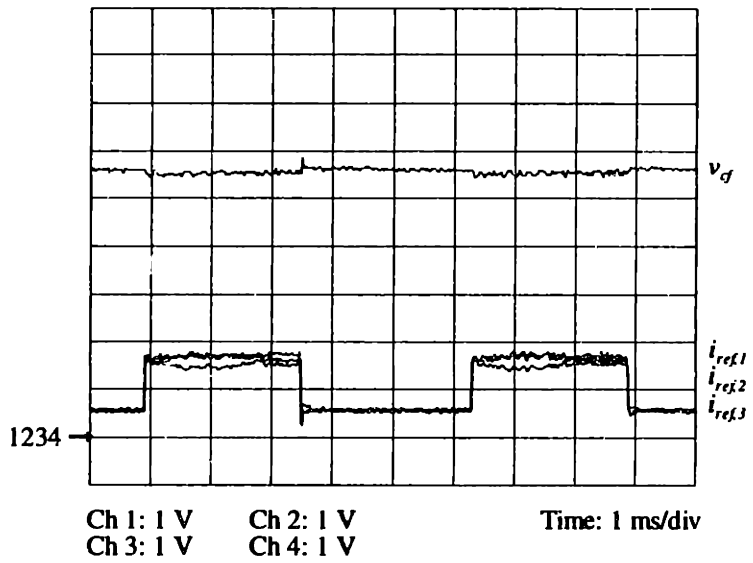


Figure 4.16 Response of the prototype system to load steps between 27% and 83% of full load (673 Ω and 224 Ω). Current signals are represented at a scale factor of 200 V/A.

prototype system at approximately 66% of full load both with and without current-sharing control. Without current-sharing control, there is a significant imbalance in average output current among the three cells. The inverse relationship between switching frequency and average output current is also apparent. With current-sharing control, the switching frequencies and average cell output currents are almost precisely equal. This high degree of current sharing is achieved by using the information encoded in the frequency content of the output switching ripple, without additional interconnections.

Figure 4.15 shows the static current-sharing characteristic over the load range of the system both with and without current-sharing control. Without current sharing, there are significant current imbalances over much of the load range, while with current sharing the cells share current to within 5% of the average over the entire load range. This high degree of active current sharing is obtained with less than 5% load regulation over the entire load range.

Current-sharing behavior was also investigated under transient conditions. Figure 4.16 shows the current-sharing behavior for load steps between 673 Ω and 224 Ω, corresponding to approximately 27% and 83% of full load. The current-sharing behavior is seen to be stable for even large load steps. Figure 4.17 shows the reference current transient response for two cells when current-sharing control is turned on. Again, accurate current sharing is rapidly achieved with stable dynamics. What may be concluded from these results is that the switching ripple method can be used to achieve accurate static and dynamic current sharing without the need for additional interconnections among cells.

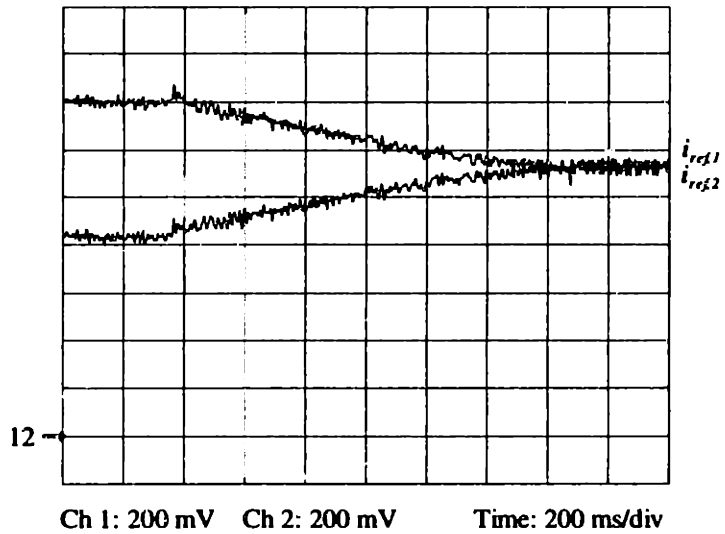


Figure 4.17 Current reference transient response for two cells when current sharing is turned on with $R_L = 500\ \Omega$. Currents are represented at 200 V/A.

4.4 An Alternative Switching-Ripple-Based Approach

The current-sharing control implementation described in the previous sections operates by indirectly extracting current-sharing information from the switching ripple frequency content and using it to enforce current sharing. The presented approach is both simple and effective. However, given that the output voltage harmonic content contains information about the individual cell currents, it is reasonable to ask if quantities such as the average or rms cell currents can be *directly* extracted from the output voltage harmonic content for use in current-sharing control. This section explores that possibility, and examines the advantages and disadvantages of such an approach. For simplicity and consistency, a cellular system composed of buck converter cells operating at the edge of discontinuous conduction will again be considered.

4.4.1 An Rms Current Estimator

The switching frequency and ripple current harmonic content of a converter cell operating at the edge of discontinuous conduction is uniquely related to its average output current. Thus, the aggregate voltage ripple due to paralleled cells operating at the edge of discontinuous conduction contains information about the individual cell output currents. This section presents a method for estimating the rms cell reference current of such a system directly from the output voltage ripple. The rms cell reference current for an N-cell converter system is defined as

$$i_{rms}(t) = \sqrt{\frac{\sum_{i=1}^{N} i_{ref,k}^2}{N}} \tag{4.3}$$

where $i_{ref,k}$ is the reference current (or equivalently, the average output current) of the k^{th} cell. Knowledge of the rms cell current can be used by the individual cells to implement a current-sharing control scheme.

Consider the relationship between the reference current, switching frequency, and harmonic content of a buck converter cell operating at the edge of discontinuous conduction. The output current of the k^{th} cell can be written as a Fourier Series

$$I_k = \sum_{n=-\infty}^{\infty} C_{n,k}\delta(\omega - n\omega_k) \tag{4.4}$$

where ω_k is given by

$$\omega_k = \frac{\pi v_{cf}(V_{in} - v_{cf})}{V_{in} L i_{ref,k}} \quad . \tag{4.5}$$

Approximating the output current as a piecewise-linear function, the n^{th} Fourier coefficient for the output current of the k^{th} cell can be expressed as

$$C_{n,k} = \frac{m_2}{2\pi n^2 \omega_k}(1 - e^{jn\omega_k \Delta t_2}) - \frac{m_2 \Delta t_2}{2\pi jn} e^{jn\omega_k \Delta t_2} + \frac{m_1}{2\pi n^2 \omega_k}(e^{-jn\omega_k \Delta t_1} - 1) - \frac{m_1 \Delta t_1}{2\pi jn} e^{-jn\omega_k \Delta t_1} \tag{4.6}$$

where $m_1 = (V_{in} - v_{cf})/L$, $m_2 = -v_{cf}/L$, $\Delta t_1 = 2i_{ref,k} / m_1$, and $\Delta t_2 = -2i_{ref,k} / m_2$ [37]. For the ripple component of i_k , $C_{0,k} = 0$, while all other terms are given by **(4.6)**.

Careful examination of **(4.5)** and **(4.6)** reveals that the values $C_{n,k}$ are proportional to $i_{ref,k}$, while ω_k is inversely proportional to $i_{ref,k}$. This is due to the fact that the *shape* of $i_k(t)$ is invariant to the value of $i_{ref,k}$; the waveform is merely scaled in time and magnitude for different values of $i_{ref,k}$, as illustrated in Fig. 4.2. Recognizing this, we can define normalized variables which are independent of $i_{ref,k}$:

$$\hat{C}_n = \frac{C_{n,k}}{i_{ref,k}} \tag{4.7}$$

and

$$\hat{\omega} = \omega_k \cdot i_{ref,k} \quad . \tag{4.8}$$

Because the normalized variables are independent of $i_{ref,k}$, they are the same for every converter cell, provided that the cells are identical.

Employing the normalized variable representation, we now compute the power spectra of the cell output ripple current and voltage and their derivatives. The power spectrum of the output ripple current for the k^{th} cell can be expressed as

$$S_{\tilde{i}_k} = 2\pi \sum_{n=-\infty}^{\infty} i_{ref,k}^2 |\hat{C}_n|^2 \delta(\omega - n\omega_k) \quad . \tag{4.9}$$

Assuming that the load impedance is much greater than the filter capacitor impedance for the switching frequency and above, the transfer function from ripple current to ripple voltage is $H(\omega) = 1/(j\omega C_f)$, and the power spectrum of the output voltage ripple due to the k^{th} cell can be written as

$$S_{\tilde{v}_{cf,k}} = \frac{2\pi}{C_f^2} \sum_{n=-\infty}^{\infty} \frac{i_{ref,k}^4}{n^2\hat{\omega}^2} |\hat{C}_n|^2 \delta(\omega - n\omega_k) \quad . \tag{4.10}$$

Differentiation in the time domain corresponds to the application of a transfer function $H(\omega) = j\omega$ in the frequency domain. Thus, the power spectrum of the first derivative of the current ripple of the k^{th} cell can be written as

$$S_{\tilde{i}'_k} = 2\pi \sum_{n=-\infty}^{\infty} n^2\hat{\omega}^2 |\hat{C}_n|^2 \delta(\omega - n\omega_k) \quad , \tag{4.11}$$

the power spectrum of the first derivative of the voltage ripple can be written as

$$S_{\tilde{v}'_{cf,k}} = \frac{2\pi}{C_f^2} \sum_{n=-\infty}^{\infty} i_{ref,k}^2 |\hat{C}_n|^2 \delta(\omega - n\omega_k) \quad , \tag{4.12}$$

and the power spectrum of the second derivative of the voltage ripple can be written as

$$S_{\tilde{v}''_{cf,k}} = \frac{2\pi}{C_f^2} \sum_{n=-\infty}^{\infty} n^2\hat{\omega}^2 |\hat{C}_n|^2 \delta(\omega - n\omega_k) \quad . \tag{4.13}$$

If all of the cells are operating at different frequencies (or even at the same frequency with uncorrelated phases), then the power spectrum of the total ripple is the sum of the power spectra of the the individual cell ripples. Thus, we can write

$$S_{\tilde{v}'_{cf}} = \left[\frac{2\pi}{C_f^2} \sum_{n=-\infty}^{\infty} |\hat{C}_n|^2 \delta(\omega - n\omega_k) \right] \cdot \sum_{k=1}^{N} i_{ref,k}^2 \tag{4.14}$$

and

$$S_{\tilde{v}''_{cf}} = \left[\frac{2\pi}{C_f^2} \sum_{n=-\infty}^{\infty} n^2 \omega^2 |\hat{C}_n|^2 \delta(\omega - n\omega_k) \right] \cdot N \quad . \tag{4.15}$$

Note that **(4.14)** is proportional to the sum of the squares of the cell reference currents, while **(4.15)** is proportional to the number of cells. The spectral content of the output voltage ripple (and its derivatives) thus contain information useful for computing the rms reference current. The desired information can be extracted by computing the rms values of the time-domain waveforms. The rms of a time-domain waveform is related to its power spectrum by

$$rms\{x(t)\} = \sqrt{\frac{1}{2\pi} \int_{-\infty}^{\infty} S_x(\omega) d\omega} \quad . \tag{4.16}$$

Applying **(4.16)** to **(4.9)**, **(4.11)**, **(4.14)** and **(4.15)** yields

$$rms\left\{ \tilde{i}_k(t) \right\} = \sqrt{i_{ref,k}^2 \sum_n |\hat{C}_n|^2} \tag{4.17}$$

$$rms\left\{ \tilde{i}'_k(t) \right\} = \sqrt{\omega^2 \sum_n |n\hat{C}_n|^2} \tag{4.18}$$

$$rms\left\{ \tilde{v}'_{cf}(t) \right\} = \sqrt{\left[\frac{1}{C_f^2} \sum_n |\hat{C}_n|^2 \right] \cdot \sum_{k=1}^{n} i_{ref,k}^2} \tag{4.19}$$

$$rms\left\{ \tilde{v}''_{cf}(t) \right\} = \sqrt{\left[\frac{\omega^2}{C_f^2} \sum_n |n\hat{C}_n|^2 \right] \cdot N} \quad . \tag{4.20}$$

Consider taking the ratio of **(4.19)** to **(4.20)**. This yields a quantity that is proportional to the rms cell current:

$$\frac{rms\left\{ \tilde{v}'_{cf}(t) \right\}}{rms\left\{ \tilde{v}''_{cf}(t) \right\}} = \sqrt{\left[\frac{\sum_n |\hat{C}_n|^2}{\omega^2 \sum_n |n\hat{C}_n|^2} \right] \cdot \frac{\sum_{k=1}^{n} i_{ref,k}^2}{N}} \tag{4.21}$$

To cancel the proportionality constant in **(4.21)**, we multiply by the ratio of **(4.18)** to **(4.17)** and also multiply each side by $i_{ref,k}$. This yields the desired estimate of the rms cell current:

$$i_{est} = \frac{rms\left\{\tilde{v}'_{cf}(t)\right\}\, rms\left\{\tilde{i}'_{k}(t)\right\}\, i_{ref,k}}{rms\left\{\tilde{v}''_{cf}(t)\right\}\, rms\left\{\tilde{i}_{k}(t)\right\}} = \sqrt{\frac{\sum_{k=1}^{n} i^2_{ref,k}}{N}} \qquad (4.22)$$

This result means that by properly combining the rms values of i_k and v_{cf} and their derivatives, the rms cell current can be computed. The value of this result is that while all of the quantities on the left side of (4.22) can be measured or computed locally at each cell, their combination computes the rms of *all* of the cell output currents. This is possible because the output voltage ripple and its derivatives contain information about all of the cell currents, as seen in (4.19) and (4.20). The additional factors in (4.22) compute needed proportionality constants in an in-line fashion, without requiring a priori knowledge of the circuit parameters or operating point. Also note that the computation does not require a priori knowledge of the number of cells, since this information is implicitly contained in (4.20). In summary, (4.22) allows computation of the rms cell reference current using only information locally measurable at each cell, without requiring a priori knowledge of the number of cells, circuit parameters or operating point.

4.4.2 Rms Current Estimator Implementation

The implementation of an rms estimator based on (4.22) is significantly more complicated than that of the estimator structures presented in sections 3.3 and 4.2. Nevertheless, a direct implementation of the estimator in analog circuitry is quite possible, as is an equivalent microprocessor-based implementation. This section will present an analog implementation of an rms cell current estimator based on (4.22).

The estimator implements the following rms current estimation equation

$$i_{est}(t) = \frac{rmsdc\left\{K_1\tilde{v}'_{cf}(t)\right\}\, rmsdc\left\{K_3\tilde{i}'_{k}(t)\right\}\, i_{ref,k}}{rmsdc\left\{K_1K_2\tilde{v}''_{cf}(t)\right\}\, rmsdc\left\{\tilde{i}_{k}(t)\right\}} \qquad (4.23)$$

where *rmsdc* denotes operation of a conventional integrated circuit rms-to-dc converter, and K_1, K_2, and K_3 are scaling constants used to keep intermediate computations in range.

A functional block diagram of the implemented estimator circuit is shown in Fig. 4.18. Detailed circuit diagrams for the estimator may be found in Appendix B of [37]. The estimator of Fig. 4.18 is

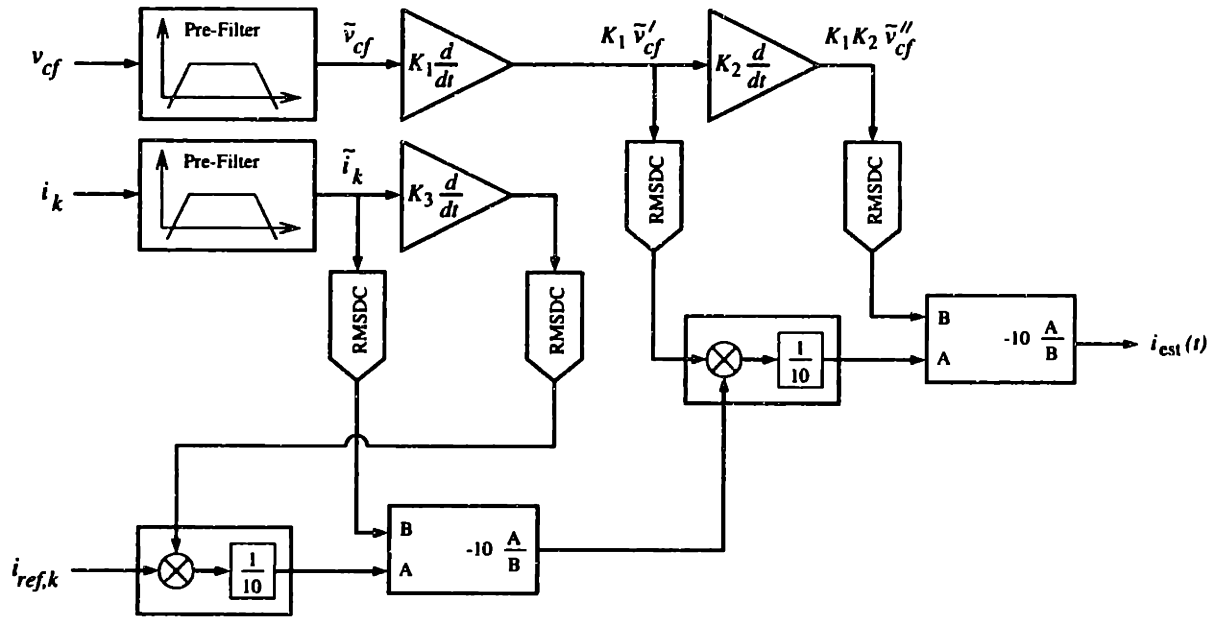


Figure 4.18 Functional block diagram of the prototype rms reference current estimator.

composed of four stages: (1) a prefilter stage, (2) a gain and differentiation stage, (3) an rms-to-dc conversion stage, and (4) a multiplication and division stage. The estimator is designed to be used with converter cells of the type described in section 4.2.1 operating within a load current range of 1 to 10 mA (which corresponds to a 1 to 10 kHz switching frequency range).

The pre-filter stage comprises a pair of bandpass filters which isolate the ripple components of the output voltage and local-cell current signals, respectively. The bandpass filters attenuate both the low-frequency and high-frequency (noise) components of the measured signals, while passing the ripple-frequency components. Each bandpass filter is composed of the series connection of a second-order low-pass Butterworth filter (f_c = 500 Hz) and a second-order high-pass Butterworth filter (f_c = 20 kHz).

The gain and differentiation stage computes the required derivatives of $\tilde{v}_{cf}$ and $\tilde{i}_k$ and provides the proper signal scaling for the remaining stages. Band-limited differentiator circuits are used which act as differentiators for the frequency range of interest, but whose gain rolls off like an integrator above 50

kHz in order to attenuate high-frequency noise. The differentiation gains K_1, K_2, and K_3 are set to make the best use of the input range of the rms-to-dc converters, while providing proper signal scaling for the final result (which requires that $K_2 = K_3$).

The rms-to-dc conversion stage computes local-time approximations to the rms values of the required signals. AD637 integrated circuit rms-to-dc converters connected in the two-pole Sallen-Key filter arrangement (1% settling time of 8 ms) are used for this purpose. The effects of using such local-time approximations to the rms (in terms of frequency resolution and response speed) are addressed in Chapter 2.

The multiplication and division stage computes the final estimate from the different factors in **(4.23)**. As shown in Fig. 4.18, the required computations are broken up into two multiplications and two divisions. The multiplications are performed using AD633 integrated circuit multipliers. Each division circuit is constructed by placing an AD633 multiplier in the feedback path of an LF347 op amp. This approach is more cumbersome than other possible implementations, such as the use of higher-order computational units or logarithm-based division circuits, but is less costly.

4.4.3 Experimental Results and Evaluation

An rms current estimator of the described design was constructed and used with a single converter cell of the type described in Section 4.2.1. The estimator was tested by using it to estimate the cell's own reference current over the load range. (For a single cell, the rms reference current of all cells equals the cell's own reference current as per **(4.1)**). As illustrated in Fig. 4.19, the results of this test indicate that while the rms current estimator does track the reference current, estimation errors as high as 10% occur over the load range.

The intermediate waveforms used in computing the rms current estimate are shown in Fig. 4.20. The derivative of the output ripple current has an approximately square waveshape, but with sloped tops and bottoms. The sloping is due to the fact that the inductor current waveform is not truly piecewise linear, as was assumed in the first order model of the system used in the calculation of **(4.5)** and **(4.6)**. The result of this is that the *shape* of $i_k(t)$ is not truly invariant to the value of $i_{ref,k}$, leading to slight errors in the resulting estimate, especially at high reference current levels where bowing of the inductor current is significant. More generally, it may be concluded that the accuracy of the estimation approach depends heavily on the modeling assumptions used in its development. Inaccuracies in modeling the converter and its waveforms, including second order ripple effects, filter capacitor ESR, etc., can cause inaccuracies in the estimation process.

Perhaps a more significant source of error is the susceptibility of the estimator to noise, also observable in Fig. 4.20. As expected, the first derivative of the output voltage ripple is proportional to the cell output current ripple, with only slight ripple due to switching noise. However, while the second derivative of the output voltage ripple has the correct general shape, it suffers from severe ringing due to noise, especially at the switching transitions. This heavily-amplified noise component is captured by the rms-to-dc conversion stage and affects the final estimate. The cascade of differentiators used in the rms current estimator causes heavy amplification of switching noise, and is unlikely to be practical in the high-noise environment of a full-power switching converter system. Further development of this estimation method for use in load-sharing control was abandoned primarily for this reason. Nevertheless, it should be pointed out that similar estimation techniques may be quite viable for estimating other quantities or for use with other converter types.

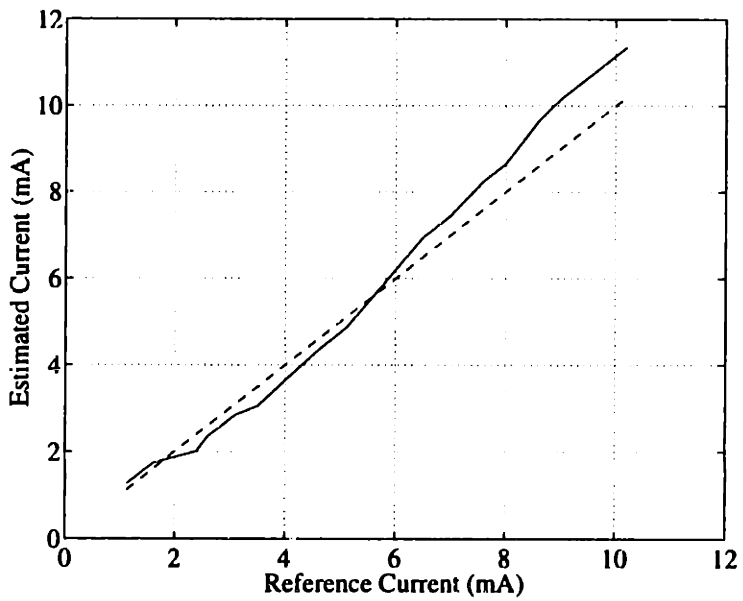


Figure 4.19 Estimation performance of the rms reference current estimator with a single cell.

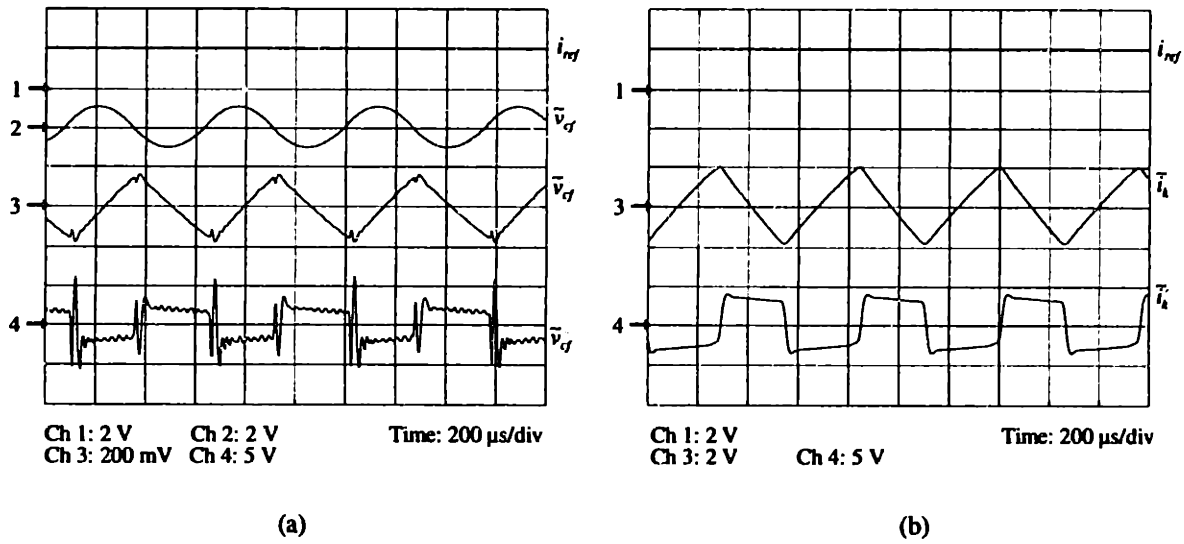


Figure 4.20 Circuit waveforms of the prototype converter and rms current estimator.

4.5 Conclusion

This chapter has explored the switching ripple method of current sharing introduced in chapter 2. This approach, which is based on encoding the current-sharing information in the switching ripple of the converter cells, eliminates the need for additional current-sharing interconnections among converters. A practical implementation of the approach is presented, including methods and circuits for controlling the cell switching patterns, decoding the current-sharing information from the output switching ripple, and controlling the output voltage and current sharing. An experimental evaluation of this implementation approach based on a 2-cell prototype system is also presented. It is shown that accurate and stable current sharing is obtainable over a wide load range using this approach. An alternative method of decoding current-sharing information from the output voltage ripple is also developed and experimentally evaluated. We conclude that the switching ripple method of current sharing can be implemented with simple circuitry, and allows load sharing to be obtained without the need for additional interconnections among cells.

Chapter 5

Stability Analysis of Nonlinear Current-Sharing Techniques

The ability to accurately predict load-sharing stability and system dynamics is an important aspect of the design of a cellular converter architecture, and has been the subject of recent attention [26, 29,42-44]. However, all of these analyses focus on linear feedback control methods, and are based on feeding back either the average current output of the cells or the current of a designated "master" cell. While these are important cases, many distributed load-sharing control methods, including those introduced in Chapters 2-4, use feedback based on other quantities, and have inherently nonlinear dynamics. This chapter addresses the dynamic analysis of systems employing nonlinear load-sharing control techniques, and validates these analyses against experimental results. Section 5.1 analyzes nonlinear load-balancing control methods which are linearizable about a constant operating point. This follows the approach of a recently-developed analysis of the linear feedback case [29,43], but explicitly considers the linearization of nonlinear current-sharing control laws. Section 5.2 applies this approach to the frequency-based current-sharing control scheme developed in Chapters 2 and 3, and validates it against both simulation and experimental results. Section 5.3 analyzes a widely-used nonlinear feedback control scheme which is not easily handled by linearization in the general case [32], and identifies conditions under which it is easily analyzed. The dynamics of the method are analyzed for this important special case, and validated against experimental results.

5.1 Linearization-Based Analysis

Here we address the dynamic analysis of an N-cell, dc-output parallel converter system about a fixed operating point. As shown in Fig. 5.1, we model the j^{th} cell as a voltage source $v_{r,j}$ (equal to the cell reference voltage) in series with an output impedance Z_j, while the load is modeled as an impedance Z_L. The individual load-sharing controllers, which operate by adjusting the local reference voltages according to the load-balance condition, have nonlinear dynamics

$$\frac{dv_{r,j}}{dt} = g_j(v_{r,j}, i_1, \ldots, i_N) \quad for \quad j \in [1,N] \; . \tag{5.1}$$

We consider the dynamic behavior of such a system about a fixed operating point where

$$g_j(V_o, I_1, \ldots, I_N) = 0 \quad for \quad j \in [1,N] \; . \tag{5.2}$$

The functions $g_j(\bullet)$ are assumed to have continuous first derivatives at the operating point, allowing the operating point stability and small-signal dynamics to be determined using Liapunov's indirect method (i.e., linearization). The linearized system dynamics are determined by considering the behavior of small perturbations such that:

$$\begin{aligned} i_j &= I_j + \hat{i}_j \quad for \quad j \in [1,N] \\ v_{r,j} &= V_{r,j} + \hat{v}_{r,j} \quad for \quad j \in [1,N] \end{aligned} \tag{5.3}$$

Expanding the equations **(5.1)** in a Taylor series about the operating point **(5.2)** and neglecting higher order terms, we find

$$\begin{aligned} \frac{d\hat{v}_{r,j}}{dt} &= \frac{\partial g_j}{\partial v_{r,j}} \hat{v}_{r,j} + \frac{\partial g_j}{\partial i_1} \hat{i}_1 + \cdots + \frac{\partial g_j}{\partial i_N} \hat{i}_N \\ &= J_{j0} \cdot \hat{v}_{r,j} + J_{j1} \cdot \hat{i}_1 + \cdots + J_{jN} \cdot \hat{i}_N \end{aligned} \tag{5.4}$$

where the partial derivatives are evaluated at the operating point.

Proceeding from the linear equations **(5.4)**, the approach outlined in [29] is directly employed to analyze the system dynamics. Taking the Laplace Transform of these equations, and denoting transformed quantities with capital letters, we find the equations

$$s\hat{V}_{r,j} = J_{j0}\hat{V}_{r,j} + J_{j1}\hat{I}_1 + \cdots + J_{jN}\hat{I}_N \; . \tag{5.5}$$

Using the relations

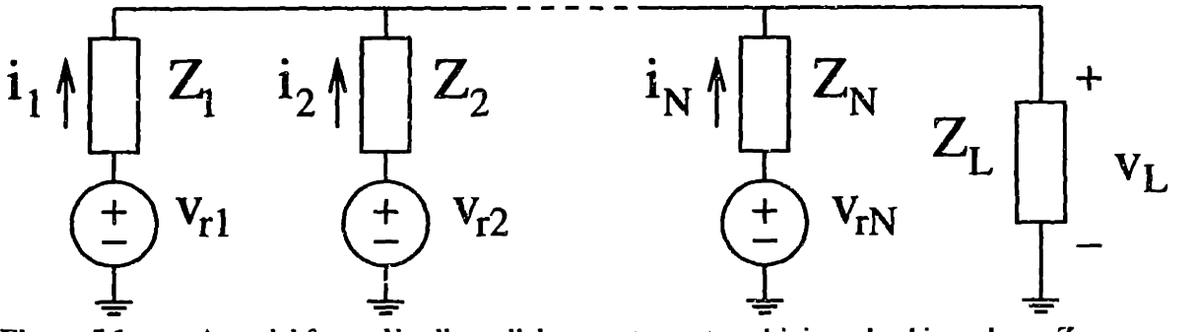


Figure 5.1 A model for an N-cell parallel converter system driving a load impedance Z_L.

$$\hat{V}_{rj} = \hat{I}_j Z_j + \hat{V}_o \tag{5.6}$$

and

$$\hat{V}_o = Z_L[\hat{I}_1 + \cdots + \hat{I}_N] \tag{5.7}$$

these equations (5.5) can be rewritten as

$$(s - J_{j0}) Z_j \hat{I}_j + \sum_{k=1}^{N} [(s - J_{j0}) Z_L - J_{jk}] \hat{I}_k = 0 \quad . \tag{5.8}$$

Furthermore, if each cell treats all other cells identically (i.e., if the functions $g_j(\cdot)$ are symmetric with respect to the currents of the other cells), then we may write

$$J_{jl} = J_{j*} \quad \forall \quad l \neq 0, j \; . \tag{5.9}$$

Employing this simplification, the equations (5.8) may be rewritten as

$$(s - J_{j0}) Z_j \hat{I}_j + (J_{j*} - J_{jj}) \hat{I}_j + \sum_{k=1}^{N} [(s - J_{j0}) Z_L - J_{j*}] \hat{I}_k = 0 \; . \tag{5.10}$$

Assembling the equations in the following matrix form

$$\left(\begin{bmatrix} (s - J_{10}) Z_1 + J_{1*} - J_{11} & \cdots & 0 \\ 0 & \ddots & 0 \\ 0 & \cdots & (s - J_{N0}) Z_N + J_{N*} - J_{NN} \end{bmatrix} + \begin{bmatrix} (s - J_{10}) Z_L - J_{1*} \\ \vdots \\ (s - J_{N0}) Z_L - J_{N*} \end{bmatrix} \cdot [1 \; 1 \; \cdots \; 1] \right) \cdot \begin{bmatrix} \hat{I}_1 \\ \vdots \\ \hat{I}_N \end{bmatrix} = 0$$

we identify the natural frequencies as the values of s for which the above system has a nontrivial solution. Due to the special form of the matrix multiplying the current vector, it can be shown that the characteristic polynomial of the system is the numerator of [29,43]:

$$\left(1 + \sum_{j=1}^{N} \frac{(s - J_{j0}) Z_L - J_{j*}}{(s - J_{j0}) Z_j + J_{j*} - J_{jj}} \right) \left(\prod_{k=1}^{N} [(s - J_{k0}) Z_k + J_{k*} - J_{kk}] \right) = 0 \; . \tag{5.12}$$

The stability and dynamics of the system can be found by solving for the roots of this equation, or through the use of other stability criteria. Thus, under the conditions outlined in the above section, the stability and dynamics of a distributed nonlinear current-sharing control system can be determined about a specified operating point.

5.2 Application of the Linearization-Based Approach

To illustrate the application of this analysis technique and demonstrate its validity, we consider the

nonlinear frequency-based current-sharing technique developed in Chapters 2 and 3. In this technique, each cell generates a signal whose frequency is related to its output current. The cells are able to calculate the root-mean-square of the generated frequencies. Each cell has a load-sharing controller which adjusts the local reference voltage based on the difference between its own generated frequency and the rms frequency.

The linearization-based analysis technique will first be applied to a very simple two-cell system and compared to simulation results. The approach will then be applied to the low-power system developed in Chapter 3, and compared to experimental results.

5.2.1 Simulation Example

We consider a simple two-cell example of frequency-based current sharing in which the cells have a resistive output impedance characteristic. The frequencies generated by the cells are related to their output currents in the following manner:

$$\begin{aligned} f_1 &= a + bi_1 \\ f_2 &= a + bi_2 \end{aligned} \tag{5.13}$$

and the cells base their load-sharing control on the rms frequency

$$f_{rms} = \sqrt{\frac{f_1^2 + f_2^2}{2}} \ . \tag{5.14}$$

We consider the case where the individual cells adjust their references via integral control:

$$\frac{dv_{r,1}}{dt} = c\left[f_{rms} - f_1\right] = g_1(v_{r,1}, i_1, i_2) \tag{5.15}$$

and

$$\frac{dv_{r,2}}{dt} = c\left[f_{rms} - f_2\right] = g_2(v_{r,2}, i_1, i_2) \ . \tag{5.16}$$

Calculating the parameters of (5.4), we find

$$
\begin{aligned}
J_{10} &= J_{20} = 0 \\
J_{11} &= J_{22} = -\frac{bc}{2} \\
J_{12} &= J_{21} = \frac{bc}{2} \\
Z_L &= \frac{R_L}{sC_fR_L + 1}
\end{aligned}
\tag{5.17}
$$

The following system parameters are selected: $C_f = 10$ μF, $Z_1 = Z_2 = 66.67$ Ω, $a = 1$ kHz, $b = 1$ kHz/A, and c = 1000 V/(kHz-s). We consider the dynamics about the operating point $v_o = 370.3$ V and $v_{r1} = v_{r2} = 395$ V, which corresponds to a load resistance R_L of approximately 500 Ω and cell output currents $I_1 = I_2 = 0.37$ A. Substituting the numerical values of the parameters into (5.12) and simplifying yields

$$(s + 3200)(s+15)s = 0 \tag{5.18}$$

which indicates that the system has poles at -3200, -15, and 0 Np/Sec.

To validate this result, we simulate the system and endeavor to identify each natural frequency and its associated eigenvector. The system was first simulated from an initial condition in which v_o, v_{r1} and v_{r2} were all at 395 V, yielding an initial condition vector in the direction of $[\,1, 0, 0\,]^T$, where the state vector of the linearized system is defined as $[\hat{v}_o, \hat{v}_{r1}, \hat{v}_{r2}]^T$. The response to this initial condition was that the reference voltages remained constant at their steady-state values, while the output voltage

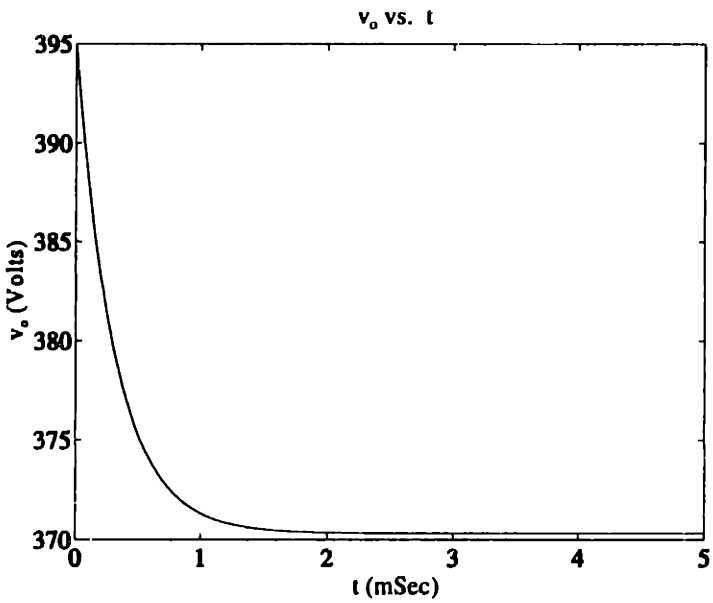


Figure 5.2 Output voltage response from initial condition $v_o = v_{r1} = v_{r2} = 395$ V.

decayed to its steady-state value as shown in Fig. 5.2. This first-order response is consistent with a pole located at s = -3200 Np/s as estimated by its 63% fall time. Furthermore, because the response remained in the direction of the initial condition vector, we conclude that the initial condition vector is the eigenvector corresponding to this pole.

Next, the system was simulated from an initial condition in which v_o was at its steady-state value of 370.3 V, v_{r1} was 400 V and v_{r2} was 390 V, yielding an initial condition vector in the direction $[\ 0,\ 1,\ -1]^T$. The response to this initial condition was that the output voltage remained at its steady state value, while the reference voltages transitioned to their steady-state values as shown in Fig. 5.3. This differential-mode response corresponds to a pole at s = -15 Np/Sec with its eigenvector in the direction of the initial condition.

Finally, the system was simulated from an initial condition in which v_o was at 375 V, while v_{r1} and v_{r2} were both at 400 V. This corresponds to an initial condition vector in the direction $[\ k,\ 1,\ 1\ ]^T$, where

$$k = \frac{R_L Z_1 + R_L Z_2}{R_L Z_1 + R_L Z_2 + Z_1 Z_2} \tag{5.20}$$

which is the voltage division ratio between the paralleled cell output resistances and the load resistance. Simulation of the system resulted in a response which remained static at this initial condition. This can be viewed as corresponding to a pole at s = 0 (an infinitely slow first-order decay) with an eigenvector in the direction of the initial condition. It should be pointed out that this initial condition (and any other in the direction of $[\ k,\ 1,\ 1]$ which falls within the allowed range of reference adjustment) represents a steady-state operating point of the system. This is due to the integral control law used for current balancing in this example. Adoption of a controller with finite dc gain (such as a first-order, high-gainlow-pass filter) would result in all the poles appearing strictly in the left half plane.

It may be concluded that, at least for this simple example, the presented linearization-based approach accurately predicts the system dynamics about an operating point. The three poles in the two-cell system correspond to the dynamics of the output voltage response, the differential-mode reference voltageresponse, and the (weighted) common-mode response of the output voltage and reference voltages.

5.2.2 Experimental Example

To further validate the approach, we analyze a two-cell converter system of the type developed in

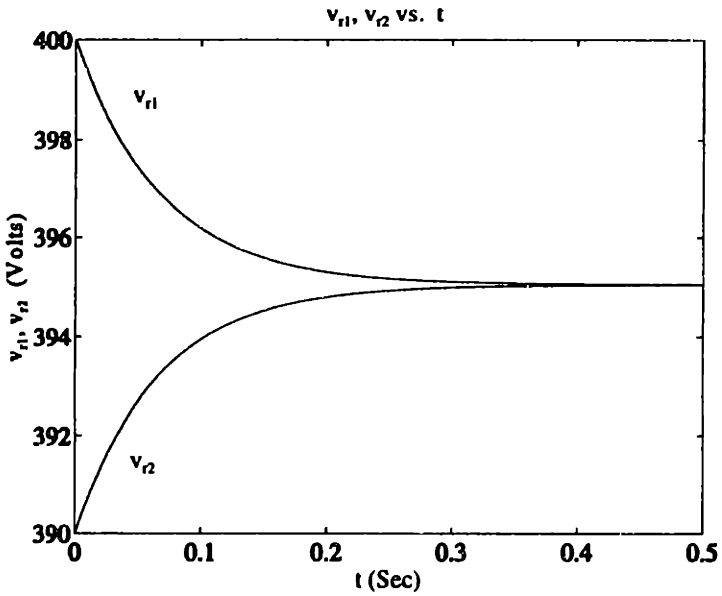


Figure 5.3 Reference voltage response from initial condition $v_o = 370.3$ V, $v_{r1} = 400$ V, and $v_{r2} = 390$ V.

Chapter 3, and compare the analytical predictions to experimental results. We begin by developing a model for the system of the form of Fig. 5.1, and then proceed to analyze the current-sharing dynamics of the system.

We model each converter cell as a voltage source of the value of the cell reference voltage in series with an output impedance. The appropriate output impedance can be determined by examining the cell control characteristics. Figure 5.4 shows a block diagram of the cell control structure used in the experimental system. The voltage control loop operates with the current-controlled power stage to generate a cell output current that depends on the error between the output voltage and the local reference voltage. The output voltage controller used in the prototype system yields a transfer function from error voltage v_{err} to cell output current i_{out} of

$$\frac{i_{out}}{v_{err}}(s) = \frac{125}{0.18s + 1} \quad \frac{mA}{V} \tag{5.21}$$

which corresponds to a cell output impedance of

$$Z_j(s) = \frac{0.18s + 1}{125} \quad \frac{V}{mA} \quad . \tag{5.22}$$

This cell output impedance, which can be represented as the series combination of a resistor (8 Ω) and an inductor (1.42 H), appears in series with each cell's reference voltage in the model of Fig. 5.1. The

parallel combination of the filter capacitance and load resistance forms a load impedance

$$Z_L = \frac{R_L}{sC_f R_L + 1} \tag{5.23}$$

which completes the model of Fig 5.1.

We now analyze the current-sharing control mechanism used in the prototype system. To achieve current-sharing, each cell in the prototype system encodes information about its output current in the frequency of an output perturbation signal, and adjusts its reference voltage based on the difference between its own perturbation frequency and the rms of the two perturbation frequencies. As with the previous example, current-sharing information is encoded via the relations **(5.13)**, with a = 5 kHz and b = 0.2 kHz/mA for the prototype system. In the control circuitry of the prototype system, frequency values are represented as voltages using a scaling factor of 1 V/kHz. Expressing frequency values in **(5.13)** in terms of their equivalent voltages yields the representation:

$$\begin{aligned} v_{\omega,1} &= a' + b' i_1 \\ v_{\omega,2} &= a' + b' i_2 \end{aligned} \tag{5.24}$$

where a' = 5 V, and b' = 0.2 V/mA.

Each cell computes an estimate of the rms value of the perturbation frequencies. Neglecting the dynamics of the estimation process, and expressing frequency values in terms of equivalent voltages, the rms frequency estimate can be expressed as

$$v_{\omega,est} = \sqrt{\frac{v_{\omega,1}^2 + v_{\omega,2}^2}{2}}\,. \tag{5.25}$$

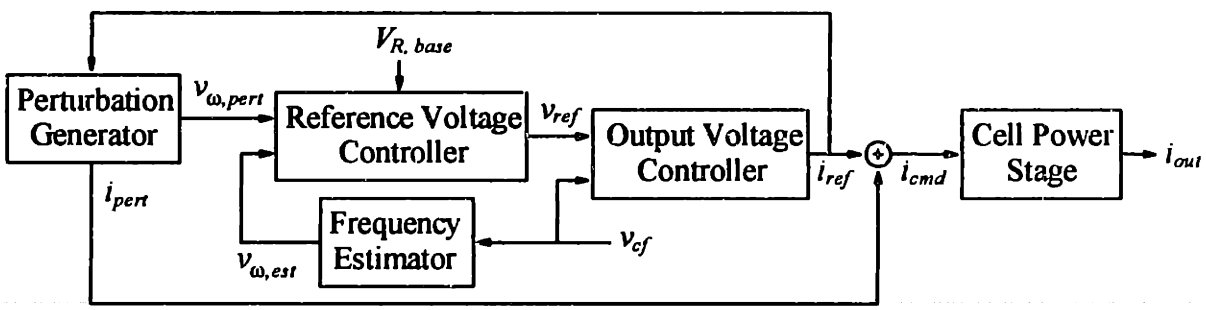


Figure 5.4 Block diagram of the control structure for a cell.

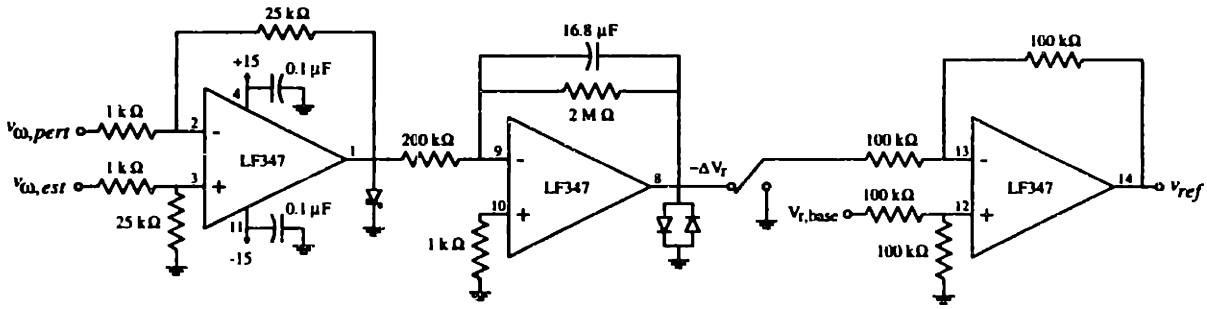


Figure 5.5 The load-sharing compensator used in the prototype converter system.

Current-sharing is achieved in the experimental system by adjusting the local cell reference voltages within limits about a base value $V_{r,base}$. As shown in Fig. 3.11, repeated here as Fig. 5.5, each cell has a high gain, single-pole compensator which generates the adjustment Δv_r based on the difference between the local cell perturbation frequency $v_{\omega pert}$ (equal to $v_{\omega k}$ for the k^{th} cell) and the estimated rms frequency $v_{\omega est}$. The differential equation describing the adjustment of the local cell reference voltage is

$$\begin{aligned} \frac{d\Delta v_r}{dt} &= C_A(v_{\omega,est} - v_{\omega,pert}) - C_B\Delta v_r \\ &\approx 0.3(v_{\omega,est} - v_{\omega,pert}) - 0.03\Delta v_r \end{aligned} \tag{5.26}$$

which may also be expressed in the form

$$\frac{d\Delta v_r}{dt} = g(\Delta v_r, i_1, i_2) \tag{5.27}$$

using the relations **(5.24)** and **(5.25)**. Computing the partial derivatives in the expansion **(5.4)**, we find

$$\begin{aligned} J_{10} &= J_{20} = -C_B \approx -0.03\ s^{-1} \\ J_{11} &= J_{22} = -\tfrac{1}{2}bC_A \approx -0.03\ V/mA \\ J_{12} &= J_{21} = \tfrac{1}{2}bC_A \approx 0.03\ V/mA \end{aligned} \tag{5.28}$$

for perturbations away from steady-state operating points where $I_1 = I_2$. Forming **(5.12)** for this system and factoring yields

$$(s + 556.9)(s + 7638.6)(s + 0.03)(s + 2.79 + j5.83)(s + 2.79 - j5.83) = 0. \tag{5.29}$$

We now compare the dynamics predicted in **(5.29)** to the behavio. of the exp nental system. The leftmost two poles in **(5.29)** match those of a single-cell system in which the single cell has a fixed reference voltage and exactly half of the output impedance of the cells in the two-cell system. These poles thus correspond to the common-mode response of the two cells to disturbances in the output voltage. Figure 5.6 shows the output voltage response to a load step from 349 Ω to 390 Ω. The transient

response is composed of a voltage increase with a fast time constant, followed by a decay at a slower time constant. (The small, high-frequency ripple in the output voltage is a perturbation component used to carry current-sharing information in the experimental system.) For comparison, Fig 5.7 shows the ac response to a similar load step of the single-cell "common mode" system, which has its poles at the locations of the leftmost two terms of **(5.29)**. From the similarity of the rise and fall times seen in figures 5.6 and 5.7, we conclude that **(5.29)** predicts the common-mode dynamic behavior of the experimental system to within reasonable experimental accuracy.

The remaining three pole locations in **(5.29)** describe the dynamics of the reference adjustment and current-sharing process. Figure 5.8 shows the reference current response of the cells during a large-signal transient induced by making electrical connections which disturbed the cell reference voltages. During this transient, the output voltage remained relatively unchanged, while the swings in current sharing occurred as the current-sharing control loops adjusted the reference voltages to re-establish current sharing. Based on the natural frequency and the damping ratio, the observed time response matches that of a system with a zero at $s = 0$ and poles at $s = -2.9 \pm j5.0$. This corresponds reasonably well to the complex pole pair at $s = -2.8 \pm j5.8$ predicted by the linearized analysis, especially given the

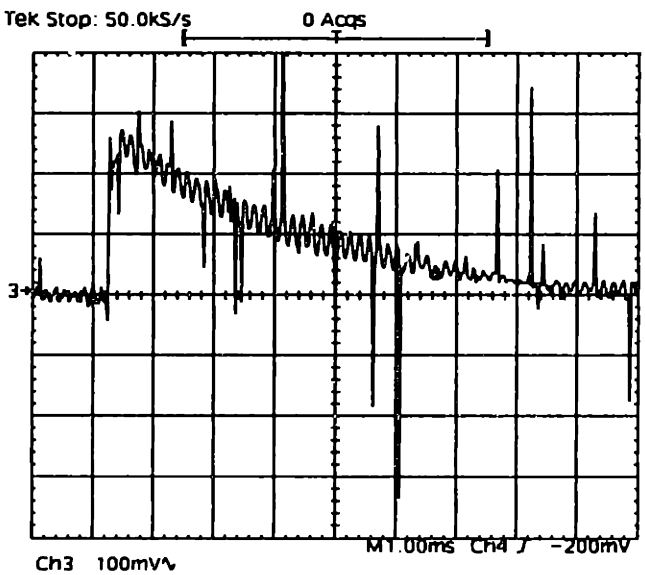


Figure 5.6 Voltage response of the two-cell experimental system to a load step from 349 Ω to 390 Ω.

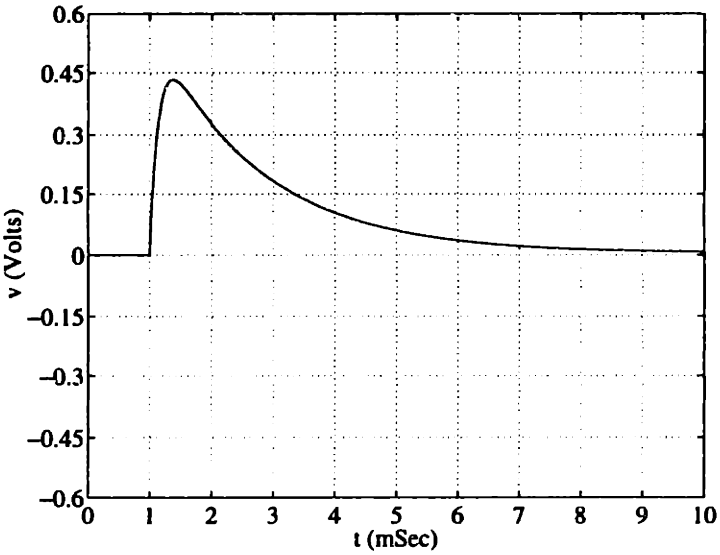


Figure 5.7 Response of the single-cell averaged model of Fig 5.6 to a step in load from 349 Ω to 390 Ω. This response has poles at s = -557 and s = -7639.

large-signal nature of the transient.

Behavior associated with the remaining pole predicted by the linearized analysis was also sometimes observed after the reference voltages were disturbed, especially when the disturbance was severe. After such a disturbance, a small, very slow adjustment of the output voltage (and cell currents) to a final steady-state value could sometimes be observed, typically ending with the reference voltages near the

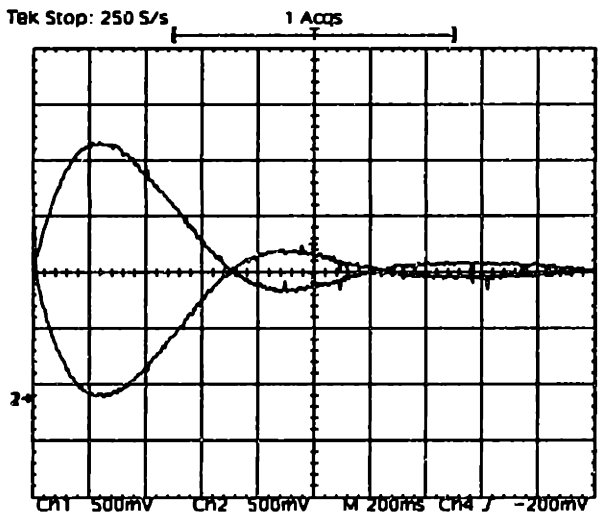


Figure 5.8 Dynamic response of the cell reference currents to a disturbance of the reference voltages in the two-cell experimental system while operating at a load resistance of 390 Ω.

edge of their adjustment range. When observed, this adjustment took as much as twenty or more seconds to complete, with an approximately linear transition to a final value. This behavior matches that of a slow first-order response which saturates before reaching its final value (due to the clamping of the reference voltage adjustments), and is at least qualitatively consistent with the pole at $s = -0.03$ predicted by the linearized analysis.

What may be concluded from these results is that the presented approach allows prediction of system stability and dynamics about an operating point for nonlinear feedback control laws which are linearizable. This is useful, since many load-sharing control methods rely on such nonlinear feedback control laws.

5.3 Analysis of the Load-Sharing Control Method used in the UC3907

While the preceding analysis is useful for a broad range of load-sharing control methods, others are not amenable to this approach due to the difficulty of linearizing the system or due to the limited range of perturbations for which the linearized analysis is accurate. One widely-used load-sharing method which is not easily handled by linearization is the peak-current control scheme implemented the UC3907 load-sharing control IC [32]. Dynamic analyses of the master-slave current-sharing technique (in which the local cells compare their currents to that of a fixed master) are sometimes employed to predict the behavior of the peak-current control scheme of the UC3907 [43,44]. However, in the UC3907 method, the cell carrying the highest current acts as master, and the master designation can switch dynamically among cells with current-sharing perturbations of just a few percent. This can lead to behavior not predicted by these analyses. This section will establish an important special case in which the master cannot switch, thus allowing the system to be easily analyzed.

The load-sharing control scheme implemented in the UC3907 operates as follows: Each cell shifts its own voltage reference via integral control based on the difference between its own output current and the maximum output current of all the cells minus a small offset; i.e.

$$\frac{dv_{r,j}}{dt} = \begin{cases} K_j[i_{\max} - \Delta I - i_j] & for \quad v_{r,j,base} < v_{r,j} < v_{r,j,\max} \\ 0 & otherwise \end{cases} \tag{5.30}$$

where K_j and i_j are the (integral) control gain and output current of the j^{th} cell, i_{max} is the maximum output current of all of the cells, and ΔI is a small offset. The j^{th} reference is adjustable over a small range from

a base value $v_{r,j,base}$ to a maximum value $v_{r,j,max}$, and is prevented from going outside of this range by clamping of the reference at the boundaries. The offset ΔI ensures that the highest-current cell will carry slightly more current than the other cells under static conditions, thus preventing the maximum current signal from chattering among different cell currents. The offset also guarantees that the voltage reference of the highest-current cell will always be driven towards its base value.

The dynamics of this current-balancing control scheme will be analyzed for the case where the output impedances of the cells are resistive. This is typical of current-mode controlled converters under proportional control, for example. We will first analyze the case where the cell output resistances are constant, and then consider the case where the output resistances vary with load. We will also make the simplifying assumption that all the cells are identical except for their references and current-sharing control gains. That is, it is assumed that the cells all have identical output impedances, sensor gains, etc. While these assumptions are somewhat limiting, they are still reasonable for many cases of practical interest, including the high-power cellular converter system developed in Chapter 8.

5.3.1 Analysis for Constant Cell Output Impedances

We first consider the case in which the cell output impedances are constant across load. As shown in Fig. 5.9, the j^{th} cell is modeled as voltage source $v_{r,j}$ (equal to the reference voltage) in series with a cell output impedance $R_j = G_j^{-1}$. The j^{th} cell thus has output current

$$i_j = G_j[v_{r,j} - v_o] \ . \tag{5.31}$$

For the considered case of identical constant cell output admittances ($G_1 = \cdots = G_N = G_{out}$) a cell with a higher reference voltage always carries more current than a cell with a lower reference voltage. We will assume without loss of generality that the N^{th} cell has the highest base reference voltage. Because the offset ΔI always drives the highest current cell's reference towards its base value, within a short time after startup the N^{th} cell will have the highest reference voltage and output current.

Using **(5.31)** , we can express the sensitivity of differences in cell currents to changes in output voltage as

$$\frac{\partial}{\partial v_o}[i_j - i_k] = G_j - G_k \ . \tag{5.32}$$

It may be inferred from this equation that for the case of identical output impedances, differences

between the cell currents do not depend on the output voltage. This means that the N^{th} cell will carry the highest current permanently, regardless of changes in output voltage (yielding $i_{max} = i_N$). Under this condition, the control scheme is easily analyzed using frequency-domain techniques already developed for Master-Slave current-sharing control [43,44], or through time-domain analysis. (One slight difference between the UC3907 control law **(5.30)** and the forms used in **(5.1)** or in [43] is the existence of the constant term ΔI. However, this element is easily accommodated, and does not affect the resulting natural frequencies.) Furthermore, due to the structure of the control law **(5.30)**, the reference voltage adjustment process is not influenced by changes in output voltage.

While the control scheme can be easily analyzed via frequency-domain techniques for this special case, a time-domain analysis is presented here to clearly illustrate the reference adjustment process. The system will be analyzed for a capacitive output filter and an *R-L-E* load, though other cases are easily handled. During operation, the reference voltage of the maximum-current cell (the N^{th} cell) is always "frozen" at its base value. Consider what happens when any other cell reaches one of its adjustment boundaries (and thus momentarily ceases to change). Both that cell's current and the N^{th} cell's current are then only affected by the output voltage, and the difference between the two cell currents is not affected by output voltage. As a result, there is no mechanism for the current-sharing error (which initially drove the cell's reference to the boundary) to change, and the reference of that cell will remain permanently frozen there. Similarly, if the error term in **(5.30)** driving the reference change of a cell reaches zero (implying that the cell is carrying exactly ΔI less current than the N^{th} cell), that cell's reference voltage will become permanently frozen. Thus, if the rate of change of a cell's reference voltage *ever* goes to zero (as determined in **(5.30)**), the cell's reference will be frozen permanently at that value.

Consider the dynamics of such a system where M of the N cells have "active" or "unfrozen" references, while the other K-N references are frozen at constant values. Arbitrarily grouping the "active

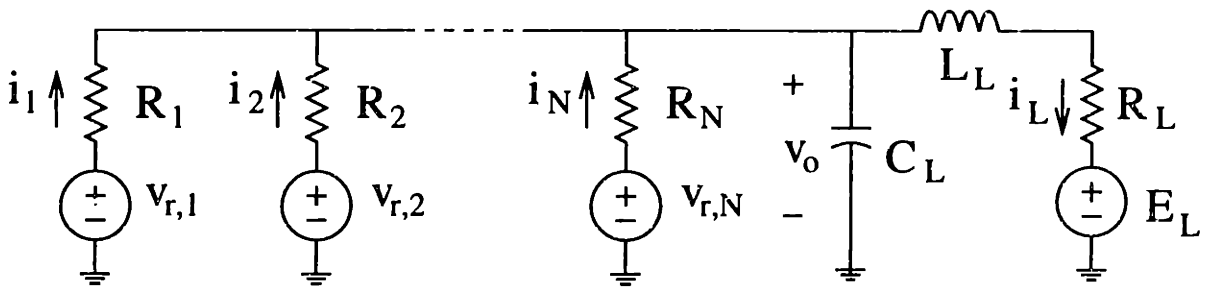


Figure 5.9 A model for an N-cell parallel converter system with resistive cell output impedances, a capacitive output filter, and an *R-L-E* load.

reference" cells as the first M cells, we write

$$\begin{aligned}\frac{\partial v_{r,j}}{\partial t} &= K_j(i_{max} - \Delta I - i_j) \\ &= K_j G_N(v_{r,N} - v_o) - K_j \Delta I - K_j G_j(v_{r,j} - v_o)\end{aligned} \tag{5.33}$$

for $1 \le j \le M$. Each of these equations is valid until the reference becomes "frozen" as described above. We express the output voltage and current dynamics as

$$\frac{dv_o}{dt} = \frac{1}{C_L}\left[-i_L + \sum_{j=1}^{N} G_j(v_{r,j} - v_o) \right] \tag{5.34}$$

and

$$\frac{di_L}{dt} = \frac{1}{L_L}\left[v_o - i_L R_L - E_L \right]. \tag{5.35}$$

Describing this in a state-space format (which is valid until a reference becomes "frozen", thus changing the system), we get

$$\dot{x} = Ax + Bu \tag{5.36}$$

where

$$x = [i_L \quad v_o \quad v_{r1} \quad v_{r2} \cdots v_{rM}]^T \tag{5.37}$$

$$u = [E_L \quad \Delta I \quad v_{r,M+1} \quad v_{r,M+2} \cdots v_{r,N}]^T \tag{5.38}$$

$$A = \begin{bmatrix} -\frac{R_L}{L_L} & \frac{1}{L_L} & 0 & 0 & \cdots & 0 \\ -\frac{1}{C_L} & -\frac{1}{C_L}\sum_{i=1}^{N} G_i & \frac{G_1}{C_L} & \frac{G_2}{C_L} & \cdots & \frac{G_k}{C_L} \\ 0 & K_1(G_1 - G_N) & -K_1 G_1 & 0 & \cdots & 0 \\ 0 & K_2(G_2 - G_N) & 0 & -K_2 G_2 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & K_M(G_M - G_N) & 0 & 0 & \cdots & -K_M G_M \end{bmatrix} \tag{5.39}$$

$$B = \begin{bmatrix} -\frac{1}{L_L} & 0 & 0 & 0 & \cdots & 0 \\ 0 & 0 & \frac{G_{M+1}}{C_L} & \frac{G_{M+2}}{C_L} & \cdots & \frac{G_N}{C_L} \\ 0 & -K_1 & 0 & 0 & \cdots & K_1 G_N \\ 0 & -K_2 & 0 & 0 & \cdots & K_2 G_N \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & -K_M & 0 & 0 & \cdots & K_M G_N \end{bmatrix} \tag{5.40}$$

The natural frequencies of the system are the eigenvalues of the A matrix, and only change when a reference "freezes". Under the assumption that the converter output impedances are identical, we have

$$A = \begin{bmatrix} -\frac{R_L}{L_L} & \frac{1}{L_L} & 0 & 0 & \cdots & 0 \\ -\frac{1}{C_L} & -\frac{NG}{C_L} & \frac{G}{C_L} & \frac{G}{C_L} & \cdots & \frac{G}{C_L} \\ 0 & 0 & -K_1 G & 0 & \cdots & 0 \\ 0 & 0 & 0 & -K_2 G & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & -K_M G \end{bmatrix} \tag{5.41}$$

from which the natural frequencies are easily identified. The "active" references respond with first-order time constants

$$\tau_j = \frac{1}{GK_j} \tag{5.42}$$

(i.e. with pole locations $s_j = -GK_j$). As can be seen from the special structure of the matrix **(5.41)**, the load dynamics are decoupled from the reference adjustment dynamics. The poles associated with the load are at

$$s = -\left[\frac{R_L}{2L_L} + \frac{NG}{2C_L}\right] \pm \sqrt{\left[\frac{R_L}{2L_L} + \frac{NG}{2C_L}\right]^2 - \frac{1 + NGR_L}{L_L C_L}} \tag{5.43}$$

and correspond (not surprisingly) to the pole locations of the circuit of Fig. 5.9 with all voltage sources fixed.

Under the presented assumptions, the behavior of a parallel converter system using this load-sharing scheme is large-signal linear, and can be easily determined via piecewise linear modeling. The linear model **(5.27)** is used, with the system matrices changing as the number of active references change. Under these assumptions, the system dynamics are always stable, and the load dynamics are decoupled from the current-sharing dynamics.

5.3.2 Analysis for Load-Dependent Output Impedances

The preceding analysis is valid for cases where the cell output resistances do not change with operating point. However, in many systems, including the switched mode rectifier explored in Chapter 8, the cell output impedances are resistive but vary with load. We now analyze this case, with the objective of establishing what differences in behavior can be expected from the preceding case.

We consider the case where the output current of each cell is a monotonic (increasing) function $f(\cdot)$ of the error between the cell reference voltage and the output voltage:

$$i_{out,k} = f(v_{r,k} - v_o) = f(v_{err,k}) \ , \tag{5.44}$$

and define the cell output admittance at a nominal output voltage as:

$$G_k = \frac{1}{R_k} = \frac{\partial f}{\partial v_{err}}\Big|_{V_{err}} \ . \tag{5.45}$$

In essence, we address the case where the output voltage of a cell increasingly droops as more current is drawn from it, and define the output resistance at a specific operating point as the negative of the droop characteristic slope at that point.

In the load-varying output resistance case, a cell with a higher reference voltage still always carries more current than a cell with a lower reference voltage. As a result, a single cell will always act as the master, and the small signal dynamics about an operating point can still be easily evaluated. However, for large-signal disturbances there is some dissimilarity from the constant output resistance case. When the cell output resistances vary across load, the difference between the j^{th} cell's current and the N^{th} cell's current (which appears in **(5.30)**) is a function of the output voltage. To see this, consider Fig. 5.10.

Figure 5.10 (a) shows the difference in cell currents for two different operating points when the output resistances are identical and constant with load current. As can be seen in the figure (as well as from the result of **(5.32)**), the difference between cell currents does not depend on output voltage. However, as shown in Fig 5.10 (b), the difference in cell currents does depend on the output voltage when the resistances are identical but load-varying.

This fact can have a strong impact on the current-sharing behavior of a parallel system using this control method. Consider the two-cell case. The control law **(5.30)** drives the non-dominant cell reference voltage until it operates at a current ΔI below that of the dominant cell (assuming that it does not hit its adjustment boundary first). If the cell output resistances change heavily with load, the voltage reference difference required to support this ΔI difference is small where the output resistances are low, and large where the output resistances are high. This means that the non-dominant reference needs to

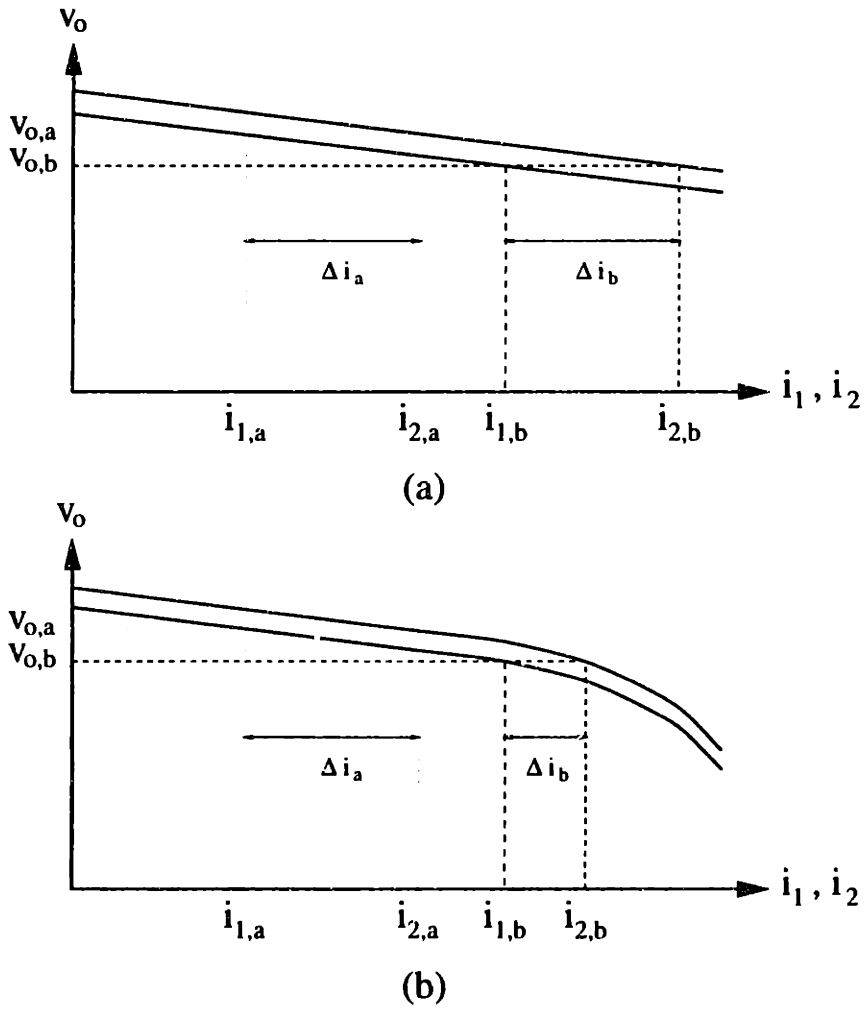


Figure 5.10 Load-line diagrams illustrating current-sharing behavior for a two-cell system. (a) Constant cell output resistances. (b) Load-varying cell output resistances.

re-adjust under different loading conditions. Furthermore, whenever the loading condition changes from an operating point where the output resistances are high to an operating point where the output resistances are low, the current imbalances during the adjustment process can be significant. What may be concluded from this is that in systems where the output resistances vary heavily across load, load changes can dramatically and repeatedly disturb the current sharing among cells. This contrasts with the case of constant output resistances, in which the current-sharing dynamics are decoupled from the output dynamics even for large-signal disturbances and current sharing is permanently maintained once established. It should be pointed out that the degree to which this is an issue is a function of how much the output resistances vary across the load range. The less the output impedances vary across load, the smaller the possible current-sharing disturbance during a load change.

While the load-sharing dynamics and output dynamics are not decoupled, they are stable. Given a constant load, the output voltage will settle stably with dynamics that depend on the nonlinear damping of the cell output resistances. This typically occurs on a much shorter time scale than the reference adjustment process. Given a constant output voltage, the control law **(5.30)** will drive the non-dominant references monotonically to their steady-state values, and the cell currents will also transition monotonically to their steady-state values. Thus, while there are significant differences between the constant and load-varying output resistance cases, both have stable, predictable dynamics.

5.3.3 Experimental Example

To verify the analysis approach and demonstrate its use, we analyze a two-cell system utilizing UC3907 load-sharing IC's, and compare the analytical predictions to experimental results. As illustrated in Fig. 5.11, each cell is a low-power linear regulator whose reference voltage is derived from the adjusted internal reference of the UC3907. The simple op-amp circuit connected to the UC3907 generates a no-load cell output voltage that is exactly twice the adjusted internal reference voltage (i.e. 4.0-4.2 V). Each cell has an output resistance of 4.7 Ω (due to the current-sense resistor at the cell output) and can deliver a full-load current of 30 mA. The two-cell system has a 10 μF output filter capacitance, and drives an *R-L* load, where L = 1.4 mH.

The gain of the load-sharing compensation integrator, K_j, can be computed as the product of the current-sense resistor value, the current sense amplifier gain (20), the adjustment amplifier transconductance (0.003), the internal gain (0.057), and the external gain (2), all divided by the compensation capacitor value. The 4.7 μF compensation capacitor used in the prototype system yields a reference adjustment gain K_j of approximately 6857 V/(A-S), with a significant amount of possible

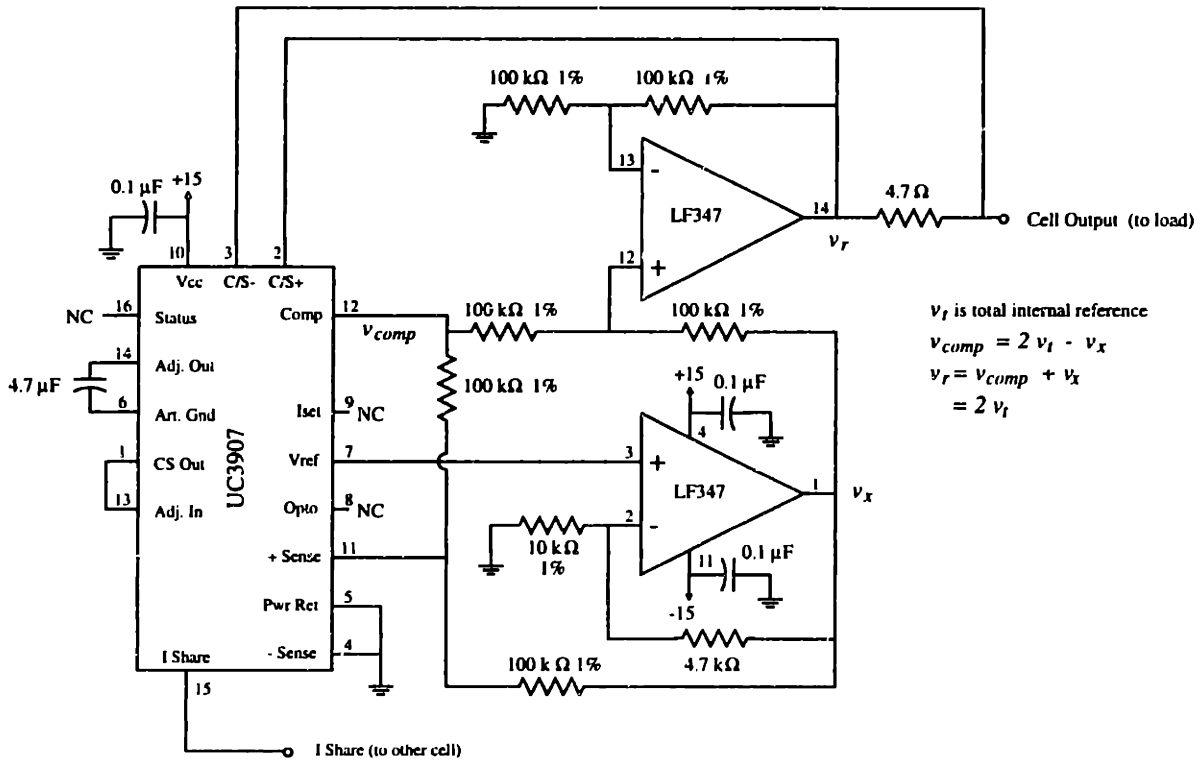


Figure 5.11 A low-power linear regulator cell used to test the dynamics of the UC3907 load-sharing IC. The no-load output voltage of the cell is twice the value of the UC3907 internal reference voltage.

variability (3690 to 10800 V/(A-s)) due to the uncertainty in parameters such as the adjustment amplifier transconductance.

Given this value of K_p **(5.42)** predicts first-order current-sharing adjustment dynamics with a time constant of approximately 685 µs. Figure 5.12 shows the transient response of the cell output currents when a short on the current-sharing line is removed (with R_L = 3.3 kΩ). When the short is removed, the references of both cells are at their lowest values. The reference of the master remains at this value when the short is removed, while the other cell raises its reference voltage to achieve current sharing. The reference adjustment response has a forced component, due to the offset ΔI, as well as a natural component. From the 63% rise time of the response, we estimate a time constant of about 1.2 ms, which is consistent with the predicted dynamics to within the level of parameter uncertainty in the UC3907.

Figure 5.13 shows the transient response of the prototype system to load steps between 90 Ω and 1000 Ω. For the load step to 1000 Ω, the system poles are located at -500,000 and -41,000 Np/s (as estimated by the 63% rise times of Fig. 5.13 (a)), while **(5.43)** predicts poles at s = -717180 and -42260 Np/s. Similarly, for the load step to 90 Ω, **(5.43)** predicts pole locations of -60249 and -46590 Np/s. The actual position of one pole (at -66,000 Np/s) is easily estimated from the load resistor voltage

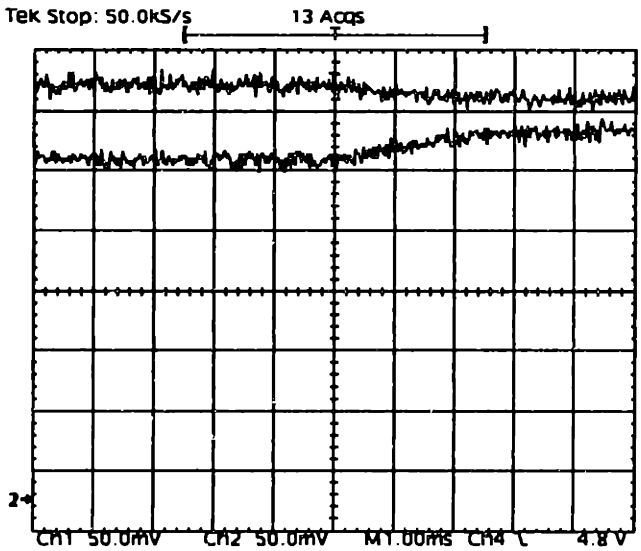


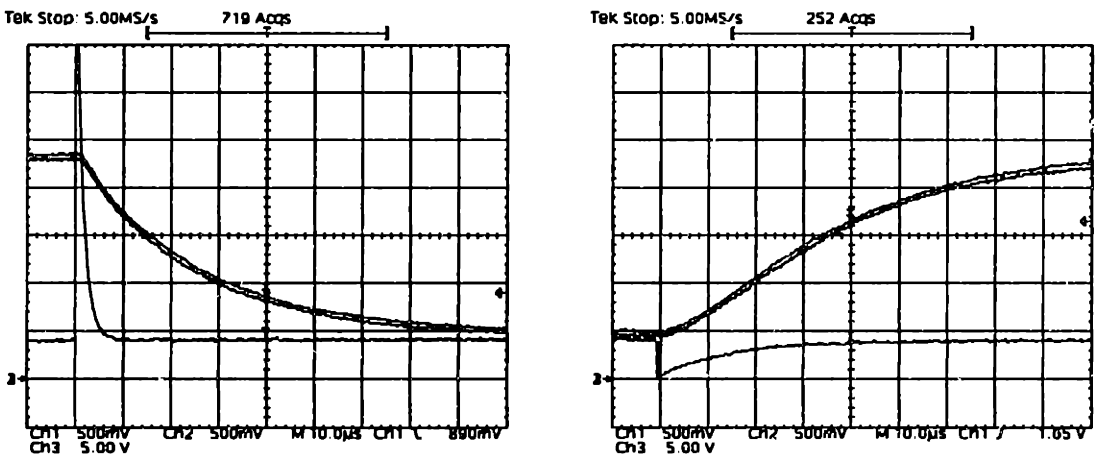
Figure 5.12 Transient response of the cell output currents to the removal of a short circuit on the current-sharing line at $t = 0$. Recorded signals correspond to the outputs of the current-sense amplifiers, with the system operating at a load resistance of 3.3 kΩ.

response in Fig. 5.13 (b). However, the other pole location is harder to identify directly, since both poles contribute to the cell current responses and the poles are not widely separated. Nevertheless, comparisons to simulations indicate that the predicted pole location corresponds accurately to the observed response. The predictions thus closely match the observed responses. Furthermore, current-sharing is not disturbed by these large load steps, indicating that, as predicted, current-sharing is not affected by changes in output voltage, and the reference adjustment dynamics are decoupled from the output voltage dynamics. What may be concluded from these results is that, under the constraints on which it is based, the dynamics of a system employing the UC3907 load-sharing IC can be accurately predicted.

5.4 Conclusion

The ability to predict the load-sharing dynamics is an important aspect of the design of a cellular converter system. This chapter addressed the analysis of systems employing nonlinear distributed load-sharing techniques. Section 5.1 presented a methodology for analyzing nonlinear load-balancing control methods which are linearizable about an operating point, while Section 5.2 applied this approach to the load-balancing control scheme of Chapter 3. The approach is was demonstrated and validated through both simulation and experiment. Section 5.3 addressed the dynamics of a widely-used technique which

is not easily handled by linearization in the general case. The dynamics of this control scheme have been established for an important special case, and validated against experimental results.



(a) (b)

Figure 5.13 Transient response of the prototype system output voltage and cell currents to load steps: (a) From 1000 Ω to 90 Ω. (b) From 90 Ω to 1000 Ω. Channels 1 and 2 show the current-sense amplifier outputs, while channel 3 shows the output voltage.

Chapter 6

Ripple Cancellation in Cellular Converter Systems

6.1 Introduction

One of the primary benefits of a cellular conversion approach is the large degree of input and output ripple cancellation which can be achieved among cells, leading to reduced ripple in the aggregate input and output waveforms. Consider operation of the N-cell parallel converter system shown in Fig. 6.1. If all of the cells are clocked synchronously, as illustrated in Fig. 6.2 (a) for a two-cell system, then the system behaves exactly as a single large converter. However, as we will show in section 6.2, if the cells are clocked independently (and hence operate at slightly different frequencies) as illustrated in Fig. 6.2 (b), the rms input and output current ripples will be reduced by a factor of $N^{1/2}$ due to the passive (*stochastic*) ripple cancellation which occurs among cells. Active ripple cancellation methods can yield even higher performance benefits. The active method of *interleaving*, illustrated in Fig. 6.2 (c), is well known. (See [7] for a review.) In the interleaving method, the cells are operated at the same switching frequency with their switching waveforms displaced in phase over a switching period. The benefits of this technique are due to harmonic cancellation among the cells, and include low ripple amplitude and high ripple frequency in the aggregate input and output waveforms. For a broad class of topologies, interleaved operation of N cells yields an N-fold increase in fundamental current ripple frequency, and a reduction in peak ripple magnitude by a factor of N or more compared to synchronous operation [7-10].

This chapter investigates passive and active ripple cancellation techniques which are well suited to a cellular architecture. The degree of passive ripple cancellation expected among the cells of a parallel converter system is analytically quantified for the case of independently clocked cells. It is shown that the rms ripple current of an N-cell parallel converter system with independent clocking is a factor of $N^{1/2}$ lower than for the case where the clocks are synchronized. The chapter also introduces a distributed implementation of the interleaving method of ripple cancellation. The distributed implementation requires no centralized control, automatically accommodates varying numbers of converter cells, and is

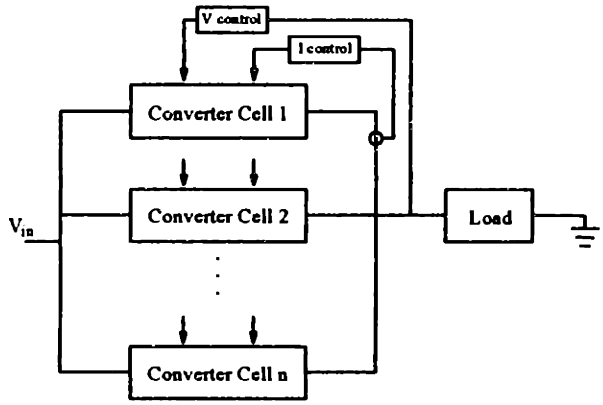


Figure 6.1 A cellular converter system supplying a single load.

highly tolerant of subsystem failures. A three-cell prototype converter system implementing the distributed interleaving method is also presented. Experimental results from the prototype system corroborate the analytical predictions and demonstrate the benefits of the distributed interleaving approach.

6.2 Passive Ripple Cancellation

This section quantifies the amount of passive, or *stochastic*, ripple cancellation which occurs among paralleled converter cells which are clocked independently. We will show that rms input and output current ripple is reduced by a factor of $N^{1/2}$ with independent clocking as compared to

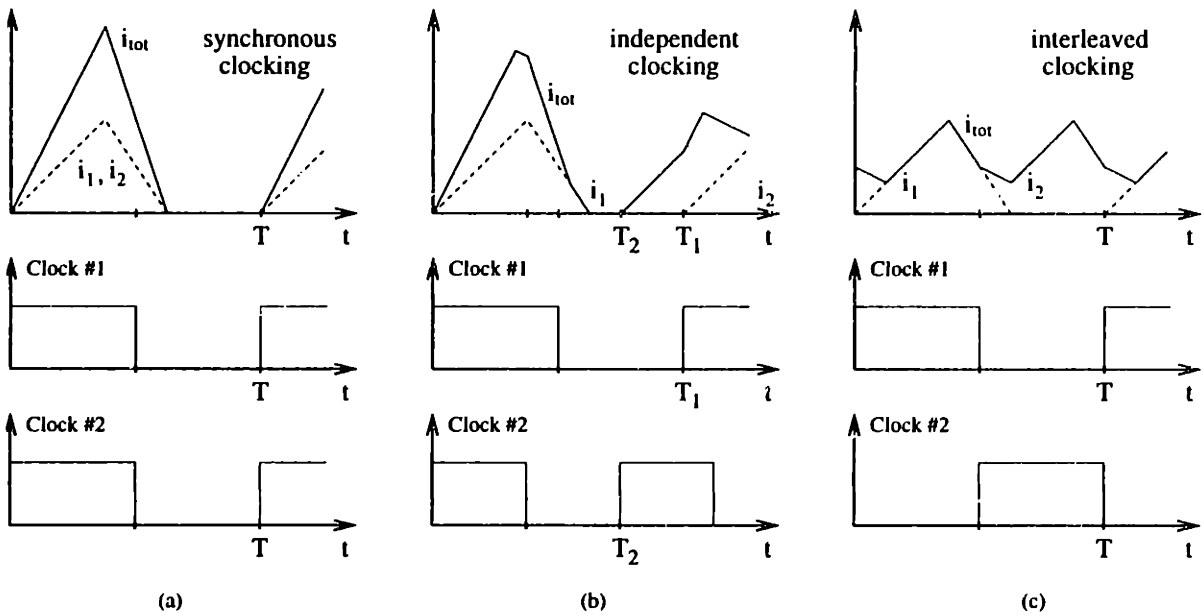


Figure 6.2 Clocking and cell current waveforms for paralleled power converters: (a) synchronous clocking, (b) independent clocking, and (c) interleaved clocking.

synchronized clocking of the cells (and as compared to an equivalent single converter). This derivation applies to the case of paralleled converters operating under fixed-frequency PWM control, though other cases are easily accommodated (see Chapter 7, for example).

Consider the output (or input) ripple current i_x due to N identical paralleled converter cells with synchronized clocks. The ripple current is exactly N times the ripple current due to a single cell, and can be expressed as a Fourier series

$$i_x = \sum_{n=-\infty}^{\infty} NC_n e^{jn\omega_o t} \tag{6.1}$$

where

$$\omega_o = \frac{2\pi}{T} . \tag{6.2}$$

The power spectral density of the ripple current is then

$$S_{i_x}(\omega) = 2\pi \sum_{n=-\infty}^{\infty} N^2 |C_n|^2 \, \delta(\omega - n\omega_o). \tag{6.3}$$

This yields an rms ripple current value of:

$$i_{x,rms} = \sqrt{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i_x}(\omega)d\omega} = \sqrt{\sum_{n=-\infty}^{\infty} N^2 |C_n|^2} . \tag{6.4}$$

Now we consider operation of the converter cells with independent clocking, where the k^{th} cell operates with a clock period $T_k \approx T$. We can express the ripple current of the k^{th} converter cell as:

$$i'_{rip,k} = \sum_{n=-\infty}^{\infty} C_{k,n} e^{jn\omega_k t} \tag{6.5}$$

where

$$\omega_k = \frac{2\pi}{T_k} \tag{6.6}$$

To first order, the shape and magnitude of the ripple current waveform does not change significantly with

small variations of the switching period T_k. Thus, as long as the switching periods of the cells are relatively close, we may approximate

$$C_{k,n} \approx C_n \ . \tag{6.7}$$

The percent error in Fourier magnitudes using this approximation is typically less than or equal to the percent difference between T_k and T. The power spectral density of the k^{th} cell's ripple current is

$$S_{i'_{ripk}}(\omega) = 2\pi \sum_{n=-\infty}^{\infty} |C_{k,n}|^2 \delta(\omega - n\omega_k) \ . \tag{6.8}$$

Because the T_k's are not identical due to independent clocking, the power spectral density of the total ripple current is the sum of the power spectral densities of the individual cell ripple currents. Thus, the power spectral density of the total ripple current i'_x is

$$\begin{aligned} S_{i'_x}(\omega) &= 2\pi \sum_{k=1}^{N} \sum_{n=-\infty}^{\infty} |C_{k,n}|^2 \, \delta(\omega - n\omega_k) \\ &\approx 2\pi \sum_{k=1}^{N} \sum_{n=-\infty}^{\infty} |C_n|^2 \, \delta(\omega - n\omega_k) \ . \end{aligned} \tag{6.9}$$

This leads to an rms ripple current of

$$i'_{x,rms} = \sqrt{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i'_x}(\omega)d\omega} \approx \sqrt{N \sum_{n=-\infty}^{\infty} |C_n|^2} \approx \frac{i_{x,rms}}{\sqrt{N}} \ . \tag{6.10}$$

Thus, the rms ripple current with independent clocking is a factor of $N^{1/2}$ lower than that obtained with synchronized clocking of the cells. A similar reduction in rms input and output voltage ripple is to be expected.

6.3 Distributed Interleaving

Interleaving is a widely used method of active ripple cancellation for paralleled power converters. Interleaving N parallel (or series) connected converter cells requires that the cells be operated at the same switching frequency but phase displaced with respect to one another by $2\pi/N$ radians. This is done in order to cancel the first N harmonic components in the aggregate input and output waveforms.

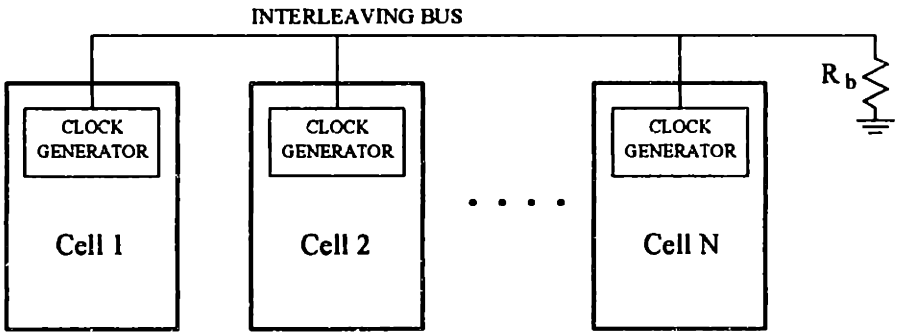


Figure 6.3 The distributed interleaving approach.

Interleaved operation is conventionally achieved by using a centralized control circuit to supply properly phased clock or synchronization pulses to the individual cells. Typical implementations include the use of a shift register or a counter and decoder to generate the shifted clock pulses [8].

The conventional approach is effective and simple for systems with a fixed number of cells. To be effective in a cellular converter architecture, however, an interleaving scheme should be able to accommodate a varying number of cells and maintain operation after some cells have failed. This is difficult to achieve via conventional (centralized) control methods, due to the circuit and interconnection complexity required to generate the proper number of pulses and direct them to the appropriate cells. Furthermore, any failure of the centralized control circuit will cause failure of the whole system, which is undesirable if high reliability is to be achieved. These limitations have led to the development of the distributed interleaving approach described here.

6.3.1 The Distributed Interleaving Approach

In the new distributed interleaving approach, the circuitry needed to attain interleaved operation is distributed among the cells, with only minimal connections among cells. The connections among cells are non critical, i.e., failure of the connection disrupts only the interleaving function, not the basic operation of the system. Unlike the conventional approach, each cell generates its own clock pulses, and only uses intercell information to determine exact frequency and phasing of the local clock. The approach automatically accommodates varying numbers of cells. If an individual cell is removed or fails, the remaining cells automatically interleave among themselves. Any failures affecting the information-sharing connections inhibit the interleaving, but do not cause the system to fail. These attributes lead to a flexible, reliable and robust interleaving system.

To achieve distributed interleaving, all of the cells are connected by an *interleaving bus*, typically consisting of a single wire (Fig. 6.3). Each cell has its own clock generator, and places information about

the frequency and phase of its local clock on the interleaving bus, generally in the form of signals related to the clock waveform itself. Using the aggregated information on the interleaving bus, each cell adjusts the frequency and phase of its own clock to achieve the desired interleaved effect.

6.3.2 A Practical Implementation Method

Consider the implementation of distributed interleaving shown in Fig. 6.3. Each cell contains its own clock generator. The clock generators are connected together by a single-wire interleaving bus, which is terminated in a known resistance, R_b, connected to ground. The structure of the clock generator circuit is illustrated in Fig. 6.4. Each clock generator contains a voltage-controlled oscillator (VCO) whose frequency (and phase) can be varied over a small range with a control voltage. The VCO generates both a sinusoidal and a square wave output voltage. The square wave output is used for the local clock. The sinusoidal output is run through a voltage-to-current converter, which drives a current proportional to the sinusoidal voltage onto the interleaving bus and through R_b. The voltage of the bus will thus be proportional to the vector sum of the sinusoidal VCO outputs of all the cells. Each clock generator senses this voltage and subtracts out its own contribution, leaving a signal which is the aggregate voltage of the other cells. A phase detector compares this signal to the output of the cell's local oscillator. A filtered version of the phase detector output is used for the control input to the VCO. This is done to drive the oscillator 180° out of phase with the aggregate output of the other cells. Each clock generator is thus designed to phase-lock out of phase with the aggregate output of the others.

When the cells are not operating in a locked condition, the voltage on the interleaving bus is the nonzero aggregate of all of the individual clock generator voltages, and the voltage at the input of each cell's phase detector is the aggregate voltage of the other cells. The output of the phase detector is a waveform whose average is either positive or negative depending on whether the aggregate voltage of

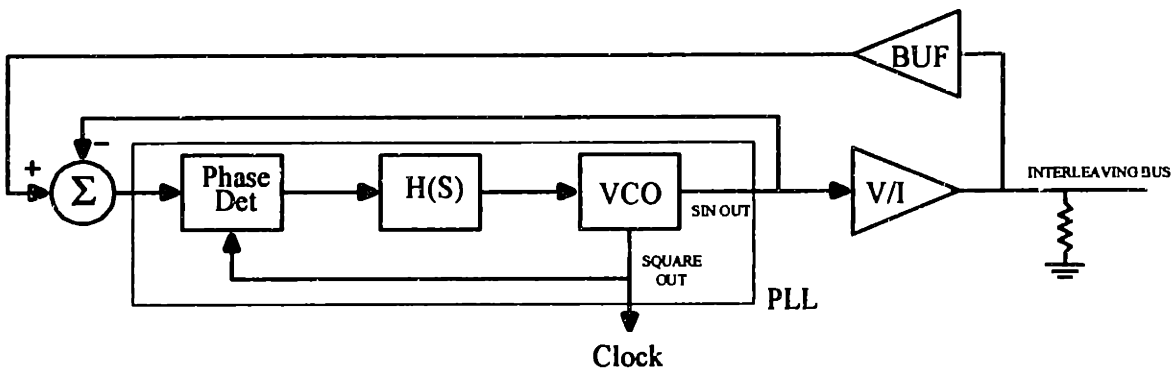


Figure 6.4 Structure of the clock generator for the example implementation.

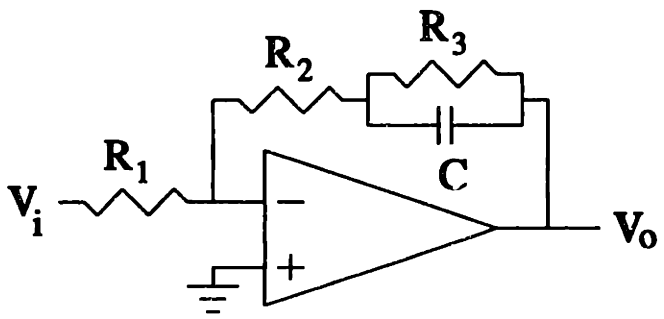


Figure 6.5 Loop filter structure for the prototype system. C = 0.22 μF, R_1 = 100 kΩ, R_2 = 10 kΩ, R_3 = 4.3 MΩ.

the other cells leads or lags the desired 180° position (relative to the local cell's voltage). When the converter cells are operating in a locked condition, the voltage on the interleaving bus is approximately zero, since the currents injected onto the bus are almost exactly out of phase; the average output voltage of each phase detector only deviates from zero enough to maintain the proper input voltage to its VCO.

When two clock generators are connected to the interleaving bus, they each phase-lock 180° out of phase with the other. When three clock generators are connected, they each phase-lock 180° out of phase with the vector sum of the other two, leading to a locked condition where each clock is 120° out of phase with the others. For situations where more than three clock generators are connected, there is more than one possible locking condition. However, they all involve sub-groups of cells interleaving among themselves.

6.3.3 System Design Issues

The design of a distributed interleaving system using phase-locking techniques requires careful attention to the system dynamics. The system dynamics are addressed in the context of the design of a three cell prototype system operating at approximately 50 kHz. First, consider the design of the phase-locked loop (PLL) within the clock generator circuit of Fig. 6.4. The PLL comprises a phase detector, a loop filter *H(s)*, and a voltage-controlled oscillator [45]. The phase detector generates an output voltage whose average is related to the phase difference between the input waveform and the local oscillator. The multiplier phase detector employed in the prototype system yields a nonlinear relationship which can be modeled as a linear gain (K_d = 4.8 V/rad) for small perturbations away from the locked condition. The voltage-controlled oscillator converts a step in input voltage to a step in output frequency (ramping phase), and hence can be modeled (in a linearized sense) as an integrator with a gain

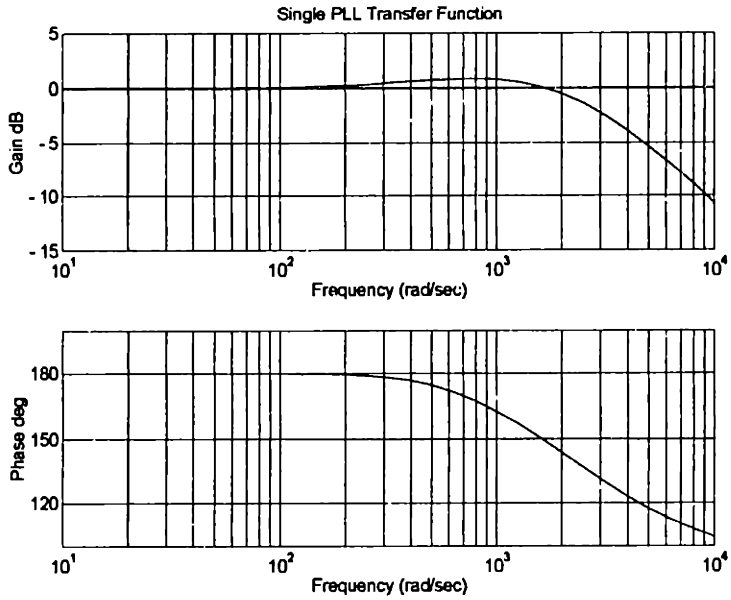


Figure 6.6 Input to output phase transfer function for the linearized model of a single prototype clock generator circuit.

($K_o = 6289$ rad/(V-s)). The loop filter $H(s)$ serves both to remove high-frequency components from the phase detector output and to compensate the closed-loop dynamics of the PLL. To limit the steady-state phase error of the system while allowing a limited degree of play in the phase alignment, an active loop filter of the type in Fig. 6.5 was selected. As described in [45], this type of loop filter yields a steady-state phase error of

$$\theta_v = \frac{\Delta\omega}{K_o K_d H(0)} \tag{6.11}$$

where $\Delta\omega$ is the maximum frequency deviation of the oscillator. For the parameters of the prototype system, this yields less than 1.4° of phase error for a 5 kHz frequency deviation, which was deemed acceptable. The resulting PLL design has the (linearized) input to output phase transfer function shown in Fig. 6.6. This design provided sufficient lock range and tracking range for the task. Note that the 90° phase shift associated with the multiplier phase detector along with an additional 90° phase shift in the VCO sine wave output was employed to achieve the 180° phase lock position desired for the interleaving system. The additional clock generator components are simple op-amp circuits whose dynamics can be neglected in the prototype system.

It must be recognized that the individual clock generators are themselves interconnected in a feedback configuration, yielding closed-loop system dynamics which are a function of the individual

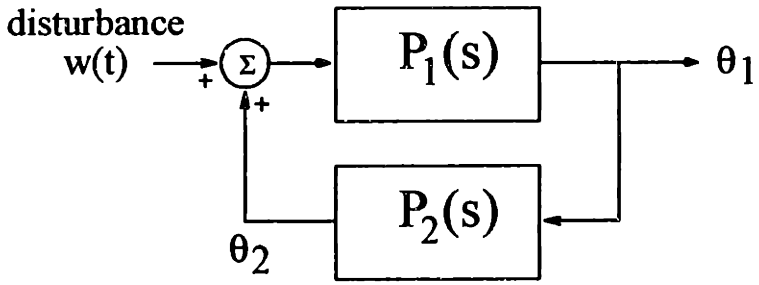


Figure 6.7 Feedback model for predicting the dynamics of a two-cell distributed interleaving system.

clock generator dynamics. We can find the closed loop dynamics of a two-cell clock generator system using the feedback model of Fig. 6.7, where we have denoted the (linearized) input to output phase transfer function of the k^{th} clock generator as $P_k(s)$. For the prototype system design, this approach yields closed-loop system poles at s = -5542, -496.3, -1.05, and 0 Np/s. The pole at the origin behaves as an integrator, and may at first seem to indicate only marginal stability of the system. However, in reality, this pole merely indicates that a step input phase disturbance can cause the system to settle at a different frequency (e.g., with ramping output phase in the linearized model). Thus, the fact that the desired phase lock condition can occur over a range of frequencies yields the pole at the origin in the linearized model. The limited adjustment range of the VCOs prevents this fact from causing problems. If a disturbance brings one of the clock generators to the edge of its adjustment range, the other clock generator will lock out of phase with it at that frequency with the dynamics of a *single* clock generator. A similar feedback configuration analysis can be made for the three-cell case. This also yields a mixture of stable high- and low-frequency poles and a pole at the origin.

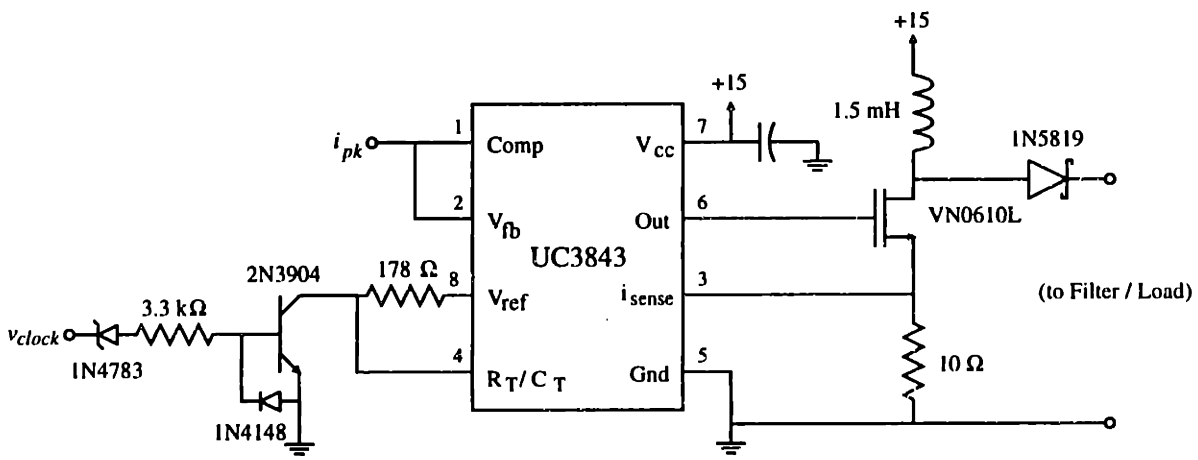


Figure 6.8 Schematic of the prototype boost converter cell power stage.

6.4 Experimental Results

To validate the proposed distributed interleaving implementation, and to allow ripple comparisons to be made among different clocking schemes, a 3-cell low-power boost converter system operating at approximately 50 kHz has been constructed. As illustrated in Fig. 6.8, each cell employs a conventional UC3843 current-mode control chip with its on-chip oscillator overridden by the local clock generator circuit. The converter cells have a boost inductance of 1.5 mH, and operate in discontinuous mode under peak current control. The boost converter system operates from an input voltage of 15 V, and has an output filter capacitance of 0.22 μF. Experimental results presented in this chapter are for operation with a load resistance of 390 Ω and a peak cell turn-off current of approximately 55 mA, yielding an output voltage of approximately 25 V. As illustrated in Fig. 6.9, the clock generators themselves were constructed with available discrete components: an AD633 differential multiplier was used as a

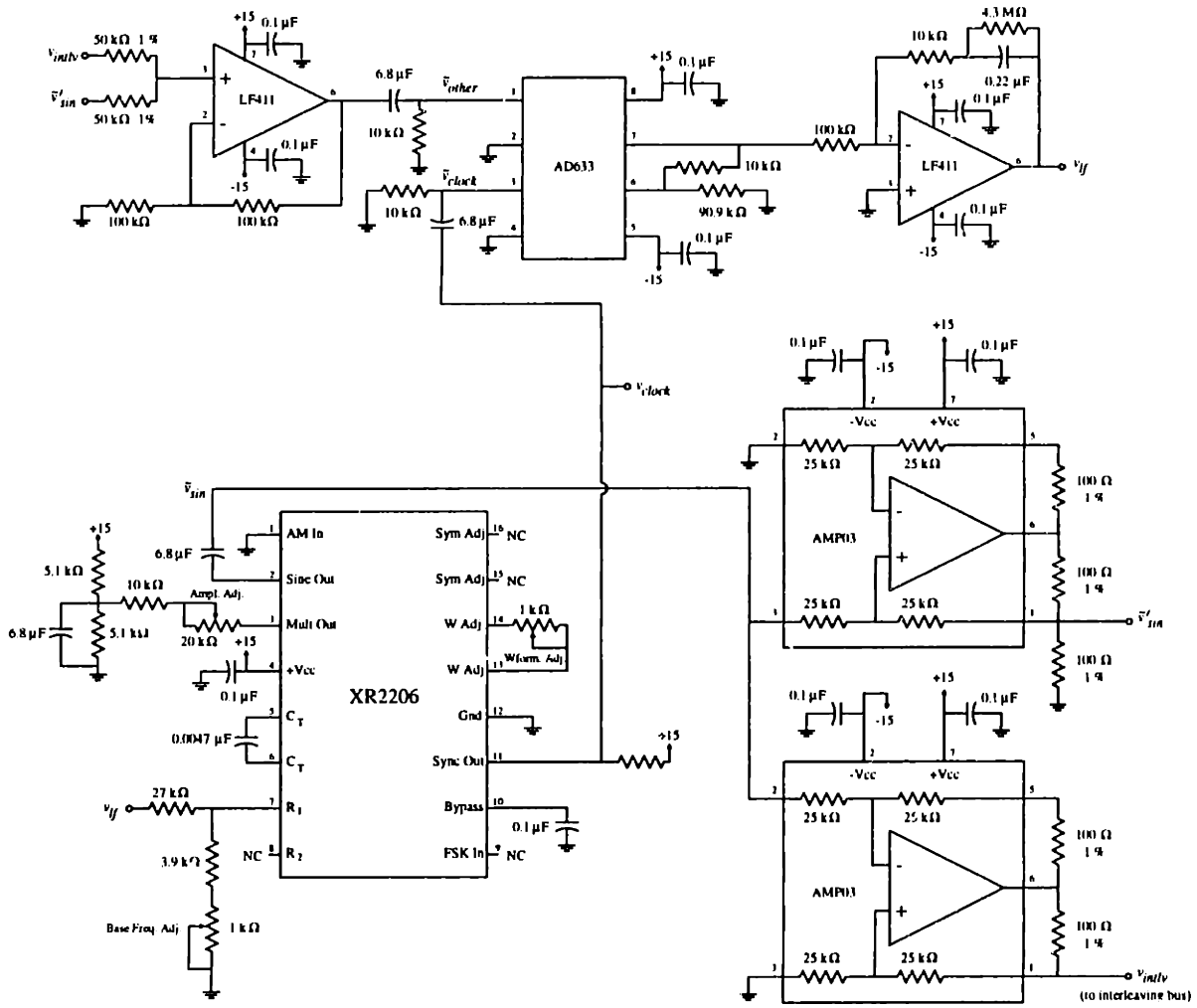


Figure 6.9 Schematic of the prototype clock generator circuit.

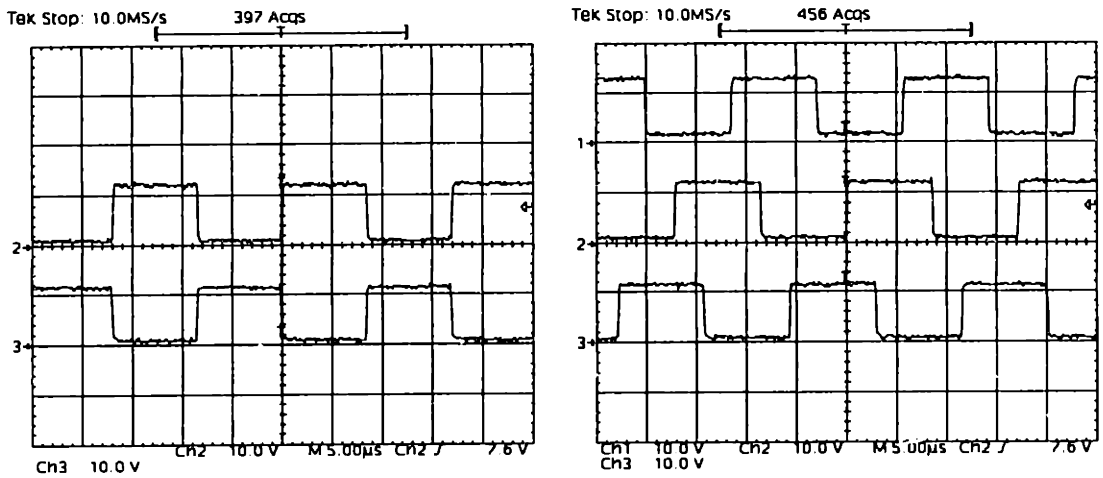


Figure 6.10 Experimental clock waveforms for the prototype distributed interleaving system with two and three cells.

phasedetector, while an XR2206 monolithic

function generator was used as the VCO. The remaining components were simple operational amplifier circuits. It should be pointed out that this design was optimized for experimental convenience, and clock generators of this type can be constructed with far fewer integrated circuits. For example, the implementation used in the cellular converter system described in Chapter 8 requires only 3 ICs.

Figure 6.10 shows the clock waveforms from the prototype system with 2 and 3 converter cells connected to the interleaving bus. Phase locking was found to be very stable with acceptable locking and tracking characteristics for both the two and three cell case. The correct phasing of the clock waveforms to within design specifications (1.5°) is obtained under all conditions. On start up, the clock generators achieve lock within a few seconds, typically settling at the top end of the adjustment range (approximately 57 kHz). This result is consistent with the dynamic model of the previous section. The response speed is far more rapid for small perturbations such as the removal of a cell.

To verify the ripple cancellation benefits of the approach, and to corroborate the analysis of Section 6.2, the input current and output voltage ripple were measured with synchronous clocking, independent clocking, and (distributed) interleaved clocking of the three cells. Rms ripple, phase, and frequency measurements were made using the numerical computation functions of a TDS 420 Oscilloscope. As shown in Fig. 6.11(a), synchronized clocking of the cells leads

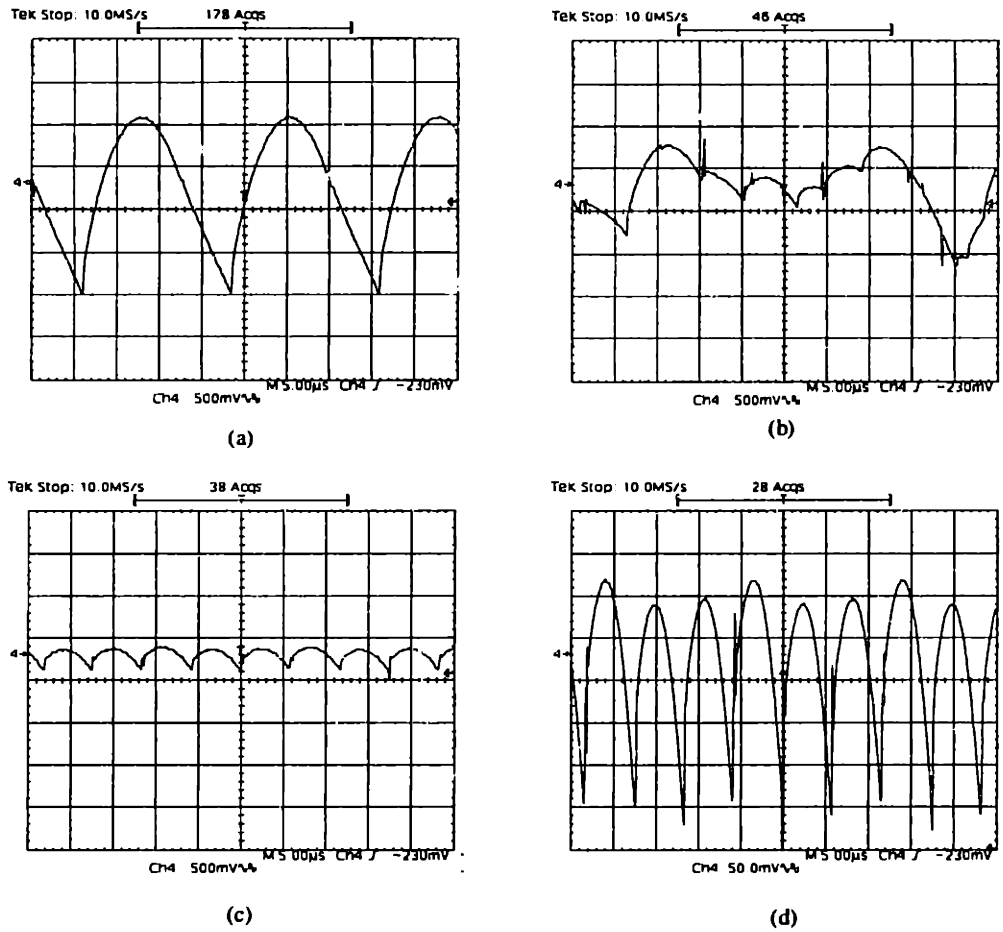


Figure 6.11 Output voltage ripple waveforms for the prototype system. (a) Synchronized clocking. (b) Independent clocking (stochastic ripple cancellation). (c) Interleaved clocing. (d) Interleaved clocking @ 50 mV/div.

to an output voltage ripple of approximately 2.1 $V_{p\text{-}p}$, and 0.653 V_{rms}. As shown in Fig. 6.11(b), independent clocking of the cells (yielding stochastic ripple cancellation) leads to a time-varying output voltage ripple, with the rms ripple reduced down to 0.35 ± 0.03 V_{rms}. This amount of ripple reduction is consistent with the analysis of Section 6.2 for independent clocking (which predicts 0.38 V_{rms}), and corroborates the results presented there. Operation under distributed interleaving, as shown in Fig. 6.11(c) and (d), yields a ripple of 0.3 $V_{p\text{-}p}$ and 0.072 V_{rms}, with the first major ripple component at three times the individual clocking frequency. This represents a factor of 7 reduction in peak-to-peak ripple over synchronized clocking. Ideally, a factor of at least 9 reduction should be obtained: a factor of three from the current ripple cancellation, and a factor of three from the frequency increase across the capacitive output filter [7-10]. The reason for this discrepancy is shown in Fig. 6.11(d), where it is seen

that the cancellation of the fundamental ripple frequency is not perfect due to second order effects such as phasing error, differences in the boost inductors and sense resistors, etc. Nevertheless, use of the prototype distributed interleaving circuitry yields a tremendous performance improvement over both synchronized and independent clocking of the converter system.

Measurements of the input current ripple of the prototype system also demonstrated the benefits of the approach. Figure 6.12(a) shows the net input current drawn by the prototype system with the cells clocked synchronously, while Fig. 6.12(b) shows the input current under independent clocking. As with the output voltage ripple, independent clocking leads to a time-varying ripple waveform with a reduced rms value compared to the synchronously clocked case. Figure 6.12(c) shows the input current with distributed interleaving, while Fig. 6.12(d) shows the ripple component of the input current at a higher magnification. As can be seen in Figures 6.12(c) and (d), operation under distributed interleaving yields a tremendous factor of 22 reduction in peak-to-peak input current ripple compared to the synchronously clocked case. This is much greater than the minimum reduction of a factor of 3 guaranteed across the whole operating range of the converter system, and is due to the fact that the operating point in the example is at a current level where the input current ripple cancellation is nearly perfect. Other operating points yield a much smaller reduction in ripple. Cancellation of the output current ripple, and hence the output voltage ripple, is not as good at this operating point because of the difference in waveform shape between the input and output currents. (Numerical and analytical analyses of the variation in ripple cancellation versus waveform shape and operating point can be found in [7-10].) What may be concluded from these results is that the distributed interleaving approach is practical, and offers large performance benefits without the need for centralized control.

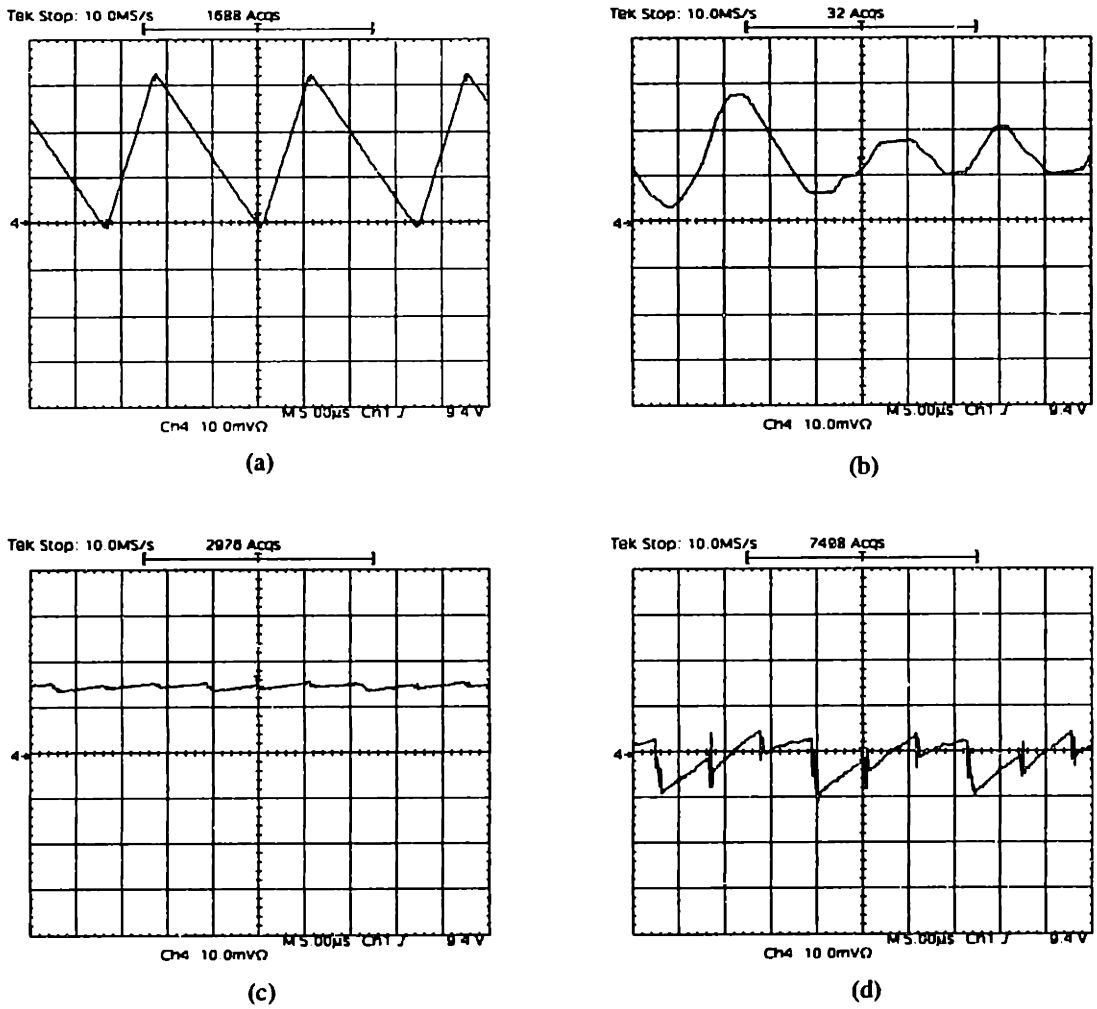


Figure 6.12 Input current waveforms for the prototype system. (a) Synchronized clocking at 50 mA/div. (b) Independent clocking (stochastic ripple cancellation) at 50 mA/div. (c) Interleaved clocking at 50 mA/div. (d) Interleaved clocking at 5 mA/div, ac coupled.

6.5 Other Approaches

The distributed interleaving implementation described in this chapter generates $2\pi/N$ interleaving for up to 3 cells, above which the locking conditions are as yet unknown. While this may at first seem very restrictive, it should be pointed out that the benefits of interleaving cease to accrue beyond a very limited number of cells due to mismatches among cells [8]. This effect was seen in the prototype system, and is especially true for systems employing distributed current-sharing techniques (where small current mismatches inevitably exist), and in systems operating at high frequencies (where small time delays correspond to large phase mismatches). For systems with large N, groups of three cells can be

interleaved, with stochastic ripple cancellation occurring among the interleaved groups. Nevertheless, in some cases it may be desirable to generate $2\pi/N$ interleaved clock waveforms for higher numbers of cells. This is achievable through means similar to those described here, but at the expense of increased complexity in the clock generator circuit structure and/or the interconnection structure.

6.6 Conclusion

This chapter has investigated passive and active ripple cancellation techniques which are well suited to a cellular architecture. The degree of passive ripple cancellation expected among the cells of a parallel converter system has been analytically quantified for the case of independently clocked cells, and compared to experimental results. It has been shown that the rms ripple current of an N-cell parallel converter system with independent clocking is a factor of $N^{1/2}$ lower than for the case where the clocks are synchronized.

The chapter has also introduced a distributed approach to interleaving converter cells in which the circuitry required to attain interleaving is distributed among the cells. Unlike conventional methods, the new approach requires no centralized control, automatically accommodates varying numbers of cells, and is highly tolerant of subsystem failures. A general methodology for achieving distributed interleaving has been proposed, along with a specific implementation approach and its experimental verification. Performance of the prototype system under synchronized clocking, independent clocking and interleaved clocking has been measured and compared to analytical predictions. The experimental results corroborate the analytical predictions and demonstrate the tremendous benefits of the distributed interleaving approach.

Chapter 7

Design Considerations for Cellular Converters with Applications to a Cellular Inverter System

7.1 Introduction

Realizing the benefits of a cellular architecture requires suitable converter topologies and control techniques. This chapter discusses some key considerations in the design of cellular converter systems, including the impact of replicated and added components and the need for instantaneous current-sharing among cells. The chapter also presents a new cellular inverter implementation which addresses these design issues. We show that this architecture mitigates some of the major drawbacks of the single resonant pole inverter (RPI), on which it is based. Furthermore, we present an enhanced control algorithm which significantly reduces converter stresses and losses for many operating conditions and is applicable to both the RPI and the parallel architecture.

7.2 Design Considerations for Cellular Converters

When evaluating a potential cellular converter design, it is instructive to compare the cellular converter to an equivalent single converter in order to establish the benefits and limitations of the cellular approach. We use this comparison here to identify some basic issues that should be addressed when designing a cellular converter system.

7.2.1 Distributed Components vs. Replicated and Added Components

From a topological perspective, one could consider a cellular converter to be composed of the elements of a single large converter which have each been broken up into N sub-elements and distributed among the cells. Each cell receives $1/N$ of the single converter's silicon die area and capacitance (at the same voltage rating) and N times the single converter's inductance and resistance (at $1/N$ of the current rating). A cellular converter constructed this way would have the same total magnetic and capacitive energy storage, the same total silicon device area and switch stress factor, and (to first order) incur the

same losses as its single converter equivalent.

Nevertheless, some components of a cellular architecture cannot be considered as subdivided elements of a single large converter. These components, including many of the sensing and control elements, must be *replicated* for each of the cells instead of being broken down from a large element and distributed. For example, while a single large converter might require a single PWM controller, an N-cell converter system would require N identical PWM controllers. Furthermore, other components in a cellular converter do not correspond to any elements in a single converter, and must be considered as *added* components. Such components include, for example, the circuitry for controlling current sharing, which is not needed in a single converter.

The differences between distributed components and replicated or added components become important when evaluating the cost impact of a cellular implementation. We will assume that, to first order, the cost of the distributed components in a cellular converter is the same as that of the equivalent components in a single converter, since the silicon VA rating, magnetic energy storage, and capacitive energy storage are the same in both cases. While many effects, including packaging costs, production volumes, etc., can limit the validity of this assumption, it is reasonable for a first-pass analysis. Based on this assumption, it is clear that added and replicated components in a cellular converter system lead to additional costs. As a result, reducing the cost impact of added and replicated components is a key design goal for constructing a competitive cellular converter. This implies, for example, that converter topologies with very simple control and sensing requirements tend to be more favorable for use in a cellular architecture. Furthermore, this result favors maximizing the individual cell ratings within a given manufacturing framework, and tends to place a lower bound on useful cell ratings, since replicated and added component costs tend to be a larger fraction of the total cost as the cell power level decreases.

It should be pointed out that while these results have significant implications for the design of cellular converters they do not reflect the entire tradeoff between the single-converter and cellular design approaches. For example, the ability to achieve a large degree of ripple cancellation among cells of a cellular architecture (as described in Chapter 6) can be used to reduce the energy storage and filtration requirements of a cellular converter as compared to a single converter with the same input and output waveform ripple. Similarly, the reduction in individual component sizes in a cellular architecture can sometimes allow the use of higher frequency design techniques and improved manufacturing processes, and the distribution of heat generation in a cellular architecture may ease the thermal management requirements. All of these factors can lead to advantages for the cellular design approach in terms of cost.

7.2.2 Current Sharing

Constructing a large converter by paralleling smaller converter cells requires that a current sharing mechanism be implemented to prevent the destructive overload of individual cells and to equalize the stress among cells (an important consideration for high reliability). Current sharing can be achieved by using an appropriate control scheme in conjunction with a magnetic structure which absorbs the instantaneous voltage differences between cells. Stated another way, the individual cells should be made to behave as current sources for times on the order of the switching period.

In many power conversion applications, including dc-dc conversion, the existing magnetic components required for performing the conversion function can be used for current sharing. In other applications, including some ac-dc and dc-ac conversion tasks, no pre-existing components are available, and additional magnetic components must be *added* for a cellular design. The interphase transformer (IPT) is the standard magnetic structure for paralleling two converters [48-50], and can be extended to more converter cells using many legged IPTs [51,52] or whiffletree connections of IPTs [52,53]. However, these designs are inappropriate for paralleling large numbers of cells because they are difficult to manufacture and the cells cannot be made autonomous (an important condition for increased system reliability). Another approach is to place an inductor at the output of each bridge leg [3,16,30]. This structure results in a converter system which is modular and more manufacturable. However, the size of the output inductor is an important design parameter, since it can represent an appreciable fraction of converter size and cost. Minimization of the energy storage requirement of the output inductor is thus a key design goal for a practical cellular architecture.

As an example, consider the single-phase half-bridge converter of Fig. 7.1 operating under hysteretic current control. The converter is loaded by a voltage source v_o, which, for times on the order of the switching period, represents the output filter, the load, and other paralleled cells. Given a maximum switching frequency f_{sw}, a reference current i_{ref}, and a specified hysteresis band Δi_{band}, the energy storage requirement of the inductor is:

$$W_l = \frac{i_{ref} V_{dc}}{16 f_{sw}} \frac{(1+k)^2}{k} \tag{7.1}$$

where $k = \Delta i_{band}/i_{ref}$. Figure 7.2 shows a plot of (7.1) as a function of k, and shows that the minimum point of this curve is at $k = 1$, with only minor costs in increased energy storage for values over 1. Operation with a ripple ratio approaching or exceeding 1 results in the smallest energy storage

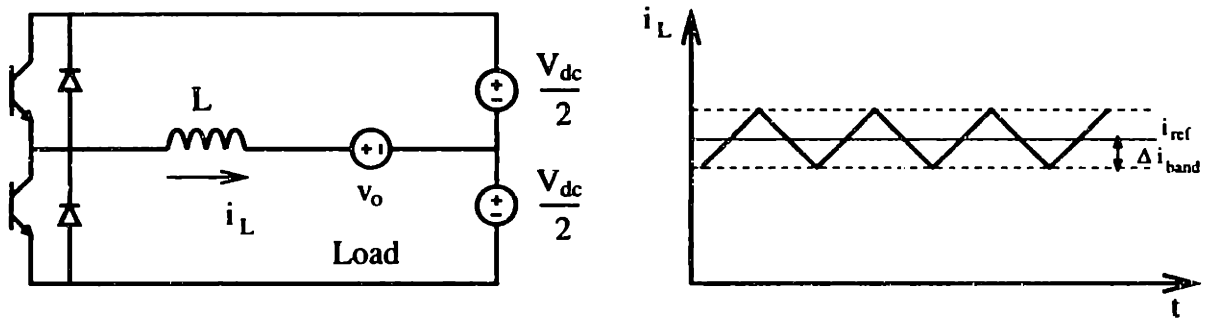


Figure 7.1 A half-bridge current-controlled inverter and its output current waveform.

requirement on the output inductor.

Operation with high ripple and low magnetic energy storage is typically more advantageous in a cellular converter system than in a single large converter. In a single large converter, high ripple currents lead to difficulties in filtering the input and output waveforms. For this reason, in converters which require them, the magnetic elements are typically sized for small ripple waveforms, despite the increase in energy stored. In a cellular architecture, however, ripple cancellation among cells can often be used to reduce the input and output ripple to acceptable levels while minimizing the magnetic energy storage.

In addition to minimizing the magnetic energy storage required for current sharing, operation with a large ripple ratio can be used to obtain soft switching of the devices. Soft-switched operation is

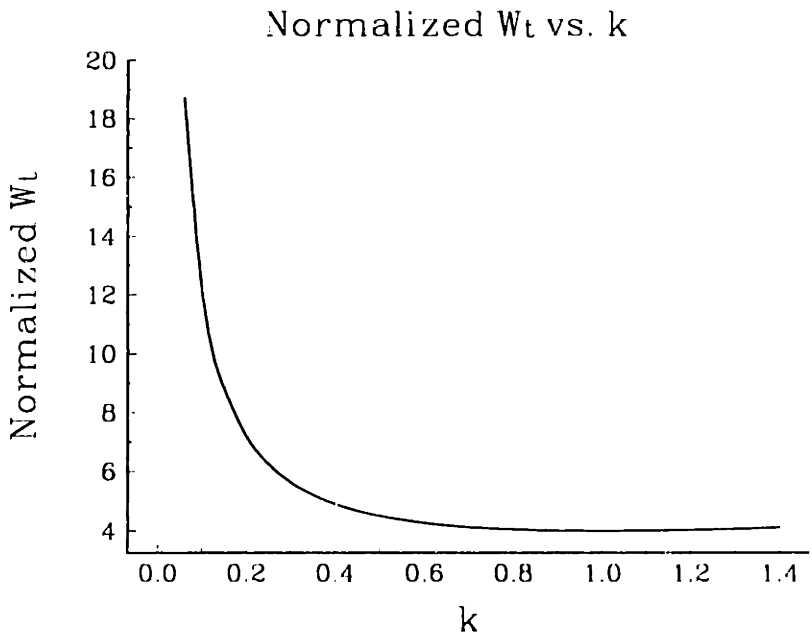


Figure 7.2 Output inductor energy storage requirement as a function of ripple ratio, k.

desirable because the reduction of switching losses allows an increase in the switching frequency and a commensurate reduction in component size. The next section introduces one example in which converter operation with a large ripple ratio is used to achieve soft switching.

7.3 The Resonant Pole Inverter

The Resonant Pole Inverter (RPI) is a hysteresis-controlled converter which maintains zero-voltage switching by operating with a ripple ratio k slightly greater than 1. This section introduces the resonant pole inverter, and describes both conventional and enhanced control techniques for it. The RPI converter topology is shown in Fig. 7.3 [54-61]. The operation of this converter is illustrated in Fig. 7.4 and proceeds as follows. Assume operation begins with S_1 conducting (Mode 1). If the filter capacitor is large enough to clamp the output voltage over the cycle, the inductor current will build up linearly until it reaches a current i_{p+} determined by the controller. At this point the controller turns S_1 off, and the inductor rings with the two resonant capacitors C_{r1}, C_{r2} (Mode 2) until D_2 turns on (Mode 3). S_2 is then turned on while D_2 conducts. During this time, the current in the inductor linearly decreases and reverses direction (Mode 4). When the current in the inductor reaches a level i_{p-}, the controller turns S_2 off, and the inductor rings with the resonant capacitors (Mode 5) until D_1 conducts (Mode 6). S_1 can then be turned on, and the cycle repeats. Note that all switch transitions occur at zero switch voltage.

As with standard hysteresis-based PWM, the switching frequency varies dynamically. If the length of the resonant transitions are small and do not affect the inductor current heavily, the instantaneous switching period can be approximated as

$$T \approx \frac{V_{dc} L_r (i_{p+} + |i_{p-}|)}{\frac{1}{4} V_{dc}^2 - V_{cf}^2} \tag{7.2}$$

The values of i_{p+} and i_{p-} used by the controller are constrained by the necessity of having enough energy

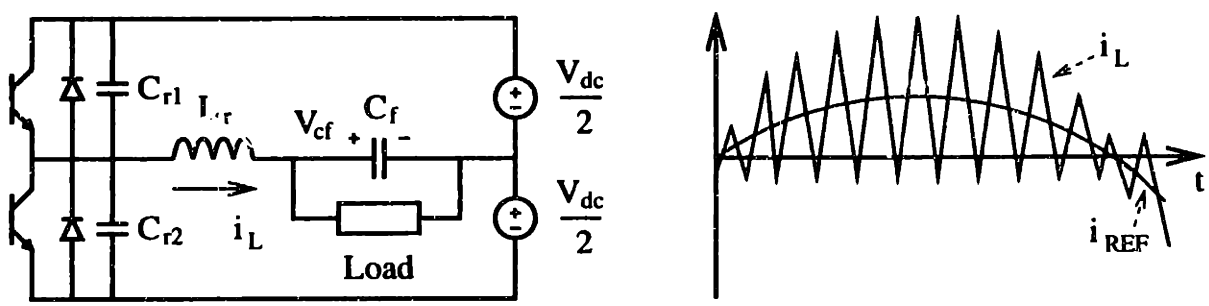


Figure 7.3 The resonant pole inverter and its output current waveform.

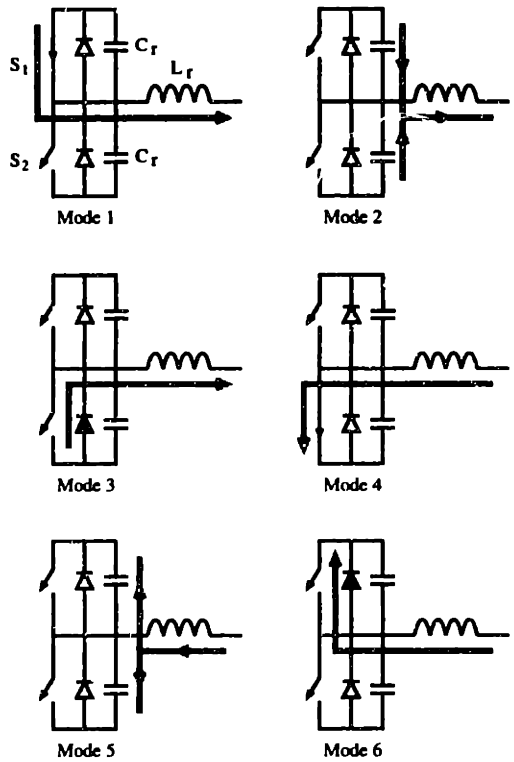


Figure 7.4 An operational cycle of the resonant pole inverter.

in the inductor to ring the resonant capacitor voltages between zero and V_{dc} to obtain zero-voltage switching. That is, when a device turns off, there must be sufficient current in the inductor to drive the bridge-leg center point voltage to the opposite rail and allow the opposing device to turn on at zero voltage. Assuming ideal components, a minimum inductor current i_{min} is needed at the end of Mode 1 if $V_{cf} > 0$, where we define

$$i_{\min}(V_{cf}) = 2\sqrt{\frac{C_r V_{dc} |V_{cf}|}{L_r}} \,. \tag{7.3}$$

No current is required for $V_{cf} \leq 0$. Similarly, the magnitude of i_{p-} must exceed i_{min} at the end of Mode 4 if $V_{cf} < 0$, and may be zero for $V_{cf} \geq 0$.

7.3.1 Conventional RPI Control

The desired local average output current i_{ref} is generated by controlling the values of i_{p+} and i_{p-}. If the time spent in the resonant transitions is small and does not severely affect the inductor current, the output current waveform can be treated as triangular, yielding an approximate local average output

current of $(i_{p+} + i_{p-})/2$. The conventional control method for generating a desired i_{ref} is shown in Table 7.1 (a). This method ensures that the inductor current is high enough at each transition by adding a margin i_m to the magnitude of both i_{p+} and i_{p-}, where i_m is a current sufficiently greater than i_{min} to ensure reliable operation.

7.3.2 Enhanced RPI Control

While the conventional control approach is simple and always ensures that the resonant inductor current constraints are met, it yields currents which are significantly higher than needed to ensure zero-voltage switching for many operating conditions. This is because the conventional control method always ensures that the magnitudes of i_{p+} and i_{p-} exceed i_{min}, even though this is not necessary for all values of V_{cf}.

Here we introduce a new control method, shown in Table 7.1 (b), which reduces peak currents, losses, and output voltage ripple for many operating conditions, and yields identical performance for all others. The new control method takes advantage of the fact that for a given output voltage polarity, there is a minimum inductor current requirement for only one of the two resonant transitions. When $V_{cf} > 0$, there is only a minimum required value for i_{p+}, and when $V_{cf} < 0$ there is only a minimum value for the magnitude of i_{p-}. Thus, when sourcing power from the converter (quadrants 1,3), only any difference between the peak current needed to source i_{REF} alone and that required for the resonant transition must be added. In quadrants 2 and 4, we are left with the conventional control method. The control method shown in Table 7.1 (b) achieves this, and is simple to implement in analog hardware.

To illustrate the benefits of this enhanced control technique, we consider the simulation results

i_{ref}	< 0	> 0
	$i_{p+} = i_z$ $i_{p-} = 2i_{ref} - i_z$ $i_z = i_m$	$i_{p+} = 2i_{ref} + i_z$ $i_{p-} = -i_z$ $i_z = i_m$

(a) Conventional RPI control

i_{ref} / V_{cf}	< 0	> 0
> 0	$i_{p+} = i_z$ $i_{p-} = 2i_{ref} - i_z$ $i_z = i_m$	$i_{p+} = 2i_{ref} + i_z$ $i_{p-} = -i_z$ $i_z = \max(i_m - 2i_{ref}, 0)$
< 0	$i_{p+} = i_z$ $i_{p-} = 2i_{ref} - i_z$ $i_z = \max(i_m + 2i_{ref}, 0)$	$i_{p+} = 2i_{ref} + i_z$ $i_{p-} = -i_z$ $i_z = i_m$

(b) Enhanced RPI control

Table 7.1 RPI control tables. (a) Conventional control. (b) Enhanced control.

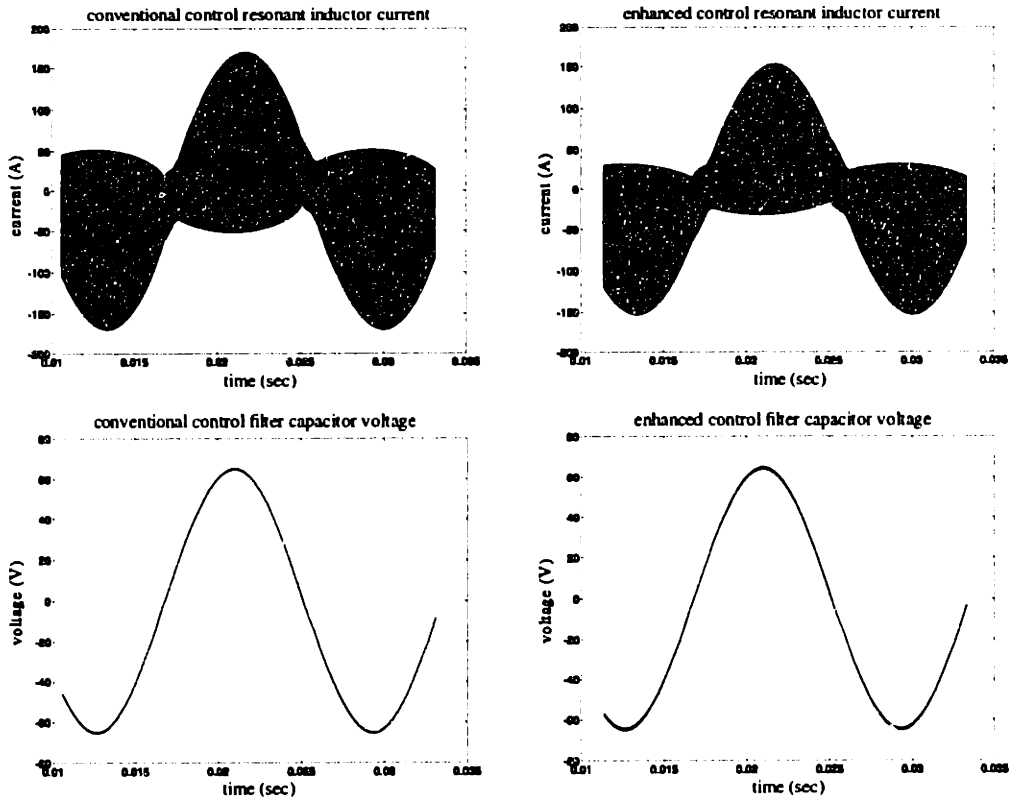


Figure 7.5 Comparison of RPI Control Methods. RPI has L_r = 15 μH, C_r = 0.16 μF, C_f = 150 μF, L_l = 1 mH, R_l = 1 Ω, and V_{dc} = 300 V.

shown in Fig. 7.5. The half bridge converter in this example is used to drive an RL load at 65 V and 60 Hz. For both control methods, the system has an outer PI voltage control loop yielding a sinusoidal output voltage, and uses a value of $i_m = i_{min}(V_{cf})$ with an additional constant safety margin for peak current calculations. The resonant inductor current is significantly reduced for the enhanced method, as are the device and filter capacitor currents. For the example shown, the rms current of the filter capacitor was reduced by over 15% compared to the conventional method. This benefit of the enhanced control algorithm is especially significant for converters which operate at partial load, since it improves partial-load efficiency by reducing the fixed losses associated with maintaining zero-voltage switching.

One minor disadvantage of the enhanced control method is that the approximate relationship among i_{ref}, i_{p+}, and i_{p-} is less accurate for the enhanced method than for the conventional method. Because the currents are lower for the enhanced method, more time is spent in the resonant transitions, and the overall waveform shape is affected more by the transitions. However, these effects are easily compensated for by using feedback, and do not pose a significant problem, as can be seen by the resulting waveform quality in Fig. 7.5.

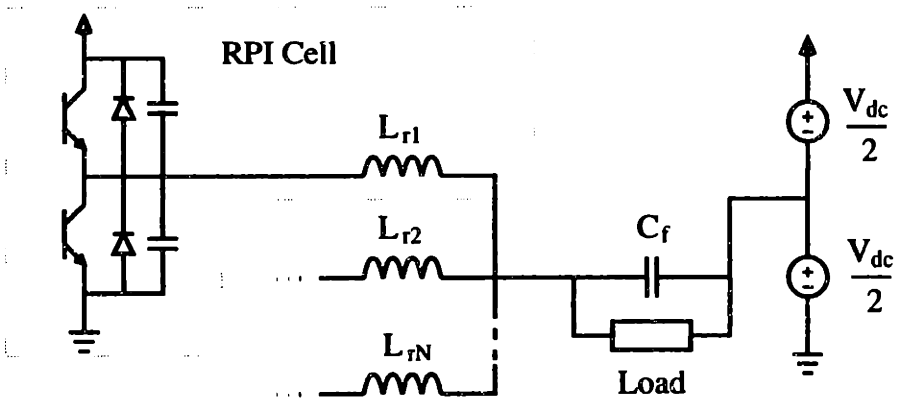


Figure 7.6 The parallel resonant pole inverter architecture (PRPI).

7.4 The Parallel Resonant Pole Inverter

An important contribution of this chapter is the development of the *parallel* resonant pole inverter (PRPI) architecture, which is based on the RPI cell structure as shown in Fig. 7.6. For simplicity, the single-phase half-bridge will be discussed here. Constructing a parallel system using RPI cells meets the objective of minimizing the size of the magnetic structure needed for current sharing, since the RPI cells operate near the minimum energy storage point of (7.1). Furthermore, because this converter is fully soft-switched, it can operate at higher frequencies than a comparable hard-switched converter for the same total losses. This increase in switching frequency further reduces the size of the required magnetic components, according to (7.1). These advantages are achieved with a minimum of added components and a simple control system. We will also show that the parallel resonant pole inverter overcomes some of the major disadvantages of the single RPI circuit.

7.4.1 Piecewise Modeling of the PRPI

This section presents a piecewise model for simulating the general N-converter parallel resonant pole inverter (PRPI) system of Fig. 7.6. The model assumes ideal switches and components, and an R-L-E load. We give state equations for the resonant inductor current and (bottom) capacitor voltage of the k^{th} converter cell in each mode, along with the boundary conditions for transition to the next mode. State equations valid under all conditions are presented for the filter capacitor voltage and load current. The resonant inductor current and bottom resonant capacitor voltage of the k^{th} converter cell are denoted as i_{Lk} and v_{Ck}, respectively.

The state equations for the filter capacitor voltage, v_{cf}, and load current, i_l, are

$$\frac{dv_{cf}}{dt} = \frac{(\sum_{k=1}^{N} i_{L,k}) - i_l}{C_f} \tag{7.4}$$

$$\frac{di_l}{dt} = \frac{v_{cf} - i_l R - E}{L_l} . \tag{7.5}$$

The equations for the k^{th} converter in Mode 1 or 6 (S_1/D_1 on, S_2/D_2 off) are

$$\frac{di_{L,k}}{dt} = \frac{\frac{1}{2}V_{dc} - v_{cf}}{L_{r,k}} \tag{7.6}$$

$$\frac{dv_{C,k}}{dt} = 0. \tag{7.7}$$

This mode is valid until the inductor current reaches the specified value (i_{p+}) and S_1 is turned off.

For the k^{th} converter in Mode 2 (S_1/D_1 off, S_2/D_2 off, top to bottom transition):

$$\frac{dv_{C,k}}{dt} = -\frac{i_{L,k}}{2C_{r,k}} \tag{7.8}$$

$$\frac{di_{L,k}}{dt} = \frac{v_{C,k} - \frac{1}{2}V_{dc} - v_{cf}}{L_{r,k}} . \tag{7.9}$$

This mode is valid while $v_{C,k} > 0$.

For the k^{th} converter in Mode 3 or 4 (S_1/D_1 off, S_2/D_2 on):

$$\frac{di_{L,k}}{dt} = \frac{-\frac{1}{2}V_{dc} - v_{cf}}{L_{r,k}} \tag{7.10}$$

$$\frac{dv_{C,k}}{dt} = 0. \tag{7.11}$$

This mode is valid until the inductor current reaches the specified value and S_2 is turned off.

For the k^{th} converter in Mode 5 (S_1/D_1 off, S_2/D_2 off, bottom to top transition):

$$\frac{dv_{C,k}}{dt} = -\frac{i_{L,k}}{2C_{r,k}} \tag{7.12}$$

$$\frac{di_{L,k}}{dt} = \frac{v_{C,k} - \frac{1}{2}V_{dc} - v_{cf}}{L_{r,k}}. \tag{7.13}$$

This mode is valid while $v_{C,k} < V_{dc}$.

The relevant state equations are solved at each time step, changing the modes of the individual converters as necessary. Piecewise simulations of this nature are used in Section 7.4.3 to model the ripple current cancellation in a PRPI.

7.4.2 Advantages of the PRPI

In addition to its other attributes, the PRPI eliminates two of the major drawbacks of the conventional RPI. As discussed in [56], the practical size of an RPI is limited by the difficulty of constructing output inductors of large enough rating. However, one can construct an N cell PRPI which is functionally equivalent to a single RPI of N times the cell VA rating, increasing the converter size by

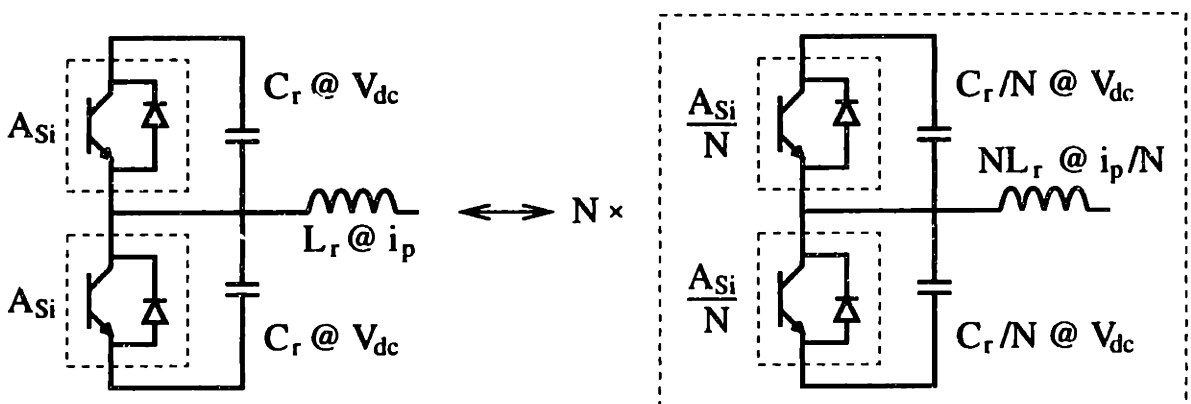


Figure 7.7 A resonant pole inverter leg and its equivalent parallel resonant pole components.

a factor of N over that achievable using a single RPI within the same manufacturing framework. To see this, consider breaking down a single RPI into N cells as shown in Fig. 7.7. Each of these converter cells will, to first order, operate at the same frequency as the original, and have $1/N$ times the losses. Thus, creating the same VA rating with equivalent parallel cells distributes the inductance in a manner which makes it far more manufacturable than a single large converter. This benefit is in addition to the fact that in practice, the smaller converters can be designed to operate at higher frequencies than a single large converter, due to reduction of parasitics and the distribution of heat generation.

Another major difficulty with resonant pole inverters is the high current ratings of the output filter capacitors [57]. Ripple cancellation among the individual converters of a PRPI significantly reduces the rms current stress on the filter capacitors, even when the cells are controlled autonomously (without active ripple cancellation). This is important, since the output filter capacitor can represent an appreciable cost component in an RPI system. We compare the relative performances of a single RPI and a 10 cell PRPI, both operating under the enhanced control method described previously, as shown in Fig. 7.8. The simulation results, obtained using the piecewise model of Section 7.4.1, show that the rms current stress on the PRPI filter capacitor is over 70% less than that in the equivalent single RPI, and the voltage ripple is lower as well. This reduction is entirely due to ripple cancellation among the outputs of the cells, and is likely to be useful for diminishing acoustic noise and EMI. As shown analytically in the next section, an N-cell PRPI will have a factor of $N^{1/2}$ less output rms current ripple than an equivalent single RPI, leading to a lower rms current rating for the output filter capacitor.

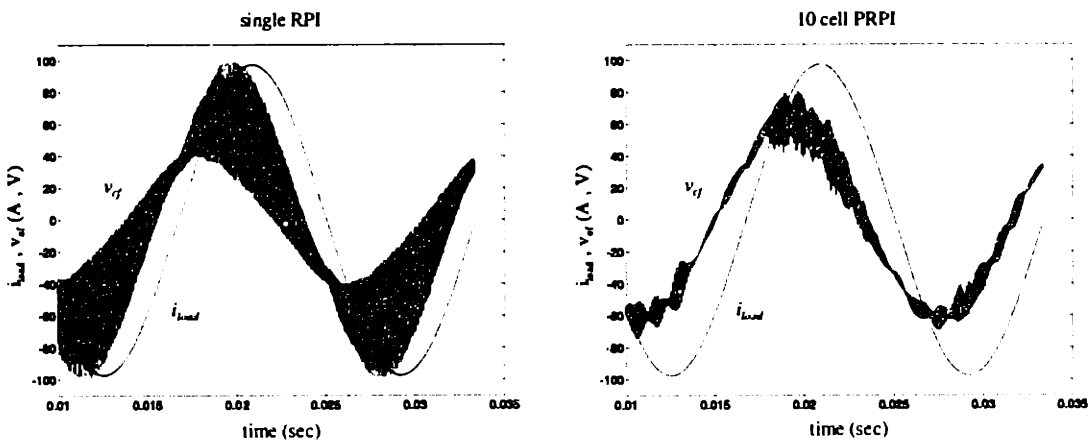


Figure 7.8 Comparison of output voltage and current for a single RPI and an equivalent ten cell PRPI system. Single RPI has $L_r = 25\ \mu$H, $C_r = 0.16\ \mu$F, $C_f = 50\ \mu$F, $L_{load} = 1$ mH, $R_{load} = 1\Omega$.

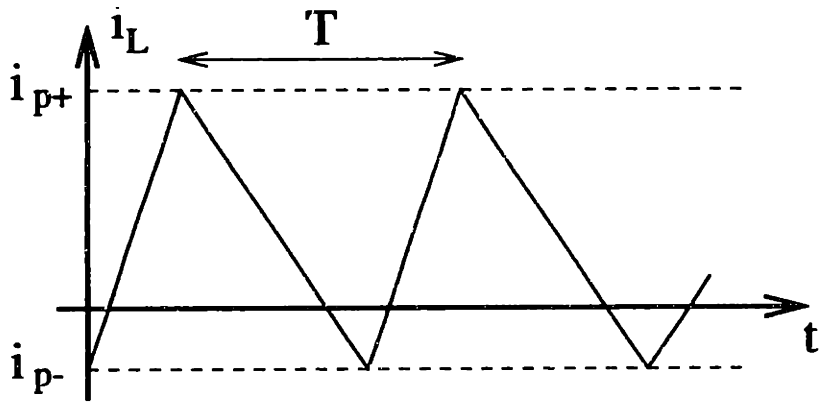


Figure 7.9 The RPI inductor current waveform at a fixed operating point.

7.4.3 Analysis of Passive Ripple Cancellation in the PRPI

A significant contribution of this chapter is the quantification of the amount of passive, or *stochastic*, ripple cancellation which occurs among cells in a PRPI. We will show that if a single large RPI is replaced by an equivalent N-cell PRPI, a $N^{1/2}$ reduction in rms output ripple current is expected under open-loop conditions when the cells are controlled autonomously (without active ripple cancellation). This derivation follows the approach developed in Chapter 6 for paralleled fixed-frequency PWM converters.

Consider a single RPI with parameters L_r, C_r operating at a fixed output voltage v_{cf} and commanded current i_{ref}. The inductor current waveform of Fig. 7.9 is periodic with a period T determined by (7.2) and has peak currents

$$\begin{aligned} i_{p+} &= 2i_{ref} + i_m \\ i_{p-} &= -i_m \end{aligned} \quad . \tag{7.14}$$

The output ripple current i_x is defined as the inductor current i_L minus its dc level. We can express i_x as a Fourier series

$$i_x = \sum_{n=-\infty}^{\infty} C_n e^{jn\omega_o t} \tag{7.15}$$

where

$$\omega_o = \frac{2\pi}{T} \quad . \tag{7.16}$$

The power spectral density of the ripple current is then

$$S_{i_x}(\omega) = 2\pi \sum_{n=-\infty}^{\infty} |C_n|^2 \, \delta(\omega - n\omega_o). \tag{7.17}$$

This yields an rms ripple current value of:

$$i_{x,rms} = \sqrt{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i_x}(\omega)d\omega} = \sqrt{\sum_{n=-\infty}^{\infty} |C_n|^2} \, . \tag{7.18}$$

Now we break down the single RPI into an equivalent N-cell PRPI as shown in Fig. 7.7, where the k^{th} cell has parameters

$$\begin{aligned} C_{r,k} &\approx \frac{C_r}{N} \\ L_{r,k} &\approx NL_r \end{aligned} \, . \tag{7.19}$$

For these parameters, we find

$$\begin{aligned} i'_{p+} &= 2\frac{i_{ref}}{N} + \frac{i_m}{N} \\ i'_{p-} &= -\frac{i_m}{N} \end{aligned} \tag{7.20}$$

and a switching period of the k^{th} cell of approximately

$$T_k \approx \frac{V_{dc}L_{r,k}(i'_{p+} + |i'_{p-}|)}{\frac{1}{4}V_{dc}^2 - V_{cf}^2} \, . \tag{7.21}$$

The output current waveforms of the cells are essentially $1/N$ scaled versions of the single RPI output current with small variations in frequency due to deviations of the individual cell parameters from their nominal values.

We can express the output ripple current of an individual PRPI cell as:

$$i'_{x,k} = \sum_{n=-\infty}^{\infty} C_{k,n} e^{jn\omega_k t} \tag{7.22}$$

where

$$\omega_k = \frac{2\pi}{T_k} \tag{7.23}$$

and

$$C_{k,n} \approx \frac{C_n}{N} \ . \tag{7.24}$$

The power spectral density of the k^{th} cell output ripple current is:

$$S_{i'_{ripk}}(\omega) = 2\pi \sum_{n=-\infty}^{\infty} |C_{k,n}|^2 \delta(\omega - n\omega_k) \ . \tag{7.25}$$

Because the T_k's are not identical due to parameter variations among the cells (including resonant component values, sensor gains, etc.), the power spectral density of the total ripple current is the sum of the power spectral densities of the individual cell ripple currents. Thus, for the PRPI case, the power spectral density of the total ripple current is

$$\begin{aligned} S_{i'_x}(\omega) &= 2\pi \sum_{k=1}^{N} \sum_{n=-\infty}^{\infty} |C_{k,n}|^2 \, \delta(\omega - n\omega_k) \\ &\approx \frac{2\pi}{N^2} \sum_{k=1}^{N} \sum_{n=-\infty}^{\infty} |C_n|^2 \, \delta(\omega - n\omega_k) \ . \end{aligned} \tag{7.26}$$

This leads to an rms ripple current of

$$i'_{x,rms} = \sqrt{\frac{1}{2\pi} \int_{-\infty}^{+\infty} S_{i'_x}(\omega) d\omega} \approx \sqrt{\frac{1}{N} \sum_{n=-\infty}^{\infty} |C_n|^2} \approx \frac{i_{x,rms}}{\sqrt{N}} \ . \tag{7.27}$$

Hence, if a single large RPI is replaced by an equivalent N-cell PRPI, a $N^{1/2}$ reduction in rms output ripple current is expected when the converters are controlled autonomously (without ripple cancellation

control).

To verify this result, the example RPI of Fig. 7.8 was simulated over one line cycle using the method of Section 7.4.1, and the rms ripple current was calculated. This was repeated for equivalent PRPI converters of 2 through 15 cells. To model the parameter variations occurring in real converters, a uniformly distributed 5% random variation in resonant component values was used. The results of these simulations, plotted in Fig. 7.10, corroborate the analysis.

Thus, the use of a PRPI significantly reduces the requirements on the output filter compared to a single RPI, even when the converters are controlled autonomously. The same ripple cancellation effects can be expected with an output voltage control loop closed, providing that the control strategy does not induce sympathetic synchronism between individual cells. Interdependent current control of the cells or locally-controlled ripple cancellation schemes would further improve the advantage of the PRPI.

7.5 Conclusion

This chapter discusses some key issues in the design of cellular converter systems, including the impact of replicated and added components and the need for instantaneous current-sharing among cells. The chapter also presents a new cellular inverter implementation based on the resonant pole inverter topology which addresses these design issues. It is shown that the new cellular implementation meets the important objective of minimizing the required output magnetics, while retaining the simplicity of the basic bridge structure. Furthermore, we show that the approach mitigates some of the major drawbacks of the single RPI.

An enhanced current control scheme applicable to both the new parallel architecture and the single RPI is also introduced. This control scheme significantly reduces converter losses and stresses under many operating conditions compared to the conventional control method.

Finally, the chapter analytically quantifies the amount of passive ripple cancellation which occurs among cells in a PRPI system. We show that a $N^{1/2}$ reduction in total rms ripple current is expected when N autonomously-controlled converters are paralleled. This important result is corroborated via piecewise simulation of the new parallel architecture.

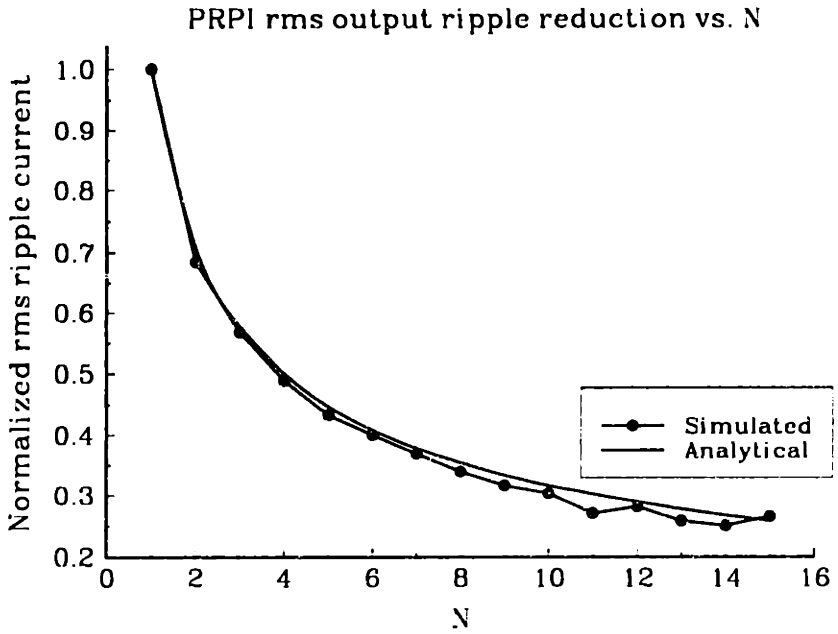


Figure 7.10 Theoretical and simulated reductions in rms current ripple vs. N for the PRPI.

Chapter 8

Design and Evaluation of a Cellular Rectifier System

8.1 Introduction

The cellular conversion approach has several potential advantages over conventional methods of designing and constructing power converter systems. To realize these advantages, however, and to allow the benefits and limitations of the approach to be fully evaluated, it is necessary to experimentally establish the viability of the cellular architecture concept at a reasonable power level. This allows the performance of the technology to be verified, and permits the identification of remaining barriers to its adoption.

This chapter describes the design, implementation, and experimental evaluation of a six-cell, six-kilowatt cellular converter. The cellular converter system implements both distributed load-sharing and distributed ripple cancellation, and mitigates some of the major drawbacks of its single converter counterpart. In addition to its function in evaluating the cellular design approach, the implemented system is designed to be a high-power test bed for new cellular converter control methods.

While the cellular architecture appears suitable for many power conversion functions, its application to rectifier design is particularly straightforward. Furthermore, the increasing importance of input power quality makes improved rectification methods important for many commercial and industrial applications. For these reasons, we have applied the cellular conversion approach to the design of a three-phase high-power-factor rectifier system. The implemented six-cell, six-kilowatt system rectifies the three-phase 208 Volt mains to a 410 Volt dc output at nearly unity power factor. These levels of voltage and power are applicable to a variety of applications, and provide a suitable framework for evaluating the cellular approach.

Section 8.2 describes some of the motivations for the use of a cellular architecture in rectifier applications, and provides an introduction to the cell topology used in the prototype system. Section 8.3 describes the operation of the selected cell topology in detail, and quantifies the effects of interleaving

the cells. Section 8.4 describes the design of the prototype system, Section 8.5 provides experimental results from the laboratory prototype, and Section 8.6 draws conclusions and presents a preliminary evaluation of the approach.

8.2 Application of the Cellular Architecture to Switched-Mode Rectification

The emergence of recent standards and recommendations on power quality reflect a growing need to reduce the impact of electronic equipment on the utility. While only voluntary measures such as IEEE Std 519-1992 are currently in place in the United States [62], European Community countries have already moved towards stronger controls. Restrictions on line harmonics are already in place for household and similar electrical equipment up to 415V, 16 A [63,64], and future regulations will apply to equipment with higher ratings [65]. These developments have lead to an increased interest in switched-mode rectifiers which draw quasi-sinusoidal input current at high power factor, and produce a controlled output voltage.

The full-bridge converter (Fig. 8.1) is often used for switched-mode rectification. However, this solution requires a high number of active switches (and attendant ancillary circuitry), and is relatively complex to control. Another approach is to utilize a single-phase switched-mode rectifier for each phase of the three-phase input, though this solution retains much of the complexity of the full-bridge converter. A desire to attain the performance advantages of these rectifiers without the high level of complexity has led to the development of the three-phase single-switch boost rectifier of Fig. 8.2. This converter topology, introduced in [66], has undergone rapid development in recent years [67-74].

The operating principle of this discontinuous-mode converter is as follows. The switch Q_1 is turned on at the beginning of each (fixed-length) switching period, and held on for a specified duty cycle, d. During this on period, the diode-bridge inputs are shorted together through the diodes and switch Q_1.

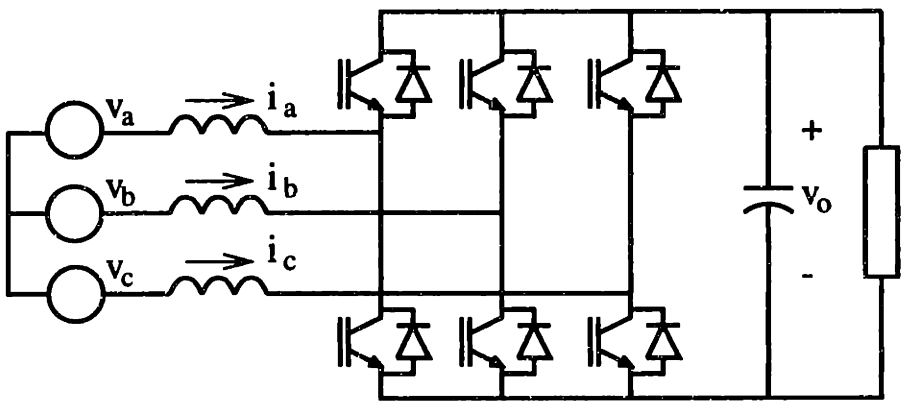


Figure 8.1 The three-phase full bridge converter configured for use as a switched-mode rectifier.

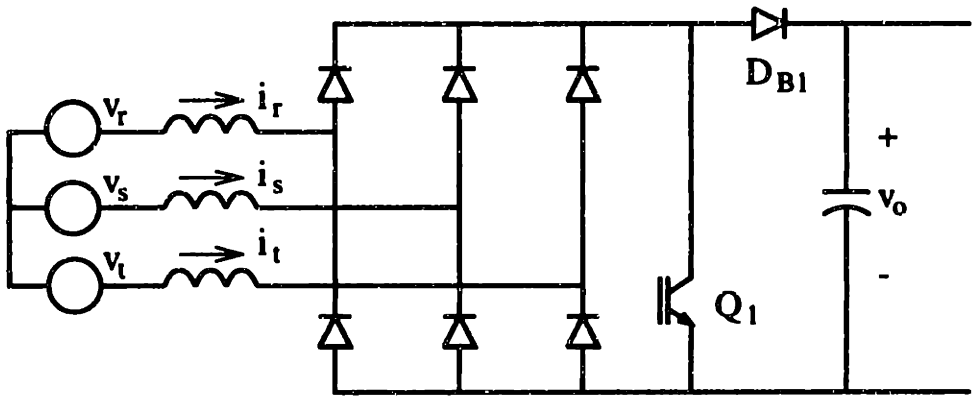


Figure 8.2 The three-phase single-switch boost rectifier.

Neglecting the effects of the input filter, the inductor currents i_r, i_s, i_t, rise from zero by an amount proportional to their respective phase voltages. When Q_1 is turned off, the inductor currents are discharged back to zero through diode D_{B1} and the output capacitor. Thus, to first order, the average current delivered from each phase is proportional to the phase voltage, yielding fundamentally resistive behavior. The average total current delivered to the output is simply controlled by varying the duty cycle of switch Q_1, while the output voltage v_o is controllable to voltages above the peak line-to-line mains voltage.

With its supporting input filter, this topology provides high power factor input current waveforms using a single ground-referenced active switch and a very simple control strategy. The discontinuous-mode operation minimizes the energy storage requirements of the input inductors and provides soft turn-off of the diodes. However, it also subjects the devices to relatively high peak current stresses. Furthermore, the converter requires a relatively large input filter to attenuate the input current switching harmonics to acceptable levels (to meet conducted EMI requirements, for example). The size of the input filter is perhaps the single largest drawback to the approach.

Obtaining a high-quality utility interface using conventional approaches seems to require either a complex converter or a large front-end filter. The cellular architecture provides an alternative to these approaches. We propose that applying the single-switch rectifier topology for the cells of a cellular architecture will result in a simple, high-quality utility interface with significant advantages over conventional approaches.

Consider the benefits of paralleling cells constructed using the single-switch rectifier topology. The single-switch rectifier has many of the desired characteristics for a utility-interface converter, except for its high level of unfiltered input ripple current harmonics. *Interleaving* of paralleled converter cells, in which the individual cells are switched out of phase, allows a high degree of harmonic cancellation

between the cell currents [7-10]. This results in greatly reduced aggregate input and output ripple, along with a commensurate reduction in filtering requirements. Interleaving of paralleled single-switch boost rectifiers has been previously demonstrated to be effective for reducing the high input current ripple associated with this topology [74,75]. By using a cellular conversion approach, and applying the concept of interleaving, the topology of Fig. 8.2 can be applied to create a simple, high power factor utility interface with minimal input filtering.

Other advantages of cellular architectures also apply to this application. For example, utility interface converters often need to be constructed in a variety of ratings. By applying a cellular architecture, it is possible to construct a family of systems with a range of ratings using a single cell design. The power rating of a specific system is determined by the number of cells used. Unlike a single large converter, the individual cells can be constructed using single-die devices in inexpensive packages, and manufactured using an automated assembly process. The coupling of these facts may lead to a significant cost advantage over a conventionally designed system. Furthermore, because a cellular system can be designed to operate after individual cell failures, significant improvements in reliability and availability may be obtained. Thus, there are several important ancillary advantages to employing a cellular architecture in rectifier applications.

8.3 The Three-Phase Single-Switch Boost Rectifier

The single-switch boost rectifier has many characteristics which make it well suited for use in a cellular architecture. Because this type of converter operates in discontinuous conduction mode, the magnetic energy storage requirements are low, and ripple cancellation techniques can yield large performance benefits. Furthermore, sensing and control for this topology is quite simple and inexpensive, thus minimizing replicated component costs. Finally, the topology is well suited to high-frequency operation, and can easily be adapted for full soft switching [70-72].

It should be pointed out that there are topological constraints associated with paralleling single-switch boost rectifiers. As described in [74,75], in order to parallel converter cells of this type, an additional boost diode must be added in the return path of each cell as shown in Fig. 8.3. The diode is needed to prevent cross-conduction among different converter cells; without it, current flowing from the positive phase and through the transistor of one cell can return through the negative phases of a different cell. Incorporating the additional diode in each cell ensures that this cannot happen, and makes the cells operate independently. In addition to causing a slight decrease in efficiency, the additional diode prevents the active switch in Fig. 8.3 from being referenced to ground. As a result, it has to be driven

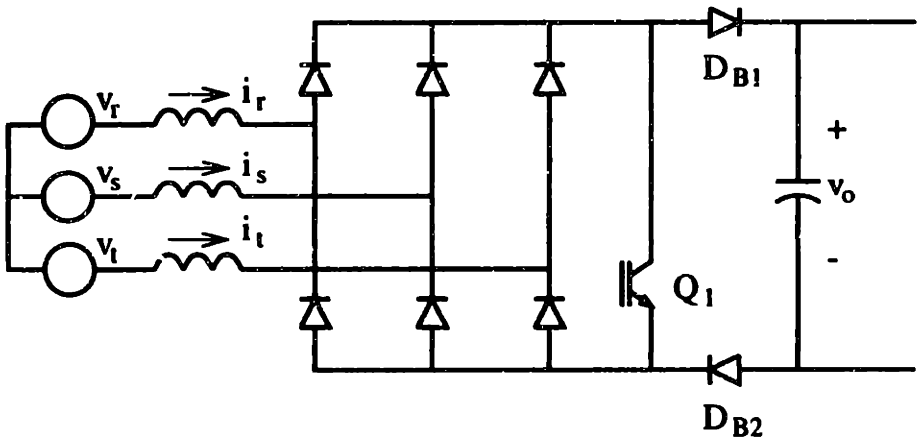


Figure 8.3 The three-phase single-switch boost rectifier with an additional diode to allow paralleling.

through a floating gate drive circuit. However, these disadvantages are heavily outweighed by the tremendous performance increases that can be gained through interleaving in a parallel architecture.

This section considers the operational details of the three-phase single-switch boost rectifier, and describes its expected performance when interleaved with other cells of the same type. We will assume the converter is supplied from a balanced, sinusoidal three-phase input, and consider only fixed-frequency operation of the converter (though other methods are possible [67]). Furthermore, we will assume that the switching frequency of the converter is much greater than the line frequency, such that the input voltages can be considered approximately constant during a switching cycle.

8.3.1 Principle of Operation

The operating principle of this converter has been well described in a number of publications including [67,68], but is reviewed here for clarity. Figure 8.4 shows a switching cycle of the single-switch rectifier during the time period when input phase *r* is the most positive and input phase *t* is the most negative. Operation at any time during a line cycle can be inferred from this case. At the beginning of State 1, all of the inductor currents are zero, and the boost switch Q_1 is turned on at zero current. During State 1, the three inductor currents rise linearly from zero at a rate proportional to their respective phase voltages. At a controlled time $t_{\mu 1} = dT$, the boost switch is turned off, and state 1 ends. At the end of state 1, the inductor currents are proportional to their individual phase voltages and to the duty ratio *d*. At the beginning of state 2, the boost diode turns on, and the three inductors begin a linear discharge through the output. The rate of discharge of the inductor currents depends on the phase voltages and the output voltage. State 2 ends at $t_{\mu 2}$, when the inductor current of phase *s* reaches zero,

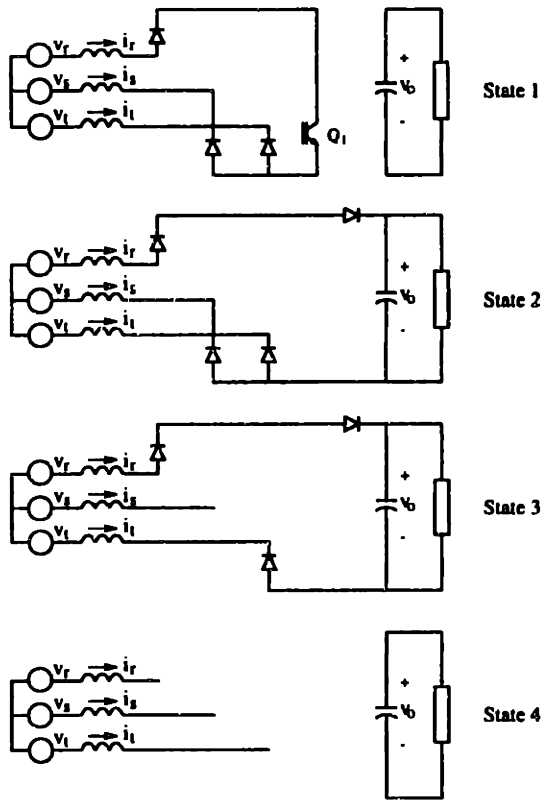


Figure 8.4 The switching cycle of the single-switch boost rectifier for the portion of the line waveform where phase *r* is the most positive and phase *t* is the most negative.

and its bridge diode ceases to conduct. During state 3, the remaining two inductor currents are equal and opposite, and discharge (at a new rate) through the output until they reach zero at time $t_{\mu 3}$, when the remaining devices turn off. During the final part of the switching cycle, State 4, no devices conduct.

To maintain discontinuous mode operation, the output voltage must be higher than the peak line-to-line input voltage, and the duty ratio of the boost switch must be held below a maximum value. Defining the boost ratio, M, as the ratio of the output voltage to the peak line-to-line input voltage

$$M = \frac{V_o}{V_{l\text{-}l,peak}} , \tag{8.1}$$

it can be shown that the maximum allowable duty ratio for discontinuous mode operation is [68]:

$$d_{max} = \frac{t_{\mu 1,max}}{T} = \frac{M - 1}{M} . \tag{8.2}$$

The output voltage of the system can be regulated directly via duty ratio control. Consider a point $\omega t = \varphi$ in the line cycle where $\varphi \in [0,\pi/6]$, and $\varphi = \pi/12$ is the peak of a line-to-line input voltage. The

local average output current at this point as a function of duty ratio, and can be shown to be [67]:

$$\bar{i}_{out} = \frac{2V_o T}{3L} \cdot \left[\frac{3d^2}{8M^2} \cdot \frac{1 - M^{-1}\cos(\varphi)\cos(2\varphi + \frac{\pi}{6})}{(1 + \sqrt{3}M^{-1}\sin(\varphi - \frac{\pi}{6}))(1 - M^{-1}\cos(\varphi - \frac{\pi}{6}))} \right] . \qquad (8.3)$$

Thus, by controlling the duty ratio, the local average converter output current, and hence the converter output voltage, can be controlled.

8.3.2 Input Line Currents

During the transistor-on state (State 1), the peak (and average) inductor current drawn from each phase is proportional to the phase voltage. The average inductor current drawn from each phase during States 2 and 3 depends on the output voltage as well as the phase voltage. For very high output voltages (where most of the conduction time is spent in State 1), the average current drawn from each phase over the whole switching cycle is proportional to the phase voltage. The converter thus draws (local average) line currents which track the phase voltages, and hence operates at unity power factor. As the output voltage is lowered, the converter spends more time in states 2 and 3, and the average input currents do not perfectly track the phase voltages. Nevertheless, over a wide range of boost ratios, the average current waveforms drawn from the line still yield a very high power factor. For example, boost ratios of greater than 1.22 yield power factors of better than 0.98 for a fixed duty ratio [68].

It should be pointed out that the line current waveforms and power factor drawn by a single-switch boost rectifier do depend on the output voltage control strategy. Low-bandwidth control of the output voltage, in which the duty ratio remains relatively constant over $1/6^{th}$ of a line cycle, yields distortion levels that are mainly dominated by the 5^{th} harmonic. High-bandwidth control of the output voltage, in which the duty ratio is allowed to vary within a line cycle, yields even lower input current distortion levels, with equal distortion due to the 5^{th} and 7^{th} harmonics. (Averaged equations for input line currents, along with nomographs showing input current waveshape and harmonic content vs. boost ratio can be found in [67] for different control strategies. In addition, Matlab routines for computing many of the quantities of interest can be found in Appendix B.) Furthermore, duty ratio control methods explicitly geared towards minimizing of the input line harmonics (to comply with harmonic standards such as [63,64]) have also been developed for this topology. What may be concluded from this is that for acceptable boost ratios and control strategies, the single-switch boost rectifier is capable of generating a controlled output voltage while operating at a high power factor.

8.3.3 Interleaving of Three-Phase Single-Switch Boost Rectifiers

One of the primary benefits of using the three-phase single-switch boost rectifier in a cellular architecture is the ability to use interleaving to cancel the large input (switching) current ripple drawn by the topology. This is an important benefit, since the input filters required for meeting EMI specifications can be quite large for this converter topology (possibly even larger than the converter itself), due to the fact that it operates in discontinuous conduction mode. This section investigates the amount of ripple reduction which can be expected through interleaving, and assesses its likely impact on system design.

One important characteristic of this rectifier is that the switching ripple frequency content includes components not only at the switching frequency and its harmonics, but at the sum and difference frequencies of the line and switching frequencies and their harmonics. Practically speaking, this means that the switching ripple energy is concentrated in bands, which we term switching harmonic *groups*, centered around multiples of the switching frequency. This occurs because the input voltage variations cause the switching ripple to vary with position in the line cycle. Computationally, the easiest way to handle this is to consider cases where the switching frequency is an exact multiple of the line frequency. In this case, all of the switching energy is concentrated at multiples of the line frequency, and the spectral content is easily calculated using discrete-time methods (see Appendix B).

The primary benefit to interleaving single-switch boost rectifiers is the reduction in input current

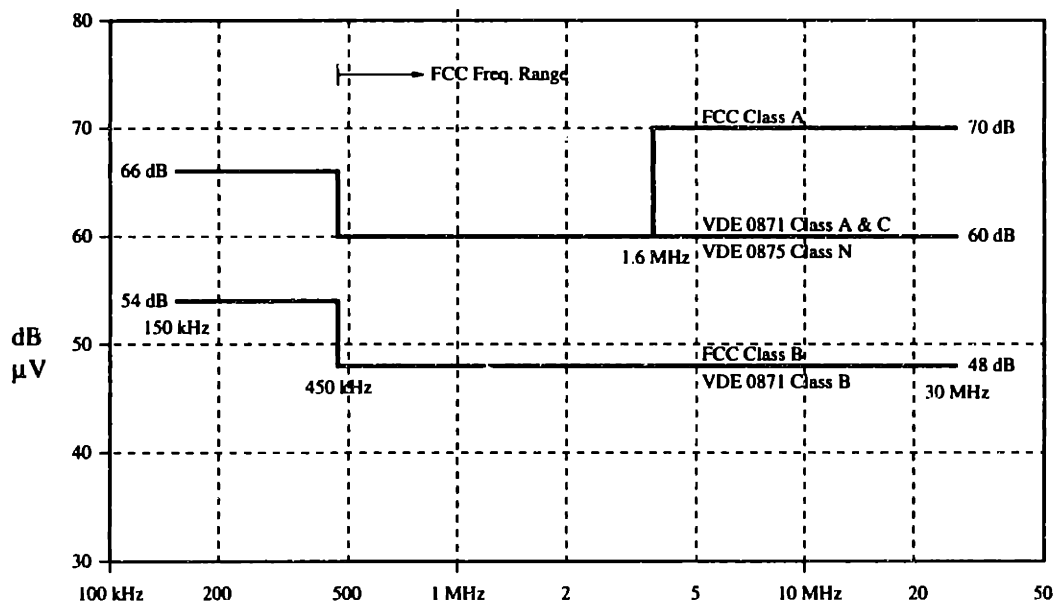


Figure 8.5 Conducted EMI limits as specified by the FCC and VDE. Conducted EMI is measured across a 50 Ω Line Impedance Stabilization Network with a receiver having a measuring bandwidth of 9 kHz.

ripple that can be achieved, and the corresponding reduction in the input EMI filter size and cost. Figure 8.5 shows some of the conducted EMI limits specified by various regulatory agencies. What may be drawn from this figure is that the limitations on input current spectral content tend to be flat over an extremely wide frequency range, and are not indexed to equipment power level. Furthermore, because the receivers used for making conducted EMI measurements have a 9 kHz measurement bandwidth, the spectral components within a switching harmonic group are lumped together for purposes of meeting EMI specifications.

Interleaving N converter cells has two beneficial effects in terms of meeting EMI limits. First, it tends to attenuate (by cancellation) the first N ripple harmonic groups in the spectrum (which are the hardest to eliminate by filtering), as well as harmonic groups at higher frequencies. Second, it reduces the net ripple amplitude by a factor N or more, thus reducing the peak ripple for which the EMI filter has to be designed.

To gain a quantitative understanding of these benefits, consider the comparison of a single large converter with equivalent interleaved converter systems having 2, 4, and 6 cells. For our purposes, an "equivalent" system has the same total magnetic energy storage, cell switching frequency, and output power as a single large converter. We consider the example of a three-kilowatt converter (L = 6.7 μH, f_{sw} = 150 kHz) which generates a 410 V output from a 208 V (line-to-line, rms) input. At each frequency, we compute the worst ripple component that occurs within each switching harmonic group across the load range of the converter and across a +10% / -15% variation in input voltage. Figure 8.6 (a) shows these worst-case spectral components for the single large converter, while Figures 8.6 (b)-(d) show the results for equivalent interleaved converter systems with 2, 4, and 6 cells.

In the single-cell system, the worst-case harmonic component to filter is 173 dB μV at 150 kHz. For the two-cell case, this worst-case first harmonic group component is reduced by some 65 dB, leaving the second harmonic-group component as the worst to be filtered (163 dB μV at 300 kHz). The reduction in amplitude and increase in frequency of the worst-case component considerably eases the requirements on the EMI filter. With four and six cells, the first major peaks are 151 dB μV at 600 kHz, and 143 dB μV at 900 kHz, respectively. (Because higher frequencies are much easier to filter, the first switching harmonic group component may in fact *still* be the hardest to filter for these highly interleaved cases.) What is clear from these results is that the amount of EMI filtration required to meet the standards of Fig. 8.5 is reduced considerably when several cells are interleaved, and is significant even for a modest degree of interleaving.

One issue that should be addressed when designing a cellular system is the effect on input current

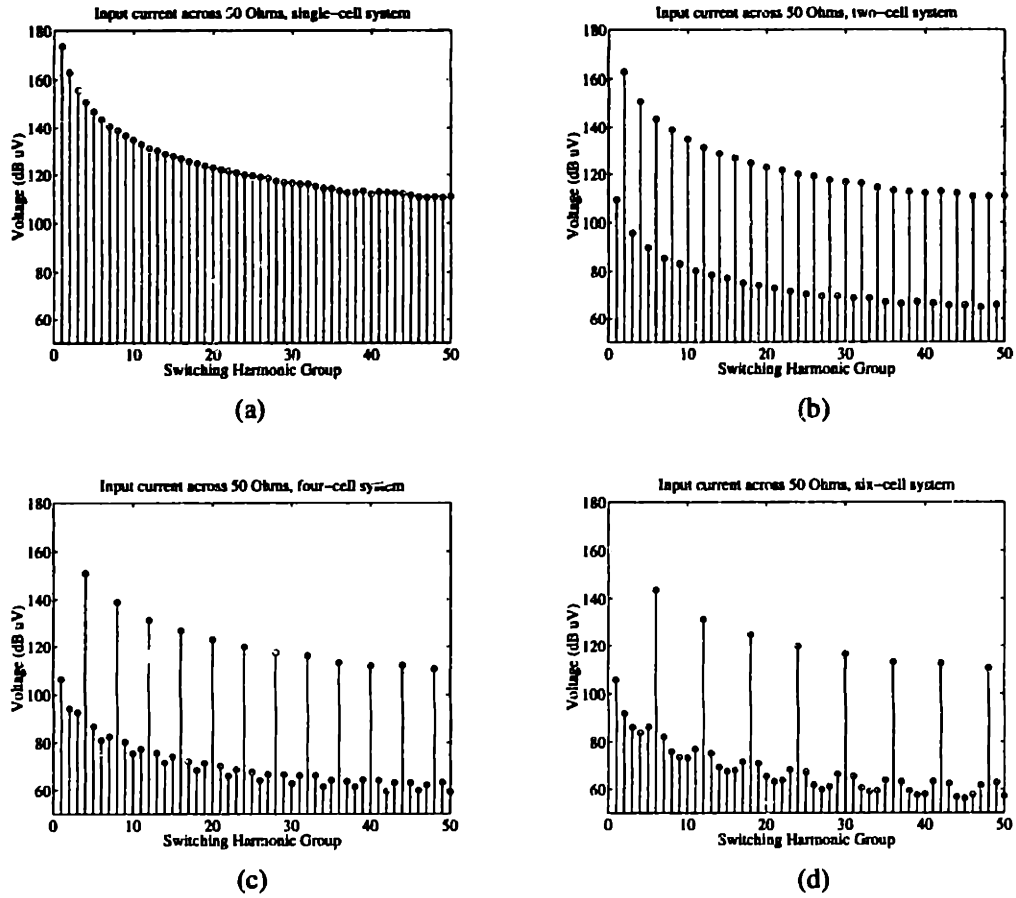


Figure 8.6 Worst case input current ripple spectral components for example three-kilowatt rectifier systems. (a) Single-cell system. (b) Two-cell system. (c) Four-cell system. (d) Six-cell system.

ripple when the number of cells in the system is allowed to vary. For example, consider the six-cell system of Fig. 8.6 (*d*). Given an EMI filter that is designed to exactly meet one of the specifications of Fig. 8.5, one might ask whether the system would meet the same EMI limits with fewer cells operating. If five of the cells were removed (leaving a single operating cell), then the worst case spectral components would be the same as in Fig. 8.6(a) but reduced by a factor of 6 (15.6 dB). Because of the lack of ripple cancellation, a single cell operating alone would not meet the EMI specification met by the full six-cell system. Thus, when designing a cellular converter system and its input filter, one must carefully specify the conditions under which ripple specifications will be met, and consider the effect of the number of operational cells on the ripple.

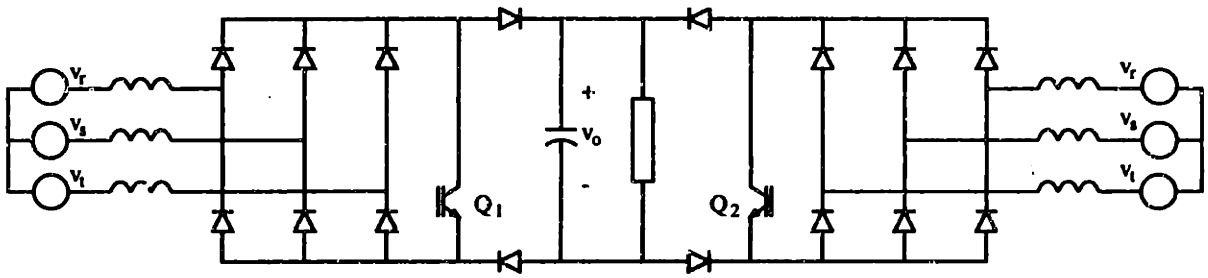


Figure 8.7 Structure of a single cell composed of two interleaved single-switch converters.

8.4 Prototype System Design

This section describes the design of a six-cell, six-kilowatt prototype system which rectifies the three-phase 208 Volt mains to a 410 Volt dc output at high power factor. The input supply voltage is assumed to stay within tolerances of +10% and -15%, while the output voltage is regulated to within ±3% of nominal. The system implements both distributed load sharing (via the UC3907 load-sharing control method [32]) and distributed interleaving (via the method developed in Chapter 6), and is designed to allow other control methods to be easily implemented through the use of "piggyback" control boards.

We will describe the system architecture and cell power stage design, the control structure, and the fusing and protection methods. The methods used to select the cell parameters and components will also be described. The methods used for computing semiconductor and magnetics losses are described in Appendix A, while Appendix B contains Matlab routines used in the system design. Full schematics and layout information for the cells are provided in Appendix C.

8.4.1 System Architecture

The prototype system has six cells, each of which has a nominal output rating of 1 kW and is designed to handle an output power of 110% of nominal. Each cell is constructed on a single printed circuit board as two interleaved single-switch boost rectifiers (which we term *half*-cells) driven from a common control circuit, as illustrated in Fig. 8.7. This affords some efficiency in the use of control and sensing circuitry, and reduces the ripple generated by an individual cell. A photograph of a completed cell is shown in Fig. 8.8, and the cell schematics and layout are provided in Appendix C.

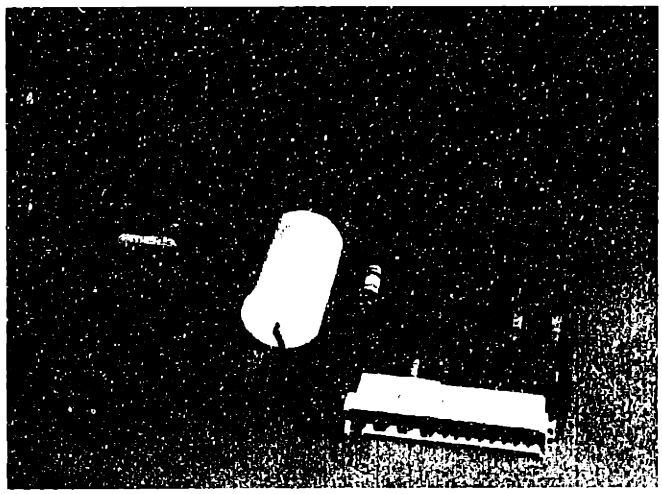


Figure 8.8 A photograph of a prototype converter cell.

In their baseline configuration, the cells implement the UC3907 distributed load-sharing control scheme [32]. A single-wire connection among all six cells is provided in the backplane for this purpose. Distributed interleaving control is implemented separately for two groups of three cells using the method developed in Chapter 6. A separate single-wire connection (interleaving bus) is provided in the backplane for each group. Within each group, up to three cells will interleave among themselves and cancel ripple, while the two *groups* cancel ripple passively, as described in Chapter 6.

The prototype system is designed to fit in a standard 19" rack assembly (ELMA Electronics, Fremont, CA). Each cell fits in a 6U (10.5") high, 14T (2.8") wide module, and connects into the

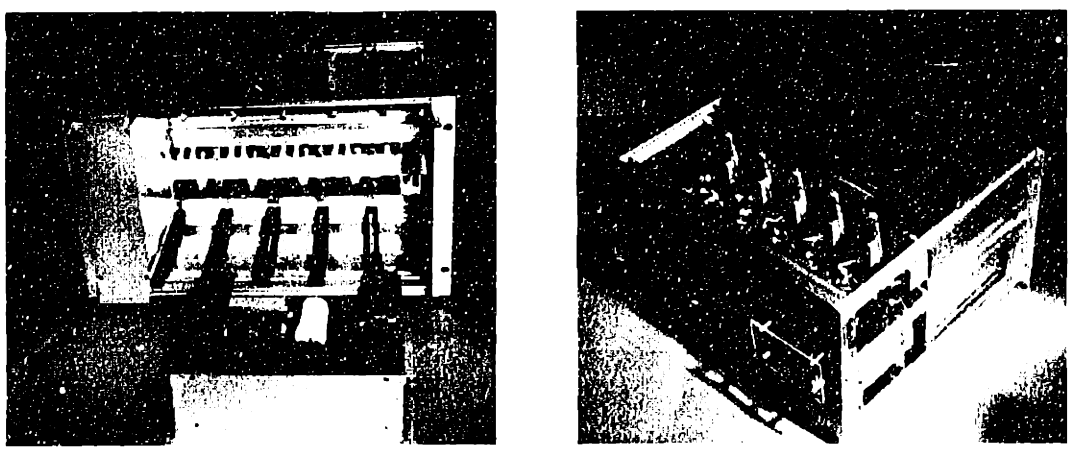


Figure 8.9 Pictures of the prototype system with covers removed.

backplane via a DIN41612MH connector. In addition to the interconnections for current-sharing and ripple cancellation, the backplane comprises a low-inductance three-phase input bus, and a low-inductance output/ground bus, both of which are wired to an external connector. The connections are such that all of the cells are connected to the low-inductance busses through similar impedances. Figure 8.9 shows the prototype system with the covers removed to show the internal structure.

8.4.2 Cell Power Stage Design

Design of the cell power stage centered on the task of selecting the cell inductances and switching frequency such that the cell would meet its rated output power over the specified input voltage range with each half-cell operating in discontinuous conduction mode. This had to be accomplished while meeting the conflicting goals of minimizing component size and cost and minimizing the losses and temperature rises. This was accomplished using the following automated procedure: Given a specified switching frequency, the method of [68] was used to select a boost inductance value which met the operational requirements and fully utilized the available conduction time in a cycle (in fact, only 90% of the theoretical maximum duty ratio was employed to leave a safety margin). Given a switching frequency and inductance value, expected semiconductor losses were computed, and candidate inductor designs were identified and their expected losses computed. This process was repeated across a wide range of switching frequencies, yielding a set of candidate designs from which the final design was selected. Methods for predicting losses for the semiconductor and magnetic elements are described in Appendix A, and Matlab code for implementing these methods can be found in Appendix B.

The identification of candidate inductor designs was based on a database of standard Ferroxcube (Phillips) square-cut 3F3 ferrite cores (sizes RM8 - RM14) and wire data. For a specified switching frequency and inductance value, each core was evaluated as follows. First, the required number of turns and resulting peak flux density were computed. If the flux density exceeded 0.3 T, the core was rejected as a candidate. Next, the largest possible wire size which fit on the core at the proper number of turns was identified. If the required current density at the largest wire size exceeded 3000 A/in^2, then the core was rejected as a candidate. Next, the expected power dissipation and worst-case temperature rise for the core were computed. If the core temperature rise exceeded 50° C, then the core was rejected. Otherwise, the inductor design was considered to be a potential candidate, and the design and its predicted characteristics were stored.

From the candidate designs, a switching frequency of 150 kHz and line inductances of 40.4 μH were selected for each half-cell. The inductors were constructed using eleven turns of twelve gauge wire on

an RM12PA315 core. This core is one size larger than necessary, to provide flexibility for future uses. IRF840G MOSFETs were used for the main boost switches, and HFA08TB60 ultra-fast recovery rectifiers were used for the boost diodes. These were attached to PC-board mountable extruded heat sinks; sufficient cooling was obtained using natural convection, due to the distributed nature of heat generation in the cellular system. MUR160 ultra-fast recovery diodes were used for the input bridges. The use of extremely fast diodes for the input bridges was found to be necessary to achieve proper operation at the selected switching frequency. Because the input is three-phase, there is little low-frequency ripple in the output voltage. Hence, only a single 10 μF film capacitor was used at the output of each cell. (It should be noted the CDE 935C4W10K capacitor used in the system is nominally rated for 400 V. However, slight derating of the operating temperature range allows its use at the slightly higher voltages encountered in the prototype system.)

In terms of fusing and protection, each cell is provided with high-speed (semiconductor) fuses at the input, and a slower fuse at the output. Inrush current limiters are placed in series with the boost inductors to soften the startup transient, and the UC3825 PWM controller provides both soft-start and current-limit protection functions. The MOSFET switches have RCD snubbers which clamp their drain voltages to a value slightly higher than the output voltage, and a Metal Oxide Varistor (MOV) provides absolute fault-condition clamping protection on the output voltage.

8.4.3 Control Design

In the baseline configuration of the system, the individual cells employ duty-ratio control of the output voltage. Due to the discontinuous conduction-mode operation of the half-cells, controlling duty ratio is equivalent to controlling the local average cell output current, as determined by **(8.3)**. Using **(8.3)**, we can make an injected current model for each half-cell

$$i_{out} = K_f d^2 \tag{8.4}$$

where K_f varies from 13.75 to 55.0 over the line cycle for the parameters of the prototype system. Considering a proportional controller

$$d = K_p\left[v_{ref} - v_o\right] \ , \tag{8.5}$$

we find an output current characteristic of

$$i_{out} = K_f K_p^2\left[V_{ref} - v_o\right]^2 \ . \tag{8.6}$$

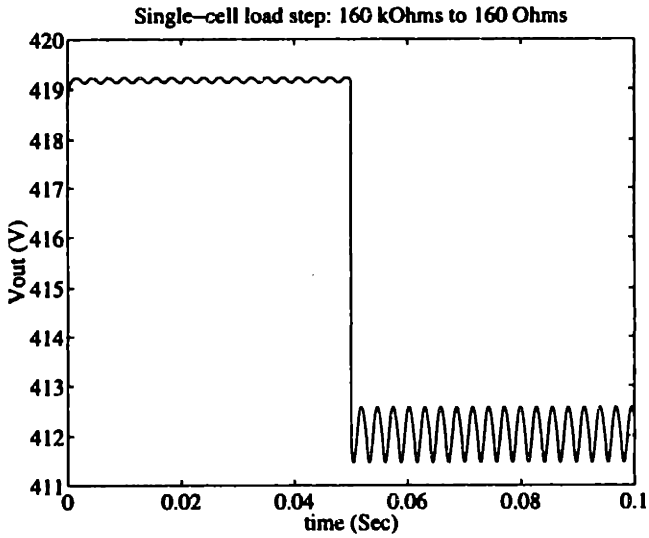


Figure 8.10 Simulated single-cell load step response from R_L = 160 kΩ to 160 Ω.

The half-cell thus has a resistive output characteristic, where the output resistance is load-varying, and also varies with position in the input line cycle; the output resistance of a full cell is precisely half that of a half-cell. It is easily shown that the incremental output resistance of each half-cell about an operating point is

$$R_{out} = \frac{1}{2K_p\sqrt{K_f I_{out}}} \tag{8.7}$$

which decreases with load current, and is only mildly affected by the position in the line cycle.

Using this model, the dynamics of a single cell or a parallel system employing the UC3907 current-sharing method are easily described using the methods of Chapter 5, and are guaranteed to be stable and well damped. For the prototype system, a proportional control gain K_p = 0.028 V^{-1} was selected. This value yields load regulation of less than 5% over the load range, and with a 10 μF output capacitor per cell yields an output voltage control bandwidth that exceeds the 360 Hz input voltage ripple frequency. Furthermore, because the output voltage is controlled with high bandwidth, the input line current harmonics are reduced as compared to low-bandwidth control [67]. Figure 8.10 shows the simulated response to a 1% to 100% load step for a single cell, and demonstrates the well damped control of the output voltage and the low feedthrough of input line ripple achievable with this control approach.

In its baseline configuration, the prototype system uses the UC3907 single-wire current-sharing control method. The resistive output impedance characteristic of the cells leads to current-sharing dynamics which are guaranteed to be stable and over damped, as described in the analysis of the UC3907

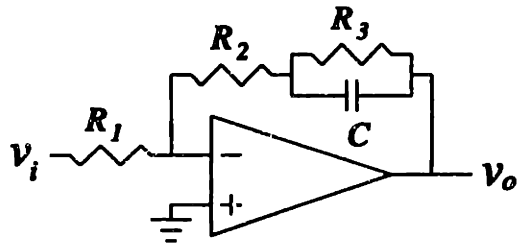


Figure 8.11 Loop filter structure for the prototype system. C = 0.68 μF, R_1 = 90.9 kΩ, R_2 = 10 kΩ, R_3 = 10 MΩ.

current-sharing method presented in Chapter 5.

Distributed interleaving among groups of (up to) three cells was implemented in the prototype system, using the method developed in Chapter 6. The clock generator design was similar to the system developed in chapter 6, with slightly different parameters. The clock generators implemented here employ a phase detector gain, K_d, of 7.95, and a VCO gain, K_v , of 6090 rad/(V-s). Both the base operation frequency and the phase detector gain can be adjusted via potentiometer settings. The loop filter of Fig. 8.11 is employed in the prototype system, yielding control dynamics which are stable and well damped for both two- and three-cell systems.

Finally, it should be noted that the control design specifications presented here are only for the baseline configuration. The prototype system includes provisions for overriding the on-board control circuits with those of a piggyback board. The controls can be overridden either for the clocking (to adjust interleaving) or for the entire control strategy (by allowing externally-generated gate drive signals to be used). Fully buffered current and voltage sense signals are provided for use by an external controller, and connections are provided for alternative current-sharing and ripple-cancellation busses to be added to the backplane. This provides a wide degree of flexibility, and makes the prototype system useful as a full-power test bed for new control methods.

8.5 Experimental Results

This section presents some experimental results from the prototype converter system. The prototype converter system was run both from the Cambridge utility through an isolation transformer, and from a Hewlett-Packard 6834B three-phase AC source. For simplicity, most results are presented with three cells operating, with additional results presented with the full complement of six cells.

The prototype system operated as designed over the entire load range. Figure 8.12 shows operation of the prototype system at 97% of full load (for three cells). As can be seen, the line current waveforms

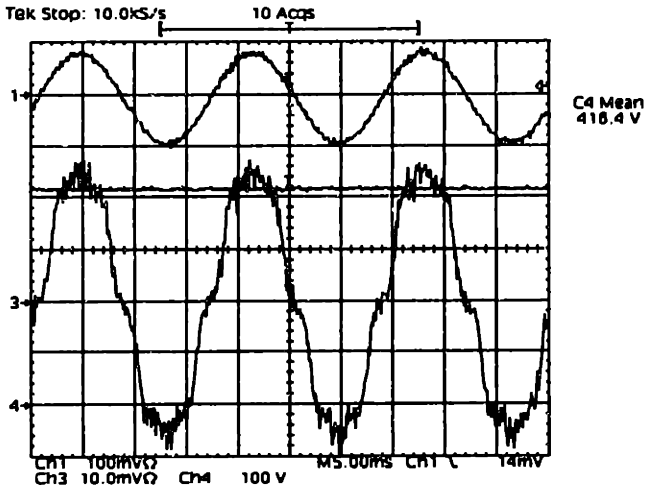


Figure 8.12 Circuit waveforms for 3 cells operating at 97% of full load (R_L = 60.2 Ω) from a 6834B AC source (60 Hz, 208 V). Channel 1 is the line voltage (200 V/div), channel 3 is the line current (5 A/div), and channel 4 is the output voltage (100 V/div). Note that the observed switching ripple is undersampled by the oscilloscope.

are quasi-sinusoidal, with the expected waveform shape (*cf* [67]). Figure 8.13 shows input line current harmonic data for the same load condition. The line harmonic content matches the theoretical predictions of [67] very closely, with the 5th and 7th harmonics contributing the majority of distortion. The power factor for this load condition is 0.994, with 10.3 % Total Harmonic Distortion (based on 40 harmonics),

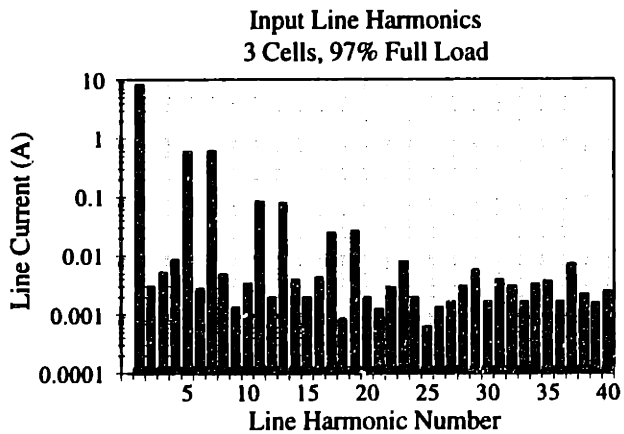


Figure 8.13 Input line harmonic data for 3 cell operating at 97% of full load (R_L = 60.2 Ω) from a 6834B AC source (60 Hz 208 V).

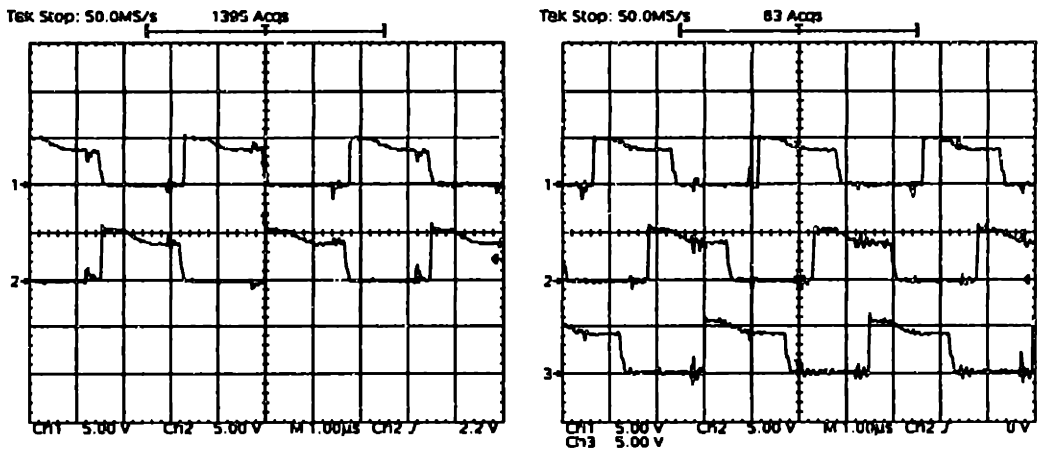


Figure 8.14 Clock waveforms for two and three cells. The system was operating at 70% of rated load in both cases.

both of which match theoretical predictions.

As can be seen from the small level of ripple in the line current of Fig. 8.12, the distributed interleaving greatly reduced the input switching ripple as compared to the non-interleaved case. The distributed interleaving circuitry functioned as expected over the load range for both the two- and three-cell cases, and the two interleaving groups operated independently (as desired) for up to the full complement of six cells. Figure 8.14 shows the clocks of the individual cells with the system at 70% of

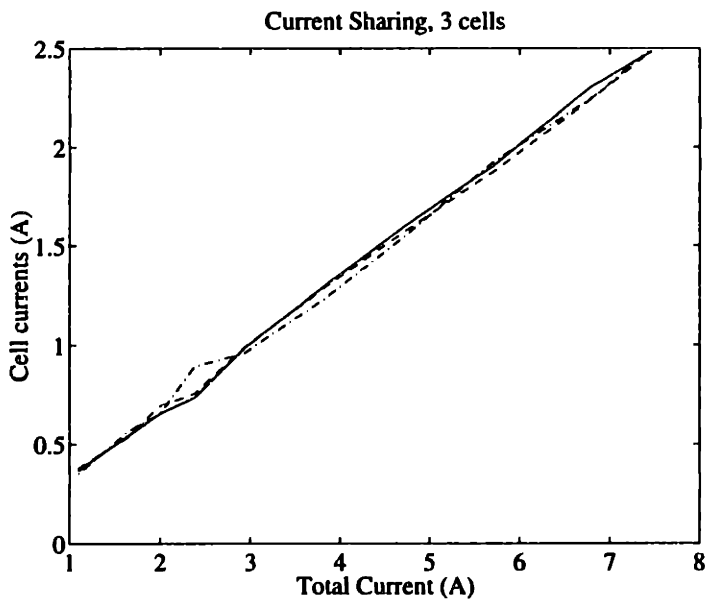


Figure 8.15 Current-sharing data for three cells.

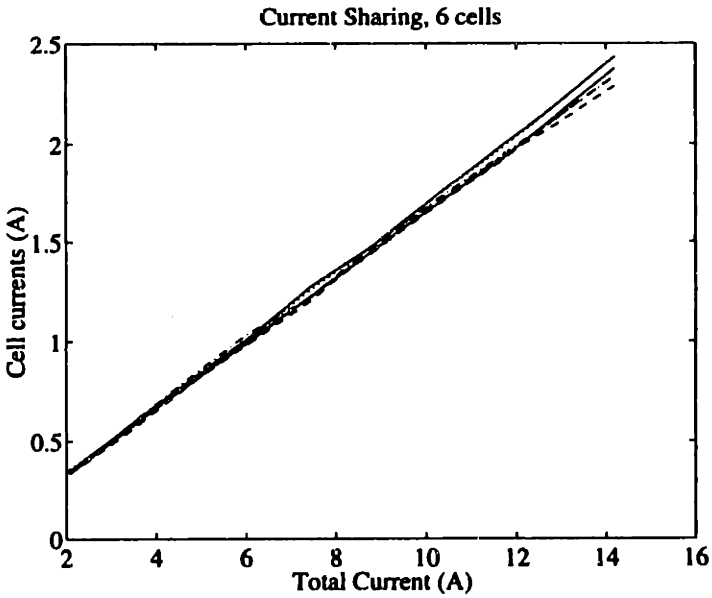


Figure 8.16 Current-sharing data for six cells.

full load for both the two- and three-cell cases. As can be seen, the distributed interleaving circuitry properly phased the individual switching waveforms in order to cancel the switching ripple in both cases.

The load-sharing and output voltage control behavior of the system also met performance expectations. Figure 8.15 shows the current-sharing characteristic for three cells over the load range, while Fig. 8.16 shows the current-sharing characteristic for six cells. Acceptable current sharing is achieved over the whole load range, with current sharing within a few percent is achieved over most of the range. The output voltage was regulated to within specifications over the whole load range, and the transient response was as expected for even large load steps. The transient behavior of the converter is shown in Fig. 8.17, which shows the output voltage response and its ac component for load steps between 20% and 60% of full load.

8.6 Conclusions

It may be concluded from these results that the prototype system successfully demonstrates the technical feasibility of the cellular design approach for this application. Controlled, high-power-factor rectification is achieved along with excellent output voltage and load-sharing regulation using entirely distributed control. The system also achieves a tremendous degree of input switching ripple cancellation as compared to a single large converter implementation, without requiring a centralized controller. This advantage alone merits the further development of the approach.

Other conclusions may also be drawn from experience with the developed system. The primary physical limitations to power throughput in the prototype system come from the dissipation limits in the active switch and bridge diodes, and to a much lesser extent, the inductors. The remaining system components (including the pc boards, bus bars, control circuitry, etc.) could all support much higher power throughput. Significantly increased power throughput could be obtained in the same physical structure at a low incremental cost through the use of larger single-die devices (in TO-247 or TO-251 packages), and/or through the addition of cooling fans within the cells. From a cost and utilization standpoint, therefore, this application would benefit from using cells rated at a higher power level than 1 kW. Furthermore, these facts support the conclusion of the previous chapter that, within a manufacturing framework, it is desirable to maximize the individual cell ratings.

Another issue exposed by the prototype system is the need for a detailed consideration of packaging and manufacturing. For example, mounting the cells within individual prefabricated modules (as was done in the prototype system) is aesthetic, helps protect the user (for hot-swap maintenance, etc.), and may add a degree of shielding between cells. However, the use of such modules adds significant cost and manufacturing effort to the task of constructing such a system, especially since it cannot be automated. The use of "bare" pc boards within a single-door enclosure is likely to be more desirable. Other packaging and manufacturing issues, including construction and mounting of heat sinks, semiconductor devices, and magnetic elements also warrant consideration.

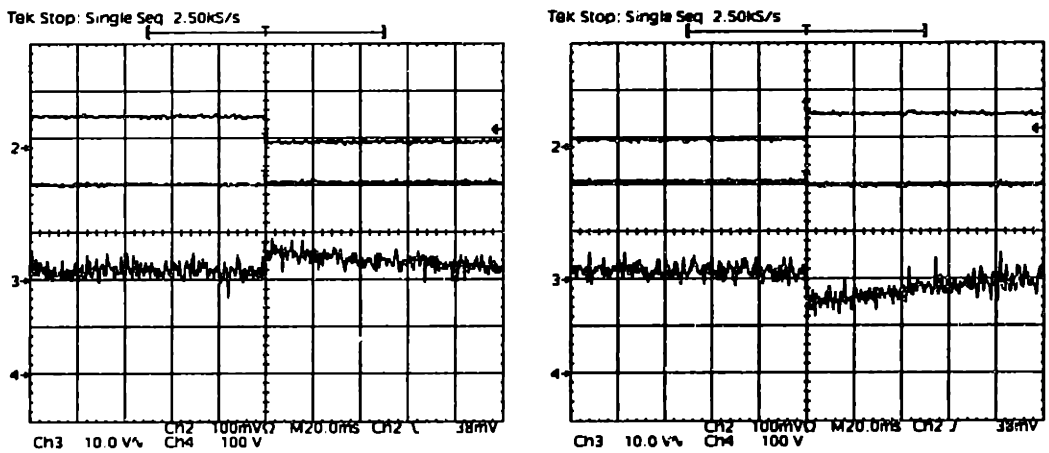


Figure 8.17 Load step responses between 20% and 60% of full load (295.6 Ω and 99.15Ω) for three cells. Channel 2 is the load step trigger, channel 3 is the ac component of the output voltage (ac coupled), and channel 4 is the output voltage (dc coupled).

Ultimately, the results achieved with the developed system to date argue compellingly for continued evaluation and development of the cellular power conversion approach. The prototype system will continue to be a useful tool for evaluating the cellular conversion approach, and due to its provisions for the use of "piggyback" control boards, will make an excellent test bed for further development of distributed control techniques.

Chapter 9

Summary and Conclusions

9.1 Thesis Summary

This thesis explores design and control of cellular converter architectures, with the aim of achieving improvements in performance, reliability, and cost over conventional approaches. Distributed control techniques are developed for both current sharing and ripple cancellation in cellular converter architectures. New current-sharing techniques for paralleled converters, which do not require the use of additional interconnections among converters to communicate current-sharing information, are developed and experimentally verified. Distributed ripple cancellation techniques are investigated and experimentally verified which do not require centralized control, automatically accommodate varying numbers of converter cells, and are highly tolerant of subsystem failures. The thesis also investigates the design of power stage topologies for cellular converters, and explores both an inverter topology and a rectifier topology which are well suited to the cellular architecture. Finally, the thesis describes the design, implementation, and experimental evaluation of a six-cell, six-kilowatt cellular rectifier system. This system implements both distributed load sharing and distributed ripple cancellation, and achieves performance levels unattainable with an equivalent single converter.

The thesis is divided into nine chapters, including this concluding chapter. Chapter 1 presents background and motivations, and provides a baseline assessment of the benefits of the cellular architecture. Chapter 2 introduces a new current-sharing approach for paralleled power converters which is based on frequency encoding of the current-sharing information. This approach has several advantages, including the ability to allow transformer isolation or elimination of current-sharing control connections.

Chapters 3 and 4 each present the design, implementation and experimental evaluation of current-sharing methods based on the frequency encoding approach introduced in Chapter 2. In the method developed in Chapter 3, current sharing information is encoded on small perturbations in output current, while in the method of Chapter 4, the cell switching ripple itself carries the current-sharing information. In each case, a three-cell prototype system implementing the method is developed and evaluated. The results of these chapters demonstrate that accurate and stable load sharing is obtainable over a wide load

range without the use of intercell connections for communicating current-sharing information.

Chapter 5 addresses the dynamic analysis of systems employing nonlinear current-sharing control techniques. The ability to predict current-sharing and output dynamics is an important part of cellular converter design. The first part of the chapter analyzes nonlinear current-sharing control techniques which are linearizable about a constant operating point. To validate the analysis, it is applied to the current-sharing control scheme developed in chapter 3 and compared to experimental results. The second part of the chapter analyzes the dynamics of the widely-used UC3907 control scheme for an important special case. This analysis, which is applicable to the prototype converter system developed in Chapter 8, is also validated against experimental results.

Chapter 6 investigates ripple cancellation techniques which are well suited to a cellular architecture. The first part of the chapter analytically quantifies the amount of passive ripple cancellation that occurs among independently clocked cells in a parallel converter system. The second part of the chapter develops a distributed implementation of the interleaving method of ripple cancellation. Experimental results from a three-cell prototype system are used to corroborate the analytical predictions of the first part of the chapter, and to demonstrate the benefits of the distributed interleaving approach.

Chapter 7 discusses some of the key considerations in the design of cellular converter systems. The chapter also presents a new cellular inverter implementation which addresses these design issues. It is shown that the architecture mitigates some of the major drawbacks of the single resonant pole inverter (RPI), on which it is based. Furthermore, the chapter presents an enhanced control algorithm which significantly reduces stresses and losses for many operating conditions, and is applicable to both the RPI and the parallel architecture.

Chapter 8 presents the development and evaluation of a six-cell, six-kilowatt cellular rectifier system. The first part of the chapter describes conventional approaches to high-power-factor rectification and limitations associated with them. The second part of the chapter analyzes the benefits that can be achieved through the use of a cellular architecture, and presents the design of the prototype cellular converter system. The final part of the chapter presents an experimental evaluation of the prototype cellular converter system. It is shown that the prototype system behaves as predicted, and achieves performance levels unattainable with an equivalent single converter.

9.2 Thesis Conclusions

There are three main conclusions that can be drawn from this thesis. The first is that distributed load-sharing control can be implemented in a parallel converter system without requiring additional

interconnections among cells or heavy load regulation. Through the use of frequency encoding, current-sharing information can be communicated directly over the input or output bus of the converter system. This is desirable in many applications, especially those in which high reliability is sought.

The second conclusion that can be drawn from this thesis is that distributed ripple cancellation techniques are both feasible and effective. Passive ripple cancellation provides an $N^{1/2}$ reduction in rms input and output ripple as compared to a single large converter, and is useful for reducing filter stresses. Active interleaving using entirely distributed control is also possible, and yields tremendous performance improvements over a single converter implementation.

The final conclusion that can be drawn from this thesis is that, while there are significant design challenges, the cellular architecture is a viable approach for the construction of large converter systems and should continue to be developed. Many of the disadvantages of the cellular conversion approach, including the need for added and replicated components, can be mitigated through proper design. This fact, coupled with the many advantages of the cellular approach, argue compellingly for its continued development.

9.3 Recommendations for Future Work

There are several directions in which the continued development of cellular converter architectures should proceed. The current-sharing methods developed in this thesis have been tested only in low-power environments. Validating these techniques at high power is a necessary next step in their development. One possibility is to implement these techniques on the prototype converter system developed in chapter 8. The development of alternative methods of encoding and decoding the current-sharing information, or alternative implementations of the existing methods, is also a worthwhile endeavor.

An important related area is that of the dynamics and control of cellular converter systems. Some baseline techniques for analyzing the dynamics of cellular converter systems have been developed here and in the literature. However, many challenges remain, including the development of large signal analysis and control design methodologies, and the development of techniques well suited to handling systems with large numbers of (perhaps physically-dispersed) cells.

Further development of active ripple-cancellation techniques is also worthwhile. Other implementations of the distributed interleaving approach developed here should be investigated, especially those which can handle more cells. Furthermore, it may be possible to develop active ripple cancellation techniques which do not require additional interconnections among cells. One approach for

achieving this, for example, may be to use feedback control at frequencies on the order of the cell switching frequency.

Future work should also be directed at establishing the cost benefits and limitations of the cellular architecture. While this thesis has focussed on mitigating the disadvantages of the cellular design approach while capitalizing on its benefits, a detailed investigation of the economics of the approach has yet to be undertaken. In addition, a careful study of the cell manufacturing process is warranted, including investigation of alternative manufacturing technologies. This may yield insights as to how to best take advantage of the cellular design approach.

Finally, development of cellular converters for some specific industrial and/or commercial applications should be undertaken. This would allow direct performance and cost comparisons to be made with existing solutions, and would provide the most realistic framework possible for the assessment of the cellular design approach.

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Appendix A

This appendix presents the methods used to predict the power dissipation in the inductors and semiconductor devices in the design of the boost rectifier of Chapter 8. Matlab code implementing these computations can be found in Appendix B.

Predictions of inductor power dissipation were broken down into predictions of core losses and winding losses. Core losses were predicted by approximating the current ripple as a sinusoid (of the same peak value as the ripple) and using an empirical model provided by Ferroxcube/Philips [76]. This model predicts the core loss to be:

$$P_{core} \approx 9.16\times10^{-13}\cdot(f_{sw})^{1.231}\cdot(0.5B_{pk})^{2.793}\cdot V_{core} \qquad \textbf{(A.1)}$$

where the switching frequency is in kilohertz, the peak flux density is in Gauss, and the core volume is in cubic centimeters. Winding loss predictions were made using the model presented in [77] (also used in [8]), which includes both skin and proximity effects. First, the spectrum of the inductor current waveform was computed at the worst-case (low line, max power) operating point of the converter. Next, an equivalent ac resistance was computed for each switching harmonic group. The winding losses were computed as the sum of the I^2R_{ac} losses for each frequency component in the spectrum.

Equivalent ac resistances can be computed as follows [77]: The skin depth for the n^{th} harmonic grouping is calculated as

$$\delta_n = \sqrt{\frac{2\rho_{Cu}}{2\pi n f_{sw}\mu_{Cu}}} \qquad \textbf{(A.2)}$$

where ρ_{Cu} and μ_{Cu} are the resistivity and permeability of copper. The equivalent square-wire thickness of the winding is computed as:

$$h_{eff} = \left(\frac{\pi}{4}\right)^{3/4}\cdot\frac{d^{3/2}}{l^{1/2}} \qquad \textbf{(A.3)}$$

where d is the (uninsulated) wire diameter, and l is the spacing between wires. Using these, the wire height in skin depths for the n^{th} switching harmonic group is

$$X_n = \frac{h_{eff}}{\delta_n} \qquad \textbf{(A.4)}$$

and ac resistance is computed via

$$M_n = \Re e\left\{ \frac{(X_n + jX_n)\cosh(X_n + jX_n)}{\sinh(X_n + jX_n)} \right\}$$

$$D_n = \Re e\left\{ \frac{2(X_n + jX_n)\sinh(\frac{1}{2}(X_n + jX_n))}{\cosh(\frac{1}{2}(X_n + jX_n))} \right\} \qquad \text{(A.5)}$$

$$R_{ac,n} = \left[M_n + \frac{(m^2-1)}{3} D_n \right] \cdot R_{dc}$$

where m is the number of layers of turns, and R_{dc} is the dc resistance of the winding. Inductor losses were computed as the sum of the core and winding losses. Core temperature rise was computed using thermal resistance data provided for the cores by Ferroxcube.

Semiconductor losses were predicted as the sum of conduction losses and switching losses. (Because all the diodes exhibit a relatively soft turn off, switching losses were only computed for the active devices.) Conduction losses for each device are computed using constant drop plus resistance models, with the average and rms device currents computed numerically via simulation and cross-checked against the analytical models of [68]. The switching loss computations for the active (MOSFET) switch are based on models presented in [78,7], and have been broken down into turn-on and turn-off losses. The turn-on losses are due to the discharge of the nonlinear capacitances of the MOSFET gate-drain junction and drain-source junction and the charging of the boost diode junction capacitance (the two boost diodes and the snubber diode are lumped together as a single diode for simplicity). Assuming the nonlinear junction capacitances have the characteristic

$$C_x(V) = \frac{K_x}{\sqrt{V}} \qquad \text{(A.6)}$$

where the values K_x can be determined from the data sheets, we find a turn-on loss for the MOSFET of

$$E_{on} = \frac{2}{3}[2K_{diode} + K_{gd} + K_{ds}](V_o)^{3/2} \quad . \qquad \text{(A.7)}$$

The dominant switching loss component is the turn-off loss, which depends on the peak current to be turned off and the gate drive characteristics. (Throughout this analysis, we assume a current-limited gate drive of peak value i_{drive}.) As illustrated in Fig. A.1, we break the turn off process into three intervals. In the first interval $[t_a, t_b]$, the gate-source voltage is reduced from the gate drive "high" voltage down

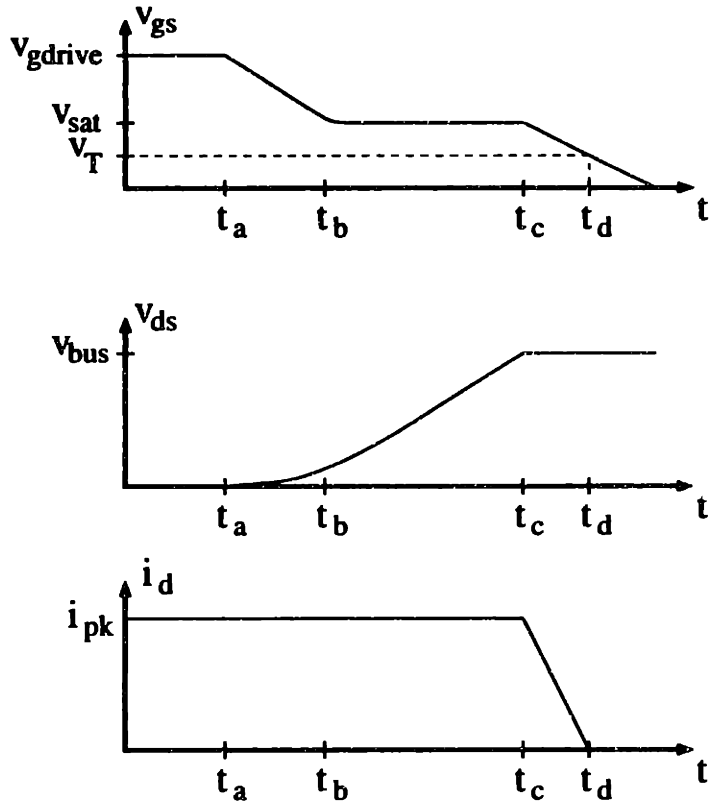

Figure A.1 Theoretical waveforms for the turn-off transition of a MOSFET.

to the saturation voltage, V_{sat}, which is that voltage exactly needed carry the drain current. The saturation voltage can be computed as

$$V_{sat} = \frac{I_{pk}}{g_{fs}} + V_T \quad . \tag{A.8}$$

During this delay period, there is no change in drain voltage or current, and hence no loss. In the second interval $[t_b, t_c]$, the gate-source voltage remains constant, and the (gate-drain) Miller capacitance, Q_m, is discharged via the gate. The length of this time period can be computed as

$$t_{cb} = \frac{2K_{gd}\sqrt{V_o}}{i_{drive}} \tag{A.9}$$

during which the drain current is constant and the drain voltage rises as

$$v_{ds}(t) = \left[\frac{i_{drive}(t - t_b)}{2K_{gd}}\right]^2 \quad for \quad t_b < t < t_c \quad .$$

and the dissipation is

$$E_{cb} = \frac{2 i_{pk} K_{gd}}{i_{drive}} \cdot (V_o)^{3/2} \quad .$$

The remaining time period $[t_c, t_d]$ is that required to reduce the gate-source voltage from the saturation voltage down to the threshold voltage V_T. As described in [8], during this time period the turn-off gate current rings up to its peak value (commutating current into source leakage inductance L_s), after which there is a constant-current discharge of the gate-source capacitance. During both of the final discharge period, we assume a linear fall of the drain current to zero. Accounting both for the commutation and constant current times, we can calculate the remaining turn-off time period as

$$\begin{aligned} t_2 &= \sqrt{L_s C_{gs}}\, asin\left(\frac{i_{drive}}{V_{sat}} \sqrt{\frac{L_s}{C_{gs}}} \right) \\ t_{dc} &= t_2 + \frac{C_{gs}(V_{sat}\cos(t_2/\sqrt{L_s C_{gs}}) - V_T)}{i_{drive}} \end{aligned} \qquad \textbf{(A.12)}$$

and the loss in this period as

$$E_{dc} = \tfrac{1}{2} t_{dc} V_o i_{pk} \quad . \qquad \textbf{(A.13)}$$

The total energy loss times the switching frequency gives the switching losses.

Appendix B

This appendix contains the Matlab routines used for analysis and design of three-phase single-switch boost rectifiers. The functions and scripts used for this purpose are as follows:

BRSIMCYC Simulates a three-phase single-switch boost rectifier cycle. Assumes the time vector is within [-pi/(6w),pi/(6w)). Returns the state trajectory over the cycle at the specified data point spacing.

BRSIMPI3 Simulate a three-phase single-switch boost rectifier over a pi/3 line cycle seqment (-pi/6 <= wt < pi/6).

BRAVGPI2 Calculates the local average line current in one phase (ir) of a three-phase single-switch boost rectifier over a pi/2 line cycle seqment (0 <= wt < pi/2).

BRSILH Simulation-based calculation of the input line harmonics of the three-phase single-switch boost rectifier. (For interleaved converters, see BRSISS and BRSISH.)

BRAILH Averaged model-based calculation of the input line harmonics of the 3-phase single-switch boost rectifier.

BRSISR Simulation-based calculation of the input switching ripple magnitude (for the r phase) from one or more interleaved, 3-phase, single-switch boost rectifiers at a specified point in the line cycle.

BRSISS Simulation-based calculation of the input switching spectrum of one or more interleaved, three-phase, single-switch boost rectifiers. All harmonics of the line frequency are calculated (including switching-frequency components) out to the nyquist limit using an FFT approach. (Also see BRSISH.)

BRSISH — Simulation-based calculation of the specified input harmonics of one or more interleaved, three-phase, single-switch boost rectifiers. The specified line frequency harmonics (including switching frequency components) are calculated using a straightforward DFT approach. (Also see BRSISS.)

BRCALIS1 — This is a routine for calculating the (normalized) input current spectrum for a set of interleaved 3 phase single-switch boost rectifiers across a space of operating points (values of d). The worst-case spectral components are identified across d. It is geared towards identifying what values of nominal boost ratio yield the best conducted EMI spectrum. Hence, the input inductance selected is a function of the boost ratio, and changes for different boost ratios.

BRCALIR1 — This is a routine for calculating the (normalized) input current ripple for a set of interleaved 3 phase single-switch boost rectifiers across a space of operating points (values of d). The routine is geared towards identifying what values of nominal boost ratio yield the best ripple. Hence, the input inductance selected is a function of the boost ratio, and changes for different boost ratios.

BRCALIS2 — This is a routine for calculating the (normalized) input current spectrum for a set of interleaved 3 phase single-switch boost rectifiers across a space of operating points (values of d and Vn). The routine is geared towards identifying the worst-case input spectral components over the expected range of input voltage and duty ratio for a specified design. (the duty ratio range for a Vn is set by the max output power Pomax.) This information can be used for design of the input EMI filter.

RUNIS1 — This script is used for examining the effects of varying M and Nint on the input current spectral components, using the BRCALIS1 routine. The routine sweeps values of M and Nint and saves the worst-case harmonic components over the range of d values used. For variations in M and Nint, the total power and energy storage of the converter system is held constant.

RUNIR1A — A script for running BRCALIR1 to get normalized ripple data as M is varied.

RUNIS2 A script for running BRCALIS2 to examine the effects for varying input line voltage on the input current spectrum.

BR_IPT This is a routine for comparing the use of 2 input inductors vs. a combination of an input inductor and an interphase transformer for interleaving two 3-phase single-switch boost rectifiers. The currents in the magnetic elements are calculated across a space of operating points (values of d) for a specified nominal boost ratio and max operating power. The input inductance selected is a function of the boost ratio, and changes for different boost ratios.

BRDVSVN This script (BRDvsVn) is used to examine the relationship between d and output power as Vn varies over a range and vo and L are held constant. This is important for dealing with input supply voltage variations.

BRDDISS Simulation-based calculation of the semiconductor device dissipation of the 3-phase single-switch boost rectifier. The converter is simulated (using BRSIMPI3) over a pi/3 interval and symmetry is used to reconstruct an input current waveform over a full cycle. Average and RMS current values for the devices are calculated numerically from the simulated waveforms (some of the results are cross-checked using averaged models). Conduction losses are then calculated using "drop plus resistance" models. Switching losses for the MOSFET are calculated using the simulation waveforms coupled with analytical models for the turn-on and turn-off losses at each switching point (using BRSWLOSS).

BRSWLOSS This routine is for calculating the switching energy loss for the boost rectifier MOSFET during one switching cycle, and is mainly used by the Matlab routine BRDDISS.

BRLDES This script is used to design the input inductors for the boost rectifier. Given the operational parameters of the boost inductor, the script generates feasable designs for the inductor based on core and wire data in the script BRLDAT.

BRLDAT This script BRLdat.m defines variables containing data for boost-rectifer inductor

design. Params for Phillips (Ferroxcube) 3F3 material ferrite square cores are defined, as is some wire table data for various guages.

IEC555 This is a script for checking against the IEC 555-2 harmonic limits using the BRAILH routine.

BRCL1 This script (BRCL1) is used to look at the averaged (load) step response of the s.s. boost rectifier under proportional duty ratio control. An averaged "injected current" model is used for the converter.

The Matlab code is designed for Matlab 4.X, and is as follows:

```
function [ir,is,it,t,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
%
% BRSIMCYC       Simulate a three-phase single-switch boost rectifier
%                cycle.  Assumes the time vector is within
%                [-pi/(6w),pi/(6w)). Returns the state trajectory over
%                the cycle at the specified data point spacing.
%                   Ver 3.0 - returns switch state data also
%                           - handles all states for -pi/6 < wt < pi/6
%
%        [ir,is,it,t,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
%           L     input boost inductor value, Henries
%           vo    output voltage, volts
%           Vn    peak line to neutral input voltage
%           w     line frequency, rad/sec
%           Tsw   switching period, sec
%           ton    switch on time, sec
%           ppc   number of time points per cycle to return.  1st
%                 point is turn-on time of switch.  Last point is
%                 before turn on of switch for the next cycle.
%           itran itran is a current level used to determine the
%                 accuracy of detection of switch state transitions.
%                 The transition boundary is considered to be reached
%                 when the magnitude of the current going to zero
%                 (causing the transition) is less than itran.
%           t0    start time of cycle, in sec. The start time should be
%                 in [-pi/(6w),pi/(6w)), and should be picked so that the
%                 entire cycle falls either in [-pi/6,0) or [0,pi/6).  This
%                 simplifies determining whether is or it goes to zero first.
%

           % set the time step, and calc constants
dt = Tsw/ppc;
K1 = Vn/(1.732051*w*L);
K2 = vo/(3*L);
K3 = (1.73205*Vn)/(2*w*L);
K4 = vo/(2*L);

           % set up initial response vectors
t = t0:dt:(t0+(ppc-1)*dt);
if w*t(length(t)) >= pi/6,
  error('Error in BRSIMCYC: time vector exceeds pi/(6*w)');
end;

ir = zeros(size(t));
is = ir;
it = is;
state = 5*ones(size(t));
           % simulate State 1 condition (switch on) for all response
           % points where the switch is on
onpts = floor(ton/dt)+1;
tempvec = ( sin( w*t(1:onpts)+(pi/6)*ones(1,onpts) ) + sin( w*t(1:onpts)-(pi/6)*ones(1,onpts) )
);
tempvec = tempvec - ( sin((w*t0+pi/6)*ones(1,onpts) ) + sin( (w*t0-pi/6)*ones(1,onpts) ) );
```

```
ir(1:onpts) = K1*tempvec;
tempvec = ( sin( w*t(1:onpts)-(5*pi/6)*ones(1,onpts) ) + sin( w*t(1:onpts)-(pi/2)*ones(1,onpts)
) );
tempvec = tempvec - ( sin( (w*t0-5*pi/6)*ones(1,onpts) ) + sin( (w*t0-pi/2)*ones(1,onpts) ) );
is(1:onpts) = K1*tempvec;
it(1:onpts) = -is(1:onpts)-ir(1:onpts);
state(1:onpts) = ones(1,onpts);
index = onpts+1;

          % calculate step to end of state 1 (switch-on time)
cur_t = t0+ton;
cur_ir = K1*( sin(w*cur_t+pi/6)-sin(w*t0+pi/6)+sin(w*cur_t-pi/6)-sin(w*t0-pi/6) );
cur_is = K1*( sin(w*cur_t-5*pi/6)-sin(w*t0-5*pi/6)+sin(w*cur_t-pi/2)-sin(w*t0-pi/2) );
cur_it = -cur_ir-cur_is;
findtransition = 0;  % currently calculating time points

while findtransition ~= 1,
          % calculate next saved time point in state 2
  dt = t(index) - cur_t;
  pred_t = cur_t+dt;
   pred_ir = cur_ir - 2*K2*(pred_t-cur_t) + K1*( sin(w*pred_t+pi/6) - sin(w*cur_t+pi/6) +
sin(w*pred_t-pi/6) - sin(w*cur_t-pi/6) );
   pred_is = cur_is + K2*(pred_t-cur_t) + K1*( sin(w*pred_t-5*pi/6) - sin(w*cur_t-5*pi/6) +
sin(w*pred_t-pi/2) - sin(w*cur_t-pi/2) );
  pred_it = -pred_ir-pred_is;

  if ((pred_is < 0) & (pred_it < 0)),
                       % predicted point is good. Keep it
    cur_t = pred_t;
    cur_ir = pred_ir;
    cur_is = pred_is;
    cur_it = pred_it;
    ir(index) = cur_ir;
    is(index) = cur_is;
    it(index) = cur_it;
    state(index) = 2;
    index = index + 1;
    if index >= ppc,
      index
      cur_ir
      cur_is
      cur_it
      t0
      error('Error in BRSIMCYC (state 2): Continuous Conduction Mode Encountered');
    end;
  else
    findtransition = 1;
                       % predicted point is not good.  Throw it away
                       % and set up flag to initiate location of state
                       % transition boundary
  end; % if pred_is, pred_it < 0
end; % while findtransition ~= 1

                       % locate transition boundary to state 3 or 4 within
                       % desired accuracy
if (t0 > 0),
       % We are looking for the end of state 2, and heading for state 3
       % since we are in 0 < wt < pi/6.
  while ( abs(cur_is) > itran),

            % we are still above the desired transition resolution
            % calculate next time point in state 2
    if (pred_is <= 0), % the point is valid for state 2. save it.
      cur_t = pred_t;
      cur_ir = pred_ir;
      cur_is = pred_is;
      cur_it = pred_it;
    else dt = min([0.95*dt, dt*(cur_is)/(cur_is-pred_is)]);

                          % interpolate to find new time step to use,
                          % with a maximum of 95% of the old step.
    end;

                       % calculate next point at specified time step
    pred_t = cur_t+dt;
     pred_ir = cur_ir - 2*K2*(pred_t-cur_t) + K1*( sin(w*pred_t+pi/6) - sin(w*cur_t+pi/6) +
sin(w*pred_t-pi/6) - sin(w*cur_t-pi/6) );
     pred_is = cur_is + K2*(pred_t-cur_t) + K1*( sin(w*pred_t-5*pi/6) - sin(w*cur_t-5*pi/6) +
sin(w*pred_t-pi/2) - sin(w*cur_t-pi/2) );
    pred_it = -pred_ir-pred_is;

  end; % while
                         % we are now close to the exact boundary.  Make
```

```
                        % approx that is approxeq 0, and ir approxeq -it.
                        % We are now effectively in state 3.

  findtransition = 0;  % currently calculating time points

  while findtransition ~= 1,
            % calculate next saved time point in state 3
    dt = t(index) - cur_t;
    pred_t = cur_t+dt;
    pred_ir = cur_ir - K4*(pred_t-cur_t) + K3*( sin(w*pred_t-pi/6) - sin(w*cur_t-pi/6) );
    pred_is = 0;
    pred_it = -pred_ir-pred_is;

    if (pred_ir > 0),
                        % predicted point is good. Keep it
      cur_t = pred_t;
      cur_ir = pred_ir;
      cur_is = pred_is;
      cur_it = pred_it;
      ir(index) = cur_ir;
      is(index) = cur_is;
      it(index) = cur_it;
      state(index) = 3;
      index = index +1;
      if index >= ppc,
        error('Error in BRSIMCYC (state 3): Continuous Conduction Mode Entered');
      end;
    else
      findtransition = 1;
                        % predicted point is not good.  Throw it away
                        % and set up flag to indicate that remaining time
                        % points that are saved are in state 5.
    end; % if pred_ir > 0
  end; % while findtransition ~= 1
else
       % we are looking for the end of state 2, and will transition to
       % state 4, since we must be in -pi/6 < wt < 0.
  while ( abs(cur_it) > itran),

            % we are still above the desired transition resolution
            % calculate next time point in state 2
    if (pred_it <= 0), % the point is valid for state 2. save it.
      cur_t = pred_t;
      cur_ir = pred_ir;
      cur_is = pred_is;
      cur_it = pred_it;
    else dt = min([0.95*dt, dt*(cur_it)/(cur_it-pred_it)]);
                    % interpolate to find new time step to use,
                    % with a maximum of 95% of the old step.
    end;

                     % calculate next point at specified time step
    pred_t = cur_t+dt;
     pred_ir = cur_ir - 2*K2*(pred_t-cur_t) + K1*( sin(w*pred_t+pi/6) - sin(w*cur_t+pi/6) +
sin(w*pred_t-pi/6) - sin(w*cur_t-pi/6) );
     pred_is = cur_is + K2*(pred_t-cur_t) + K1*( sin(w*pred_t-5*pi/6) - sin(w*cur_t-5*pi/6) +
sin(w*pred_t-pi/2) - sin(w*cur_t-pi/2) );
    pred_it = -pred_ir-pred_is;

 end; % while
                        % we are now close to the exact boundary.  Make
                        % approx that it approxeq 0, and ir approxeq -is.
                        % We are now effectively in state 4.

  findtransition = 0;  % currently calculating time points

  while findtransition ~= 1,
            % calculate next saved time point in state 4
    dt = t(index) - cur_t;
    pred_t = cur_t+dt;
    pred_ir = cur_ir - K4*(pred_t-cur_t) + K3*( sin(w*pred_t+pi/6) - sin(w*cur_t+pi/6) );
    pred_is = -pred_ir;
    pred_it = 0;

    if (pred_ir > 0),
                        % predicted point is good. Keep it
      cur_t = pred_t;
      cur_ir = pred_ir;
      cur_is = pred_is;
      cur_it = pred_it;
      ir(index) = cur_ir;
      is(index) = cur_is;
      it(index) = cur_it;
```

```
      state(index) = 4;
      index = index +1;
      if index >= ppc,
        error('Error in BRSIMCYC (state 4): Continuous Conduction Mode Entered');
      end;
    else
      findtransition = 1;
                        % predicted point is not good.  Throw it away
                        % and set up flag to indicate that remaining time
                        % points that are saved are in state 5.
    end; % if pred_ir > 0
  end; % while findtransition ~= 1
end; % if (t0 >0) (do states 2&3) else (do states 2&4)
                      % the remainder of the points in this cycle are
                      % in state 5, and all the currents have been preset
                      % to zero.  Therefore, we are effectively finished.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [ir,is,it,t,state] = brsimpi3(L,vo,Vn,w,Tsw,ton,ppc,itran);
%
% BRSIMPI3      Simulate a three-phase single-switch boost rectifier
%               over a pi/3 line cycle segment (-pi/6 <= wt < pi/6).
%               Returns the state trajectory over the time period at
%               the specified data point spacing.
%               The function BRSIMCYC is used to calculate the tra-
%               jectories within individual switching periods.
%
%    [ir,is,it,t,state] = brsimpi3(L,vo,Vn,w,Tsw,ton,ppc,itran);
%       L     Input boost inductor value, Henries.
%       vo    Output voltage, volts.
%       Vn    Peak line to neutral input voltage.
%       w     Line frequency, rad/sec.
%       Tsw   Switching period, sec. The switching period should be
%             chosen such that the line period is an integer
%             multiple of twelve times the switching period, to allow
%             an exact integer number of cycles to be simulated in both
%             the [-pi/6,0) and [0,pi/6) intervals.
%       ton   Switch on time in a cycle, sec.
%       ppc   Number of time points per switching cycle to use.  The
%             total number of points returned is this times 1/6
%             times the ratio of the line period to switching period.
%       itran The current level used to determine the accuracy of
%             locating switch state transitions (amps).  Transition
%             boundaries are considered reached when the magnitude of
%             the current going to zero to cause the transition is
%

               % check to make sure the integer frequency relation
               % between the line and switching freqs. is met.
Msc = (2*pi/w)/(12*Tsw); % # of switch cycles in pi/6 of line.
if (Msc ~= round(Msc)),
   error('Error in BRSIMPI3:  fsw/(12*fline) must be an integer.');
end;
               % set up return vectors and initialize vars.
t = zeros(1,2*Msc*ppc);
ir = t;
is = ir;
it = is;
state = it;
               % time points for the start of each cycle to simulate
               % wt in [-pi/6,pi/6)
t0 = -(Msc*Tsw):Tsw:(Msc*Tsw - Tsw/ppc);

               % loop through cycle simulations
for index = 1:2*Msc,
  [ircyc,iscyc,itcyc,tcyc,statecyc] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0(index));
  ir(((index-1)*ppc+1):(index*ppc)) = ircyc;
  is(((index-1)*ppc+1):(index*ppc)) = iscyc;
  it(((index-1)*ppc+1):(index*ppc)) = itcyc;
  t(((index-1)*ppc+1):(index*ppc)) = tcyc;
  state(((index-1)*ppc+1):(index*ppc)) = statecyc;
end;

               % We are now finished

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [ir,t] = bravgpi2(L,vo,Vn,w,Tsw,ton);
```

```
%
% BRAVGPI2      Calculates the local average line current in one phase (ir)
%               of a three-phase single-switch boost rectifier
%               over a pi/2 line cycle segment (0 <= wt < pi/2).
%               The local average current is returned at a spacing of
%               one point per switching cycle over the time period.  The
%               Averaged model equations of Kolar, et. al. (PESC 93 pp
%               696-703) are used to make the calculations.
%
%    [ir,t] = bravgpi2(L,vo,Vn,w,Tsw,ton);
%       L     Input boost inductor value, Henries.
%       vo    Output voltage, volts.
%       Vn    Peak line to neutral input voltage.
%       w     Line frequency, rad/sec.
%       Tsw   Switching period, sec. The switching period should be
%             chosen such that the line period is an integer
%             multiple of 12 times the switching period, to allow
%             an exact integer number of cycles to be calculated in a
%             pi/6 interval.
%       ton   Switch on time in a cycle, sec.


Dp = ton/Tsw;               % duty ratio of switch
M = vo/(sqrt(3)*Vn);        % voltage transfer ratio at peak line voltage
Msc = (2*pi/w)/(12*Tsw);  % Msc is # of points (switching cycles) in pi/6

                            % check for integer # points in pi/6
if Msc ~= round(Msc),
  error('Error in BRAVGPI2: fsw/(12*fline) must be an integer');
end;

t = 0:Tsw:(3*Msc-1)*Tsw;
ir = zeros(size(t));
one = ones(1,Msc);
pid6 = (pi/6)*ones;
rt3 = sqrt(3);
                        % calculate normalized ir for wt in [0,pi/6)
wt = w*t(1:Msc);
ir(1:Msc) = cos(wt) - (2/M)*cos(wt).*cos(wt + pid6) + rt3*one/(2*M);
ir(1:Msc) = ir(1:Msc) ./ (one + (rt3/M)*sin(wt - pid6));
ir(1:Msc) = (rt3*Dp*Dp/(4*M))*(ir(1:Msc) ./ (one - cos(wt - pid6)/M));

                        % calculate normalized ir for wt in [pi/6,pi/3)
wt = w*t(Msc+1:2*Msc);
ir(Msc+1:2*Msc) = cos(wt) + cos(2*wt + pid6)/(2*M);
ir(Msc+1:2*Msc) = ir(Msc+1:2*Msc) ./ (one - rt3*sin(wt - pid6)/M);
ir(Msc+1:2*Msc) = ir(Msc+1:2*Msc) ./ (one - cos(wt - pid6)/M);
ir(Msc+1:2*Msc) = (rt3*Dp*Dp/(4*M))*ir(Msc+1:2*Msc);

                        % calculate normalized ir for wt in [pi/3,pi/2)
wt = w*t(2*Msc+1:3*Msc);
ir(2*Msc+1:3*Msc) = (rt3*Dp*Dp/(4*M)) * cos(wt) ./ (one - rt3*cos(wt)/M);

                        % apply base quantity to unnormalize
ir = ir*2*vo*Tsw/(3*L);

                        % we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [ilhmag, ilhphi] = brsilh(L,vo,Vn,w,Tsw,ton,harmnums);
%
% BRSILH        Simulation-based calculation of the input line harmonics
%               of the three-phase single-switch boost rectifier.  The
%               converter is simulated (using BRSIMPI3) over a pi/3 inter-
%               val, and symmetry is used to reconstruct an input current
%               waveform over a full cycle.  The specified line harmonics
%               are calculated using a straightforward DFT approach.
%
%    [ilhmag ilhphi] = brsilh(L,vo,Vn,w,T,ton,harmnums);
%      ilhmag     Vector of magnitudes of the specified harmonics, in amps.
%      ilhphi     Vector of phases of the specified harmonics, in rad/sec.
%      L          Input boost inductor value, Henries.
%      vo         Output voltage, Volts.
%      Vn         Peak line to neutral input voltage, Volts.
%      w          Line frequency, rad/sec.
%      Tsw        Switching period, sec.
%      ton        Switch on time, sec.
%      harmnums   vector containing list of harmonic numbers to compute.
%
```

```
Msc = 2*pi/(12*w*Tsw) % Msc is # of  witch cycles in pi/6 of line

ppc = 120       % many points per cycle for accuracy
itran = 0.001    % small transition current threshold for high accuracy

                        % simulate over pi/3 line span
[ir, is, it, t, state] = brsimpi3(L,vo,Vn,w,Tsw,ton,ppc,itran);

                        % calculate ir over full line cycle from
                        % available data and symmetry properties
ir_lcyc = zeros(1,(12*Msc*ppc));
ir_lcyc(1:2*Msc*ppc) = ir;
ir_lcyc(2*Msc*ppc+1:4*Msc*ppc) = -1*is;
ir_lcyc(4*Msc*ppc+1:6*Msc*ppc) = it;
ir_lcyc(6*Msc*ppc+1:8*Msc*ppc) = -1*ir;
ir_lcyc(8*Msc*ppc+1:10*Msc*ppc) = is;
ir_lcyc(10*Msc*ppc+1:12*Msc*ppc) = -1*it;

                        % generate time vector over a line cycle
                        % starting at wt = -pi/6.
t_lcyc = 0:(Tsw/ppc):((12*Msc*ppc-1)*(Tsw/ppc));
t_lcyc = t_lcyc - pi/(6*w)*ones(size(t_lcyc));

                        % calculate input line harmonic
                        % component magnitudes using a DFT approach
K = 12*Msc*ppc; % total number of points in a cycle
dt = Tsw/ppc;   % time step between points
ilhmag = zeros(size(harmnums));
ilhphi = ilhmag;

                        % calc individual harmonics in a loop.
                        % A matrix computation would be faster
                        % but require more memory.
for n = 1:length(harmnums),
  disp(['BRSILH calculating harmonic number n = ',num2str(harmnums(n))]);
  wcos = cos(harmnums(n)*w*t_lcyc)';
  wsin = sin(harmnums(n)*w*t_lcyc)';
  an = (2/K)*ir_lcyc*wcos;
  bn = (2/K)*ir_lcyc*wsin;
                % nth harmonic is ilhmag(n)*cos(n*w*t + ilhphi(n))
  ilhmag(n) = sqrt(an*an + bn*bn);
  ilhphi(n) = atan2(-bn,an);
end;
                        % we are done

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [ilhmag, ilhphi] = brailh(L,vo,Vn,w,Tsw,ton,harmnums);
%
% BRAILH        Averaged model-based calculation of the input line
%               harmonics of the 3-phase single-switch boost rectifier.
%               The calculations of the time waveform over a pi/2 int-
%               erval are made using the routine BRAVGPI2, which uses
%               the analytical results of Kolar et. al. PESC 93,
%               pp. 696-703.  The specified line harmonics are calculated
%               using a straight-forward DFT approach.
%
%    [ilhmag ilhphi] = brailh(L,vo,Vn,w,T,ton,harmnums);
%      ilhmag     Vector of magnitudes of the specified harmonics, in amps.
%      ilhphi     Vector of phases of the specified harmonics, in rad/sec.
%      L          Input boost inductor value, Henries.
%      vo         Output voltage, Volts.
%      Vn         Peak line to neutral input voltage, Volts.
%      w          Line frequency, rad/sec.
%      Tsw        Switching period, sec.
%      ton        Switch on time, sec.
%      harmnums   vector containing list of harmonic numbers to compute.
%

Msc = 2*pi/(12*w*Tsw); % Msc is # of switch cycles in pi/6 of line

                        % simulate over pi/2 line span 0 < wt < pi/2
[ir, t] = bravgpi2(L,vo,Vn,w,Tsw,ton);

                        % calculate ir over full line cycle from
                        % available data and symmetry properties
ir_lcyc = zeros(1,(12*Msc));
ir_lcyc(1:3*Msc) = ir;
ir_lcyc(3*Msc+1) = 0;  % must be zero by symmetry
ir_lcyc(3*Msc+2:6*Msc+1) = -1*ir(3*Msc:-1:1);
```

```
ir_lcyc(6*Msc+1:12*Msc) = ir_lcyc(6*Msc+1:-1:2);

                        % generate time vector over a line cycle
                        % starting at wt = 0.
t_lcyc = 0:Tsw:((12*Msc-1)*Tsw);

                        % calculate input line harmonic
                        % component magnitudes using a DFT approach
K = 12*Msc; % total number of points in a cycle
dt = Tsw;   % time step between points
ilhmag = zeros(size(harmnums));
ilhphi = ilhmag;

                        % calc individual harmonics in a loop.
                        % A matrix computation would be faster
                        % but require more memory.
                        % Also, we are not using even symmetry info.

for n = 1:length(harmnums),
  disp(['BRAILH calculating harmonic number n = ',num2str(harmnums(n))]);
  wcos = cos(harmnums(n)*w*t_lcyc)';
  wsin = sin(harmnums(n)*w*t_lcyc)';
  an = (2/K)*ir_lcyc*wcos;
  bn = (2/K)*ir_lcyc*wsin;
                % nth harmonic is ilhmag(n)*cos(n*w*t + ilhphi(n))
  ilhmag(n) = sqrt(an*an + bn*bn);
  ilhphi(n) = atan2(-bn,an);
end;
                        % we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [i_net, pprip] = brsisr(L,vo,Vn,w,Tsw,ton,ppc,Nint,wt);
%
% BRSISR      Simulation-based calculation of the input switching ripple
%             magnitude for the r phase from one or more interleaved,
%             3-phase, single-switch boost rectifiers at a specified point
%             in the line cycle.  The ripple current from a single converter
%             at the specified point in the line cycle is calculated using
%             the BRSIMCYC routine.  If specified, the net waveform for a
%             number of converters operating out of phase is calculated.
%             The net interleaved time waveform is returned, along with the
%             peak-to-peak ripple.
%
%    [i_net, pprip] = brsisr(L,vo,Vn,w,Tsw,ton,ppc,Nint,wt);
%      i_net      Net input current (time) waveform of interleaved
%                 converters over a switching cycle for the r phase at
%                 the specified point in the line cycle (wt), in Amps.
%      pprip      Peak-to-peak input current ripple of interleaved con-
%                 verters at the specified point in the line cycle, in Amps.
%      L          Input boost inductor value (for each cell), Henries.
%      vo         Output voltage, Volts.
%      Vn         Peak line to neutral input voltage, Volts.
%      w          Line frequency, rad/sec.
%      Tsw        Switching period, sec.  The switching period should be
%                 chosen so there is an integral number of cycles in pi/6
%                 of the line period.
%      ton        Switch on time, sec.
%      ppc        Number of points to use for the switching cycle.  This
%                 number must be a multiple of Nint, to allow exact inter-
%                 leaving, and should be large to allow accurate calculation
%                 of the peak to peak ripple.
%      Nint       Number of converters interleaved ( =1 for one converter).
%      wt         Specified point in the line cycle to calculate the r-phase
%                 input ripple, in rad/sec.  Must be in the range [0,2*pi).

Msc = 2*pi/(12*w*Tsw); % Msc is # of switch cycles in pi/6 of line
itran = 0.001;    % small transition current threshold for high accuracy

                % warn user to use more points for accuracy
if ppc/Nint < 100,
  disp('BRSISR warning: More points per cycle are advisable for accurate ripple calculation');
end;

                % adjust simulation time to be in the -pi/6..pi/6 range
                % allowed by brsimcyc.  Then calculate correct wave-
                % form from symmetry considerations
if ((0 <= wt) & (wt < pi/6)),
  t0 = wt/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = irp;
```

```
elseif ((pi/6 <= wt) & (wt < pi/2)),
  t0 = (wt - pi/3)/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = -1*isp;
elseif ((pi/2 <= wt) & (wt < 5*pi/6)),
  t0 = (wt - 2*pi/3)/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = itp;
elseif (( 5*pi/6 <= wt) & (wt < 7*pi/6)),
  t0 = (wt - pi)/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = -1*irp;
elseif (( 7*pi/6 <= wt) & (wt < 3*pi/2)),
  t0 = (wt - 4*pi/3)/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = isp;
elseif (( 3*pi/2 <= wt) & (wt < 11*pi/6)),
  t0 = (wt - 5*pi/3)/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = -1*itp;
elseif ((11*pi/6 < wt) & (wt < 2*pi)),
  t0 = (wt - 2*pi)/w;
  [irp,isp,itp,tp,state] = brsimcyc(L,vo,Vn,w,Tsw,ton,ppc,itran,t0);
  ir = irp;
else
  error('Error in BRSISR: wt must be in [0,2*pi)');
end;

                        % If more than one converter interleaved,
                        % calculate sum of shifted waveforms.
                        % This approach assumes the waveforms do
                        % not change significantly for that amount
                        % of time shift.
i_net = ir;
dl = ppc/Nint;  % number of points to shift over to interleave
if dl ~= round(dl),
  error('Error in BRSISR: ppc must be a multiple of Nint.');
end;
len = length(i_net);
for k = 1:(Nint-1), % loop through and do shift and adds
  i_net(1:k*dl) = i_net(1:k*dl) + ir((len-k*dl+1):len);
  i_net(k*dl+1:len) = i_net(k*dl+1:len) + ir(1:len-k*dl);
end;

                        % calculate peak-to-peak ripple
pprip = max(i_net)-min(i_net);

                        % we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [i_lcyc, issmag, issphi] = brsiss(L,vo,Vn,w,Tsw,ton,ppc,Nint);
%
% BRSISS      Simulation-based calculation of the input switching spectrum
%             of one or more interleaved, three-phase, single-switch
%             boost rectifiers.  A single converter is simulated (using
%             BRSIMPI3) over a pi/3 interval, and symmetry is used to
%             reconstruct its input current waveform over a full cycle.
%             Shifted sums of this waveform are used to calculate the input
%             waveform if multiple converters are interleaved. The magnitudes
%             and phases of the harmonics of the periodic waveform are calc
%             ulated using an fft approach.  i(t) = sum over k of
%             (issmag(k)*cos((k-1)*w*t+issphi(k))).  The program calculates
%             for 1<= k <= ppc*pi/(w*Tsw)
%
%    [i_lcyc, issmag, issphi] = brsiss(L,vo,Vn,w,T,ton,ppc,Nint);
%      i_lcyc     net input current (time) waveform of interleaved
%                 converters over a full cycle (r phase, starting at
%                 wt = -pi/6).
%      issmag     Vector of magnitudes of the specified freqs., in amps.
%                 The kth element is for frequency (k-1)*w/(2*pi) and
%                 there are N=ppc*pi/(w*Tsw) points.
%      issphi     Vector of phases of the specified frequencies, in rad/sec.
%                 The kth element is for frequency (k-1)*w/(2*pi), and
%                 there are N=ppc*pi/(w*Tsw) points.
%      L          Input boost inductor value, Henries.
%      vo         Output voltage, Volts.
%      Vn         Peak line to neutral input voltage, Volts.
%      w          Line frequency, rad/sec.
%      Tsw        Switching period, sec.  The switching period should be
%                 chosen so there is an integral number of cycles in pi/6
```

```
%                   of the line period.
%       ton         Switch on time, sec.
%       ppc         Number of points to use per switching cycle.  This number
%                   must be large enough to allow accurate DFT calculation of
%                   the desired switching harmonics (say a factor of 10 over
%                   the maximum switching harmonic number to compute).  Also,
%                   ppc must be an integer multiple of Nint.
%       Nint        Number of converters interleaved ( =1 for one converter).
%       harmnums    Vector containing list of harmonic numbers to compute.

Msc = 2*pi/(12*w*Tsw); % Msc is # of switch cycles in pi/6 of line
itran = 0.001;     % small transition current threshold for high accuracy

                        % simulate over pi/3 line span
[ir, is, it, t, state] = brsimpi3(L,vo,Vn,w,Tsw,ton,ppc,itran);

                        % calculate ir over full line cycle from
                        % available data and symmetry properties
ir_lcyc = zeros(1,(12*Msc*ppc));
ir_lcyc(1:2*Msc*ppc) = ir;
ir_lcyc(2*Msc*ppc+1:4*Msc*ppc) = -1*is;
ir_lcyc(4*Msc*ppc+1:6*Msc*ppc) = it;
ir_lcyc(6*Msc*ppc+1:8*Msc*ppc) = -1*ir;
ir_lcyc(8*Msc*ppc+1:10*Msc*ppc) = is;
ir_lcyc(10*Msc*ppc+1:12*Msc*ppc) = -1*it;

                        % If more than one converter interleaved,
                        % calculate sum of shifted waveforms.
                        % This approach assumes the waveforms do
                        % not change significantly for that amount
                        % of time shift.
i_lcyc = ir_lcyc;
dl = ppc/Nint;  % number of points to shift over to interleave
if dl ~= round(dl),
  error('Error in BRSISS: ppc must be a multiple of Nint.');
end;
len = length(i_lcyc);
for k = 1:(Nint-1), % loop through and do shift and adds
  i_lcyc(1:k*dl) = i_lcyc(1:k*dl) + ir_lcyc((len-k*dl+1):len);
  i_lcyc(k*dl+1:len) = i_lcyc(k*dl+1:len) + ir_lcyc(1:len-k*dl);
end;
clear ir_lcyc;  % we no longer need this large variable

                        % generate time vector over a line cycle
                        % starting at wt = -pi/6.
t_lcyc = 0:(Tsw/ppc):((12*Msc*ppc-1)*(Tsw/ppc));
t_lcyc = t_lcyc - pi/(6*w)*ones(size(t_lcyc));

                        % calculate input line harmonic
                        % component magnitudes using an FFT approach
N = 12*Msc*ppc; % total number of points in a cycle
dt = Tsw/ppc;   % time step between points
                  % make start time be wt=0, not wt = -pi/6
IL = fft([i_lcyc(Msc*ppc+1:length(i_lcyc)),i_lcyc(1:Msc*ppc)]);
issmag = abs(IL(1:N/2))*2/N;
                        % include time shift to get correct phase
issphi = angle(IL(1:N/2));
                        % we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [i_lcyc, ishmag, ishphi] = brsish(L,vo,Vn,w,Tsw,ton,ppc,Nint,harmnums);
%
% BRSISH      Simulation-based calculation of the input harmonics
%             of one or more interleaved, three-phase, single-switch
%             boost rectifiers,including harmonics at and beyond the switching
%             frequency.  A single converter is simulated (using
%             BRSIMPI3) over a pi/3 interval, and symmetry is used to
%             reconstruct its input current waveform over a full cycle.
%             Shifted sums of this waveform are used to calculate the input
%             waveform if multiple converters are interleaved. The specified
%             switching harmonics are calculated using a DFT approach.
%
%    [i_lcyc, ishmag, ishphi] = brsish(L,vo,Vn,w,T,ton,ppc,Nint,harmnums);
%      i_lcyc     net input current (time) waveform of interleaved
%                 converters over a full cycle (r phase, starting at
%                 wt = -pi/6).
%      ishmag     Vector of magnitudes of the specified harmonics, in amps.
%      ishphi     Vector of phases of the specified harmonics, in rad/sec.
%      L          Input boost inductor value, Henries.
%      vo         Output voltage, Volts.
```

```
%       Vn          Peak line to neutral input voltage, Volts.
%       w           Line frequency, rad/sec.
%       Tsw         Switching period, sec.  The switching period should be
%                   chosen so there is an integral number of cycles in pi/6
%                   of the line period.
%       ton         Switch on time, sec.
%       ppc         Number of points to use per switching cycle.  This number
%                   must be large enough to allow accurate DFT calculation of
%                   the desired switching harmonics (say a factor of 10 over
%                   the maximum switching harmonic number to compute).  Also,
%                   ppc must be an integer multiple of Nint.
%       Nint        Number of converters interleaved ( =1 for one converter).
%       harmnums    Vector containing list of harmonic numbers to compute. These
%                   are harmonics of the LINE frequency (not the switching freq)
%                   since energy can be at any multiple of the line freq.

Msc = 2*pi/(12*w*Tsw); % Msc is # of switch cycles in pi/6 of line
itran = 0.001;     % small transition current threshold for high accuracy

                        % simulate over pi/3 line span
[ir, is, it, t, state] = brsimpi3(L,vo,Vn,w,Tsw,ton,ppc,itran);

                        % calculate ir over full line cycle from
                        % available data and symmetry properties
ir_lcyc = zeros(1,(12*Msc*ppc));
ir_lcyc(1:2*Msc*ppc) = ir;
ir_lcyc(2*Msc*ppc+1:4*Msc*ppc) = -1*is;
ir_lcyc(4*Msc*ppc+1:6*Msc*ppc) = it;
ir_lcyc(6*Msc*ppc+1:8*Msc*ppc) = -1*ir;
ir_lcyc(8*Msc*ppc+1:10*Msc*ppc) = is;
ir_lcyc(10*Msc*ppc+1:12*Msc*ppc) = -1*it;

                        % If more than one converter interleaved,
                        % calculate sum of shifted waveforms.
                        % This approach assumes the waveforms do
                        % not change significantly for that amount
                        % of time shift.
i_lcyc = ir_lcyc;
dl = ppc/Nint;  % number of points to shift over to interleave
if dl ~= round(dl),
  error('Error in BRSISH: ppc must be a multiple of Nint.');
end;
len = length(i_lcyc);
for k = 1:(Nint-1), % loop through and do shift and adds
  i_lcyc(1:k*dl) = i_lcyc(1:k*dl) + ir_lcyc((len-k*dl+1):len);
  i_lcyc(k*dl+1:len) = i_lcyc(k*dl+1:len) + ir_lcyc(1:len-k*dl);
end;

clear ir_lcyc;  % we no longer need this large variable

                        % generate time vector over a line cycle
                        % starting at wt = -pi/6.
t_lcyc = 0:(Tsw/ppc):((12*Msc*ppc-1)*(Tsw/ppc));
t_lcyc = t_lcyc - pi/(6*w)*ones(size(t_lcyc));

                        % calculate input line harmonic
                        % component magnitudes using a DFT approach
K = 12*Msc*ppc; % total number of points in a cycle
dt = Tsw/ppc;   % time step between points
ilhmag = zeros(size(harmnums));
ilhphi = ilhmag;

                        % calc individual harmonics in a loop.
                        % A matrix computation would be faster
                        % but require more memory.
for n = 1:length(harmnums),
  disp(['BRSISH calculating harmonic number n = ',num2str(harmnums(n))]);
  wcos = cos(harmnums(n)*w*t_lcyc)';
  wsin = sin(harmnums(n)*w*t_lcyc)';
  an = (2/K)*i_lcyc*wcos;
  bn = (2/K)*i_lcyc*wsin;
                % nth harmonic is ishmag(n)*cos(n*(2*Pi/Tsw)*t + ishphi(n))
  ishmag(n) = sqrt(an*an + bn*bn);
  ishphi(n) = atan2(-bn,an);
end;
                        % we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [ik,dvec,Lnorm] = BRCALIS1(M,pm,Nint,maxdfrac,numdsteps,fswmult);
%
```

```
%   [ik,dvec,Lnorm] = BRCALIS1(M,pm,Nint,maxdfrac,numdsteps,fswmult);
%
%                   THIS IS BRCALIS1 VERSION 2.0 !!!
% This is a routine for calculating the (normalized) input current
% spectrum for a set of interleaved 3 phase single-switch boost
% rectifiers across a space of operating points (values of d).  The
% routine is geared towards identifying what values of nominal boost
% ratio yield the best conducted EMI spectrum.  Hence, the input
% inductance selected is a function of the boost ratio, and changes
% for different boost ratios.
%
% The relavent parameters specified by the user include M (the
% boost ratio), pm (the ratio of the line frequency to the switching
% frequency), and Nint (the number of cells being interleaved).  The
% user also sets the fraction of the peak possible duty cycle to use
% as a maximum, the number of steps in duty cycle to calculate, and
% the multiple of the switching frequency to calculate out to.
%
% The results of the script are given in normalized form with
% Tsw and Vn = 1, and (total) Pout = 1 for the maximum specified
% duty cycle.  The user can calculate the currents for a system
% with real parameters (at the same M, pm, Nint, and d vals) by the
% following computation:
%           ireal = inorm*(Vn*Tsw*Lnorm/L) = inorm*(Pout/Vn)
% where Lnorm is the normalized input inductance selected by the
% routine (for each boost cell) to achieve a normalized total
% power of 1 at max d.  Lnorm is returned by the routine.  (Note
% that one must consider whether the input voltage or the output
% voltage is being held constant for comparison of normalized
% results for varying M.  For this version of the program (Ver 2)
% normalized results are directly comparable for the case where
% Vn is held constant and vo is varied with M.)
%
% The routine returns a matrix ik.  The jth row of ik has the
% spectral results for the duty cycle d = dvec(j).  The switching
% spectrum of the net input current consists of groups of (line)
% harmonics clustered around multiples of the switching frequency.
% The jth element of a row of ik contains the magnitude of the
% LARGEST harmonic in the freq range (j-0.5)*fsw <= f < (j+0.5)*fsw.
% This approach allows significant data reduction, while retaining
% information about the worst harmonic magnitude in each range.
% Note that the harmonic magnitude is the magnitude of the cosine
% component at a frequency ( e.g. X for X*cos(wt+phi) ).
%
%      ik          Matrix of spectral content over d.  Each row
%                  has the results for one d value (in dvec). The
%                  jth column elements contain the magnitude of
%                  the largest harmonic near the jth multiple of
%                  the switching frequency.
%      dvec        Vector of d values used for computing spectral
%                  components.
%      Lnorm       Value for the input inductors of each boost
%                  cell used in the normalized computations to
%                  achieve a total output power (Pout) = 1.  This
%                  value is used for de-normalization of the
%                  results.
%      M           Boost ratio: ratio of the output voltage to
%                  the peak line-line voltage.
%      pm          Period multiple.  The ratio of the line per-
%                  iod to the switching period.  This number
%                  must be an integer multiple of 12.
%      Nint        The number of cells being interleaved.
%      maxdfrac    The fraction of the maximum possible duty
%                  cycle ( which is (M-1)/M ) to use as the
%                  largest simulated value of d.  This number
%                  must be between 0 and 1. (Typically, it must
%                  be less than 1 by at least a small margin.)
%      numdsteps   The number of steps in duty cycle to sim-
%                  ulate over ( up to maxdfrac*(M-1)/M ).
%      fswmult     The multiple of the switching frequency to
%                  return harmonic data up to.  This number
%                  must be less than ppc/2 ( currently = 60 ).
%

rt3 = sqrt(3); % constant definitions
C1 = (rt3 - 1)/(rt3+1);

Vn = 1;    % input peak line to neutral voltage
Tsw = 1;   % switching period
vo = sqrt(3)*M; % output voltage
w = 2*pi/pm; % line angular frequency

maxd = (M-1)/M;     % maximum duty cycle allowed for discontin. conduction
```

```
maxd = maxdfrac*maxd;  % limit to specified fraction of theoretical maximum

% we want Pout = 1 at maximum d for our normalized
% parameter selections.  We can obtain this by selecting
% L properly as follows:

L = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
L = M*(L + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
L = L + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
L = (L - rt3/(2*M))*3/pi;
L = real(Nint*(maxd)^2*M^2*(L-1));

        % return this L value to the user
Lnorm = L;

        % anciliary variables
itran = 0.001;      % ask for high accuracy on current transitions
ppc = 120;          % num points per cycle.  Ideally we can look at up
                    % to ppc/2 harmonics of the switching frequency with
                    % the fft, but we must ensure that frequency content
                    % is low in that range to eliminate aliasing problems.
if fswmult >= ppc/2,
  error(['Error in BRCALIS1: fswmult must be < ppc/2 = ',num2str(ppc/2)]);
end;

                    % The BRSISS routine returns the components at all
                    % harmonics of the line.  In order to save space, the
                    % routine takes groups of harmonics clustered around
                    % each multiple of the switching freqency, and
                    % saves the largest magnitude from each group.
                    % The jth group is over the frequency range
                    %        (j-0.5)*fsw <= fsw < (j+0.5)*fsw
                    % Each group has pm elements.
                    % In this manner, the worst-case harmonic components
                    % are saved while reducing the data storage requirement
                    % by a factor of pm.
iklen = fswmult; % # of worst case harmonic groups stored.

ik = zeros(numdsteps,iklen); % The matrix of stored data

for dlp = 1:numdsteps,      % loop through set of d's and collect data
  d = dlp*maxd/numdsteps;
  disp(['calculating spectrum for d = ', num2str(d)]);
  [iss, issmag,issphi] = brsiss(L,vo,Vn,w,Tsw,d*Tsw,ppc,Nint);
  for iklp = 1:iklen,       % find & store highest harmonic in each group
    ik(dlp,iklp) = max(issmag( (iklp-0.5)*pm:((iklp+0.5)*pm-1) ));
  end; % for iklp
end; % for dlp

              % set up vectors of d and f (= f/fsw) values calculated
dvec = (1:numdsteps)*maxd/numdsteps;
              % Cross check that selection of L generated max Pout = 1
if abs((3*issmag(2)*Vn/2 - 1)) > 0.05,
  error('Error in BRCALIS1: Selection of L did not yield Pout,max = 1');
end;

% we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [irip,dvec,wtvec,Lnorm] = BRCALIR1(M,pm,Nint,maxdfrac,numdsteps,nptspi2);
%
%   [irip,dvec,wtvec,Lnorm] = BRCALIR1(M,pm,Nint,maxdfrac,numdsteps,nptspi2);
%
% This is a routine for calculating the (normalized) input current
% ripple for a set of interleaved 3 phase single-switch boost
% rectifiers across a space of operating points (values of d).  The
% routine is geared towards identifying what values of nominal boost
% ratio yield the best ripple.  Hence, the input inductance selected
% is a function of the boost ratio, and changes for different boost
% ratios.
%
% The relavent parameters specified by the user include M (the
% boost ratio), pm (the ratio of the line frequency to the switching
% frequency), and Nint (the number of cells being interleaved).  The
% user also sets the fraction of the peak possible duty cycle to use
% as a maximum, the number of steps in duty cycle to calculate, and
% the number of samples of the ripple magnitude to evaluate in pi/2
% of the line cycle.
%
% The results of the script are given in normalized form with
```

```
% Tsw and Vn = 1, and (total) Pout = 1 for the maximum specified
% duty cycle.  The user can calculate the currents for a system
% with real parameters (at the same M, pm, Nint, and d vals) by the
% following computation:
%           ireal = inorm*(Vn*Tsw*Lnorm/L) = inorm*(Pout/Vn)
% where Lnorm is the normalized input inductance selected by the
% routine (for each boost cell) to achieve a normalized total
% power of 1 at max d.  Lnorm is returned by the routine.  (Note
% that one must consider whether the input voltage or the output
% voltage is being held constant for comparison of normalized
% results for varying M.  For this routine normalized results are
% directly comparable for the case where Vn is held constant and
% vo is varied with M.)
%
% The routine returns a matrix irip.  The jth row of irip has the
% results for the duty cycle d = dvec(j). The jth element of a row
% contains the peak-to peak input current ripple magnitude at
% wtvec(j).
%       irip        Matrix of current ripple over d, wt.  Each row
%                   has the results for one d value (in dvec). The
%                   jth column elements contain the magnitude of
%                   the ripple at wtvec(j).
%       dvec        Vector of d values used for computing ripple.
%       wtvec       Vector of wt values at which ripple is computed.
%                   The elements span the range 0-pi/2.
%       Lnorm       Value for the input inductors of each boost
%                   cell used in the normalized computations to
%                   achieve a total output power (Pout) = 1.  This
%                   value is used for de-normalization of the
%                   results.
%       M           Boost ratio: ratio of the output voltage to
%                   the peak line-line voltage.
%       pm          Period multiple.  The ratio of the line per-
%                   iod to the switching period.  This number
%                   must be an integer multiple of 12.
%       Nint        The number of cells being interleaved.
%       maxdfrac    The fraction of the maximum possible duty
%                   cycle ( which is (M-1)/M ) to use as the
%                   largest simulated value of d.  This number
%                   must be between 0 and 1. (Typically, it must
%                   be less than 1 by at least a small margin.)
%       numdsteps   The number of steps in duty cycle to sim-
%                   ulate over ( up to maxdfrac*(M-1)/M ).
%       nptspi2     The number of points at which to compute the
%                   current ripple in [0,pi/2].  Points are evenly
%                   spaced and include 0, pi/2.
%
%

rt3 = sqrt(3); % constant definitions
C1 = (rt3 - 1)/(rt3+1);

Vn = 1;   % input peak line to neutral voltage
Tsw = 1;  % switching period
vo = sqrt(3)*M; % output voltage
w = 2*pi/pm; % line angular frequency

maxd = (M-1)/M;     % maximum duty cycle allowed for discontin. conduction
maxd = maxdfrac*maxd;  % limit to specified fraction of theoretical maximum

% we want Pout = 1 at maximum d for our normalized
% parameter selections.  We can obtain this by selecting
% L properly as follows:

L = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
L = M*(L + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
L = L + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
L = (L - rt3/(2*M))*3/pi;
L = real(Nint*(maxd)^2*M^2*(L-1));

        % return this L value to the user
Lnorm = L;

        % anciliary variables
itran = 0.001;      % ask for high accuracy on current transitions
ppc = 1440;         % num points per cycle.  This should be high to get
                    % accurate peak-to-peak ripple calculation, especially
                    % with many interleaved converters.
dwt = pi/(2*(nptspi2-1)); % step size for angular position
                          % both 0 and pi/2 points are included
irip = zeros(numdsteps,nptspi2); % The matrix of stored data

for dlp = 1:numdsteps,      % loop through set of d's and collect data
```

```
  d = dlp*maxd/numdsteps;
  disp(['calculating ripple for d = ',num2str(d)]);
  disp(' ');
  wt = -1*dwt;
  for k = 1:nptspi2-1,  % loop through angular position except for pi/2
    wt = wt+dwt;
%%% disp(['calculating for d = ',num2str(d),', wt = ',num2str(wt)]);
    [i_net,irip(dlp,k)] = brsisr(L,vo,Vn,w,Tsw,d*Tsw,ppc,Nint,wt);
  end;
                        % at exactly pi/2, the ripple must be zero
  irip(dlp,nptspi2) = 0;
end; % for dlp

                          % define the d and wt vectors for plotting
dvec = (1:numdsteps)*maxd/numdsteps;
wtvec = (0:(nptspi2-1))*dwt;

% we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [ikv,ikvworst] = BRCALIS2(L,vo,w,Tsw,Nint,Vnvec,Pomax,numdsteps,fswmult);
%
%    [ikv,ikvworst] = BRCALIS2(L,vo,w,Tsw,Nint,Vnvec,Pomax,numdsteps,fswmult);
%
% This is a routine for calculating the (normalized) input current
% spectrum for a set of interleaved 3 phase single-switch boost
% rectifiers across a space of operating points (values of d and
% Vn).  The routine is geared towards identifying the worst-case
% input spectral components over the expected range of input
% voltage and duty ratio for a specified design. (the duty ratio
% range for a Vn is set by the max output power Pomax.) This
% information can be used for design of the input EMI filter.
%
% The relavent parameters specified by the user include the
% input inductance, output voltage, switching and line freq-
% uencies, number of cells interleaved, and the total output
% power rating of the converter.  The user also specifies both
% the input voltages to calculate the spectral components for
% and the number of steps in duty cycle to use at each input
% voltage. (The max duty cycle used at each Vn is determined by
% the output power rating of the converter.) The user also spec-
% ifies the multiple of the switching frequency to return data
% up to.
%
% The routine returns a matrix ik.  The jth row of ik has the
% worst-case spectral results over d for the input voltage Vnvec(j).
% The switching spectrum of the net input current consists of groups
% of (line) harmonics clustered around multiples of the switching
% frequency. The jth element of a row of ik contains the magnitude
% of the LARGEST harmonic (over all tested d's) in the freq range
%             (j-0.5)*fsw <= f < (j+0.5)*fsw.
% This approach allows significant data reduction, while retaining
% information about the worst harmonic magnitude in each range over
% all values of duty cycle in the operating power range.
% Note that the harmonic magnitude is the magnitude of the cosine
% component at a frequency ( e.g. X for X*cos(wt+phi) ).
%
%      ikv         Matrix of spectral content over Vn.  Each row
%                  has the results for one Vn value (in Vnvec).
%                  The jth column elements contain the magnitude of
%                  the largest harmonic near the jth multiple of
%                  the switching frequency occuring for any value
%                  of duty cycle tested. Elements are in Amps.
%      ikvworst    Vector containing the largest harmonic magnitude
%                  in each frequency range over all values of Vn (and
%                  d) tested, Amps.
%      L           Input boost inductor value for each cell, Henries.
%      vo          Output voltage, Volts.
%      w           Line frequency, rad/sec.
%      Tsw         Switching period, sec.  The switching period should be
%                  chosen so that the line period is an integral multiple
%                  of twelve times the switching period.
%      Nint        Number of cells being interleaved.
%      Vnvec       Vector of peak line to neutral input voltages to test.
%                  elements are in Volts.
%      Pomax       Maximum power rating of the converter over all input
%                  line conditions, Watts.  (note: this parameter defines
%                  the range of d values tested at each Vn.  Pomax must
%                  be in the range achievable for all specified operating
%                  conditions.
```

```
%       numdsteps  The number of steps in duty cycle to sim-
%                  ulate over ( up to maxdfrac*(M-1)/M ).
%       fswmult    The multiple of the switching frequency to
%                  return harmonic data up to.  This number
%                  must be less than ppc/2 ( currently = 60 ).
%


%%%%%%% Test code for script %%%%%%%
%L = 50.6e-06;
%vo = 820;
%w = 2*pi*50;
%Tsw = 2*pi/(w*996);
%Nint = 1;
%Vnvec = 230*1.414*[0.85 1.0 1.1];
%Pomax = 7000;
%numdsteps = 2
%fswmult = 7;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


rt3 = sqrt(3); % constant definitions
C1 = (rt3 - 1)/(rt3+1);
pm = 2*pi/(w*Tsw);
                                    % storage for worst components at each Vn
ikv = zeros(length(Vnvec),fswmult);
                                    % storage for worst components over Vn
ikvworst = zeros(1,fswmult);

for Vnlp = 1:length(Vnvec),
  Vn = Vnvec(Vnlp)
  M = vo/(rt3*Vn); % boost ratio

  % we want to specify the proper max d to achieve Pout for the specified
  % Vn.  our normalized We can obtain this by selecting dmax properly as
  % follows:

  K = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
  K = M*(K + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
  K = K + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
  K = (K - rt3/(2*M))*3/pi;
  K = real(Tsw*vo*vo*(K-1)/(3*Pomax));
  dmax = sqrt(L/K);

       % anciliary variables
  itran = 0.001;      % ask for high accuracy on current transitions
  ppc = 120;          % num points per cycle.  Ideally we can look at up
                      % to ppc/2 harmonics of the switching frequency with
                      % the fft, but we must ensure that frequency content
                      % is low in that range to eliminate aliasing problems.
  if fswmult >= ppc/2,
    error(['Error in BRCALIS1: fswmult must be < ppc/2 = ',num2str(ppc/2)]);
  end;

                    % The BRSISS routine returns the components at all
                    % harmonics of the line.  In order to save space, the
                    % routine takes groups of harmonics clustered around
                    % each multiple of the switching freqency, and
                    % saves the largest magnitude from each group.
                    % The jth group is over the frequency range
                    %         (j-0.5)*fsw <= fsw < (j+0.5)*fsw
                    % Each group has pm elements.
                    % In this manner, the worst-case harmonic components
                    % are saved while reducing the data storage requirement
                    % by a factor of pm.
  iklen = fswmult; % # of worst case harmonic groups stored.
  ik = zeros(numdsteps,iklen); % The matrix of stored data over d at
                               % the current Vn

  for dlp = 1:numdsteps,      % loop through set of d's and collect data
    d = dlp*dmax/numdsteps;
    disp(['calculating spectrum for d = ', num2str(d)]);
    [iss, issmag,issphi] = brsiss(L,vo,Vn,w,Tsw,d*Tsw,ppc,Nint);
    for iklp = 1:iklen,       % find & store highest harmonic in each group
      ik(dlp,iklp) = max(issmag( (iklp-0.5)*pm:((iklp+0.5)*pm-1) ));
    end; % for iklp
  end; % for dlp

       % now take the worst cases over the d values and store them in ikv
  for iklp = 1:fswmult,
    ikv(Vnlp,iklp) = max(ik(:,iklp));
  end; % for iklp
end; % for Vnlp
```

```
      % now take the worst cases over the Vn values stored
for ikvlp = 1:fswmult,
  ikvworst(ikvlp) = max(ikv(:,ikvlp));
end;

% we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% RUNIS1
% This script is used for examining the effects of varying M and Nint
% on the input current spectral components, using the BRCALIS1 routine.
% The routine sweeps values of M and Nint and saves the worst-case
% harmonic components over the range of d values used.  For variations
% in M and Nint, the total power and energy storage of the converter
% system is held constant.
%

Mvec  = [1.25 1.5, 1.75, 2.0]; % vector of boost ratios to test
pm = 996;          % ratio of the line period to the switching period

maxdfrac = 0.98;  % fraction of theoretical maximum duty cycle to use
numdsteps = 10;    % number of steps in duty ratio to use
fswmult = 50;      % number of harmonic groups to check out

                   % each row of ikworst contains the worst component mag-
                   % nitudes for a value of M.  the jth column of each row
                   % contains the magnitude of the largest harmonic grouped
                   % about the jth multiple of the switching frequency.

%%%%%%%%%%%%%%%%%%%%%%%%
Nint = 1;          % number of cells interleaved
ikworst1 = zeros(length(Mvec),fswmult);
for mlp = 1:length(Mvec),
  M = Mvec(mlp)
  [ik1,dvec,Lnorm] = brcalis1(M,pm,Nint,maxdfrac,numdsteps,fswmult);

                   % calculate the largest harmonic magnitude in each
                   % grouping over the duty cycle vals calculated
  for iklp = 1:fswmult,
     ikworst1(mlp,iklp) = max(ik1(:,iklp));
  end; % for iklp
end; % for mlp

%%%%%%%%%%%%%%%%%%%%%%%%
Nint = 2;          % number of cells interleaved
ikworst2 = zeros(length(Mvec),fswmult);
for mlp = 1:length(Mvec),
  M = Mvec(mlp)
  [ik2,dvec,Lnorm] = brcalis1(M,pm,Nint,maxdfrac,numdsteps,fswmult);

                   % calculate the largest harmonic magnitude in each
                   % grouping over the duty cycle vals calculated
  for iklp = 1:fswmult,
     ikworst2(mlp,iklp) = max(ik2(:,iklp));
  end; % for iklp
end; % for mlp

%%%%%%%%%%%%%%%%%%%%%%
Nint = 4;          % number of cells interleaved
ikworst4 = zeros(length(Mvec),fswmult);
for mlp = 1:length(Mvec),
  M = Mvec(mlp)
  [ik4,dvec,Lnorm] = brcalis1(M,pm,Nint,maxdfrac,numdsteps,fswmult);

                   % calculate the largest harmonic magnitude in each
                   % grouping over the duty cycle vals calculated
  for iklp = 1:fswmult,
     ikworst4(mlp,iklp) = max(ik4(:,iklp));
  end; % for iklp
end; % for mlp

%%%%%%%%%%%%%%%%%%%%%%
Nint = 6;          % number of cells interleaved
ikworst6 = zeros(length(Mvec),fswmult);
for mlp = 1:length(Mvec),
  M = Mvec(mlp)
  [ik6,dvec,Lnorm] = brcalis1(M,pm,Nint,maxdfrac,numdsteps,fswmult);

                   % calculate the largest harmonic magnitude in each
                   % grouping over the duty cycle vals calculated
  for iklp = 1:fswmult,
```

```
    ikworst6(mlp,iklp) = max(ik6(:,iklp));
  end; % for iklp
end; % for mlp

% save the data to a file
save 'isv2mat1'

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% RUNIR1A
% a script for running BRCALIR1 to get normalized
% ripple data as M is varied.

% set params
pm = 996;
maxdfrac = 0.98;
numdsteps = 6;
nptspi2 = 18;
Nint = 1
M = 1.25

% do simulations at M = 1.5, 2.0
Nint = 1
M = 1.25
[M125N1rip, dvec125, wtvec,Lnorm1] = brcalir1(M,pm,Nint,maxdfrac,numdsteps,nptspi2);
M = 1.5
[M15N1rip, dvec15, wtvec,Lnorm1] = brcalir1(M,pm,Nint,maxdfrac,numdsteps,nptspi2);
M = 2.0
[M20N1rip, dvec20, wtvec,Lnorm1] = brcalir1(M,pm,Nint,maxdfrac,numdsteps,nptspi2);


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% RUNIS2
% This script is used for examining the effects of varying Vn and Nint
% on the input current spectral components, using the BRCALIS2 routine.

%%%%%%%%%%%%%%%%%%%%%%%%
L = 50.6e-06;          % input boost inductor (each cell)
vo = 820;              % output voltage
w = 2*pi*50;           % line period
Tsw = 2*pi/(w*996);    % switching period
Nint = 1;              % number of cells interleaved
                       % vector of input voltages to test over
Vnvec = 230*1.414*[0.85 1 1.1];
Pomax = 7000;          % maximum total output power
numdsteps = 6;         % number of duty cycle steps to test over
fswmult = 50;          % number of switching freq harmonic groups to save

              % call the calculation routine
[ikv1,ikvworst1] = brcalis2(L,vo,w,Tsw,Nint,Vnvec,Pomax,numdsteps,fswmult);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [iin,iu,i1,i2,dvec,wtvec,Lnorm] = BR_IPT(M,pm,maxdfrac,numdsteps,nptspi2);
%
%   [iin,iu,i1,i2,dvec,wtvec,Lnorm] = BR_IPT(M,pm,Nint,maxdfrac,numdsteps,nptspi2);
%
% This is a routine for comparing the use of input inductors vs.
% a combination of an input inductor and an interphase transformer
% interleaving a pair of 3 phase single-switch boost rectifiers.  The
% currents in the magnetic elements are calculated across a space of
% operating points (values of d) for a specified nominal boost ratio
% and max operating power.  The input inductance selected is a function
% of the boost ratio, and changes for different boost ratios.
%
% The relavent parameters specified by the user include M (the
% boost ratio), and pm (the ratio of the line frequency to the
% switching freq).  The user also sets the fraction of the peak
% possible duty cycle to use as a maximum, the number of steps in
% duty cycle to calculate, and the number of samples of the current
% magnitudes to evaluate in pi/2 of the line cycle.
%
% The results of the script are given in normalized form with
% Tsw and Vn = 1, and (total) Pout = 1 for the maximum specified
% duty cycle.  The user can calculate the currents for a system
% with real parameters (at the same M, pm, and d vals) by the
% following computation:
%          ireal = inorm*(Vn*Tsw*Lnorm/L) = inorm*(Pout/Vn)
% where Lnorm is the normalized input inductance selected by the
% routine (for each boost cell) to achieve a normalized total
% power of 1 at max d.  Lnorm is returned by the routine.  (Note
```

```
% that one must consider whether the input voltage or the output
% voltage is being held constant for comparison of normalized
% results for varying M.  For this routine normalized results are
% directly comparable for the case where Vn is held constant and
% vo is varied with M.)
%
% The routine returns matrices iin, iu, i1, i2.  The jth row of one
% of these matrices has the results for the duty cycle d = dvec(j).
% The jth element of a row contains the peak current magnitude at
% wtvec(j). iin is the net input current (and current for the inductor
% in the IPT case), iu is the IPT magnetizing current, i1, i2 are
% the output currents (and the inductor currents in the normal
% inductor case).
%
%      iin,iu,i1,i2
%                Matrices of peak currents over d, wt.  Each row
%                has the results for one d value (in dvec). The
%                jth column elements contain the magnitude of
%                the ripple at wtvec(j).
%      dvec      Vector of d values used for computing ripple.
%      wtvec     Vector of wt values at which ripple is computed.
%                The elements span the range 0-pi/2.
%      Lnorm     Value for the input inductors of each boost
%                cell used in the normalized computations to
%                achieve a total output power (Pout) = 1.  This
%                is the value for each inductor in the standard
%                two inductor case.  In the IPT case, the input
%                inductor and magnetizing inductance both have
%                the value of Lnorm/2, which yields identical
%                behavior with the standard inductor approach.
%                Lnorm is also used for de-normalization of the
%                results.
%      M         Boost ratio: ratio of the output voltage to
%                the peak line-line voltage.
%      pm        Period multiple.  The ratio of the line per-
%                iod to the switching period.  This number
%                must be an integer multiple of 12.
%      maxdfrac  The fraction of the maximum possible duty
%                cycle ( which is (M-1)/M ) to use as the
%                largest simulated value of d.  This number
%                must be between 0 and 1. (Typically, it must
%                be less than 1 by at least a small margin.)
%      numdsteps The number of steps in duty cycle to sim-
%                ulate over ( up to maxdfrac*(M-1)/M ).
%      nptspi2   The number of points at which to compute the
%                current ripple in [0,pi/2).  Points are evenly
%                spaced.
%

rt3 = sqrt(3); % constant definitions
C1 = (rt3 - 1)/(rt3+1);

Nint = 2; % number of converters interleaved
Vn = 1;   % input peak line to neutral voltage
Tsw = 1;  % switching period
vo = sqrt(3)*M; % output voltage
w = 2*pi/pm; % line angular frequency

maxd = (M-1)/M;    % maximum duty cycle allowed for discontin. conduction
maxd = maxdfrac*maxd;  % limit to specified fraction of theoretical maximum

% we want Pout = 1 at maximum d for our normalized
% parameter selections.  We can obtain this by selecting
% L properly as follows:

L = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
L = M*(L + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
L = L + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
L = (L - rt3/(2*M))*3/pi;
L = real(Nint*(maxd)^2*M^2*(L-1));

        % return this L value to the user
Lnorm = L;

        % anciliary variables
itran = 0.001;      % ask for high accuracy on current transitions
ppc = 1440;         % num points per cycle.  This should be high to get
                    % accurate peak-to-peak ripple calculation.
dwt = pi/(2*(nptspi2));  % step size for angular position

iin = zeros(numdsteps,nptspi2); % The matrices of stored data
iu = iin;
i1 = iu;
```

```
i2 = i1;

for dlp = 1:numdsteps,      % loop through set of d's and collect data
  d = dlp*maxd/numdsteps;
  disp(['calculating ripple for d = ',num2str(d)]);
  disp(' ');
  wt = -1*dwt;
  for k = 1:nptspi2,  % loop through angular position except for pi/2
    wt = wt+dwt;
    disp(['calculating for d = ',num2str(d),', wt = ',num2str(wt)]);
                        % calculate net input current for 2 converters
    [i_in,ijunk] = brsisr(L,vo,Vn,w,Tsw,d*Tsw,ppc,Nint,wt);
                        % calculate inductor current for 1 converter
    [i_1,ijunk] = brsisr(L,vo,Vn,w,Tsw,d*Tsw,ppc,1,wt);
                        % all maximum currents can now be calculated
    iin(dlp,k) = max(abs(i_in));
    i1(dlp,k) = max(abs(i_1));
    i2(dlp,k) = max(abs(i_in - i_1));
    iu(dlp,k) = max(abs(2*i_1 - i_in));
  end;
end; % for dlp

                            % define the d and wt vectors for plotting
dvec = (1:numdsteps)*maxd/numdsteps;
wtvec = (0:(nptspi2-1))*dwt;

% we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% This script (BRDvsVn) is used to examine the relationship between
% duty cycle and output power as Vn varies over a range and vo and
% L are held constant.  This is important for dealing with input
% supply voltage variations.

%%% w = 2*pi*50;
%%% Tsw = 2*pi/(w*960);
%%% Vnvec = 230*1.414*[0.85 0.9 0.95 1.0 1.05 1.10];
%%% vo = 820;
%%% Pomax = 7800/0.94; % desired Pout / expected efficiency
%%% numdsteps = 2

w = 2*pi*60;
Tsw = (2*pi/w)/1680;
Vnvec = 120*sqrt(2)*[0.85 0.9 1.0 1.1];
vo = 400;
Pomax = 450;
numdsteps = 2;

rt3 = sqrt(3); % constant definitions
C1 = (rt3 - 1)/(rt3+1);

% we want Pout = Pomax at maximum d for our parameter
% selections.  We must choose L based on the maximum input
% voltage (i.e. minimum value of M) to yield a system which
% can put out the rated power over the whole Vn range.  We
% can obtain this by selecting L properly as follows:

M = vo/(rt3*max(Vnvec));
maxd = (M-1)/M;
L = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
L = M*(L + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
L = L + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
L = (L - rt3/(2*M))*3/pi;
L = real(Tsw*vo^2*(maxd)^2*(L-1)/(3*Pomax))


% Lets see the d value required to meet Pout as Vn varies

dvec = zeros(size(Vnvec));
dmax = dvec;
for Vnlp = 1:length(Vnvec),
  Vn = Vnvec(Vnlp)
  M = vo/(rt3*Vn); % boost ratio

  % we want to specify the proper d to achieve Pout for the specified
  % Vn.  our normalized We can obtain this by selecting d properly as
  % follows:
  K = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
  K = M*(K + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
  K = K + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
```

```
  K = (K - rt3/(2*M))*3/pi;
  K = real(Tsw*vo*vo*(K-1)/(3*Pomax));
  dvec(Vnlp) = sqrt(L/K); % d needed for specified power @ M
  dmax(Vnlp) = (M-1)/M;   % max d for discontinuous conduction @ M
end;

% Lets look at how the max power and the max power for a limited d
% change as Vn changes.
Podmax = zeros(size(Vnvec)); % Max power for DCM operation at any M
Podlim = Podmax; % Power given by d for const Pout.  Should be const
Podcon = Podmax; % Power given by a const d = dmax at Mmin

for Vnlp = 1:length(Vnvec),
  Vn = Vnvec(Vnlp);
  M = vo/(rt3*Vn);

  % first calc Podmax
  d = dmax(Vnlp);
  P = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
  P = M*(P + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
  P = P + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
  P = (P - rt3/(2*M))*3/pi;
  P = real(Tsw*vo^2*(d)^2*(P-1)/(3*L))
  Podmax(Vnlp) = P;

  % next calc Podlim
  d = dvec(Vnlp);
  P = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
  P = M*(P + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
  P = P + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
  P = (P - rt3/(2*M))*3/pi;
  P = real(Tsw*vo^2*(d)^2*(P-1)/(3*L))
  Podlim(Vnlp) = P;

  % next calc Podcon
  d = min(dvec);
  P = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
  P = M*(P + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
  P = P + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
  P = (P - rt3/(2*M))*3/pi;
  P = real(Tsw*vo^2*(d)^2*(P-1)/(3*L))
  Podcon(Vnlp) = P;

end; % for Vnlp

% we are done

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [Pqcon,Pdcon,Pbrdcon,Pswon,Pswoff] =
brddiss(L,vo,Vn,w,Tsw,ton,idrive,Kdiode,Kgd,Kds,Cgs,gfs,VT,Ls,Rdson,Vdf,Rdf,Vbrdf,Rbrdf);
%
% BRDDISS    Simulation-based calculation of the semiconductor device
%            dissipation of the 3-phase single-switch boost rectifier. The
%            converter is simulated (using BRSIMPI3) over a pi/3 interval
%            and symmetry is used to reconstruct an input current
%            waveform over a full cycle.  Average and RMS current values
%            for the devices are calculated numerically from the simulated
%            waveforms (some of the results are cross-checked using
%            averaged models).  Conduction losses are then calculated
%            using "drop plus resistance" models.  Switching losses for
%            the MOSFET are calculated using the simulation waveforms
%            coupled with analytical models for the turn-on and
%            turn-off losses at each switching point.
%
%  [Pqcon,Pdcon,Pbrdcon,Pswon,Pswoff] = brddiss(L,vo,Vn,w,Tsw,ton,idrive,
%                       Kdiode,Kgd,Kds,Cgs,gfs,VT,Ls,Rdson,Vdf,Rdf,Vbrdf,Rbrdf);
%      L          Input boost inductor value, Henries.
%      vo         Output voltage, Volts.
%      Vn         Peak line to neutral input voltage, Volts.
%      w          Line frequency, rad/sec.
%      Tsw        Switching period, sec.
%      ton        Switch on time, sec.
%      vo         boost converter output voltage, Volts.
%      ipk        peak switch current at turn-off, Amps
%      idrive     peak gate drive current, amps
%      Kdiode     diode junction capacitance coeff, Farad-Volts^0.5
%      Kgd        gate-drain capacitance coeff, Farad-Volts^0.5
%      Kds        drain-source capacitance coeff, Farad-Volts^0.5
%      Cgs        Gate source capacitance, Farads (charge/volt @ Vgs=VT)
%                 This is the effective linear capacitance to discharge
```

```
%                (below the saturated part) when turning off the device
%      gfs       approx transconductance, Mhos: idrain = gfs*(Vgs-VT)
%      VT        MOSFET threshold voltage, Volts
%      Ls        Source inductance of MOSFET switch, Henries
%      Rdson     MOSFET on-state resistance, Ohms
%      Vdf       Boost diode base forward drop, Volts
%      Rdf       Boost diode incremental resistance, Ohms
%      Vbrdf     Bridge diode base forward drop, Volts
%      Rbrdf     Bridge diode incremental resistance, Ohms
%


Msc = 2*pi/(12*w*Tsw); % Msc is # of switch cycles in pi/6 of line

ppc = 120;       % many points per cycle for accuracy
dt = Tsw/ppc;
d = ton/Tsw;
rt3 = sqrt(3);
C1 = (rt3 - 1)/(rt3 + 1);
M = vo/(rt3*Vn);
itran = 0.001;   % small transition current threshold for high accuracy

                    % simulate over pi/3 line span
[ir, is, it, t, state] = brsimpi3(L,vo,Vn,w,Tsw,ton,ppc,itran);

                % Calculate mean and mean-square current for main switch

                  % set devon to one for those time steps where the
                  % main switch is conducting, and zero for other times
devon = ones(size(state)) - sign(state - ones(size(state)));
                  % switch current: sampled, average, and rms
iq = ir .* devon;
clear devon
iqave = ones(size(iq))*(iq')/length(iq)
iqrms = sqrt(iq*iq'/length(iq))

      % Cross check numerical calculation of RMS switch current
      % using Kolar's 1995 result (IEEE Trans P.E. Vol 31, No. 3)
iqrmschk = d^3*(0.125 + 3*rt3/(16*pi))/(M^2);
iqrmschk = 2*vo*Tsw*sqrt(iqrmschk)/(3*L);
if abs(iqrms - iqrmschk) > 0.1*iqrms,
  error('Error in BRDDISS: Crosscheck of rms switch current calc. failed');
end;

                  % boost diode current: sampled, average, and rms
id = ir - iq;
idave = ones(size(id))*(id')/length(id)
idrms = sqrt(id*id'/length(id))

      % Cross check numerical calculation of average diode current
      % using Kolar's 1995 result (IEEE Trans P.E. Vol 31, No 3)
idavechk = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
idavechk = M*(idavechk+ atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
idavechk = idavechk+atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
idavechk = (idavechk - rt3/(2*M))*3/pi;
idavechk = real((idavechk-1)*2*vo*Tsw/(3*L)*(d*d/2));
if abs(idave - idavechk) > 0.1*idave,
  idave
  idavechk
  error('Error in BRDDISS: Crosscheck of avg diode current calc. failed');
end;

                    % Calculate ir over full line cycle from
                    % available data and symmetry properties.
                    % This is for calculating input bridge diss.
ir_lcyc = zeros(1,(12*Msc*ppc));
ir_lcyc(1:2*Msc*ppc) = ir;
ir_lcyc(2*Msc*ppc+1:4*Msc*ppc) = -1*is;
ir_lcyc(4*Msc*ppc+1:6*Msc*ppc) = it;
ir_lcyc(6*Msc*ppc+1:8*Msc*ppc) = -1*ir;
ir_lcyc(8*Msc*ppc+1:10*Msc*ppc) = is;
ir_lcyc(10*Msc*ppc+1:12*Msc*ppc) = -1*it;

                    % Calculate the average and RMS currents in a bridge
                    % diode from a cycle of the line current in a phase.
                    % A bridge diode carries current for one half of a
                    % line cycle (pos or neg half). We will calculate
                    % based on the pos. half of the line current cycle.
ibrd = 0.5*(ir_lcyc + ir_lcyc.*sign(ir_lcyc));
clear ir_lcyc
ibrdave = ones(size(ibrd))*(ibrd')/length(ibrd);
ibrdrms = sqrt(ibrd*ibrd'/length(ibrd));
clear ibrd
```

```
      % Cross check numerical calculation of average bridge diode current
      % using the fact that ibrdav = (idave+iqave)/3.
ibrdavechk = (idave + iqave)/3;
if abs(ibrdave - ibrdavechk) > 0.1*ibrdave,
  ibrdave
  ibrdavechk
  error('Error in BRDDISS: Crosscheck of avg bridge diode current calc. failed');
end;

%  Calculate device conduction losses based on ave and rms currents
Pqcon = (iqrms^2)*Rdson; % FET is entirely on-state resistance loss.
Pdcon = idave*Vdf + (idrms^2)*Rdf;
Pbrdcon = ibrdave*Vbrdf + (ibrdrms^2)*Rbrdf;

%  Calculate switching losses over a full cycle

%%%%                % For a first pass, we will assume that the peak
%%%%                % switch current does not fluctuate too drastically
%%%%                % over the pi/6 segment of line cycle, and calculate
%%%%                % the losses based on the highest turned-off current
%%%%                % level
%%%%ipk = max(iq)
%%%%[Eon,Eoff] = brswloss(vo,ipk,idrive,Kdiode,Kgd,Kds,Cgs,gfs,VT,Ls);
%%%%Pswon = Eon/Tsw;
%%%%Pswoff = Eoff/Tsw;


                  % We will do an accurate switching loss calculation
                  % by finding the peak turn-off current in each
                  % cycle and calculating its associated loss.
Eoffvec = zeros(1,Msc);
for swofflp = 1:Msc,
  ipk = max(iq((swofflp-1)*ppc+1:swofflp*ppc));
  [Eon,Eoff] = brswloss(vo,ipk,idrive,Kdiode,Kgd,Kds,Cgs,gfs,VT,Ls);
  Eoffvec(swofflp) = Eoff;
end; % for swofflp
Pswoff = 12*w*sum(Eoffvec)/(2*pi);
Pswon = Eon/Tsw;

                     % we are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [Eon,Eoff] = brswloss(vo,ipk,idrive,Kdiode,Kgd,Kds,Cgs,gfs,VT,Ls);
%
%  function [Eon,Eoff] = brswloss(vo,ipk,idrive,Kdiode,Kgd,Kds,Cgs,gfs,VT,Ls);
%
%  This routine is for calculating the switching energy loss for the boost
%  rectifier MOSFET during one switching cycle, and is mainly used by the
%  Matlab routine BRDDISS.  The approaches used in this function
%  for computing these losses are addressed in "Power MOSFETS: Theory and
%  Application" by Grant and Gower, Chapter 4 (esp. pp 135-139).  Some
%  concepts are also well addressed in Brett Miwa's thesis (MIT 1992).
%  As in these works, we will consider a "constant current" gate drive
%  and nonlinear junction capacitances of the form C(V) = K/sqrt(V).
%
%  vo              boost converter output voltage, Volts.
%  ipk             peak switch current at turn-off, Amps
%  idrive          peak gate drive current, amps
%  Kdiode          diode junction capacitance coeff, Farad-Volts^0.5
%  Kgd             gate-drain capacitance coeff, Farad-Volts^0.5
%  Kds             drain-source capacitance coeff, Farad-Volts^0.5
%  Cgs             Gate source capacitance, Farads (charge/volt @ Vgs=VT)
%  gfs             approx transconductance, Mhos: idrain = gfs*(Vgs-VT)
%  VT              MOSFET threshold voltage, Volts
%  Ls              Source inductance of MOSFET switch, Henries
%

% First, we will calculate turn-off times and losses.

% The first section of turn-off fall time having power dissipation, tcb,
% is when the miller Capacitance is being charged up.  Ecb is the energy
% dissipated in this time window.
tcb = 2*Kgd*sqrt(vo)/idrive;
Ecb = (2*ipk*Kgd*vo^(1.5))/(3*idrive);

% The second section of turn-off fall time is that required to reduce the
% gate voltage from the saturation voltage down to the threshold VT.  This
% time period may be dominated by either the time to discharge the Gate-
% source capacitance, or the time to change the current in the source lead
% inductance.  We will use the behavior of a simple L,C, current source and
```

```
% ideal diode model to get an estimate of the time this takes.  We will
% also make the simple approximation that current fall is linear during the
% this entire time period (tdc).
          % saturation voltage (of Vgs) during turn-off
Vsat = VT + ipk/gfs;

          % calculation of tdc is implemented as follows:
normaloff = 0; % flag to find unexpected turn-off process

t1 = sqrt(Ls*Cgs)*atan2(sqrt(Vsat*Vsat - VT*VT),VT);
if (Vsat*sqrt(Cgs/Ls) < idrive),
  tdc = t1;
%%%%%%%%%%  disp('BRSWLOSS finds unclamped Ls,Cgs ring for turn-off!');
else
  t2 = sqrt(Ls*Cgs)*asin(idrive*sqrt(Ls/Cgs)/Vsat);
  if (t2 > t1),
    tdc = t1;
%%%%%%%%%%    disp('BRSWLOSS finds pre-clamped Ls,Cgs ring for turn-off');
  else
    tdc = t2 + Cgs*(Vsat*cos(t2/sqrt(Ls*Cgs)) - VT)/idrive;
%    disp('-------------------------');
%    disp('BRSWLOSS finds:')
%    disp(['tdc = ',num2str(tdc)]);
%    disp(['t2 =  ',num2str(t2)]);
    normaloff = 1;
  end; % if t2 > t1
end; % if (Vsat*sqrt...
tfall = tcb+tdc;
%disp(['BRSWLOSS finds tfall = ',num2str(tfall)]);
if normaloff == 0,
  disp('WARNING: Unusual turn-off found in BRSWLOSS');
end;

          % Energy loss calculation assumes linear current fall in tdc.
Edc = 0.5*tdc*vo*ipk;

% Now calculate the capacitive turn-on losses of the switch
Eon = (2*Kdiode + Kgd + Kds)*vo*sqrt(vo)*2/3;
Eoff = Edc + Ecb;
% We are done


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% This script is used to design the input inductors
% for the boost rectifier.  Given the operational
% parameters of the boost inductor, the script generates
% feasable designs for the inductor based on core and
% wire data in the script BRLDAT.  The script tries to
% design an inductor based on each core in the data set
% and retains those which are feasable.  For each design
% the script calculates core losses and winding losses
% ( including losses due to skin and proximity effect)
% based on fitted empirical data and theoretical models.
% The loss data ( and expected core temperature rise)
% are retained with the design parameters for all
% feasible designs, and are stored in the specified
% diary file.

% Set up parameters for this test
% We will use parameters set up to be realistic
vo = 400;
Vnbase = sqrt(2)*120;   % three phase 208, with tolerance
Vnmin = 0.85*Vnbase;
Vn = Vnmin;
Nint = 1;
maxdfrac = 0.9; % fraction of max theoretical duty cycle
w = 2*pi*60;              % 60 Hz
outfname = 'ldes100.asc'; % output file name
Tsw = (2*pi/w)/1680;     % fsw about 150 kHz
L = 60.7e-06; % L is specified in Henries
Msc = 2*pi/(12*w*Tsw); % Msc is # of switch cycles in pi/6 of line
ppc = 120;        % many points per cycle for accuracy
dt = Tsw/ppc;
rt3 = sqrt(3);
C1 = (rt3 - 1)/(rt3 + 1);
Pomax = 550; % command duty cycle for this power
maxdfrac = 0.9; % fraction of max theoretical duty cycle
%%%%%%  d = maxdfrac*(M-1)/M;
                % We will use Mmax (low line) for loss computations
                % and we will run at Pomax (full power)
M = vo/(rt3*Vnmin)
```

```
Vn = Vnmin;
  % we want to specify the proper d to achieve Pout for the specified
  % Vn.  We can obtain this by selecting d properly as follows:
  K = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
  K = M*(K + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
  K = K + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
  K = (K - rt3/(2*M))*3/pi;
  K = real(Tsw*vo*vo*(K-1)/(3*Pomax));
  d = sqrt(L/K); % d needed for specified power @ M
ton = d*Tsw
if d > 1.001*maxdfrac*(M-1)/M,
  error('BRLDES: Duty cycle commanded exceeds maximum specified value.');
end;
itran = 0.001;   % small transition current threshold for high accuracy

% Simulate the converter and calculate the inductor current
% and its input spectrum one line cycle.  The result is then
% used to calculate the core and winding losses, as well as
% the energy storage required.

[i_lcyc, issmag, issphi] = brsiss(L,vo,Vn,w,Tsw,ton,ppc,Nint);
%%%%%%save 'ilwave2.mat' i_lcyc issmag issphi
%%%%%%load 'ilwave2.mat';
i_lrms = sqrt(i_lcyc*i_lcyc'/length(i_lcyc));
ipk = max(i_lcyc);

% Run the script which sets up core and wire data
brldat;

% Save program responses to the output file.
diary(outfname);
disp(['L = ',num2str(L)]);
% Loop through available cores and synthesize
% inductor designs.
for core = 1:numcores,
  designok = 1; % assume this core design works
             % Calc number of turns needed on this
             % core to get desired L value.
  N = round(1000*sqrt(1000*L/AL(core)));
             % Calculate B at peak current in gauss
             % for this N.
  Bpk = 0.1*AL(core)*N*ipk/Ac(core);
             % If required peak B is more than 3000
             % gauss, then we are too close to the
             % Bsat = 3300 gauss, and the design is
             % not acceptable
  if Bpk > 3000,
    designok = 0;  % design is not ok
    disp([corename(core,:),' rejected: Bpk = ',num2str(Bpk),' gauss.']);
  end;
             % If design is still ok, try to find a
             % wire size which fits on the core.
             % Select largest wire which fits.
             % This may not be at all optimal.
  guage = minguage-1;
  while designok == 1,
    guage = guage + 1; % check next guage
    if guage > maxguage,
      designok = 0 % acceptable wire guage not found,
                   % this design is not acceptable
      disp([corename(core,:),' rejected: no wire fits.']);
    end;
    winarea = N/tpsqin(guage);
    if winarea < wa(core),
      break; % This wire guage is ok,
             % break out of loop
    end;
  end; % while designok == 1;

             % If design is still ok, check to make
             % sure that current in wire is at an
             % acceptable level.  Reject the design
             % if not.  We require the rms current
             % density to be less than 3000 A/in^2.
  if designok == 1,
    Jwire = i_lrms/(pi*(dwire(guage)/2)^2);
    if Jwire >= 3000,
      designok = 0;
      disp([corename(core,:),' rejected: Jwire = ',num2str(Jwire),' A/in^2.']);
    end; % if Jwire
  end; % if designok

             % If the design is still ok, calculate
```

```
            % the inductor losses.  These losses
            % include the core losses and the
            % winding losses.
  if designok == 1,
            % Calculate core losses.  This eqn. is
            % a fit of empirical data.  Pcore is in
            % watts, fsw is in kHz, B is in gauss,
            % Vc is in cm^3.  This is a conservative
            % estimate based on the peak flux swing
            % encountered in the cycle.
    Pcore = 9.16e-13*(1e-03/Tsw)^1.231*(Bpk/2)^2.793*Vc(core);

            % Calculate winding losses using the approach
            % of Carsten (PCIM Nov. 1986, pp 34 - 46).  We
            % calculate an equivalent resistance at each freq
            % which accounts for both skin & proxim effect.
            % This is used to calc total winding loss from
            % the spectrum of the inductor current.

            % dc resistance of the winding = resistance per
            % inch x inches per turn x # of turns
    Rdc = Rperl(guage)*lpt(core)*N;
            % equiv square-wire thickness of conductor (Carsten)
    heff = (pi/4)^0.75*dwire(guage)^1.5/sqrt(dinsu(guage));
            % approx number of wiring layers needed
            % assume 90% horizontal packing
    m = round(N/(0.9*ww(core)/dinsu(guage)));
            % each frequency component in the inductor current is
            % a multiple of the line frequency.  We will calculate
            % loss components at each multiple of the line freq:
            % i(t) = sum over k of (issmag(k)*cos((k-1)*w*t+issphi(k))).
            % we have data for 1 <= k <= ppc*pi/(w*Tsw).  We will
            % calculate Rmult, which is the ratio of the effective
            % ac resistance to the dc resistance at each k value
            % up to a predefined switching frequency multiple fswmult.
    fswmult = 10;
    k = 1:(6*2*fswmult*Msc-1);
            % Calc skin depth at each frequency.
            % This actually varies vs. T, wire
            % composition, etc.
    skind = 2.6*ones(size(k))./sqrt((k)*w/(2*pi));
            % Using Carsten's calculations:
    Xk = heff*ones(size(skind))./skind; % eff. wire thickness in skin depths
    Xcplx = Xk + i*Xk;
    M1 = real(Xcplx.*(cosh(Xcplx)./sinh(Xcplx)));
    D1 = real(2*Xcplx.*(sinh(0.5*Xcplx)./cosh(0.5*Xcplx)));
    Rmult = M1 + (m^2-1)*D1/3;
    Rmult = [1,Rmult]; % include dc term
    Pwind = sum(issmag(1:6*2*fswmult*Msc) .* issmag(1:6*2*fswmult*Msc) .* ...
            (Rdc*Rmult));
  end; % if designok = 1 calc inductor losses

             % if design is ok, calculate core temperature
             % rise, and reject design if it is too high.
             % we define too high as >= 50 deg Celcius.
  if designok == 1,
    deltaT = Rth(core)*(Pwind+Pcore);
    if deltaT > 80,
      designok = 0;
      disp([corename(core,:),' rejected: delta T = ',num2str(deltaT),' deg C.']);
    end;
  end;

       % If the design is ok, display the data
  if designok == 1,
    disp('                ');
    disp([corename(core,:),' :']);
    disp(['N = ',num2str(N),' of guage ',num2str(guage)]);
    disp(['Bpk ',num2str(Bpk)]);
    disp(['Jwire = ',num2str(Jwire),' A/in^2']);
    disp(['Pcore = ',num2str(Pcore),' Watts']);
    disp(['Pwind = ',num2str(Pwind),' Watts']);
    disp(['Ptot = ',num2str(Pcore+Pwind),' Watts']);
    disp(['delta T = ',num2str(deltaT),' deg C']);
    disp('----------------------------');
  end; % if designok = 1
end; % for core
diary off;
% we are finished.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% This script BRLdat.m defines variables containing data
```

```
% for boost-rectifer inductor design.  Params for Phillips
% (Ferroxcube) 3F3 material ferrite square cores are
% defined, as is some wire table data for various guages.
%
% The core data is for Phillips ferrite square cores, sizes
% RM8 to RM14.  These cores seem to be a good choice for the
% application.  The 3F3 material is specified for its low
% loss characteristics.  The data sets are as follows:
%   Quantity               Var name         units
%   Number of cores        numcores         numerical
%   Core name              corename         text
%   AL (mH@1000 turns)     AL               numerical
%   eff. core area         Ac               cm^2
%   eff. core volume       Vc               cm^3
%   core thermal Resist.   Rth              deg C / W
%   core winding area      wa               in^2
%   core winding width     ww               in
%   avg. length per turn   lpt              in
%
% The wire data is taken directly from the phillips ferrite
% components data book and the New England Wire Co. data
% book.  The data for a given guage is
% indexed by the guage number, so dwire(12) is the diameter
% of 12 guage wire.  The wire data specified is as follows:
%   Quantity               Var name         units
%   min wire guage         minguage         numeric
%   max wire guage         maxguage         numeric
%   bare wire diameter     dwire            in
%   insulated diameter     dinsu            in
%   Turns / in^2           tpsqin           numeric
%   Resistance / length    Rperl            Ohms / in.
%

%%%%%%%%%%%%%%%%%% Core data, Phillips 3F3 square cores RM6 - RM14

% Core names
corename = [...
'RM6SPA63  ' ; 'RM6SPA100 ' ; 'RM6SPA160 ' ; 'RM6SPA250 ' ; 'RM6SPA315 '; ...
'RM8PA160  ' ; 'RM8PA250  ' ; 'RM8PA315  ' ; 'RM8PA400  ' ; ...
'RM10PA160 ' ; 'RM10PA250 ' ; 'RM10PA315 ' ; 'RM10PA400 ' ; 'RM10PA630 ' ; ...
'RM12PA160 ' ; 'RM12PA250 ' ; 'RM12PA315 ' ; 'RM12PA400 ' ; ...
'RM14PA250 ' ; 'RM14PA315 ' ; 'RM14PA400 ' ; 'RM14PA630 ' ; 'RM14PA1000' ];

numcores = length(corename);

% AL is mH for 1000 Turns
AL = [  63 ; 100 ; 160 ; 250 ; 315 ; ...
       160 ; 250 ; 315 ; 400 ; ...
       160 ; 250 ; 315 ; 400 ; 630 ; ...
       160 ; 250 ; 315 ; 400 ; ...
       250 ; 315 ; 400 ; 630 ; 1000 ];

% Ac is effective core area in cm^2
Ac = [ 0.37 ; 0.37 ; 0.37 ; 0.37 ; 0.37 ; ...
       0.52 ; 0.52 ; 0.52 ; 0.52 ; ...
       0.83 ; 0.83 ; 0.83 ; 0.83 ; 0.83 ; ...
       1.46 ; 1.46 ; 1.46 ; 1.46 ; ...
       1.98 ; 1.98 ; 1.98 ; 1.98 ; 1.98 ];

% Vc is effective core volume in cm^3
Vc = [  1.09 ;  1.09 ;  1.09 ;  1.09 ;  1.09 ; ...
        1.85 ;  1.85 ;  1.85 ;  1.85 ; ...
        3.47 ;  3.47 ;  3.47 ;  3.47 ;  3.47 ; ...
        8.34 ;  8.34 ;  8.34 ;  8.34 ; ...
       13.90 ; 13.90 ; 13.90 ; 13.90 ; 13.90 ];

% Rth is core thermal resistance in deg. C / W
Rth = [ 60 ; 60 ; 60 ; 60 ; 60; ...
        38 ; 38 ; 38 ; 38 ; ...
        30 ; 30 ; 30 ; 30 ; 30 ; ...
        23 ; 23 ; 23 ; 23 ; ...
        19 ; 19 ; 19 ; 19 ; 19 ];

% wa is core (bobbin) winding area in square inches
wa = [ 0.024 ; 0.024 ; 0.024 ; 0.024 ; 0.024 ; ...
       0.048 ; 0.048 ; 0.048 ; 0.048 ; ...
       0.066 ; 0.066 ; 0.066 ; 0.066 ; 0.066 ; ...
       0.120 ; 0.120 ; 0.120 ; 0.120 ; ...
       0.170 ; 0.170 ; 0.170 ; 0.170 ; 0.170 ];

% ww is core (bobbin) winding width in inches
ww = [ 0.254 ; 0.254 ; 0.254 ; 0.254 ; 0.254 ; ...
       0.365 ; 0.365 ; 0.365 ; 0.365 ; ...
```

```
       0.409 ; 0.409 ; 0.409 ; 0.409 ; 0.409 ; ...
       0.567 ; 0.567 ; 0.567 ; 0.567 ; ...
       0.726 ; 0.726 ; 0.726 ; 0.726 ; 0.726 ];

% lpt is average wire length per turn in inches
lpt = [ 1.18 ; 1.18 ; 1.18 ; 1.18 ; 1.18 ; ...
        1.65 ; 1.65 ; 1.65 ; 1.65 ; ...
        2.00 ; 2.00 ; 2.00 ; 2.00 ; 2.00 ; ...
        2.40 ; 2.40 ; 2.40 ; 2.40 ; ...
        2.80 ; 2.80 ; 2.80 ; 2.80 ; 2.80 ];

%%%%%%%%%%%%%%% Wire Data, vectors indexed by guage number (10-30 ga);

% no data for guages 1 - 10;
gablank = [NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ];
maxguage = 30;
minguage = 10;

% bare wire diameter in inches
dwire = [ gablank ; ...
          0.1019 ; 0.0907 ; 0.0808 ; 0.0719 ; 0.0641 ; 0.0571 ; ...
          0.0508 ; 0.0453 ; 0.0403 ; 0.0359 ; 0.0320 ; 0.0285 ; ...
          0.0254 ; 0.0226 ; 0.0201 ; 0.0179 ; 0.0159 ; 0.0142 ; ...
          0.0126 ; 0.0113 ; 0.0100 ];

% (Nominal) heavy film insulated wire diameter in inches.
% Taken from New England Wire Co. Data book.
dinsu = [ gablank ; ...
          0.1056 ; 0.0938 ; 0.0837 ; 0.0749 ; 0.0675 ; 0.0602 ; ...
          0.0539 ; 0.0482 ; 0.0431 ; 0.0386 ; 0.0346 ; 0.0309 ; ...
          0.0276 ; 0.0249 ; 0.0223 ; 0.0199 ; 0.0178 ; 0.0161 ; ...
          0.0144 ; 0.0130 ; 0.0116 ];

% turns per square inch (heavy film insulated wire, machine wound)
% Taken from Phillips ferrite core data book.  This is more
% conservative than the New England Wire Co. data book estimate.
tpsqin = [ gablank ; ...
             89 ;  112 ;  140 ;  176 ;  221 ;  259 ;  327 ; ...
            407 ;  509 ;  634 ;  794 ;  989 ; 1238 ; 1532 ; ...
           1893 ; 2351 ; 2932 ; 3711 ; 4581 ; 5621 ; 7060 ];

% resistance per length in Ohms / inch (from Phillips data book)
Rperl = 1.0e-05 * [ gablank ; ...
                      8.333 ;  10.500 ;  13.167 ;  16.667 ; ...
                     21.083 ;  26.500 ;  33.500 ;  42.167 ; ...
                     53.250 ;  67.083 ;  84.167 ; 106.667 ; ...
                    135.000 ; 169.167 ; 214.167 ; 270.000 ; ...
                    341.667 ; 428.333 ; 544.167 ; 676.667 ; ...
                    866.667 ];
% The previous values are at 20 deg C.  We should scale them
% for operation at 100 deg C.
Rperl = Rperl*(1 + 0.004*(100-20));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% This is a script for checking against the IEC 555-2 harmonic
% limits.  It should be noted that this spec only applies to
% systems with less than or equal to 15 A rms per phase.  We
% will use the parameters expected for our prototype system

L  = 60.7e-06
vo = 400
Vn = 120*1.414*1.1; % high line
w = 2*pi*60
Pomax = 550; % max output power
permult = 1680/6;   % permult shoud be even to give integer # of cycles in pi/6.
Tsw = ((2*pi/w)/6)/permult % 1/permult of 1/6th of a line period
M = vo/(sqrt(3)*Vn);
maxdfrac = 0.9;  % max fraction of ideal duty cycle to allow
maxd = maxdfrac*(M-1)/M;

% we want to specify the proper max d to achieve Pout for the specified
% Vn.  our normalized We can obtain this by selecting dmax properly as
% follows:
rt3 = sqrt(3);
C1 = (rt3 - 1)/(rt3+1);
K = atan( ((rt3-1)*M/(rt3+1) - rt3)/sqrt(M*M-3) );
K = M*(K + atan( rt3/sqrt(M*M-3) ))/sqrt(M*M-3);
K = K + atan(C1*sqrt((M+1)/(M-1)))*3*M/sqrt(M*M-1);
K = (K - rt3/(2*M))*3/pi;
K = real(Tsw*vo*vo*(K-1)/(3*Pomax));
d = sqrt(L/K);
if d > 1.001*maxd,
```

```
  error('IEC555: Commanded d exceeds allowed maximum.');
end;
ton = d*Tsw;
harmnums = 1:40;
iec555 = zeros(size(harmnums));
for harm = 1:40,
  if (harm/2) == round(harm/2),
    % even harmonic
    iec555(harm) = 0.23*8/harm;
  else
    % odd harmonic
    iec555(harm) = 0.15*15/harm;
  end;
end;
iec555(1)  = NaN;
iec555(2)  = 1.08;
iec555(3)  = 2.30;
iec555(4)  = 0.43;
iec555(5)  = 1.14;
iec555(6)  = 0.30;
iec555(7)  = 0.77;
iec555(9)  = 0.40;
iec555(11) = 0.33;
iec555(13) = 0.21;

% BRAILH to calculate averaged model input line harmonics
 [ilhavmag, ilhavphi] = brailh(L,vo,Vn,w,Tsw,ton,harmnums);
% convert magnitude data to RMS
ilhavmag = ilhavmag/sqrt(2);
% we are done

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% This script (BRCL1) is used to look at the averaged (load) step
% response of the s.s. boost rectifier under proportional duty ratio
% control.  An averaged "injected current" model is used for the
% converter.

% set up program constants
Vref = 420;           % no load reference voltage
L  = 40.4e-06;        % input inductance
Vn = 120*1.414;       % nominal line voltage
w = 2*pi*60           % line angular frequency
permult = 2520/6;     % permult is # switching cycles in 1/6 cycle.
                      % permult shoud be even to give integer # of
                      % cycles in pi/6. Set for fsw = 150 kHz.
Tsw = ((2*pi/w)/6)/permult % 1/permult of 1/6th of a line period
dwt = w*Tsw;          % phase step in one switching period
maxdfrac = 0.9;       % max fraction of ideal duty cycle to allow
C= 5.0e-06;           % output capacitance, in Farads
numlcyc = 6;          % number of line cycles to simulate over
npts = numlcyc*permult*6; % number of points to store
Kp = 0.028;          % proportional gain: d/Verr. Old val = 0.015

% set up initial conditions
tvec = (0:npts-1)*Tsw; % time points
vovec = zeros(size(tvec)); % output voltage points
dvec = vovec;           % commanded duty ratio points
idvec = vovec;        % average current
id2vec = vovec;          % simpler approx to average current
R = 32000;            % Load resistance, in ohms
wt = 0;               % initial starting phase
stepdir = 1;          % direction for changing wt
                      % we swing back & forth in [0,pi/6].
                      % get the correct answer
vovec(1) = 418.76;    % initial output voltage

% loop through and calculate response
for lp = 1:npts-1,
  if lp > npts/2,
    R = 320;
  end;
  M = vovec(lp)/(sqrt(3)*Vn); % current boost ratio
  if M <= 1,
    error('M fell below 1');
  end;
  maxd = maxdfrac*(M-1)/M;
  d = Kp*(Vref - vovec(lp));
  if d > maxd, % limit duty cycle
    d = maxd;
    disp('d limited to maxd');
  end; % if
  if d < 0,
```

```
    d = 0;
  end; % if
  dvec(lp) = d;
  id = 2*vovec(lp)*Tsw*3*d*d*(1-cos(wt)*cos(2*wt+pi/6)/M) ...
       / ((3*L*8*M*M) * (1 + sqrt(3)*(sin(wt-pi/6))/M) ...
       * (1 - cos(wt-pi/6)/M));
  id2 = 2*vovec(lp)*Tsw/(3*L) * 3*d*d / ((8*M*M)*(...
        1-cos(wt-pi/6)/M)); % a simplified approximation
  id2vec(lp) = id2;
  idvec(lp) = id;
%%%%%
%%  vovec(lp+1) = vovec(lp) + Tsw*(id - vovec(lp)/R)/C;
%%%%%
  vovec(lp+1) = id*R + (vovec(lp)-id*R)*exp(-Tsw/(R*C));
  wt = wt + stepdir*dwt;
  if wt >= pi/6,
    stepdir = -1*stepdir;
  end; % if
  if wt <= 0,
     stepdir = -1*stepdir;
  end; % if
end; % for
% we are done
```

Appendix C

This appendix lists the manufacturing information for the boost rectifier cells of Chapter 8. The appendix includes schematics, a bill of materials, a parts list, and scaled artwork for the cells. This data was generated in the Tango-Schematic and Tango-PCB software packages. Note that the inrush current limiters (Digi-key type KC0008L-ND) were added directly in series with the inductor windings, and were not placed on the pc board itself.

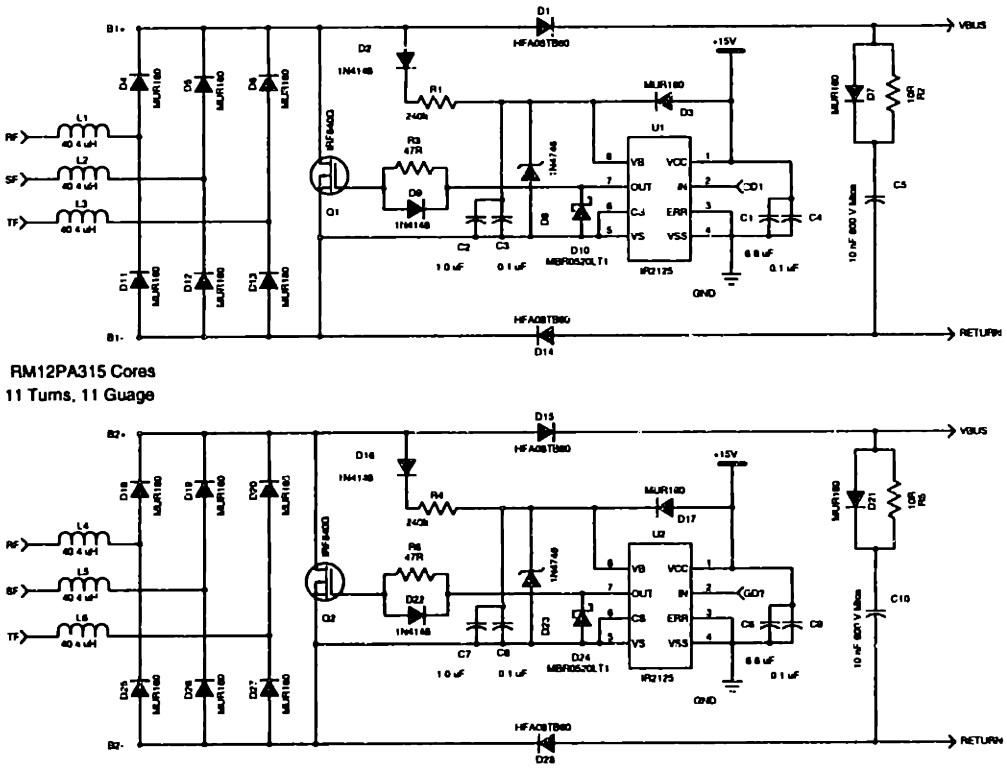

Figure C.1 Boost rectifier cell schematics, sheet 1.

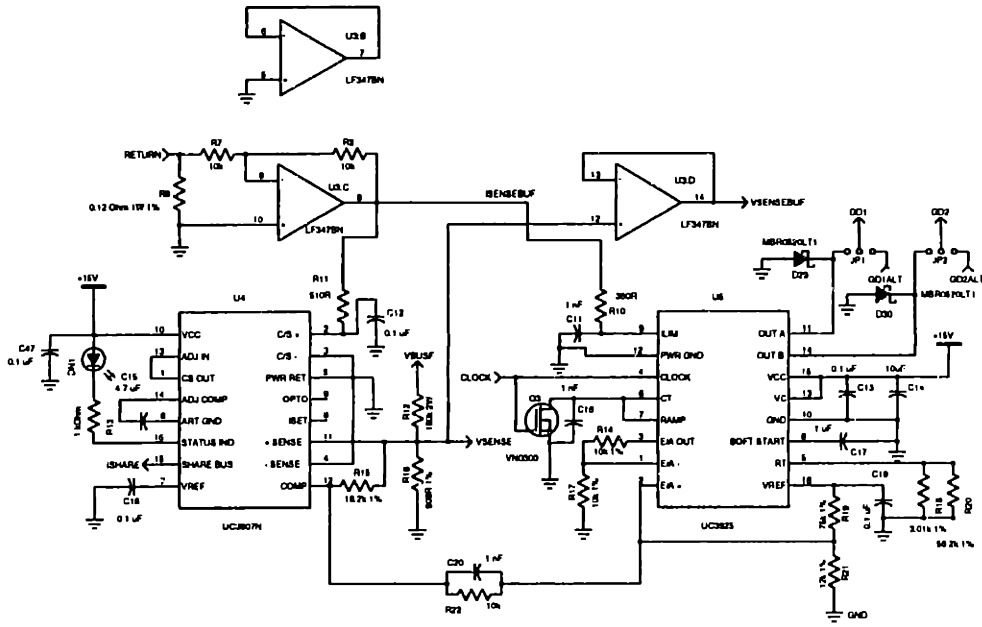

Figure C.2 Boost rectifier cell schematics, sheet 2.

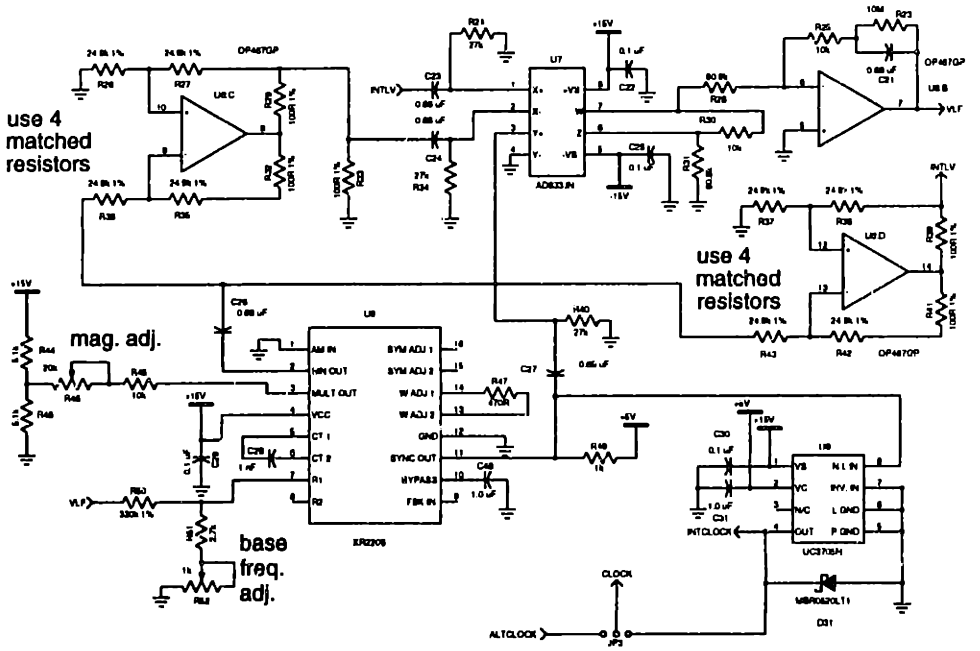

Figure C.3 Boost rectifier cell schematics, sheet 3.

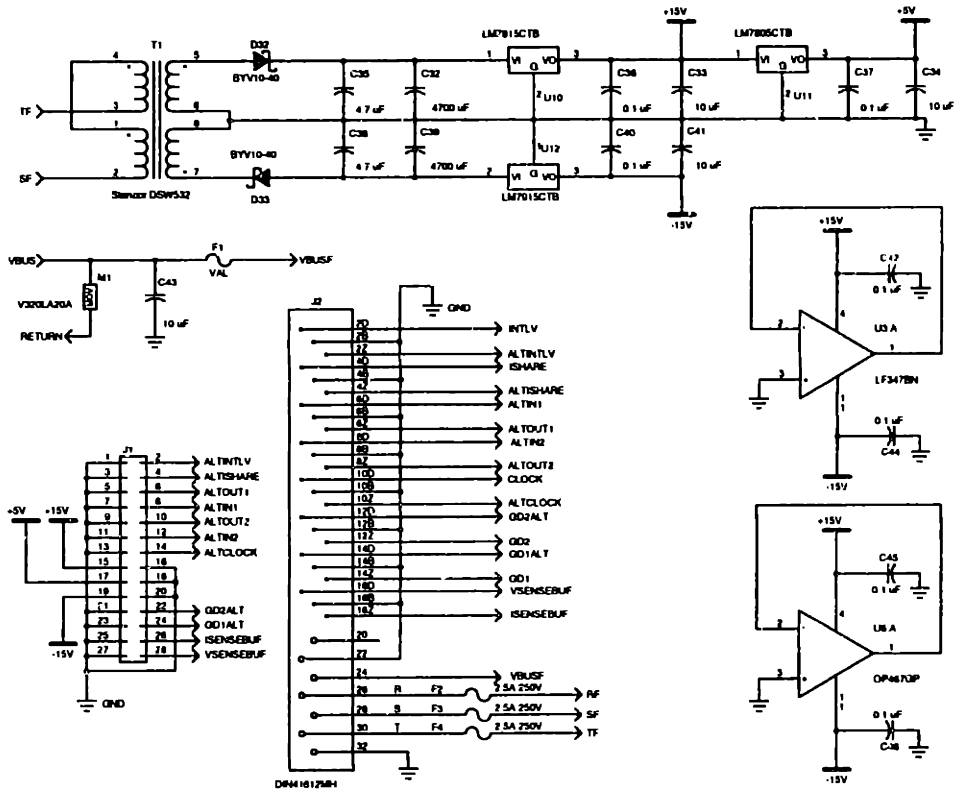

Figure C.4 Boost rectifier cell schematics, sheet 4.

Bill of Materials:

Quantity	Type	Value	Ref Designators
2	1N4746	VAL	D8,D23
1	AD633JN		U7
20	CAP	0.1 UF	C3,C4,C8,C9,C12,C13,C18, C19,C22,C25,C29,C30,C36, C37,C40,C42,C44,C45,C46, C47
5	CAP	0.68 UF	C21,C23,C24,C26,C27
4	CAP	1 NF	C11,C16,C20,C28
5	CAP	1.0 UF	C2,C7,C17,C31,C48
3	CAP	4.7 UF	C15,C35,C38
2	CAP	6.8 UF	C1,C6
2	CAP	10 NF 600 V MICA	C5,C10
4	CAP	10 UF	C33,C34,C41,C43
1	CAP	10UF	C14
2	CAP	2200 UF	C32,C39
1	DIN41612MH	VAL	J2
4	DIODE	1N4148	D2,D9,D16,D22
4	DIODE	HFA08TB60	D1,D14,D15,D28
3	FUSE	3.0A 250V	F2,F3,F4
1	FUSE		F1
1	HEADER2X14		J1
6	IND	40.4 UH	L1,L2,L3,L4,L5,L6
2	IR2125		U1,U2
2	JUMPER3		JP1,JP2,JP3
2	KM100 Heat Sink		HS1,HS2
1	LED		DN1
1	LF347BN		U3

Quantity	Type	Value	Ref Designators
1	LM7805CTB		U11
1	LM7815CTB		U10
1	LM7915CTB		U12
2	MOSFETN	IRF840G	Q1,Q2
1	MOSFETNCHAN	VN0300	Q3
1	MOV	V320LA20A	M1
16	MUR160		D3,D4,D5,D6,D7,D11,D12, D13,D17,D18,D19,D20,D21, D25,D26,D27
1	OP467GP		U6
1	POT	1K	R52
1	POT	20K	R46
1	RES	0.12 OHM 1W 1%	R9
1	RES	1 KOHM	R13,R49
1	RES	2.7K	R51
1	RES	3.01K 1%	R18
2	RES	5.1K	R44,R48
5	RES	10K	R7,R8,R22,R25,R45
2	RES	10K 1%	R14,R17
1	RES	10M	R23
2	RES	10R	R2,R5
1	RES	12K 1%	R21
1	RES	18.2K 1%	R15
8	RES	24.9K 1%	R26,R27,R35,R36,R37,R38, R42,R43
3	RES	27K	R24,R34,R40
2	RES	47R	R3,R6
1	RES	56.2K 1%	R20
1	RES	75K 1%	R19
3	RES	90.9K	R28,R30,R31
5	RES	100R 1%	R29,R32,R33,R39,R41
1	RES	180K 2W	R12
2	RES	240K	R1,R4
1	RES	330K 1%	R50
1	RES	390R	R10
1	RES	470R	R47
1	RES	560R	R11
1	RES	909R 1%	R16
2	SCHOTTKYDIODE	BYV10-40	D32,D33
5	SCHOTTKYDIODE	MBR0520LT1	D10,D24,D29,D30,D31
1	UC3705N		U9
1	UC3825		U5
1	UC3907N		U4
1	XFMR_DSW532	STANCOR DSW532	T1
1	XR2206		U8

Parts List

Ref Designator	Pattern	Type	Value
C1	CAP.(TANT.)	CAP	6.8 UF
C2	CAP.(TANT.)	CAP	1.0 UF
C3	CAP.(TANT.)	CAP	0.1 UF
C4	CAP.(TANT.)	CAP	0.1 UF
C5	CAP.(10NFMICA)	CAP	10 NF 600 V MICA
C6	CAP.(TANT.)	CAP	6.8 UF
C7	CAP.(TANT.)	CAP	1.0 UF
C8	CAP.(TANT.)	CAP	0.1 UF
C9	CAP.(TANT.)	CAP	0.1 UF
C10	CAP.(10NFMICA)	CAP	10 NF 600 V MICA
C11	CAP.(1NFFILM)	CAP	1 NF
C12	CAP.(CERAM.)	CAP	0.1 UF
C13	CAP.(CERAM.)	CAP	0.1 UF
C14	CAP.(TANT.)	CAP	10UF
C15	CAP.(TANT.)	CAP	4.7 UF
C16	CAP.(1NFFILM)	CAP	1 NF
C17	CAP.(TANT.)	CAP	1 UF
C18	CAP.(CERAM.)	CAP	0.1 UF
C19	CAP.(CERAM.)	CAP	0.1 UF
C20	CAP.(1NFFILM)	CAP	1 NF
C21	CAP.(TANT.)	CAP	0.68 UF
C22	CAP.(CERAM.)	CAP	0.1 UF
C23	CAP.(TANT.)	CAP	0.68 UF
C24	CAP.(TANT.)	CAP	0.68 UF
C25	CAP.(CERAM.)	CAP	0.1 UF
C26	CAP.(TANT.)	CAP	0.68 UF
C27	CAP.(TANT.)	CAP	0.68 UF
C28	CAP.(1NFFILM)	CAP	1 NF
C29	CAP.(CERAM.)	CAP	0.1 UF
C30	CAP.(CERAM.)	CAP	0.1 UF
C31	CAP.(TANT.)	CAP	1.0 UF
C32	CAP.(ELECT.)	CAP	4700 UF
C33	CAP.(TANT.)	CAP	10 UF
C34	CAP.(TANT.)	CAP	10 UF
C35	CAP.(TANT.)	CAP	4.7 UF
C36	CAP.(CERAM.)	CAP	0.1 UF
C37	CAP.(CERAM.)	CAP	0.1 UF
C38	CAP.(TANT.)	CAP	4.7 UF
C39	CAP.(ELECT.)	CAP	2200 UF
C40	CAP.(CERAM.)	CAP	0.1 UF
C41	CAP.(TANT.)	CAP	10 UF
C42	CAP.(CERAM.)	CAP	0.1 UF
C43	CAP.(935C4W10K)	CAP	10 UF 400 V
C44	CAP.(CERAM.)	CAP	0.1 UF
C45	CAP.(CERAM.)	CAP	0.1 UF
C46	CAP.(CERAM.)	CAP	0.1 UF
C47	CAP.(CERAM.)	CAP	0.1 UF
C48	CAP.(TANT.)	CAP	1.0 UF
D1	DIODEHFA08TB60	DIODE	HFA08TB60
D2	DIODE(DO-35)	DIODE	1N4148
D3	DIODE(MUR160TR)	MUR160	
D4	DIODE(MUR160TR)	MUR160	
D5	DIODE(MUR160TR)	MUR160	
D6	DIODE(MUR160TR)	MUR160	
D7	DIODE(MUR160TR)	MUR160	
D8	DIODE(DO-41)	1N4746	
D9	DIODE(DO-35)	DIODE	1N4148
D10	DIODE(SOD123)	SCHOTTKYDIODE	MBR0520LT1
D11	DIODE(MUR160TR)	MUR160	
D12	DIODE(MUR160TR)	MUR160	
D13	DIODE(MUR160TR)	MUR160	
D14	DIODEHFA08TB60	DIODE	HFA08TB60
D15	DIODEHFA08TB60	DIODE	HFA08TB60
D16	DIODE(DO-35)	DIODE	1N4148
D17	DIODE(MUR160TR)	MUR160	
D18	DIODE(MUR160TR)	MUR160	
D19	DIODE(MUR160TR)	MUR160	
D20	DIODE(MUR160TR)	MUR160	
D21	DIODE(MUR160TR)	MUR160	
D22	DIODE(DO-35)	DIODE	1N4148
D23	DIODE(DO-41)	1N4746	
D24	DIODE(SOD123)	SCHOTTKYDIODE	MBR0520LT1

Ref Designator	Pattern	Type	Value
D25	DIODE(MUR160TR)	MUR160	
D26	DIODE(MUR160TR)	MUR160	
D27	DIODE(MUR160TR)	MUR160	
D28	DIODEHFA08TB60	DIODE	HFA08TB60
D29	DIODE(SOD123)	SCHOTTKYDIODE	MBR0520LT1
D30	DIODE(SOD123)	SCHOTTKYDIODE	MBR0520LT1
D31	DIODE(SOD123)	SCHOTTKYDIODE	MBR0520LT1
D32	DIODE(DO-41)	SCHOTTKYDIODE	BYV10-40
D33	DIODE(DO-41)	SCHOTTKYDIODE	BYV10-40
DN1	LED100	LED	
F1	FUSE(13/32X3/2)	FUSE	
F2	FUSE(PC-TRON)	FUSE	3.0A 250V
F3	FUSE(PC-TRON)	FUSE	3.0A 250V
F4	FUSE(PC-TRON)	FUSE	3.0A 250V
HS1	HEATSINKKM100-1	KM100 Heat Sink	
HS2	HEATSINKKM100-1	KM100 Heat Sink	
J1	HEADER(2X14)	HEADER2X14	
J2	DIN41612MH	DIN41612MH	
JP1	JMP3	JUMPER3	
JP2	JMP3	JUMPER3	
JP3	JMP3	JUMPER3	
L1	INDUCTOR	IND	40.4 UH
L2	INDUCTOR	IND	40.4 UH
L3	INDUCTOR	IND	40.4 UH
L4	INDUCTOR	IND	40.4 UH
L5	INDUCTOR	IND	40.4 UH
L6	INDUCTOR	IND	40.4 UH
M1	MOV(V320LA20A)	MOV	V320LA20A
Q1	IRF840G	MOSFETN	IRF840G
Q2	IRF840G	MOSFETN	IRF840G
Q3	VN0300(TO92SGD)	MOSFETNCHAN	VN0300
R1	RES400	RES	240K
R2	RES400	RES	10R
R3	RES400	RES	47R
R4	RES400	RES	240K
R5	RES400	RES	10R
R6	RES400	RES	47R
R7	RES350	RES	10K
R8	RES350	RES	10K
R9	RSENSE	RES	0.12 OHM 1W 1%
R10	RES350	RES	390R
R11	RES350	RES	560R
R12	RESISTOR(2W)	RES	180K 2W
R13	RES350	RES	1 KOHM
R14	RES350	RES	10K 1%
R15	RES350	RES	18.2K 1%
R16	RES350	RES	909R 1%
R17	RES350	RES	10K 1%
R18	RES350	RES	3.01K 1%
R19	RES350	RES	75K 1%
R20	RES350	RES	56.2K 1%
R21	RES350	RES	12K 1%
R22	RES350	RES	10K
R23	RES350	RES	10M
R24	RES350	RES	27K
R25	RES350	RES	10K
R26	RES350	RES	24.9K 1%
R27	RES350	RES	24.9K 1%
R28	RES350	RES	90.9K
R29	RES350	RES	100R 1%
R30	RES350	RES	90.9K
R31	RES350	RES	90.9K
R32	RES350	RES	100R 1%
R33	RES350	RES	100R 1%
R34	RES350	RES	27K
R35	RES350	RES	24.9K 1%
R36	RES350	RES	24.9K 1%
R37	RES350	RES	24.9K 1%
R38	RES350	RES	24.9K 1%
R39	RES350	RES	100R 1%
R40	RES350	RES	27K
R41	RES350	RES	100R 1%
R42	RES350	RES	24.9K 1%
R43	RES350	RES	24.9K 1%
R44	RES350	RES	5.1K

Ref Designator	Pattern	Type	Value
R45	RES350	RES	10K
R46	POT.(TOPKNOB)	POT	20K
R47	RES350	RES	470R
R48	RES350	RES	5.1K
R49	RES350	RES	1K
R50	RES350	RES	330K 1%
R51	RES350	RES	2.7K
R52	POT.(TOPKNOB)	POT	1K
T1	XFORMERDSW-532	XFMR_DSW532	STANCOR DSW532
U1	DIP8	IR2125	
U2	DIP8	IR2125	
U3	DIP14	LF347BN	
U4	DIP16	UC3907N	
U5	DIP16	UC3825	
U6	DIP14	OP467GP	
U7	DIP8	AD633JN	
U8	DIP16	XR2206	
U9	DIP8	UC3705N	
U10	LM78XX/LM79XX	LM7815CTB	
U11	LM78XX/LM79XX	LM7805CTB	
U12	LM78XX/LM79XX	LM7915CTB	

Copies of the pc board artwork (at a reduced scale) are provided here. These layers include the silk screen, the top layer, the ground plane, the middle layer, the bottom layer, the solder mask, and the pad master. Note that by convention the ground plane is plotted in inverse.

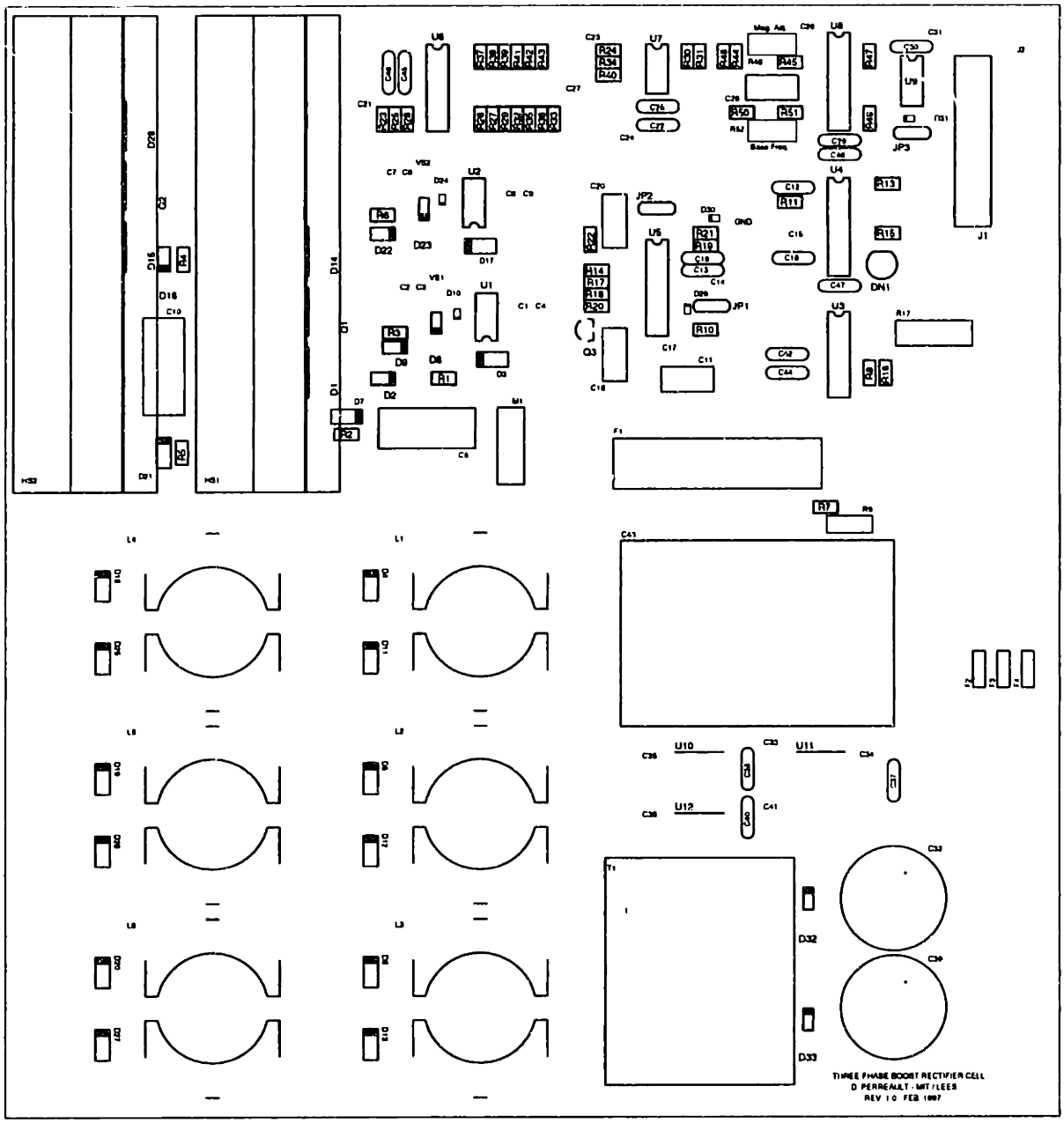

Figure C.5 Silkscreen plot.

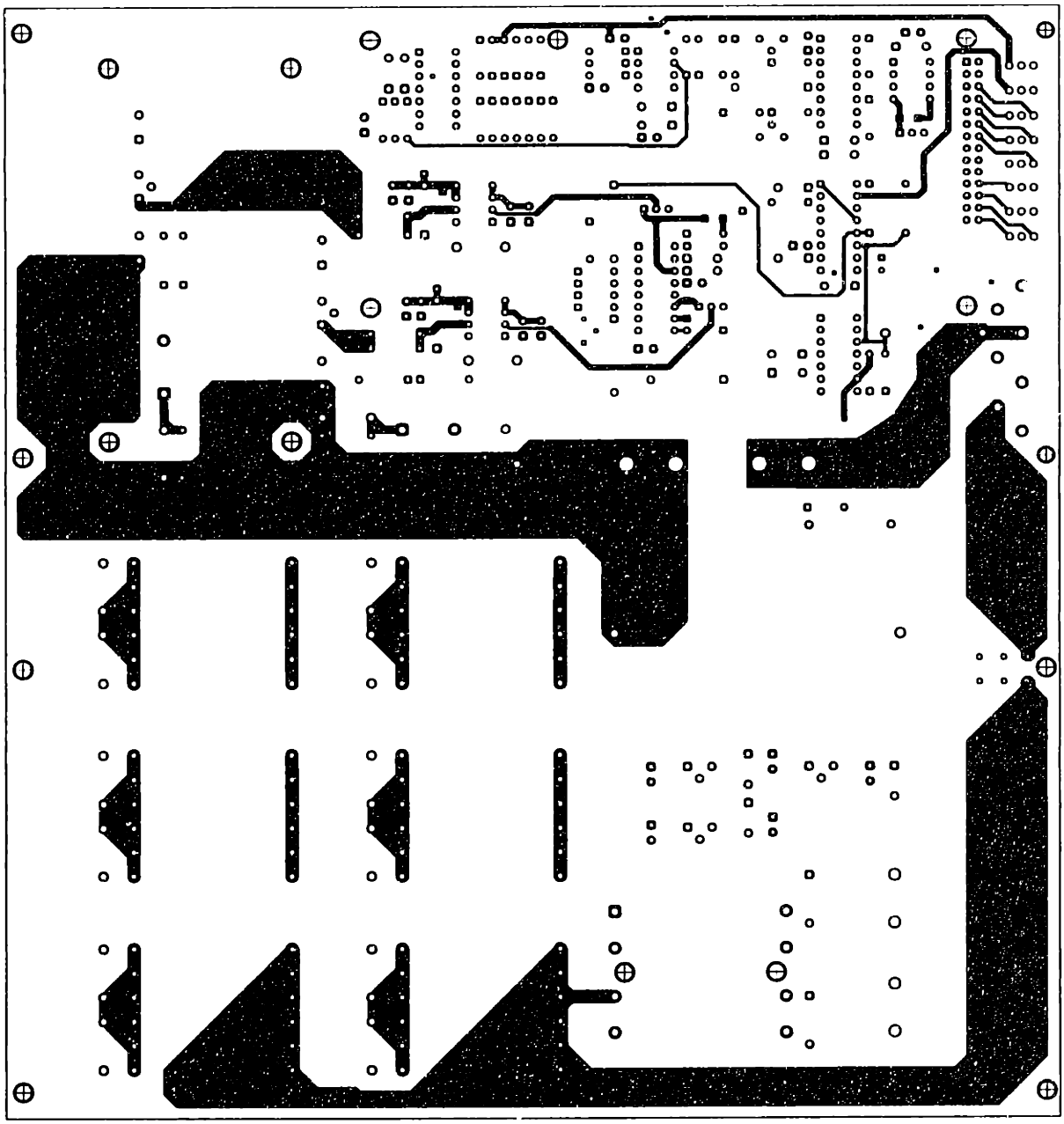

Figure C.6 Top layer plot.

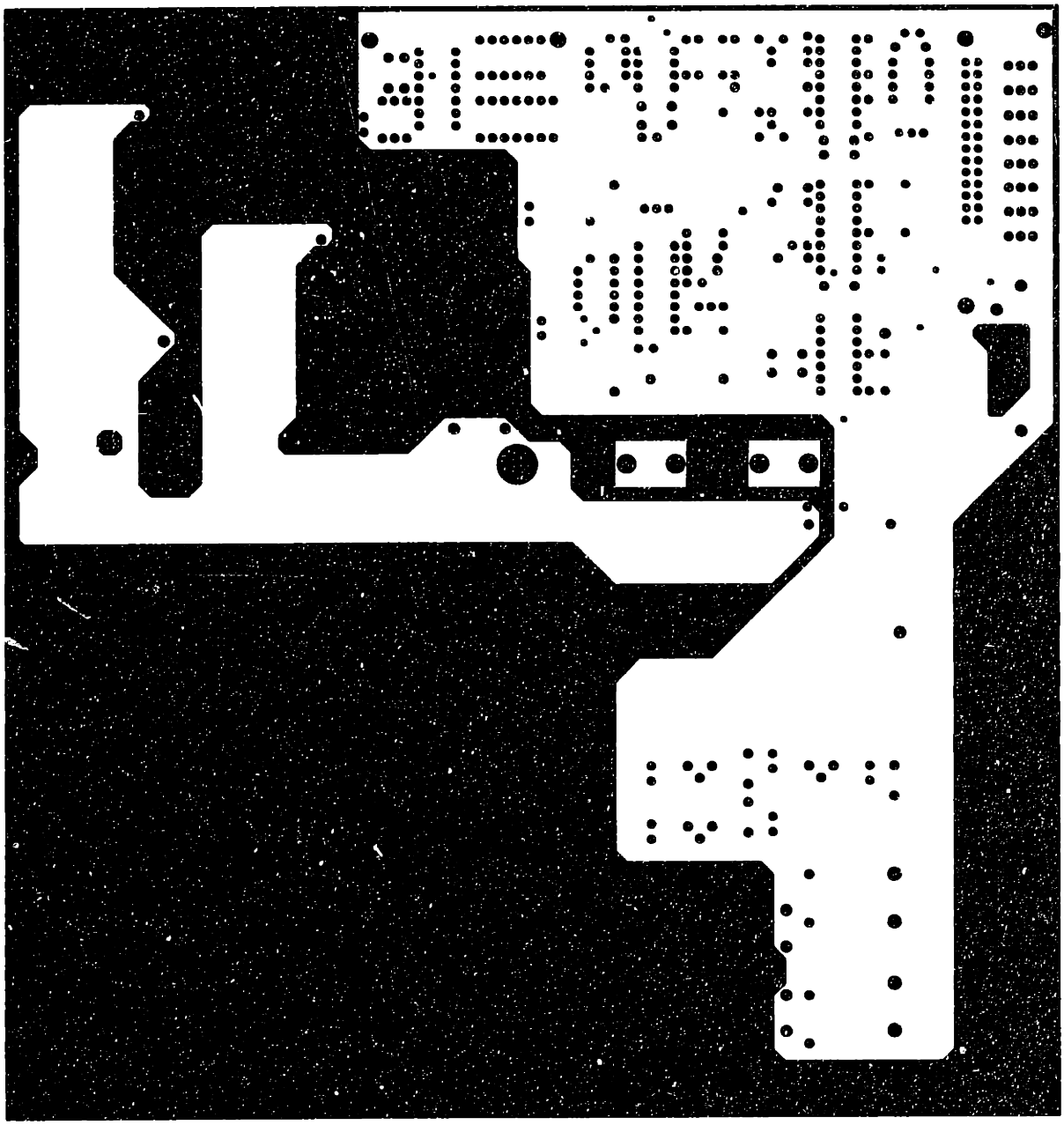

Figure C.7 Ground plane plot (in reverse).

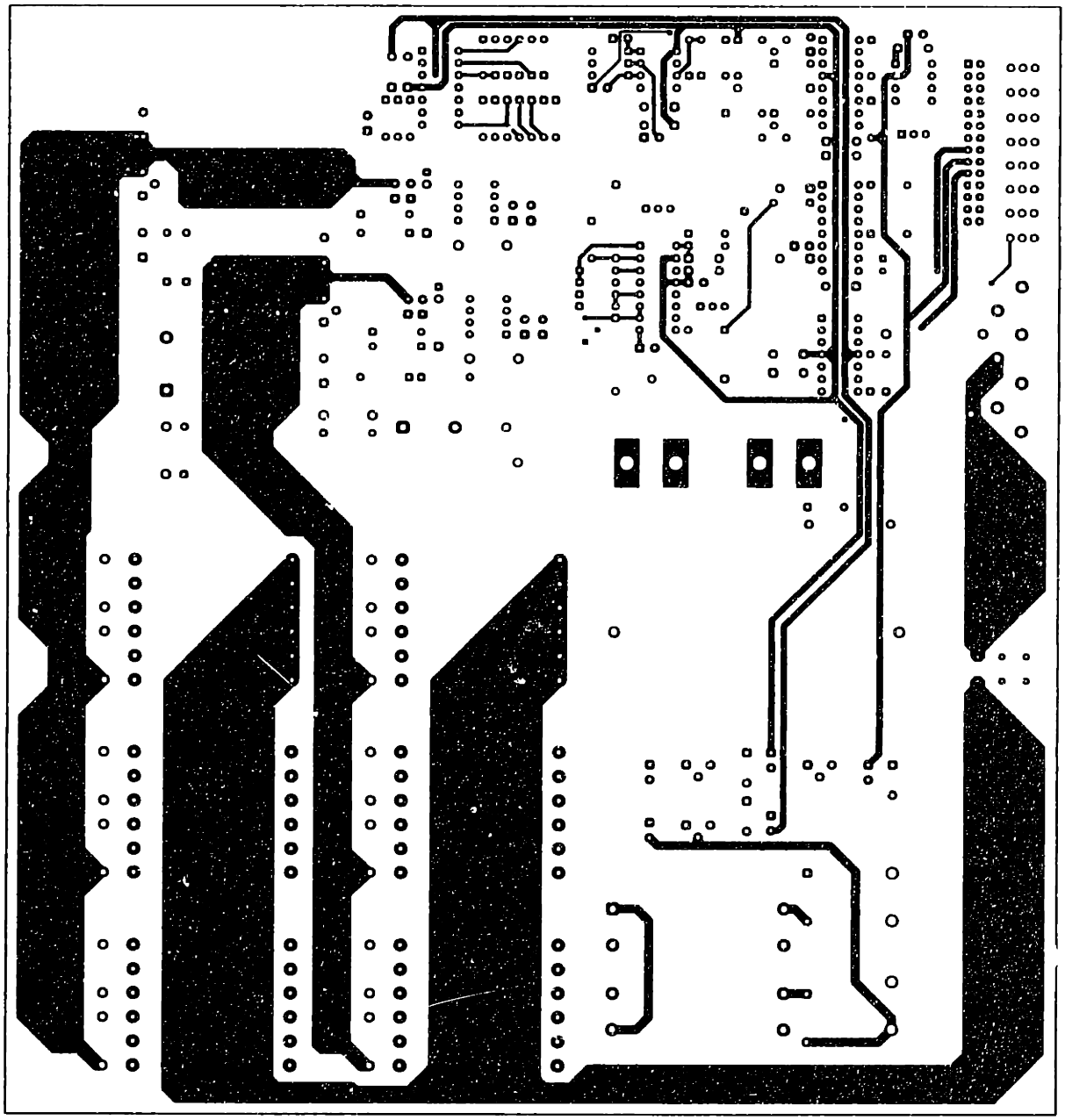

Figure C.8 Middle layer plot.

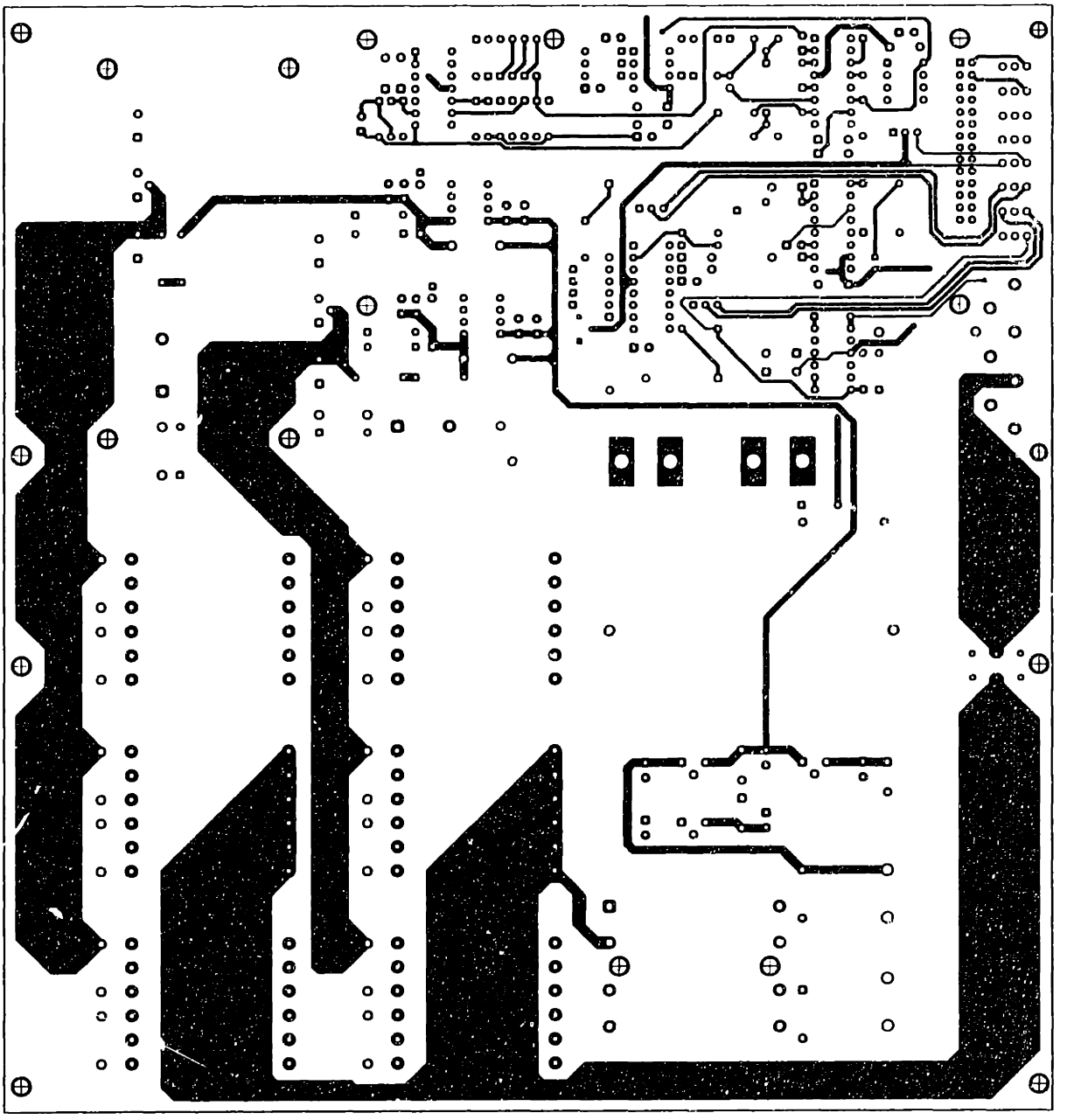

Figure C.9 Bottom layer plot.

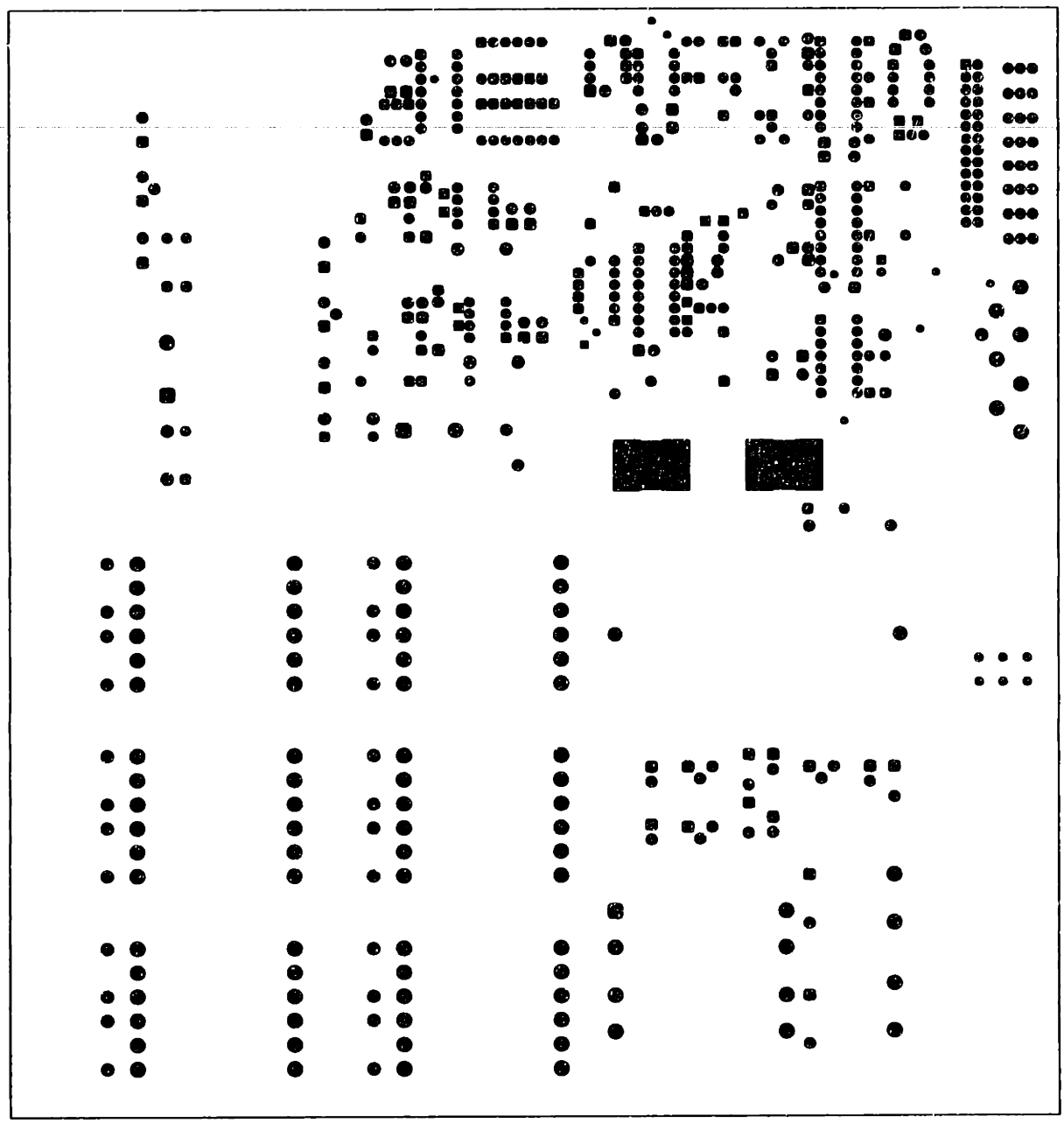

Figure C.10 Solder mask plot.

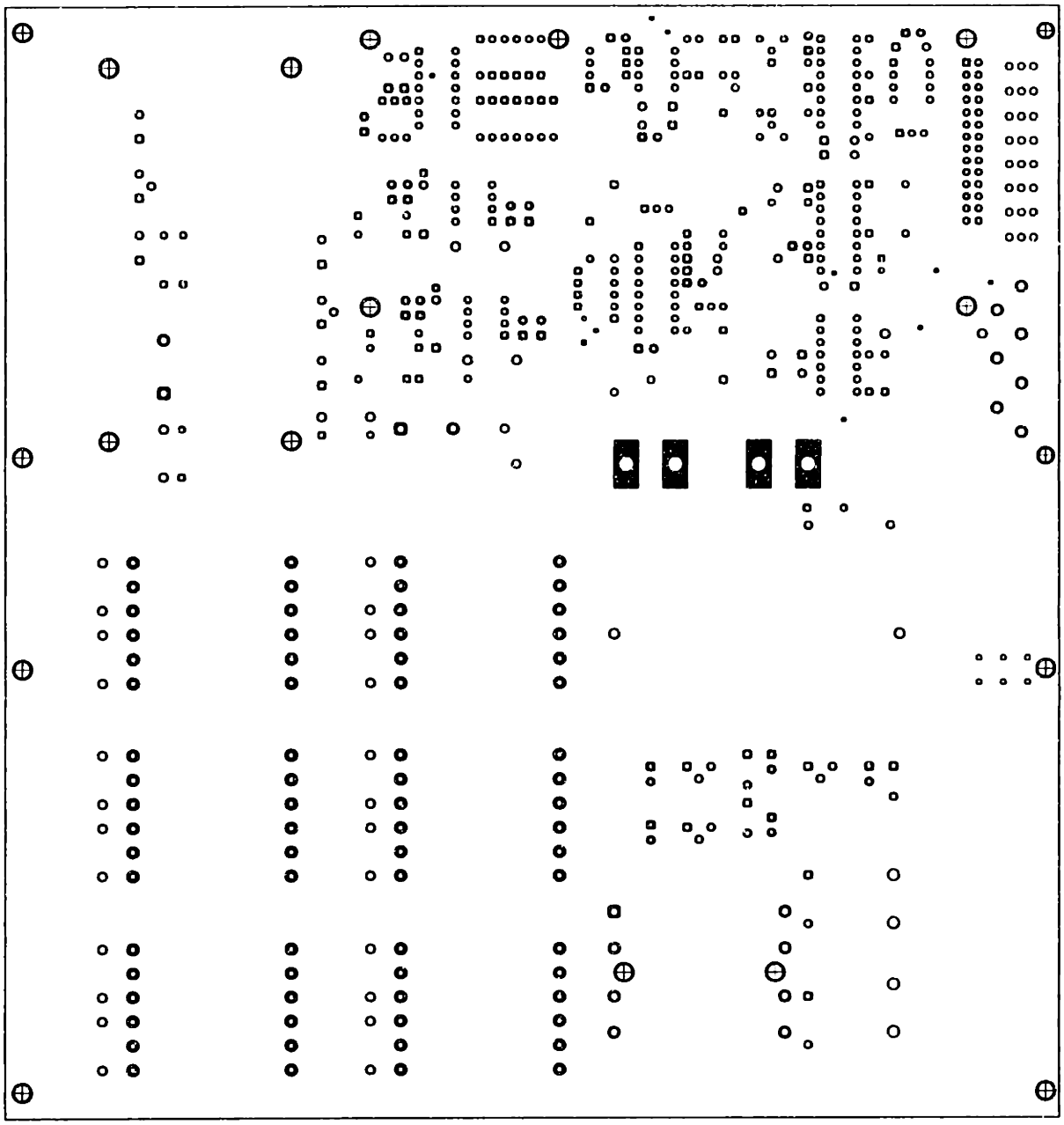

Figure C.11 Pad master plot.